

JZ4770

Mobile Application Processor

Data Sheet

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1 Overview

JZ4770 is a mobile application processor targeting for multimedia rich and mobile devices like smartphone, tablet computer, mobile digital TV, and GPS. This SOC introduces a kind of innovative architecture to fulfill both high performance mobile computing and high quality video decoding requirements addressed by mobile multimedia devices. JZ4770 provides high-speed CPU computing power, good 3D experience and fluent 1080p video replay.

The CPU (Central Processing Unit) core, equipped with 16kB instruction and 16kB data level 1 cache, and 256kB level 2 cache, operating at 1000MHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst processor engine. XBurst is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is powered with another XBurst processor engine. The SIMD instruction set implemented by XBurst engine, in together with the on chip video accelerating engine and post processing unit, delivers high video performance. The maximum resolution of 1080p in the formats of H.264, VC-1, MPEG-2, MPEC-4, RealVideo and VP8 are supported in decoding, the maximum resolution of 720p in the format of H.264 are supported in encoding.

The GPU (Graph Processing Unit) core supports numerous 2D/3D graphics applications. It delivers hardware acceleration for 2D and 3D graphics displays, and supports screen sizes range from the smallest cell phones to full HD 1080p displays. It supports the standard APIs such as OpenGL ES2.0 and 1.1, and Open VG. The OS of Android, Linux and Windows are supported. The GPU provides high performance, high quality graphics and low power consumption.

The memory interface supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or 4-bit/8-bit/12-bit/16-bit/24-bit ECC MLC/TLC NAND flash memory for cost sensitive applications. It provides the interface to DDR2, DDR and LPDDR memory chips with lower power consumption.

On-chip modules such as audio CODEC, multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. GPS baseband is embedded. TV encoder unit 10-bits DAC provide composite TV signal output in PAL or NTSC format. The LCD controller support up to 1920x1080 output, LVDS as well as plain RGB output which support external HDMI transmitter. The EPD controller supports mainstream vendors' EPD panels in market, up to 5-bit grayscale and 8-zone concurrent updating. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. The TS (Transport stream) interface provides enough bandwidth to connect to an external mobile digital TV demodulator. Other peripherals such as USB OTG and USB 1.1 host, Ethernet MAC with MII and RMII interface, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

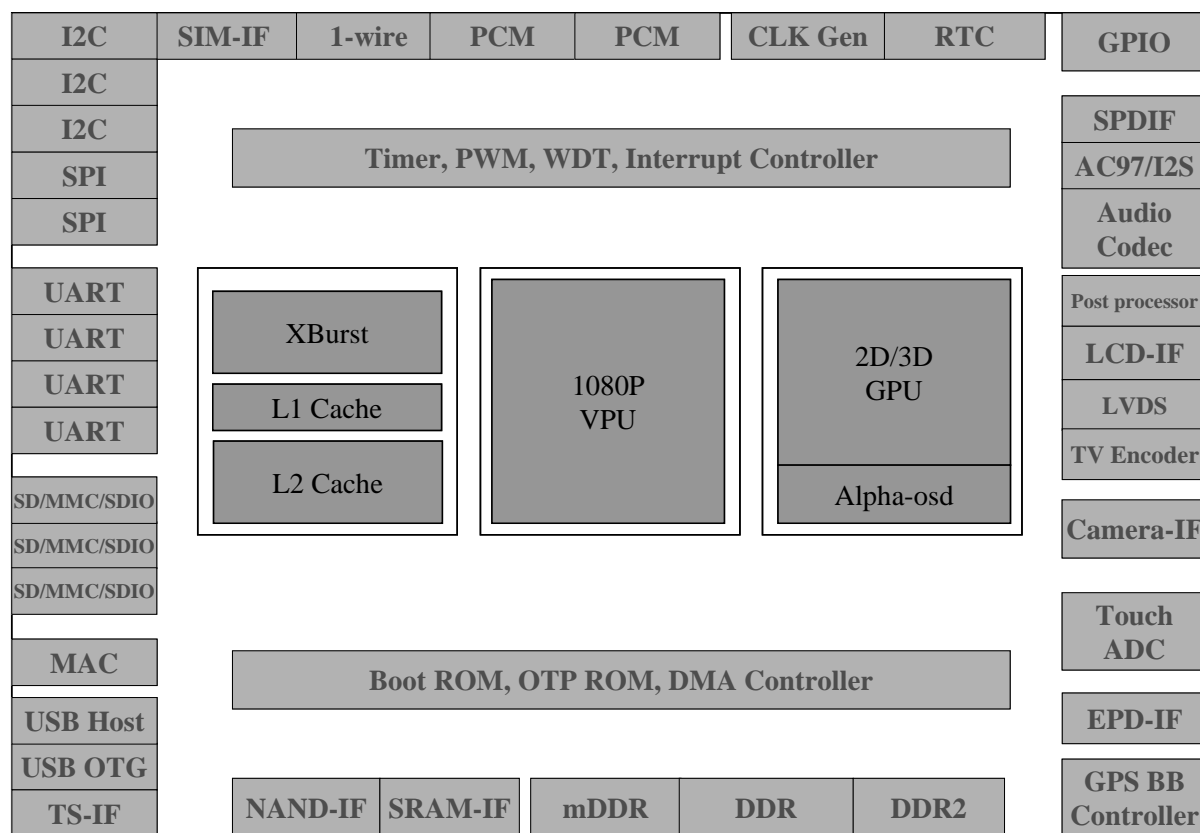


Figure 1-1 JZ4770 Diagram

1.2 Features

1.2.1 CPU Core

- XBurst CPU
 - XBurst[®] RISC instruction set
 - XBurst[®] SIMD instruction set
 - XBurst[®] FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
 - XBurst[®] 8-stage pipeline micro-architecture up to 1000MHz
- MMU
 - 32-entry joint-TLB
 - 4 entry Instruction TLB
 - 4 entry data TLB
- L1 Cache
 - 16kB instruction cache
 - 16kB data cache
- Hardware debug support
- 16kB tight coupled memory
- L2 Cache
 - 256kB unify cache

1.2.2 VPU Core

- XBurst CPU for video processing
 - XBurst[®] RISC instruction set
 - XBurst[®] SIMD instruction set
 - XBurst[®] 8-stage pipeline micro-architecture up to 500MHz
- Video acceleration engine
 - Motion compensation
 - Motion estimation
 - De-block
 - DCT/IDCT for 4x4 block
 - Parser
- 48kB tight coupled memory
- 28kB scratch RAM

1.2.3 GPU Core

- 2D graphic
 - Bit BLT and stretch BLT
 - Line/Rectangle
 - ROP2, ROP3, ROP4/Alpha blending/scaling/Filter
 - Rotation (90/180/270 degree)/Mirror/Transparency/Rendering

- Pixel rate up to 200M pix/s
- 3D graphic
 - OpenGL ES2.0 compliance, including extensions
 - OpenGL ES1.1/OpenVG 1.1 compliance
 - DirectFB/GDI/DirectDraw compliance
 - Geometry rate up to 20M tri/s
 - Pixel rate up to 200M pix/s
- Alpha-osd
 - Support ARGB8888, RGB565, RGB555
 - Each layer has an alpha value for all pixels
 - Up to 800*480
 - Software can change overlay orders
 - The level of overlay can be set by software
 - Software must make sure the address of source and destination are 64-word aligned
 - Support 64-burst in AHB bus
 - In RGB656 & RGB555mode, software must make sure each line aligned in word

1.2.4 Memory Sub-systems

- DDR Controller
 - Support DDR2, DDR, mobile DDR (LPDDR) memory
 - Support x16 and x32 external DDR data width
 - Support clock frequency ratio – (BUS clock) : (DDR clock) = 2:1
 - Support clock frequency ratio – (BUS clock) : (DDR clock) = 1:1
 - Support clock-stop mode
 - Support auto-refresh and self-refresh
 - Support power-down mode and deep-power-down mode
 - Programmable DDR timing parameters
 - Programmable DDR row and column address width
- Static memory interface
 - Direct interface to SRAM, ROM, Burst ROM, and NOR Flash
 - Six chip-select pins for static memory, each can be configured separately
 - Support 8 or 16 bits data width
 - 6 bits address
- NAND flash interface
 - Support 4-bit/8-bit/12-bit/16-bit/24-bit MLC/TLC NAND as well as SLC NAND
 - Support all 8-bit/16-bit NAND Flash devices regardless of density and organization
 - Support automatic boot up from NAND Flash devices
- BCH Controller
 - Support 4-bit/8-bit/12-bit/16-bit/20-bit/24-bit ECC encoding and decoding for NAND
- Direct memory access controllers
 - BDMA controller
 - 3 independent DMA channels

- Support data transfer between normal memory (NAND, SRAM, etc.) / BCH and system memory (DDR)
- General purpose DMA
 - 12 independent DMA channels
 - Support data transfer between On-chip Peripherals (e.g. I2C, MSC, etc.) and system memory (DDR)
 - APB bus bridge
- Common features
 - Descriptor supported
 - Transfer data units: byte, 2-byte (half word), 4-byte (word), 16-byte, 32-byte or 64-byte
 - Transfer number of data unit: 1 ~ 224
 - Independent source and target port width: 8-bit, 16-bit, 32-bit
- The XBurst processor system supports little endian only

1.2.5 AHB Bus Arbiter

- Provide a fair chance for each AHB master to possess the AHB bus
- Fulfill the back-to-back feature of AHB protocol
- Automatic privilege for some masters and programmable privilege for others. Round-robin possession for masters in the same privilege

1.2.6 System Devices

- Clock generation and power management
 - On-chip oscillator circuit for an 32768Hz clock and an 12MHz clock
 - On-chip phase-locked loops (PLL) with programmable multiple-ratio. Internal counter are used to ensure PLL stabilize time
 - PLL on/off is programmable by software
 - ICLK, PCLK, HCLK, HHCLK, MCLK and LCLK frequency can be changed separately for software by setting division ratio
 - Supports six low-power modes and function: NORMAL mode; DOZE mode; IDLE mode; SLEEP mode; HIBERNATE mode; and MODULE-STOP function
 - Support module power-down
- RTC (Real Time Clock)
 - 32-bit second counter
 - 1Hz from 32768hz
 - Alarm interrupt
 - Independent power
 - A 32-bits scratch register used to indicate whether power down happens for RTC power
- Interrupt controller
 - Total 32 maskable interrupt sources from on-chip peripherals and external request through GPIO ports

- Interrupt source and pending registers for software handling
 - Unmasked interrupts can wake up the chip in sleep or standby mode
- Timer and counter unit with PWM output and/or input edge counter
 - Provide eight separate channels, six of them have input signal transition edge counter
 - 16-bit A counter and 16-bit B counter with auto-reload function every channel
 - Support interrupt generation when the A counter underflows
 - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
 - Every channel has PWM output
- OS timer
 - One channel
 - 32-bit counter and 32-bit compare register
 - Support interrupt generation when the counter matches the compare register
 - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Watchdog timer
 - 16-bit counter in RTC clock with 1, 4, 16, 64, 256 and 1024 clock dividing selected
 - Generate power-on reset

1.2.7 Audio/Display/UI Interfaces

- LCD controller
 - Single-panel display in active mode, and single- or dual-panel displays in passive mode
 - 2, 4, 16 greyscales and up to 4096 colors in STN mode
 - 2, 4, 16, 256, 4K, 32K, 64K, 256K and 16M colors in TFT mode
 - 24-bit data bus
 - Support 1,2,4,8 pins STN panel, 16bit, 18bit and 24bit TFT and 8bit I/F TFT
 - Display size up to 1920x1080 pixels
 - 256x16 bits internal palette RAM
 - Support ITU601/656 data format
 - Support smart LCD (SRAM-like interface LCD module)
 - Support delta RGB
 - One single color background and two foreground OSD
 - Compressed frame supported
 - Support LVDS signal output
- TV encoder
 - Support NTSC or PAL
 - Support CVBS signal
 - 10 bits DAC
- EPD controller
 - Supports Electro-Phoretic Display and compatible devices
 - Supports different size of display panel
 - Supports different width of pixel data

- Supports internal DMA operation and register operation
- Image post processor
 - Video frame resize
 - Color space conversion: 420/444/422 YUV to RGB convert
 - Bi-cubic algorithm supported
 - Video enhancement
- Camera interface module
 - Input image size up to 4096×4096 pixels
 - Supports CCIR656 data format
 - YCbCr 4:2:2 and YCbCr 4:4:4 data format
 - Raw data input
 - 64×32 image data receive FIFO with DMA support
- On-chip audio CODEC
 - 24-bit DAC, SNR: 95dB
 - 24-bit ADC, SNR: 90dB
 - Sample rate: 8/9.6/11.025/12/16/22.05/24/32/44.1/48/96kHz
 - L/R channels line input
 - 2 MICs input, differential or single-ended
 - L/R channels headphone output amplifier support up to 16ohm load
 - Capacitor-coupled
 - Mono differential line out
 - Mono 450mW amplifier for speaker out for 8ohm load
- AC97/I2S/SPDIF controller
 - Supports 8, 16, 18, 20 and 24 bit for sample for AC-link and I2S/MSB-Justified format
 - Support 2/4/6/8 channels data out for I2S
 - Support compress data format for SPDIF
 - DMA transfer mode support
 - Support variable sample rate mode for AC-link format
 - Power down mode and two wake-up mode support for AC-link format
 - Programmable Interrupt function support
 - Support the on-chip CODEC
 - Support off-chip CODEC
 - Support off-chip HDMI transmitter audio
- Two PCM interfaces
 - Data starts with the frame PCMSYN or one PCMCLK later
 - Support three modes of operation for PCM: Short frame sync mode, Long frame sync mode, Multi-slot mode
 - Data is transferred and received with the MSB first
 - Support master mode and slave mode
 - The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
 - The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK.
 - 8/16 bit sample data sizes supported

- DMA transfer mode supported
- Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction
- SADC
 - 12-bit, 1Msps/200ksps
 - XP/XN, YP/YN inputs for touch screen
 - Battery voltage inputs for internal/external resistor divider respectively
 - 2 generic input channels
 - 5mW@1Msps, 2.2mW@200ksps

1.2.8 On-chip Peripherals

- General-Purpose I/O ports
 - Total GPIO pin number is ???, where ? are dedicated and all others are shared
 - Each pin can be configured as general-purpose input or output or multiplexed with internal chip functions
 - Each pin can act as a interrupt source and has configurable rising/falling edge or high/low level detect manner, and can be masked independently
 - Each pin can be configured as open-drain when output
 - Each pin can be configured as internal resistor pull-up/down on or off
- Three I2C bus interfaces
 - Only supports single master mode
 - Supports I2C standard-mode and F/S-mode up to 400 kHz
 - Double-buffered for receiver and transmitter
 - Supports general call address and START byte format after START condition
- Two Synchronous serial interfaces (SSI0, SSI1)
 - Up to 50MHz speed
 - Supports three formats: TI's SSP, National Microwire, and Motorola's SPI
 - Configurable 2 - 17 (or multiples of them) bits data transfer
 - Full-duplex/transmit-only/receive-only operation
 - Supports normal transfer mode or Interval transfer mode
 - Programmable transfer order: MSB first or LSB first
 - 17-bit width, 128-level deep transmit-FIFO and receive-FIFO
 - Programmable divider/prescaler for SSI clock
 - Back-to-back character transmission/reception mode
- One-wire bus interface
 - Overdrive and regular speed
 - Master only
 - LSB first
 - Bit or byte operate modes
- USB 1.1 host interface
 - Open Host Controller Interface (OHCI)-compatible and USB Revision 1.1-compatible
 - Full speed and low speed

- Embedded USB 1.1 PHY
- USB 2.0 OTG interface
 - Compliant with USB protocol revision 2.0 OTG
 - High speed and full speed supported for device role
 - High speed, full speed and low speed supported for host role
 - Embedded USB OTG PHY
- Ethernet MAC interface
 - Compliant with IEEE802.3
 - 10/100 Mbps data transfer rate with full and half duplex modes
 - MII/RMII interface to talk to an external PHY
- Three MMC/SD/SDIO controllers (MSC0, MSC1, MSC2)
 - Support automatic boot up from MSC0, which has 4-bit data bus
 - MSC1 with 4-bit data bus
 - Compliant with “The MultiMediaCard System Specification version 4.2”
 - Compliant with “SD Memory Card Specification version 2.0” and “SDIO Card Specification version 1.0” with 1 command channel and 4 data channels
 - Up to 320 Mbps data rate in MSC0
 - Up to 320 Mbps data rate in MSC1
 - Supports up to 10 cards (including one SD card)
 - Maskable hardware interrupt for SD I/O interrupt, internal status, and FIFO status
- Four UARTs (UART0, UART1, UART2, UART3)
 - 5, 6, 7 or 8 data bit operation with 1 or 1.5 or 2 stop bits, programmable parity (even, odd, or none)
 - 32x8bit FIFO for transmit and 32x11bit FIFO for receive data
 - Interrupt support for transmit, receive (data ready or timeout), and line status
 - Supports DMA transfer mode
 - Provide complete serial port signal for modem control functions
 - Support slow infrared asynchronous interface (IrDA)
 - IrDA function up to 115200bps baudrate
 - UART function up to 3.7Mbps baudrate
 - Hardware flow control
- SIM IF
 - Supports normal card and UIM card
 - 8-bit, 16-level receive-/transmit- FIFO
 - Supports asynchronous character (T=0) communication modes
 - Supports asynchronous block (T=1) communication modes
 - Supports setting of clock-rate conversion factor F (372, 512, 558, etc.), and bit-rate adjustment factor D (1, 2, 4, 8, 16, 32, 12, 20, etc.)
 - Supports extra guard time waiting
 - Auto-error detection in T=0 receive mode
 - Auto-character repeat in T=0 transmit mode
 - Transforms inverted format to regular format and vice versa
 - Support stop clock function in some power consuming sensitive applications

- Transport stream slave interface
 - 8-bit or 1-bit data bus selectable
 - Support PID filtering
- OTP Slave Interface
 - Total 256 bits. Lower 128bits are read-able and write-able, Higher 128bits are read only

1.2.9 Bootrom

- 8kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	65nm CMOS low power
Power supply voltage	General purpose I/O: 1.6~3.6V DDR I/O for mDDR: 1.8V± 0.2V DDR I/O for DDR: 2.5V± 0.2V DDR I/O for DDR2: 1.8V± 0.2V RTC I/O: 3.0V~3.6V EFUSE programming: 2.5V± 10% Analog power supply 1: 2.5V± 10% Analog power supply 2: 3.3V± 10% Core: 1.2 -0.1/+0.2 V
Package	BGA379 14mm x 14mm x 1.1mm, 0.65mm pitch
Operating frequency	1000MHz

2 Packaging and Pinout Information

2.1 Overview

JZ4770 processor is offered in 379-pin LFBGA package, which is 14mm x 14mm x 1.1mm outline, 21 x 21 matrix ball grid array and 0.65mm ball pitch, show in Figure 2-1. The JZ4770 pin to ball assignment is show in Figure 2-2.

The detailed pin description is listed in Table 2-1~Table 2-26.

2.2 Solder Process

JZ4770 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in [J-STD-020C](#).

2.3 Moisture Sensitivity Level

JZ4770 package moisture sensitivity is level 3.

2.4 JZ4770 Package

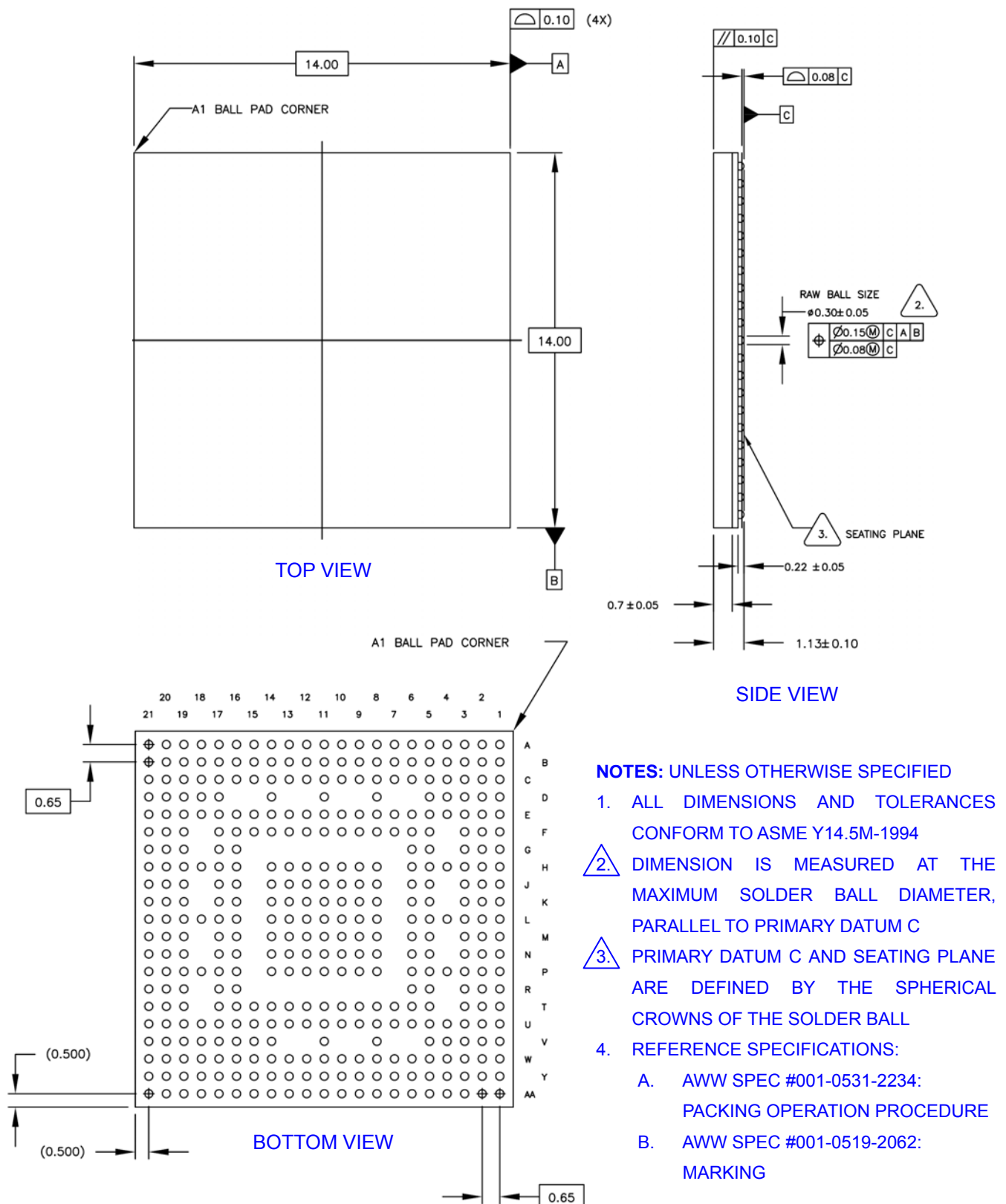


Figure 2-1 JZ4770 package outline drawing

JZ4770 Ball Assignment Ver1.0

BGA379, 14mm x 14mm x 1.2mm, 0.65pitch, top view

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	A	B	C	D	E	F	G	H	I	J	K	L	M	N	P	R	T	U	V	W	Y	AA																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						
SD1	SD3	SD6	SD11	RD_	SD5	SD7	SD12	SD13	SD14	SD15	SD16	SD17	SD18	SD19	SD20	SD21	SD22	SD23	SD24	SD25	SD26	SD27	SD28	SD29	SD30	SD31	SD32	SD33	SD34	SD35	SD36	SD37	SD38	SD39	SD40	SD41	SD42	SD43	SD44	SD45	SD46	SD47	SD48	SD49	SD50	SD51	SD52	SD53	SD54	SD55	SD56	SD57	SD58	SD59	SD60	SD61	SD62	SD63	SD64	SD65	SD66	SD67	SD68	SD69	SD70	SD71	SD72	SD73	SD74	SD75	SD76	SD77	SD78	SD79	SD80	SD81	SD82	SD83	SD84	SD85	SD86	SD87	SD88	SD89	SD90	SD91	SD92	SD93	SD94	SD95	SD96	SD97	SD98	SD99	SD100	SD101	SD102	SD103	SD104	SD105	SD106	SD107	SD108	SD109	SD110	SD111	SD112	SD113	SD114	SD115	SD116	SD117	SD118	SD119	SD120	SD121	SD122	SD123	SD124	SD125	SD126	SD127	SD128	SD129	SD130	SD131	SD132	SD133	SD134	SD135	SD136	SD137	SD138	SD139	SD140	SD141	SD142	SD143	SD144	SD145	SD146	SD147	SD148	SD149	SD150	SD151	SD152	SD153	SD154	SD155	SD156	SD157	SD158	SD159	SD160	SD161	SD162	SD163	SD164	SD165	SD166	SD167	SD168	SD169	SD170	SD171	SD172	SD173	SD174	SD175	SD176	SD177	SD178	SD179	SD180	SD181	SD182	SD183	SD184	SD185	SD186	SD187	SD188	SD189	SD190	SD191	SD192	SD193	SD194	SD195	SD196	SD197	SD198	SD199	SD200	SD201	SD202	SD203	SD204	SD205	SD206	SD207	SD208	SD209	SD210	SD211	SD212	SD213	SD214	SD215	SD216	SD217	SD218	SD219	SD220	SD221	SD222	SD223	SD224	SD225	SD226	SD227	SD228	SD229	SD230	SD231	SD232	SD233	SD234	SD235	SD236	SD237	SD238	SD239	SD240	SD241	SD242	SD243	SD244	SD245	SD246	SD247	SD248	SD249	SD250	SD251	SD252	SD253	SD254	SD255	SD256	SD257	SD258	SD259	SD260	SD261	SD262	SD263	SD264	SD265	SD266	SD267	SD268	SD269	SD270	SD271	SD272	SD273	SD274	SD275	SD276	SD277	SD278	SD279	SD280	SD281	SD282	SD283	SD284	SD285	SD286	SD287	SD288	SD289	SD290	SD291	SD292	SD293	SD294	SD295	SD296	SD297	SD298	SD299	SD300	SD301	SD302	SD303	SD304	SD305	SD306	SD307	SD308	SD309	SD310	SD311	SD312	SD313	SD314	SD315	SD316	SD317	SD318	SD319	SD320	SD321	SD322	SD323	SD324	SD325	SD326	SD327	SD328	SD329	SD330	SD331	SD332	SD333	SD334	SD335	SD336	SD337	SD338	SD339	SD340	SD341	SD342	SD343	SD344	SD345	SD346	SD347	SD348	SD349	SD350	SD351	SD352	SD353	SD354	SD355	SD356	SD357	SD358	SD359	SD360	SD361	SD362	SD363	SD364	SD365	SD366	SD367	SD368	SD369	SD370	SD371	SD372	SD373	SD374	SD375	SD376	SD377	SD378	SD379	SD380	SD381	SD382	SD383	SD384	SD385	SD386	SD387	SD388	SD389	SD390	SD391	SD392	SD393	SD394	SD395	SD396	SD397	SD398	SD399	SD400	SD401	SD402	SD403	SD404	SD405	SD406	SD407	SD408	SD409	SD410	SD411	SD412	SD413	SD414	SD415	SD416	SD417	SD418	SD419	SD420	SD421	SD422	SD423	SD424	SD425	SD426	SD427	SD428	SD429	SD430	SD431	SD432	SD433	SD434	SD435	SD436	SD437	SD438	SD439	SD440	SD441	SD442	SD443	SD444	SD445	SD446	SD447	SD448	SD449	SD450	SD451	SD452	SD453	SD454	SD455	SD456	SD457	SD458	SD459	SD460	SD461	SD462	SD463	SD464	SD465	SD466	SD467	SD468	SD469	SD470	SD471	SD472	SD473	SD474	SD475	SD476	SD477	SD478	SD479	SD480	SD481	SD482	SD483	SD484	SD485	SD486	SD487	SD488	SD489	SD490	SD491	SD492	SD493	SD494	SD495	SD496	SD497	SD498	SD499	SD500	SD501	SD502	SD503	SD504	SD505	SD506	SD507	SD508	SD509	SD510	SD511	SD512	SD513	SD514	SD515	SD516	SD517	SD518	SD519	SD520	SD521	SD522	SD523	SD524	SD525	SD526	SD527	SD528	SD529	SD530	SD531	SD532	SD533	SD534	SD535	SD536	SD537	SD538	SD539	SD540	SD541	SD542	SD543	SD544	SD545	SD546	SD547	SD548	SD549	SD550	SD551	SD552	SD553	SD554	SD555	SD556	SD557	SD558	SD559	SD560	SD561	SD562	SD563	SD564	SD565	SD566	SD567	SD568	SD569	SD570	SD571	SD572	SD573	SD574	SD575	SD576	SD577	SD578	SD579	SD580	SD581	SD582	SD583	SD584	SD585	SD586	SD587	SD588	SD589	SD590	SD591	SD592	SD593	SD594	SD595	SD596	SD597	SD598	SD599	SD600	SD601	SD602	SD603	SD604	SD605	SD606	SD607	SD608	SD609	SD610	SD611	SD612	SD613	SD614	SD615	SD616	SD617	SD618	SD619	SD620	SD621	SD622	SD623	SD624	SD625	SD626	SD627	SD628	SD629	SD630	SD631	SD632	SD633	SD634	SD635	SD636	SD637	SD638	SD639	SD640	SD641	SD642	SD643	SD644	SD645	SD646	SD647	SD648	SD649	SD650	SD651	SD652	SD653	SD654	SD655	SD656	SD657	SD658	SD659	SD660	SD661	SD662	SD663	SD664	SD665	SD666	SD667	SD668	SD669	SD670	SD671	SD672	SD673	SD674	SD675	SD676	SD677	SD678	SD679	SD680	SD681	SD682	SD683	SD684	SD685	SD686	SD687	SD688	SD689	SD690	SD691	SD692	SD693	SD694	SD695	SD696	SD697	SD698	SD699	SD700	SD701	SD702	SD703	SD704	SD705	SD706	SD707	SD708	SD709	SD710	SD711	SD712	SD713	SD714	SD715	SD716	SD717	SD718	SD719	SD720	SD721	SD722	SD723	SD724	SD725	SD726	SD727	SD728	SD729	SD730	SD731	SD732	SD733	SD734	SD735	SD736	SD737	SD738	SD739	SD740	SD741	SD742	SD743	SD744	SD745	SD746	SD747	SD748	SD749	SD750	SD751	SD752	SD753	SD754	SD755	SD756	SD757	SD758	SD759	SD760	SD761	SD762	SD763	SD764	SD765	SD766	SD767	SD768	SD769	SD770	SD771	SD772	SD773	SD774	SD775	SD776	SD777	SD778	SD779	SD780	SD781	SD782	SD783	SD784	SD785	SD786	SD787	SD788	SD789	SD790	SD791	SD792	SD793	SD794	SD795	SD796	SD797	SD798	SD799	SD800	SD801	SD802	SD803	SD804	SD805	SD806	SD807	SD808	SD809	SD810	SD811	SD812	SD813	SD814	SD815	SD816	SD817	SD818	SD819	SD820	SD821	SD822	SD823	SD824	SD825	SD826	SD827	SD828	SD829	SD830	SD831	SD832	SD833	SD834	SD835	SD836	SD837	SD838	SD839	SD840	SD841	SD842	SD843	SD844	SD845	SD846	SD847	SD848	SD849	SD850	SD851	SD852	SD853	SD854	SD855	SD856	SD857	SD858	SD859	SD860	SD861	SD862	SD863	SD864	SD865	SD866	SD867	SD868	SD869	SD870	SD871	SD872	SD873	SD874	SD875	SD876	SD877	SD878	SD879	SD880	SD881	SD882	SD883	SD884	SD885	SD886	SD887	SD888	SD889	SD890	SD891	SD892	SD893	SD894	SD895	SD896	SD897	SD898	SD899	SD900	SD901	SD902	SD903	SD904	SD905	SD906	SD907	SD908	SD909	SD910	SD911	SD912	SD913	SD914	SD915	SD916	SD917	SD918	SD919	SD920	SD921	SD922	SD923	SD924	SD925	SD926	SD927	SD928	SD929	SD930	SD931	SD932	SD933	SD934	SD935	SD936	SD937	SD938	SD939	SD940	SD941	SD942	SD943	SD944	SD945	SD946	SD947	SD948	SD949	SD950	SD951	SD952	SD953	SD954	SD955	SD956	SD957	SD958	SD959	SD960	SD961	SD962	SD963	SD964	SD965	SD966	SD967	SD968	SD969	SD970	SD971	SD972	SD973	SD974	SD975	SD976	SD977	SD978	SD979	SD980	SD981	SD982	SD983	SD984	SD985	SD986	SD987	SD988	SD989	SD990	SD991	SD992	SD993	SD994	SD995	SD996	SD997	SD998	SD999	SD1000	SD1001	SD1002	SD1003	SD1004	SD1005	SD1006	SD1007	SD1008	SD1009	SD1010	SD1011	SD1012	SD1013	SD1014	SD1015	SD1016	SD1017	SD1018	SD1019	SD1020	SD1021	SD1022	SD1023	SD1024	SD1025	SD1026	SD1027	SD1028	SD1029	SD1030	SD1031	SD1032	SD1033	SD1034	SD1035	SD1036	SD1037	SD1038	SD1039	SD1040	SD1041	SD1042	SD1043	SD1044	SD1045	SD1046	SD1047	SD1048	SD1049	SD1050	SD1051	SD1052	SD1053	SD1054	SD1055	SD1056	SD1057	SD1058	SD1059	SD1060	SD1061	SD1062	SD1063	SD1064	SD1065	SD1066	SD1067	SD1068	SD1069	SD1070	SD1071	SD1072	SD1073	SD1074	SD1075	SD1076	SD1077	SD1078	SD1079	SD1080	SD1081	SD1082	SD1083	SD1084	SD1085	SD1086	SD1087	SD1088	SD1089	SD1090	SD1091	SD1092	SD1093	SD1094	SD1095	SD1096	SD1097	SD1098	SD1099	SD1100	SD1101	SD1102	SD1103	SD1104	SD1105	SD1106	SD1107	SD1108	SD1109	SD1110	SD1111	SD1112	SD1113	SD1114	SD1115	SD1116	SD1117	SD1118	SD1119	SD1120	SD1121	SD1122	SD1123	SD1124	SD1125	SD1126	SD1127	SD1128	SD1129	SD1130	SD1131	SD1132	SD1133	SD1134	SD1135	SD1136	SD1137	SD1138	SD1139	SD1140	SD1141	SD1142	SD1143	SD1144	SD1145	SD1146	SD1147	SD1148	SD1149	SD1150	SD1151	SD1152	SD1153	SD1154	SD1155	SD1156	SD1157	SD1158	SD1159	SD1160	SD1161	SD1162	SD1163	SD1164	SD1165	SD1166	SD1167	SD1168	SD1169	SD1170	SD1171	SD1172	SD1173	SD1174	SD1175	SD1176	SD1177	SD1178	SD1179	SD1180	SD1181	SD1182	SD1183	SD1184	SD1185	SD1186	SD1187	SD1188	SD1189	SD1190	SD1191	SD1192	SD1193	SD1194	SD1195	SD1196	SD1197	SD1198	SD1199	SD1200	SD1201	SD1202	SD1203	SD1204	SD1205	SD1206	SD1207	SD1208	SD1209	SD1210	SD1211	SD1212	SD1213	SD1214	SD1215	SD1216	SD1217	SD1218	SD1219	SD1220	SD1221	SD1222	SD1223	SD1224	SD1225	SD1226	SD1227	SD1228	SD1229	SD1230	SD1231	SD1232	SD1233	SD1234	SD1235	SD1236	SD1237	SD1238	SD1239	SD1240	SD1241	SD1242	SD1243	SD1244	SD1245	SD1246	SD1247	SD1248	SD1249	SD1250	SD1251	SD1252	SD1253	SD1254	SD1255	SD1256	SD1257	SD1258	SD1259	SD1260	SD1261	SD1262	SD1263	SD1264	SD1265	SD1266	SD1267	SD1268	SD1269	SD1270	SD1271	SD1272	SD1273	SD1274	SD1275	SD1276	SD1277	SD1278	SD1279	SD1280	SD1281	SD1282	SD1283	SD1284	SD1285	SD1286	SD1287	SD1288	SD1289	SD1290	SD1291	SD1292	SD1293	SD1294	SD1295	SD1296	SD1297	SD1298	SD1299	SD1300	SD1301	SD13

2.5 Pin Description^{[1][2]}

2.5.1 DDR

Table 2-1 DDR(mDDR, DDR2, DDR) Pins (74)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
D0	IO	B16	Bi-dir, Single-end	D0: DDR data bus bit 0 in 32-bit and 16-bit data bus	VDD _{MEM}
D1	IO	A16	Bi-dir, Single-end	D1: DDR data bus bit 1 in 32-bit and 16-bit data bus	VDD _{MEM}
D2	IO	C15	Bi-dir, Single-end	D2: DDR data bus bit 2 in 32-bit and 16-bit data bus	VDD _{MEM}
D3	IO	B15	Bi-dir, Single-end	D3: DDR data bus bit 3 in 32-bit and 16-bit data bus	VDD _{MEM}
D4	IO	C14	Bi-dir, Single-end	D4: DDR data bus bit 4 in 32-bit and 16-bit data bus	VDD _{MEM}
D5	IO	D14	Bi-dir, Single-end	D5: DDR data bus bit 5 in 32-bit and 16-bit data bus	VDD _{MEM}
D6	IO	A15	Bi-dir, Single-end	D6: DDR data bus bit 6 in 32-bit and 16-bit data bus	VDD _{MEM}
D7	IO	E14	Bi-dir, Single-end	D7: DDR data bus bit 7 in 32-bit and 16-bit data bus	VDD _{MEM}
D8	IO	B13	Bi-dir, Single-end	D8: DDR data bus bit 8 in 32-bit data bus	VDD _{MEM}
D9	IO	E11	Bi-dir, Single-end	D9: DDR data bus bit 9 in 32-bit data bus	VDD _{MEM}
D10	IO	C12	Bi-dir, Single-end	D10: DDR data bus bit 10 in 32-bit data bus	VDD _{MEM}
D11	IO	C13	Bi-dir, Single-end	D11: DDR data bus bit 11 in 32-bit data bus	VDD _{MEM}
D12	IO	C11	Bi-dir, Single-end	D12: DDR data bus bit 12 in 32-bit data bus	VDD _{MEM}
D13	IO	A12	Bi-dir, Single-end	D13: DDR data bus bit 13 in 32-bit data bus	VDD _{MEM}
D14	IO	A13	Bi-dir, Single-end	D14: DDR data bus bit 14 in 32-bit data bus	VDD _{MEM}
D15	IO	B12	Bi-dir, Single-end	D15: DDR data bus bit 15 in 32-bit data bus	VDD _{MEM}
D16	IO	E9	Bi-dir, Single-end	D16: DDR data bus bit 16 in 32-bit data bus	VDD _{MEM}
D17	IO	A8	Bi-dir, Single-end	D17: DDR data bus bit 17 in 32-bit data bus	VDD _{MEM}
D18	IO	B9	Bi-dir, Single-end	D18: DDR data bus bit 18 in 32-bit data bus	VDD _{MEM}
D19	IO	B8	Bi-dir, Single-end	D19: DDR data bus bit 19 in 32-bit data bus	VDD _{MEM}
D20	IO	A9	Bi-dir, Single-end	D20: DDR data bus bit 20 in 32-bit data bus	VDD _{MEM}
D21	IO	D8	Bi-dir, Single-end	D21: DDR data bus bit 21 in 32-bit data bus	VDD _{MEM}
D22	IO	C8	Bi-dir, Single-end	D22: DDR data bus bit 22 in 32-bit data bus	VDD _{MEM}
D23	IO	A7	Bi-dir, Single-end	D23: DDR data bus bit 23 in 32-bit data bus	VDD _{MEM}
D24 D8	IO	E6	Bi-dir, Single-end	D24: DDR data bus bit 24 in 32-bit data bus D8: DDR data bus bit 8 in 16-bit data bus	VDD _{MEM}
D25 D9	IO	C7	Bi-dir, Single-end	D25: DDR data bus bit 25 in 32-bit data bus D9: DDR data bus bit 9 in 16-bit data bus	VDD _{MEM}
D26 D10	IO	D5	Bi-dir, Single-end	D26: DDR data bus bit 26 in 32-bit data bus D10: DDR data bus bit 10 in 16-bit data bus	VDD _{MEM}
D27 D11	IO	B6	Bi-dir, Single-end	D27: DDR data bus bit 27 in 32-bit data bus D11: DDR data bus bit 11 in 16-bit data bus	VDD _{MEM}
D28 D12	IO	C5	Bi-dir, Single-end	D28: DDR data bus bit 28 in 32-bit data bus D12: DDR data bus bit 12 in 16-bit data bus	VDD _{MEM}
D29 D13	IO	C6	Bi-dir, Single-end	D29: DDR data bus bit 29 in 32-bit data bus D13: DDR data bus bit 13 in 16-bit data bus	VDD _{MEM}
D30 D14	IO	B5	Bi-dir, Single-end	D30: DDR data bus bit 30 in 32-bit data bus D14: DDR data bus bit 14 in 16-bit data bus	VDD _{MEM}
D31 D15	IO	A5	Bi-dir, Single-end	D31: DDR data bus bit 31 in 32-bit data bus D15: DDR data bus bit 15 in 16-bit data bus	VDD _{MEM}
DA0	O	E17	Output, Single-end	DA0: DDR address bus bit 0	VDD _{MEM}
DA1	O	B18	Output, Single-end	DA1: DDR address bus bit 1	VDD _{MEM}
DA2	O	B19	Output, Single-end	DA2: DDR address bus bit 2	VDD _{MEM}

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DA3	O	C18	Output, Single-end	DA3: DDR address bus bit 3	VDD _{MEM}
DA4	O	F5	Output, Single-end	DA4: DDR address bus bit 4	VDD _{MEM}
DA5	O	B3	Output, Single-end	DA5: DDR address bus bit 5	VDD _{MEM}
DA6	O	D4	Output, Single-end	DA6: DDR address bus bit 6	VDD _{MEM}
DA7	O	E4	Output, Single-end	DA7: DDR address bus bit 7	VDD _{MEM}
DA8	O	A3	Output, Single-end	DA8: DDR address bus bit 8	VDD _{MEM}
DA9	O	G5	Output, Single-end	DA9: DDR address bus bit 9	VDD _{MEM}
DA10	O	A19	Output, Single-end	DA10: DDR address bus bit 10	VDD _{MEM}
DA11	O	C4	Output, Single-end	DA11: DDR address bus bit 11	VDD _{MEM}
DA12	O	E5	Output, Single-end	DA12: DDR address bus bit 12	VDD _{MEM}
DA13	O	F16	Output, Single-end	DA13: DDR address bus bit 13	VDD _{MEM}
DA14	O	B17	Output, Single-end	DA14: DDR address bus bit 14	VDD _{MEM}
DA15	O	D17	Output, Single-end	DA15: DDR address bus bit 15	VDD _{MEM}
DA16	O	E15	Output, Single-end	DA16: DDR address bus bit 16	VDD _{MEM}
DCS0_	O	C17	Output, Single-end	DCS0_: DDR chip select 0	VDD _{MEM}
DCS1_	O	A17	Output, Single-end	DCS1_: DDR chip select 1	VDD _{MEM}
RAS_	O	C16	Output, Single-end	RAS_: DDR row address strobe	VDD _{MEM}
CAS_	O	E16	Output, Single-end	CAS_: DDR column address strobe	VDD _{MEM}
DWE_	O	A18	Output, Single-end	DWE_: DDR write enable	VDD _{MEM}
DQS0S	IO	E13	Bi-dir, Single-end	DQS0S: DDR data byte 0 strobe in 32-bit and 16-bit data bus	VDD _{MEM}
DQS1S	IO	D11	Bi-dir, Single-end	DQS1S: DDR data byte 1 strobe in 32-bit data bus	VDD _{MEM}
DQS2S	IO	E10	Bi-dir, Single-end	DQS2S: DDR data byte 2 strobe in 32-bit data bus	VDD _{MEM}
DQS3S DQS1S	IO	E7	Bi-dir, Single-end	DQS3S: DDR data byte 3 strobe in 32-bit data bus DQS1S: DDR data byte 1 strobe in 16-bit data bus	VDD _{MEM}
DQS0	IO	B14	Bi-dir, Differential	DQS0: DDR data byte 0 strobe positive in 32-bit and 16-bit data bus	VDD _{MEM}
DQS0_	IO	A14		DQS0_: DDR data byte 0 strobe negative in 32-bit and 16-bit data bus	VDD _{MEM}
DQS1	IO	B11	Bi-dir, Differential	DQS1: DDR data byte 1 strobe positive in 32-bit data bus	VDD _{MEM}
DQS1_	IO	A11		DQS1_: DDR data byte 1 strobe negative in 32-bit data bus	VDD _{MEM}
DQS2	IO	A10	Bi-dir, Differential	DQS2: DDR data byte 2 strobe positive in 32-bit data bus	VDD _{MEM}
DQS2_	IO	B10		DQS2_: DDR data byte 2 strobe negative in 32-bit data bus	VDD _{MEM}
DQS3 DQS1	IO	B7	Bi-dir, Differential	DQS3: DDR data byte 3 strobe positive in 32-bit data bus DQS1: DDR data byte 1 strobe positive in 16-bit data bus	VDD _{MEM}
DQS3_ DQS1_	IO	A6		DQS3_: DDR data byte 3 strobe negative in 32-bit data bus DQS1_: DDR data byte 1 strobe negative in 16-bit data bus	VDD _{MEM}
DM0	O	E12	Output, Single-end	DM0: DDR data byte 0 mask in 32-bit and 16-bit data bus	VDD _{MEM}
DM1	O	C10	Output, Single-end	DM1: DDR data byte 1 mask in 32-bit data bus	VDD _{MEM}
DM2	O	C9	Output, Single-end	DM2: DDR data byte 2 mask in 32-bit data bus	VDD _{MEM}
DM3 DM1	O	E8	Output, Single-end	DM3: DDR data byte 3 mask in 32-bit data bus DM1: DDR data byte 1 mask in 16-bit data bus	VDD _{MEM}
CKO	O	B4	Output, Differential	CKO: DDR clock output	VDD _{MEM}
CKO_	O	A4		CKO_: DDR inverse clock output	VDD _{MEM}
CKE	O	C3	Output, Single-end	CKE: DDR clock enable	VDD _{MEM}
VREFmem	AI	F11		VREFmem: DDR/DDR2 input reference voltage	VDD _{MEM}

2.5.2 BOOT and storage

Table 2-2 Static-Memory/MSC0/SPI0/DMA/1WIRE Pins (36; all GPIO shared: PA0~29, PB0~5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 PA0	IO IO	D3	8mA, pullup-pe	SD0: Static memory/NAND data bus bit 0 PA0: GPIO group A bit 0	VDDIO _{on}
SD1 PA1	IO IO	A1	8mA, pullup-pe	SD1: Static memory/NAND data bus bit 1 PA1: GPIO group A bit 1	VDDIO _{on}
SD2 PA2	IO IO	A2	8mA, pullup-pe	SD2: Static memory/NAND data bus bit 2 PA2: GPIO group A bit 2	VDDIO _{on}
SD3 PA3	IO IO	B1	8mA, pullup-pe	SD3: Static memory/NAND data bus bit 3 PA3: GPIO group A bit 3	VDDIO _{on}
SD4 PA4	IO IO	E3	8mA, pullup-pe	SD4: Static memory/NAND data bus bit 4 PA4: GPIO group A bit 4	VDDIO _{on}
SD5 PA5	IO IO	E2	8mA, pullup-pe	SD5: Static memory/NAND data bus bit 5 PA5: GPIO group A bit 5	VDDIO _{on}
SD6 PA6	IO IO	C1	8mA, pullup-pe	SD6: Static memory/NAND data bus bit 6 PA6: GPIO group A bit 6	VDDIO _{on}
SD7 PA7	IO IO	F2	8mA, pullup-pe	SD7: Static memory/NAND data bus bit 7 PA7: GPIO group A bit 7	VDDIO _{on}
SD8 PA8	IO IO	H4	8mA, pullup-pe	SD8: Static memory/NAND data bus bit 8 PA8: GPIO group A bit 8	VDDIO _{on}
SD9 PA9	IO IO	B2	8mA, pullup-pe	SD9: Static memory/NAND data bus bit 9 PA9: GPIO group A bit 9	VDDIO _{on}
SD10 PA10	IO IO	C2	8mA, pullup-pe	SD10: Static memory/NAND data bus bit 10 PA10: GPIO group A bit 10	VDDIO _{on}
SD11 PA11	IO IO	D1	8mA, pullup-pe	SD11: Static memory/NAND data bus bit 11 PA11: GPIO group A bit 11	VDDIO _{on}
SD12 PA12	IO IO	F3	8mA, pullup-pe	SD12: Static memory/NAND data bus bit 12 PA12: GPIO group A bit 12	VDDIO _{on}
SD13 PA13	IO IO	G2	8mA, pullup-pe	SD13: Static memory/NAND data bus bit 13 PA13: GPIO group A bit 13	VDDIO _{on}
SD14 PA14	IO IO	H5	8mA, pullup-pe	SD14: Static memory/NAND data bus bit 14 PA14: GPIO group A bit 14	VDDIO _{on}
SD15 PA15	IO IO	J5	8mA, pullup-pe	SD15: Static memory/NAND data bus bit 15 PA15: GPIO group A bit 15	VDDIO _{on}
SA0 (CL) PB0	O IO	H3	8mA, pulldown-pe, rst-pe	SA1: Static memory address bus bit 0 If NAND flash is used, this pin is used as NAND CL (command latch) pin PB0: GPIO group B bit 0	VDDIO _{on}
SA1 (AL) PB1	O IO	J2	8mA, pulldown-pe, rst-pe	SA1: Static memory address bus bit 1 If NAND flash is used, this pin is used as NAND AL (address latch) pin PB1: GPIO group B bit 1	VDDIO _{on}
SA2 PB2	O IO	J3	8mA, pullup-pe	SA2: Static memory address bus bit 2 PB2: GPIO group B bit 2	VDDIO _{on}
SA3 PB3	O IO	G1	8mA, pullup-pe	SA3: Static memory address bus bit 3 PB3: GPIO group B bit 3	VDDIO _{on}
SA4 DREQ1 MII_CRS PB4(FRB1)	O I I IO	J1	8mA, pullup-pe	SA4: Static memory address bus bit 4 DREQ1: External DMA request input 1 MII_CRS: Ethernet carrier sense for MII PB4: GPIO group B bit 4. NAND flash FRB input 1 candidate	VDDIO
SA5 DACK1 PB5(FRB1)	O O IO	L5	8mA, pullup-pe	SA5: Static memory address bus bit 5 DACK1: External DMA acknowledge output 1 PB5: GPIO group B bit 5. NAND flash FRB input 1 candidate	VDDIO
RD_ PA16	O IO	D2	8mA, pullup-pe, rst-pe	RD_: Static memory read strobe PA16: GPIO group A bit 16	VDDIO _{on}

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
WE_ PA17	O IO	E1	8mA, pullup-pe, rst-pe	WE_: Static memory write strobe PA17: GPIO group A bit 17	VDDIO _{On}
FRE_ MSC0_CLK SSI0_CLK PA18	O O O IO	H2	8mA, pullup-pe, rst-pe	FRE_: NAND read enable MSC0_CLK: MSC (MMC/SD) 0 clock output SSI0_CLK: SSI 0 clock output PA18: GPIO group A bit 18	VDDIO _{On}
FWE_ MSC0_CMD SSI0_CE0_ PA19	O IO O IO	G3	8mA, pullup-pe, rst-pe	FEW_: NAND write enable MSC0_CMD: MSC (MMC/SD) 0 command SSI0_CE0_: SSI 0 chip enable 0 PA19: GPIO group A bit 19	VDDIO _{On}
MSC0_D0 SSI0_DR PA20(FRB0)	IO I IO	F1	8mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 SSI0_DR: SSI 0 data input PA20: GPIO group A bit 20. NAND flash FRB (ready/busy) input 0	VDDIO _{On}
CS1_ MSC0_D1 SSI0_DT PA21	O IO O IO	H6	8mA, pullup-pe, rst-pe	CS1_: NAND/NOR/SRAM chip select 1 MSC0_D1: MSC (MMC/SD) 0 data bit 1 SSI0_DT: SSI 0 data output PA21: GPIO group A bit 21	VDDIO _{On}
CS2_ MSC0_D2 PA22	O IO IO	K5	8mA, pullup-pe, rst-pe	CS2_: NAND/NOR/SRAM chip select 2 MSC0_D2: MSC (MMC/SD) 0 data bit 2 PA22: GPIO group A bit 22	VDDIO _{On}
CS3_ MSC0_D3 PA23	O IO IO	J6	8mA, pullup-pe, rst-pe	CS3_: NAND/NOR/SRAM chip select 3 MSC0_D3: MSC (MMC/SD) 0 data bit 3 PA23: GPIO group A bit 23	VDDIO _{On}
CS4_ PA24	O IO	K2	8mA, pullup-pe, rst-pe	CS4_: NAND/NOR/SRAM chip select 4 PA24: GPIO group A bit 24	VDDIO
CS5_ PA25	O IO	L3	8mA, pullup-pe, rst-pe	CS5_: NAND/NOR/SRAM chip select 5 PA25: GPIO group A bit 25	VDDIO
CS6_ RDWR_ PA26	O O IO	M3	8mA, pullup-pe, rst-pe	CS6_: NAND/NOR/SRAM chip select 6 RDWR_: Static memory access indicator, 1 for read and 0 for write PA26: GPIO group A bit 26	VDDIO
WAIT_ PA27(FRB1)	I IO	L4	8mA, pullup-pe	WAIT_: Slow static memory/device wait signal PA27: GPIO group A bit 27. NAND flash FRB input 1 candidate	VDDIO
DREQ0 PA28(FRB1)	I IO	H1	8mA, pullup-pe	DREQ0: External DMA request input 0 PA28: GPIO group A bit 28. NAND flash FRB input 1 candidate	VDDIO
DACK0 OWI PA29(FRB1)	O IO IO	K3	8mA, pullup-pe	DACK0: External DMA acknowledge output 0 OWI: One wire interface PA29: GPIO group A bit 29. NAND flash FRB input 1 candidate	VDDIO

2.5.3 LCD

Table 2-3 LCDC Pins (28; all GPIO shared: PC0~27)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_B0 LCD_REV PC0	O O IO	J20	8mA, pullup-pe	LCD_B0: LCD Blue data bit 0 LCD_REV: LCD REV output for special TFT PC0: GPIO group C bit 0	VDDIO
LCD_B1 LCD_PS PC1	O O IO	J21	8mA, pullup-pe	LCD_B1: LCD Blue data bit 1 LCD_PS: LCD PS output for special TFT PC1: GPIO group C bit 1	VDDIO
LCD_B2 PC2	O IO	K21	8mA, pullup-pe	LCD_B2: LCD Blue data bit 2 PC2: GPIO group C bit 2	VDDIO
LCD_B3 PC3	O IO	M14	8mA, pullup-pe	LCD_B3: LCD Blue data bit 3 PC3: GPIO group C bit 3	VDDIO
LCD_B4 PC4	O IO	K20	8mA, pullup-pe	LCD_B4: LCD Blue data bit 4 PC4: GPIO group C bit 4	VDDIO
LCD_B5 PC5	O IO	L16	8mA, pullup-pe	LCD_B5: LCD Blue data bit 5 PC5: GPIO group C bit 5	VDDIO
LCD_B6 PC6	O IO	K19	8mA, pullup-pe	LCD_B6: LCD Blue data bit 6 PC6: GPIO group C bit 6	VDDIO
LCD_B7 PC7	O IO	N14	8mA, pullup-pe	LCD_B7: LCD Blue data bit 7 PC7: GPIO group C bit 7	VDDIO
LCD_PCLK PC8	O IO	L21	16mA, pullup-pe	LCD_PCLK: LCD pixel clock PC8: GPIO group C bit 8	VDDIO
LCD_DE PC9	O IO	L20	8mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC9: GPIO group C bit 9	VDDIO
LCD_G0 LCD_SPL PC10	O O IO	L18	8mA, pullup-pe, rst-pe	LCD_G0: LCD Green data bit 0 LCD_SPL: LCD SPL output PC10: GPIO group C bit 10	VDDIO
LCD_G1 PC11	O IO	L17	8mA, pullup-pe	LCD_G1: LCD Green data bit 1 PC11: GPIO group C bit 11	VDDIO
LCD_G2 PC12	O IO	N21	8mA, pullup-pe	LCD_G2: LCD Green data bit 2 PC12: GPIO group C bit 12	VDDIO
LCD_G3 PC13	O IO	L19	8mA, pullup-pe	LCD_G3: LCD Green data bit 3 PC13: GPIO group C bit 13	VDDIO
LCD_G4 PC14	O IO	P17	8mA, pullup-pe	LCD_G4: LCD Green data bit 4 PC14: GPIO group C bit 14	VDDIO
LCD_G5 PC15	O IO	R16	8mA, pullup-pe	LCD_G5: LCD Green data bit 5 PC15: GPIO group C bit 15	VDDIO
LCD_G6 PC16	O IO	R17	8mA, pullup-pe	LCD_G6: LCD Green data bit 6 PC16: GPIO group C bit 16	VDDIO
LCD_G7 PC17	O IO	P16	8mA, pullup-pe	LCD_G7: LCD Green data bit 7 PC17: GPIO group C bit 17	VDDIO
LCD_HSYN PC18	IO IO	M16	8mA, pullup-pe	LCD_HSYN: LCD line clock/horizontal sync PC18: GPIO group C bit 18	VDDIO
LCD_VSYN PC19	IO IO	M21	8mA, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PC19: GPIO group C bit 19	VDDIO
LCD_R0 LCD_CLS PC20	O O IO	M19	8mA, pullup-pe	LCD_R0: LCD Red data bit 0 LCD_CLS: LCD CLS output PC20: GPIO group C bit 20	VDDIO
LCD_R1 PC21	O IO	N16	8mA, pullup-pe	LCD_R1: LCD Red data bit 1 PC21: GPIO group C bit 21	VDDIO
LCD_R2 PC22	O IO	P18	8mA, pullup-pe	LCD_R2: LCD Red data bit 2 PC22: GPIO group C bit 22	VDDIO
LCD_R3 PC23	O IO	M20	8mA, pullup-pe	LCD_R3: LCD Red data bit 3 PC23: GPIO group C bit 23	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_R4 PC24	O IO	N19	8mA, pullup-pe	LCD_R4: LCD Red data bit 4 PC24: GPIO group C bit 24	VDDIO
LCD_R5 PC25	O IO	N17	8mA, pullup-pe	LCD_R5: LCD Red data bit 5 PC25: GPIO group C bit 25	VDDIO
LCD_R6 PC26	O IO	P19	8mA, pullup-pe	LCD_R6: LCD Red data bit 6 PC26: GPIO group C bit 26	VDDIO
LCD_R7 PC27	O IO	M17	8mA, pullup-pe	LCD_R7: LCD Red data bit 7 PC27: GPIO group C bit 27	VDDIO

2.5.4 MAC/PCM1

Table 2-4 MAC-MII/RMII/PCM1 Pins (12; all GPIO shared: PF4~15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MII_TXD0 PF4	O IO	K1	8mA, pulldown-pe	MII_TXD0: Ethernet transmit data bit 0 for MII and RMII PF4: GPIO group F bit 4. Pull-down not enabled at and after reset	VDDIO
MII_TXD1 PF5	O IO	L1	8mA, pulldown-pe	MII_TXD1: Ethernet transmit data bit 1 for MII and RMII PF5: GPIO group F bit 5. Pull-down not enabled at and after reset	VDDIO
MII_TXCLK (RMII_CLK) PF6	I IO	L2	8mA, pulldown-pe	MII_TXCLK: Ethernet 25MHz transmit clock for MII or (RMII_CLK) ethernet 50MHz reference clock for RMII PF6: GPIO group F bit 6. Pull-down not enabled at and after reset	VDDIO
MII_RXCLK PF7	I IO	M2	8mA, pulldown-pe	MII_RXCLK: Ethernet receive clock for MII (25MHz) PF7: GPIO group F bit 7. Pull-down not enabled at and after reset	VDDIO
MII_RXER PF8	I IO	N3	8mA, pulldown-pe	MII_RXER: Ethernet receive error for MII and RMII PF8: GPIO group F bit 8. Pull-down not enabled at and after reset	VDDIO
MII_RXDV PF9	I IO	M1	8mA, pulldown-pe	MII_RXDV: Ethernet receive data valid for MII and RMII PF9: GPIO group F bit 9. Pull-down not enabled at and after reset	VDDIO
MII_RXD0 PF10	I IO	N2	8mA, pulldown-pe	MII_RXD0: Ethernet receive data bit 0 for MII and RMII PF10: GPIO group F bit 10. Pull-down not enabled at and after reset	VDDIO
MII_RXD1 PF11	I IO	N1	8mA, pulldown-pe	MII_RXD1: Ethernet receive data bit 1 for MII and RMII PF11: GPIO group F bit 11. Pull-down not enabled at and after reset	VDDIO
MII_TXEN PCM1_DO PF12	O O IO	P2	8mA, pullup-pe	MII_TXEN: Ethernet transmit enable for MII and RMII PCM1_DO: PCM 1 data out PF12: GPIO group F bit 12	VDDIO
MII_MDC PCM1_CLK PF13	O IO IO	P1	8mA, pullup-pe	MII_MDC: Ethernet management clock for MII and RMII PCM1_CLK: PCM 1 clock PF13: GPIO group F bit 13	VDDIO
MII_MDIO PCM1_SYN PF14	IO IO IO	P3	8mA, pullup-pe	MII_MDIO: Ethernet management data for MII and RMII PCM1_SYN: PCM 1 sync PF14: GPIO group F bit 14	VDDIO
MII_COL PCM1_DI PF15	I I IO	R1	8mA, pullup-pe	MII_COL: Ethernet collision for MII PCM1_DI: PCM 1 data in PF15: GPIO group F bit 15	VDDIO

2.5.5 CIM

Table 2-5 CIM/EPD/I2C2/DMIC Pins (16; all GPIO shared: PB6~19, PF16~17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM_PCLK PB6	I IO	B20	8mA, pullup-pe	CIM_PCLK: CIM pixel clock input PB6: GPIO group B bit 6	VDDIO
CIM_HSYN PB7	I O	G17	8mA, pullup-pe	CIM_HSYN: CIM horizontal sync input PB7: GPIO group B bit 7	VDDIO
CIM_VSYN PB8	I IO	C20	8mA, pullup-pe, rst-pe	CIM_VSYN: CIM vertical sync input PB8: GPIO group B bit 8	VDDIO
CIM_MCLK EPD_PWC PB9	O O IO	H17	8mA, pullup-pe	CIM_MCLK: CIM master clock output EPD_PWC: EPD power control common PB9: GPIO group B bit 9	VDDIO
CIM_D0 EPD_PWR0 PB10	I O IO	A21	8mA, pulldown-pe	CIM_D0: CIM data input bit 0. When use 8-bit data, use CIM_D0~D7 EPD_PWR0: EPD power control bit 0 PB10: GPIO group B bit 10	VDDIO
CIM_D1 EPD_PWR1 PB11	I O IO	B21	8mA, pulldown-pe	CIM_D1: CIM data input bit 1 EPD_PWR1: EPD power control bit 1 PB11: GPIO group B bit 11	VDDIO
CIM_D2 EPD_SCE2_ PB12	I O IO	D20	8mA, pullup-pe	CIM_D2: CIM data input bit 2 EPD_SCE2_: EPD source driver chip select 2 PB12: GPIO group B bit 12	VDDIO
CIM_D3 EPD_SCE3_ PB13	I O IO	E19	8mA, pullup-pe	CIM_D3: CIM data input bit 3 EPD_SCE3_: EPD source driver chip select 3 PB13: GPIO group B bit 13	VDDIO
CIM_D4 EPD_SCE4_ PB14	I O IO	C21	8mA, pullup-pe	CIM_D4: CIM data input bit 4 EPD_SCE4_: EPD source driver chip select 4 PB14: GPIO group B bit 14	VDDIO
CIM_D5 EPD_SCE5_ PB15	I O IO	F19	8mA, pullup-pe	CIM_D5: CIM data input bit 5 EPD_SCE5_: EPD source driver chip select 5 PB15: GPIO group B bit 15	VDDIO
CIM_D6 EPD_PWR2 PB16	I O IO	E20	8mA, pulldown-pe	CIM_D6: CIM data input bit 6 EPD_PWR6: EPD power control bit 2 PB16: GPIO group B bit 16	VDDIO
CIM_D7 EPD_PWR3 PB17	I O IO	F20	8mA, pulldown-pe	CIM_D7: CIM data input bit 7 EPD_PWR7: EPD power control bit 3 PB17: GPIO group B bit 17	VDDIO
CIM_D8 EPD_BD0 DMIC_CLK PB18	I O O IO	D21	8mA, pulldown-pe	CIM_D8: CIM data input bit 8 EPD_BD0: EPD border management bit 0 DMIC_CLK: Digital MIC clock output PB18: GPIO group B bit 18	VDDIO
CIM_D9 EPD_BD1 DMIC_IN PB19	I O I IO	G19	8mA, pulldown-pe	CIM_D9: CIM data input bit 9 EPD_BD1: EPD border management bit 1 DMIC_IN: Digital MIC input PB19: GPIO group B bit 19	VDDIO
CIM_D10 EPD_BD2 I2C2_SDA PF16	I O IO	E21	8mA, pullup-pe	CIM_D10: CIM data input bit 10 EPD_BD2: EPD border management bit 2 I2C2_SDA: I2C 2 serial data PF16: GPIO group F bit 16	VDDIO
CIM_D11 EPD_BD3 I2C2_SCK PF17	I O IO	H18	8mA, pullup-pe	CIM_D11: CIM data input bit 11 EPD_BD3: EPD border management bit 3 I2C2_SCK: I2C 2 serial clock PF17: GPIO group F bit 17	VDDIO

2.5.6 TSSI/SSI/MSC/UART/I2C

Table 2-6 TSSI/MSC2/SSI Pins (12; all GPIO shared: PB20~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC2_D0 SSI0_DR SSI1_DR TSD0 PB20	I I I I IO	Y8	8mA, pullup-pe	MSC2_D0: MSC (MMC/SD) 2 data bit 0 SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input TSD0: TS slave interface input data bus bit 0 PB20: GPIO group B bit 20	VDDIO
MSC2_D1 SSI0_DT SSI1_DT TSD1 PB21	IO O O I IO	W8	8mA, pullup-pe	MSC2_D1: MSC (MMC/SD) 2 data bit 1 SSI0_DT: SSI 0 data output SSI1_DT: SSI 1 data output TSD1: TS interface input data bus bit 1 PB21: GPIO group B bit 21	VDDIO
TSD2 PB22	I IO	W10	8mA, pullup-pe	TSD2: TS interface input data bus bit 2 PB22: GPIO group B bit 22	VDDIO
TSD3 PB23	I IO	P9	8mA, pullup-pe	TSD3: TS interface input data bus bit 3 PB23: GPIO group B bit 23	VDDIO
TSD4 PB24	I IO	AA9	8mA, pullup-pe	TSD4: TS interface input data bus bit 4 PB24: GPIO group B bit 24	VDDIO
TSD5 PB25	I IO	N8	8mA, pullup-pe	TSD5: TS interface input data bus bit 5 PB25: GPIO group B bit 25	VDDIO
TSD6 PB26	I IO	T9	8mA, pullup-pe	TSD6: TS interface input data bus bit 6 PB26: GPIO group B bit 26	VDDIO
TSD7 PB27	I IO	Y9	8mA, pullup-pe	TSD7: TS interface input data bus bit 7 PB27: GPIO group B bit 27	VDDIO
MSC2_CLK SSI0_CLK SSI1_CLK TSCLK PB28	O O O I IO	AA8	8mA, pullup-pe	MSC2_CLK: MSC (MMC/SD) 2 clock output SSI0_CLK: SSI 0 clock output SSI1_CLK: SSI 1 clock output TSCLK: TS interface clock input PB28: GPIO group B bit 28	VDDIO
MSC2_CMD SSI0_CE0_ SSI1_CE0_ TSSTR PB29	IO O O I IO	W9	8mA, pullup-pe, rst-pe	MSC2_CMD: MSC (MMC/SD) 2 command SSI0_CE0_: SSI 0 chip enable 0 SSI1_CE0_: SSI 1 chip enable 0 TSSTR: TS interface frame start input PB29: GPIO group B bit 29	VDDIO
MSC2_D2 SSI0_GPC SSI1_GPC TSFAIL PB30	IO O O I IO	AA7	8mA, pullup-pe	MSC2_D2: MSC (MMC/SD) 2 data bit 2 SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal TSFAIL: TS interface error package indicator input PB30: GPIO group B bit 30	VDDIO
MSC2_D3 SSI0_CE1_ SSI1_CE1_ TSFRM PB31	IO O O I IO	Y7	8mA, pullup-pe, rst-pe	MSC2_D3: MSC (MMC/SD) 2 data bit 3 SSI0_CE1_: SSI 0 chip enable 1 SSI1_CE1_: SSI 1 chip enable 1 TSFRM: TS interface frame valid input PB31: GPIO group B bit 31	VDDIO

Table 2-7 UART0/GPSBB Pins (4; all GPIO shared: PF0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RxD GPS_CLK PF0	I I IO	T5	8mA, pullup-pe	UART0_RxD: UART 0 Receiving data GPS_CLK: GPS baseband clock input from RF PF0: GPIO group F bit 0	VDDIO
UART0_CTS_ GPS_MAG PF1	I I IO	R5	8mA, pullup-pe, rst-pe	UART0_CTS_: UART 0 CTS_ input GPS_MAG: GPS baseband MAG input from RF PF1: GPIO group F bit 1	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RTS_ GPS_SIG PF2	O I IO	P6	8mA, pullup-pe, rst-pe	UART0_RTS_: UART 0 RTS_ output GPS_SIG: GPS baseband SIG input from RF PF2: GPIO group F bit 2	VDDIO
UART0_TxD PF3	O IO	T6	8mA, pullup-pe, rst-pe	UART0_TxD: UART 0 transmitting data PF3: GPIO group F bit 3	VDDIO

Table 2-8 MSC1/SSI, Pins (6; all GPIO shared: PD20~25)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_D0 SSI0_DR SSI1_DR PD20	IO I I IO	D18	8mA, pullup-pe	MSC1_D0: MSC (MMC/SD) 1 data bit 0 SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input PD20: GPIO group D bit 20	VDDIO
MSC1_D1 SSI0_DT SSI1_DT PD21	IO O O IO	F17	8mA, pullup-pe	MSC1_D1: MSC (MMC/SD) 1 data bit 1 SSI0_DT: SSI 0 data output SSI1_DT: SSI 1 data output PD21: GPIO group D bit 21	VDDIO
MSC1_D2 SSI0_GPC SSI1_GPC PD22	IO O O IO	C19	8mA, pullup-pe	MSC1_D2: MSC (MMC/SD) 1 data bit 2 SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal PD22: GPIO group D bit 22	VDDIO
MSC1_D3 SSI0_CE1_ SSI1_CE1_ PD23	IO O O IO	A20	8mA, pullup-pe, rst-pe	MSC1_D3: MSC (MMC/SD) 1 data bit 3 SSI0_CE1_: SSI 0 chip enable 1 SSI1_CE1_: SSI 1 chip enable 1 PD23: GPIO group D bit 23	VDDIO
MSC1_CLK SSI0_CLK SSI1_CLK PD24	O O O IO	D19	8mA, pullup-pe	MSC1_CLK: MSC (MMC/SD) 1 clock output SSI0_CLK: SSI 0 clock output SSI1_CLK: SSI 1 clock output PD24: GPIO group D bit 24	VDDIO
MSC1_CMD SSI0_CE0_ SSI1_CE0_ PD25	IO O O IO	E18	8mA, pullup-pe, rst-pe	MSC1_CMD: MSC (MMC/SD) 1 command SSI0_CE0_: SSI 0 chip enable 0 SSI1_CE0_: SSI 1 chip enable 0 PD25: GPIO group D bit 25	VDDIO

Table 2-9 UART1/MII Pins (4; all GPIO shared: PD26~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART1_RxD MII_RXD2 PD26	I I IO	L6	8mA, pullup-pe	UART1_RxD: UART 1 Receiving data MII_RXD2: Ethernet receive data bit 2 for MII PD26: GPIO group D bit 26	VDDIO
UART1_CTS_ MII_RXD3 PD27	I I IO	M5	8mA, pullup-pe	UART1_CTS_: UART 1 CTS_ input MII_RXD3: Ethernet receive data bit 3 for MII PD27: GPIO group D bit 27	VDDIO
UART1_TxD MII_TXD2 PD28	O O IO	M6	8mA, pullup-pe, rst-pe	UART1_TxD: UART 1 transmitting data MII_TXD2: Ethernet transmit data bit 2 for MII PD28: GPIO group D bit 28	VDDIO
UART1_RTS_ MII_TXD3 PD29	O O IO	M8	8mA, pullup-pe, rst-pe	UART1_RTS_: UART 1 RTS_ output MII_TXD3: Ethernet transmit data bit 3 for MII PD29: GPIO group D bit 29	VDDIO

Table 2-10 UART2 Pins (0/4/4; all GPIO shared: PC28~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART2_RxD PC28	I IO	T7	8mA, pullup-pe	UART2_RxD: UART 2 Receiving data PC28: GPIO group C bit 28	VDDIO
UART2_CTS_ PC29	I IO	U7	8mA, pullup-pe	UART2_CTS_: UART 2 CTS_ input PC29: GPIO group C bit 29	VDDIO
UART2_TxD PC30	O IO	P8	8mA, pullup-pe, rst-pe	UART2_TxD: UART 2 transmitting data PC30: GPIO group C bit 30	VDDIO
UART2_RTS_ PC31	O IO	U8	8mA, pullup-pe, rst-pe	UART2_RTS_: UART 2 RTS_ output PC31: GPIO group C bit 31	VDDIO

Table 2-11 I2C0/I2C1 Pins (4; all GPIO shared: PD30~31, PE30~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
I2C0_SDA PD30	IO IO	R6	8mA, pullup-pe	I2C0_SDA: I2C 0 serial data PD30: GPIO group D bit 30	VDDIO
I2C0_SCK PD31	IO IO	T8	8mA, pullup-pe	I2C0_SCK: I2C 0 serial clock PD31: GPIO group D bit 31	VDDIO
I2C1_SDA PE30	IO IO	R19	8mA, pullup-pe	I2C1_SDA: I2C 1 serial data PE30: GPIO group E bit 30	VDDIO
I2C1_SCK PE31	IO IO	T19	8mA, pullup-pe	I2C1_SCK: I2C 1 serial clock PE31: GPIO group E bit 31	VDDIO

Table 2-12 MSC Pins (10; all GPIO shared: PE20~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_CLK MSC1_CLK MSC2_CLK PE28	O O O IO	V1	16mA, pullup-pe	MSC0_CLK: MSC (MMC/SD) 0 clock output MSC1_CLK: MSC (MMC/SD) 1 clock output MSC2_CLK: MSC (MMC/SD) 2 clock output PE28: GPIO group E bit 28	VDDIO
MSC0_CMD MSC1_CMD MSC2_CMD PE29	IO IO IO IO	V2	8mA, pullup-pe	MSC0_CMD: MSC (MMC/SD) 0 command MSC1_CMD: MSC (MMC/SD) 1 command MSC2_CMD: MSC (MMC/SD) 2 command PE29: GPIO group E bit 29	VDDIO
MSC0_D0 MSC1_D0 MSC2_D0 PE20	IO IO IO IO	R2	8mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 MSC1_D0: MSC (MMC/SD) 1 data bit 0 MSC2_D0: MSC (MMC/SD) 2 data bit 0 PE20: GPIO group E bit 20	VDDIO
MSC0_D1 MSC1_D1 MSC2_D1 PE21	IO IO IO IO	P4	8mA, pullup-pe	MSC0_D1: MSC (MMC/SD) 0 data bit 1 MSC1_D1: MSC (MMC/SD) 1 data bit 1 MSC2_D1: MSC (MMC/SD) 2 data bit 1 PE21: GPIO group E bit 21	VDDIO
MSC0_D2 MSC1_D2 MSC2_D2 PE22	IO IO IO IO	T1	8mA, pullup-pe	MSC0_D2: MSC (MMC/SD) 0 data bit 2 MSC1_D2: MSC (MMC/SD) 1 data bit 2 MSC2_D2: MSC (MMC/SD) 2 data bit 2 PE22: GPIO group E bit 22	VDDIO
MSC0_D3 MSC1_D3 MSC2_D3 PE23	IO IO IO IO	T2	8mA, pullup-pe	MSC0_D3: MSC (MMC/SD) 0 data bit 3 MSC1_D3: MSC (MMC/SD) 1 data bit 3 MSC2_D3: MSC (MMC/SD) 2 data bit 3 PE23: GPIO group E bit 23	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_D4 MSC1_D4 MSC2_D4 PE24	IO IO IO IO	R3	8mA, pullup-pe	MSC0_D4: MSC (MMC/SD) 0 data bit 4 MSC1_D4: MSC (MMC/SD) 1 data bit 4 MSC2_D4: MSC (MMC/SD) 2 data bit 4 PE24: GPIO group E bit 24	VDDIO
MSC0_D5 MSC1_D5 MSC2_D5 PE25	IO IO IO IO	U1	8mA, pullup-pe	MSC0_D5: MSC (MMC/SD) 0 data bit 5 MSC1_D5: MSC (MMC/SD) 1 data bit 5 MSC2_D5: MSC (MMC/SD) 2 data bit 5 PE25: GPIO group E bit 25	VDDIO
MSC0_D6 MSC1_D6 MSC2_D6 PE26	IO IO IO IO	T3	8mA, pullup-pe	MSC0_D6: MSC (MMC/SD) 0 data bit 6 MSC1_D6: MSC (MMC/SD) 1 data bit 6 MSC2_D6: MSC (MMC/SD) 2 data bit 6 PE26: GPIO group E bit 26	VDDIO
MSC0_D7 MSC1_D7 MSC2_D7 PE27	IO IO IO IO	U2	8mA, pullup-pe	MSC0_D7: MSC (MMC/SD) 0 data bit 7 MSC1_D7: MSC (MMC/SD) 1 data bit 7 MSC2_D7: MSC (MMC/SD) 2 data bit 7 PE27: GPIO group E bit 27	VDDIO

Table 2-13 SSI Pins (6; all GPIO shared: PE14~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI0_DR SSI1_DR PE14	I I IO	V8	8mA, pullup-pe	SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input PE14: GPIO group E bit 14	VDDIO
SSI0_CLK SSI1_CLK PE15	O O IO	W7	8mA, pullup-pe	SSI0_CLK: SSI 0 clock output SSI1_CLK: SSI 1 clock output PE15: GPIO group E bit 15	VDDIO
SSI0_CE0_ SSI1_CE0_ PE16	O O IO	Y6	8mA, pullup-pe, rst-pe	SSI0_CE0_: SSI 0 chip enable 0 SSI1_CE0_: SSI 1 chip enable 0 PE16: GPIO group E bit 16	VDDIO
SSI0_DT SSI1_DT PE17	O O IO	AA5	8mA, pullup-pe	SSI0_DT: SSI 0 data output SSI1_DT: SSI 1 data output PE17: GPIO group E bit 17	VDDIO
SSI0_CE1_ SSI1_CE1_ PE18	O O IO	U9	8mA, pullup-pe, rst-pe	SSI0_CE1_: SSI 0 chip enable 1 SSI1_CE1_: SSI 1 chip enable 1 PE18: GPIO group E bit 18	VDDIO
SSI0_GPC SSI1_GPC PE19	O O IO	AA6	8mA, pullup-pe	SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal PE19: GPIO group E bit 19	VDDIO

2.5.7 PCM0/PCM1/PS2/SCC/PWM/AIC/UART

Table 2-14 PCM0/PS2/SCC Pins (10; all GPIO shared: PD0~9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PCM0_DO PD0	O IO	U18	8mA, pullup-pe	PCM0_DO: PCM 0 data out PD0: GPIO group D bit 0	VDDIO
PCM0_CLK PD1	IO IO	U16	8mA, pullup-pe	PCM0_CLK: PCM 0 clock PD1: GPIO group D bit 1	VDDIO
PCM0_SYN PD2	IO IO	T17	8mA, pullup-pe	PCM0_SYN: PCM 0 sync PD2: GPIO group D bit 2	VDDIO
PCM0_DI PD3	I IO	T16	8mA, pullup-pe	PCM0_DI: PCM 0 data in PD3: GPIO group D bit 3	VDDIO
PS2_MCLK PD4	IO IO	T10	8mA, pullup-pe	PS2_MCLK: PS/2 mouse clock PD4: GPIO group D bit 4	VDDIO
PS2_MDATA PD5	IO IO	V11	8mA, pullup-pe	PS2_MDATA: PS/2 mouse data PD5: GPIO group D bit 5	VDDIO
PS2_KCLK PD6	IO IO	T11	8mA, pullup-pe	PS2_KCLK: PS/2 keyboard clock PD6: GPIO group D bit 6	VDDIO
PS2_KDATA PD7	IO IO	U11	8mA, pullup-pe	PS2_KDATA: PS/2 keyboard data PD7: GPIO group D bit 7	VDDIO
SCC_DATA PD8	IO IO	T12	8mA, pullup-pe	SCC_DATA: Smartcard controller (7816-3) data PD8: GPIO group D bit 8	VDDIO
SCC_CLK CLK48M_I PD9	O I IO	U12	8mA, pullup-pe	SCC_CLK: Smartcard controller (7816-3) clock CLK48M_I: 48MHz clock input for USB1.1 host PD9: GPIO group D bit 9	VDDIO

Table 2-15 PWM/AIC/UART3/EPD Pins (17; all GPIO shared: PE0~9, 11~13, PD10~13)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 PE0	IO IO	P10	8mA, pulldown-pe	PWM0: PWM output or pulse input 0 PE0: GPIO group E bit 0. Pull-down not enabled at and after reset	VDDIO
PWM1 PE1	O IO	U10	8mA, pulldown-pe	PWM1: PWM 1 output. This PWM can run in sleep mode in RTCLK clock PE1: GPIO group E bit 1. Pull-down not enabled at and after reset	VDDIO
PWM2 PE2	O IO	W1	8mA, pullup-pe	PWM2: PWM 2 output. This PWM can run in sleep mode in RTCLK clock PE2: GPIO group E bit 2. Pull-up not enabled at and after reset	VDDIO
PWM3 PE3	IO IO	N5	8mA, pullup-pe	PWM3: PWM output or pulse input 3 PE3: GPIO group E bit 3. Pull-up not enabled at and after reset	VDDIO
PWM4 PE4	IO IO	P5	8mA, pullup-pe	PWM4: PWM output or pulse input 4 PE4: GPIO group E bit 4	VDDIO
PWM5 UART3_TxD SCLK_RSTN PE5	IO O O IO	F21	8mA, pullup-pe, rst-pe	PWM5: PWM output or pulse input 5 UART3_TxD: UART 3 transmitting data SCLK_RSTN: AIC9 I2S system clock output or AC97 reset output PE5: GPIO group E bit 5	VDDIO
PWM6 PD10	IO IO	W13	8mA, pullup-pe	PWM6: PWM output or pulse input 6 PD10: GPIO group D bit 10	VDDIO
PWM7 PD11	IO IO	P12	8mA, pullup-pe	PWM7: PWM output or pulse input 7 PD11: GPIO group D bit 11	VDDIO
UART3_RxD BCLK EPD_PWR4 PD12	I IO O IO	G20	8mA, pulldown-pe	UART3_RxD: UART 3 Receiving data BCLK: AIC AC97 bit clock/I2S unified or DAC bit clock EPD_PWR6: EPD power control bit 4 PD12: GPIO group D bit 12	VDDIO
LRCLK EPD_PWR5 PD13	IO O IO	H19	8mA, pulldown-pe	LRCLK: AIC AC97 frame SYNC/I2S unified or DAC Left/Right clock EPD_PWR6: EPD power control bit 5 PD13: GPIO group D bit 13	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AIC_SDATI EPD_PWR6 PE6	I O IO	H16	8mA, pullup-pe	AIC_SDATI: AIC AC97/I2S serial data input EPD_PWR6: EPD power control bit 6 PE6: GPIO group E bit 6	VDDIO
AIC_SDATO EPD_PWR7 PE7	O O IO	G21	8mA, pulldown-pe	AIC_SDATO: AIC AC97/I2S serial data output or SPDIF output EPD_PWR6: EPD power control bit 7 PE7: GPIO group E bit 7	VDDIO
UART3_CTS_ BCLK_AD PE8	I IO IO	J17	8mA, pullup-pe	UART3_CTS_: UART 3 CTS_ input BCLK_AD: AIC I2S ADC bit clock PE8: GPIO group E bit 8	VDDIO
UART3_RTS_ LRCLK_AD PE9	O IO O	H20	8mA, pullup-pe, rst-pe	UART3_RTS_: UART 3 RTS_ output LRCLK_AD: AIC I2S ADC Left/Right clock PE9: GPIO group E bit 9	VDDIO
SDATO1 PE11	O IO	J16	8mA, pullup-pe	SDATO1: AIC I2S serial data output 1 for AIC0 PE11: GPIO group E bit 11	VDDIO
SDATO2 PE12	O IO	H21	8mA, pullup-pe	SDATO2: AIC I2S serial data output 2 for AIC0 PE12: GPIO group E bit 12	VDDIO
SDATO3 PE13	O IO	K16	8mA, pullup-pe	SDATO3: AIC I2S serial data output 3 for AIC0 PE13: GPIO group E bit 13	VDDIO

2.5.8 System/JTAG/UART3/OTG/GPIO

Table 2-16 GPIO Pins (5, GPIO PF18~22)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PF18	IO	J19	8mA, pullup-pe	PF18: GPIO group F bit 18	VDDIO
PF19	IO	AA21	8mA, pulldown-pe	PF19: GPIO group F bit 19	VDDIO
PF20	IO	U19	8mA, pulldown-pe	PF20: GPIO group F bit 20	VDDIO
PF21	IO	K17	8mA, pullup-pe	PF21: GPIO group F bit 21	VDDIO
PF22	IO	V19	8mA, pulldown-pe	PF22: GPIO group F bit 22	VDDIO

Table 2-17 JTAG/UART3/PS2 Pins (5, GPIO PA30~31 are used to control)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST_	I	U15	Schmitt, pull-down	TRST_: JTAG reset	VDDIO
TCK UART3_RTS_ PS2_MCLK	I O IO	P13	8mA, Schmitt, pulldown-pe, rst-pe	TCK: JTAG clock UART3_RTS_: UART 3 RTS_output PS2_MCLK: PS/2 mouse clock PA30 is used to select between JTAG and PS2, PA31 is used to select between JTAG and UART and control the pull-down enable	VDDIO
TMS UART3_CTS_ PS2_MDATA	I I IO	U13	8mA, Schmitt, pullup-pe, rst-pe	TMS: JTAG mode select UART3_CTS_: UART 3 CTS_input PS2_MDATA: PS/2 mouse data PA30 is used to select between JTAG and PS2, PA31 is used to select between JTAG and UART and control the pull-down enable	VDDIO
TDI UART3_RxD PS2_KCLK	I I IO	P14	8mA, Schmitt, pullup-pe, rst-pe	TDI: JTAG serial data input UART3_RxD: UART 3 Receiving data PS2_KCLK: PS/2 keyboard clock PA30 is used to select between JTAG and PS2, PA31 is used to select between JTAG and UART and control the pull-down enable	VDDIO
TDO UART3_TxD PS2_KDATA	O O IO	U14	8mA, Schmitt, pullup-pe, rst-pe	TDO: JTAG serial data output UART3_TxD: UART 3 transmitting data PS2_KDATA: PS/2 keyboard data PA30 is used to select between JTAG and PS2, PA31 is used to select between JTAG and UART and control the pull-down enable	VDDIO

Table 2-18 System Pins (3, all GPIO shared: PD17~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PD17 (BOOT_SEL0)	I IO	T14	8mA, pullup-pe	PD17: GPIO group D bit 17 It is taken as BOOT select bit 0 by Boot ROM code	VDDIO
PD18 (BOOT_SEL1)	I IO	T15	8mA, pullup-pe	PD18: GPIO group D bit 18 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO
PD19 (BOOT_SEL2)	I IO	T13	8mA, pullup-pe	PD19: GPIO group D bit 19 It is taken as BOOT select bit 2 by Boot ROM code	VDDIO

Table 2-19 USB OTG Digital Pins (1, all GPIO shared: PE10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DRVVBUS PE10	O IO	U6	8mA, pulldown-pe, rst-pe	DRVVBUS: USB OTG VBUS driver control signal PE10: GPIO group E bit 10	VDDIO

Table 2-20 EXCLK output Pins (1, all GPIO shared: PD15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLKO PD15	O IO	W6	8mA, pulldown-pe, rst-pe	EXCLKO: output external clock PD15: GPIO group D bit 15	VDDIO

2.5.9 Digital power/ground

Table 2-21 IO/Core power supplies for FBGA-379 package (51)

Pin Names	IO	Loc	Pin Description	Power
VDDmem	P	F6 G6 F7 F8 F9 F10 F12 F13 F14 F15	VDDmem: 10 IO digital power for DDR, 1.8V~2.5V	-
VSSmem	P	H8 J8 K8 H9 H10 H11 H12 H13 H14 J14 G16	VSSmem: 11 IO digital ground for DDR, 0V	-
VDDIO _n	P	K6	VDDIO _n : (or VDDIO _{nand}) 1 IO digital power for NAND power domain, 1.8V~3.3V	-
VDDIO	P	P11 N12 M13 N13	VDDIO: 4 IO digital power for none DDR/NAND, 3.3V	-
VSS	P	J9 K9 L9 K10 L10 M10 N10 K11 L11 M11 N11 K12 L12 M12 L13	VSS: 15 IO digital ground for none DDR and CORE digital ground, 0V	-
VDDcore	P	L8 M9 N9 J10 J11 J12 J13 K13 K14 L14	VDDcore: 10 CORE digital power, 1.2V	-

2.5.10 Analog

Table 2-22 Audio CODEC Pins (19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AOHPL	AO	Y17		AOHPL: Left headphone out	AVD _{CDC}
AOHPR	AO	AA17		AOHPR: Right headphone out	AVD _{CDC}
AOHPM	AO	W16		AOHPM: Headphone common mode output	AVD _{CDC}
AOHPMS	AI	Y16		AOHPMS: Headphone common mode sense input	AVD _{CDC}
AOLP	AO	Y15		AOLP: Line out positive	AVD _{CDC}
AOLN	AO	AA16		AOLN: Line out negative	AVD _{CDC}
MICP1	AI	U17		MICP1: Microphone 1 input or input positive	AVD _{CDC}
MICN1	AI	V18		MICN1: Microphone 1 input negative	AVD _{CDC}
MICP2	AI	AA19		MICP2: Microphone 2 input positive	AVD _{CDC}
MICN2	AI	Y19		MICN2: Microphone 2 input negative	AVD _{CDC}
MICBIAS	AO	W19		MICBIAS: Microphone bias	AVD _{CDC}
AIL	AI	Y20		AIL: Left line input	AVD _{CDC}
AIR	AI	AA20		AIR: Right line input	AVD _{CDC}
VCAP	AO	Y18		VCAP: Voltage Reference Output. An electrolytic capacitor more than 10 μ F in parallel with a 0.1 μ F ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise?	AVD _{CDC}
HPSENSE	AI	V16		HPSENSE: Sense of headphone jack insertion	AVD _{CDC}
AVDCDC	P	W18		AVDCDC: CODEC analog power, 2.5V	-
AVSCDC	P	V17		AVSCDC: CODEC analog ground	-
AVDHP	P	AA18		AVDHP: Headphone amplifier power, 2.5V	-
AVSHP	P	W17		AVSHP: Headphone amplifier ground	-

Table 2-23 USB 2.0 OTG, USB 1.1 host (10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
OTG_DP	AIO	Y14		OTG_DP: USB OTG data plus	AVD _{OTG}
OTG_DM	AIO	AA14		OTG_DM: USB OTG data minus	AVD _{OTG}
VBUS	AIO	W15		VBUS: USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin	AVD _{OTG}
OTG_ID	AI	V15		OTG_ID: USB mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDOTG25.	AVD _{OTG}
TXR_RKL	AIO	W14		TXR_RKL: Transmitter resistor tune. It connects to an external resistor of 44.2 Ω with 1% tolerance to analog ground AVSOTG25, that adjusts the USB 2.0 high-speed source impedance	AVD _{OTG}
UHC_DP	AIO	AA3		USB_DP: USB 1.1 host data plus	AVD _{USB}
UHC_DM	AIO	Y4		USB_DM: USB 1.1 host data minus	AVD _{USB}
AVDUSB	P	AA15		AVDUSB: USB 1.1 host & USB OTG analog power, 3.3V	-
AVDOTG25	P	Y13		AVDOTG25: USB OTG analog power, 2.5V	-
AVSUSB	P	V14		AVSUSB: USB 1.1 host & USB OTG analog ground	-

Table 2-24 SAR ADC Pins (9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
XP_BR	AIO	AA10		XP_BR: Touch screen input, X+ for 4-wire, bottom-right for 5-wire, or ADC general purpose input	AVD _{AD}
XN_TL	AIO	Y12		XN_TL: Touch screen input, X- for 4-wire, top-left for 5-wire, or ADC general purpose input	AVD _{AD}
YP_TR	AIO	Y10		YP_TR: Touch screen input Y+ for 4-wire, top-right for 5-wire, or ADC general purpose input	AVD _{AD}
YN_BL	AIO	AA12		YN_BL: Touch screen input Y- for 4-wire, bottom-left for 5-wire, or ADC general purpose input	AVD _{AD}
WIPER	AIO	AA13		WIPER: Top sheet connection for 5-wire touch screen or ADC general purpose input	AVD _{AD}
AUX	AI	W11		AUX: ADC general purpose input	AVD _{AD}
VBAT	AI	W12		VBAT: Battery voltage input with external resistance divider or ADC general purpose input	1.2V
AVDAD	P	AA11		AVDAD: ADC analog power, 3.3 V	-
AVSAD	P	Y11		AVDAD: ADC analog ground	-

Table 2-25 EFUSE Pins (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AVDEFUSE	P	U3		AVDEFUSE: EFUSE programming power, 0V/2.5V	AVD _{AD}

Table 2-26 Video DAC Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LUMA	AO	V3		LUMA: DAC analog output for CVBS or luminance of S-Video	AVD _{DA}
AVDDA	P	Y1		AVDDA: Power supply for LUMA and CHROMA output, 3.3 V (IO1:AVD33R, IO2:AVD33G, IO3:AVDD, VDWELL)	-
AVSDA	P	W2		AVSDA: Ground for LUMA and CHROMA output (IO1/IO2: AVS33R, AVS33G, AVSS, VSSUB)	-
REXT	AO	U4		REXT: For external resistor. $REXT(ohm) = VREFIN(V) * 7.31 / I_{OFS}(A)$	AVD _{DA}

Table 2-27 LVDS Pins (14)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LVDS_CKP LCD_VSYN	AO O	R21		LVDS_CKP: LVDS CLK output positive for LCD LCD_VSYN: LCD frame clock/Vertical sync	AVD _{LVDS}
LVDS_CKN LCD_HSYN	AO O	P20		LVDS_CKN: LVDS CLK output negative for LCD LCD_HSYN: LCD line clock/horizontal sync	AVD _{LVDS}
LVDS_D0P LCD_G1	AO O	R20		LVDS_D0P: LVDS date channel 0 output positive for LCD LCD_G1: LCD Green data bit 1	AVD _{LVDS}
LVDS_D0N LCD_DE	AO O	T21		LVDS_D0N: LVDS date channel 0 output negative for LCD LCD_DE: STN AC bias drive/non-STN data enable	AVD _{LVDS}
LVDS_D1P LCD_G3	AO O	T20		LVDS_D1P: LVDS date channel 1 output positive for LCD LCD_G3: LCD Green data bit 3	AVD _{LVDS}
LVDS_D1N LCD_G2	AO O	U21		LVDS_D1N: LVDS date channel 1 output negative for LCD LCD_G3: LCD Green data bit 2	AVD _{LVDS}

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LVDS_D2P LCD_G5	AO O	U20		LVDS_D2P: LVDS data channel 2 output positive for LCD LCD_G4: LCD Green data bit 5	AVD _{LVDS}
LVDS_D2N LCD_G4	AO O	V21		LVDS_D2N: LVDS data channel 2 output negative for LCD LCD_G5: LCD Green data bit 4	AVD _{LVDS}
LVDS_D3P LCD_G7	AO O	V20		LVDS_D3P: LVDS data channel 3 output positive for LCD LCD_G6: LCD Green data bit 7	AVD _{LVDS}
LVDS_D3N LCD_G6	AO O	W21		LVDS_D3N: LVDS data channel 3 output negative for LCD LCD_G7: LCD Green data bit 6	AVD _{LVDS}
AVDLVDS12	P	P21		AVDLVDS12: Power supply for LVDS output, 1.2 V	AVD _{LVDS}
AVSLVDS12	P	N20		AVSLVDS12: Ground for LVDS output 1.2V power	AVD _{LVDS}
AVDLVDS	P	Y21		AVDLVDS: Power supply for LVDS output, 3.3 V	-
AVSLVDS	P	W20		AVSLVDS: Ground for LVDS output	-

Table 2-28 CPM Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK	AI	AA4	2~30 MHz Oscillator, OSC on/off	EXCLK: OSC input or 12MHz clock input	VDDIO
XCLK	AO	Y5		XCLK: OSC output	VDDIO
AVDPLL	P	AA1		AVDPLL: PLL analog power, 1.2V	-
AVSPLL	P	Y2		AVSPLL: PLL analog ground	-

Table 2-29 RTC Pins (9, 2 with GPIO input: PA30, PD14)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	Y3	32768Hz Oscillator	RTCLK: OSC input	VDD _{RTC}
XRTCLK	AO	AA2		XRTCLK: OSC output or 32768Hz clock input	VDD _{RTC}
PWRON	O	V5	8mA	PWRON: Power on/off control of main power	VDD _{RTC}
CLK32K PD14	O IO	U5	8mA, pullup-pe	32768Hz clock output PD14: GPIO group D bit 14. When main power down, this pin is controlled by RTC register: CLK32K or PD14, pull-up enable/disable, input/output if it is PD14, 0/1 if it is PD14 output	VDD _{RTC}
WKUP PA30	I I	V4	Schmitt	WKUP: Wakeup signal after main power down PA30: GPIO group A bit 30, input/interrupt only	VDD _{RTC}
PPRST_	I	W3	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDD _{RTC}
VDDRTC	P	W4		VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down	-
LDO_CAP	AIO	W5		LDO_CAP: Capacitor pin for RTC LDO	
TEST_E	I	N6	Schmitt, pull-down	TEST_E: Manufacture test enable, program readable	VDD _{RTC}

NOTES:

- 1 The meaning of phases in IO cell characteristics are:
 - a Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.
 - b Output, Single-end: output and single-ended DDR IO are used.
 - c Output, Differential: output and differential signal DDR IO are used.
 - d Bi-dir, Differential: bi-direction and differential signal DDR IO are used.

- e 8/16mA out: The IO cell's output driving strength is about 8/16mA.
 - f Pull-up: The IO cell contains a pull-up resistor.
 - g Pull-down: The IO cell contains a pull-down resistor.
 - h Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
 - i Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.
 - j rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull disabled
 - k Schmitt: The IO cell is Schmitt trig input.
- 2 All GPIO shared pins are reset to GPIO input.
- 3 These IOs are 5V input tolerance.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDmem power supplies voltage			V
VDDIO power supplies voltage			V
VDDIOOn power supplies voltage			V
VDDcore power supplies voltage			V
AVDPLL power supplies voltage			V
AVDEFUSE power supplies voltage			V
VDDRTC power supplies voltage			V
AVDOTG25 power supplies voltage			V
AVDUSB power supplies voltage			V
AVDAD power supplies voltage			V
AVDDA power supplies voltage			V
AVDCDC power supplies voltage			V
AVDHP power supplies voltage			V
AVDLVDS12 power supplies voltage			V
AVDLVDS power supplies voltage			V
Input voltage to VDDmem supplied non-supply pins			V
Input voltage to VDDIO supplied non-supply pins with 5V tolerance			V
Input voltage to VDDIO supplied non-supply pins without 5V tolerance			V
Input voltage to VDDIOOn supplied non-supply pins			V
Input voltage to VDDRTC supplied non-supply pins			V
Input voltage to AVDCDC supplied non-supply pins			V
Input voltage to AVDOTG25 supplied non-supply pins			V
Input voltage to AVDUSB supplied non-supply pins			V
Input voltage to AVDAD supplied non-supply pins			V
Input voltage to AVDDA supplied non-supply pins			V
Output voltage from VDDmem supplied non-supply pins			V
Output voltage from VDDIO supplied non-supply pins			V
Output voltage from VDDIOOn supplied non-supply pins			V

Output voltage from VDDRTC supplied non-supply pins			V
Output voltage from AVDOTG25 supplied non-supply pins			V
Output voltage from AVDUSB supplied non-supply pins			V
Output voltage from AVDAD supplied non-supply pins			V
Output voltage from AVDDA supplied non-supply pins			V
Output voltage from AVDCDC supplied non-supply pins			V
Output voltage from AVDLVDS supplied non-supply pins			V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
V_{MEM}	VDDmem voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
	VDDmem voltage for SSTL2 (DDR)	2.3	2.5	2.7	V
	VDDmem voltage for LPDDR	1.7	1.8	1.9	V
V_{IO}	VDDIO voltage	1.62	–	3.63	V
V_{ION}	VDDION voltage	1.62	–	3.63	V
V_{CORE}	VDDcore voltage	1.08	1.2	1.40	V
V_{PLL}	AVDPLL analog voltage	1.08	1.2	1.40	V
V_{EFUSE}	AVDEFUSE voltage	2.25	2.5	2.75	V
V_{RTC}	VDDRTC voltage	2.5	–	3.6	V
V_{OTG25}	AVDOTG25 voltage	2.25	2.5	2.75	V
V_{USB}	AVDUSB voltage	3.0	–	3.6	V
V_{ADC}	AVDAD voltage	3.0	3.3	3.6	V
V_{DAC}	AVDDA voltage	3.0	3.3	3.6	V
V_{CDC}	AVDCDC voltage	2.25	2.5	2.75	V
V_{HP}	AVDHP voltage	2.25	2.5	2.75	V
V_{LVDS12}	AVDLVDS12 voltage	1.08	1.2	1.40	V
V_{LVDS}	AVDLVDS voltage	3.0	3.3	3.6	V

Table 3-3 Recommended operating conditions for VDDmem supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{I18}	Input voltage for DDR2/LPDDR applications	0		1.9	V
V_{O18}	Output voltage for DDR2/LPDDR applications	0		1.9	V
V_{I25}	Input voltage for DDR application	0		2.7	V
V_{O25}	Output voltage for DDR application	0		2.7	V

Table 3-4 Recommended operating conditions for VDDIO/VDDION/VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	1.17		3.6	V
V_{IL18}	Input low voltage for 1.8V I/O application	–0.3		0.63	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7		3.6	V
V_{IL25}	Input low voltage for 2.5V I/O application	–0.3		0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2		3.6	V
V_{IL33}	Input low voltage for 3.3V I/O application	–0.3		0.8	V

Table 3-5 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T _A	Ambient temperature	0		85	°C

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-6 DC characteristics for VDDmem supplied pins in DDR2 application

Symbol	Parameter	Min	Typical	Max	Unit
V_{REFMEM}	Reference voltage supply	0.49	0.5	0.51	V_{MEM}
V_{TT}	Terminal Voltage	$V_{REFMEM} - 0.4$	V_{REFMEM}	$V_{REFMEM} + 0.4$	V
V_{IH}	DC input logic high	$V_{REFMEM} + 0.125$		$V_{MEM} + 0.3$	V
V_{IL}	DC input logic low	-0.3		$V_{REFMEM} - 0.125$	V
V_{IN}	DC input signal voltage	-0.3		$V_{MEM} + 0.3$	V
V_{ID}	DC differential input voltage	0.25		$V_{MEM} + 0.6$	V
I_L	Leakage current			± 0.2	μA

Table 3-7 DC characteristics for VDDmem supplied pins in DDR2 application

(Full driving strength case)

Symbol	Parameter	Condition	Typical	Unit
I_{OH}	Minimum DC source current of output driver	$V_{OH} = V_{MEM}(\text{Min}) - 0.28V$	-13.4	mA
I_{OL}	Minimum DC sink current of output driver	$V_{OL} = 0.28V$ and $V_{MEM} = 1.7V$	13.4	mA
RT	Terminal resistor		25	Ω
RS	Series resistor		20	Ω

Table 3-8 DC characteristics for VDDmem supplied pins in DDR2 application

(Half driving strength case)

Symbol	Parameter	Condition	Typical	Unit
I_{OH}	Minimum DC source current of output driver	$V_{OH} = V_{MEM}(\text{Min}) - 0.28V$	-6.7	mA
I_{OL}	Minimum DC sink current of output driver	$V_{OL} = 0.28V$ and $V_{MEM} = 1.7V$	6.7	mA
RT	Terminal resistor		50	Ω
RS	Series resistor		20	Ω

Table 3-9 DC characteristics for VDDmem supplied pins in DDR application

Symbol	Parameter	Min	Typical	Max	Unit
V_{REFMEM}	Reference voltage supply	0.49	0.5	0.51	V_{MEM}
V_{TT}	Terminal Voltage	$V_{REFMEM} - 0.4$	V_{REFMEM}	$V_{REFMEM} + 0.4$	V
V_{IH}	DC input logic high	$V_{REFMEM} + 0.15$		$V_{MEM} + 0.3$	V
V_{IL}	DC input logic low	-0.3		$V_{REFMEM} - 0.15$	V
V_{IN}	DC input signal voltage	-0.3		$V_{MEM} + 0.3$	V
V_{ID}	DC differential input voltage	0.3		$V_{MEM} + 0.6$	V
I_L	Leakage current			± 0.2	μA

Table 3-10 DC characteristics for VDDmem supplied pins in DDR application (Class I)

Symbol	Parameter	Condition	Typical	Unit
I_{OH}	Minimum DC source current of output driver	$V_{OH} = 1.7V$	-8.1	mA
I_{OL}	Minimum DC sink current of output driver	$V_{OL} = 0.56$	8.1	mA
RT	Terminal resistor		50	Ω
RS	Series resistor		25	Ω

Table 3-11 DC characteristics for VDDmem supplied pins in DDR application (Class II)

Symbol	Parameter	Condition	Typical	Unit
I_{OH}	Minimum DC source current of output driver	$V_{OH} = 1.7V$	-16.2	mA
I_{OL}	Minimum DC sink current of output driver	$V_{OL} = 0.56$	16.2	mA
RT	Terminal resistor		25	Ω
RS	Series resistor		25	Ω

Table 3-12 DC characteristics for VDDmem supplied pins in LPDDR application

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH}	DC input high voltage	$0.7 * V_{MEM}$		$V_{MEM} + 0.3$	V
V_{IL}	DC input low voltage	-0.3		$0.3 * V_{MEM}$	V
V_{OH}	DC output high voltage ($I_{OH} = -0.1mA$)	$0.9 * V_{MEM}$			V
V_{OL}	DC output low voltage ($I_{OH} = 0.1mA$)			$0.1 * V_{MEM}$	V
I_L	Leakage current			± 0.2	μA

Table 3-13 DC characteristics for VDDIO/VDDIO_n/VDDR_{TC} supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	0.79	0.86	0.94	V
V_{T+}	Schmitt trig low to high threshold point	0.95	1.06	1.16	V
V_{T-}	Schmitt trig high to low threshold point	0.58	0.69	0.79	V
V_{TPU}	Threshold point with pull-up resistor enabled	0.79	0.86	0.94	V

V _{TPD}	Threshold point with pull-down resistor enabled		0.79	0.86	0.94	V
V _{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.95	1.06	1.16	V
V _{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.58	0.68	0.78	V
V _{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.96	1.07	1.17	V
V _{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.59	0.69	0.79	V
I _L	Input Leakage Current @ V _I =1.8V or 0V				±10	µA
I _{OZ}	Tri-State output leakage current @ V _I =1.8V or 0V				±10	µA
R _{PU}	Pull-up Resistor		66	114	211	kΩ
R _{PD}	Pull-down Resistor		58	103	204	kΩ
V _{OL}	Output low voltage				0.45	V
V _{OH}	Output high voltage		1.35			V
I _{OL}	Low level output current @ V _{OL} (max)	8mA	5.3	9.8	15.8	mA
		16mA	10.8	19.7	31.8	mA
I _{OH}	High level output current @ V _{OH} (min)	8mA	3.3	8.3	16.6	mA
		16mA	6.6	16.5	33.2	mA

Table 3-14 DC characteristics for VDDIO/VDDIO_{on}/VDDR_{TC} supplied pins for 2.5V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.06	1.17	1.27	V
V_{T+}	Schmitt trig low to high threshold point	1.27	1.40	1.50	V
V_{T-}	Schmitt trig high to low threshold point	0.86	0.98	1.09	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.05	1.16	1.25	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.06	1.17	1.27	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.27	1.39	1.48	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.85	0.97	1.08	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.27	1.41	1.50	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	0.88	0.99	1.10	V
I_L	Input Leakage Current @ $V_I=1.8V$ or $0V$			± 10	μA
I_{OZ}	Tri-State output leakage current @ $V_I=1.8V$ or $0V$			± 10	μA
R_{PU}	Pull-up Resistor	43	69	120	k Ω
R_{PD}	Pull-down Resistor	41	66	124	k Ω
V_{OL}	Output low voltage			0.7	V
V_{OH}	Output high voltage	1.7			V

I_{OL}	Low level output current @ $V_{OL}(\max)$	8mA	11.6	19.4	28.4	mA
		16mA	23.3	39.1	57.2	mA
I_{OH}	High level output current @ $V_{OH}(\min)$	8mA	9.3	19.4	34.6	mA
		16mA	18.6	38.7	69.2	mA

Table 3-15 DC characteristics for VDDIO/VDDIO_n/VDDR_{TC} supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V _T	Threshold point		1.39	1.50	1.65	V
V _{T+}	Schmitt trig low to high threshold point		1.62	1.75	1.90	V
V _{T-}	Schmitt trig high to low threshold point		1.18	1.29	1.44	V
V _{TPU}	Threshold point with pull-up resistor enabled		1.36	1.48	1.64	V
V _{TPD}	Threshold point with pull-down resistor enabled		1.40	1.52	1.66	V
V _{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.62	1.75	1.89	V
V _{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.16	1.28	1.43	V
V _{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.64	1.77	1.91	V
V _{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.19	1.31	1.45	V
I _L	Input Leakage Current @ V _I =1.8V or 0V				±10	µA
I _{OZ}	Tri-State output leakage current @ V _I =1.8V or 0V				±10	µA
R _{PU}	Pull-up Resistor		34	51	81	kΩ
R _{PD}	Pull-down Resistor		35	51	88	kΩ
V _{OL}	Output low voltage				0.4	V
V _{OH}	Output high voltage		2.4			V
I _{OL}	Low level output current @ V _{OL} (max)	8mA	10.0	15.2	20.2	mA
		16mA	20.2	30.6	40.6	mA
I _{OH}	High level output current @ V _{OH} (min)	8mA	13.9	28.0	48.2	mA
		16mA	27.8	56.0	96.3	mA

3.4 Power On, Reset and BOOT

3.4.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the JZ4770 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-16 gives the timing parameters. Following are the names of the power.

- VDDRTC
- AVDAUD: AVDCDC, AVDHP
- VDD12: all 1.2V power supplies, include VDDCORE, AVDPLL, AVDLVDS12
- VDD: all other digital IO, include DDR power supplies: VDDMEM, VDDIO, VDDIO_n
- AVD: all other analog power supplies: AVDAD, AVDDA, AVDOTG25, AVDUSB, AVDLVDS
- AVDEFUSE

Table 3-16 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t _{R_VDDRTC}	VDDRTC rise time ^[1]	0	5	ms
t _{R_VDD}	VDD rise time ^[1]	0	5	ms
t _{D_VDD}	Delay between VDDRTC arriving 50% (or 90%) to VDD33 arriving 50% (or 90%)	0	–	ms
t _{R_VDD12}	VDD12 rise time ^[1]	0	5	ms
t _{D_VDD12}	Delay between VDD arriving 50% (or 90%) to VDD12 arriving 50% (or 90%)	–1	1	ms
t _{R_AVDAUD}	AVDAUD rise time ^[1]	0	5	ms
t _{D_AVDAUD}	Delay between VDD12 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0.01	1	ms
t _{R_AVD}	AVD rise time ^[1]	0	5	ms
t _{D_AVDA}	Delay between VDD arriving 50% to AVD arriving 50%	–1	1	ms
t _{D_PPRST_}	Delay between VDDAUD stable and PPRST_ deasserted	0	–	ms ^[2]
t _{D_VPEFUSE}	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

- 1 The power rise time is defined as 10% to 90%.
- 2 The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

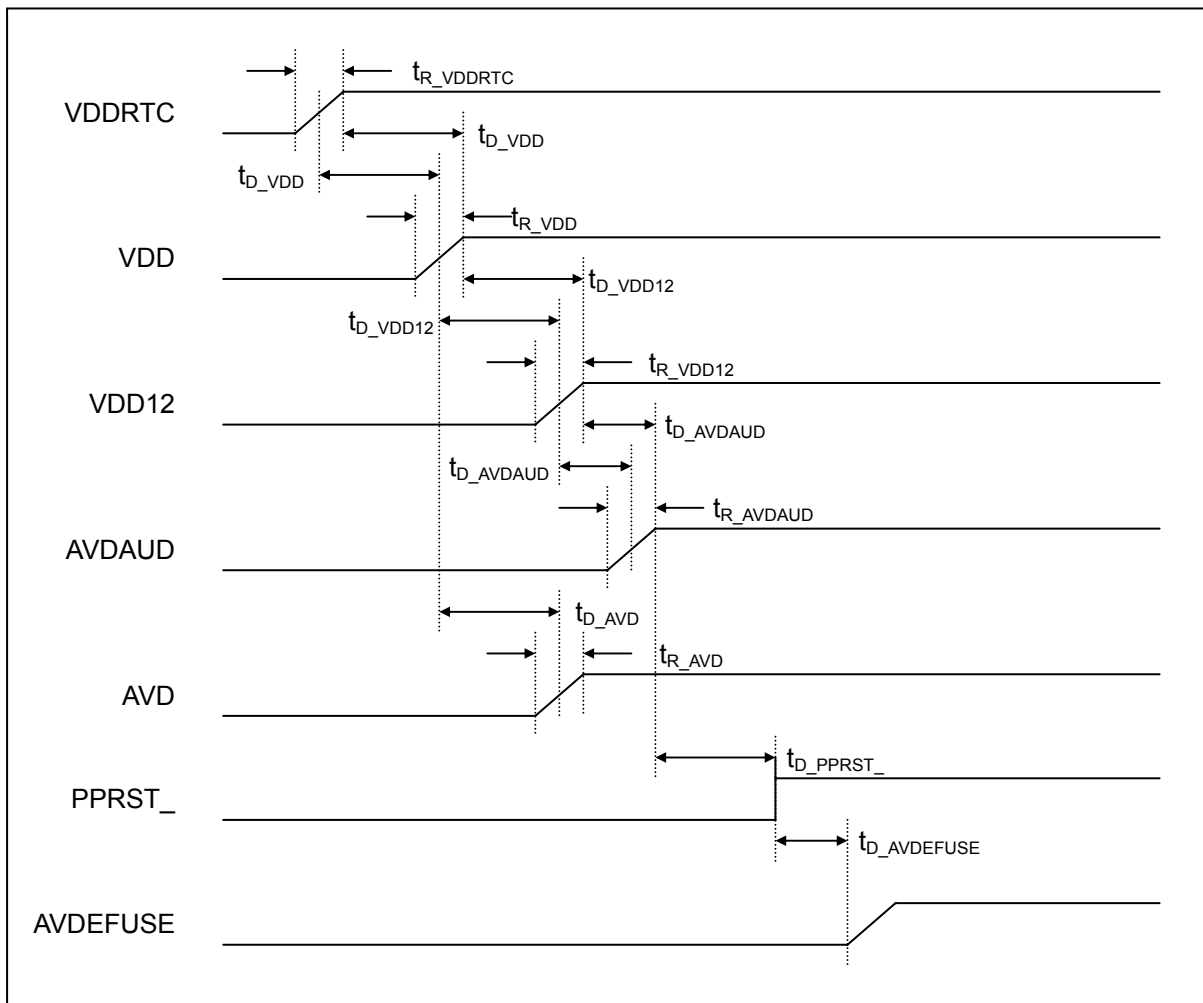


Figure 3-1 Power-On Timing Diagram

3.4.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.

This reset is triggered when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.

This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.

This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is

recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description ^{[1][2]}” for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs and the video DAC are put in suspend mode.

3.4.3 BOOT

JZ4770 supports 6 different boot sources depending on BOOT_SEL0, BOOT_SEL1 and BOOT_SEL2 pins values. Table 3-17 lists them.

Table 3-17 Boot from 3 boot sources

BOOT_SEL2	BOOT_SEL1	BOOT_SEL0	Boot From
1	1	1	NAND flash at CS1
1	0	0	SD card: MSC0
1	0	1	SPI: SPI0/CE0
0	1	1	NOR flash at CS4
1	1	0	USB2.0 OTG as device with EXCLK = 12MHz
0	0	0	iNAND: at MSC0
0	0	1	USB2.0 OTG as device with EXCLK = 26MHz
0	1	0	USB2.0 OTG as device with EXCLK = 19.2MHz

The boot procedure is showed in the following flow chart:

- In case of NAND/SDcard/iNAND/SPI boot, if it fails, enter USB boot.
- In case of USB boot, if it cannot connect to USB host within 10 seconds, restart the boot procedure.
- In case of NOR boot, if it fails, restart the boot procedure.
- If the boot procedure has been repeated more than 10 times, enter hibernating mode.

