F1C500s Datasheet

Revision 1.0

Nov.05, 2015

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Revision History

Revision	Date	Description
V1.0	Nov.05,2015	Initial Release Version

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1.Overview

The F1C500s processor is based on the ARM9 CPU architecture with a high degree of functional integration, which targeted for smart automotive applications. F1C500s supports 2 channels TV-IN, 1 channel CSI, and combined with powerful video encoding capability, which can easily achieve HD driving record . To reduce the BOM costs, F1C500s built-in DDR1 memory, and it is packed with SD/MMC,USB2.0,TWI,SPI,UART,I2S/PCM interfaces to meet the flexible peripheral configuration requirements of automotive system.F1C500s perfectly supports various applications of mainstream operating systems such as Andriod, Linux,etc.F1C500s outperforms competitors in terms of its powerful performance, flexible scalability and cost-efficiency.

Applications:

- Digital Video Record
- Audio playback

2. Features

2.1. CPU Architecture

The F1C500s platform is based on ARM9 CPU architecture.

- Five-stage pipeline architecture
- Support 16KByte D-Cache
- Support 32KByte I-Cache

2.2. Memory Subsystem

This section consists of internal memory and external memory:

- **Boot ROM**
- **SDRAM**
- **SD/MMC Interface**

Boot ROM

- Internal memory
- On-Chip ROM boot loader
- Support system boot from SPI Nor/Nand Flash, and SD/TF card
- Support system code download through USB OTG

SDRAM

- SIP DDR1

SD/MMC Interface

- External memory
- Support secure digital memory protocol commands (up to SD2.0)
- Support secure digital I/O protocol commands (up to SDIO2.0)
- Support multimedia card protocol commands (up to eMMC4.41)
- Support one SD (Verson1.0 to 2.0) or MMC (version 3.3 to eMMC4.41)
- Support hardware CRC generation and error detection
- Support host pull-up control
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65535 bytes
- Support descriptor-based internal DMA controller
- Internal 128 bytes FIFO for data transfer
- Support 3.3V IO pad

2.3. System Peripheral

This section includes:

- **Timer**
- **INTC**
- **CCU**
- **DMA**
- **PWM**

Timer

- Three timers

- Support watchdog reset
- Support audio and video synchronize counter

INTC
- Support up to 64 interrupts
- Support 4-level priority
- Support interrupt mask
- Support interrupt fast forcing
- Support one external interrupt

CCU
- Support 6 PLLs
- Control of clock generation, division, distribution and gating
- Control of device software reset

DMA
- Support Normal DMA and Dedicated DMA
- Support two kinds of interrupt
- Support hardware continuous transfer mode

PWM
- Support two PWM outputs
- Support cycle mode and pulse mode
- Support 24MHz maximum output frequency

2.4. Display Subsystem

This section includes:
- **Display Engine**
- **Display Output**

Display Engine
- Support four layers overlay, each layer size up to 2048x2048 pixels
- Support Alpha blending / color key
- Support multi-format input formats
  - 1/2/4/8/16/32 bpp color
  - YUV444/YUV422/YUV420/YUV411
- Support hardware cursor
- Support scaling function for one layer
  - ARGB8888/YUV444/YUV420/YUV422/YUV411
  - Input and output size up to 1280x720 pixels
  - Resize ratio from 1/16X to 32X
  - 4-tap 32-phase anti-aliasing filter in horizontal and vertical direction
  - Scaler supports write-back to memory function

Display Output
- LCD RGB interface, TTL interface, up to 1280x720@60fps
- LCD Serial RGB interface, CCIR656 interface, up to 720x576@60fps
- LCD i8080 interface with 18/16/9/8 bit, up to 800x480@60fps
- LCD Dither function, support RGB666/RGB565 interface
- TV CVBS output, support NTSC/PAL, with auto plug detecting

2.5. Video Engine

- Support H.264 BP/MP/HP up to 1280x720@30fps decoding

- Support format MPEG1 and MPEG2 up to 1280x720@30fps decoding
- Support format MPEG4 SP/ASP GMC and H.263 including Sorenson Spark up to 1280x720@30fps decoding
- Support MJPEG encode up to 1280x720@30fps, 1920x1080@25fps
- Support JPEG encode size up to 8192 x 8192
- Support JPEG decode size up to 16384 x 16384

2.6. Image Subsystem

This section includes:

- **CSI**
- **CVBS Input**

CSI

- Support 8-bit CMOS-sensor interface
- Support YUV camera up to 5Mega pixel
- Support CCIR656 protocol for NTSC and PAL

CVBS Input

- Support NTSC/PAL
- Support 3D comb filter
- Support two TV CVBS channels:TVIN0,TVIN1

2.7. Audio Subsystem

Audio Codec

- Two audio digital-to-analog(DAC) channels
- Stereo capless headphone drivers:
  - Up to 100dB DR
  - Supports DAC Sample Rates from 8KHz to 192KHz
- Support analog/ digital volume control
- Analog low-power loop from FM/ line-in /microphone to headphone outputs
- Three audio inputs:
  - One microphone input
  - Stereo FM left/right input
  - One Line-in input
- One audio analog-to-digital(ADC) channel
  - 96dB SNR@A-weight
  - Supports ADC Sample Rates from 8KHz to 48KHz
  - Support Auto Gain Control(AGC)

2.8. System Peripherals

This section includes:

- **USB 2.0 OTG**
- **KEYADC**
- **TP**
- **Digital Audio Interface**
- **UART**
- **SPI**
- **TWI**
- **IR**
- **RSB™**

- OWA

USB 2.0 OTG

- Support AMBA AHB Slave mode
- Support the Host Negotiation Protocol (HNP) and the Session Request Protocol (SRP)
- Support the UTMI+ Level 3 interface . The 8-bit bidirectional data buses are used.
- 64-Byte Endpoint 0 for Control Transfer (Endpoint0)
- Support High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Support point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Include automatic ping capabilities
- Soft connect/disconnect function
- Perform all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Include interface to an external Dedicated Central DMA controller. Data is transferred through Special bus for saving AHB bus bandwidth
- Support industry-standard single port SRAM for USB Configurable Data FIFO. The size is 2048 byte with 32-bit word width. The RAM can be used by other modules when USB OTG disable

KEYADC

- 6-bit resolution
- Support hold key and general key
- Support single key and continuous key
- Sample rate up to 250Hz

TP

- 12-bit SAR type analog-to-digital converter
- 4-wire I/F
- Dual Touch Detect
- Touch-pressure measurement
- Sampling frequency: 2MHz
- Single-Ended conversion of touch screen inputs and ratio metric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change function

Digital Audio Interface

- I2S or PCM configured by software
- Master / Slave Mode operation configured by software
- I2S Audio data sample rate from 8KHz to 192KHz
- I2S Data format for standard I2S, Left Justified and Right Justified
- PCM supports linear sample (8-bits or 16-bits), 8-bits u-law and A-law commanded sample

UART

- Three UART controllers
- Compatible with industry-standard 16550 UARTs
- Support IRDA version 1.0 SIR protocol with maximum baud rate to 115200bps for all UARTs
- Support for word length from 5 to 8 bits,an optional parity bit, and 1,1.5 or 2 stop bits
- Programmable parity(even,odd and no parity)
- 32-Bytes Transmit and receive data FIFOs
- Support DMA controller interface
- Software/ Hardware Flow Control
- Interrupt support for FIFOs, Status Change

SPI

- Two SPI controllers

- Full-duplex synchronous serial interface
- Master/Slave configurable
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the chip select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable

TWI

- Three TWI controllers
- Software-programmable for Slave or Master
- Support repeated START signal
- Multi-master systems supported
- Allow 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and general call address detection
- Interrupt on address detection
- Support speeds up to 400Kbits/s (‘fast mode’)
- Allow operation from a wide range of input clock frequencies

IR

- Full physical layer implementation
- Support CIR for remote control
- 64x8bits FIFO for data buffer
- Programmable FIFO thresholds

RSB™

- Support speed up to 20MHz with ultra low power
- Support push-pull bus
- Support host mode
- Support programmable output delay of CD signal
- Support parity check for address and data transmission
- Support multi-devices

OWA

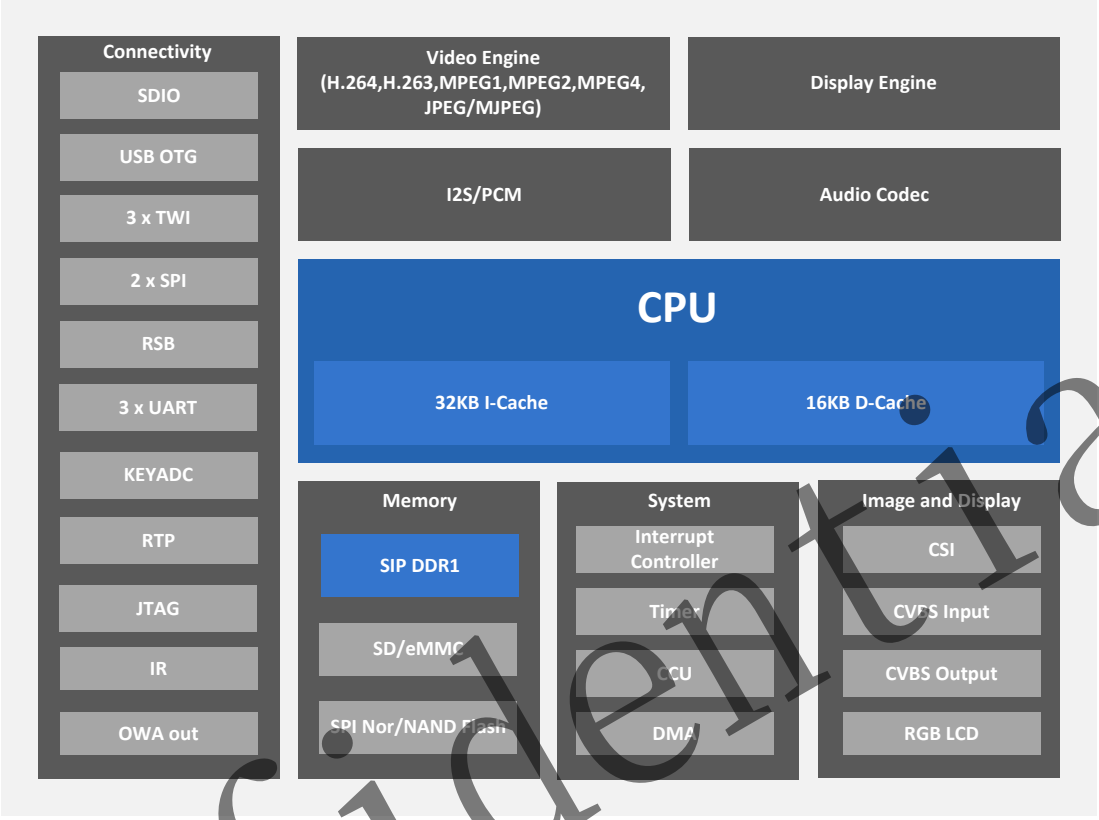
- EC-60958 transmitter and receiver functionality
- Support SPDIF Interface
- Support channel status capture on the receiver
- Support channel status insertion for the transmitter
- Support Parity checking on the receiver
- Support Parity generation on the transmitter
- One 32×24bits FIFO (TX) for audio data transfer
- Programmable FIFO thresholds
- Interrupt and DMA support

2.9. Package

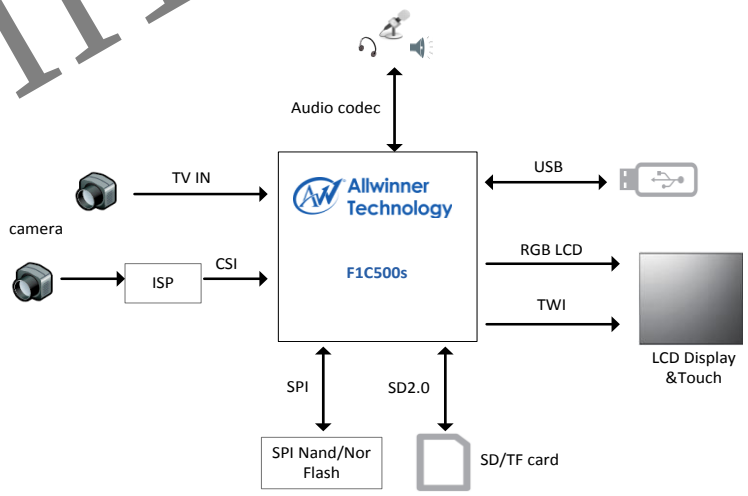
- QFN88,10 x 10mm

3. Block Diagram

The block diagram of F1C500s processor is as follows:



The typical application diagram of F1C500s is as follows:



4.Pin Description

4.1. Pin Characteristics

Following table describes the F1C500s pin characteristics from seven aspects: *BALL#, Pin Name, Default Function, Type, Reset* State, Default Pull Up/Down and Buffer Strength.

(1). ***Default function*** defines the default function of each pin, especially for pins with multiplexing functions;
(2). ***Pin types*** : O for output, I for input, I/O for input/output, A for analog, AI for analog input, AO for analog output, AI/O for analog input/output, OD for Open-Drain, P for power and G for ground;
(3). ***Reset state*** defines the state of the terminal at reset: Z for high-impedance.
(4). ***Default Pull up/down*** defines the presence of an internal pull up or pull down resistor. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;
(5). ***Buffer strength*** defines the driver strength of the associated output buffer. It is tested in the condition that VCC= 3.0V, strength=MAX;

Pin Num(1)	Pin Name	Default Function	Pin Type(2)	Reset State(3)	Default Pull Up/ Down(4)	Buffer Strength(5) (mA)
GPIOC						
59	PC0	GPIO	I/O	Disabled	-	-
60	PC1	GPIO	I/O	Disabled	Pull-up	-
61	PC2	GPIO	I/O	Disabled	-	-
62	PC3	GPIO	I/O	Disabled	-	-
GPIOD						
6	PD0	GPIO	I/O	Disabled	-	-
7	PD1	GPIO	I/O	Disabled	-	-
8	PD2	GPIO	I/O	Disabled	-	-
9	PD3	GPIO	I/O	Disabled	-	-
10	PD4	GPIO	I/O	Disabled	-	-
11	PD5	GPIO	I/O	Disabled	-	-
12	PD6	GPIO	I/O	Disabled	-	-
13	PD7	GPIO	I/O	Disabled	-	-
14	PD8	GPIO	I/O	Disabled	-	-
15	PD9	GPIO	I/O	Disabled	-	-
16	PD10	GPIO	I/O	Disabled	-	-
17	PD11	GPIO	I/O	Disabled	-	-
18	PD12	GPIO	I/O	Disabled	-	-
19	PD13	GPIO	I/O	Disabled	-	-
21	PD14	GPIO	I/O	Disabled	-	-
23	PD15	GPIO	I/O	Disabled	-	-
24	PD16	GPIO	I/O	Disabled	-	-
25	PD17	GPIO	I/O	Disabled	-	-
26	PD18	GPIO	I/O	Disabled	-	-
27	PD19	GPIO	I/O	Disabled	-	-
28	PD20	GPIO	I/O	Disabled	-	-
29	PD21	GPIO	I/O	Disabled	-	-
GPIOE						
49	PE0	GPIO	I/O	Disabled	-	-
48	PE1	GPIO	I/O	Disabled	-	-
47	PE2	GPIO	I/O	Disabled	-	-
46	PE3	GPIO	I/O	Disabled	-	-
45	PE4	GPIO	I/O	Disabled	-	-
44	PE5	GPIO	I/O	Disabled	-	-
43	PE6	GPIO	I/O	Disabled	-	-

42	PE7	GPIO	I/O	Disabled	-	-
41	PE8	GPIO	I/O	Disabled	-	-
40	PE9	GPIO	I/O	Disabled	-	-
39	PE10	GPIO	I/O	Disabled	-	-
38	PE11	GPIO	I/O	Disabled	-	-
37	NC	-	-	-	-	-
GPIOF						
58	PF0	GPIO	I/O	Disabled	-	-
57	PF1	GPIO	I/O	Disabled	-	-
56	PF2	GPIO	I/O	Disabled	-	-
55	PF3	GPIO	I/O	Disabled	-	-
54	PF4	GPIO	I/O	Disabled	-	-
53	PF5	GPIO	I/O	Disabled	-	-
USB						
67	UVCC	-	P	-	-	-
68	USB-DM	-	A	-	-	-
69	USB-DP	-	A	-	-	-
Audio Codec						
81	VRA1	-	A	-	-	-
83	VRA2	-	A	-	-	-
82	AGND	-	P	-	-	-
85	FMINR	-	A	-	-	-
84	FMINL	-	A	-	-	-
87	MICIN	-	A	-	-	-
86	LINL	-	A	-	-	-
88	HPR	-	A	-	-	-
1	HPL	-	A	-	-	-
3	HPCOM	-	A	-	-	-
4	HPVCC	-	P	-	-	-
2	HPCOMFB	-	A	-	-	-
80	AVCC	-	P	-	-	-
Touch Panel						
66	TPX1	-	A	-	-	-
65	TPX2	-	A	-	-	-
64	TPY1	-	A	-	-	-
63	TPY2	-	A	-	-	-
TV IN						
73	TV_VCC	-	P	-	-	-
74	TVGND	-	P	-	-	-
75	TV_VRN	-	A	-	-	-
76	TV_VRP	-	A	-	-	-
77	TVIN1	-	A	-	-	-
78	TVIN0	-	A	-	-	-
KEYADC						
79	LRADC0	-	A	-	-	-
TV OUT						
72	TVOUT	-	A	-	-	-
Clock						
52	HOSCO	-	A	-	-	-
51	HOSCI	-	A	-	-	-
Miscellaneous Signal						
70	RESET	-	I	-	-	-
SIP DDR1						
33	SVREF	-	P			
Power						
5,20,50	VCC-IO	-	P	-	-	-
30,31,32,34,36	VCC-DRAM	-	P	-	-	-
22,35,71	VDD-CORE	-	P	-	-	-

4.2. GPIO Multiplexing Functions

Following table provides a description of the GPIO multiplexing functions of F1C500s.

Port	Default Function	IO Type	Default IO State	Default Pull-up/ down	Multiplexing Function 2	Multiplexing Function 3	Multiplexing Function 4	Multiplexing Function 5	Multiplexing Function 6
GPIOA									
PA0	GPIO	A	DIS	Z	TPX1		DA_BCLK	UART1_RTS	SPI1_CS
PA1	GPIO	A	DIS	Z	TPX2		DA_LRCK	UART1_CTS	SPI1_MOSI
PA2	GPIO	A	DIS	Z	TPY1	PWM0	DA_IN	UART1_RX	SPI1_CLK
PA3	GPIO	A	DIS	Z	TPY2	IR_RX	DA_OUT	UART1_TX	SPI1_MISO
GPIOB									
PB3	GPIO	I/O	DIS	Z	DDR_REF_D	IR_RX			
GPIOC									
PC0	GPIO	I/O	DIS	Z	SPI0_CLK	SDC1_CLK			
PC1	GPIO	I/O	DIS	Pull-up	SPI0_CS	SDC1_CMD			
PC2	GPIO	I/O	DIS	Z	SPI0_MISO	SDC1_D0			
PC3	GPIO	I/O	DIS	Z	SPI0_MOSI	UART0_TX			
GPIOD									
PD0	GPIO	I/O	DIS	Z	LCD_D2	TWI0_SDA	RSB_SDA		EINTD0
PD1	GPIO	I/O	DIS	Z	LCD_D3	UART1_RTS			EINTD1
PD2	GPIO	I/O	DIS	Z	LCD_D4	UART1_CTS			EINTD2
PD3	GPIO	I/O	DIS	Z	LCD_D5	UART1_RX			EINTD3
PD4	GPIO	I/O	DIS	Z	LCD_D6	UART1_TX			EINTD4
PD5	GPIO	I/O	DIS	Z	LCD_D7	TWI1_SCK			EINTD5
PD6	GPIO	I/O	DIS	Z	LCD_D10	TWI1_SDA			EINTD6
PD7	GPIO	I/O	DIS	Z	LCD_D11	DA_MCLK			EINTD7
PD8	GPIO	I/O	DIS	Z	LCD_D12	DA_BCLK			EINTD8
PD9	GPIO	I/O	DIS	Z	LCD_D13	DA_LRCK			EINTD9
PD10	GPIO	I/O	DIS	Z	LCD_D14	DA_IN			EINTD10
PD11	GPIO	I/O	DIS	Z	LCD_D15	DA_OUT			EINTD11
PD12	GPIO	I/O	DIS	Z	LCD_D18	TWI0_SCK	RSB_SCK		EINTD12
PD13	GPIO	I/O	DIS	Z	LCD_D19	UART2_TX			EINTD13
PD14	GPIO	I/O	DIS	Z	LCD_D20	UART2_RX			EINTD14
PD15	GPIO	I/O	DIS	Z	LCD_D21	UART2_RTS	TWI2_SCK		EINTD15
PD16	GPIO	I/O	DIS	Z	LCD_D22	UART2_CTS	TWI2_SDA		EINTD16
PD17	GPIO	I/O	DIS	Z	LCD_D23	OWA_OUT			EINTD17
PD18	GPIO	I/O	DIS	Z	LCD_CLK	SPI0_CS			EINTD18
PD19	GPIO	I/O	DIS	Z	LCD_DE	SPI0_MOSI			EINTD19
PD20	GPIO	I/O	DIS	Z	LCD_HSYNC	SPI0_CLK			EINTD20
PD21	GPIO	I/O	DIS	Z	LCD_VSYNC	SPI0_MISO			EINTD21
GPIOE									
PE0	GPIO	I/O	DIS	Z	CSI_HSYNC	LCD_D0	TWI2_SCK	UART0_RX	EINTE0
PE1	GPIO	I/O	DIS	Z	CSI_VSYNC	LCD_D1	TWI2_SDA	UART0_TX	EINTE1
PE2	GPIO	I/O	DIS	Z	CSI_PCLK	LCD_D8	CLK_OUT		EINTE2
PE3	GPIO	I/O	DIS	Z	CSI_D0	LCD_D9	DA_BCLK	RSB_SCK	EINTE3
PE4	GPIO	I/O	DIS	Z	CSI_D1	LCD_D16	DA_LRCK	RSB_SDA	EINTE4
PE5	GPIO	I/O	DIS	Z	CSI_D2	LCD_D17	DA_IN		EINTE5
PE6	GPIO	I/O	DIS	Z	CSI_D3	PWM1	DA_OUT	OWA_OUT	EINTE6

PE7	GPIO	I/O	DIS	Z	CSI_D4	UART2_TX	SPI1_CS		EINTE7
PE8	GPIO	I/O	DIS	Z	CSI_D5	UART2_RX	SPI1_MOSI		EINTE8
PE9	GPIO	I/O	DIS	Z	CSI_D6	UART2_RTS	SPI1_CLK		EINTE9
PE10	GPIO	I/O	DIS	Z	CSI_D7	UART2_CTS	SPI1_MISO		EINTE10
PE11	GPIO	I/O	DIS	Z	CLK_OUT		IR_RX		EINTE11
GPIOF									
PF0	GPIO	I/O	DIS	Z	SDC0_D1	DBG_MS	IR_RX		EINTF0
PF1	GPIO	I/O	DIS	Z	SDC0_D0	DBG_DI			EINTF1
PF2	GPIO	I/O	DIS	Z	SDC0_CLK	UART0_RX			EINTF2
PF3	GPIO	I/O	DIS	Z	SDC0_CMD	DBG_DO			EINTF3
PF4	GPIO	I/O	DIS	Z	SDC0_D3	UART0_TX			EINTF4
PF5	GPIO	I/O	DIS	Z	SDC0_D2	DBG_CK	PWM1		EINTF5

4.3. Detailed Pin Description

Pin Name	Description	Type
GPIO		
PC[3:0]	Port C Bit[3:0]	I/O
PD[21:0]	Port D Bit[21:0]	I/O
PE[11:0]	Port E Bit[11:0]	I/O
PF[5:0]	Port F Bit[5:0]	I/O
USB		
USB-DM	USB DM Signal	A I/O
USB-DP	USB DP Signal	A I/O
UVCC	USB 3.3V power	P
Audio Codec		
HPL	Headphone Left Output	AO
HPR	Headphone Right Output	AO
HPCOM	Headphone Common Reference	AO
HPCOMFB	Headphone Common Reference Feedback Input	AI
HPVCC	Headphone Amplifier Power	P
FMINL	FM in Left Input	AI
FMINR	FM in Right Input	AI
LINEIN	Line in Input	AI
MICIN	Microphone Input	AI
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
AVCC	Analog Power	P
AGND	Analog Ground	G
Digital Audio		
DA_MCLK	Digital Audio Master Clock	O
DA_BCLK	Digital Audio sample rate Clock	I/O
DA_LRCK	Digital Audio Left & Right channel Clock	I/O

DA_IN	Digital Audio Data Out	I
DA_OUT	Digital Audio Data in	O
RSB		
RSB_SCK	RSB Clock	I/O
RSB_SDA	RSB Data	I/O
Touch Panel		
TPX1	Touch Panel X1 Input	AI
TPX2	Touch Panel X2 Input	AI
TPY1	Touch Panel Y1 Input	AI
TPY2	Touch Panel Y1 Input	AI
TV-Out		
TVOUT	TV CVBS Output	AO
TV-IN		
TVIN0	TV CVBS Input 0	AI
TVIN1	TV CVBS Input 1	AI
TVAVCC	TV Analog VCC for TVIN and TVOUT	P
TVAGND	TV Analog GND for TVIN and TVOUT	G
TVIN_VRP	TV Input Voltage Reference Positive	AI
TVIN_VRN	TV Input Voltage Reference Negative	AI
Clock		
HOSCI	24MHz Crystal Input	AI
HOSCO	24MHz Crystal Output	AO
Miscellaneous Signal		
RESET#	Chip Reset Signal	I
PWM[1:0]	Pulse Width Modulation Output	O
ADC		
LRADC0	ADC Input for Key	I
LCD		
LCD[7:2]	LCD Data Bus Bit[7:2]	O
LCD[15:10]	LCD Data Bus Bit[15:10]	O
LCD[23:18]	LCD Data Bus Bit[23:18]	O
LCD_CLK	LCD Clock	O
LCD_DE	LCD Data Enable	O
LCD_HSYNC	LCD Horizon Sync	O
LCD_VSYNC	LCD Vertical Sync	O
SPI(x=[1:0])		
SPIx_MOSI	SPI Master Output Slave Input	I/O
SPIx_MISO	SPI Master Input Slave Output	I/O
SPIx_CS	SPI Chip Select Signal	I/O
SPIx_CLK	SPI Clock	I/O
UART(x=[2:0])		

UARTx_TX	UART Data Transmit	O
UARTx_RX	UART Data Receive	I
UARTx_CTS	UART Clear to Send	I
UARTx_RTS	UART Request to Send	O
IR		
IR_RX	IR Receive Signal	I
CSI		
CSI_PCLK	CSI Pixel Clock signal	I
CSI_HSYNC	CSI Horizontal Synchronization Signal	I
CSI_VSYNC	CSI Vertical Synchronization Signal	I
CSI_D[7:0]	CSI Data Bit[7:0]	I
SDC		
SDC0_D[3:0]	SD/MMC/SDIO Data Bit[3:0]	I/O
SDC0_CLK	SD/MMC/SDIO Clock	O
SDC0_CMD	SD/MMC/SDIO Command	I/O
SDC1_D0	SD/MMC/SDIO Data Bit0	I/O
SDC1_CLK	SD/MMC/SDIO Clock	O
SDC1_CMD	SD/MMC/SDIO Command	I/O
TWI(x=[2:0])(Open-Drain)		
TWIx-SCK	TWI Clock	I/O
TWIx-SDA	TWI Data	I/O

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
T_{stg}	Storage Temperature	-65	150	°C
$I_{I/O}$	In/Out current for input and output	-40	40	mA
VCC-IO	Power Supply for I/O	-0.3	3.6	V
AVCC	Power Supply for Codec	-0.3	3.1	V
TV_AVCC	Power Supply for TV	-0.3	3.6	V
VDD-CORE	Power Supply for Internal Digital Logic	-0.3	1.3	V
UVCC	Power Supply for USB	-0.3	3.6	V
VCC-DRAM	Power Supply for DDR1	-0.3	2.7	V

5.2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_a	Ambient Operating Temperature[Commercial]	-20	-	85	°C
VCC-IO	Power Supply for I/O	3.0	3.3	3.6	V
AVCC	Power Supply for Codec	2.5	2.8	3.1	V
TV_AVCC	Power Supply for TV	3.0	3.3	3.6	V
VDD-CORE	Power Supply for Internal Digital Logic	1.0	1.1	1.2	V
UVCC	Power Supply for USB	3.0	3.3	3.6	V
VCC-DRAM	Power Supply for DDR1	2.3	2.5	2.7	V

5.3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7 * VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3 * VCC-IO	V
R_{PU}	Input pull-up resistance	50	100	150	KΩ
R_{PD}	Input pull-down resistance	50	100	150	KΩ
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO -0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA

C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.4. Oscillator Electrical Characteristics

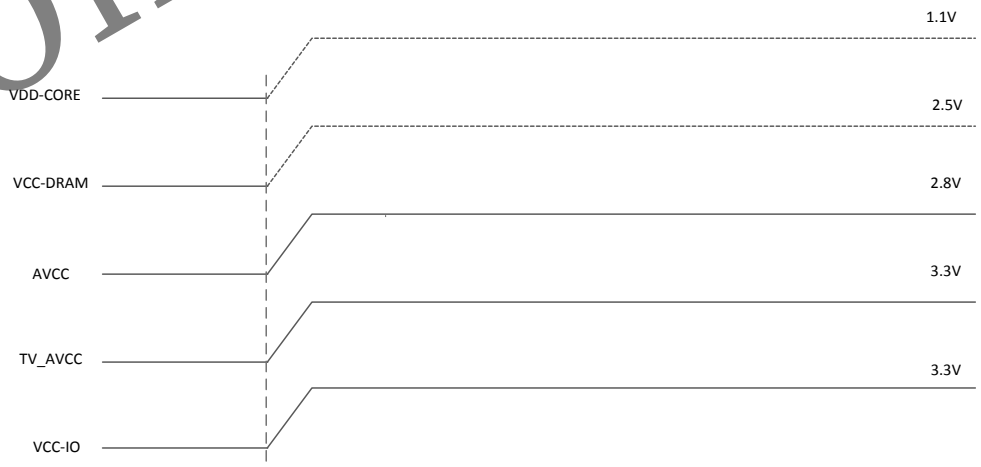
The 24.000MHz crystal is connected between the OSC24MI and OSC24MO.The following table lists the 24.000MHz crystal specifications.

Symbol	Parameter	Min	Typ	Max	Unit
$1/(t_{CPMAIN})$	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25°C	-50	-	50	ppm
	Oscillation Mode	Fundamental		-	
	Maximum Change Over Temperature Range	-50	-	50	ppm
P_{ON}	Drive Level	-	-	300	uW
C_L	Equivalent Load Capacitance	12	18	22	pF
R_S	Series Resistance(ESR)	-	25	-	Ω
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	5	6.5	7.5	pF
R_{BIAS}	Internal Bias Resistor	0.4	0.5	0.6	MΩ

5.5. Power Up/Down Sequence

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operations.

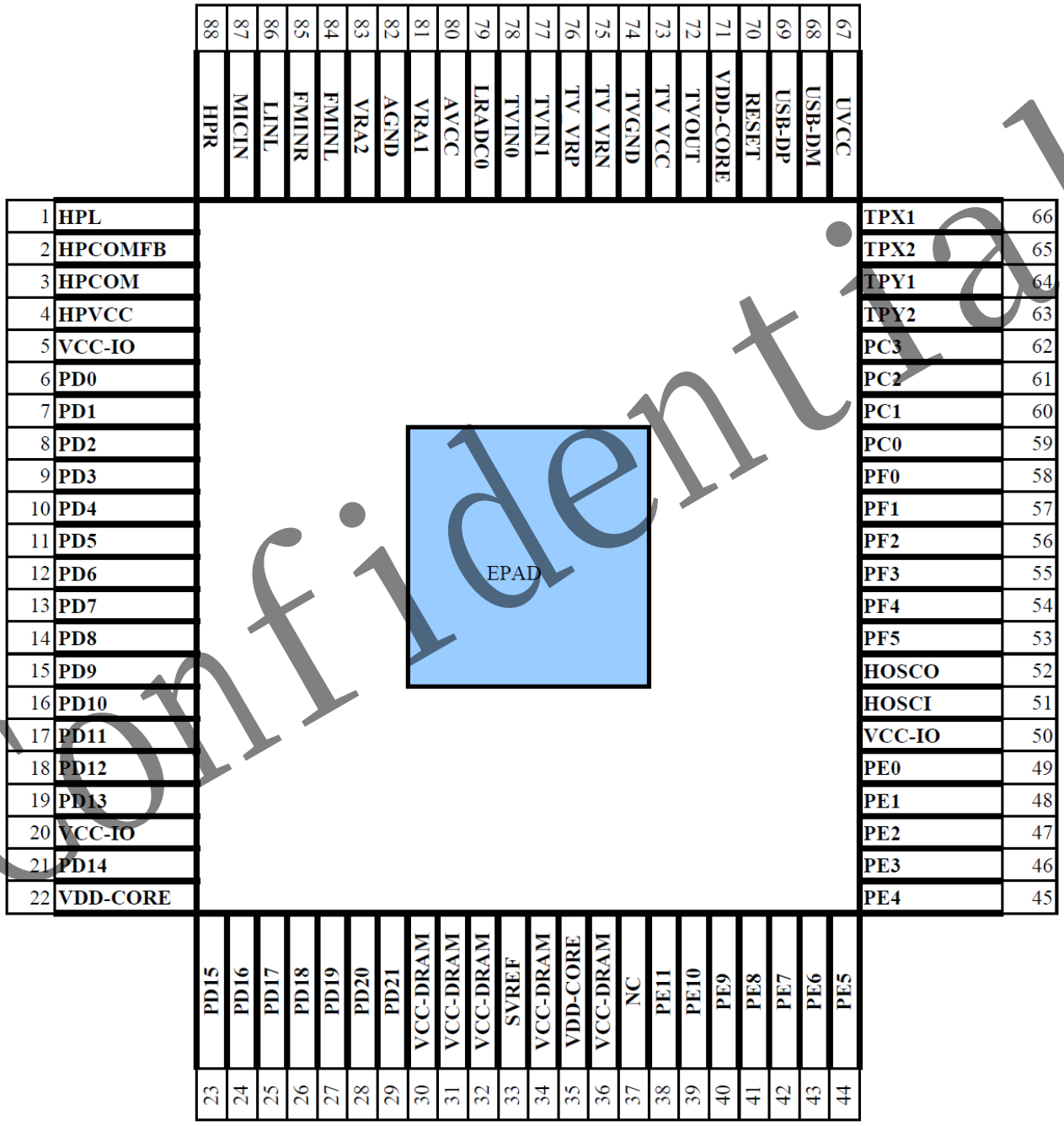
Power Up Sequence



No special restrictions for power down sequence.

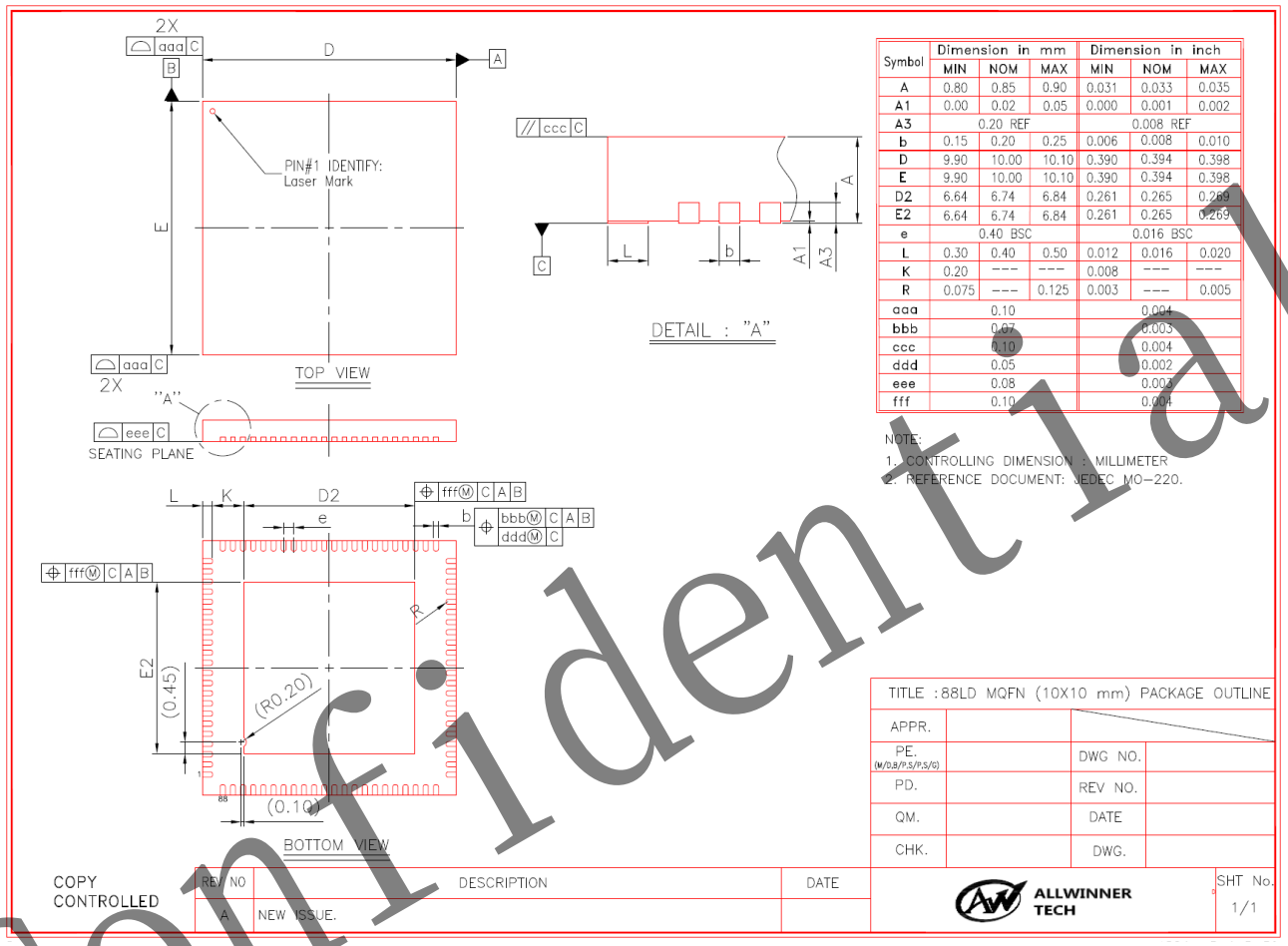
6. Pin Assignment

6.1. Pin Map



6.2. Package Dimension

The following figure shows the top, bottom, and side views of F1C500s package dimension.



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D2	6.64	6.74	6.84	0.261	0.265	0.269
E2	6.64	6.74	6.84	0.261	0.265	0.269
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	0.125	0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

