F1C100 Processer

Datasheet

V1.0

2011-3-31

1   Revision History

Version	Date	Section/ Page	Changes compared to previous issue
V1.0	2011-3-31		Initial version

Table of Contents

2 Description

The F1C100 processor is a highly integrated programmable platform for Media Application. The F1C100 processor contains a rich set of peripherals connected to the ARM926-EJS via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance. The general-purpose peripherals include functions such as USB HS/FS DRD, UART, SPI, TWI, LCD controller, TV encoder, SD/MMC I/F, SDRAM I/F, a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. In addition to these general-purpose peripherals, the processor contains high speed serial and parallel ports for interfacing to a variety of audio and video function.

3 Feature

The systems include the following feature:
- ARM926-EJS 16KB I-Cache/16KB D-Cache
- Support 16 bits SDR
- Two 32-bit Programmed Timers
- Enhanced 8-CH Direct-Memory-Access Controller
- Built in Pulse Width Modulator
- Built in USB 2.0 HS
- Built in Touch Panel Interface
- Built in Low Resolution A/D convertor
- On-chip Sigma-Delta A/D with SNR up to 95dB（A-Weight）
- On-chip Sigma-Delta D/A and PA with SNR up to 100dB（A-Weight）
- On-Chip ROM Boot loader
- Built in HDTV encoder
- Built in LCD controller
- Built in IrDA for remote control
- Built in audio codec for headphone and microphone application
- Support SLC/MLC NAND flash up to 64bits ECC
- Support SD/TF/MMC card
- Fully support PMU application
- Video Decoder Engine(all format up to 1280*720@30fps)
  - ◆ H.264
    Fully compatible with ISO-14496-10 in BP/MP/HP
    Supports CABAC/CAVLC
    Supports frame/field/MAFF structure
    Variable block size(16x16, 16x8, 8x16, 8x8, 8x4, 4x8 and 4x4)
  - ◆ MPEG-1
    Fully compatible with ISO/IEC 11172-2 Mpeg1 specification

        Support I, P, B, D pictures

◆ MPEG-2

        Fully compatible with ISO/IEC 13818-2 Mpeg2 specification in Main profile

        Support I, P, B pictures

        Support field coded picture and frame coded picture

◆ MPEG-4

        Fully compatible with ISO-14496-2 SP/ASP

        Supports GMC up to three wrapping points

        Supports H.264 baseline profile

        Supports Xvid

■ Package

- LQFP128

■ 3.3V for I/O, and 1.2V for Internal digital circuit

4 Functional Block Diagram

System Peripheral	ARM926-EJS I/D-Cache 16KB	Multi-Media
Timer		HD JPEG Decoder
PLL		Video Decoder
PWM		NTSC, PAL CVBS Out
DMA		
LRADC		

AHB/APB Bus

Peripheral Interface		Memory Subsystem
TWI		SRAM
SPI		ROM
UART		SDR
IR		NAND
PIO		
USB OTG	CCM	DE/TCON
SD/MMC		
Audio Codec	PMU	
Touch Panel		
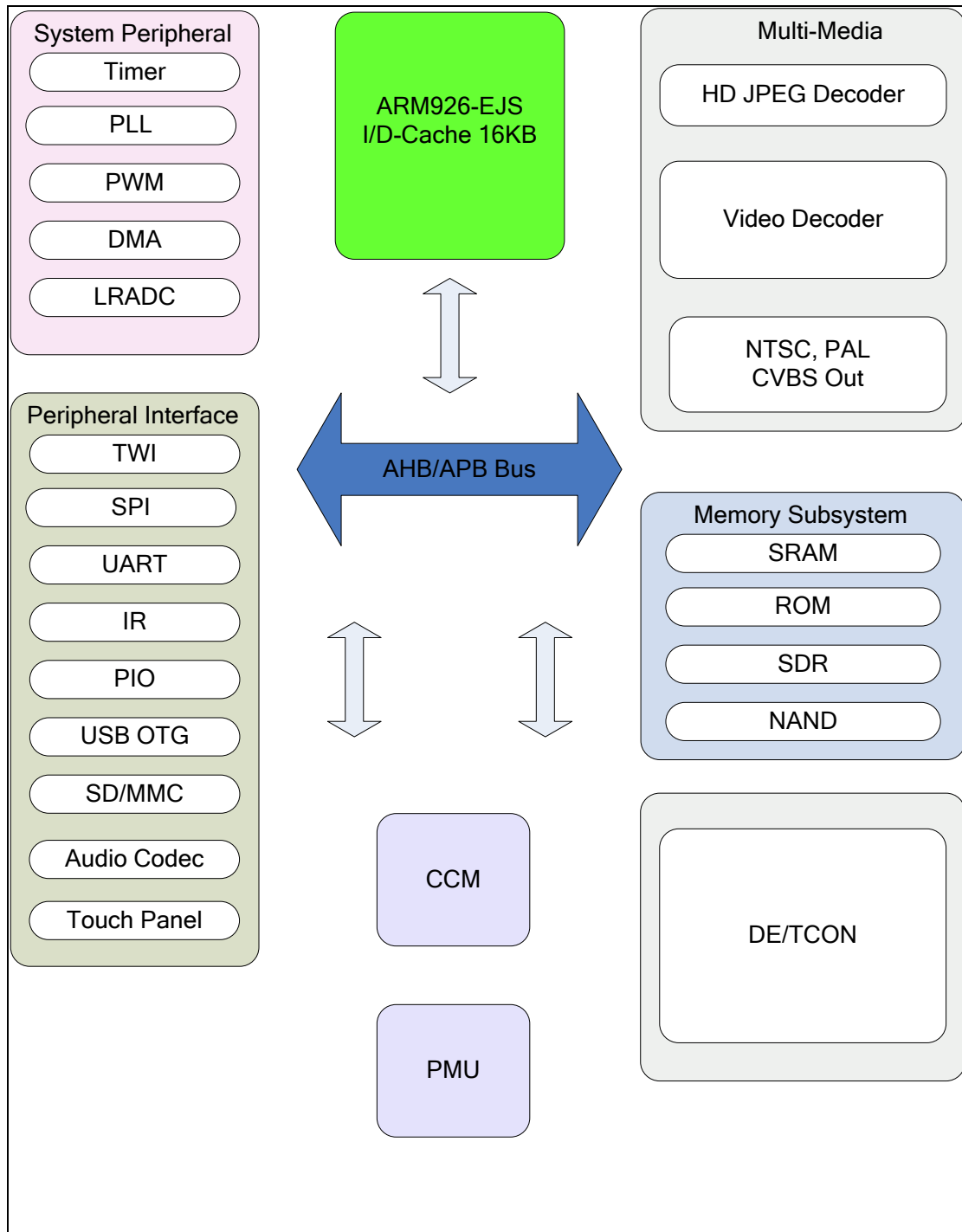
5 Pin Assignment
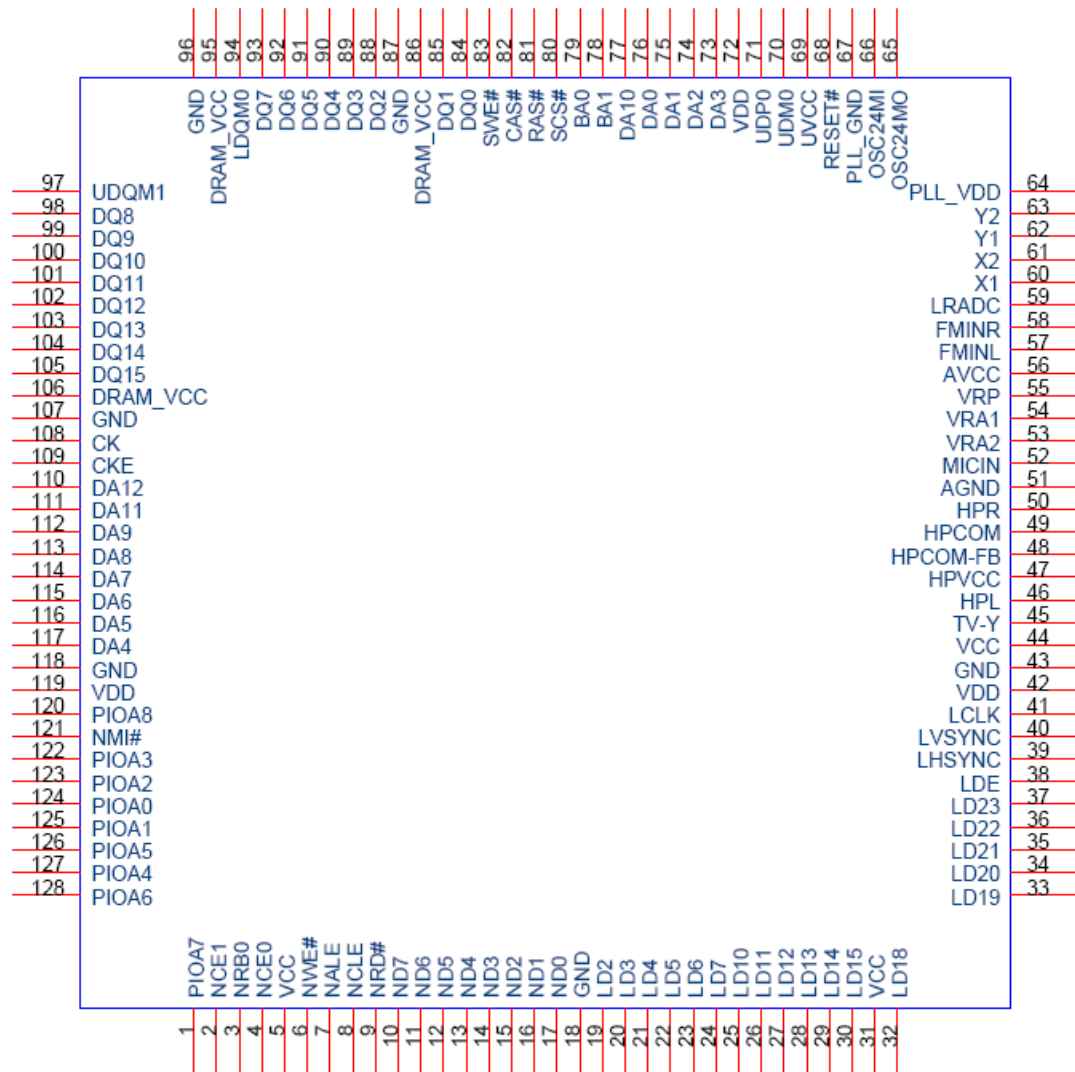
F1C100 Package Diagram

6 Pin Description

6.1 SDR Interface Pin

Pin Num	Pin Name	Type	Default Status	Description
108	CK	O		DRAM CK Clock
109	CKE	O		DRAM Clock Enable

80	SCS#	O		DRAM Chip Select
81	RAS#	O		DRAM Row Address Strobe
82	CAS#	O		DRAM Column Address Strobe
83	SWE#	O		DRAM Write Enable
79	BA0	O		DRAM Bank Address 0
78	BA1	O		DRAM Bank Address 1
84	DQ0	I/O		DRAM Data Bus Bit 0
85	DQ1	I/O		DRAM Data Bus Bit 1
88	DQ2	I/O		DRAM Data Bus Bit 2
89	DQ3	I/O		DRAM Data Bus Bit 3
90	DQ4	I/O		DRAM Data Bus Bit 4
91	DQ5	I/O		DRAM Data Bus Bit 5
92	DQ6	I/O		DRAM Data Bus Bit 6
93	DQ7	I/O		DRAM Data Bus Bit 7
98	DQ8	I/O		DRAM Data Bus Bit 8
99	DQ9	I/O		DRAM Data Bus Bit 9
100	DQ10	I/O		DRAM Data Bus Bit 10
101	DQ11	I/O		DRAM Data Bus Bit 11
102	DQ12	I/O		DRAM Data Bus Bit 12
103	DQ13	I/O		DRAM Data Bus Bit 13
104	DQ14	I/O		DRAM Data Bus Bit 14
105	DQ15	I/O		DRAM Data Bus Bit 15
94	DQM0	O		DRAM Input Data Mask for DQ0~DQ7
97	DQM1	O		DRAM Input Data Mask for DQ8~DQ15
76	DA0	O		DRAM Address Bit 0
75	DA1	O		DRAM Address Bit 1
74	DA2	O		DRAM Address Bit 2
73	DA3	O		DRAM Address Bit 3
117	DA4	O		DRAM Address Bit 4
116	DA5	O		DRAM Address Bit 5
115	DA6	O		DRAM Address Bit 6
114	DA7	O		DRAM Address Bit 7
113	DA8	O		DRAM Address Bit 8
112	DA9	O		DRAM Address Bit 9
77	DA10	O		DRAM Address Bit 10
111	DA11	O		DRAM Address Bit 11
110	DA12	O		DRAM Address Bit 12

6.2 NAND Flash Interface Pin

Pin Num	Pin Name	Type	Default Status	Description
6	NWE#	I/O		NAND Flash Write Enable
9	NRD#	I/O		NAND Flash Read Enable
7	ALE	I/O		NAND Flash Address Latch Enable
8	CLE	I/O		NAND Flash Command Latch Enable
4	NCE0#	I/O	pull-up	NAND Flash Chip Enable 0
2	NCE1#	I/O	pull-up	NAND Flash Chip Enable 1
3	NRB0#	I/O		NAND Flash Ready/ Busy 0
17	ND0	I/O		NAND Flash Data Bus Bit 0
16	ND1	I/O		NAND Flash Data Bus Bit 1
15	ND2	I/O		NAND Flash Data Bus Bit 2
14	ND3	I/O		NAND Flash Data Bus Bit 3
13	ND4	I/O		NAND Flash Data Bus Bit 4
12	ND5	I/O		NAND Flash Data Bus Bit 5
11	ND6	I/O		NAND Flash Data Bus Bit 6
10	ND7	I/O		NAND Flash Data Bus Bit 7

6.3 LCD Interface Pin

Pin Num	Pin Name	Type	Default Status	Description
19	LCDD2	I/O		LCD Data Bus Bit 2
20	LCDD3	I/O		LCD Data Bus Bit 3
21	LCDD4	I/O		LCD Data Bus Bit 4
22	LCDD5	I/O		LCD Data Bus Bit 5
23	LCDD6	I/O		LCD Data Bus Bit 6
24	LCDD7	I/O		LCD Data Bus Bit 7
25	LCDD10	I/O		LCD Data Bus Bit 10
26	LCDD11	I/O		LCD Data Bus Bit 11
27	LCDD12	I/O		LCD Data Bus Bit 12
28	LCDD13	I/O		LCD Data Bus Bit 13
29	LCDD14	I/O		LCD Data Bus Bit 14

30	LCDD15	I/O		LCD Data Bus Bit 15
32	LCDD18	I/O		LCD Data Bus Bit 18
33	LCDD19	I/O		LCD Data Bus Bit 19
34	LCDD20	I/O		LCD Data Bus Bit 20
35	LCDD21	I/O		LCD Data Bus Bit 21
36	LCDD22	I/O		LCD Data Bus Bit 22
37	LCDD23	I/O		LCD Data Bus Bit 23
41	LCDCLK	I/O	pull-up	LCD Clock
38	LCDDE	I/O	pull-down	LCD Data Enable
39	LCDHSYNC	I/O	pull-down	LCD Horizon Sync
40	LCDVSYNC	I/O	pull-down	LCD Vertical Sync

6.4 USB Interface Pin

Pin Num	Pin Name	Type	Default Status	Description
70	USBDM			USB DM signal
71	USBDP			USB DP signal
69	UVCC			USB 3.3V power

6.5 Touch Panel Interface Pin

Pin Num	Pin Name	Type	Default Status	Description
60	X1			Touch Panel X1 input
61	X2			Touch Panel X2 input
62	Y1			Touch Panel Y1 input
63	Y2			Touch Panel Y1 input

6.6 Audio Codec Interface Pin

Pin Num	Pin Name	Type	Default Status	Description
46	HPL			Headphone Left Channel Output
50	HPR			Headphone Right Channel Output
49	HPCOM			Headphone Common Mode
48	HPCOM-FB			Headphone Common Mode Feedback
47	HPVCC			Headphone 3.0V power bypass
57	FMINL			Line Input Left Channel
58	FMINR			Line Input Right Channel

52	MICINL			Microphone Left Channel Input

6.7 TV-Out Interface Pin

Pin Num	Pin Name	Type	Default Status	Description
45	TV-CVBS			TV CVBS DAC Output

6.8 Clock Pin

Pin Num	Pin Name	Type	Default Status	Description
66	X24M-IN			24MHz Crystal Input
65	X24M-OUT			24MHz Crystal Output
64	PLL-VDD			PLL power bypass
67	PLL-GND			PLL Analog ground

6.9 General Purpose IO Pin

Pin Num	Pin Name	Type	Default Status	Description
124	PIOA0	I/O	High-Z	GPIO Port A Bit 0
125	PIOA1	I/O	High-Z	GPIO Port A Bit 1
123	PIOA2	I/O	High-Z	GPIO Port A Bit 2
122	PIOA3	I/O	High-Z	GPIO Port A Bit 3
127	PIOA4	I/O	High-Z	GPIO Port A Bit 4
126	PIOA5	I/O	High-Z	GPIO Port A Bit 5
128	PIOA6	I/O	High-Z	GPIO Port A Bit 6
1	PIOA7	I/O	High-Z	GPIO Port A Bit 7
120	PIOA8	I/O	High-Z	GPIO Port A Bit 8

6.10   Miscellaneous Signal Pin

Pin Num	Pin Name	Type	Default Status	Description
121	NMI#			Not Mask Interrupt Input
68	RESET#		pull-up	Chip Reset Signal
55	VRP			Codec voltage3 bypass
54	VRA1			Codec voltage1 bypass
53	VRA2			Codec voltage2 bypass
59	LRADC			Low resolution ADC input for key

6.11 Power and Ground Pin

Pin Num	Pin Name	Type	Default Status	Description
5,31,44	VCC			IO VCC 3.3V Power
86,95,106	DRAM-VCC			DRAM VCC power
42,72,119	VDD			Core VDD 1.2V power
18,43,87,96, 107,118	GND			Core/ IO GND
56	AVCC			Analog 3.0V power
51	AGND			Analog GND

7 Power Domain

For the F1C100, it has a several power domains for different application.

Name	Power Range	Note
VCC	3.3V (3.0~3.6)	For IO
VDD	1.08~1.40V	For Core
PLL-VDD	1.25V	For 24MHz crystal /PLL
AVCC	3.0V	For analog module
UVCC	3.3V	For USB IO
DRAM-VCC	3.3V	For SDR DRAM

8 Module Description

8.1 Clock Control Module

8.1.1 CCM Overview
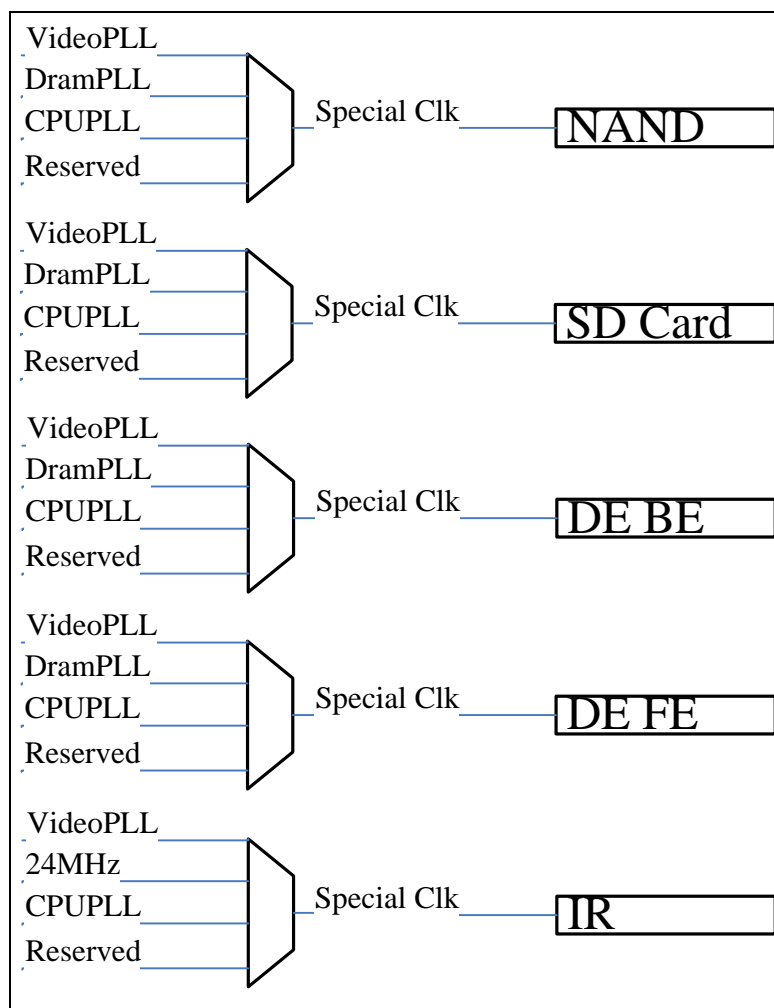
In the Soc, 6 PLL are built in.

- CPU PLL
- Display PLL(27MHz~330MHz)
- DRAM PLL(60MHz~400MHz)
- Audio PLL(24.576MHz or 22.5792MHz)
- Video Engine PLL(range: 30MHz~276MHz)
- USB PLL(fixed to 480MHz)

Only one external 24mhz oscillator is needed for SOC clock.

8.1.2 CCM Diagram
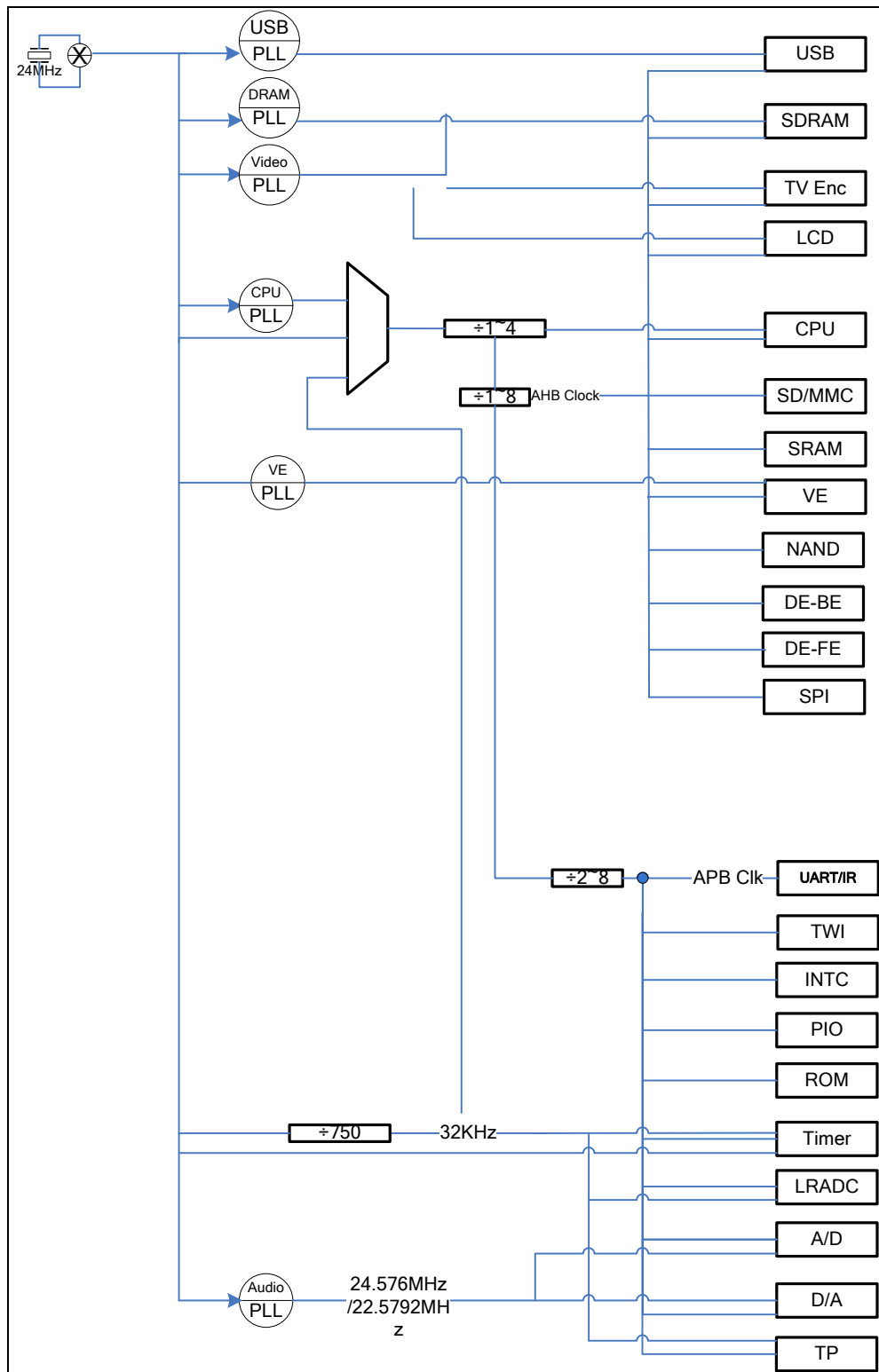
8.2 Interrupt Controller

8.2.1 Interrupt Overview

The interrupt controller has the following feature:

- Controls the nIRQ and FIQ of the Processor
- Sixty-three individually maskable interrupt sources
- One external NMI interrupt source
- 4-Level Priority Controller
- 4 External Sources of Edge-sensitive or Level-sensitive
- Fast Forcing

It provides handling of up to sixty-four interrupt sources. The 4-level Priority Controller allows the user to define the priority for each interrupt source, thus permitting higher priority interrupts to be serviced even if a lower priority interrupt is being treated. The fast forcing feature redirects any internal or external source to provide a fast interrupt rather than a normal interrupt.

8.2.2 Interrupt Diagram
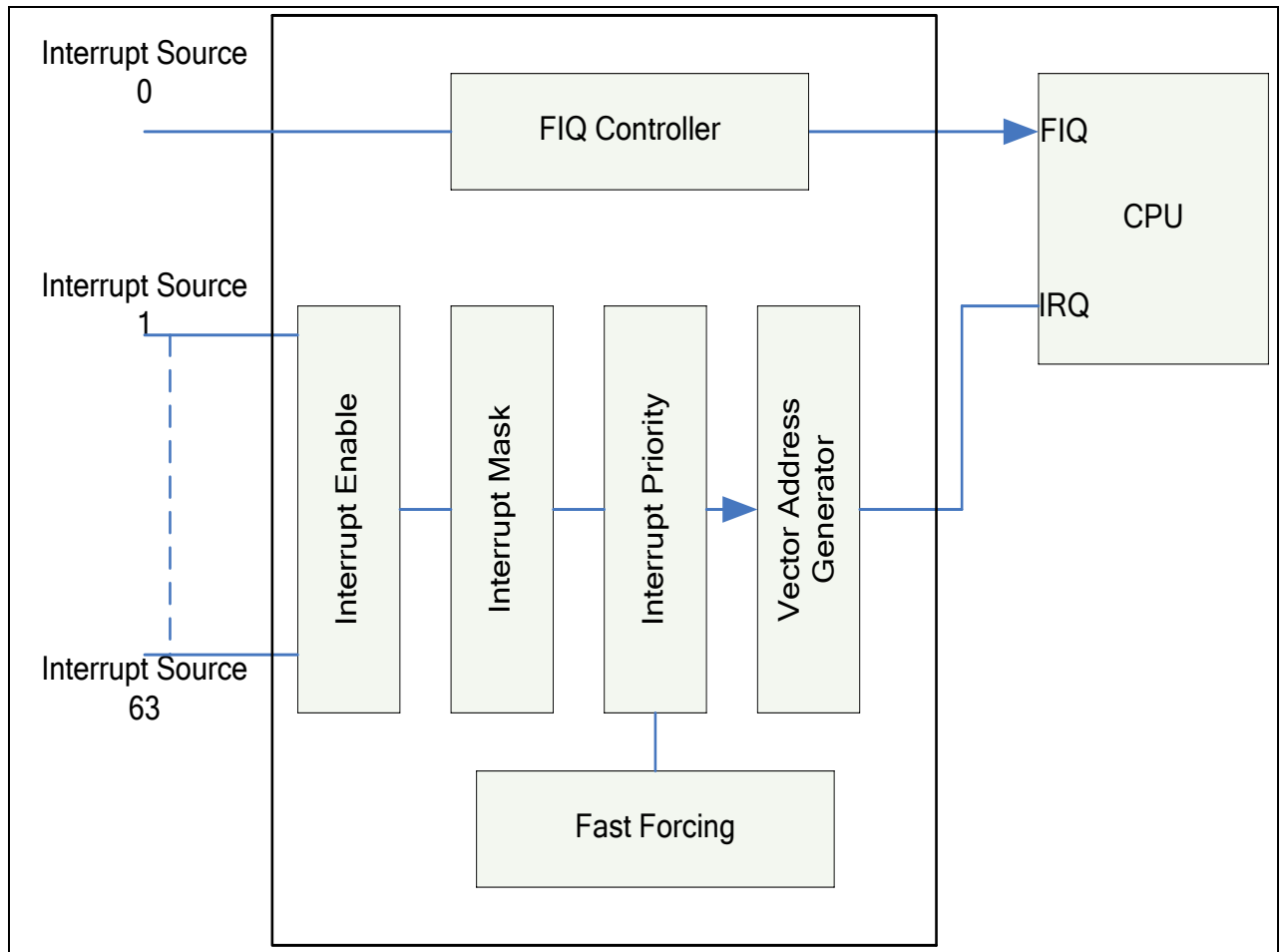
8.3 Timer

8.3.1 Timer Overview

 he SOC implements 2 timers.

Timer 0 can take their inputs from OSC24M crystal or CLK32K。 They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 32-bit programmable overflow counter and work in auto-reload mode or no-reload mode.
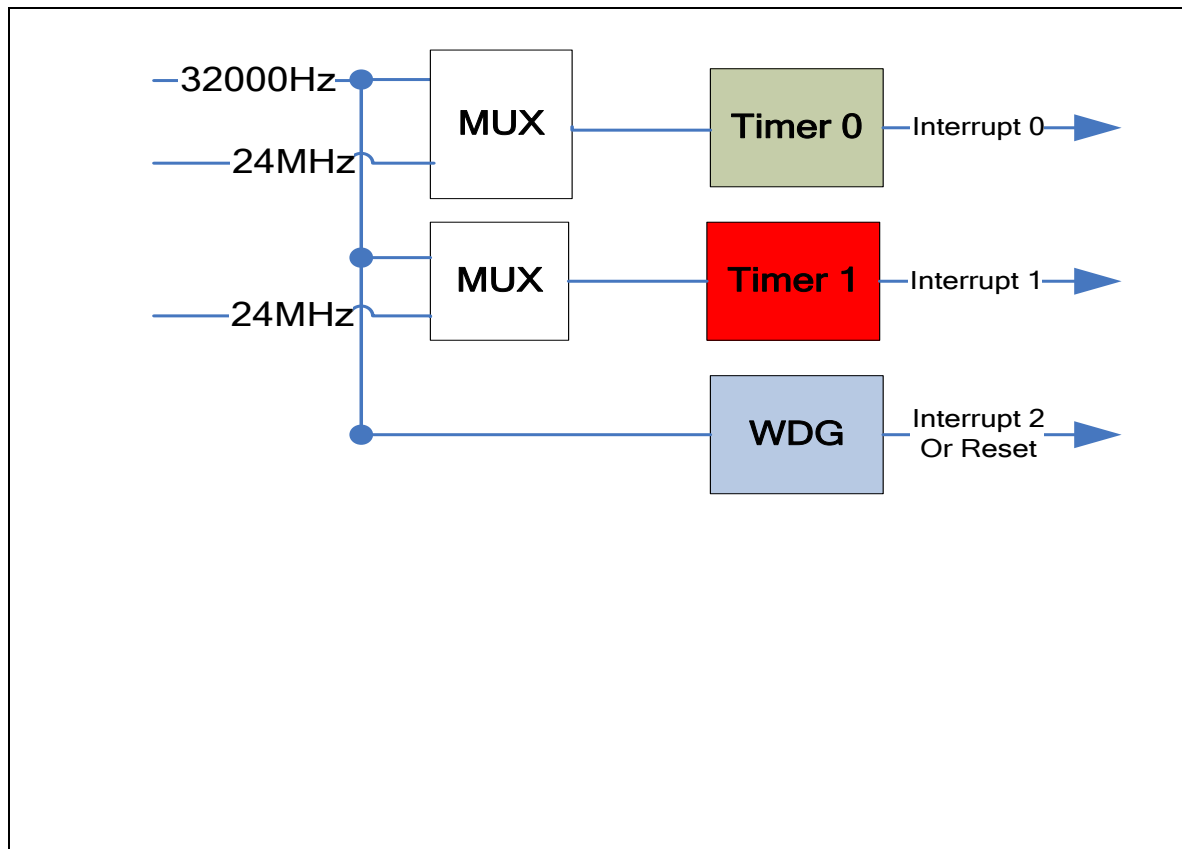
Timer 1 is used for OS to generate a periodic interrupt.

The watch-dog is used to resume the controller operation when it had been disturbed by

malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 171 seconds(35hours for 32K clock). It can generate a general reset or a interrupt request.

8.3.2 Timer Diagram

8.4 Pulse Width Modulator

8.4.1 PWM Overview

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to active state and count from 0x0000.

The PWM divider divides the clock (24MHz) by 1-4096 according to the pre-scalar bits in the PWM control register.

In PWM cycle mode, the output will be a square waveform; the frequency is set to the period register. In PWM pulse mode, the output will be a pulse.

8.5 DMA

8.5.1 DMA Overview

There are three kinds of DMA in the SOC. One is Normal DMA with 4 channels, the second   is Dedicated DMA with 4 channels and the last is the Special function DMA for display engine.

For normal DMA, only one channel can be active and the sequence is according to the priority level. While for the dedicated DMA, at most 4 channel can be active at the same time if their source or destination has no conflict.

DMA can support 8-bit/16-bit/32-bit data width. The data width of Source and Destination can be different, but the address should be aligned.

For Normal DMA, the address should be aligned with the data width.

Although the increase mode of NDMA should be address aligned, but its byte counter should not be multiple.

8.6 SDRAM Interface

8.6.1 DRAM Controller Description

The DRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all in-dusty-standard single data rate (SDR) ordinary SDRAM. It supports up to a 1G bits memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type.

The DRAMC includes the following features:
- Support SDR SDRAM of clock frequency up to PC166
- Support Memory Capacity up to 1G bits
- Support one chip select signals, it can support memory capacity up to 128 M Bytes
- Fifteen address lines including two bank address lines
- Data IO size can up to 16-bit for SDR
- Automatically generates initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be chosen for different application

■   Random read or write operation is supported

8.7   NAND Flash Interface

The NFC is one NAND Flash Controller which supports all NAND/MLC flash memory available in the market. New type flash can be supported by software re-configuration. The NFC can support 2 NAND flash with 3.3 V voltage supply. There are 2 separate chip select lines (CE#) for connecting up to 2 flash chips with2 R/B signals.

The On-the-fly error correction code (ECC) is built-in NFC for enhancing reliability. BCH-16/-24/-28/-32/-40/-48/-56/-60/-64 is implemented and it can detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NFC provides automatic timing control for reading or writing external Flash. The NFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three kind of modes are supported for serial read access. The conventional serial access is mode 0 and mode 1 is for EDO type and mode 2 for extension EDO type. NFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NAND Flash Controller (NFC) includes the following features:
●   Supports industry-standard AMBA Host Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian bus.
●   Supports AHB 32-bit bus width
●   Supports all SLC/MLC/TLC flash and EF-NAND memory available in the market
●   Software configure seed for randomize engine
●   Software configure method for adaptability to a variety of system and memory types
●   Supports 8-bit Data Bus Width
●   Supports 1024, 2048, 4096, 8192, 16384 bytes size per page
●   Supports 3.3 V voltage supply Flash
●   Up to 2 flash chips which are controlled by NFC_CEx#
●   Supports Conventional and EDO serial access method for serial reading Flash
●   On-the-fly BCH error correction code which correcting up to 64 bits per 512 or 1024 bytes
●   Corrected Error bits number information report
●   ECC automatic disable function for all 0xff data
●   NFC status information is reported by its' registers and interrupt is supported
●   One Command FIFO
●   External DMA is supported for transferring data
●   Two 256x32-bit RAM for Pipeline Procession

■ Support self –debug for NFC debug

8.8 SD Card Interface

8.8.1 SD Card Overview

The SD/MMC can be configured either as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Mem), Secure Digital I/O (SDIO), Multimedia Cards (MMC), and Consumer Electronics Advanced Transport Architecture (CE-ATA).

The SD/MMC controller includes the following features:

- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian bus.
- Support AMBA AHB Slave mode
- Supports Secure Digital memory protocol commands
- Supports Secure Digital I/O protocol commands
- Supports Multimedia Card protocol commands
- Supports CE-ATA digital protocol commands
- Supports Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Supports one SD or MMC (3.3 or 4.0) or CE-ATA device
- Supports hardware CRC generation and error detection
- Supports programmable baud rate
- Supports host pull-up control
- Supports SDIO interrupts in 1-bit and 4-bit modes
- Supports SDIO suspend and resume operation
- Supports SDIO read wait
- Supports block size of 1 to 65535 bytes
- Internal 16x32-bit (64 bytes total) FIFO for data transfer
- DMA interface for dedicated DMA transfer
- Only support 3.3 V IO pad

8.9 USB Interface

8.9.1 USB Overview

The USB is a Dual-Role Device (DRD) controller, which supports both device and host functions and is full compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a. It can also be configured as a Host-only or Device-only controller, full compliant with the USB 2.0

Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode. The USB/OTG connects to the industry-standard AMBA High-Performance Bus (AHB) for communication with other system modules, such as CPU, System Memory. It is fully compliant with the AMBA Specification, Revision 2.0. As a AHB slave device, microcontroller can access its Control and Status Registers (CSRs), the Data FIFO (DFIFO), and queues. Industry standard Single Port RAM (SPRAM) is supported for saving area and power. The Single Port RAM is used as Data FIFO. Standard USB transceiver can be used through its UTMI+PHY Level2 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus. In AHB slave mode, the data transfer between the USB/OTG and the system memory is handled by the application. For saving CPU bandwidth, USB/OTG DMA interface can support one external DMA controller to take care of the data transfer between the memory and USB/OTG core. The driver sets up the transfer and the USB/OTG interrupts the CPU only on transfer completion or and error condition. One central DMA engine is designed for the data transfer in system role. The DMA function can be disabled by software. The Host Negotiation Protocol (HNP), Session Request Protocol (SRP), and other critical functions are implemented in hardware for processing efficiency. The USB/OTG core also supports USB power saving functions.

The USB2.0 OTG controller System-Level block diagram is showed below:

The USB2.0 OTG controller (SIE) includes the following features:

- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports 32-bit Little Endian bus and its frequency can up to 180Mhz with 0.13 um CMOS technology.
- Support AMBA AHB Slave mode
- Complies with USB 2.0 Specification and its On-The-Go Supplement to the USB 2.0 Specification (Revision 1.0a)
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode and support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
- Supports the Host Negotiation Protocol (HNP) and the Session Request Protocol (SRP)
- Supports the UTMI+ Level 3 interface . The 8-bit bidirectional data buses are used.
- 64-Byte Endpoint 0 for Control Transfer (Endpoint0)
- Supports up to 3 User-Configurable Endpoints for Bulk , Isochronous, Control and Interrupt bi-directional transfers (Endpoint1, Endpoint2)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Includes interface to an external Dedicated Central DMA controller; data is transferred through Special bus for saving ABH bus bandwidth

● Supports industry-standard Single Port SRAM for USB Configurable Data FIFO; The size is 2048 byte with 32-bit word width; The RAM can be used by other modules when USB/OTG disable

8.10 Two Wire Interface

8.10.1 TWI Controller Description

This 2-Wire Controller is designed to be used as an interface between CPU host and the serial 2-Wire bus. It can support all the standard 2-Wire transfer, including Slave and Master. The communication to the 2-Wire bus is carried out on a byte-wise basis using interrupt or polled handshaking. This 2-Wire Controller can be operated in standard mode (100K bps) or fast-mode, supporting data rate up to 400K bps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

The 2-Wire Controller includes the following features:

■ Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0.
■ Supports APB 16-bits bus width
■ Software-programmable for Slave or Master
■ Supports Repeated START signal
■ Allows 10-bit addressing with 2-Wire bus
■ Performs arbitration and clock synchronization
■ Own address and General Call address detection
■ Interrupt on address detection
■ Supports speeds up to 400Kbits/s ('fast mode')
■ Allows operation from a wide range of input clock frequencies

8.10.2 TWI Controller Timing Diagram

Data transferred are always in a unit of 8-bit (byte), followed by an acknowledge bit. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCL low to force the transmitter into a wait state while waiting the response from microprocessor.

Data transfer with acknowledge is obligatory. The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCL holding between each byte. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or leave it high to send a "not acknowledge") to the

transmitter.

When a slave receiver doesn't acknowledge the slave address (unable to receive because of no resource available), the data line must be left high by the slave so that the master can then generate a STOP condition to abort the transfer. Slave receiver can also indicate not to want to send more data during a transfer by leave the acknowledge signal high. And the master should generate the STOP condition to abort the transfer.

Below diagram provides an illustration the relation of SDA signal line and SCL signal line on the 2-Wire serial bus.
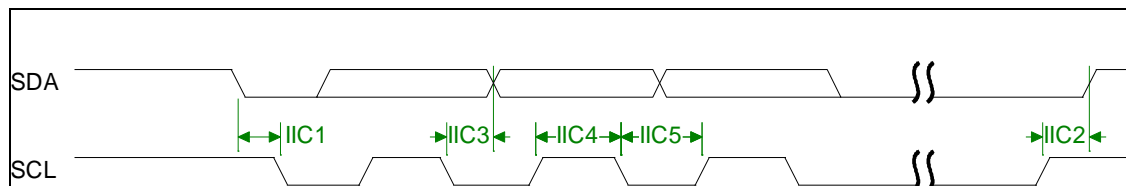
2-Wire Timing Diagram

8.11   SPI Interface

8.11.1 SPI Description

The SPI is the Serial Peripheral Interface which allows rapid data communication with less software interrupts. It can work at two modes: Master mode and Slave mode. It includes the following features:

- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Support AMBA AHB Slave mode
- Full-duplex synchronous serial interface
- Master/Slave configurable
- Two chip selects to support multiple peripherals for SPI0 and SPI1 has one chip select
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- DMA support

8.11.2 SPI Timing Diagram

The serial peripheral interface master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling

clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four kinds of modes are listed below:

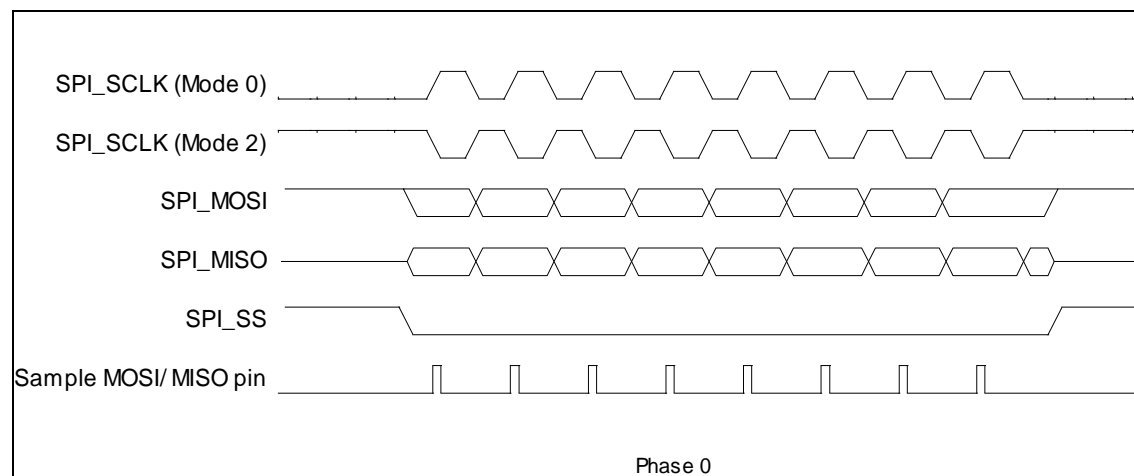| SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Failing, Setup	Rising, Sample

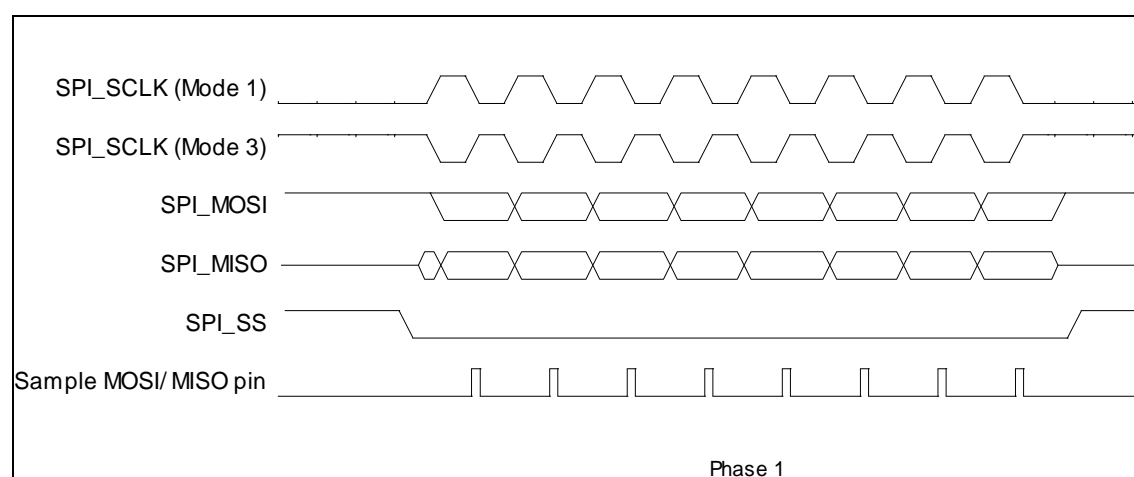Figure 1 SPI Phase 0 Timing Diagram

Figure 2 SPI Phase 1 Timing Diagram

8.12   UART Interface

8.12.1 UART Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 modes, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO conditions.

For integration in systems where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR Mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART includes the following features:
- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Supports APB 16-bit bus width
- Compatible with industry-standard 16550 UARTs
- DMA controller interface
- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Support IrDa 1.0 SIR
- Interrupt support for FIFOs, Status Change
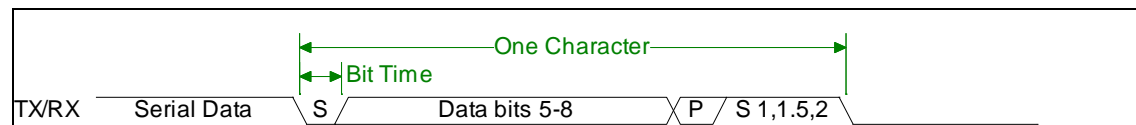
8.12.2 UART Timing Diagram

Figure 1 UART Serial Data Format
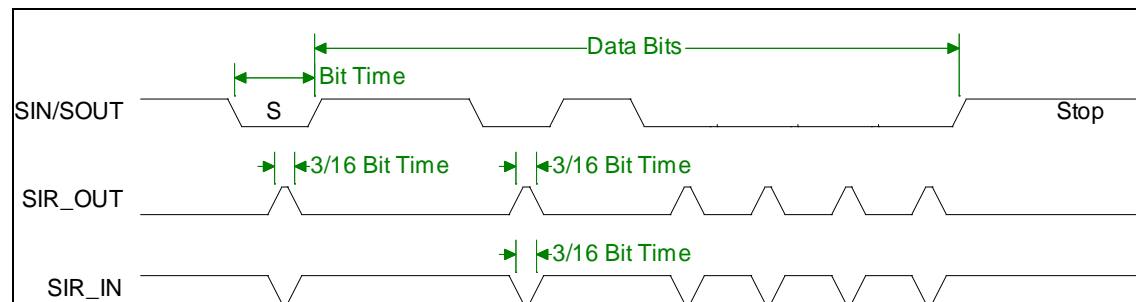
Figure 2 Serial IrDA Data Format

8.13 IR Interface

8.13.1 IR Overview

Fast Infrared Interface (FIR) signals are multiplexed with UART2 signals using a system configuration for a complete infrared interface that supports SIR, CIR, MIR, and FIR modes. The Serial Infrared (SIR) protocol, which supports data rate which supports data rates up to 1.875 Mbit/s, is implemented in each UART module. The IR includes the following features:

- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Supports APB 16-bits bus width
- Compliant with IrDA 1.1 for MIR and FIR
- Full physical layer implementation
- Supports 0.576 Mbit/s and 1.152 Mbit/s Medium Infrared (MIR) physical layer protocol
- Support 4 Mbit/s FIR physical layer protocol defined by IrDA version 1.4
- Support CIR for remote control or wireless keyboard
- Hardware CRC16 for MIR and CRC32 for FIR
- Programmable FIFO thresholds
- Interrupt and DMA Support

The MIR packet consists these fields: Two beginning flags (STA), an address, Control fields, Data fields, a frame check sequence (CRC) field and a minimum of one ending flag (STO).

STA	STA	Address	Control and DATA	CRC16	STO

MIR Packet Structure

The fields in MIR packet are defined as follows:

• STA, STO

   The MIR use the same symbol, 8'b0111, 1110, for both STA and STO.

• 8-bits Address Field

• 8-bits Control Field plus up to 2045 bytes in the data field

• 16-bits CRC field

The address, control, data, and CRC fields are not transmitted in original form: They are first converted according to the MIR standards.

The FIR packet consists these fields: Preamble field (PA), Beginning flag (STA), Address (ADR), Control fields, Data fields, A frame check sequence (CRC) field and A minimum of one ending flag (STO).

PA	STA	Address	Control and DATA	CRC32	STO

FIR Packet Structure

The fields in FIR packet are defined as follow:

• PA—   the preamble field is used by the receiver to establish phase lock. The preamble field consists of exactly sixteen repeated transmissions of the following stream of symbols: b'1000, 0000, 1010, and 1000

• STA— The STA consists of exactly one transmission of the following stream of symbols: b'0000, 1100,0000,1100,0110,0000,0110,0000

• STO— The STO consists of exactly one transmission of a stream of symbols: b'0000, 1100,0000,1100,0000,0110,0000,0110

• ACD—the payload data is encoded as 4 PPM. The encoded symbols reside in the ACD field and can be up to 2048 bytes long.

• CRC32—The CRC field consists of the 4 PPM encoded data, resulting from the IEEE 802 CRC32

Algorithm for cyclic redundancy check as applied to the payload data contained in the packet.

For MIR data rates, the NZR modulation scheme is used. A '0' is represented by a light pulse. The optical pulse duration is nominally 1/4 of bit duration. The LED is off when a '1' is transmitted.

Data Bit	Data Symbol (Address, Control and Data)
0	1000
1	0000

MIR Modulation Scheme

For 4 Mbit/s FIR, the modulation scheme is 4 PPM. In this modulation, a pair of bits is one data symbol. A data symbol is divided into four chips, only one of which contains an optical pulse. The nominal pulse duration is 125 ns. A '1' is represented by a light pulse.

Data Symbol	4 PPM Data Symbol
00	1000

01	0100
10	0010
11	0001

FIR Modulation Scheme

For 0.576Mbit/s MIR, the serial clock is 12 times of 0.576 MHz witch it is 6.912 MHz. For 1.152Mbit/s MIR, the serial clock is 12 times of 0.576 MHz witch it is 13.824 MHz. For 4Mbit/s FIR, the serial clock is 24 MHz.

Mode	Serial Clock Frequency(MHz)
MIR(0.576M)	6.912 (12*0.576)
MIR(1.152M)	13.824 (12*1.152)
FIR(4M)	24

For saving CPU resource, CIR receiver is implemented in hardware. The CIR receiver samples the inputting signal on the programmable frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to saving bandwidth. The FIFO is 8-bits width in the depth of 16 levels The MSB bit is used to record the parity of the receiving CIR signal. The high level is represented as '1' and the low level is represented as '0'. The rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low level) is more than 128, the byte is used.

On the air, there is always some noise. One threshold can be set to filter this noise to reduce system loading and improve the system stability.

8.13.2 IR Timing Diagram

Please refer to IrDA Specification.

8.14 Audio Codec

8.14.1 Description

The embedded Audio Codec is a high-quality stereo audio codec with headphone amplify.

8.14.2 Feature

- On-chip 20-bits DAC for play-back
- On-chip 20-birs ADC for recorder
- Support analog/ digital volume control
- Support 48K and 44.1K sample family
- Support FM/ Microphone recorder
- Support Volume Zero-Cross Over change
- Stereo headphone amplifier that can be operated in capless headphone mode
- Support Virtual Ground to automatic change to True Ground to protect headphone amplifier

8.14.3 Audio Codec Block Diagram
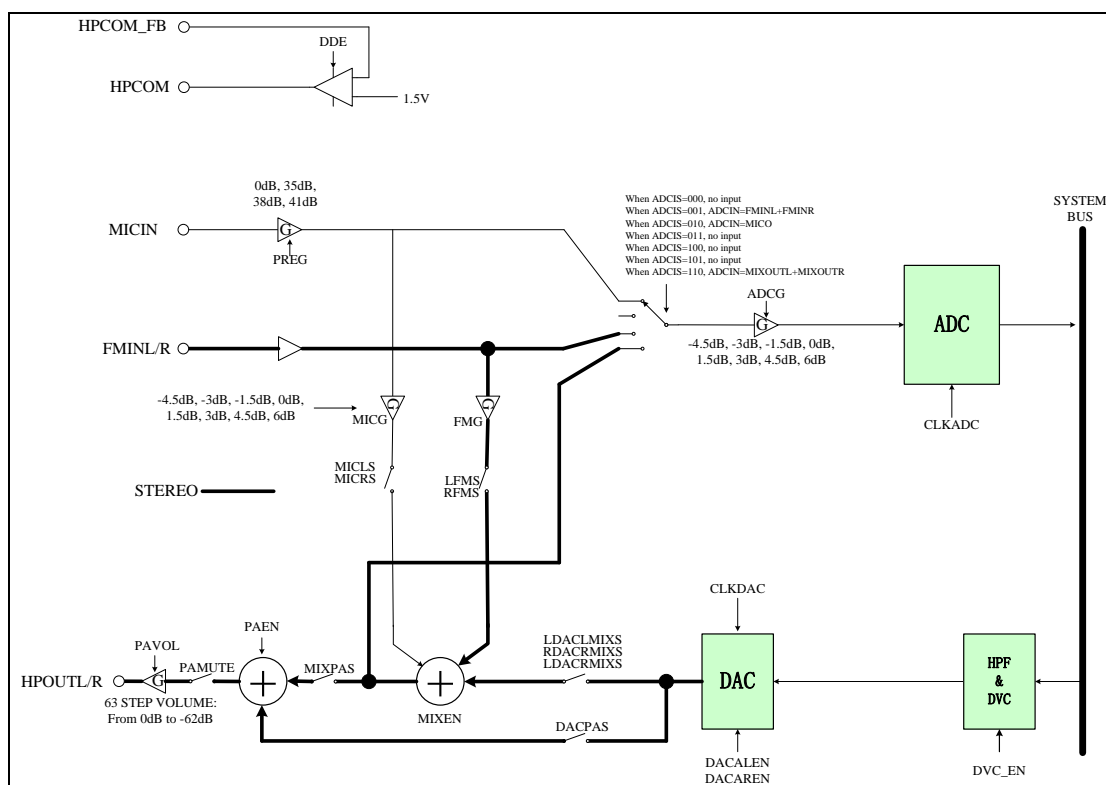
8.15　LRADC

8.15.1 Description

LRADC is 6-bits resolution for key application. The LRADC can work up to maximum conversion rate of 250Hz.

8.15.2 Feature

- Supports industry-standard AMBA peripheral Bus(APB) and it is fully compliant with the AMBA specification, Revision 2.0
- Supports APB 32-bits bus width
- Interrupt Support
- Support Hold Key and General Key
- Support Single Key and Continue Key Mode
- 6-bits Resolution
- Voltage input range between 0 to 2/3 AVCC(AVCC is LRADC reference voltage)

8.16　Touch Panel

8.16.1 Description

TPADC is 11-bit for touch screen application or for normal ADC application. The TPADC can work up to maximum conversion rate of 64KHZ. The TPADC can also used for 4-channel normal ADC application.

Touch Panel Controller's features are listed below:
- Supports industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0
- Supports APB 32-bit bus width
- Interrupt support
- 11-bit Resolution
- Voltage input range between 0V to 2/3AVCC
- Sample rate up to 64K
- Software configured sample period for Touch Screen application
- 4 channels auxiliary analogy input for normal ADC application
- Normal DMA support

8.17 GPIO Interface

8.17.1 Port Description

The chip has 4 ports for multi-functional input/out pins. They are shown below:

■ Port A(PA): 9 input/output port

■ Port C(PC): 16 input/output port

■ Port D(PD): 22 input/output port

■ Port E(PE) : 4 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions not used. 5 external PIO interrupt sources are supported and interrupt mode can be configured by software.

8.17.2 Port Configuration Table

PORT A	MULTIPLEX FUNCTION SELECT				
PA0	INPUT/OUPUT	SDC0_D1		SPI1_CS0	EINT0
PA1	INPUT/OUTPUT	SDC0_D0		SPI1_MOSI	EINT1
PA2	INPUT/OUTPUT	SDC0_CLK	UART0_TX	SPI1_CLK	
PA3	INPUT/OUTPUT	SDC0_CMD		SPI1_MISO	
PA4	INPUT/OUTPUT	SDC0_D3	UART0_RX		EINT2
PA5	INPUT/OUTPUT	SDC0_D2		IR_RX	EINT3
PA6	INPUT/OUTPUT	TWI0_SCK	NCE2		
PA7	INPUT/OUTPUT	TWI0_SDA	NCE3		
PA8	INPUT/OUTPUT	PWM0	SPI1_CS1		EINT4

Port A (PA) Multiplex Function Select Table

PORT C	MULTIPLEX FUNCTION SELECT				
PC0	INPUT/OUTPUT	NWE#	SPI0_MOSI		
PC1	INPUT/OUTPUT	ALE	SPI0_MISO		
PC2	INPUT/OUTPUT	CLE	SPI0_CLK		
PC3	INPUT/OUTPUT	NCE1	SPI0_CS		
PC4	INPUT/OUTPUT	NCE0			

PC5	INPUT/OUTPUT	NRD#	SDC2_CMD		
PC6	INPUT/OUTPUT	NRB0	SDC2_CLK		
PC7	INPUT/OUTPUT	NRB1			
PC8	INPUT/OUTPUT	ND0	SDC0_D0		
PC9	INPUT/OUTPUT	ND1	SDC0_D1		
PC10	INPUT/OUTPUT	ND2	SDC0_D2		
PC11	INPUT/OUTPUT	ND3	SDC0_D3		
PC12	INPUT/OUTPUT	ND4	SDC2_D0		
PC13	INPUT/OUTPUT	ND5	SDC2_D1		
PC14	INPUT/OUTPUT	ND6	SDC2_D2		
PC15	INPUT/OUTPUT	ND7	SDC2_D3		

Port C (PC) Multiplex Function Select Table

PORT D(PD)	**MULTIPLEX FUNCTION SELECT**				
PD2	INPUT/OUTPUT	LCD2			
PD3	INPUT/OUTPUT	LCD3			
PD4	INPUT/OUTPUT	LCD4			
PD5	INPUT/OUTPUT	LCD5			
PD6	INPUT/OUTPUT	LCD6			
PD7	INPUT/OUTPUT	LCD7			
PD10	INPUT/OUTPUT	LCD10			
PD11	INPUT/OUTPUT	LCD11			
PD12	INPUT/OUTPUT	LCD12			
PD13	INPUT/OUTPUT	LCD13			
PD14	INPUT/OUTPUT	LCD14			
PD15	INPUT/OUTPUT	LCD15			
PD16	INPUT/OUTPUT	LCDCLK			
PD17	INPUT/OUTPUT	LCDDE			
PD18	INPUT/OUTPUT	LCDHSYNC			
PD19	INPUT/OUTPUT	LCDVSYNC			
PD22	INPUT/OUTPUT	LCD18			
PD23	INPUT/OUTPUT	LCD19			

PD24	INPUT/OUTPUT	LCD20			
PD25	INPUT/OUTPUT	LCD21			
PD26	INPUT/OUTPUT	LCD22			
PD27	INPUT/OUTPUT	LCD23			

Port D (PD) Multiplex Function Select Table

| PORT E(PE)	MULTIPLEX FUNCTION SELECT				
PE0	INPUT/OUTPUT	EINT0	X1		
PE1	INPUT/OUTPUT	EINT1	X2		
PE2	INPUT/OUTPUT	EINT2	Y1		
PE3	INPUT/OUTPUT	EINT3	Y2		

Port E (PE) Multiplex Function Select Table

8.18 TV Encoder

8.18.1 Feature

■ Multi-standard support for NTSC-M, NTSCJAPAN, PAL (B, D, G, H, I, M, N, Combination N)@27M clock

■ Video input data port supports: YCbCr422 16-bit, YCbCr444 24-bit or RGB444 24-bit input format,

■ Video output data port supports: 1 X10-bit DAC data output, Composite(CVBS)

■ Plug status auto detecting

8.18.2 Block diagram
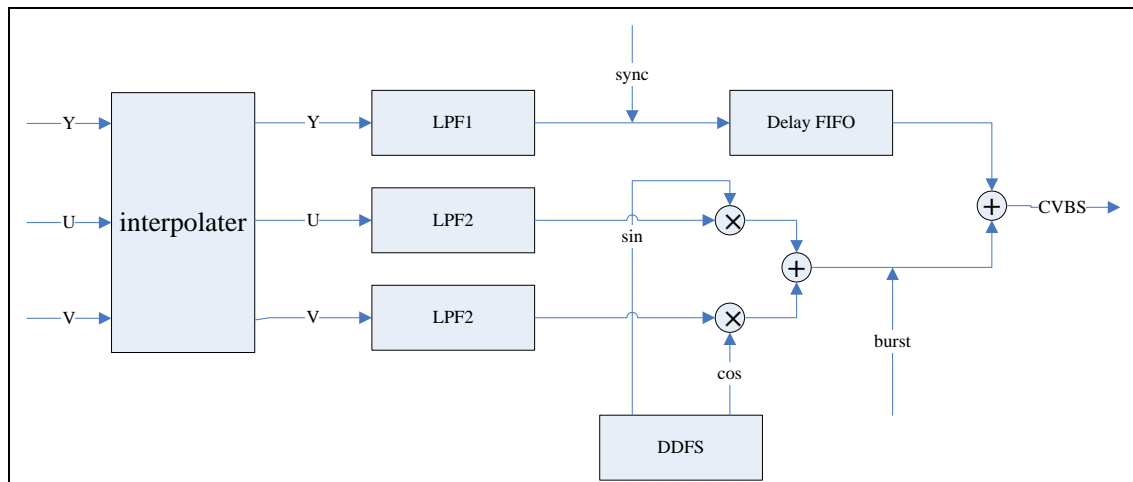
8.19   Universal LCD/TV Timing Controller

8.19.1 Feature

- Support HV-DE-Sync (digital parallel RGB) input LCD panels
- Support HV-DE-Sync (digital serial RGB, both delta and stripe panel) input LCD panels
- Support TTL (digital RGB) input LCD panels
- Support Analog RGB input LCD panels
- Support 18/16/9/8bit 8080 CPU I/F panels
- CCIR656 output interface for LCD panel or TV encoder
- TV timing for TV encoder and HDMI transmitter
- Internal line scaling and Gamma correction

8.20   Video Decoder Engine

8.20.1 Video Decoder Engine Overview

The video engine is a high performance multi-standard video codec IP that can the H.264
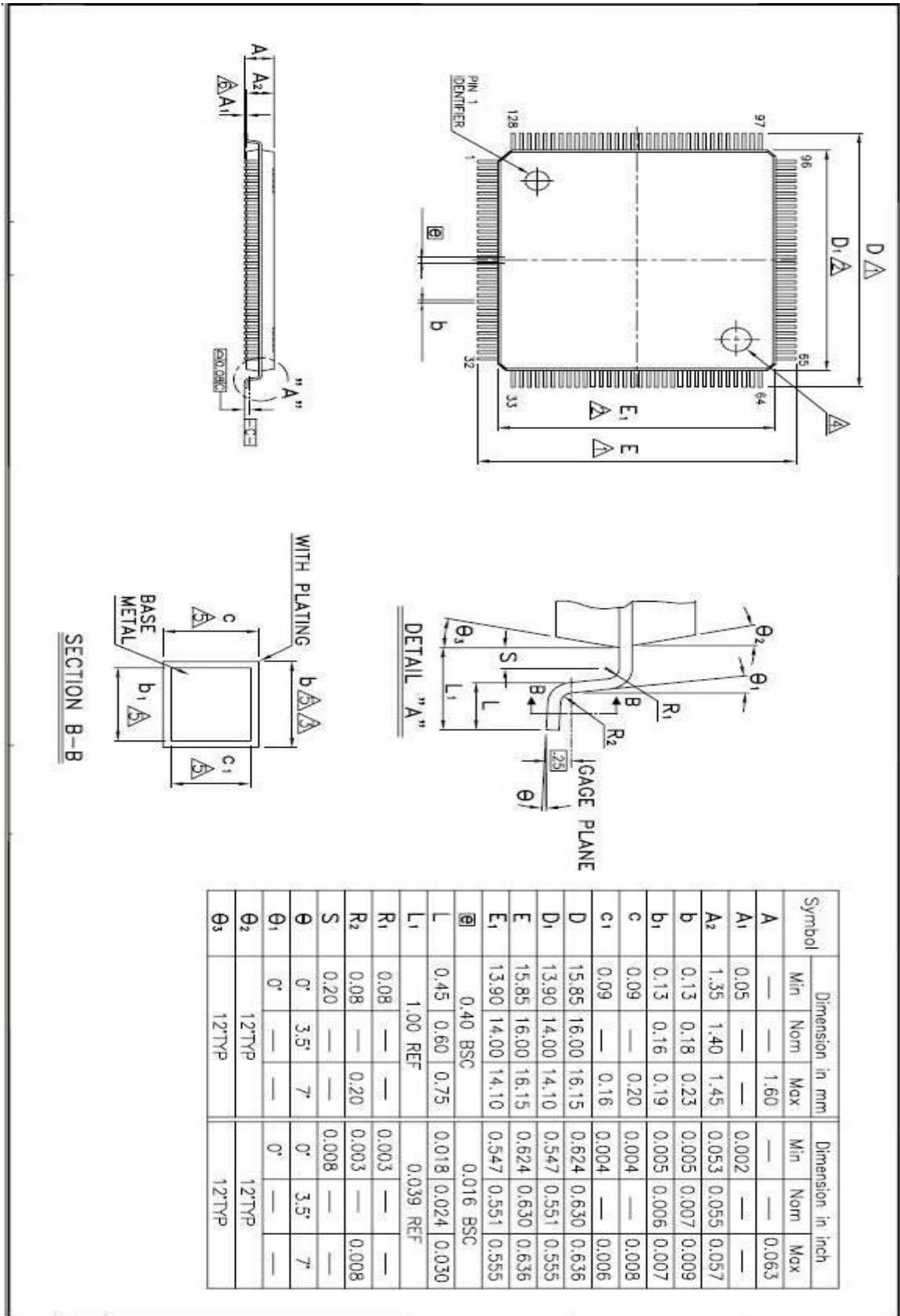BP/MP/HP, Mpeg-4 SP/ASP, H.263,Mpeg 1/2, Jpeg and Sorenson Spark decoding.

It connects with the system via the 32-bits AHB bus for system control and 32-bit MEM bus for

data throughput. In default status, the two buses are gated off to video engine. The video engine also takes advantage of on-chip memories to achieve high performance and these memories can also be mapped to AHB bus for testing or other applications. The video engine uses one dedicated PLL for working clock .. In default status, The PLL is disabled and video engine has no working clock and is in reset status.

In decoding mode, the video engine reads the bitstreams stored in external SDRAM and the decoded final pictures are also stored in external SDRAM. After one picture is decoded, the video engine will inform the host controller with interrupt or status flags.

9 Package Specifications

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		