SY8308

High Efficiency, 8.0A 40V Input Synchronous Step Down Regulator

General Description

The SY8308 develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 8A continuous current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8308 operates over a wide input voltage range from 4V to 40V. The device adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads.

Ordering Information

SY8308 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8308RBC	QFN3.5×3.5-20	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom):25mΩ/12mΩ
- 4~40V Input Voltage Range
- 8.0A Output Current Capability
- Selectable 350 kHz/500kHz Switching Frequency
- PFM/PWM Selectable Light Load Operation Mode
- Instant PWM Architecture to Achieve Fast Transient Responses.
- Programmable Soft-start Limits the Inrush Current
- Programmable Valley Current Limit Threshold
- Hic-cup Mode Output Short Circuit Protection
- Power Good Indicator
- 0.6V±1% Reference Voltage
- Compact Package: QFN3.5×3.5-20

Applications

- LCD-TV
- SetTop Box
- Notebook
- Storage
- High Power AP Router
- Networking

Typical Applications

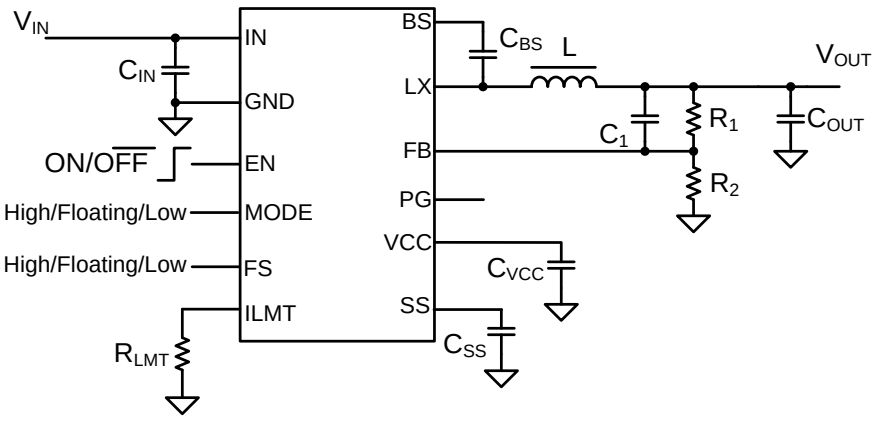
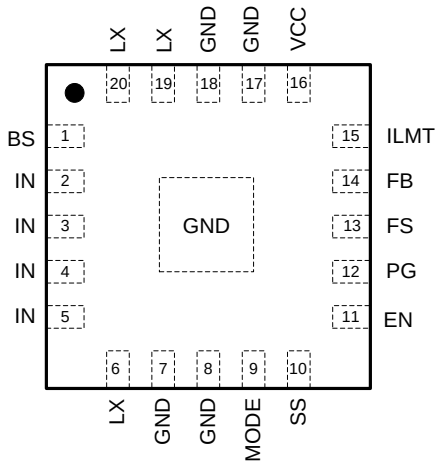


Figure1. Schematic Diagram

Pinout (top view)



(QFN3.5×3.5-20)

Top Mark: BDY***xyz***, **(**Device code: BDY, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin.
IN	2,3,4,5	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
LX	6,19,20	Inductor pin. Connect this pin to the switching node of the inductor.
GND	7,8,17,18, Exposed pad	Ground pin.
MODE	9	Operating mode selection under light load. Pull this pin low for PFM operating; pull this pin high or floating for PWM operation.
SS	10	Soft-start programming pin. Connect a capacitor from this pin to ground to program the soft-start time. t_{ss}(ms)=Css(nF)×0.6V/6μA. Leave this pin open for default 1ms soft-start.
EN	11	Enable control. Pull high to turn on. Do not leave it floating.
PG	12	Power good Indicator. Open-drain output when the output voltage is within 85% to 122% of regulation point.
FS	13	Switching frequency selection. Pull this pin low for 350kHz; pull this pin high or floating for 500kHz.
FB	14	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.6× (1+R_1/R_2).
ILMT	15	Valley current limit programming. I_{LMT_VALLEY}(A)=3600/R_{LMT}(kΩ). Leave this pin open for default 6A valley current limit threshold.
VCC	16	Internal 3.3V output. Decouple this pin to ground with at least a 4.7μF capacitor.

Block Diagram

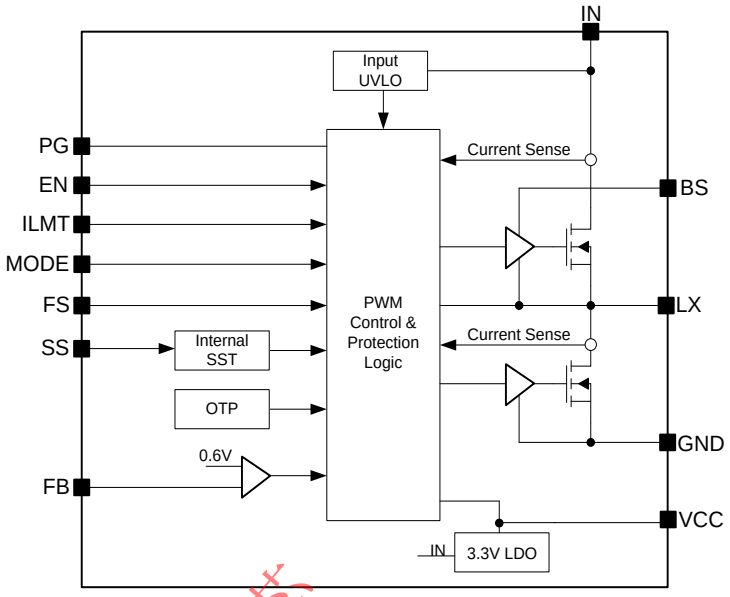


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 40V
BS-LX, VCC, FB Voltage---------- -0.3V to 4V
LIMT, FS, PG, EN, MODE, SS, LX Voltage---------- -0.3V to VIN + 0.3V
Power Dissipation, P_D @ T_A = 25°C, QFN3.5×3.5-20 ---------- 3.6W
Package Thermal Resistance (Note 2)
Θ_{JA} ---------- 28°C/W
Θ_{JC} ----------4°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 10ns duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 40V
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, I_{OUT} = 1A, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		40	V
Input UVLO Threshold	V_{UVLO}				3.9	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		60		μA
Shutdown Current	I_{SHDN}	EN=0			4	μA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			25		mΩ
Bottom FET RON	$R_{DS(ON)2}$			12		mΩ
Bottom FET Valley Current Limit Program Range	$I_{LMT,RNG}$	R_{LMT}=300kΩ~600kΩ	6		12	A
Bottom FET Valley Current Limit Setting Accuracy	I_{LMT}	R_{LMT}=300kΩ	9.6	12	14.4	A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$	MODE=High	3.5			A
EN Input Voltage High	$V_{EN,H}$		1.5			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
EN Leakage Current	I_{EN}				1	μA
MODE Input Voltage High	$V_{MODE,H}$		V_{CC}-0.8			V
MODE Input Voltage High	$V_{MODE,L}$				0.4	V
MODE Leakage Current	I_{MODE}				1	μA
FS Input Voltage High	$V_{FS,H}$		V_{CC}-0.8			V
FS Input Voltage High	$V_{FS,L}$				0.4	V
FS Leakage Current	I_{FS}				1	μA
Power Good Threshold	$V_{PG,TH}$	V_{FB} falling, PG from high to low	81	85	89	%V_{REF}
		V_{FB} rising, PG from low to high	85	90	95	%V_{REF}
		V_{FB} falling, PG from low to high	104	110	116	%V_{REF}
		V_{FB} rising, PG from high to low	116	122	128	%V_{REF}
Power Good Delay	$t_{PG,DLY}$	Low to high		200		μs
		High to low		10		μs
Power Good Low Voltage	V_{PG_LOW}	Sink 5mA to PG pin, FB=0.6V			0.4	V
Soft-start Charging Current	I_{SS}			6		μA
Internal Soft-start Time	t_{SS}	SS floating		1		ms
Output Over Voltage Threshold	V_{OVP}	V_{FB} rising	116	122	128	%V_{REF}
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			10		%V_{REF}
Output OVP Delay	$t_{OVP,DLY}$			15		μs
Output Under Voltage Protection Threshold	$V_{OUT,UVP}$	V_{FB} falling	45	50	55	%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			200		μs
UVP Hic-cup ON Time	$t_{UVP,ON}$	SS floating		3		ms
UVP Hic-cup OFF Time	$t_{UVP,OFF}$	SS floating		21		ms
Switching Frequency	f_{SW}	FS=Floating, CCM	400	500	600	kHz
VCC Output Voltage	V_{VCC}		3.15	3.3	3.45	V

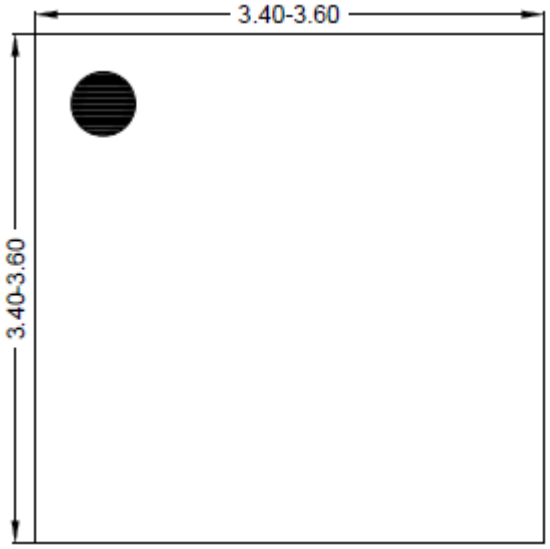
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Min ON Time	$t_{ON,MIN}$			80		ns
Min OFF Time	$t_{OFF,MIN}$			160		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

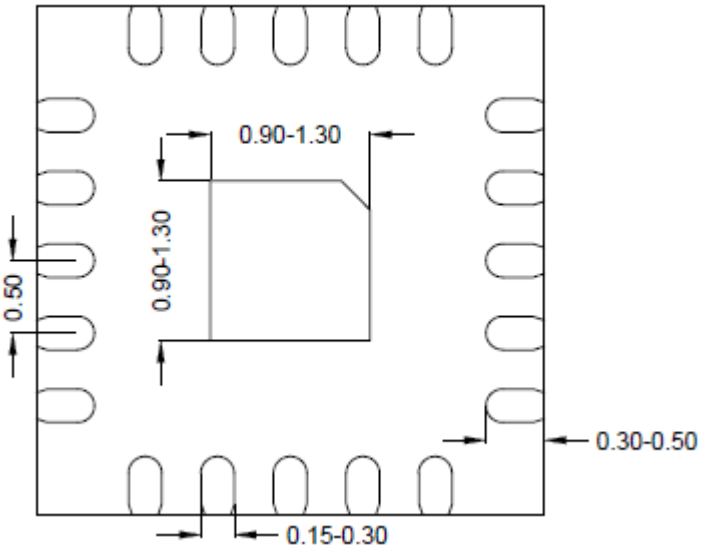
Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

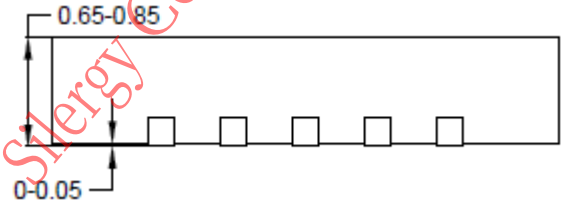
QFN3.5×3.5-20 Package Outline



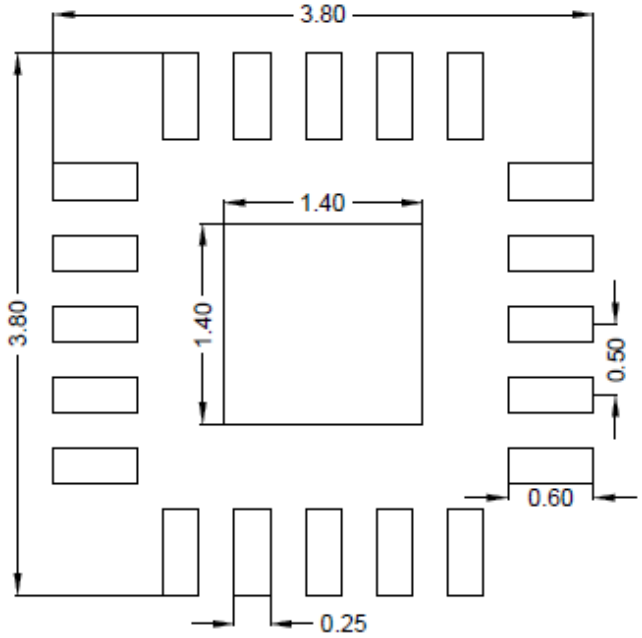
Top view



Bottom view



Side view

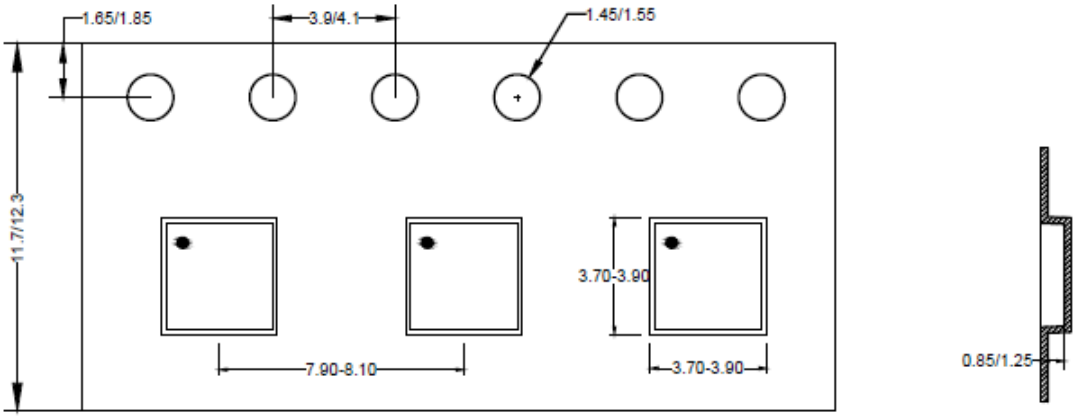


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

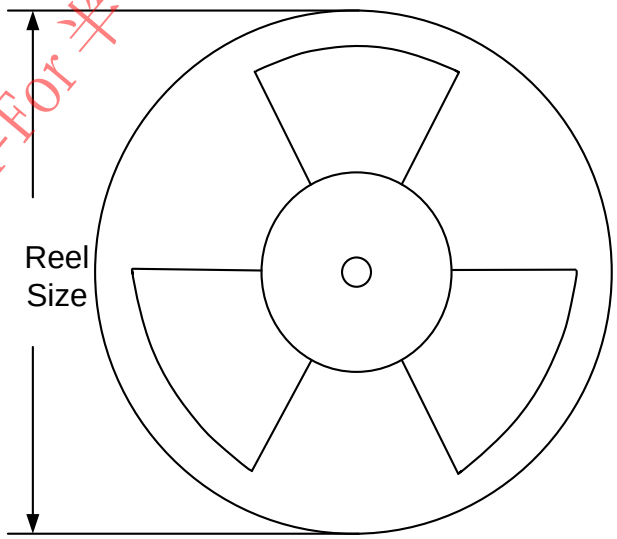
Taping & Reel Specification

1. QFN3.5×3.5-20 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3.5×3.5	12	8	13"	400	400	3000

3. Others: NA