■ Dynamic RAMs

Memory Size	Tuno No	Memory	Access	Cycle	Refresh	Supply	Power Consumption max. (mW)		Dealine		Process	Devices
(bit)	Type No.	Composition (Word × bit)	Time max. (ns)	Time min. (ns)	Cycle (cycle/ms)	Voltage (V)	max. (Operating	mW) Stand-by	Package	No.	Process	Remarks
	MN41256A-08	262,144 × 1		, , , , , , , , , , , , , , , , , , , ,	(-),	(*)	Operating	Stand-by	DIP016-P-0300A	M8		
Ì	MN41256AJ-08		80	160	256/4ms	4.5 ~ 5.5	440	16.5	QFJ018-P-R290	M32	NMOS	● Page mode
	MN41256AL-08								ZIP016-P-0300	M2	- 111100	
ł	MN41257A-08								DIP016-P-0300A	M8		
+		262,144 × 1	80	160	256/4ms	4.5 ~ 5.5	440	16.5	QFJ018-P-R290	M32	NMOS	Nibble mode
256K	MN41257AJ-08	1			200,	1.0 0.0	•••	1			111110	• PAIDDIC MOGC
	MN41257AL-08								ZIP016-P-0300	M2		
}	MN41464A-08	-							DIP018-P-0300A	M8		
	MN41464AJ-08	65,536 × 4	80	160	256/4ms	4.5 ~ 5.5	440	16.5	QFJ018-P-R290	M32	NIMOS	♠ D
	MN41464AL-08	65,556 A 4	80	100	200/41118	4.5 ~ 5.5	440	10.5	ZIP018-P-0350	М3	NMOS	Page mode
	MN41464AZ-08								ZIP020-P-0400	M4		
	MN41464AS-08								SOP024-P-0425	M24		
	MN41C1000A-06		60	110			468					
	MN41C1000A-07 MN41C1000A-08		70 80	130 150			440 413		DIP018-P-0300C	M10		
	MN41C1000AL-06		60	110			468	_				● High-speed page mode
İ	MN41C1000AL-07		70	130			440	0.275	ZIP020-P-0400	M4	CMOS	
ļ	MN41C1000AL-08	1,048,576 × 1	80	150			413	(CMOS)				
	MN41C1000ASJ-06		60	110	512/8ms	4.5 ~ 5.5	468	5.5 (TTL) (level)				
	MN41C1000ASJ-07 MN41C1000ASJ-08		70 80	130 150	512/ 01115		440 413		SOJ026-P-0300A	M20		
-	MN41C1000AT-06		60	110			468					
	MN41C1000AT-07		70	130			440		TSOP020-P-0616	M33		
	MN41C1000AT-08		80	150			413					
	MN41C1000ATR-06		60	110			468					
	MN41C1000ATR-07 MN41C1000ATR-08		70 80	130 150			440 413		TSO P020-P-0616R	M34		
-			60	110			468					
	MN41C1002A-06 MN41C1002A-07	1,048,576 × 1	70	130	512/8ms	4.5 ~ 5.5	440	0.275 (CMOS) (level) 5.5 (TTL) (level)	DIP018-P-0300C	M10	_	● Static column mode
	MN41C1002A-08		80	150			413					
	MN41C1002AL-06		60	110			468		,			
	MN41C1002AL-07 MN41C1002AL-08		70 80	130 150			440 413		ZIP020-P-0400	M4	CMOS	
1M			60	110			468					
	MN41C1002ASJ-06 MN41C1002ASJ-07		70	130			440		SOJ026-P-0300A	M20		
	MN41C1002ASJ-08		80	150			413					
	MN41C1002AT-06		60	110			468					
	MN41C1002AT-07 MN41C1002AT-08		70 80	130 150			440 413	((((((((((((((((((((TSOP020-P-0616	M33		
	MN41C1002AT-08	_	60	110			468	1				
	MN41C1002ATR-07		70	130			440		TSOP020-P-0616R	M34		
	MN41C1002ATR-08		80	150			413					
	MN41C4256A-06		60	110			468					
	MN41C4256A-07 MN41C4256A-08		70 80	130 150			440 413		DIP018-P-0300C	M10		
		1	60	110	<u> </u>		468	-				
	MN41C4256AL-06 MN41C4256AL-07	262,144 × 4	70	130			440	0.275	ZIP020-P-0400	M4		
	MN41C4256AL-08		80	150]		413	(CMOS)				
	MN41C4256ASJ-06		60	110	512/8ms	4.5 ~ 5.5	468	` ` ` '	00100		CMOS	High-speed
	MN41C4256ASJ-07 MN41C4256ASJ-08		70 80	130 150	0.25, 0.113	1.0 0.0	440 413	5.5	SOJ026-P-0300A	M20	Cinco	page mode
			60	110			468	(TTL)		-	_	
- 1	MN41C4256AT-06 MN41C4256AT-07		70	130			440	(level)	TSOP020-P-0616	M33		
			80	150			413				_	
	MN41C4256AT-08											
	MN41C4256AT-08 MN41C4256ATR-06 MN41C4256ATR-07		60 70	110 130			468 440	_	TSOP020-P-0616R	M34	_	

■ Dynamic RAMs (continued)

Memory		Memory	Access	Cycle	Refresh	Supply	Power Con	sumption				
Size (bit)	Type No.	Composition			Cycle	Voltage	max. (1	Package		Process	Remarks
(bit)	MN41C4258A-06 MN41C4258A-07	(Word × bit)	60 70	min. (ns) 110 130	(cycle/ms)	(V)	Operating 468 440	Stand-by 0.275 (CMOS)	DIP018-P-0300C	No. M10		
-	MN41C4258AL-06 MN41C4258AL-06 MN41C4258AL-07 MN41C4258AL-08		80 60 70 80	150 110 130 150	512/8ms		413 468 440 413		ZIP020-P-0400	M4		
	MN41C4258ASJ-06 MN41C4258ASJ-07 MN41C4258ASJ-08	262,144 × 4	60 70 80	110 130 150		4.5 ~ 5.5	468 440 413	- (level) 5.5	SOJ026-P-0300A	M20	CMOS	Static column mode
	MN41C4258AT-06 MN41C4258AT-07 MN41C4258AT-08		60 70 80	110 130 150			468 440 413	(TTL level)	TSOP020-P-0616	M 33		
	MN41C4258ATR-06 MN41C4258ATR-07 MN41C4258ATR-08		60 70 80	110 130 150			468 440 413		TSOP020-P-0616R	M34		
	MN42C1000A-06 MN42C1000A-07 MN42C1000A-08	-	60 70 80	110 130 150			468 440 413		DIP018-P-0300C	M10		High-speed page mode CBR-self-refresh
	MN42C1000AL-06 MN42C1000AL-07 MN42C1000AL-08	-	60 70 80	110 130 150			468 440 413	0.275 (CMOS) level	ZIP020-P-0400	M4	CMOS	
1M	MN42C1000ASJ-06 MN42C1000ASJ-07 MN42C1000ASJ-08	1,048,576 × 1	60 70 80	110 130 150	512/64ms	4.5 ~ 5.5	413	5.5 (TTL (level)	SOJ026-P-0300A	M20		
	MN42C1000AT-06 MN42C1000AT-07 MN42C1000AT-08		60 70 80	110 130 150			468 440 413		TSOP020-P-0616	M33		
_	MN42C1000ATR-06 MN42C1000ATR-07 MN42C1000ATR-08		60 70 80	110 130 150			468 440 413		TSOP020-P-0616R	M34		
	MN42C4256A-06 MN42C4256A-07 MN42C4256A-08	262,144 × 4	60 70 80	110 130 150	512/64ms	4.5 ~ 5.5	468 440 413	0.275 (CMOS level) 5.5 (TTL level)	DIP018-P-0300C	M10	CMOS	● High-speed page mode ● CBR-self-refresh
	MN42C4256AL-06 MN42C4256AL-07 MN42C4256AL-08		60 70 80	110 130 150			468 440 413		ZIP020-P-0400	M4		
	MN42C4256ASJ-06 MN42C4256ASJ-07 MN42C4256ASJ-08		60 70 80	110 130 150			468 440 413		SOJ026-P-0300A	M20		
	MN42C4256AT-06 MN42C4256AT-07 MN42C4256AT-08		60 70 80	110 130 150			468 440 413		TSOP020-P-0616	M33		
	MN42C4256ATR-06 MN42C4256ATR-07 MN42C4256ATR-08		60 70 80	110 130 150			468 440 413		TSOP020-P-0616R	M34		
_	MN414100AL-07 MN414100AL-08 MN414100ASJ-07	_	70 80 70	130 150			550 495 550	0.275 (CMOS.)	ZIP020-P-0400	M4	_	
-	MN414100ASJ-08 MN414100ATT-07	4,194,304 × 1	80 70	150 130	. 1024/16ms	4.5 ~ 5.5	495 550	[level]	SOJ026-P-0300A TSOP026-P-0300A	M20 M35	CMOS	High-speed page mode
4M	MN414100ATT-08 MN414100ATTR-07 MN414100ATTR-08	_	70 80	150 130 150			495 550 495	(TTL)	TSOP026-P-0300AR	M36		
	MN414400AL-07 MN414400AL-08		70 80	130 150			550 495	0.275	ZIP020-P-0400	M4	CMOS	
_	MN414400ASJ-07 MN414400ASJ-08	1,048,576 × 4	70 80 70	130 150	1024/16ms	4.5 ~ 5.5	550 495	(CMOS level)	SOJ026-P-0300A	M20		High-speed page mode
	MN414400ATT-07 MN414400ATT-08 MN414400ATTR-07	× 4	70 80 70	130 150 130			550 495 550	5.5 (TTL (level)	TSOP026-P-0300A	M35		"
	MN414400ATTR-08		80	150			495		TSOP026-P-0300AR	M36		

■ Dynamic RAMs (continued)

Memory	Type No.	Memory	Access	Cycle	Refresh Cycle (cycle/ms)	Supply	Power Consumption max. (mW)		Package		Process	Bonseiler
Size (bit)		Composition (Word × bit)	Time max. (ns)	Time min. (ns)		Voltage (V)	max. (i Operating	MW) Stand-by	Package	No.	Process	Remarks
(5.1.)	MN424100AL-07	(**SIU /\ DIU)	70	130	1024/128ms	_	550		ZIP020-P-0400	M4		
	MN424100AL-08 MN424100ASJ-07	4,194,304	70	130			495 550 495	0.275 (CMOS) level	SOJ026-P-0300A	M20		● High-speed
	MN424100ASJ-08 MN424100ATT-07	×1	70	130			550	5.5	TSOP026-P-0300A	M35	CMOS	page mode CBR-self-refresh
	MN424100ATT-08		80	150			495	(TTL)				
	MN424100ATTR-07 MN424100ATTR-08		70 80	130 150			550 495	, ,	TSOP026-P-0300AR	M36		
	MN424400AL-07 MN424400AL-08		70 80	130 150			550 495	0.275	ZIP020-P-0400	M4		
	MN424400ASJ-07 MN424400ASJ-08	1,048,576	70 80	130 150	1024/128ms	4.5 ~ 5.5	550 495	(CMOS level)	SOJ026-P-0300A	M20	CMOS	High-speed page mode
	MN424400ATT-07 MN424400ATT-08	×4	70 80	130 150	10247 120118	4.5 - 5.5	550 495	5.5 (TTL)	TSOP026-P-0300A	M35	CMOS	● CBR-self-refresh
	MN424400ATTR-07 MN424400ATTR-08	1	70 80	130 150			550 495	(level)	TSOP026-P-0300AR	M36		
	MN414170SJ-08	-							SOJ040-P-0400	M23		● 1 CAS /2 WE
	▲MN414170TT-08	262,144 × 16	80	150	1024/16ms	4.5 ~ 5.5	605		TSOP044-P-0400A	M44		High-speed
	▲MN414170TTR-08							2.75	TSOP044-P-0400AR	M45	CMOS	page mode
	MN414260\$J-08	262,144 × 16			512/8ms	4.5 ~ 5.5	880	(CMOS level) 5.5 (TTL level)	SOJ040-P-0400	M23		● 2CAS/1WE ● High-speed page mode
	▲MN414260TT-08		80	150					TSOP044-P-0400A	M44		
	MN414260TTR-08								TSOP044-P-0400AR	M45		
	MN414270SJ-08	262,144 × 16			512/8ms	4.5 ~ 5.5	880		SOJ040-P-0400	M23		● 1CAS/2WE
	▲MN414270TT-08		80	150					TSOP044-P-0400A	M44		High-speed
4M	▲MN414270TTR-08								TSOP044P-0400AR	M45		page mode
	MN424170SJ-08	262,144 × 16	-				605		S0J040-P-0400	M23		• 1CAS/2WE
	▲MN424170TT-08		80	150	1024/128ms	4.5 ~ 5.5			TSOP044-P-0400A	M44		● High-speed
	▲MN424170TTR-08							0.275	TSOP044-P-0400AR	M45	-	page mode CBR-self-refresh
		262,144		150	512/64ms	4.5 ~ 5.5	880	(CMOS)	SOJ040-P-0400	M23	CMOS	• 2CAS/1WE
	MN424260SJ-08		90					(level)	TSOP044-P-0400A			12
	▲MN424260TT-08	× 16	80					5.5				page mode
	▲MN424260TTR-08							(TTL)	TSOP044-P-0400AR	M45		● CBR-self-refresh
	MN424270SJ-08	262,144			512/64ms	4.5 ~ 5.5	880		SOJ040-P-0400	M23		● 1CAS/2WE ● High-speed
	▲MN424270TT-08	× 16	80	150					TSOP044-P-0400A	M44		page mode
	▲MN424270TTR-08								TSOP044-P-0400AR	M45		● CBR-self-refresh
	▲MN41V4400SJ-06 ▲MN41V4400SJ-07 ▲MN41V4400SJ-08		60 70 80	110 130 150			288 252 216		SOJ026-P-0300A	M20		
	▲MN41V4400TT-06 ▲MN41V4400TT-07	1,048.576 × 4	60 70 80	110 130 150	1024/16ms	3.0 ~ 3.6	288 252 216	0.18 (CMOS) level	TSO P026-P-0300A	M35	cmos	High-speed page mode
	▲MN41V4400TT-08 ▲MN41V4400TTR-06 ▲MN41V4400TTR-07		60 70	110 130	-		288 252		TSOP026-P-0300AR	M36	-	
	▲MN41V4400TTR-08 ▲MN41V4800SJ-06		80 60	150 110			216 288				CMOS	
	▲MN41V4800SJ-07 ▲MN41V4800SJ-08		70 80	130 150	1024/16ms		252 216	0.18 (CMOS level)	SOJ028-P-0400	M21		i A Uigh ang - J
	▲ MN41V4800TT-06 ▲ MN41V4800TT-07 ▲ MN41V4800TT-08	524,288 × 8	60 70 80	70 130		3.0 ~ 3.6	288 252 216		TSOP028-P-0400	M37		 CAS before
	▲MN41V4800TTR-06 ▲MN41V4800TTR-07 ▲MN41V4800TTR-08		60 70 80	110 130 150			288 252 216		TSO P028-P-0400R	M38		RAS-self-refresh

[▲] Under development

 $(Package\ Symbol)\ \ DIP = \underline{D}ual_\underline{I}n-Line\ \underline{P}lastic\ Package,\ ZIP = \underline{Z}igzag_\underline{I}n-Line\ \underline{P}lastic\ Package$

 $SOJ = \underline{\underline{\underline{Y}}} \\ \underline{\underline{Y}} \\ \underline{\underline{\underline{Y}}} \\ \underline{\underline{Y}} \\ \underline{$

■ Dynamic RAMs (continued)

Memory Size	Type No.	Memory Composition	Access Time	Cycle Time	Refresh Cycle (cycle/ms)	Supply Voltage (V)	Power Con		Package		Process	Remarks
(bit)		(Word × bit)	max. (ns)	min. (ns)			Operating	Stand-by		No.		remand
	▲MN42V4400SJ-06 ▲MN42V4400SJ-07 ▲MN42V4400SJ-08	1,048,576 × 4	60 70 80	110 130 150	1024/16ms	3.0 ~ 3.6	288 252 216		SOJ026-P-0300A	M20		
	▲MN42V4400TT-06 ▲MN42V4400TT-07 ▲MN42V4400TT-08		60 70 80	110 130 150			288 252 216	0.18 (CMOS level)	TSOP026-P-0300A	M35	смоѕ	High-speed page modeCBR-self-refresh
4M	▲MN42V4400TTR-06 ▲MN42V4400TTR-07 ▲MN42V4400TTR-08		60 70 80	110 130 150			288 252 216		TSOP026-P-0300AR	M36		
	▲MN42V4800SJ-06 ▲MN42V4800SJ-07 ▲MN42V4800SJ-08		60 70 80	110 130 150			288 252 216		SOJ028-P-0400	M21		
	▲MN42V4800TT-06 ▲MN42V4800TT-07 ▲MN42V4800TT-08	524,288 × 8	60 70 80	110 130 150	1024/16ms	3.0 ~ 3.6	288 252 216	0.18 (CMOS) level	TSOP028-P-0400	M37	CMOS	High-speed page modeCBR-self-refresh
	▲MN42V4800TTR-06 ▲MN42V4800TTR-07 ▲MN42V4800TTR-08		60 70 80	70 130			288 252 216		TSOP028-P-0400R	M38	_	
	MN4116100SJ-08	10.757.910		150	4096/64ms	4.5 ~ 5.5	522.5	11 (TIL level)	SOJ028-P-0400A	M22		
	MN4116100TT-08	16,777,216 × 1	80						TSOP028-P-0400A	М39	CMOS	 High-speed page mode
	MN4116100TTR-08]							TSOP028-P-0400AR	M40	1	<u> </u>
	MN4116400SJ-08	4,194,304 × 4			4096/64ms		522.5	1.1 (CMOS) level	SOJ028-P-0400A	M22	CMOS	High-speed page mode
	MN4116400TT-08		80	150		4.5 ~ 5.5			TSO P028-P-0400A	M39		
	MN4116400TTR-08							ĺ .	TSOP028-P-0400AR	M40		F-84
	MN4117100SJ-08	16,777,216 × 1	80					11	SOJ028-P-0400A	M22		
	MN4117100TT-08			150	2048/32ms	4.5 ~ 5.5	687.5	(TIL)	TSOP028-P-0400A	M39	CMOS	 High-speed page mode
	MN4117100TTR-08							(level)	TSOP028-P-0400AR	M40		1 3
	MN4117400SJ-08		80		2048/32ms	4.5 ~ 5.5		1.1	SOJ028-P-0400A	M22		
	MN4117400TT-08	4,194,304 × 4		150			687.5	(CMOS level	TSOP028-P-0400A	M39	CMOS	 High-speed page mode
	▲MN4117400TTR-08								TSOP028-P-0400AR	M40	1 1	
16M	▲MN41V16100SJ-05	16,777,216 × 1	50	90		3.0 ~ 3.6	288 252 216 180	1.8	SOJ026-P-0300B	M19	CMOS	High-speed page mode
	▲MN41V16100SJ-06		60	110	4096/64ms							
	▲MN41V16100SJ-07		70 80	130 150								
	▲MN41V16100SJ-08											
	▲MN41V16400SJ-05		50	90			288					
	▲MN41V16400SJ-06	4,194,304	60	110	4096/64ms	3.0 ~ 3.6	252	1.8	SOJ026-P-0300B	M19	CMOS	High-speed page mode
	▲MN41V16400SJ-07	$\times 4$	70 80	130 150			216 180					
	▲MN41V16400SJ-08											
	▲MN41V17100SJ-05		50	90			468					
	▲MN41V17100SJ-06	16,777,216 × 1	60	110	2048/32ms	3.0 ~ 3.6	396	1.8	SOJ026-P-0300B	M19	CMOS	High-speed
	▲MN41V17100SJ-07		70 80	130 150			324 288	1.8	.9.2.2 00000			page mode
	▲MN41V17100SJ-08						20					
	▲MN41V17400SJ-05		50	90	2048/32ms	3.0 ~ 3.6	468					-
	▲MN41V17400SJ-06	4,194,304	60	110			396	1.8	SOJ026-P-0300B	M19	CMOS	● High-speed
	▲MN41V17400SJ-07] ×4	70 80	130 150			324 288		-5-201 0000D		2200	page mode
l	▲MN41V17400SJ-08											

[▲] Under development

 $\begin{array}{ll} \text{(Package Symbol)} & \text{DIC} = \underline{\underline{D}} \text{ual-}\underline{\underline{I}} \text{n-Line }\underline{\underline{C}} \text{eramic Package, DIP} = \underline{\underline{D}} \text{ual-}\underline{\underline{I}} \text{n-Line }\underline{\underline{P}} \text{lastic Package, SOW} = \underline{\underline{S}} \text{mall }\underline{\underline{O}} \text{utline Package} \\ \text{SOJ} = \underline{\underline{S}} \text{mall }\underline{\underline{O}} \text{utline }\underline{\underline{J}} \text{-} \text{Bend Package, SOP} = \underline{\underline{S}} \text{mall }\underline{\underline{O}} \text{utline }\underline{\underline{P}} \text{ackage} \\ \end{array}$

■ Dynamic RAMs (continued)

Memory Size (bit)	Туре No.	Memory Composition (Word × bit)	Access Time max. (ns)	Cycle Time min. (ns)	Refresh Cycle (cycle/ms)	Supply Voltage (V)	Power Con max. (Operating		Package	No.	Process	Remarks
	▲MN42V16100SJ-05 ▲MN42V16100SJ-06 ▲MN42V16100SJ-07 ▲MN42V16100SJ-08	16,777,216 × 1	50 60 70 80	90 110 130 150	4096/256ms	3.0 ~ 3.6	288 252 216 180	0.36	SOJ026-P-0300B	M19	CMOS	● High-speed page mode
16M	▲MN42V16400SJ-05 ▲MN42V16400SJ-06 ▲MN42V16400SJ-07 ▲MN42V16400SJ-08	4,194,304 × 4	50 60 70 80	90 110 130 150	4096/256ms	3.0 ~ 3.6	288 252 216 180	0.36	SOJ026-P-0300B	M19	CMOS	● High-speed page mode
	▲MN42V17100SJ-05 ▲MN42V17100SJ-06 ▲MN42V17100SJ-07 ▲MN42V17100SJ-08	16,777.216 × 1	50 60 70 80	90 110 130 150	2048/256ms	3.0 ~ 3.6	468 396 324 288	0.36	SOJ026-P-0300B	M19	cmos	● High-speed page mode
	▲MN42V17400SJ-05 ▲MN42V17400SJ-06 ▲MN42V17400SJ-07 ▲MN42V17400SJ-08	4,194,304 . × 4	50 60 70 80	90 110 130 150	2048/256ms	3.0 ~ 3.6	468 396 324 288	0.36	SOJ026-P-0300B	M19	CMOS	High-speed page mode

[▲] Under development

 $\begin{array}{ll} ({\sf Package \: Symbol}) & {\sf DIC} = \underline{{\sf D}ual\text{-}}\underline{{\sf In\text{-}Line}\: \underline{{\sf Ceramic\: Package}}, {\sf DIP} = \underline{{\sf D}ual\text{-}}\underline{{\sf In\text{-}Line\: \underline{P}lastic\: Package}}, {\sf SOW} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}} \\ & {\sf SOJ} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}} \\ & {\sf SOJ} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf S}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ & {\sf SOP} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\: \underline{P}ackage}}, \\ \\ & {\sf Q} = \underline{{\sf Q}mall\: \underline{{\sf Q}utline\:$