Chapter 3 — Enhanced Timers

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- Timers Introduction
- Enhanced Timer Programming

Timers Introduction

This section provides the information necessary for software engineers to program and use the extension enhanced timers.

The enhanced timers, up to two, can be selected at configuration stage. Enhanced timer 0, if selected, is connected by default to the low priority “irq3” interrupt line. Enhanced timer 1, if selected, is by default connected to the high priority “irq7” interrupt line.

Feature Summary

- Support for up to two 32-bit enhanced timers – selected at configuration stage.
- Timers automatically reset and restart their operation after generating an interrupt.
- Timers can be programmed to count all clock cycles or only the clock cycles when the processor is not halted.
- Timers can be programmed to generate a system reset.

Enhanced Timer Programming

Enhanced timer 0 and timer 1 are almost identical, the only difference being that timer 0 is connected to interrupt line “irq3” and timer 1 is connected to interrupt line “irq7”. Either one or both timers may be selected at configuration time.

The enhanced timers are connected to a system clock signal that operates even when the processor is in sleep mode. This enables the timers to be used to generate interrupt signals that will “wake” the processor from sleep mode.

- Timer 0
- Timer 1
- Programming
- Build Configuration Register

Timer 0

Timer 0 has three registers mapped in the auxiliary register address space as shown below.

Table 1 Timer 0 Registers

Register name	Register address	Description
Count	0x21	Initial timer count value
Control	0x22	Timer operating mode
Limit	0x23	Counting limit value

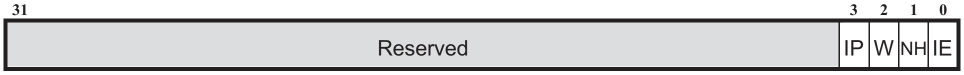

Figure 4 Timer 0 Control Register

- (IE) Interrupt Enable flag – enables the generation of an interrupt after the timer has reached its limit condition. If this bit is not set then no interrupt will be generated.

  IE = 0 at reset

  IE = 0 Interrupt generation disabled

  IE = 1 Interrupt generation enabled

- (NH) Not Halted mode – setting of this flag causes cycles to be counted only when the processor is not halted.

  NH = 0 at reset

  NH = 0 Count every clock cycle

  NH = 1 Count clocks only when processor is not halted

- (W) Watchdog mode – enables the generation of a system reset signal after the timer has reached its limit condition. If this bit is not set then no watchdog reset will be generated. Note that the reset signal is activated two cycles after the limit condition has been reached.

  W = 0 at reset

  W = 0 Watchdog reset generation disabled

  W = 1 Watchdog reset generation enabled

- (IP) Interrupt Pending flag –this read only flag reflects the value of the timer interrupt line (irq3)

  IP = 0 indicates the value of the interrupt line is low

  IP = 1 indicates the value of the interrupt line is high

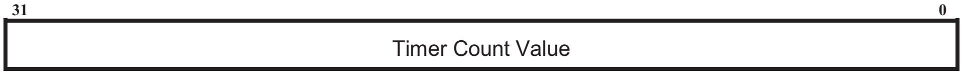

Figure 5 Timer 0 Count Value Register

The Timer count value is a read/write register. Writing to this register sets the initial count value for the timer. Subsequently, the register can be read to reflect the timer 0 count progress.

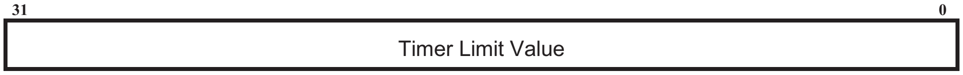

Figure 6 Timer 0 Limit Value Register

The Timer Limit value is a read/write register. The programmer should write the limit value into this register. The limit value is the value after which an interrupt is to be generated.

Timer 1

Timer 1 has three registers mapped in the auxiliary register address space as shown below.

Table 2 Timer 1 Registers

Register name	Register address	Description
Count	0x100	Initial timer count value
Control	0x101	Timer operating mode
Limit	0x102	Counting limit value

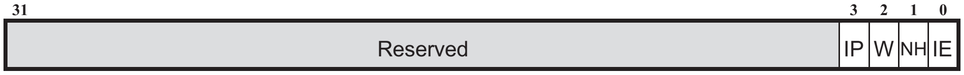

Figure 7 Timer 1 Control Register

- **(IE)** Interrupt Enable flag – enables the generation of an interrupt after the timer has reached its limit condition. If this bit is not set then no interrupt will be generated.

  IE = 0 at reset

  IE = 0 Interrupt generation disabled

  IE = 1 Interrupt generation enabled

- **(NH)** Not Halted mode – setting of this flag causes cycles to be counted only when the processor is not halted.

  NH = 0 at reset

  NH = 0 Count every clock cycle

  NH = 1 Count clocks only when processor is not halted

- **(W)** Watchdog mode – enables the generation of a system reset signal after the timer has reached its limit condition. If this bit is not set then no watchdog reset will be generated. . Note that the reset signal is activated two cycles after the limit condition has been reached.

  W = 0 at reset

  W = 0 Watchdog reset generation disabled

  W = 1 Watchdog reset generation enabled

- (IP) Interrupt Pending flag –this read only flag reflects the value of the timer interrupt line (irq7)

  IP = 0 indicates the value of the interrupt line is low

  IP = 1 indicates the value of the interrupt line is high

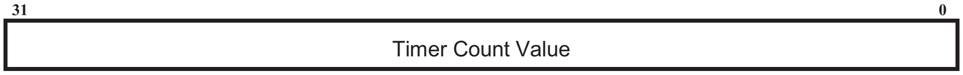

Figure 8 Timer 1 Count Value Register

The Timer count value is a read/write register. Writing to this register sets the initial count value for the timer. Subsequently, the register can be read to reflect the timer 1 count progress

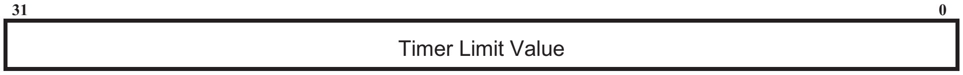

Figure 9 Timer 1 Limit Value Register

The Timer Limit value is a read/write register. The programmer should write the limit value into this register. The limit value is the value after which an interrupt is to be generated.

Programming

The Timer starts counting from the “count” value upwards until it reaches the “limit” value after which a level type interrupt is generated. It then automatically restarts to count from 0 upward until it reaches the limit value again and the cycle is repeated until the control register is updated. It is up to the software to clear the timer interrupts. Once an interrupt is generated, writing to the “control” register clears it. This should be performed during the interrupt service routine.

In order to program the enhanced timer, the user writes the limit value in to the timer “limit” register. Next, the programmer sets up the control flags according to the desired mode of operation by updating the timer “control” register. Finally, the count value is written in to the timer “count” Register. There is no bit addressing capability in the auxiliary address space and thus all of the control flags should be programmed in one write access to the control register.

The timer Limit register is set to 0x00FFFFFF at reset for full backward compatibility. If updated, then it can always be reset to 0x00FFFFFF for backward compatible mode of operation.

The “count” register may be updated even when the timer is running in which case the internal count register is updated with the new count value and the timer starts counting up from the updated value.

The programming of the watchdog reset signal is similar except that the (W) control bit should be set. The system reset signal will be activated two cycles after reaching the limit value (it takes one cycle for the interrupt to be activiated). If both the (IE) and (W) bits are set then only the watchdog reset is activiated since the reset will clear the processor and the interrupt will be lost anyway.

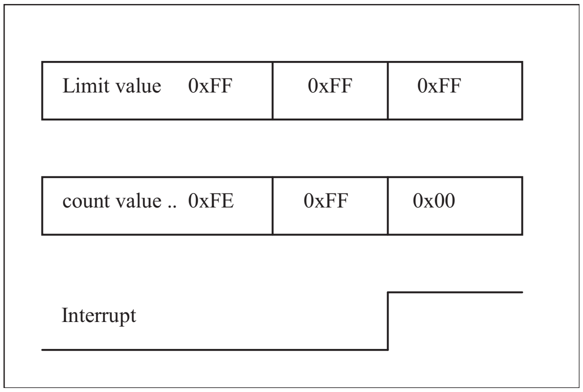

Figure 10 Interrupt Generated after Timer Reaches Limit Value

Build Configuration Register

A new Build Configuration Register (timer_build_value) is defined at the auxiliary address space at location [0x75] to indicate the presence of enhanced timers.

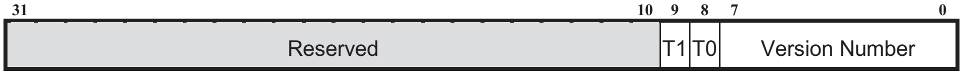

Figure 11 "Timer_Build_Register" BCR

- The whole register is read only and writes to this location have no effect
- Bits 10 up to 31 are reserved for future use and read back as 0x0.
- Bit 9 (T1) when set indicates that enhanced timer 1 is present.
- Bit 8 (T0) when set indicates that enhanced timer 0 is present.
- Bits 0-7 indicate the version number of the enhanced timers (currently 0x03). If no timers are present then the version number field is set to 0x00. If either timer 0 or timer 1 is present then the version number is set to 0x03.