Delta Smart House

Acoustic Monitoring

Dan Choi

BME/EE 05’

Abstract: Acoustic monitoring has been a largely unexplored area of research. Typical observational research has been concentrated on visual monitoring involving cameras in areas such as face recognition and tracking. The main reason the acoustic monitoring project has become a priority is because MERL (Mitsubishi Electronics Research Laboratories) is interested in a joint effort to develop an entire microphone array system to be used in the DELTA Smart House for acoustic monitoring. This opportunity is the first that involves collaboration with another research lab which makes this project particularly interesting and necessary for the Smart House to expand its network of research.

The motivation behind acoustic monitoring lies in developing reliable way to monitoring the activities and equipment inside the house. With enough microphones, the source and identity of a noise can be determined. This process of noise location and identification can be used to determine a spatially accurate image of a room, even in complete darkness. Imaging a room opens up many security possibilities as the noises of an intruder could be easily tracked and reported to a security company or the police. Additionally, the acoustic monitoring offers a preventative measure for system failure. Oftentimes, the first characteristic that changes in the event of impending failure is the acoustic pattern of a system. Monitoring the sounds of all the various systems in a house would allow the homeowner to predict system failure and repair the system before anything disastrous occurs.

Once completed, the proposed acoustic monitoring system will be fairly modular, which will allow it to be added, removed, or changed in a fairly simple

manner. The system can therefore be inserted into the house at almost any point after the completed construction of the house.

Background Information

There two main technologies that exist that the acoustic monitoring project will be based on: the NIST Mark III microphone array design and the large scale microphone array developed by MIT. Both projects offer ideas of how to build and use a microphone array but are different enough for us to warrant developing our own array.

The Mark III microphone array by NIST is a 64 microphone array design that will be used as a basis for the 1024 microphone array which will be developed for the Smart House. The 64 microphone array design will be daisy chained to form an array big enough for the acoustic monitoring project. The hardware for the Mark III is broken up into a mother board and 8 microboards. The microboard is comprised of microphones, amplifiers, and analog to digital converters. The figure below shows the microboard.

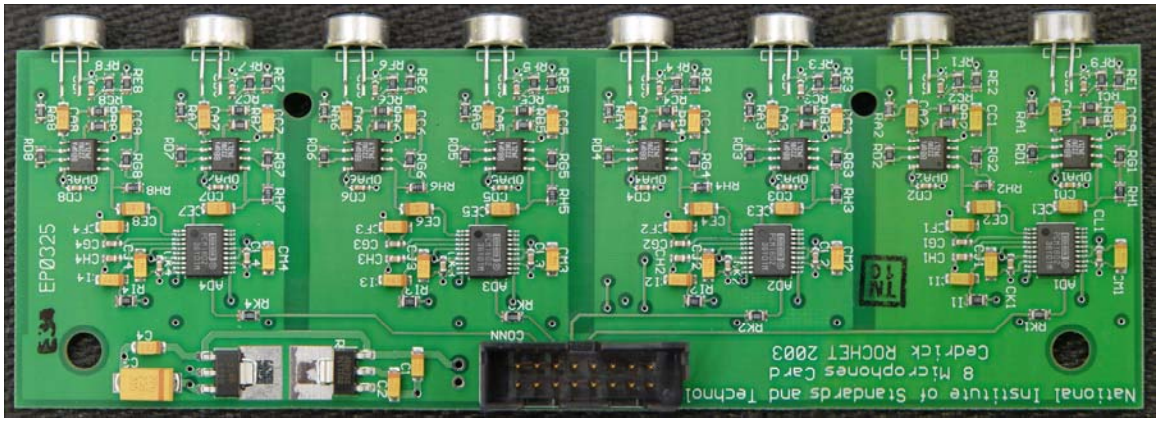

Figure 1: NIST Mark II Microboard

The analog to digital converter translates the audio information into data that can be read by a computer. Because there will be so many analog to digital converters involved with

the large scale microphone array, the integrity of the clock that feeds into the ADC's is important to providing accurate audio data. In order to daisy chain the motherboards and microboards, the clock integrity must be maintained to within 1ns. The Mark III model works within the 1ns error, but whether it remains within the 1ns when 1024 microphones are put together has not been determined.

In the first iteration of the Mark microphone array, a DSP board was attached to the microboards as well but then later removed in the Mark III design. Due to the large number of inputs that will exist because of the 1024 transducers, a DSP board will be added again to the microboards. The added DSPs will perform beamforming, which will allow certain data to be selected out and transmitted instead of wasting bandwidth by transmitting all the data simultaneously.

MIT currently has a working 1020 microphone array, which is the closest technology to what the acoustic monitoring project aims to develop.

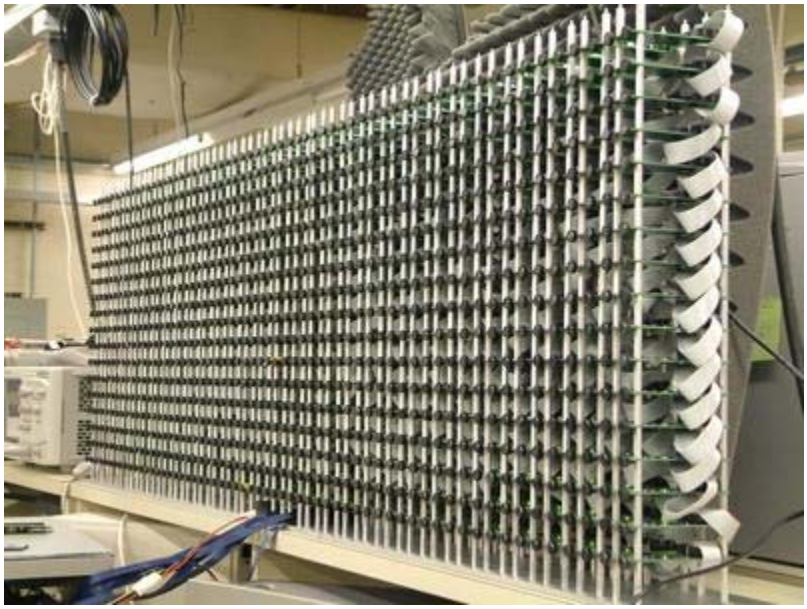

Figure 2: 1020 Microphone LOUD (Large Acoustic Data Array Project at MIT)

The array is of the same scale that the Smart House wishes to develop while also utilizing DSP chips to perform beamforming. The main differences between the MIT microphone array and the proposed Smart House array are the test bed for the array and the purpose behind the array. The MIT microphone array was developed to display the capacity of the DSP chip that was designed specifically for the microphone array. The test bed of MIT's array is simply a lab area set up with a rectangular outline comprised of the microphones. The Smart House and MERL microphone array is being developed for monitoring mechanical systems in the house as well as for surveillance purposes. The test bed has a much more interesting test bed than the rectangular shape used by MIT, a house.

In order for the array to be suitable to fit inside a house, the design for the chips will need to change from the linear, 8-microphone model, to a more modular, 2-microphone model. If the lines from the microboard to the microphone become different distances, the capacitances that build up from the traveled lines will also need to be taken into account as they will affect the 1ns clock integrity goal.

The acoustic monitoring project should fit well into the Smart House as there are other planned monitoring systems. By combining with the possible face recognition projects or the RFID tracking project, acoustic monitoring will be another layer of monitoring, which would add to the robustness of the tracking systems of the house.

Technical Discussion

The 1ns threshold of the clock is a result of dealing with a problem called clock skew. Whenever a signal is transmitted through different branches of wire, the distances

traveled and the subtle differences in fabrication can lead to the same outputs not occurring simultaneously. The difference between the data arrival time of the slowest data lines and the fastest data line is called clock skew. The minute differences are typically not important; however, in this case, the minute differences can be important to the ADC, which runs at a clock speed of several hundred megahertz. Had the project been completely analog without the need for data acquisition, the clock skew would not be an issue due to the lack of an ADC. Because the ADC is required to analyze and beamform the data, clock skew must be considered. Within the hardware development, clock skew is the main hurdle before the hardware can be fabricated.

Additionally, the current design requires that the microphones be very linear by designing the microboards to hold 8 linearly placed microphones. For the purposes of testing a DSP or demonstrating a technology, the 8 microphone linear placement is sufficient; however, for the purposes of acoustic monitoring inside an active house where different areas of the house require varying densities of microphones, the linear 8 microphone model will not work as well. The physical separation of the microphones from each other should be straightforward, but the electrical effects of the separation have not been tested yet.

Design and Implementation

The main goal of this first portion of the project is to complete the hardware design, which would be followed by fabrication of the boards at MERL. Since the clock buffer on the Mark III is a cdcv304 chip by TI, the cdcv304 was used for some preliminary testing. The clock buffer is the chip that distributes the clock signal to the

rest of the board, therefore, by simulating the behavior of the clock buffer, we can predict the amount of clock skew that will occur. TI posts the IBIS version of the chip on their website for simulation use. The IBIS format is a format that treats the chip that it characterizes like a black box, which allows the manufacturer to release the behavior of the chip without releasing the complete schematics of a chip.

The first step in simulation was to test 3 clock buffer chi[s and see how the clock changes. Fong Ming and I ran the following circuit using IsSpice4:

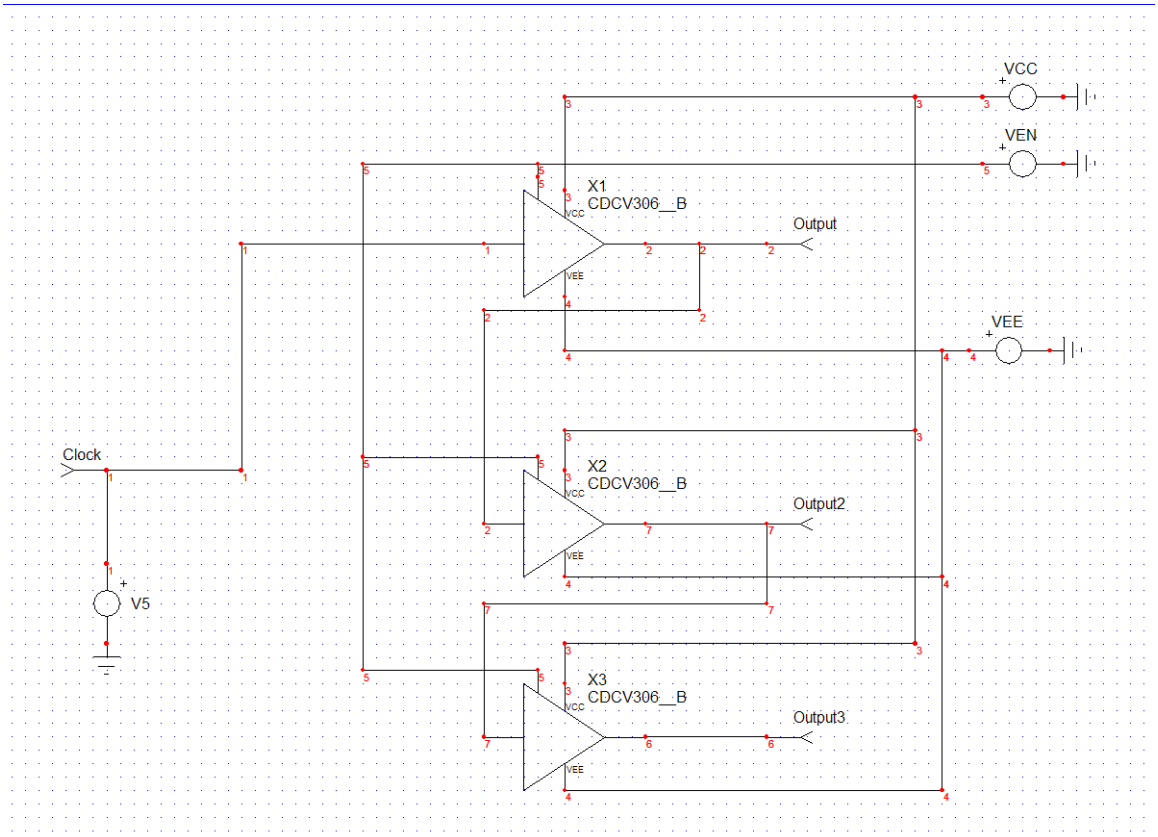

Figure 3: Simulated Clock Buffer Circuit

Only 3 clock buffers were tested due to the limitations of the demo version of IsSpice4. The following graph was the output of the above circuit.

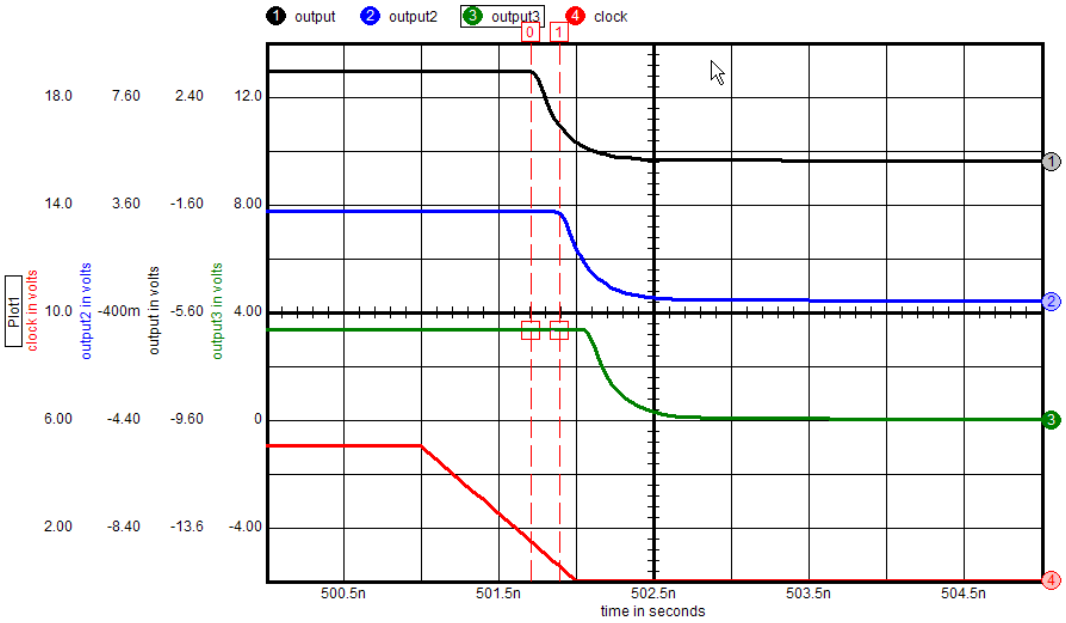

Figure 4: Clock in and output of the buffer circuit

The output clearly shows that there is a discrepancy between the input and the output in addition to a discrepancy between the different outputs, which is essentially the clock skew.

Knowing that clock skew exists between as few as 3 clock buffers, testing needs to be done to see how far reaching the clock skew effects of 192 clock buffers is. Instead of purchasing the $4000 IsSpice4 program, the HSpice program available at Duke will be used in the following manner:

- HSpice files for the needed chips will be directly obtained from TI
- The rise and fall times from the HSpice models will be used to create black boxes of clock skew and load impedances to simulate the clock skew of the buffers
- The capacitance from the traveled lines will be modeled as black boxes as well

Once the buffer circuits can be simulated, a small scale model of the circuit elements that involve the clock will be built in lab to determine the accuracy of the simulations. Once

the small scale simulations are decided to be correct to 1ns, a large scale simulation will be developed, which will precede the construction of the final large circuit.

Contacts Established

Dr. Bhiksha Raj (bhiksha@merl.com)

- Head engineer at MERL involved with the acoustic monitoring project

Dr. James Morizio (jmorizio@ee.duke.edu)

- Duke professor willing to help with HSpice simulation component

Conclusion

The acoustic monitoring project has a lot of potential with a very clear plan of action. The lack of research in the acoustic monitoring area leaves quite a bit of uncertainty as to what will be developed and discovered. The collaboration with MERL will be most valuable and should be aggressively pursued in the coming 2004-2005 year.