॥ सा विद्या या विमुक्तये ॥

भारतीय प्रौद्योगिकी संस्थान धारवाड़

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Reconfigurable Rectifier for RF Energy Harvesting System at WiFi-6 Frequency Band for 2.5 V

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- Simulation Result.
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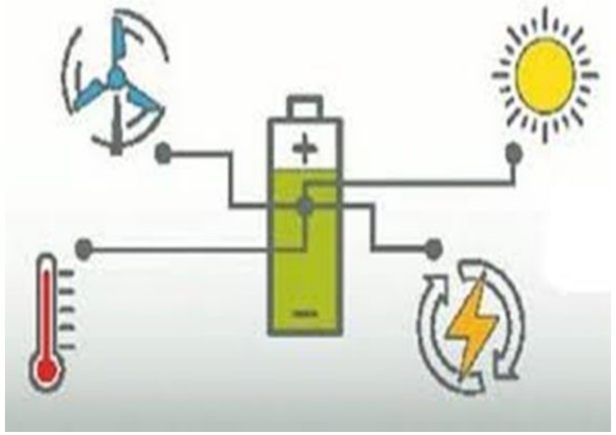
What is Energy Harvesting

Conversion of ambient energy into electrical Energy



Need of Energy Harvesting

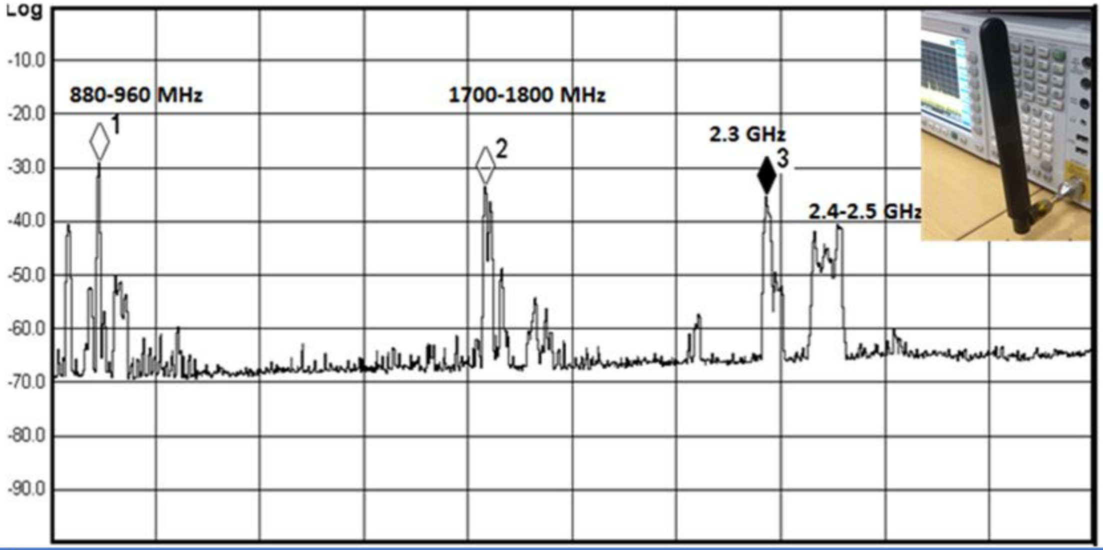
- To extend the Battery life
- Self power

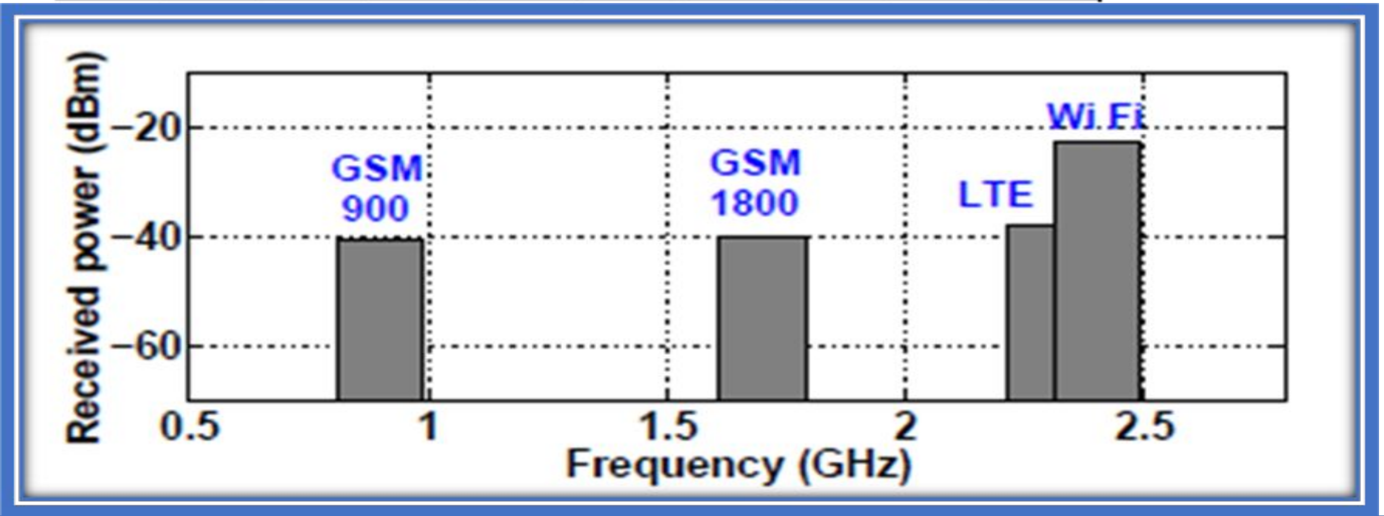
Why RF?

- Ubiquitous
- Easy to introduce in Wireless sensor nodes

Survey of Ambient RF Power

- **Received RF power using immobile R&S FSW50 spectrum analyser and a wideband antenna with a gain of 5 dBi.**





State-of-the-art challenges

- Scavenging lower input power levels
- RF power is spread across multiple bands
- Variation in input power levels
- Antenna to rectifier matching
- Minimization of controller power consumption

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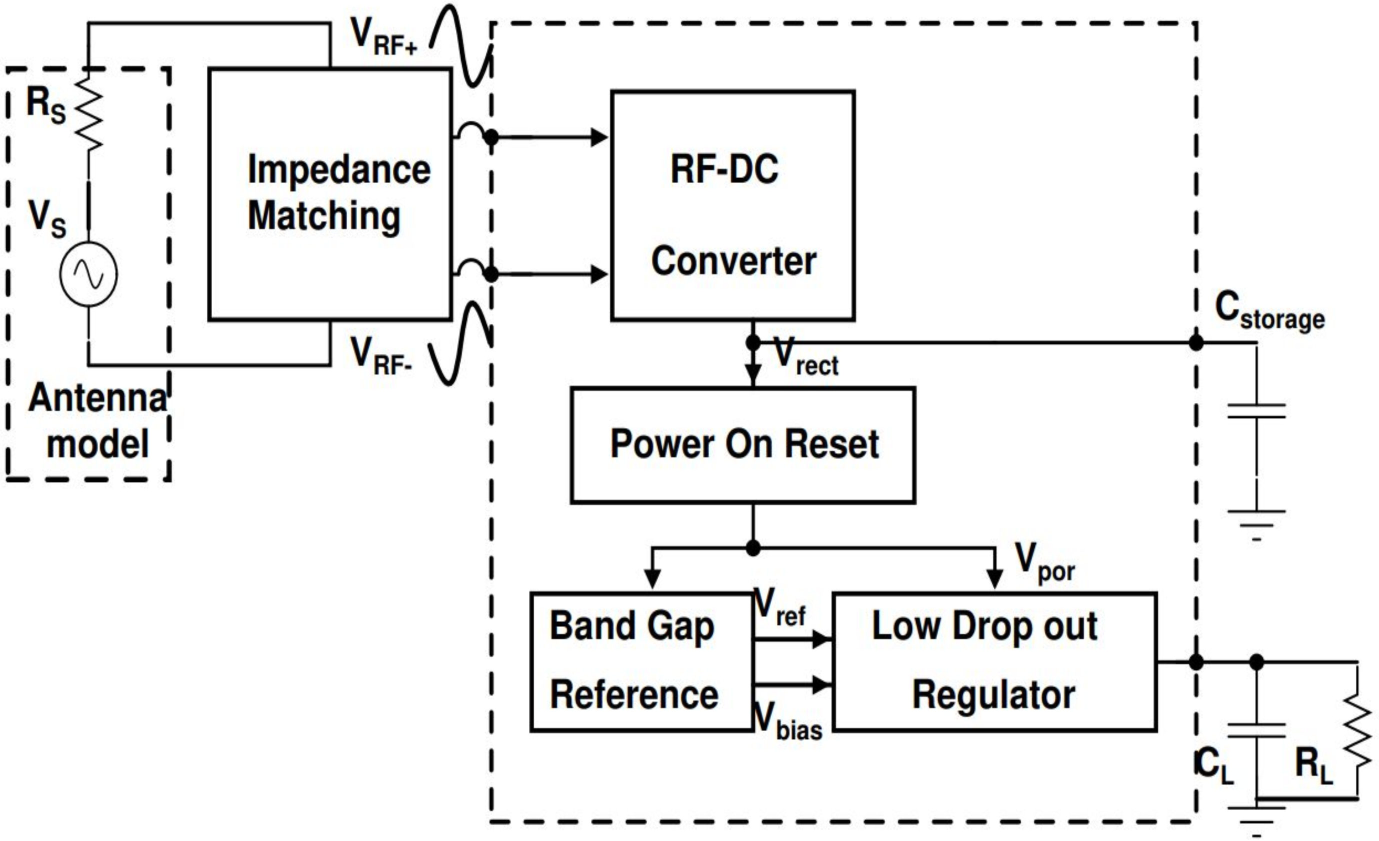
Block Diagram of RF Energy Harvesting



Problem Statement:

- Fluctuations in input power, influenced by time and distance, introduce changes in the rectifier’s impedance and disrupt its optimized operational conditions.
- Rectifier stages need to be configured for effective operation across a wide range of input power levels.

Problem Statement:

RF power is influenced by time and distance

Fluctuation in input power

+

variation in rectifier impedance

disrupts the operational condition

Reconfigurable rectifier stages

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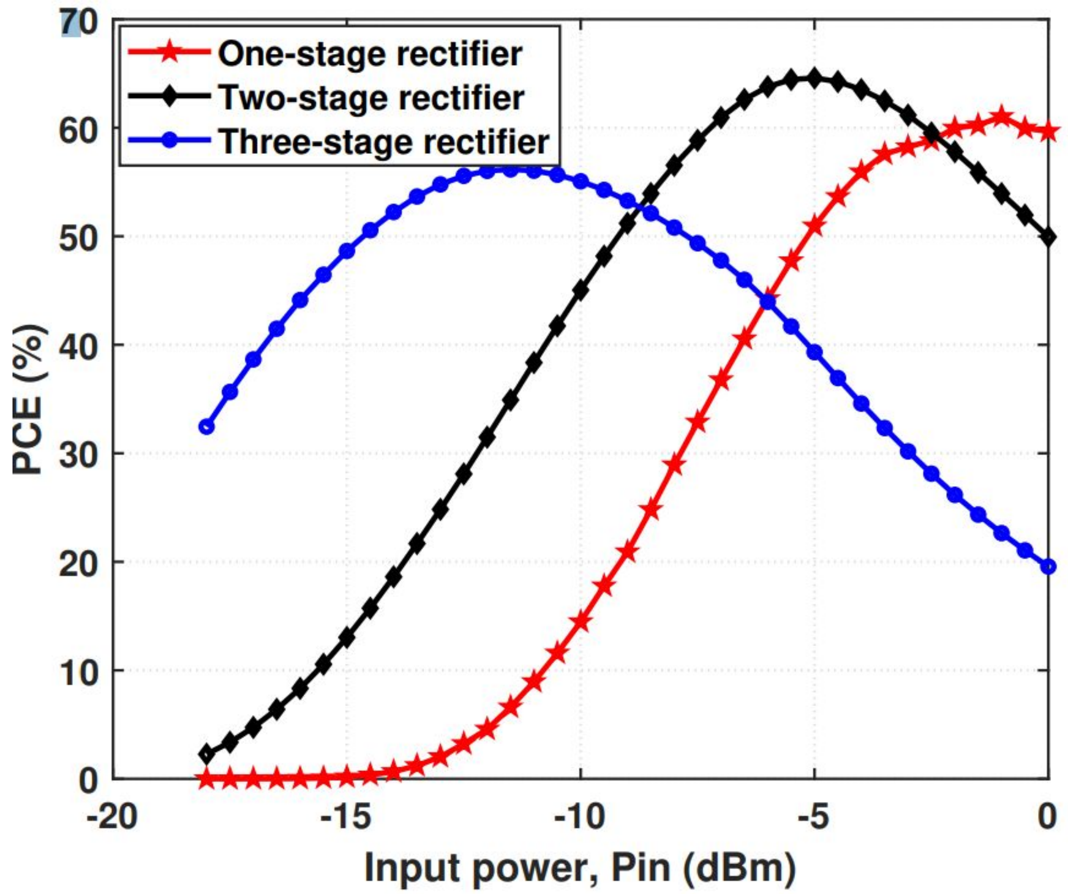
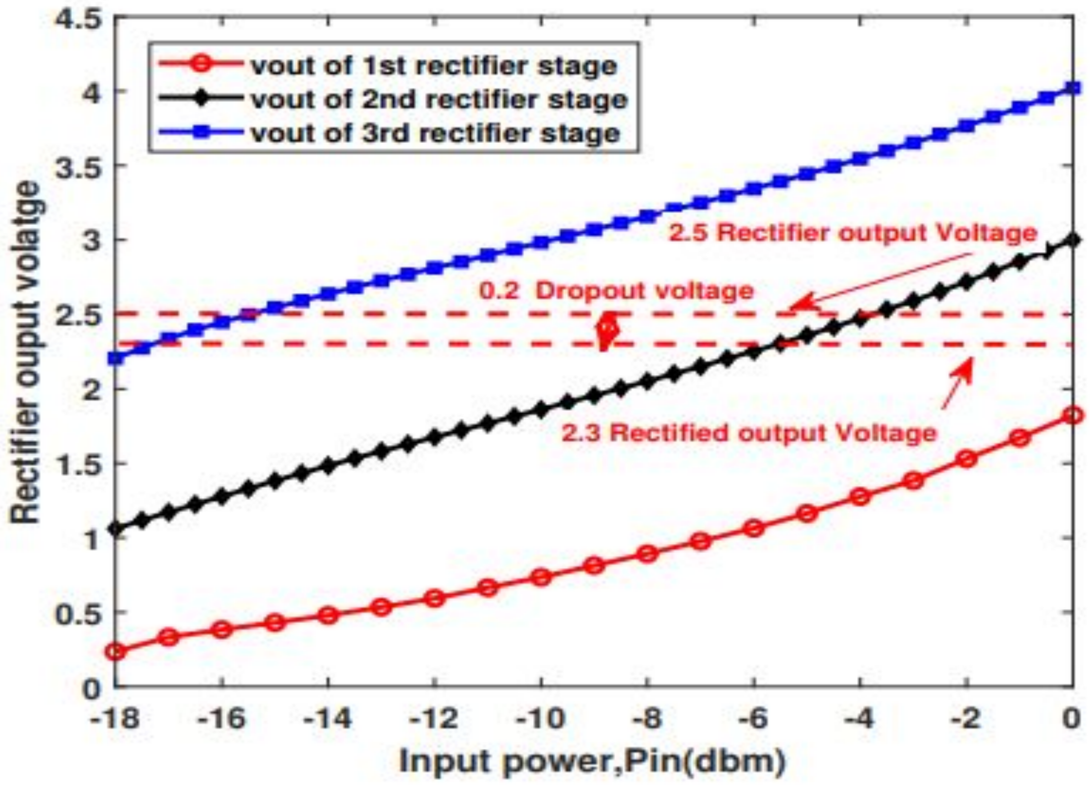
1. PCE of rectifier stages with respect to input power

- Degradation observed at lower and higher power levels due to impedance mismatch.
- Single-stage rectifier recommended at -14 dBm for efficient power conversion.
- Two-stage rectifier performs best at -5 dBm, ensuring optimal power conversion efficiency.



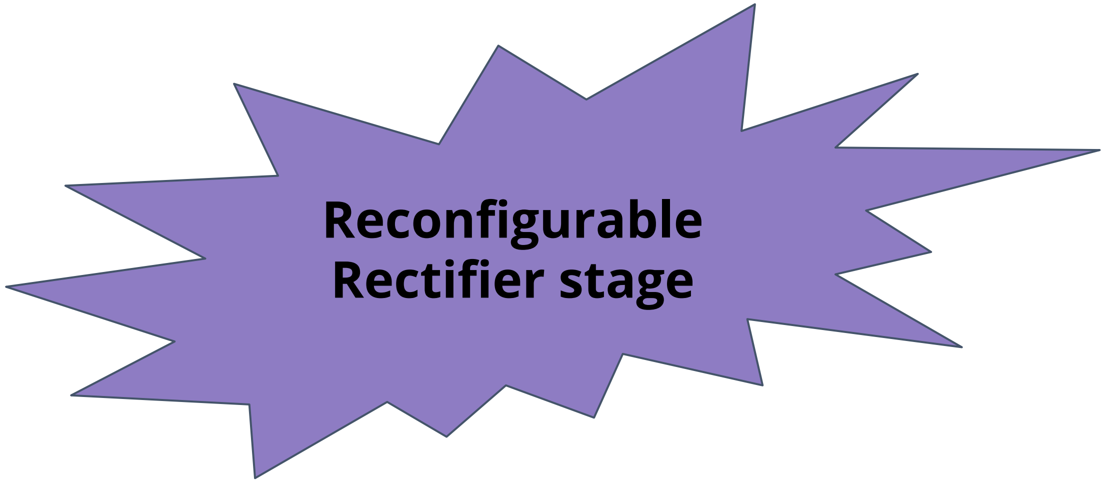
2. Input Power vs. Rectifier Stages

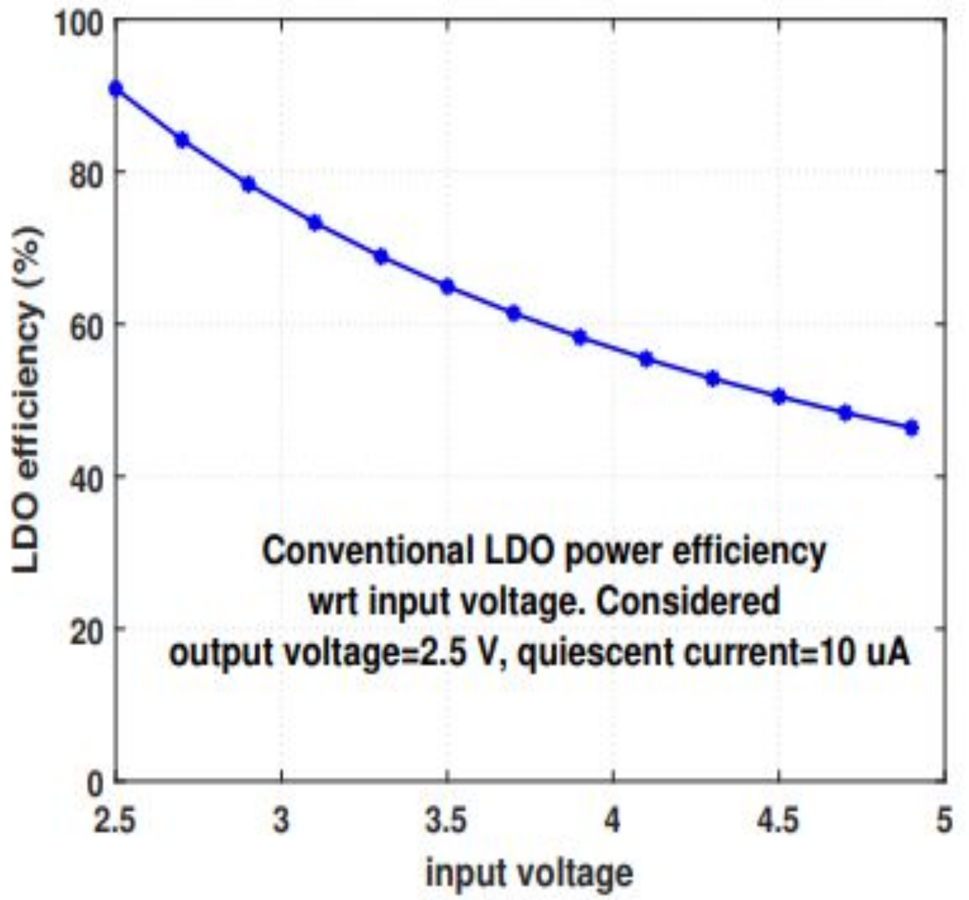
- Lower input power requires more rectifier stages.
- Higher input power requires fewer rectifier stages.



3. Input Voltage vs. LDO Efficiency:

- Optimal efficiency is achieved by setting the input voltage to the regulated voltage plus the dropout voltage.
- Maintaining the input voltage within this range enhances LDO efficiency and overall performance.





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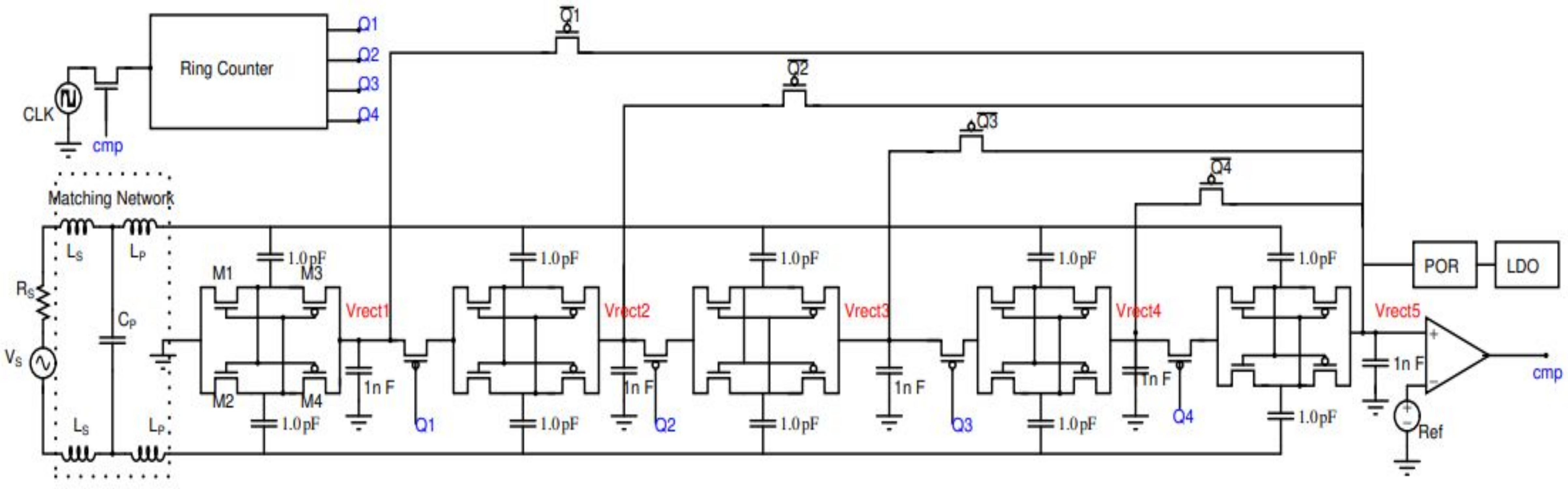
Reconfigurable Rectifier:



Block diagram (Rectifier: M1 = M2 = 3.6 µm / 0.18 µm, M3 = M4 = 18 µm / 0.18 µm)

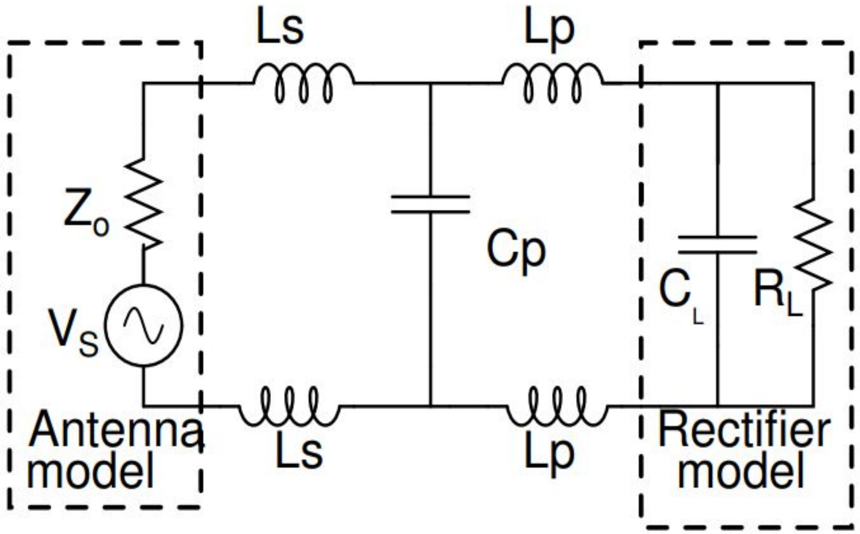
Matching Network:

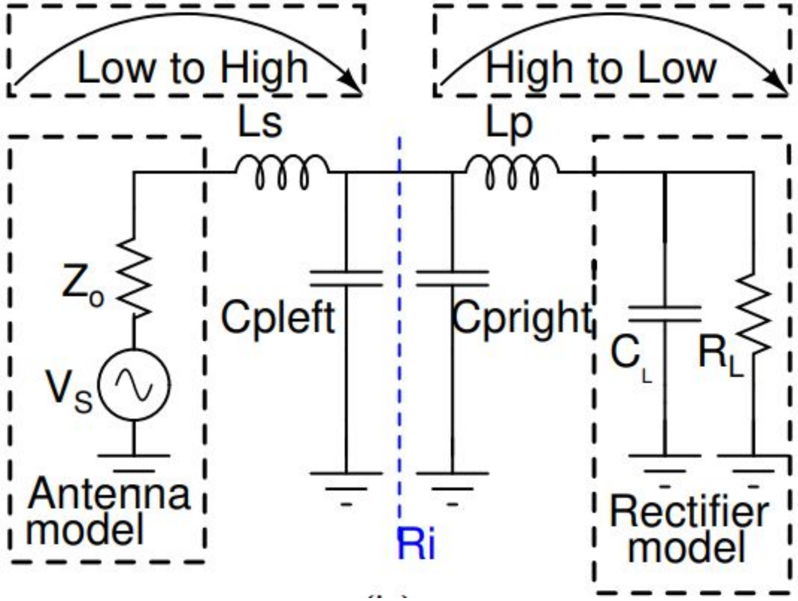
- Impedance matching ensures efficient power transfer from RF source to the load.
- Low to high matching impedance is given as

$$Z_0 = jX_{Ls} + (R_i || -jX_{c_{pleft}})$$

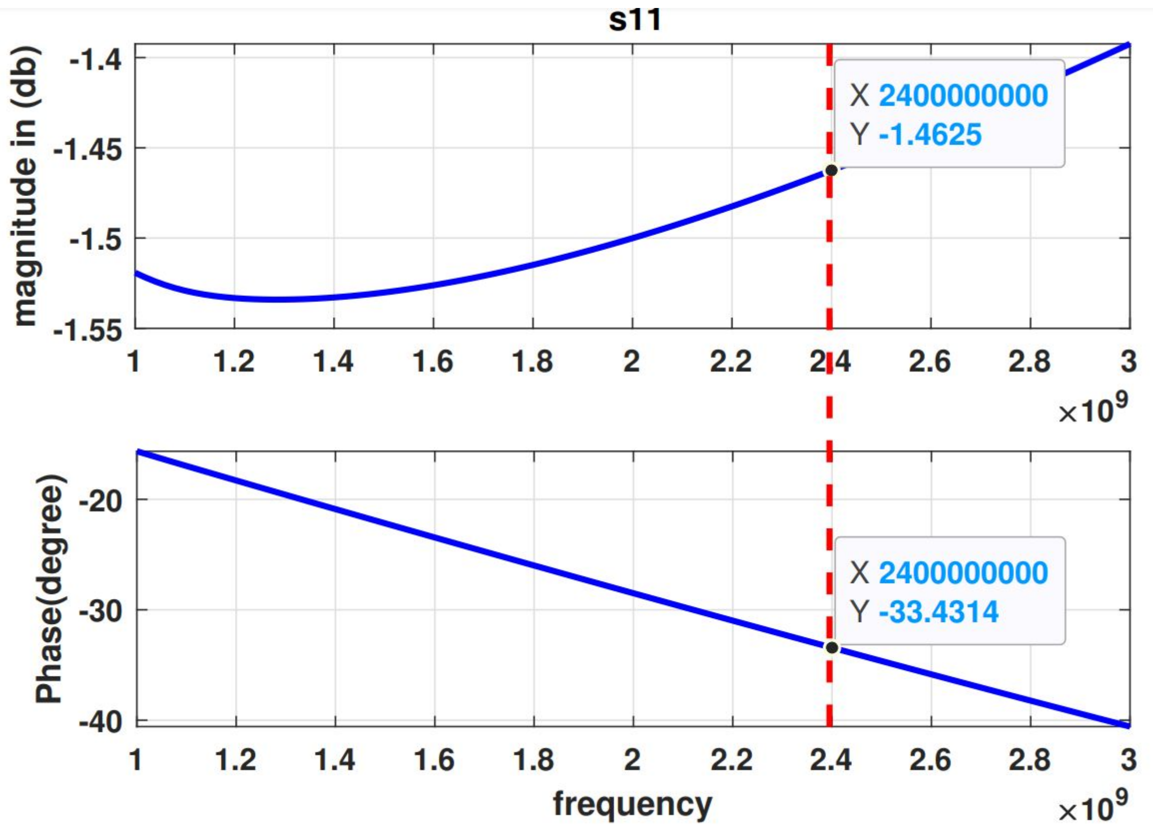
- High to Low matching impedance is given as

$$R_i = (jX_{Lp} + R_L) || -jX_{c_{pright}}$$



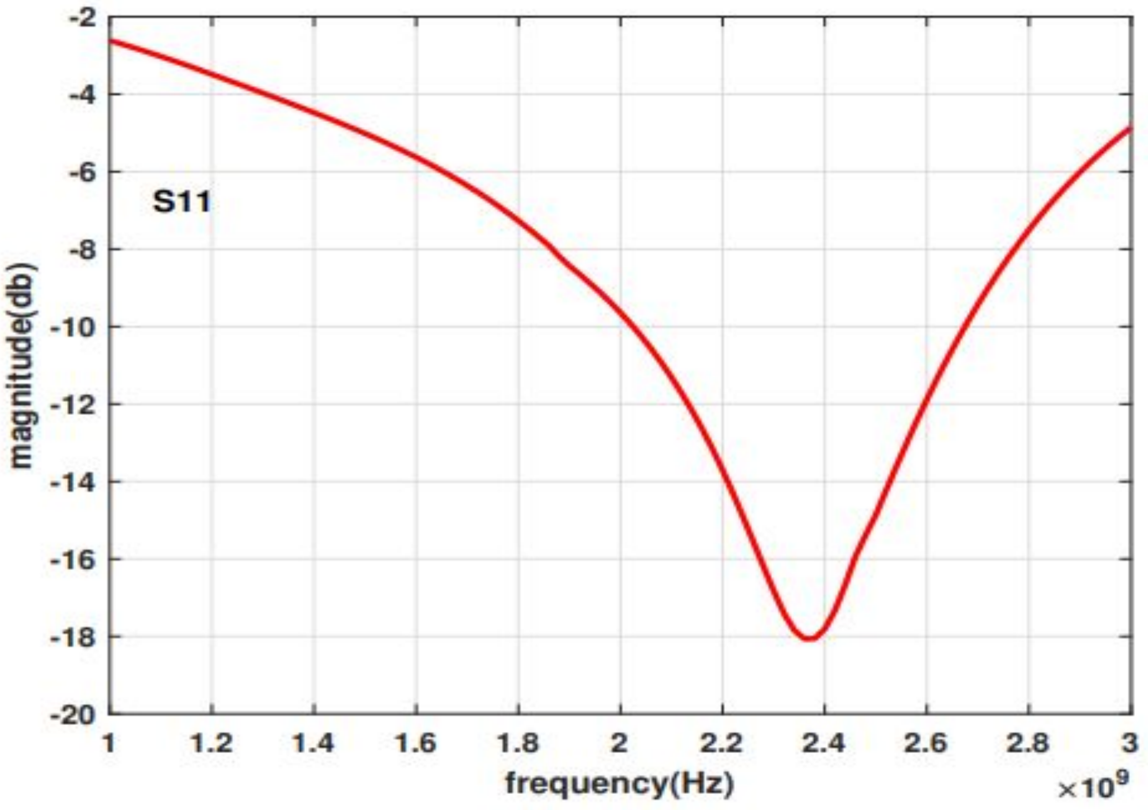


- Impedance of the rectifier is determined using Large Signal Small-Signal Power (LSSP) analysis and Harmonic Balance (HB) analysis in Cadence Virtuoso
- The magnitude and phase of Z_L at 2.4 GHz without impedance matching is -1.465 dB and -33.43 degrees at 2.4 GHz .
- L_S ,L_p and C_P values can be found using R_i and Z_L values.



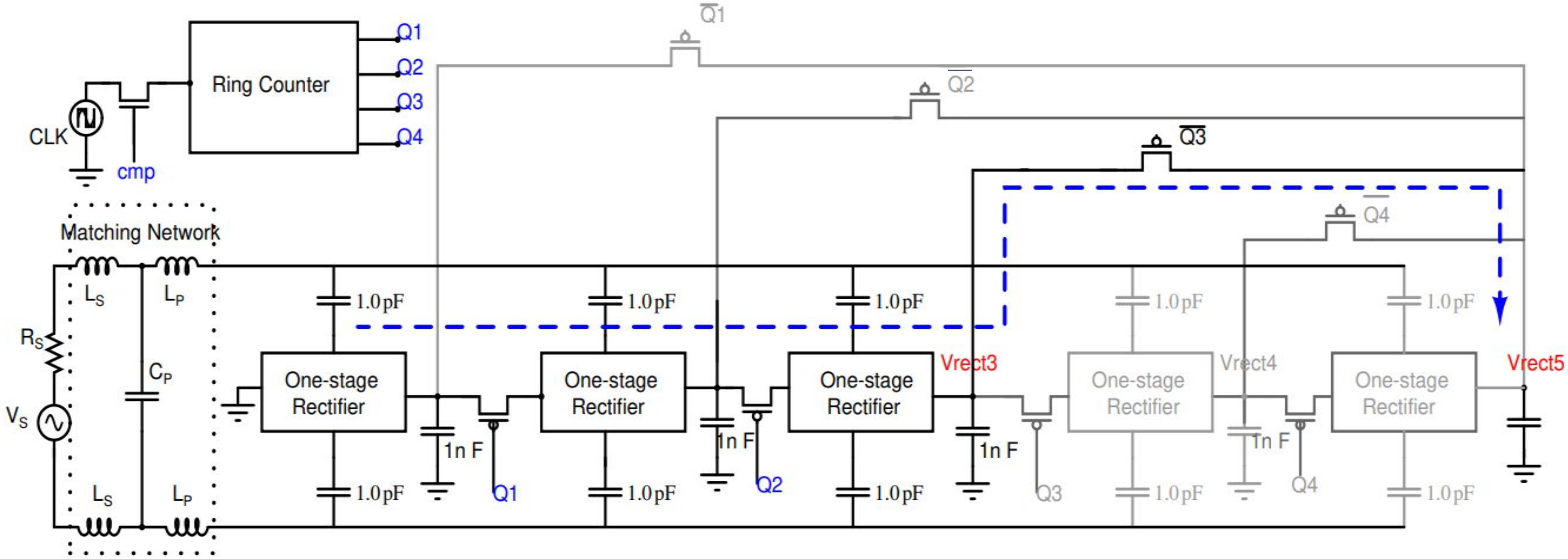
- S11 = 10^(-18/10) = 0.0158 .
- Pin = Ps(1 − |S11|) which makes efficiency

  P_{in} / P_S = 94.37%.



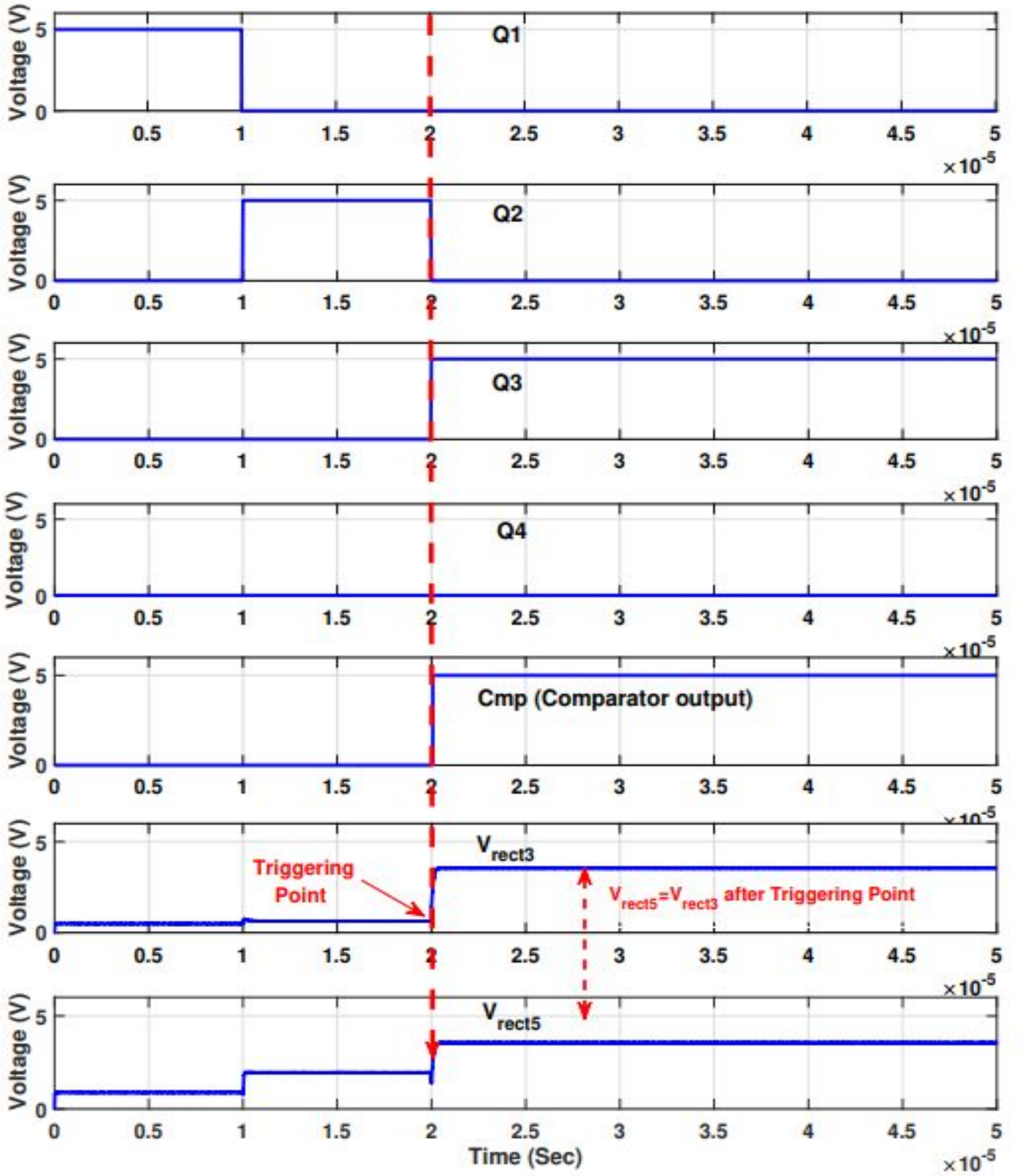
S11 PLot with impedance matching

Working of Reconfigurable Rectifier:



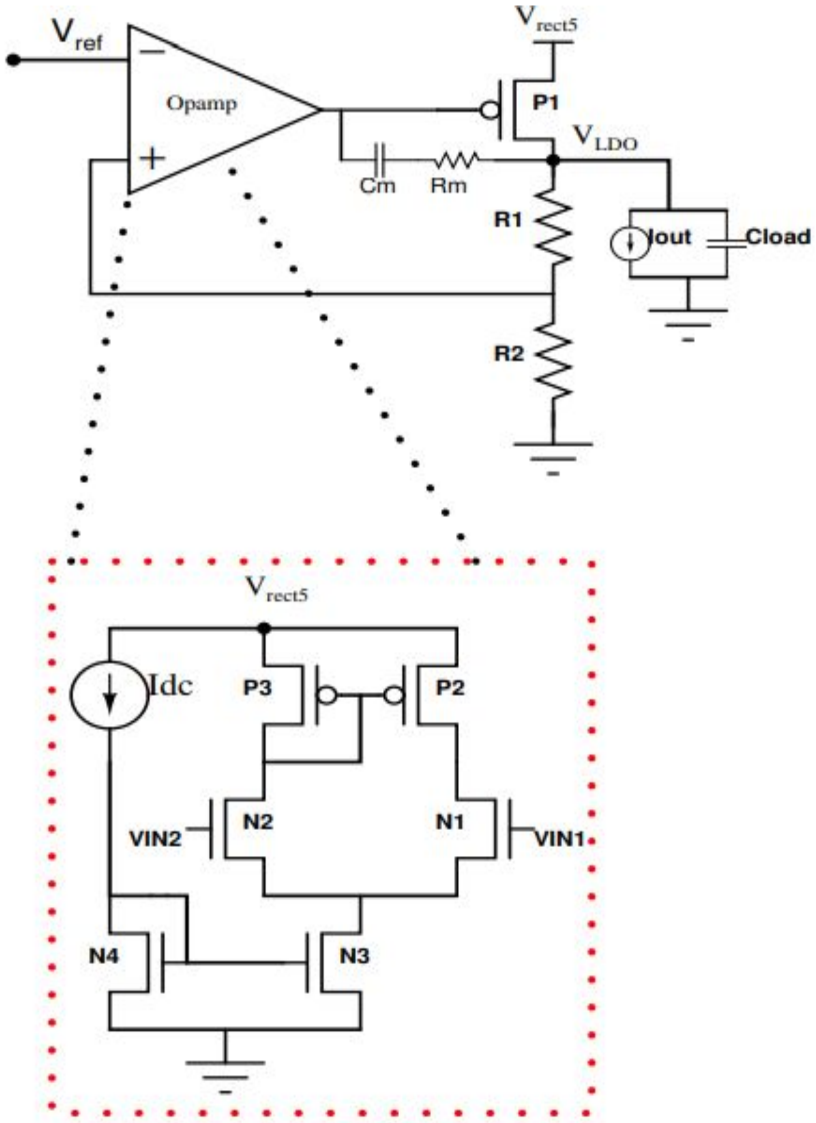
Circuit behaviour as three-stage rectifier at Ps = -5 dBm

- Q3 high state turns off its MOSFET, blocking power to the next stage.
- Q3 MOSFET also shorts third stage output to the final stage.
- Q1 and Q2 switches enable power flow to the third stage.
- Third stage output above 2.5 V triggers the comparator, producing a high output which halts the ring counter.



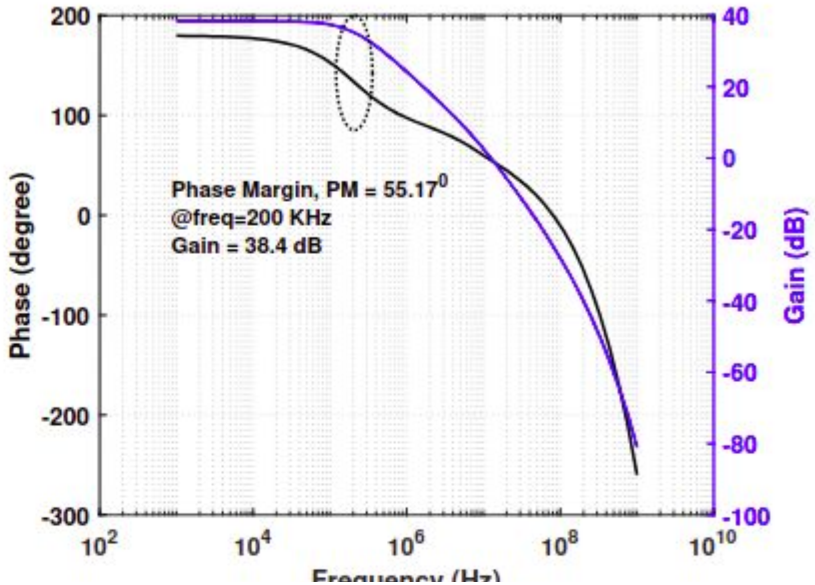
LDO (Low Dropout Regulator):

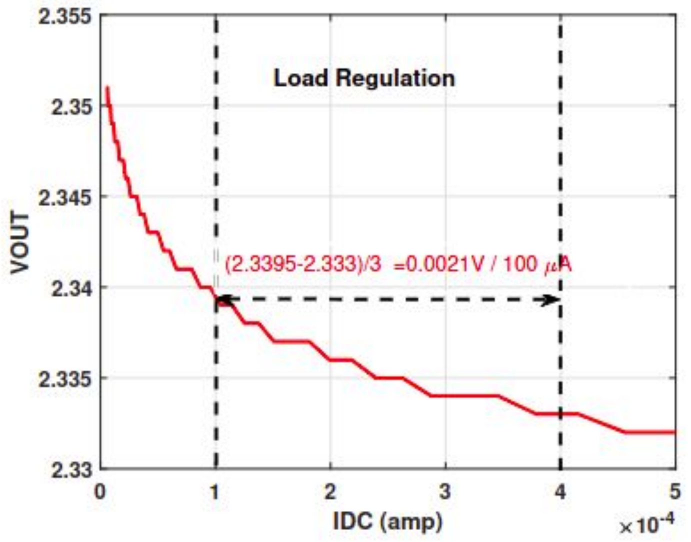
- The LDO schematic integrates NMOS and PMOS transistors.
- The specific compensating components are a 600 fF Miller capacitor and a 1.6 kOhm resistor.
- These components aim to achieve the desired phase margin and bandwidth.
- Resistors R1 and R2 are tailored to attain a 2.3 V output with a 1.725 V reference signal.



LDO

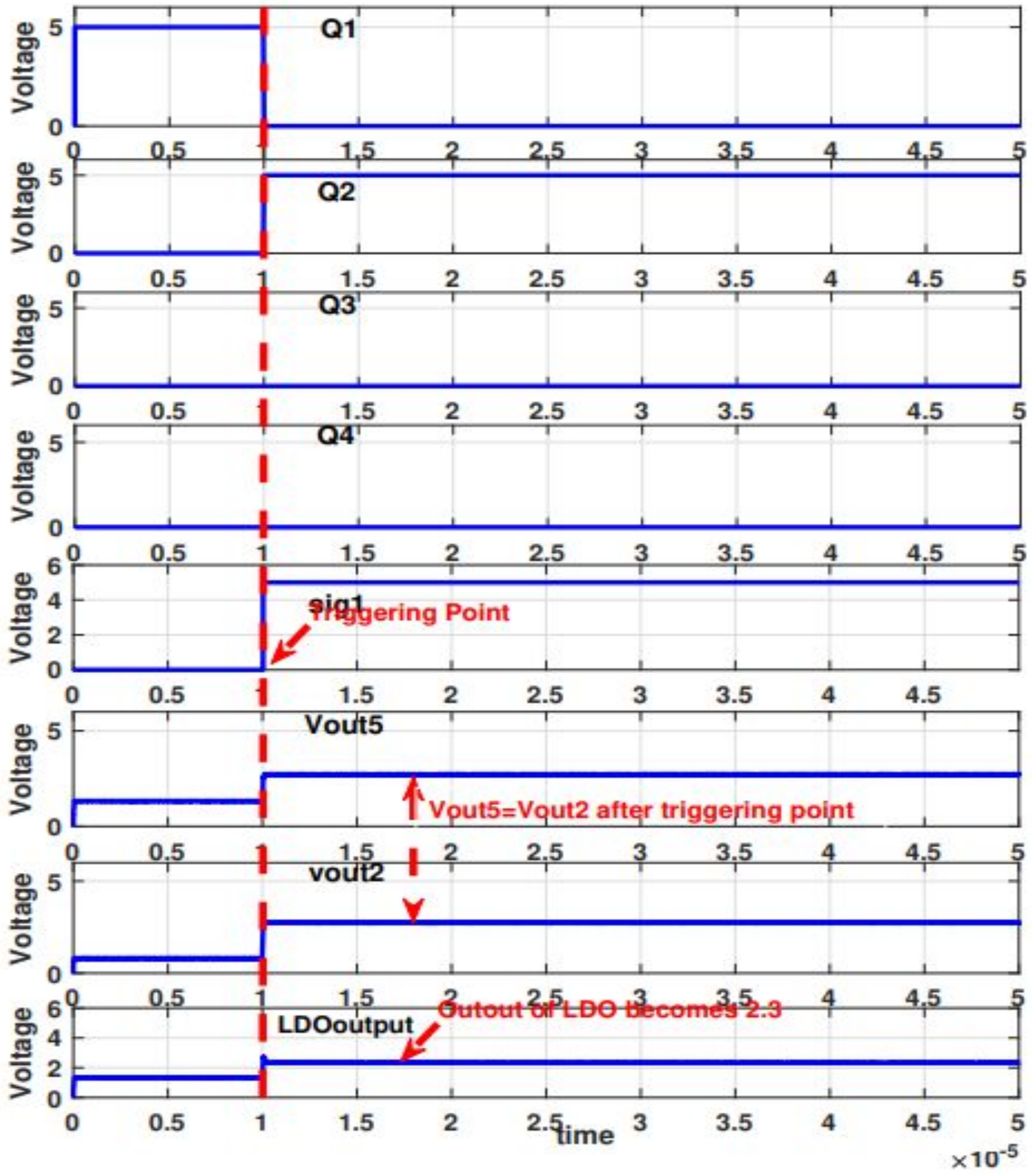
- The reconfigurable rectifier is followed up with a LDO to showcase the performance of the system.
- The LDO clearly depicts the stability of the system with a phase margin greater than 57 degree, along with a dc gain of greater then 38 dB.
- A load regulation of 2.1 mV for 100 µA change of current and a line variation of 5mV for 1V change of input line voltage is seen.





SIMULATION RESULTS:

- When Q2 is high, it deactivates the corresponding MOSFET Q2.
- Deactivation of Q2 prevents power flow to the next stage.
- It effectively shorts the output of the second rectifier stage to the final rectifier stage.
- Q1 switch facilitates power flow to the second stage.



- Since Power connection is maintained until there's a change in input power the Rectifier output voltage is maintained above 2.5 V , which subsequently directed to an LDO circuit.
- The LDO circuit ensures a stable, regulated output voltage of 2.3 V.
- This stability is maintained even with fluctuating input voltage.

CONCLUSION

- The proposed system facilitates reconfiguration to the relevant stage, ensuring maintenance of the desired voltage level while optimizing efficiency.
- Impedance-matching network values were determined through a large signal SP analysis to derive the rectifier's impedance.
- The system achieves a sensitivity of -14 dBm.
- The rectifier output voltage is stabilized at 2.5 V, with a regulated output of 2.3 V.

Thank You