Reconfigurable Rectifier for RF Energy Harvesting System at WiFi-6 Frequency Band for 2.5 V

***Abstract*—In this paper, a novel RF energy harvesting system is presented, designed to operate within the WiFi-6 frequency band. The system incorporates reconfigurable rectifier stages, offering flexibility and adaptability. Along with the rectifier stages, it includes a comparator, a ring counter, and an LDO. The system is implemented using TSMC 180 nm technology at 2.4 GHz and maintains a steady output voltage of 2.3 V. In this design, the rectifier stages are precisely adjusted to ensure that the input voltage for the LDO hovers around 2.5 V, accounting for a 200 mV dropout voltage. This adjustment significantly enhances the efficiency of the LDO. Additionally, the rectifier's conversion ratio is configured to compensate for any impedance mismatch caused by variations in the input power. The impedance of the rectifier is derived through a large signal SP analysis, allowing for the determination of appropriate impedance matching network values. As a result, the system achieves a sensitivity of -14 dBm while maintaining an output voltage of 2.3 V.**

***Index Terms*—Reconfigurable rectifier, CMOS rectifier, RF energy harvesting, Power Conversion Efficiency, LDO, LSSP.**

I. Introduction

In recent applications, Radio Frequency (RF) energy harvesting has garnered increased attention, particularly in the context of wearable [1] and implantable devices [2] used for pervasive computing in surveillance areas, enabling remote monitoring of vital health signals. A crucial component in such systems (Fig. 1) is the rectifier, which significantly impacts overall system efficiency. The available RF power exhibits rapid variations with distance (where power is inversely proportional to the square of the distance, $P_{in} \propto \frac{1}{d^2}$) and fluctuates across a wide input range. These fluctuations in input power, influenced by time and distance, introduce changes in the rectifier's impedance and disrupt its optimized operational conditions, typically set for a fixed load. Consequently, this impedance mismatch leads to a decline in rectifier performance. Therefore, it is imperative to design an optimal system capable of accommodating a wide dynamic input power range.

To address this limitation, several techniques have been introduced. In [3]- [5], parallel connection of optimized rectifiers at different incident power levels is employed to expand the input power range. These rectifiers are reconfigured using a power management unit (PMU). Nevertheless, the inclusion of an extra PMU introduces increased circuit complexity. Another approach, as described in [6] and [7], involves utilizing the maximum power point tracking method to optimize the RF-to-DC power conversion efficiency (PCE) across a wide incident power range. In [8], varactors are utilized to adjust the rectifier's impedance, compensating for changes in frequency, input power, and DC loading conditions, thereby enabling a broad input power range. Additionally, [9] explores the utilization of GaAs pHEMT to achieve high PCE across a wide input power range. However, it should be noted that these approaches introduce additional complexity to the circuit.

Resistance compression networks (RCNs) approach was proposed in [10]– [12] to reduce the sensitivity of the rectifier for input power variations. However in [10]– [12], a Dickson-based rectifier is employed whereas a differential-drive cross-coupled rectifier shows considerably enhanced performance due to small ON-resistance and reverse leakage during forward and reverse biased conditions, respectively [13]- [14].

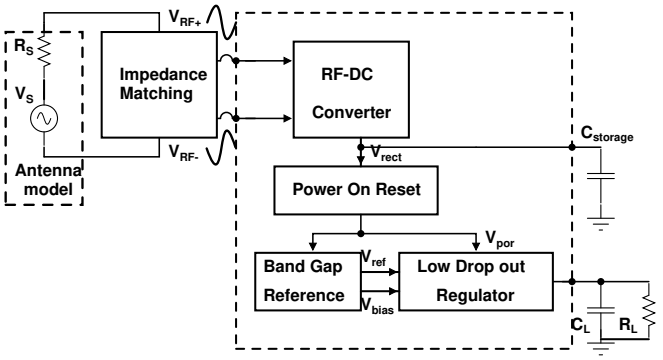

Fig. 1: Block Diagram of the RF Energy Harvesting System.

In this paper, to ensure the effective operation of the system across a wide range of input power levels, the rectifier stages are appropriately configured. This configuration aims to maintain the output voltage of the rectifier at approximately 2.5 V. By setting the output voltage at this level, the subsequent component in the system, the Low-dropout Regulator (LDO), can optimize its efficiency. The LDO accomplishes this by regulating the output voltage to a precise value of 2.3 V. This coordinated configuration between the rectifier stages and the LDO ensures that the system functions efficiently, enabling reliable and stable performance across varying input power levels.

II. Significance of Reconfigurable rectifier

The analysis of the significance of reconfigurability in rectifier stages is examined based on Fig. 1 to Fig. 4.

1) Fig. 2 demonstrates the optimal efficiency of a specific rectifier stage at a particular power level, with degradation at lower and higher power levels due to impedance mismatch. A single-stage rectifier is recommended at -14 dBm, while a two-stage rectifier performs best at -5 dBm, ensuring efficient power conversion.
2) Fig. 3 shows the relationship between input power and the number of rectifier stages needed to reach a voltage of 2.5 V. Lower input power requires more stages, while higher input power requires fewer stages.

3) Fig. 4 demonstrates the relationship between the input voltage and the efficiency of the LDO. To ensure optimal efficiency, the input voltage should be set to the regulated voltage plus the dropout voltage. Maintaining the input voltage within this range allows the LDO to operate at its highest efficiency, leading to improved performance.

To address this issue of decreasing voltage with an increase in input voltage as depicted in Fig. 4, a reconfigurable rectifier stage is proposed that automatically adjusts the number of stages to match the output voltage, and antenna impedance to maximize power transfer. Specifically, the proposed rectifier is designed to select the specific number of stages that provide the best impedance matching between the rectifier circuit and the antenna while maintaining a target output voltage level. This approach allows efficient and robust RF energy harvesting across a range of input power levels.

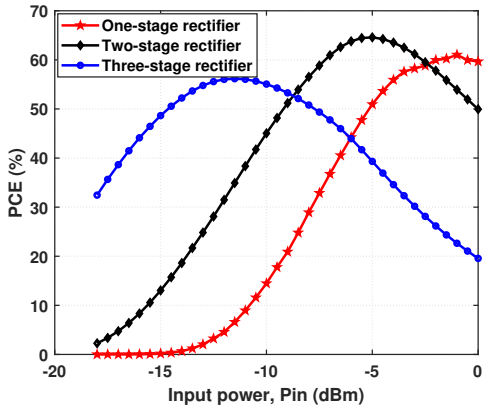

Fig. 2: PCE of rectifier stages with respect to input power.

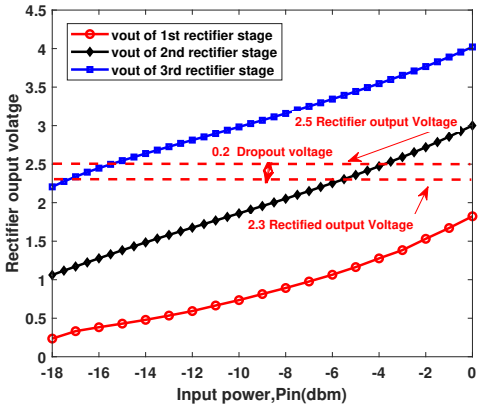

Fig. 3: Output voltages of rectifier stages with respect to input power.

III. Proposed RF Energy Harvester with Reconfigurable Rectifier

The proposed RF energy harvesting architecture is shown in Fig. 5. It incorporates a matching network for passive voltage boosting, a 5-stage rectifier for RF to DC conversion, a comparator to trigger the counter, an LDO to regulate the voltage, and a ring counter for switching. In the next section, the sub-blocks of the system are discussed.

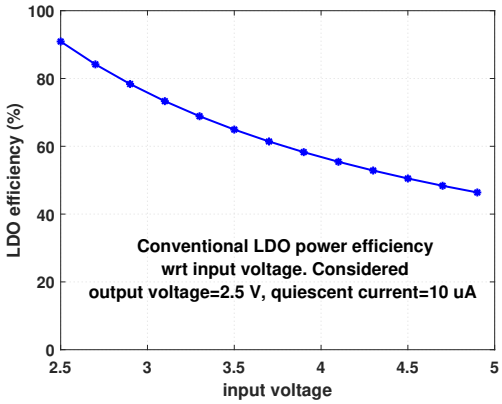

Fig. 4: Power efficiency of conventional LDO.

A. Matching Network

Impedance matching is required to ensure most of the power from the RF source is delivered to the load. The large input signal without any DC bias results in the rectifying device operating in different regions of operation namely the sub-threshold region, inversion region, and the cut-off region. Further, the impedance of the rectifier is determined using a large signal SP analysis (LSSP) HB analysis in Cadence Virtuoso.

Design methodology of Impedance Matching Network : The design incorporates a differential T-matching network, which is depicted in Fig. 6a.

From Fig. 6b, low to high matching impedance is given as,

$$Z_0 = jX_{Ls} + (R_i || - jX_{cp/2}) \tag{1}$$

where, $X_{cp_{right}} = \frac{1}{\omega C p_{right}}$, $X_{cp_{left}} = \frac{1}{\omega C p_{left}}$; $X_{C_L} = \frac{1}{\omega C_L}$; $X_{Ls} = \omega L_s$; $X_{Lp} = \omega L_p$;$Z_L = R_L + C_L$;$R_i = Z_0 + |Z_L|$.

The rectifier impedance, Z_L is derived from the reflection co-efficient, S_{11} which is given as,

$$S_{11} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2}$$

Fig. 7 shows the magnitude and phase of S_{11} at 2.4 GHz, $S_{11} = 0.651 - j0.403$ at 2.4 GHz.

Considering $Z_0 = 50$, $R_i = 235$ in equation 2, $Z_L = 137.348 - j123.948$ is obtained.

On solving equation 1,

$$-100 = 2R_i + R_i L_S \omega^2 C_{pleft} \tag{3}$$

$$25 = \frac{R_i C_{Pleft}}{L_S} \tag{4}$$

Upon solving equation 3 and equation 4, $Cp_{\text{left}} = 0.5428$, $L_s = 6.378$.

Similarly, high to low matching impedance is given as:

$$R_i = jX_{Lp} + R_L || - jX_{c_{pright}} \tag{5}$$

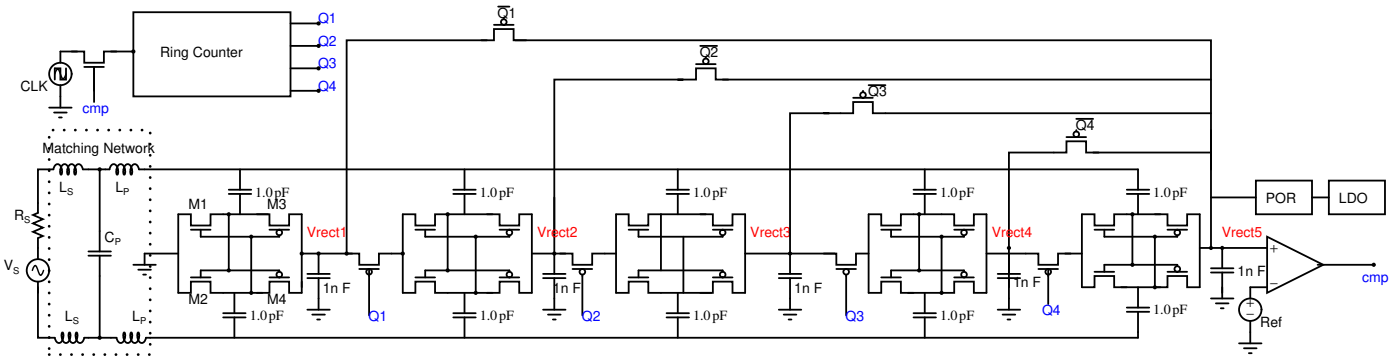

Fig. 5: Block diagram (Rectifier: M1 = M2 = 3.6 μm / 0.18 μm, M3 = M4 = 18 μm / 0.18 μm).

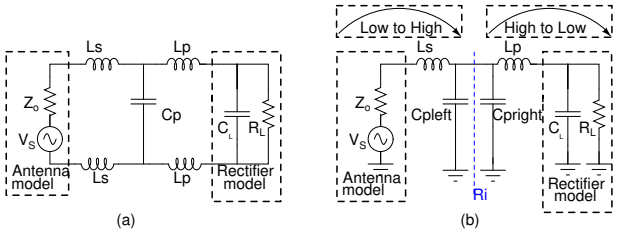

Fig. 6: (a) Differential Matching network. (b) Representation of T-Matching into L- Matching.

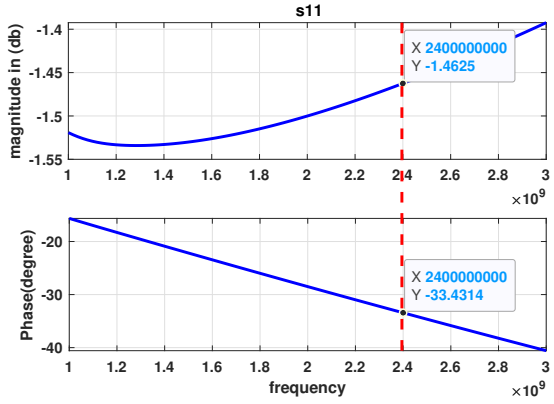

Fig. 7: Rectifier impedance without matching from LSSP simulation

From equation 6, we obtained the values $Cp_{\text{right}} = 0.2379,$ and $L_p = 15.90,.$

$$C_p = C_{pright} + c_{left} \tag{6}$$

Fig. 8 shows the value of S_{11} across the frequency range, which is equal to -18 dB at 2.4 GHz.

$$S_{11} = 10^{(-18/10)} = 0.0158$$

$$P_{\text{in}} = P_s(1 - |S11|)$$

For a source of -14 dBm proposed impedance matching network will pass P_{in} of -14.24 dBm. Further, the efficiency of the matching network is given as,

$$\text{Efficiency} = \frac{P_{in}}{P_s} \times 100 = 94.37\%$$

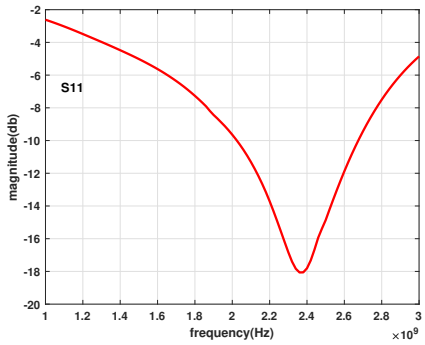

Fig. 8: S11 plot of proposed structure through LSSP simulation

B. Reconfigurable Rectifier

Working principle of reconfigurable rectifier:

The input power level plays a crucial role in the operation of the rectifier. Fig. 9 depicts the working of the 3-stage rectifier at an input power of -5 dBm. When the input power level exceeds a certain threshold, typically set at 2.5 V, the output of the third stage is fed to the overall rectifier stage output. This functionality is achieved using a ring counter, which sequentially passes a logic high signal from Q_1 to Q_4.

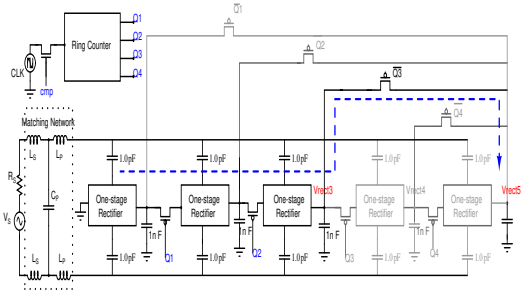

Fig. 9: Circuit behaviour of three-stage rectifier at P_s = -5 dBm.

When the Q_3 is high in the ring counter, the corresponding Q_3 MOSFET is turned off, preventing power from flowing to the next stage rectifier. Simultaneously, the $\overline{Q_3}$ MOSFET is turned on, effectively shorting the output of the third stage to the final stage. Additionally, the switches Q_1 and Q_2 are turned on, allowing power to flow up to the third stage.

Since the output of the third stage exceeds 2.5 V, it triggers the comparator, causing its output to go high. This high output from the comparator disrupts the clock signal responsible for advancing the ring counter to the next state. As a result, the connection between the third stage and the final stage is maintained until there is a change in input power. This mechanism ensures that the power from the third stage is seamlessly transferred to the final output of the rectifier when the input power reaches the specified threshold and remains connected until a new power level is detected

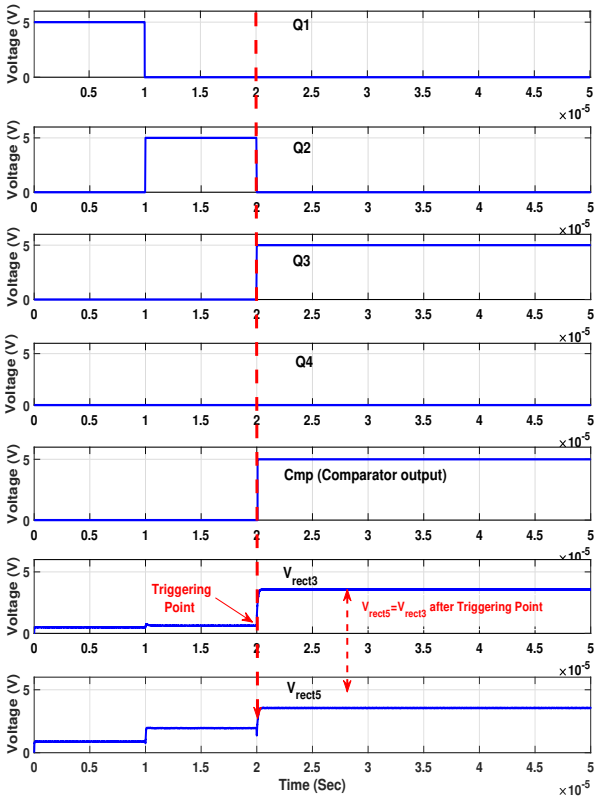

Fig. 10: Transient response of the three-stage rectifier at P_s = -5 dBm and $R_L = \infty$.

Fig. 11 illustrates the operation of the 4-stage rectifier under an input power of -10 dBm, while the corresponding output plots are presented in Fig. 12. When the input power level exceeds 2.5 V, the fourth stage of the rectifier becomes active. The output of the fourth stage is connected to the final output of the rectifier. This is achieved by turning off the Q_4 MOSFET and turning on the $\overline{Q_4}$ MOSFET, creating a short circuit between the fourth stage output and the final stage. The comparator detects the output voltage of the fourth stage, causing its output to go high and maintaining the connection until there is a change in the input power. This ensures efficient energy harvesting.

C. Low Drop-out Regulator

The schematic of the LDO is shown in Fig. 13 which incorporates an NMOS input pair and a PMOS pass transistor.

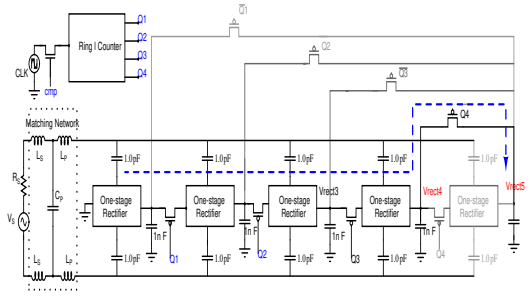

Fig. 11: Circuit behaviour of four-stage rectifier at $P_s = -10$ dBm .

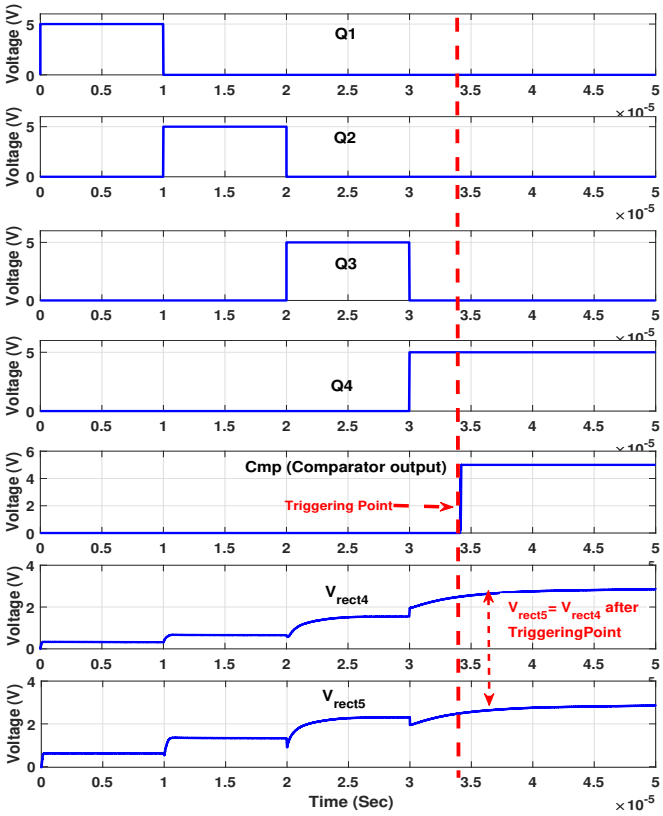

Fig. 12: Transient response of the four-stage rectifier at P_s = -10 dBm and $R_L = \infty$.

In order to achieve the desired phase margin and bandwidth, a compensating mechanism is employed, which involves the utilization of a 600 fF Miller capacitor and a 1.6 kOhm resistor. These components are specifically chosen for the purpose of compensation. Additionally, the resistors R1 and R2 are designed in such a way that they enable the output voltage to reach the target value of 2.3 V when a reference signal of 1.725 V is applied.

Fig. 14 presents a comprehensive overview of the LDO system, depicting its Gain, Phase, and Bandwidth characteristics. The LDO system demonstrates a phase margin of approximately 55 degrees, indicating its stability and ability to avoid oscillations even in the presence of disturbances or input fluctuations. Fig. 15 illustrates the load regulation behavior of the LDO system. At an output current of 100

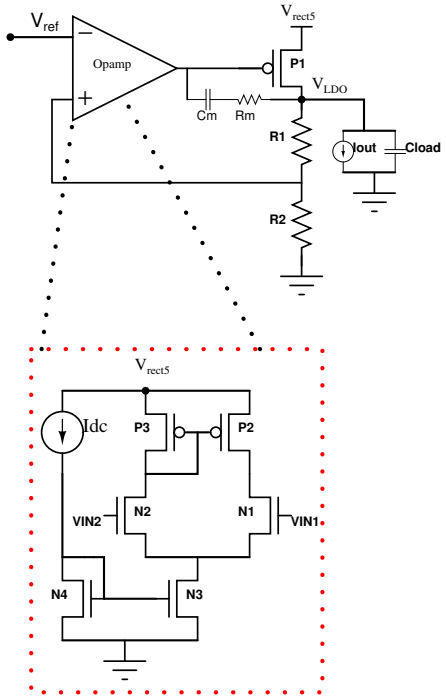

Fig. 13: Circuit diagram of LDO.

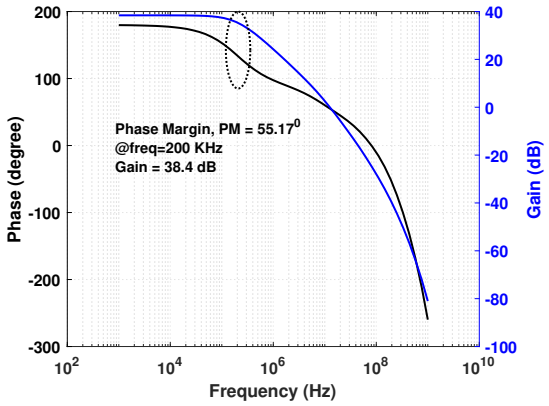

Fig. 14: Simulated plot of Gain, Phase, and Bandwidth

μA, the corresponding output voltage measures at 2.3395 V. Similarly, when the output current increases to 400 μA, the output voltage is observed to be 2.333 V. This indicates that the LDO system exhibits an output load regulation of 2.1 mV for every 100 μA change in the output current. Furthermore, Fig. 16 elucidates the response of the system to fluctuations in the input voltages. The system exhibits a load regulation of 5 mV for every 1 V change in the input voltage.

IV. Simulation Results

The proposed system, designed using TSMC 0.18 μm CMOS technology in Cadence Virtuoso IC6.1.6, has undergone thorough schematic-level simulations. Figure 17 presents the transient simulation of the complete system depicted in Fig.5. When Q_2 is high, it turns off the corresponding MOSFET Q_2, preventing power flow to the next stage and thus shorting the output of the second rectifier stage to the final rectifier stage. Q_1 switch allows power flow to the second

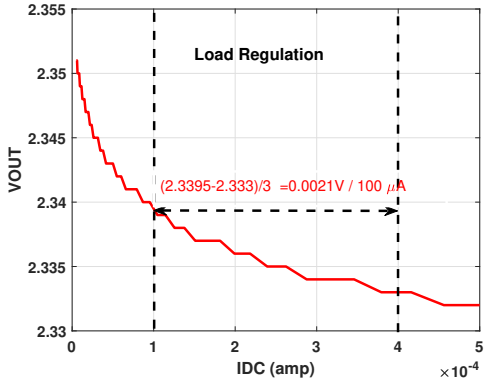

Fig. 15: Load regulation LDO

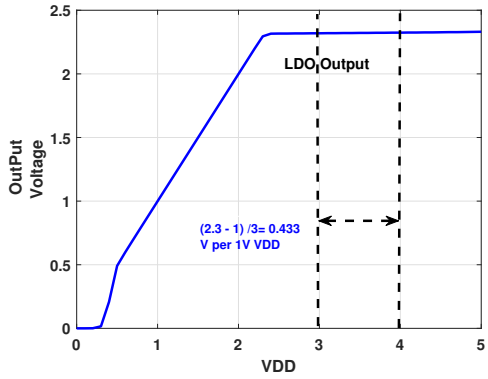

Fig. 16: Line Regulation of LDO

stage, maintaining the connection until there is a change in input power. The rectifier output voltage above 2.5 V is fed to an LDO circuit, providing a stable regulated output voltage of 2.3 V, even with fluctuating input voltage. The performance summary and comparison with previous works are shown in Table I.

V. Conclusion

Proposed system ensures reconfiguration of the system to the corresponding stage, thereby maintaining the desired voltage level while optimizing efficiency. Furthermore, the impedance-matching network values were determined by conducting a large signal SP analysis to derive the rectifier's impedance. Overall the system achieves a sensitivity of -14 dBm with a rectifier output voltage of 2.5 V and regulated output of 2.3 V.

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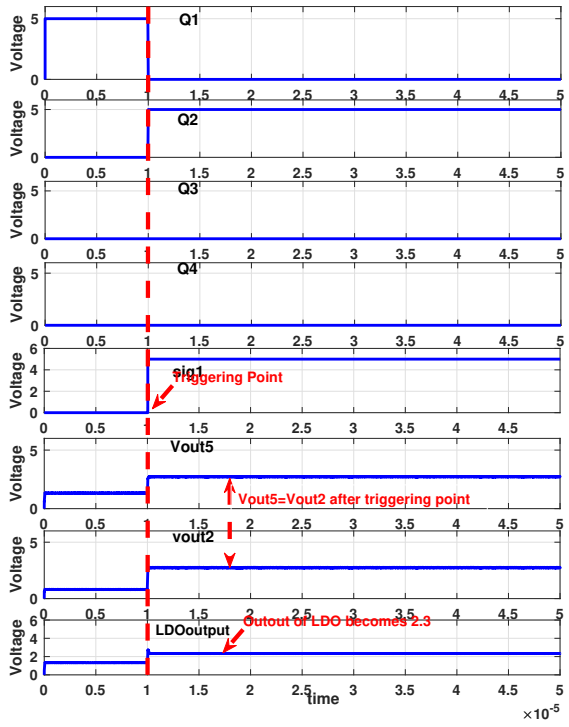

Fig. 17: Transient simulation plot of the complete system (rectifier + LDO).

TABLE I: Performance Comparison table

Ref.	Technology	Frequency	Sensitivity @ Output voltage
[15] TCASI'22	130 nm	500 MHz	-16 dBm @ 2.19 V
[16] TCASI'20	65 nm	2.45 GHz	-12 dBm @ 1 V
[17] TCASI'20	180 nm	868 MHz	-15.8 dBm @ 0.4 V
Proposed Work	180 nm	2.4 GHz	-14 dBm @ 2.5 V

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