॥ सा विद्या या विमुक्तये ॥

भारतीय प्रौद्योगिकी संस्थान धारवाड़

Indian Institute of Technology Dharwad

# CALIBRATING CIRCUITS FOR RF ENERGY HARVESTING

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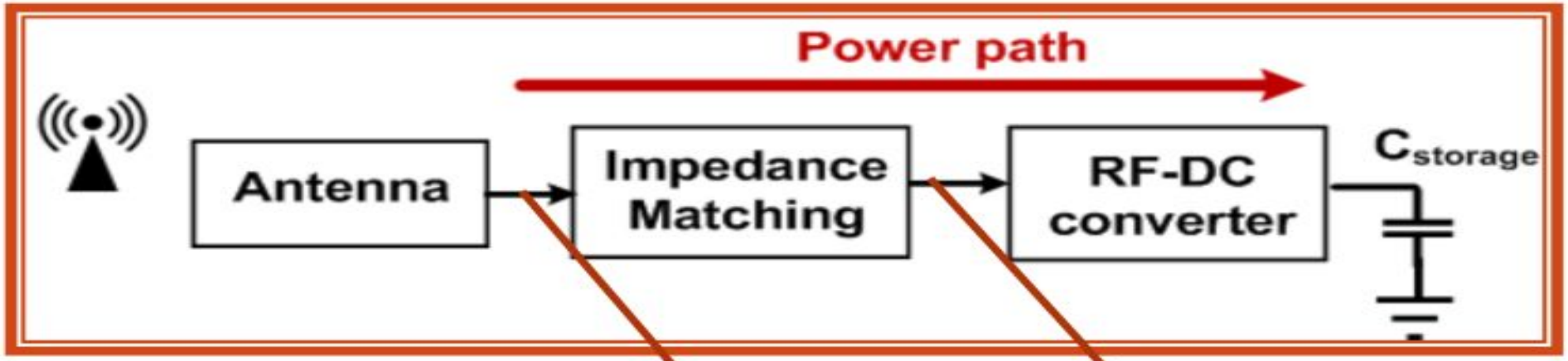
# ABSTRACT

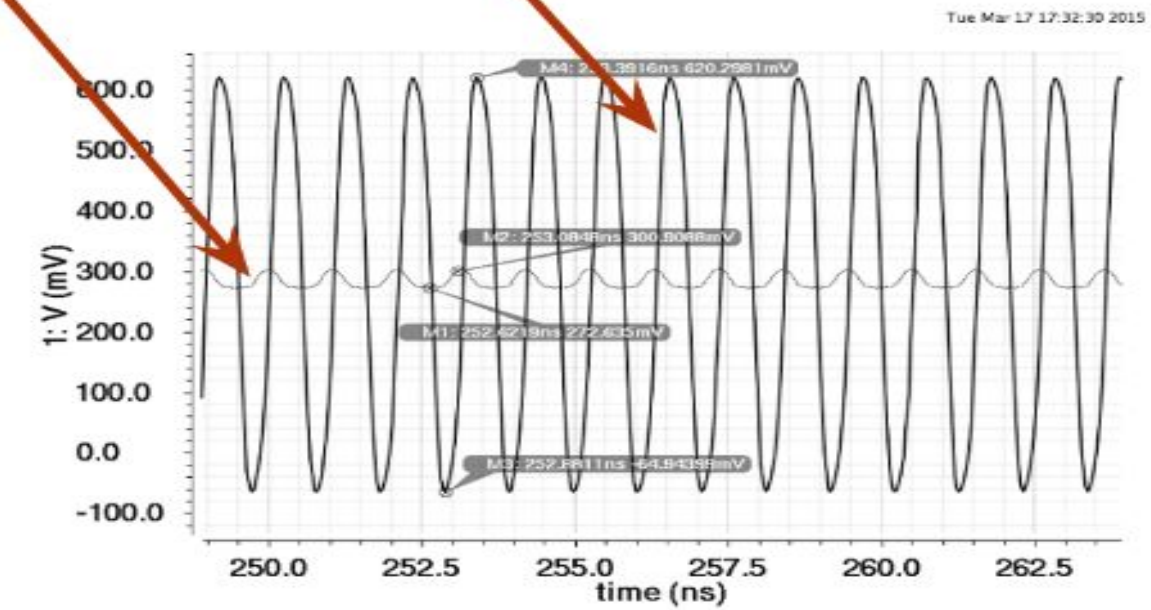

- To Demonstrates a Impedance matching network and reconfigurable rectifier stages in RF energy harvesting system, to be used with a passive wearable device operating at a distance of 6-20 m from a wireless power source.
- This RF energy harvesting circuit can harvest an input power as low as -14 dBm from both 925 MHz and 2.4 GHz, ISM frequencies.
- Circuit is implemented in a standard 0.18 µm CMOS technology.

# Motivation

- The received RF input power varies with time and distance.
- These variations in the input power causes the change in the impedance of the rectifier.
- Hence an impedance calibration circuit is required to tune the matching network values .
- Low powered signal needed to be multiplied through multiple stages of rectification.so an reconfiguration circuit for number of stages is required.




- Antenna – To receive RF power
- Impedance matching network- For maximum power transfer and passive voltage boosting
- RF-DC converter (Rectifier) – To convert AC signa; to DC



# ANTENNA

- If $P_{avail}$ is the power available at the input terminals of a receiving antenna and Ra is the radiation resistance of the antenna then the open circuited voltage (Va) developed across the antenna terminals can be found from the following equation.

$$P_{avail} = \frac{V_a^2}{8R_a}$$

# Impedance Matching Calibration network

# IMPEDANCE MATCHING NETWORK

- An impedance matching network (MN) between the antenna and rest of the circuitry in any RF system helps in transferring the maximum available power from the output of the antenna to the rest of the circuitry.
- Components used in IMN

➢ Thermal counter
➢ capacitors
➢ Inductors(LC Circuit)

```
module first_counter (clock , reset , enable ,counter_out );
input clock ;
input reset ;
input enable ;
output [3:0] counter_out ;
wire clock ;
wire reset ;
wire enable ;
reg [3:0] counter_out ;
reg [3:0]  a;
always @ (posedge clock)
begin : COUNTER
  if (reset == 1'b1) begin
    counter_out <=  4'b0001;
  end
  else if (enable == 1'b1) begin
    counter_out <=  counter_out | (counter_out<<1) ;

  end
end
endmodule
module first_counter_tb();
reg clock, reset, enable;
wire [3:0] counter_out;
initial begin
  $display ("time\t clk reset enable counter");
  $monitor ("%g\t %b   %b     %b      %b",$time, clock, reset, enable, counter_out);
  clock = 1;        // initial value of clock
  reset = 0;        // initial value of reset
  enable = 0;       // initial value of enable
  #1 reset = 1;     // Assert the reset
  #2 reset = 0;    // De-assert the reset
  #1 enable = 1;   // Assert enable
  #5 enable = 0; // De-assert enable
  $finish;      // Terminate simulation
end

// Clock generator
always begin
  #1 clock = ~clock; // Toggle clock every 5 ticks
end
first_counter mouli (clock,reset,enable,counter_out);
endmodule
```

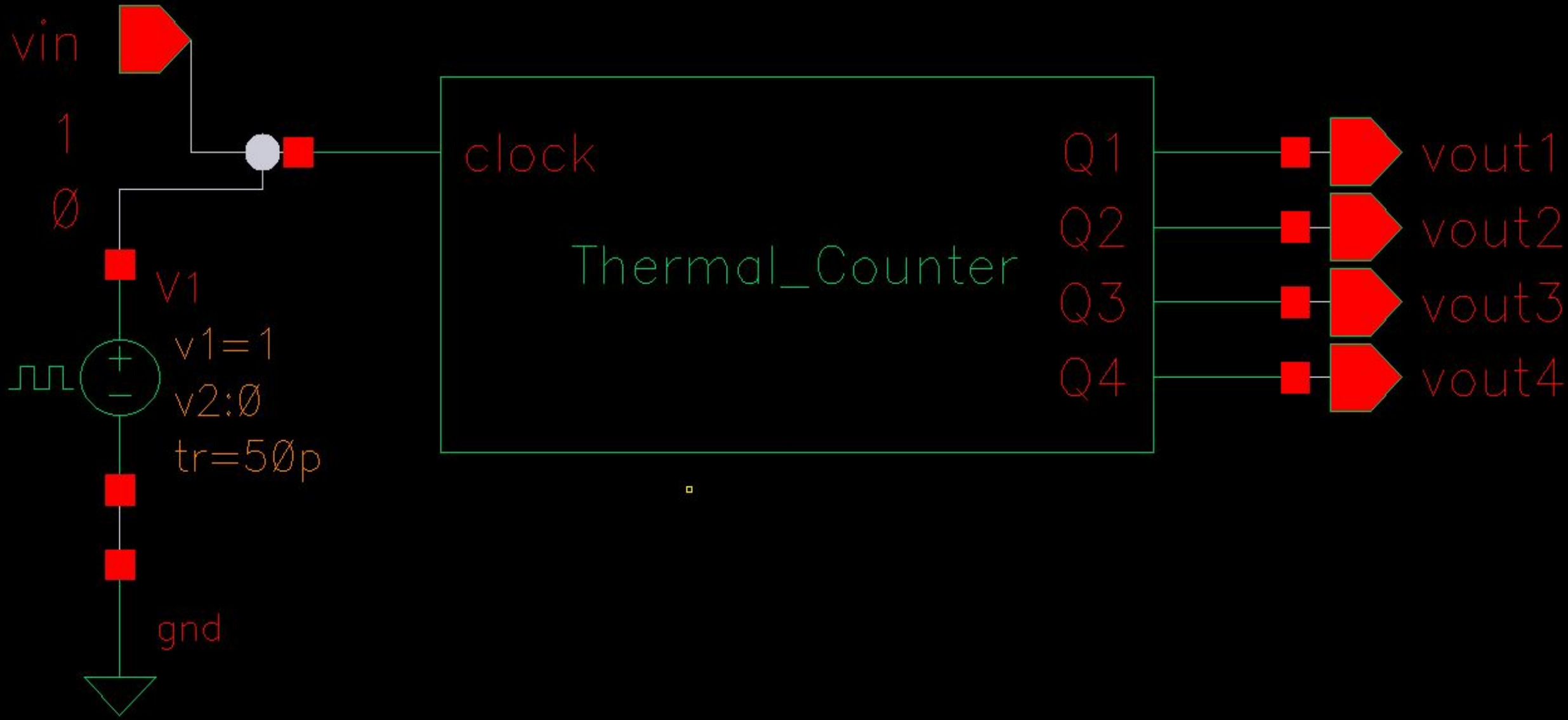
## VERILOG CODE OF THERMAL COUNTER

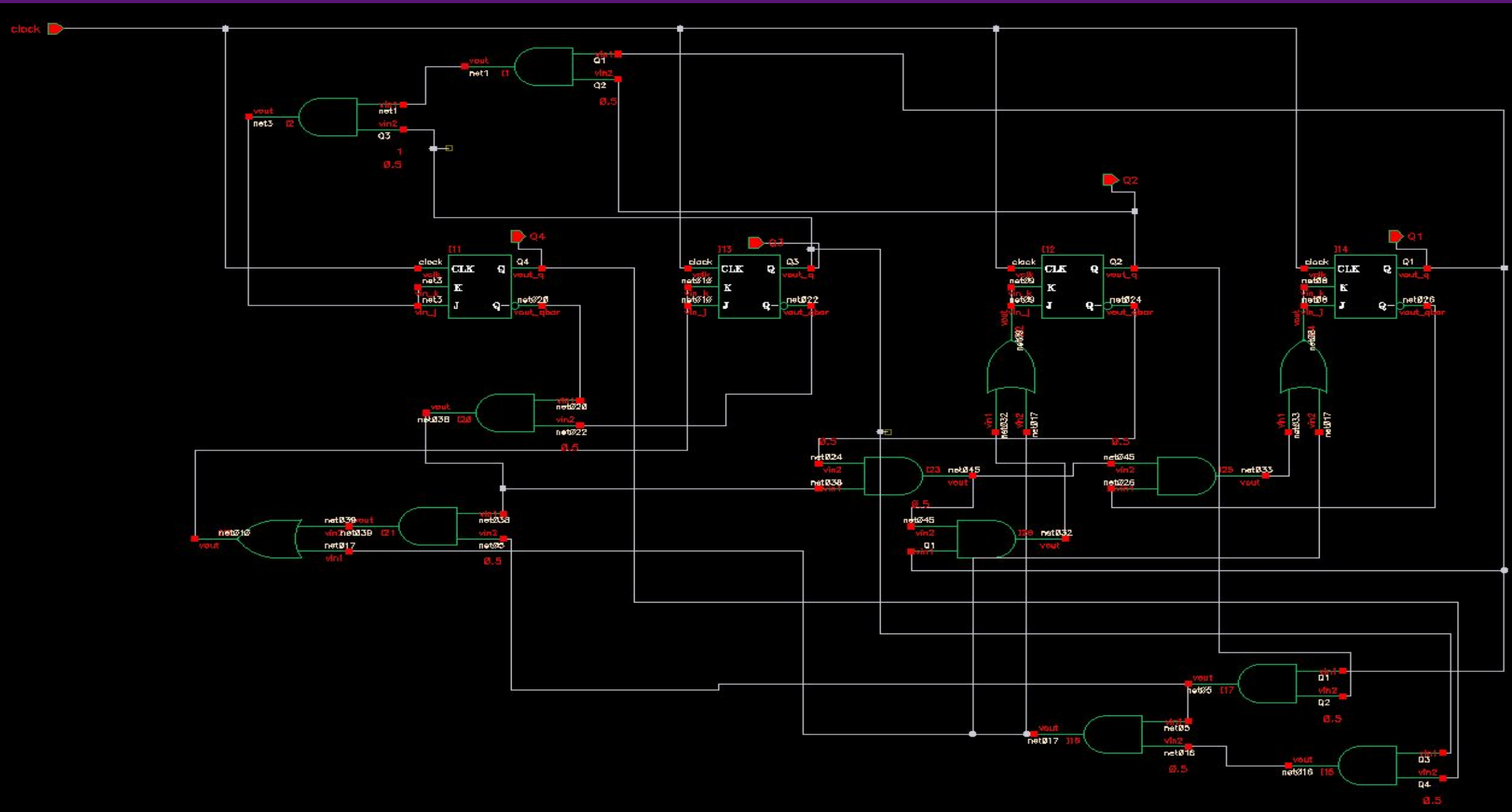
```
module first_counter (clock , reset , enable ,counter_out );
input clock ;
input reset ;
input enable ;
output [3:0] counter_out ;
wire clock ;
wire reset ;
wire enable ;
reg [3:0] counter_out ;
reg [3:0]  a;
always @ (posedge clock)
begin : COUNTER
  if (reset == 1'b1) begin
    counter_out <=  4'b0000;
  end
  else if (enable == 1'b1) begin
    counter_out <=  counter_out +1 ;

  end
end
endmodule
module first_counter_tb();
reg clock, reset, enable;
wire [3:0] counter_out;
initial begin
  $display ("time\t clk reset enable counter");
  $monitor ("%g\t %b   %b     %b      %b",$time, clock, reset, enable, counter_out);
  clock = 1;        // initial value of clock
  reset = 0;        // initial value of reset
  enable = 0;       // initial value of enable
  #1 reset = 1;     // Assert the reset
  #2 reset = 0;    // De-assert the reset
  #1 enable = 1;   // Assert enable
  #29 enable = 0; // De-assert enable
  $finish;      // Terminate simulation
end

// Clock generator
always begin
  #1 clock = ~clock; // Toggle clock every 5 ticks
end
first_counter mouli (clock,reset,enable,counter_out);
endmodule
```

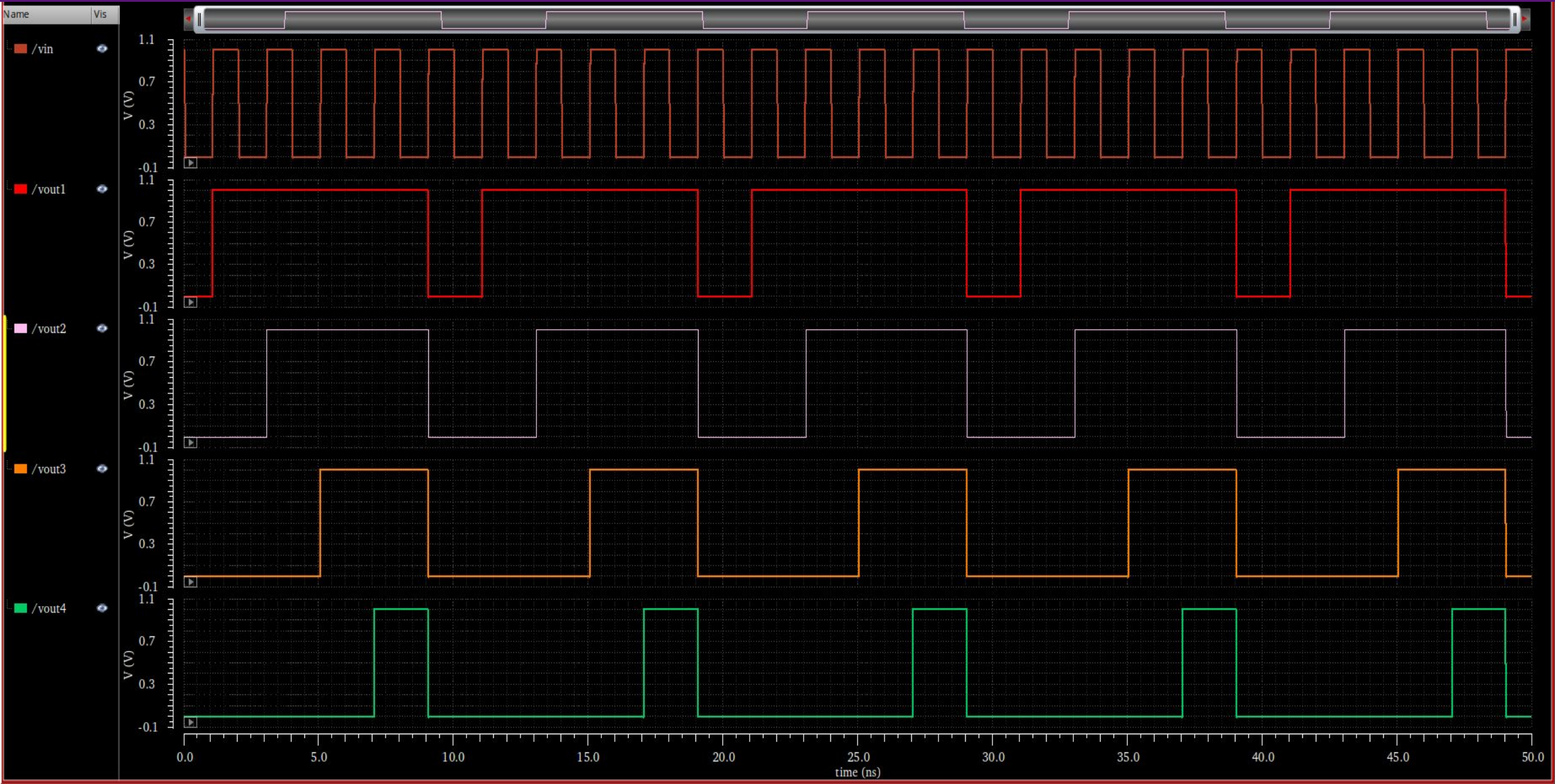
## VERILOG CODE OF BINARY COUNTER

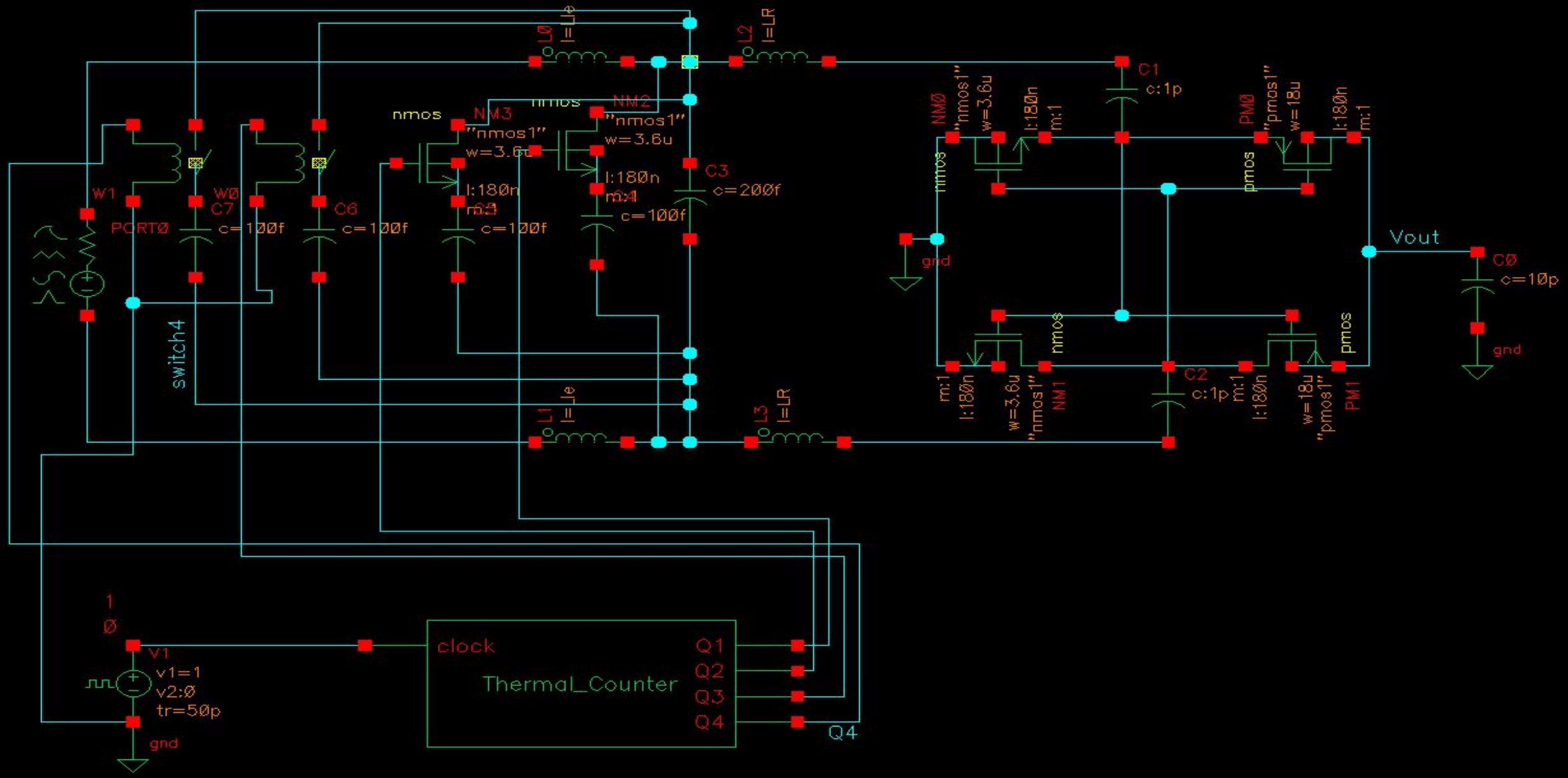
```
mouli@mouli-Victus-by-HP-Laptop-16-e0xxx:~/Desktop/m_v$ iverilog thermalcounter.v
mouli@mouli-Victus-by-HP-Laptop-16-e0xxx:~/Desktop/m_v$ vvp a.out
time     clk reset enable counter
0        1   0     0      xxxx
1        0   1     0      xxxx
2        1   1     0      0001
3        0   0     0      0001
4        1   0     1      0011
5        0   0     1      0011
6        1   0     1      0111
7        0   0     1      0111
8        1   0     1      1111
9        0   0     0      1111
mouli@mouli-Victus-by-HP-Laptop-16-e0xxx:~/Desktop/m_v$ iverilog binarycounter.v
mouli@mouli-Victus-by-HP-Laptop-16-e0xxx:~/Desktop/m_v$ vvp a.out
time     clk reset enable counter
0        1   0     0      xxxx
1        0   1     0      xxxx
2        1   1     0      0000
3        0   0     0      0000
4        1   0     1      0001
5        0   0     1      0001
6        1   0     1      0010
7        0   0     1      0010
8        1   0     1      0011
9        0   0     1      0011
10       1   0     1      0100
11       0   0     1      0100
12       1   0     1      0101
13       0   0     1      0101
14       1   0     1      0110
15       0   0     1      0110
16       1   0     1      0111
17       0   0     1      0111
18       1   0     1      1000
19       0   0     1      1000
20       1   0     1      1001
21       0   0     1      1001
22       1   0     1      1010
23       0   0     1      1010
24       1   0     1      1011
25       0   0     1      1011
26       1   0     1      1100
27       0   0     1      1100
28       1   0     1      1101
29       0   0     1      1101
30       1   0     1      1110
31       0   0     1      1110
32       1   0     1      1111
33       0   0     0      1111
mouli@mouli-Victus-by-HP-Laptop-16-e0xxx:~/Desktop/m_v$
```

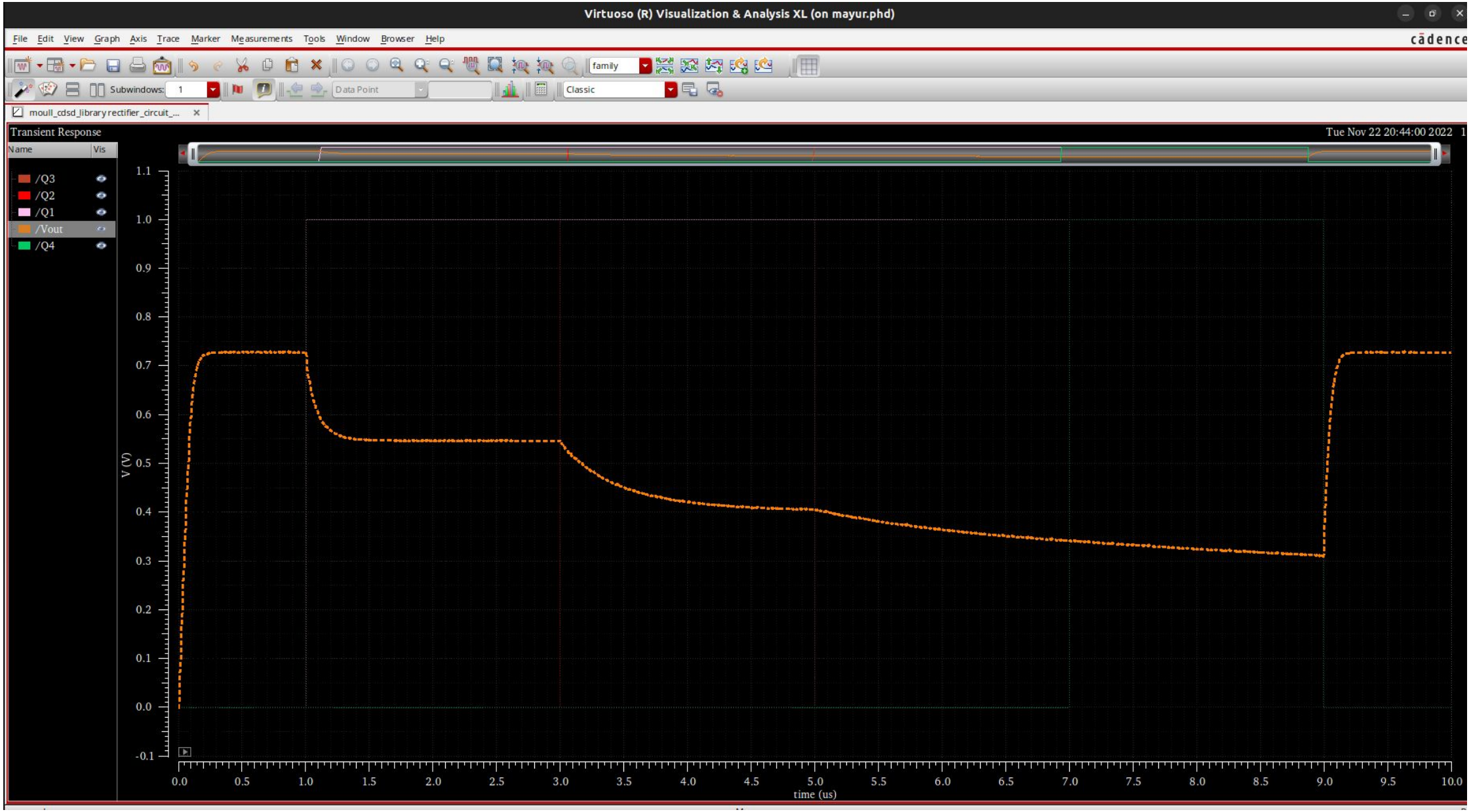
## Output of Thermal and binary counter


vin
1
0
clock
Thermal_Counter
Q1
Q2
Q3
Q4
vout1
vout2
vout3
vout4
V1
v1=1
v2:0
tr=50p
gnd


clock
Q1
Q2
Q3
Q4
CLK
K
J
Q
vout
vin1
vin2
0.5


Name
Vis
/vin
/vout1
/vout2
/vout3
/vout4
1.1
0.7
0.3
-0.1
V (V)
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
45.0
50.0
time (ns)

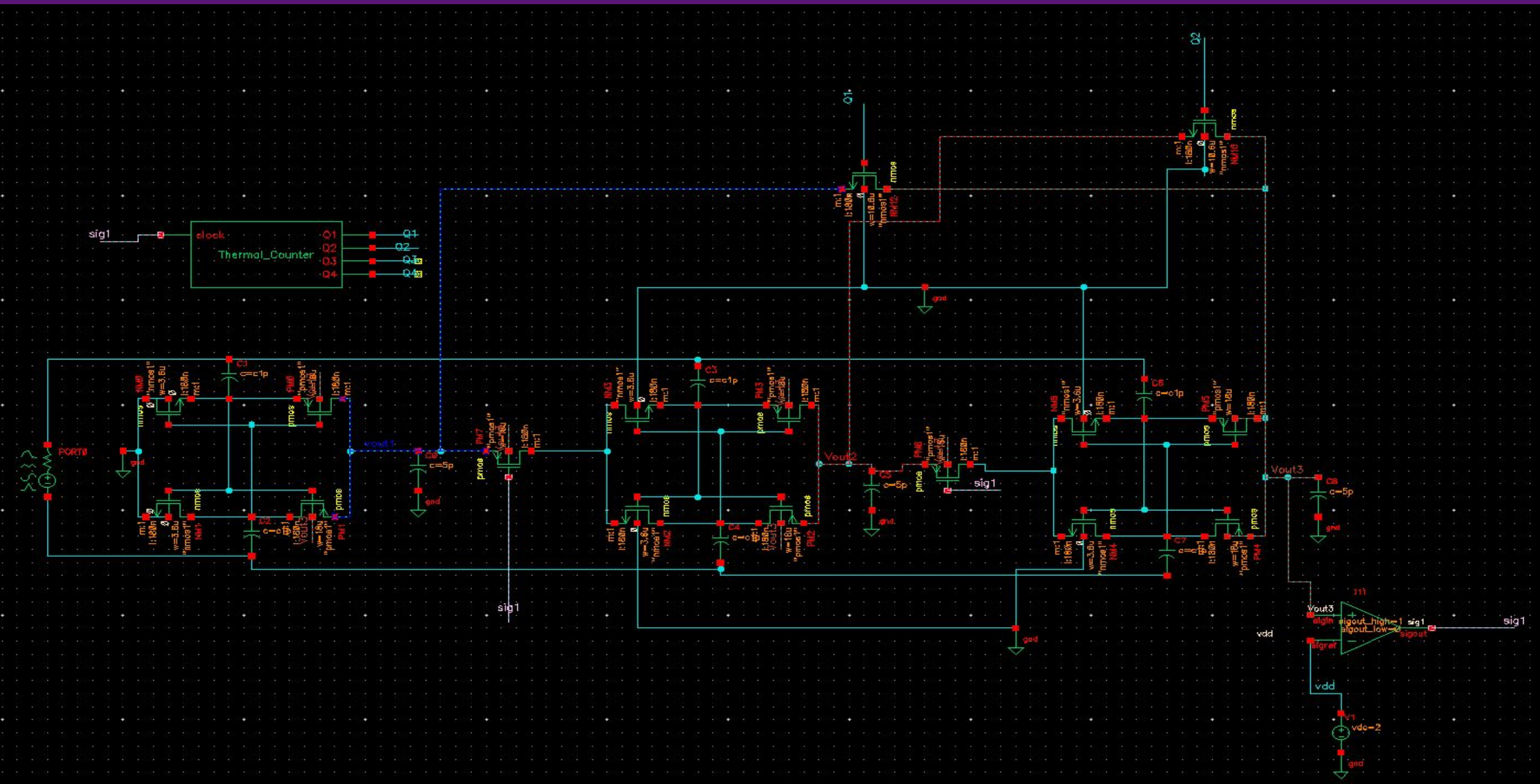

L0
l=Le
L2
l=LR
NM2
"nmos1"
w=3.6u
l:180n
m:4
C3
c=200f
c=100f
NM3
"nmos1"
w=3.6u
l:180n
m:4
c=100f
C6
c=100f
C7
c=100f
W1
PORT0
W0
switch4
L1
l=Le
L3
l=LR
NM0
"nmos1"
w=3.6u
l:180n
m:1
C1
c:1p
PM0
"pmos1"
w=18u
l:180n
m:1
Vout
C0
c=10p
gnd
C2
c:1p
NM1
PM1
1
0
V1
v1=1
v2:0
tr=50p
clock
Thermal_Counter
Q1
Q2
Q3
Q4

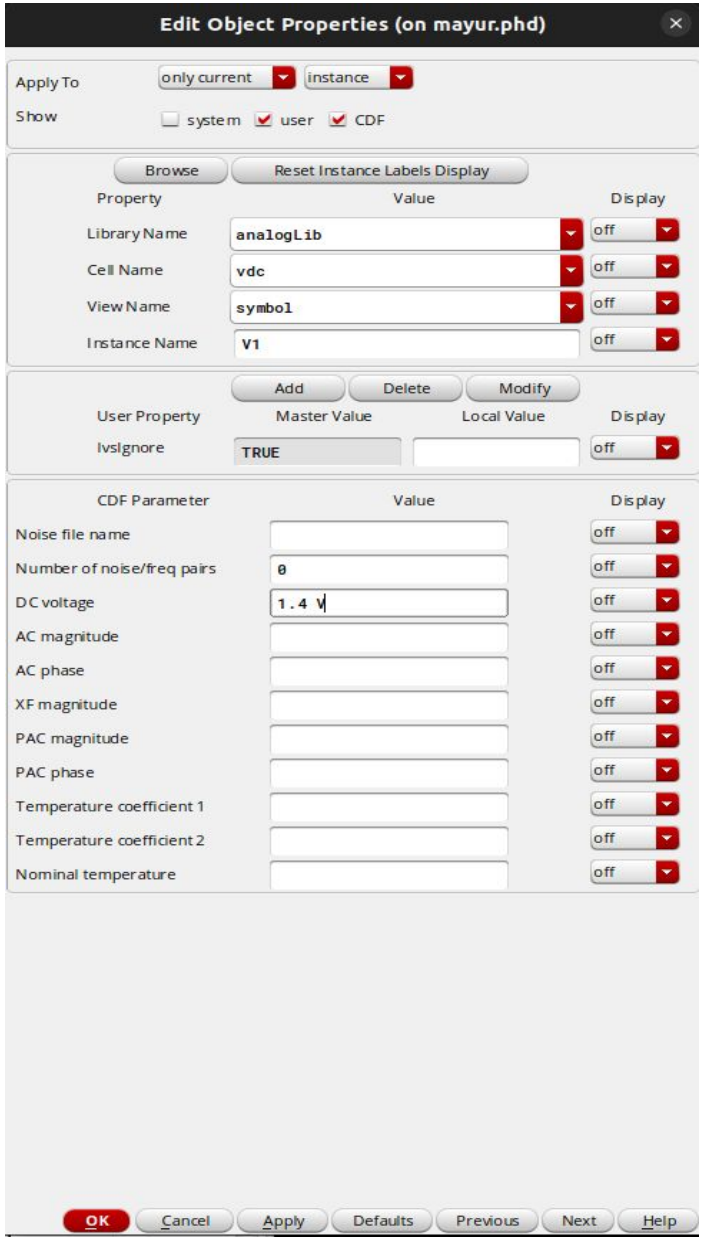

Virtuoso (R) Visualization & Analysis XL (on mayur.phd)
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindows: 1
Data Point
Classic
moull_cdsd_library rectifier_circuit_...
Transient Response
Tue Nov 22 20:44:00 2022
Name
Vis
/Q3
/Q2
/Q1
/Vout
/Q4
V (V)
time (us)

# RECONFIGURABLE CIRCUIT FOR RECTIFIER STAGES

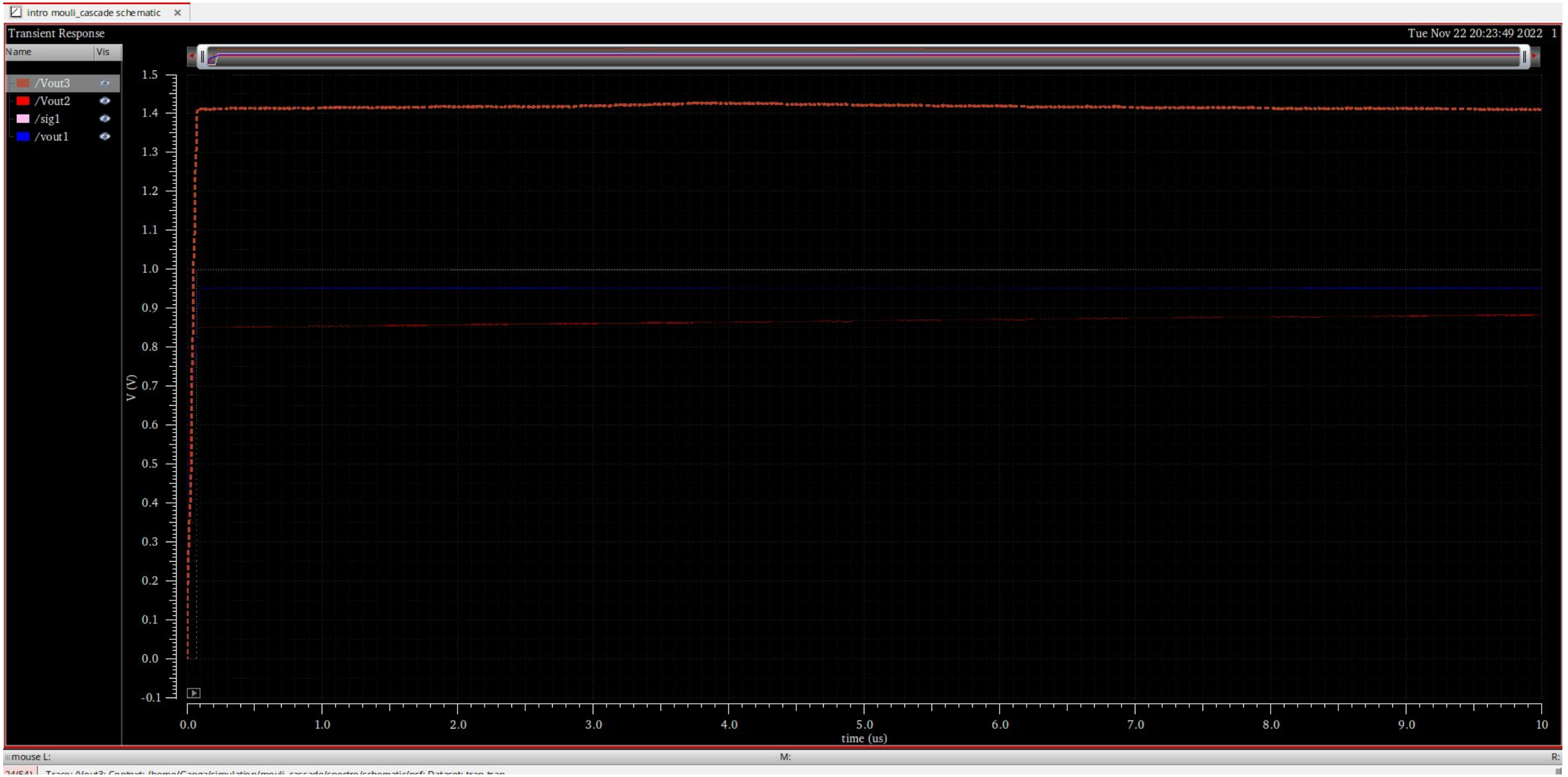
# MOTIVATION

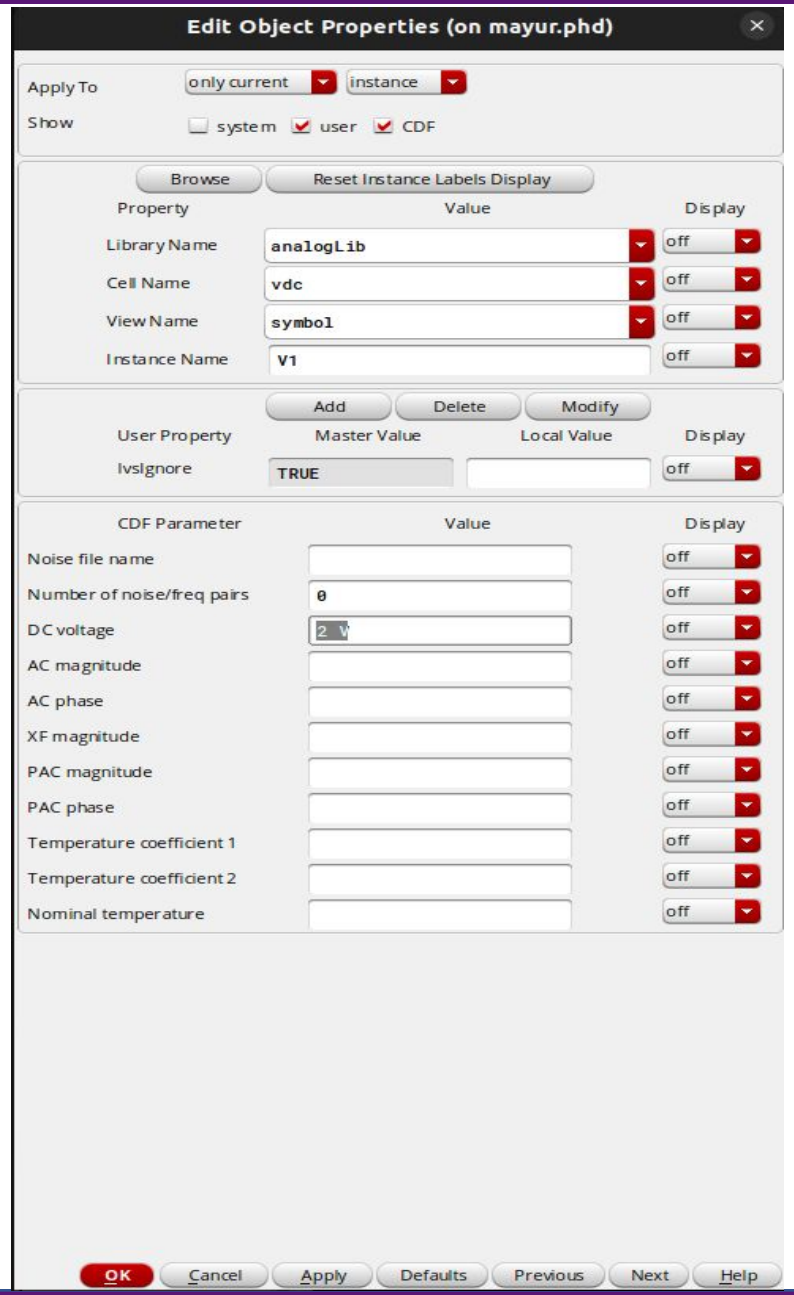
- As input power varies from 0db to -30db ,we need multiple stages of rectifiers.
- A circuit for maintaining required number of stages for input power required and that can be achieved from this Reconfigurable Rectifier stage circuit.
- The Desired output from rectifier circuit can be controlled by the comparing voltage at Comparator.
- Circuits like LDO and buck convertor  will have a loss in efficiency if their input is differ in large amount then desired output.


sig1
clock
Thermal_Counter
Q1
Q2
Q3
Q4
Vout1
Vout2
Vout3
vdd
gnd
sig1

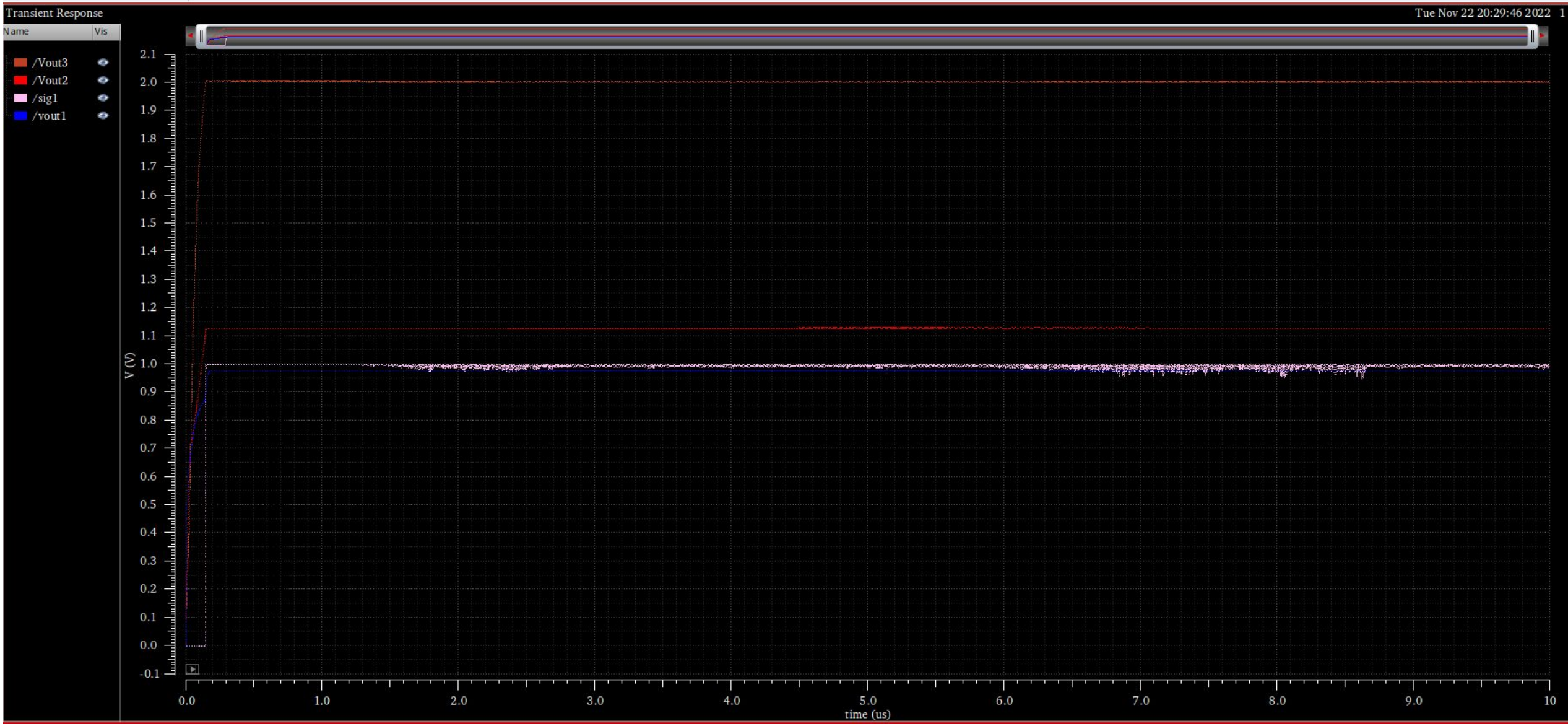



# A DESIRED 1.4 V FOR LDO CIRCUIT COMPARATOR WAS GIVEN 1.4 V


intro mouli_cascade schematic
Transient Response
Tue Nov 22 20:23:49 2022
Name
Vis
/Vout3
/Vout2
/sig1
/vout1
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
V (V)
0.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10
time (us)
mouse L:
M:
R:




# 2V OUTPUT SPECIFICATIONS


Transient Response
Tue Nov 22 20:29:46 2022 1
Name
Vis
/Vout3
/Vout2
/sig1
/vout1
V (V)
2.1
2.0
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-0.1
0.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10
time (us)

# LEARNINGS:

- IM NETWORKS
- Circuit Designing for D flip flops and basic gates with 180nm cmos technology.
- Circuit Designing for binary and thermal counters
- Reconfiguration circuits.
- Basic coding in verilog language.
- Introduced to cadence Tool
- Enjoyed the working experience for a real time Problem.

# Future plans:

- Increasing efficiency of reconfiguring rectifier stage circuit.
- 4 to 16 decoder for LDO circuit.
- Improvement of Impedance matching Network.
- Exploring Deep in RF circuit elements and improving efficiency for constraints.
- To check the overall Performance by connecting LDO to reconfigurable circuit and increase the efficiency

# REFERENCES:


- Efficient Dual Band RF Energy Harvesting Front End for Ultra Low Power Sensitive Passive Wearable Devices ,978-1-4799-6965-4/14 $31.00 © 2014 IEEE DOI 10.1109/ISED.2014.25(paper).
- https://ieeexplore.ieee.org/document/8067367
- https://ieeexplore.ieee.org/abstract/document/794456

# THANK YOU