Microprocessadores ARM

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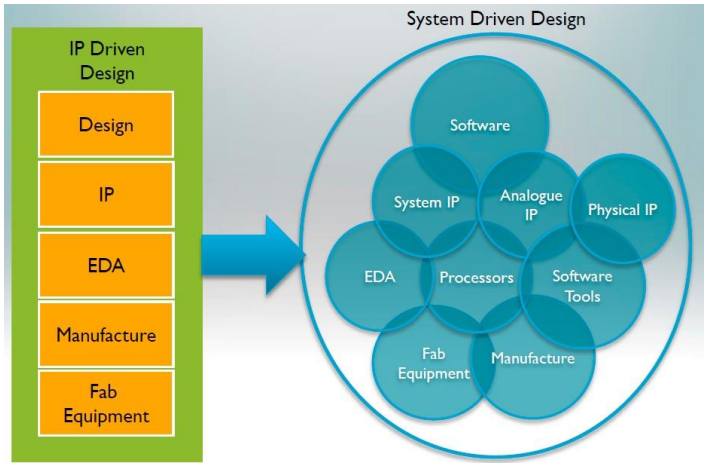
Arquitetura ARM

- Lider com microprocessadores RISC 32 bits embarcados (mais de 75%)
  - Boa relação MIPS/Watt
- Soluções para
  - Armazenamento de dados
  - Automotivo
  - Rede
  - Segurança

Arquitetura ARM

- Somente No final da década de 90 a começou a fazer sucesso se desdobrando na ARM Holdings
- Licenças de núcleo ARM é fornecida para diferentes fábricas de semicondutores.
    - Difusores ARM em si não fabricam chips
    - Licenças:
    - Softwares (bibliotecas, ferramentas e até mesmo netlists)
    - Hardwares (IPs, propostas de DSM – *Device-Specific Module ...*)



Arquitetura ARM

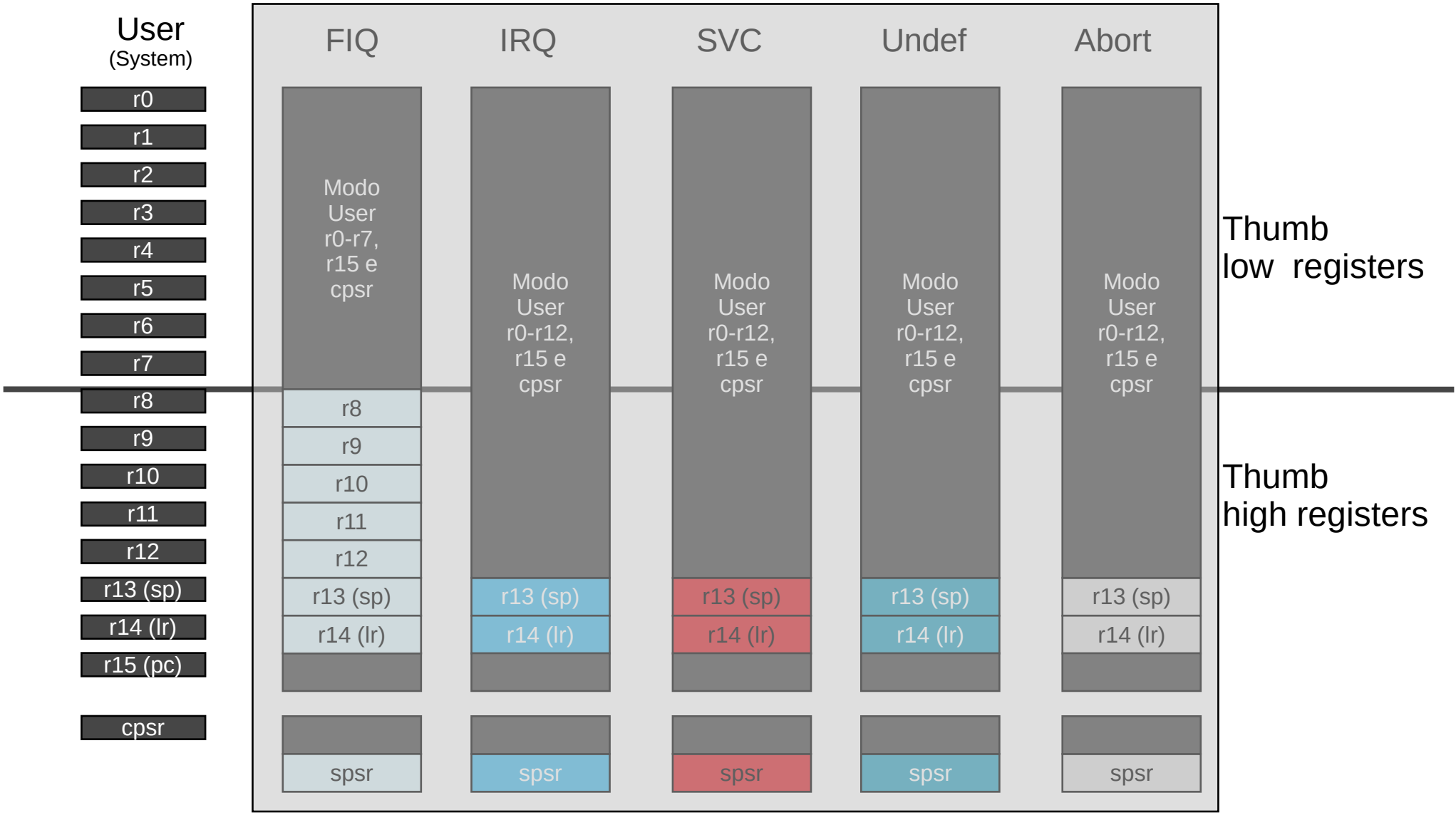
- Arquitetura ARM é nativamente de 32 bits

- Tipos de dados suportados pela plataforma ARM:
  - Byte dados de 8 bits
  - Halfword dados de 16 bits
  - Word dados de 32 bits

- A maior parte dos processadores ARM's possui dois conjuntos de instruções:
  - ARM Instruction Set: instruções de 32 bits
  - Thumb Instruction Set: instruções de 16 bits

- Alguns núcleos especiais como o Jazelle podem executar bytescodes Java: instruções de 8 bits

Organização de registradores



Versões ARM

Primeiras arquiteturas

ARM

Halfword e signed halfword

Modo System

SA-110

SA-1110

Thumb

ARM7TDMI | **ARM9TDMI**

ARM720T | **ARM940T**

Novos ARM/Thumb CLZ

Operação de saturação

Instruções de multiplica-acumula (DSP)

ARM1020E

XScale

ARM9E-S

ARM966E-S

Jazelle

(bytecode Java)

ARM9EJ-S | **ARM926EJ-S**

ARM7EJ-S | **ARM1026EJ-S**

Instruções SIMD

Multi-processamento

Suporte a dados desalinhados

ARM1136EJ-S

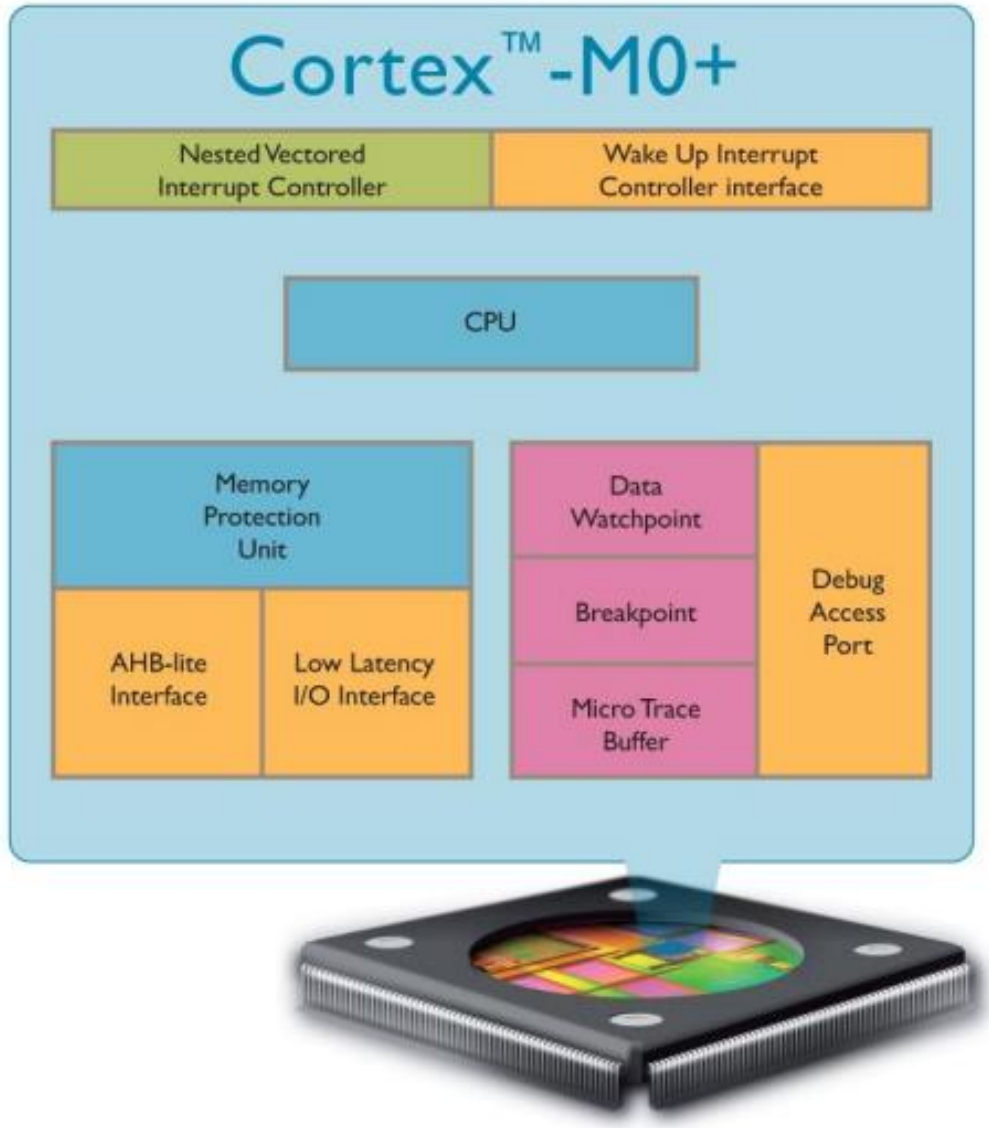
Nova família ARM

- ARM Cortex
  - Alia visão de processamento geral com recursos de processamento de sinais
  - Thumb®-2 suporta instruções de 16/32-bit para melhorar desempenho ou consumo de potência
  - Melhora manipulação de interrupções

  - 2009 – ARM® Cortex M0
  - 2012 – Cortex-M0+

Nova família ARM

- ARM Cortex M0+
  - Arquitetura ARMv6-M
  - Voltado para uso de C
  - Nested Vectored Interrupt Controller (NVIC) + Wake up Interrupt Controller (WIC)
  - Unidade de proteção de memória (MPU)
  - Debug simplificado



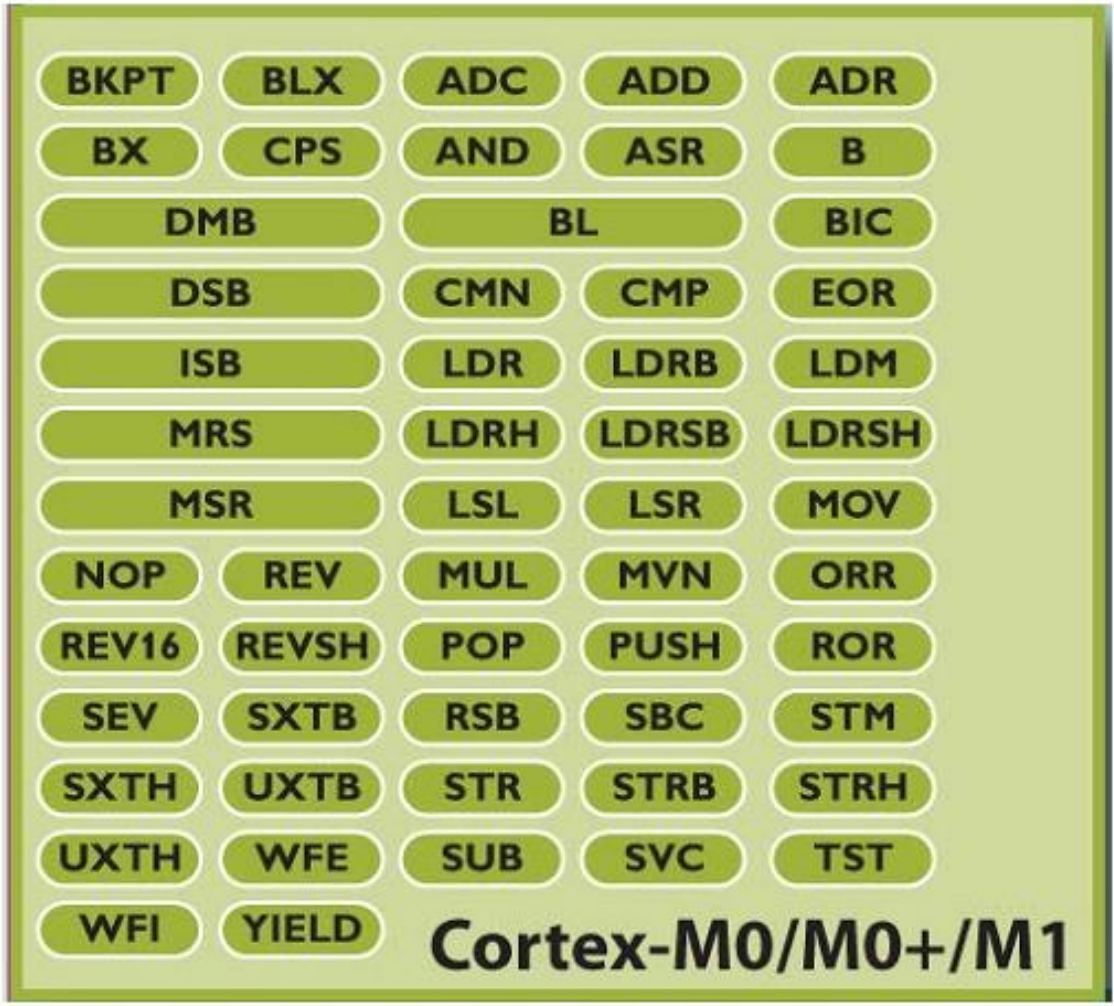
Cortex M0+

- Cerca de 56 instruções
- Maior parte de 16 bits

MOV<c> <Rd>,<Rm>

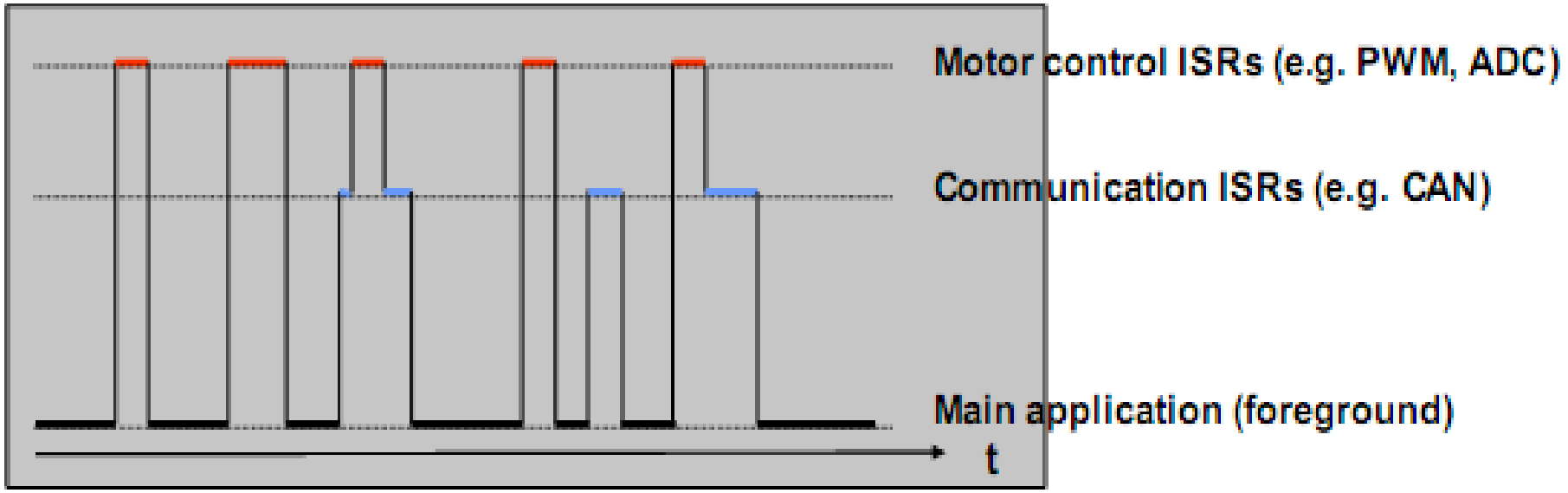
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	0	D	Rm				Rd		

- Registradores de 32 bits
- Multiplicador 32x32



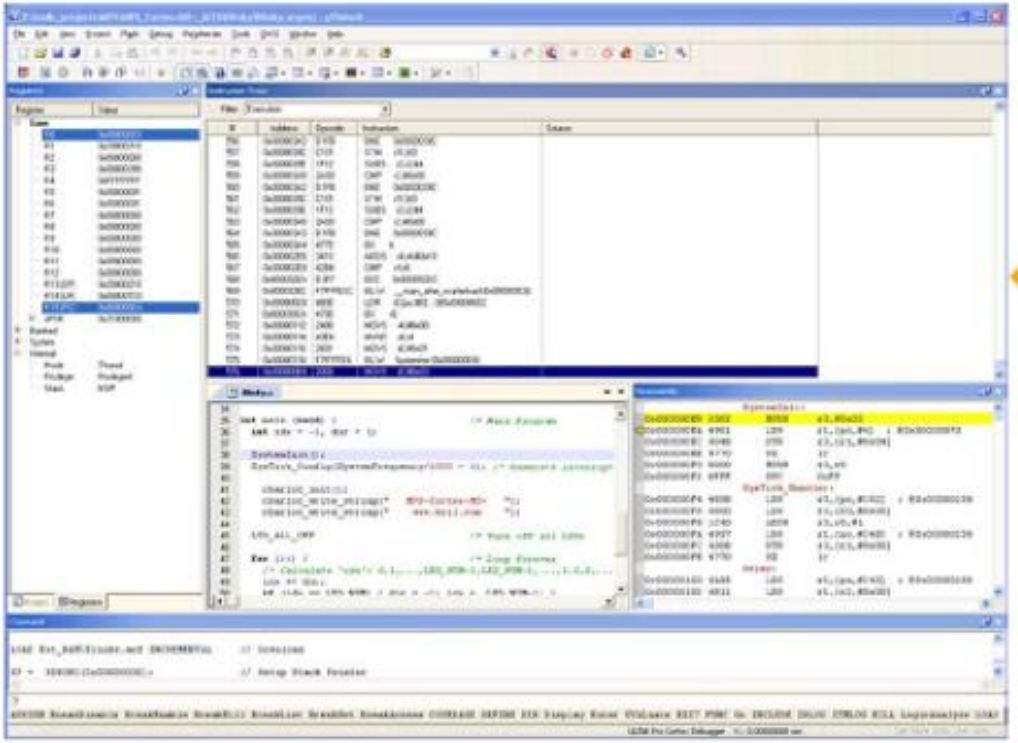
Cortex M0+

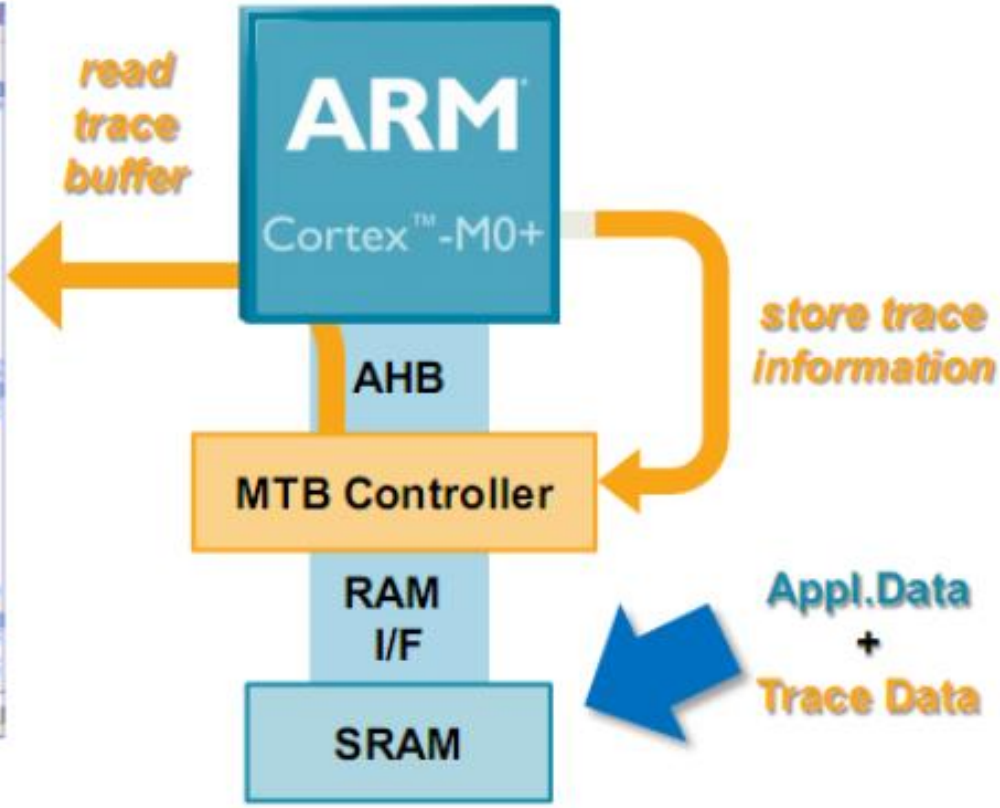
- Nested Vectored Interrupt Controller (NVIC)
  - Interrupções dentro de interrupções – Nested interrupt handling



Cortex M0+

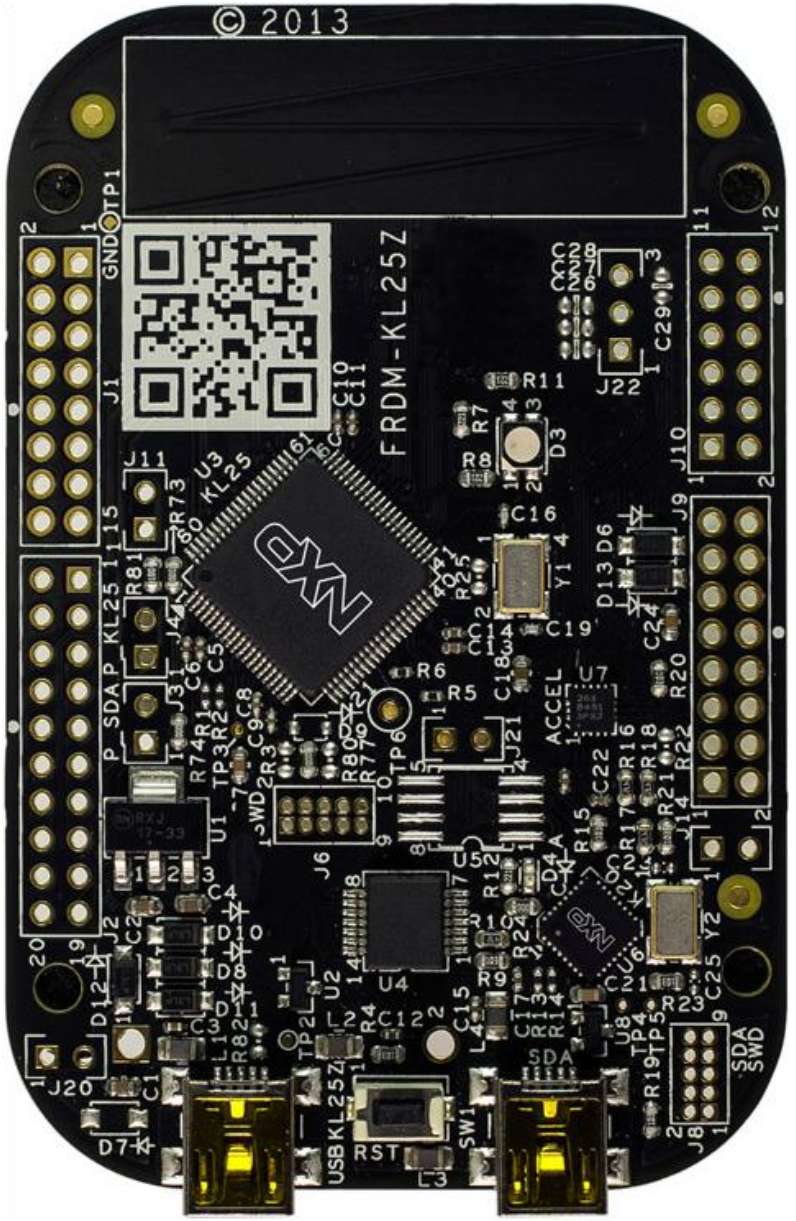
- Depuração / emulação





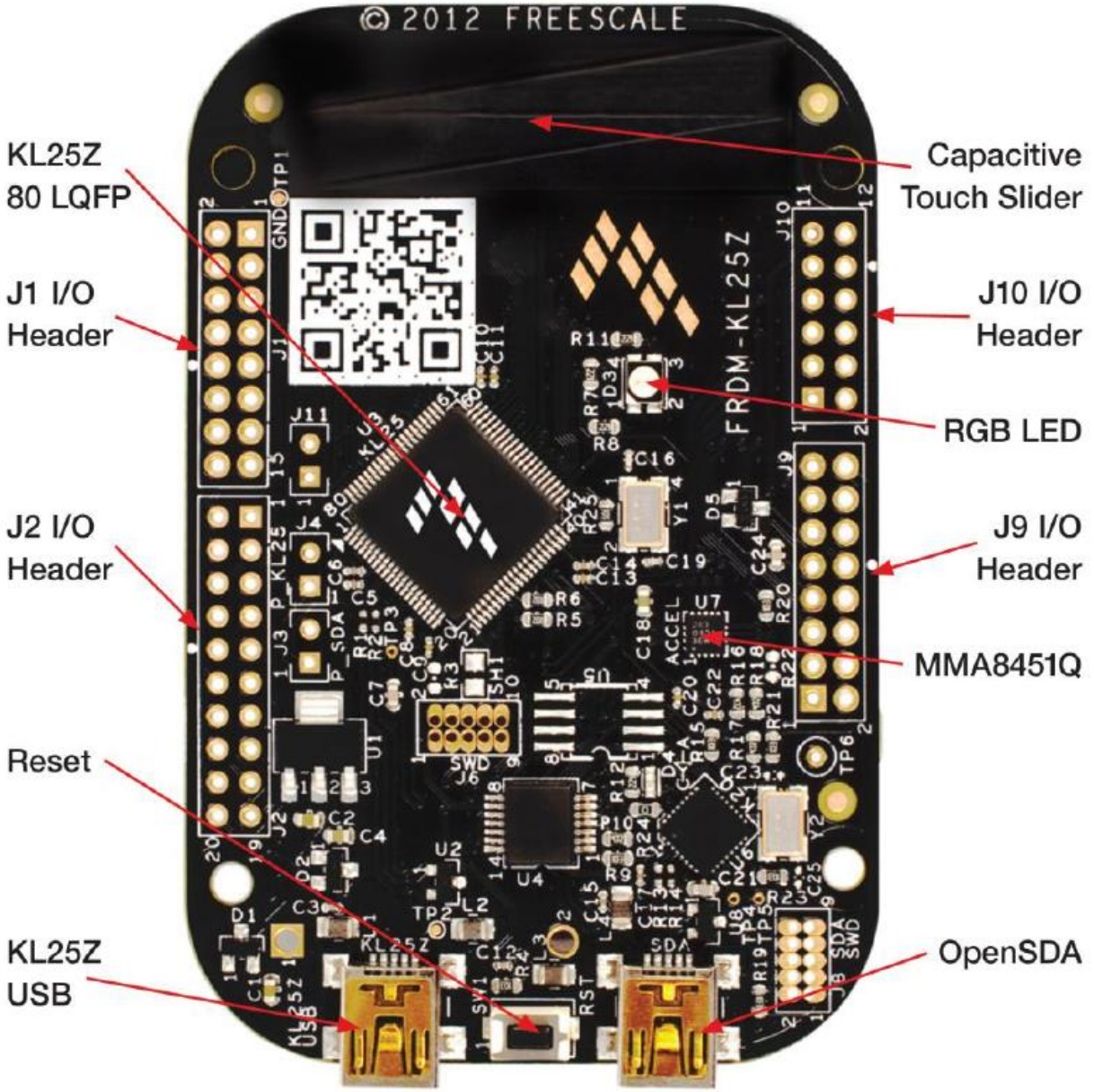
Kits de desenvolvimento

- Kit de desenvolvimento FRDM-KL25Z da empresa NXP Freescale
- Placa de propósito geral
- Visa mercado de automação e eletrônica

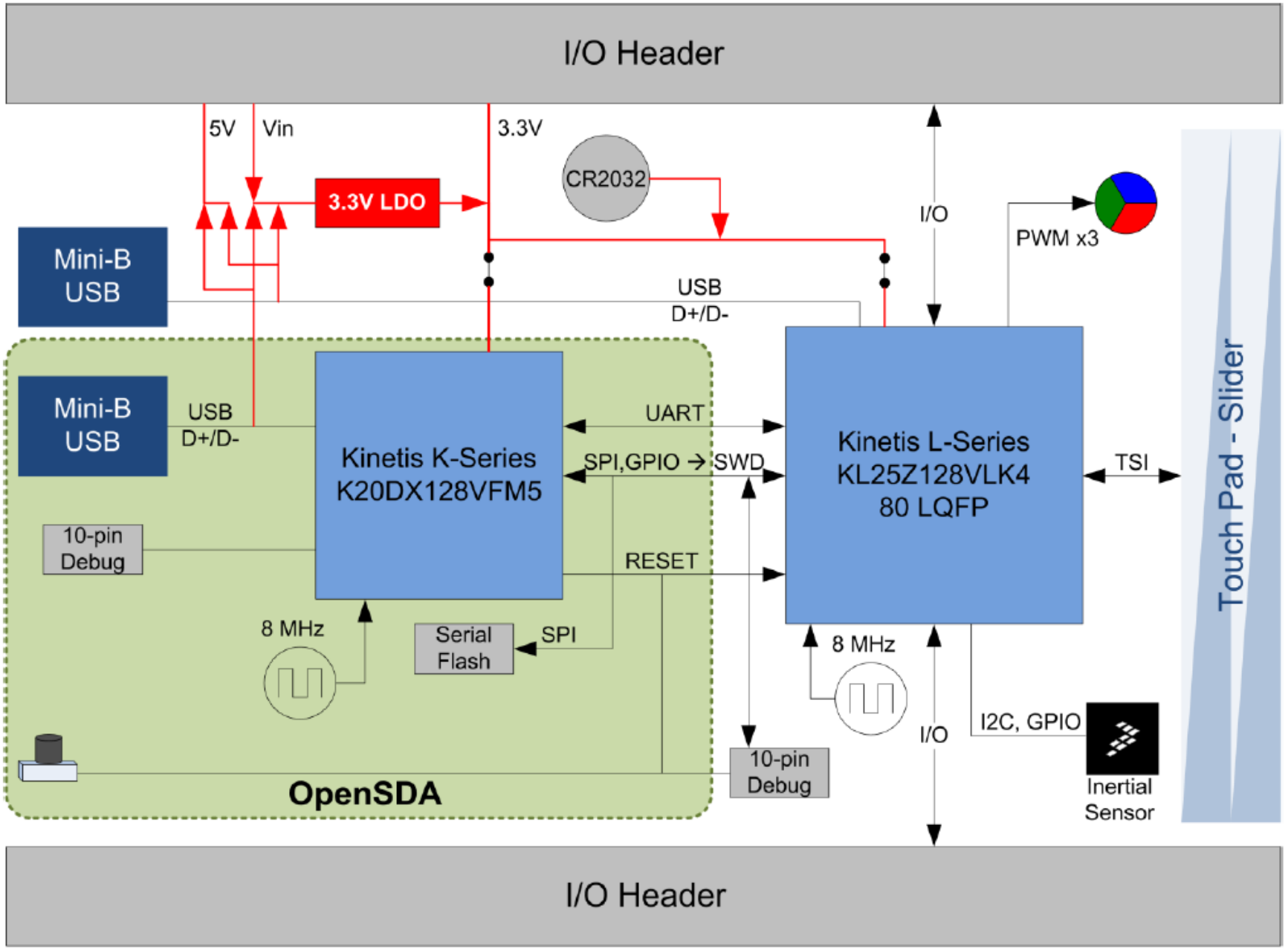


Kit FRDM-KL25Z

- CPU ARM Cortex M0+ modelo KL2x, mais especificamente MKL25Z128VLK4
- Tamanho e conexões compatíveis com Arduino



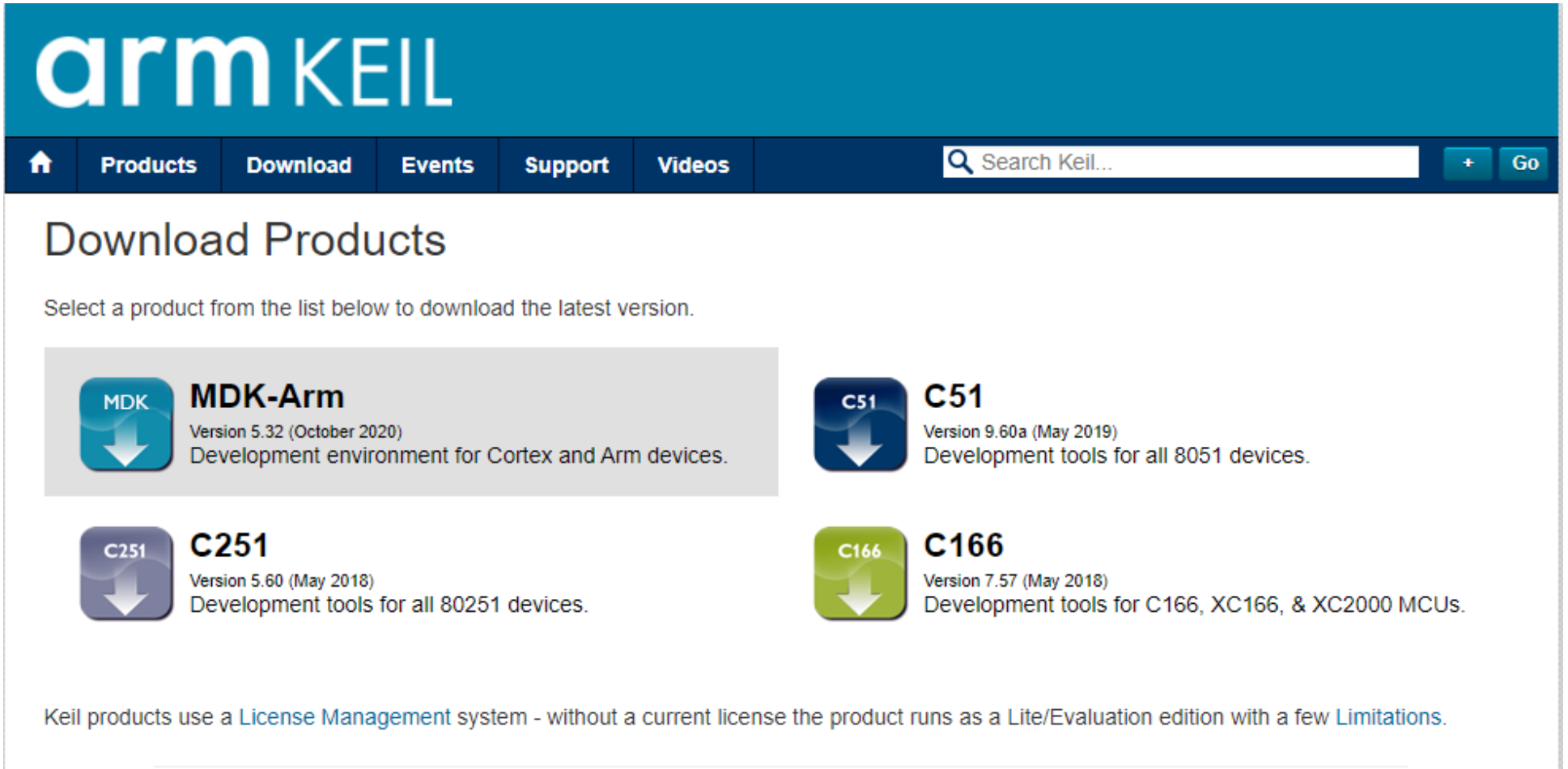
Kit FRDM-KL25Z



Software

Keil ARM

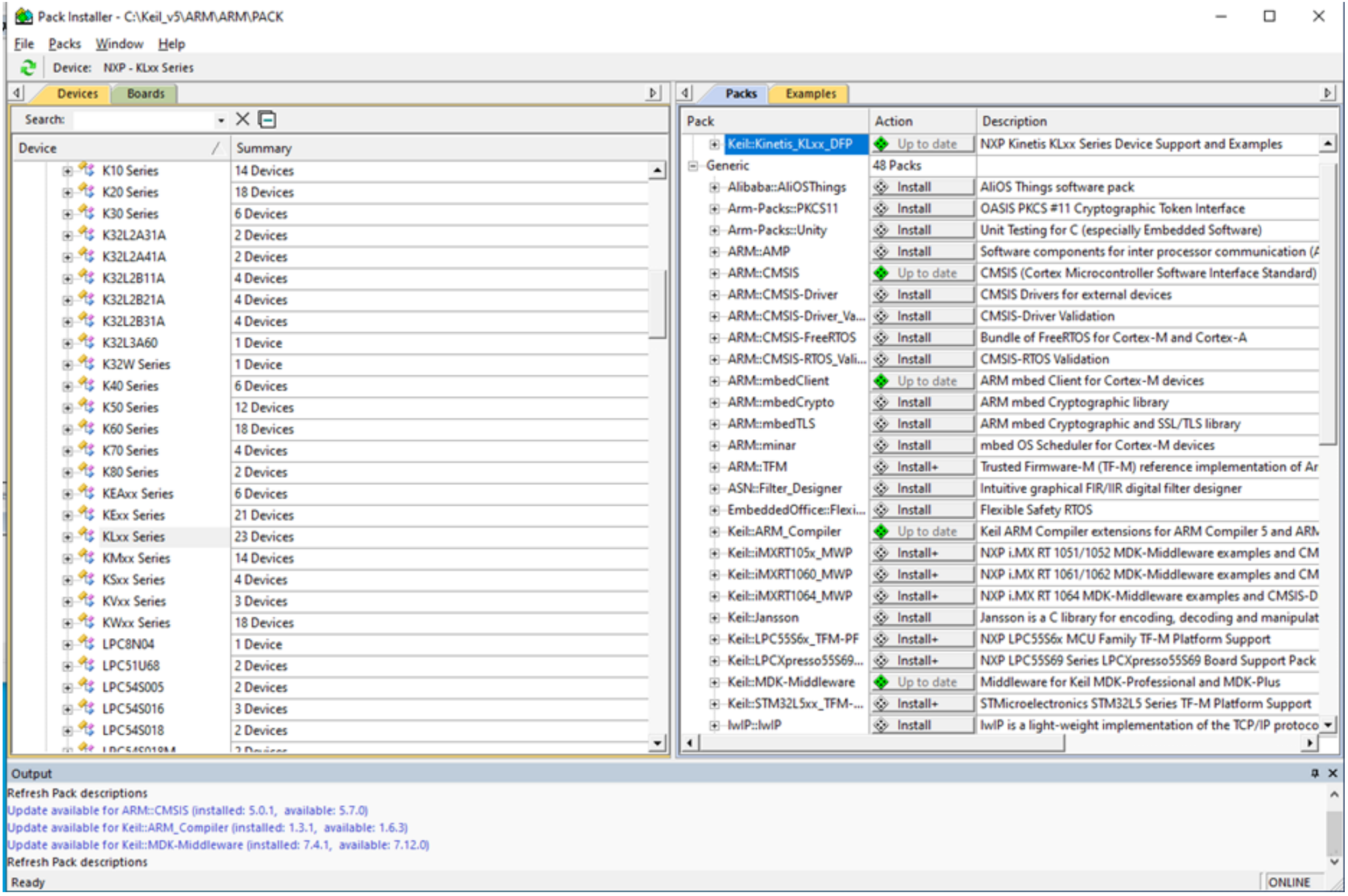
- Mesma interface Keil uVision



Software

Keil ARM

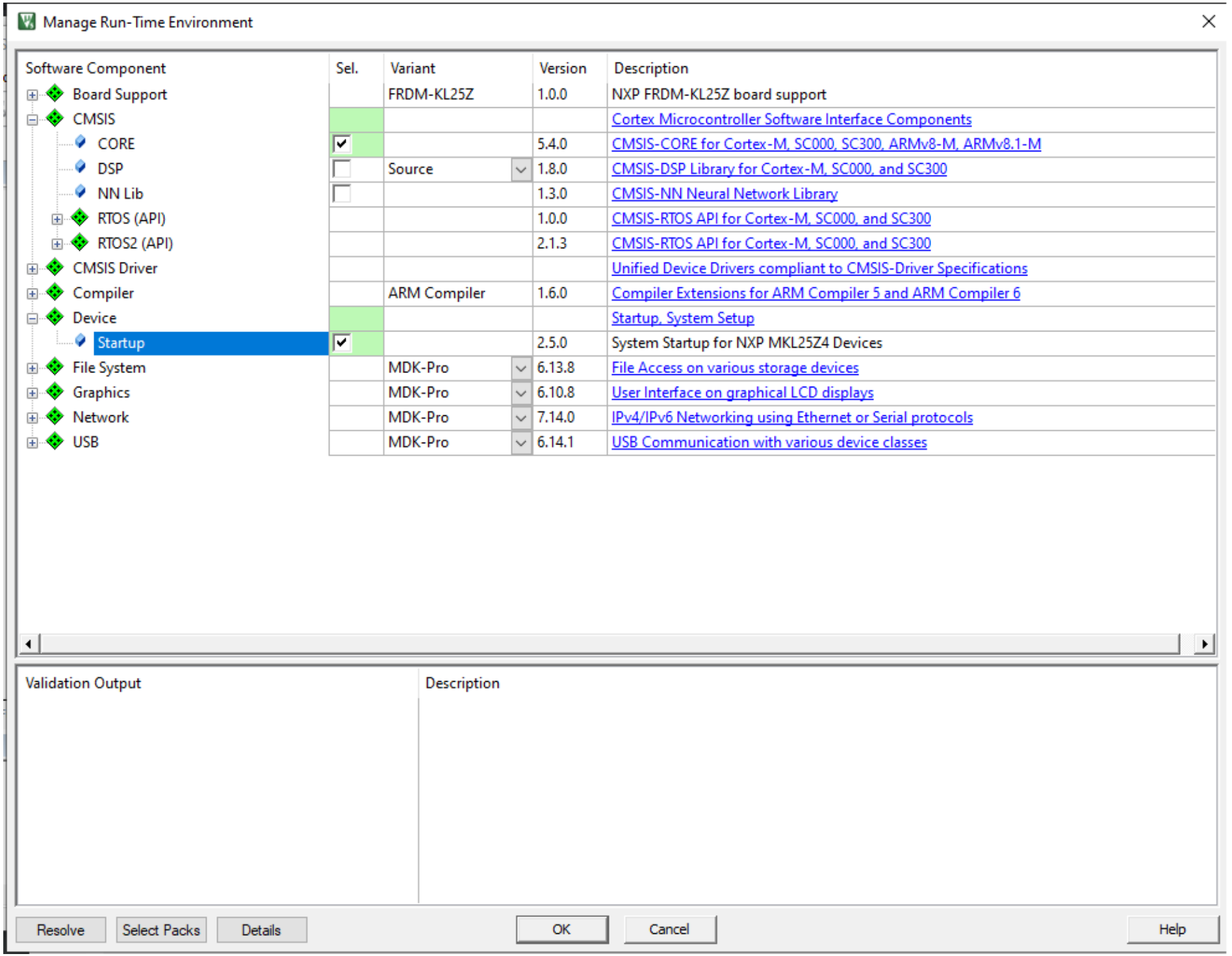
- Detalhes da instalação
  - Além da ferramenta instalar pacotes
  - No caso instalar plataforma NXP KL2x
    - CMSIS Core
    - Device Startup


Pack Installer - C:\Keil_v5\ARM\ARM\PACK
File Packs Window Help
Device: NXP - KLxx Series
Devices Boards
Search:
Device
Summary
K10 Series 14 Devices
K20 Series 18 Devices
K30 Series 6 Devices
K32L2A31A 2 Devices
K32L2A41A 2 Devices
K32L2B11A 4 Devices
K32L2B21A 4 Devices
K32L2B31A 4 Devices
K32L3A60 1 Device
K32W Series 1 Device
K40 Series 6 Devices
K50 Series 12 Devices
K60 Series 18 Devices
K70 Series 4 Devices
K80 Series 2 Devices
KEAxx Series 6 Devices
KExx Series 21 Devices
KLxx Series 23 Devices
KMxx Series 14 Devices
KSxx Series 4 Devices
KVxx Series 3 Devices
KWxx Series 18 Devices
LPC8N04 1 Device
LPC51U68 2 Devices
LPC54S005 2 Devices
LPC54S016 3 Devices
LPC54S018 2 Devices
Packs Examples
Pack
Action
Description
Keil::Kinetis_KLxx_DFP Up to date NXP Kinetis KLxx Series Device Support and Examples
Generic 48 Packs
Alibaba::AliOSThings Install AliOS Things software pack
Arm-Packs::PKCS11 Install OASIS PKCS #11 Cryptographic Token Interface
Arm-Packs::Unity Install Unit Testing for C (especially Embedded Software)
ARM::AMP Install Software components for inter processor communication
ARM::CMSIS Up to date CMSIS (Cortex Microcontroller Software Interface Standard)
ARM::CMSIS-Driver Install CMSIS Drivers for external devices
ARM::CMSIS-Driver_Va... Install CMSIS-Driver Validation
ARM::CMSIS-FreeRTOS Install Bundle of FreeRTOS for Cortex-M and Cortex-A
ARM::CMSIS-RTOS_Vali... Install CMSIS-RTOS Validation
ARM::mbedClient Up to date ARM mbed Client for Cortex-M devices
ARM::mbedCrypto Install ARM mbed Cryptographic library
ARM::mbedTLS Install ARM mbed Cryptographic and SSL/TLS library
ARM::minar Install mbed OS Scheduler for Cortex-M devices
ARM::TFM Install+ Trusted Firmware-M (TF-M) reference implementation of Ar
ASN::Filter_Designer Install Intuitive graphical FIR/IIR digital filter designer
EmbeddedOffice::Flexi... Install Flexible Safety RTOS
Keil::ARM_Compiler Up to date Keil ARM Compiler extensions for ARM Compiler 5 and ARM
Keil::iMXRT105x_MWP Install+ NXP i.MX RT 1051/1052 MDK-Middleware examples and CM
Keil::iMXRT1060_MWP Install+ NXP i.MX RT 1061/1062 MDK-Middleware examples and CM
Keil::iMXRT1064_MWP Install+ NXP i.MX RT 1064 MDK-Middleware examples and CMSIS-D
Keil::Jansson Install Jansson is a C library for encoding, decoding and manipulat
Keil::LPC55S6x_TFM-PF Install+ NXP LPC55S6x MCU Family TF-M Platform Support
Keil::LPCXpresso55S69... Install+ NXP LPC55S69 Series LPCXpresso55S69 Board Support Pack
Keil::MDK-Middleware Up to date Middleware for Keil MDK-Professional and MDK-Plus
Keil::STM32L5xx_TFM-... Install+ STMicroelectronics STM32L5 Series TF-M Platform Support
lwIP::lwIP Install lwIP is a light-weight implementation of the TCP/IP protoco
Output
Refresh Pack descriptions
Update available for ARM::CMSIS (installed: 5.0.1, available: 5.7.0)
Update available for Keil::ARM_Compiler (installed: 1.3.1, available: 1.6.3)
Update available for Keil::MDK-Middleware (installed: 7.4.1, available: 7.12.0)
Refresh Pack descriptions
Ready
ONLINE

Software

Keil ARM

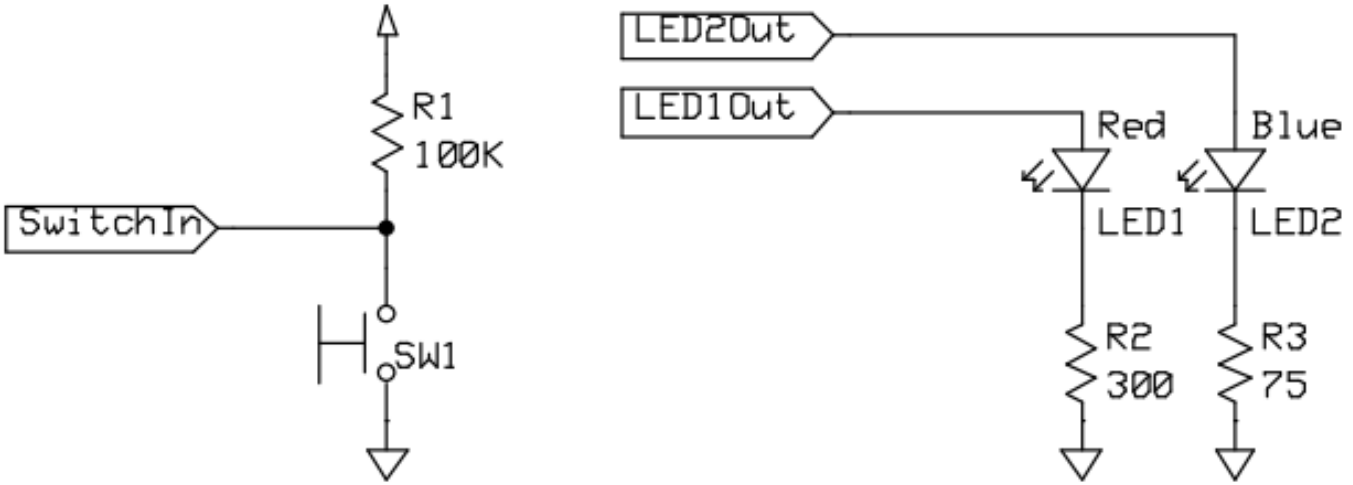
- Detalhes do projeto
  - Além do arquivo C adicionar módulos dos pacotes instalados
  - No caso instalar
    - Compilador
    - Middleware
    - CMSIS


Manage Run-Time Environment
Software Component
Sel.
Variant
Version
Description
Board Support
FRDM-KL25Z
1.0.0
NXP FRDM-KL25Z board support
CMSIS
Cortex Microcontroller Software Interface Components
CORE
5.4.0
CMSIS-CORE for Cortex-M, SC000, SC300, ARMv8-M, ARMv8.1-M
DSP
Source
1.8.0
CMSIS-DSP Library for Cortex-M, SC000, and SC300
NN Lib
1.3.0
CMSIS-NN Neural Network Library
RTOS (API)
1.0.0
CMSIS-RTOS API for Cortex-M, SC000, and SC300
RTOS2 (API)
2.1.3
CMSIS-RTOS API for Cortex-M, SC000, and SC300
CMSIS Driver
Unified Device Drivers compliant to CMSIS-Driver Specifications
Compiler
ARM Compiler
1.6.0
Compiler Extensions for ARM Compiler 5 and ARM Compiler 6
Device
Startup, System Setup
Startup
2.5.0
System Startup for NXP MKL25Z4 Devices
File System
MDK-Pro
6.13.8
File Access on various storage devices
Graphics
MDK-Pro
6.10.8
User Interface on graphical LCD displays
Network
MDK-Pro
7.14.0
IPv4/IPv6 Networking using Ethernet or Serial protocols
USB
MDK-Pro
6.14.1
USB Communication with various device classes
Validation Output
Description
Resolve
Select Packs
Details
OK
Cancel
Help

Cortex M0+

- GPIO

General-purpose (Digital !) Input and Output



Cortex M0+

- GPIO

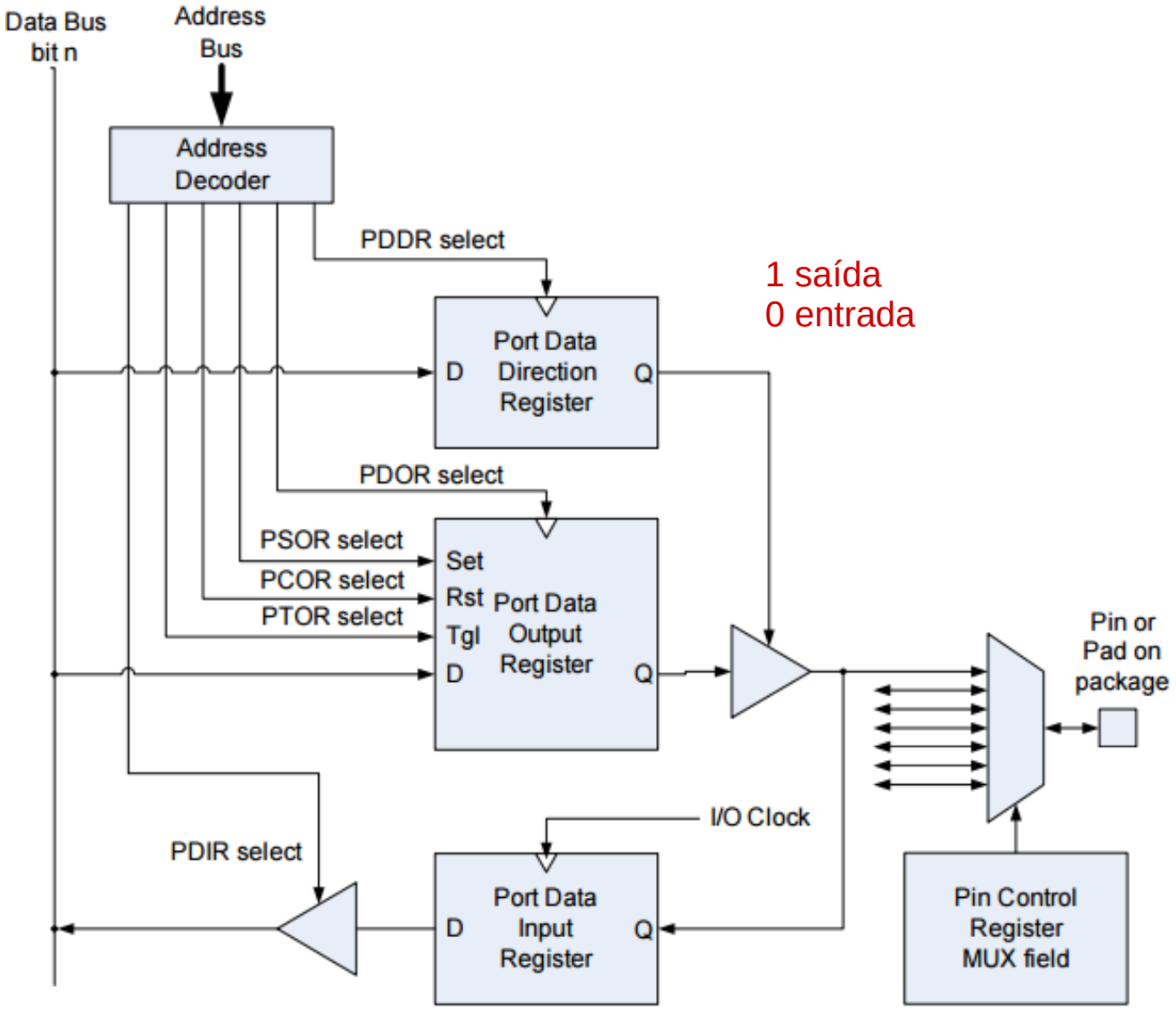
Direção PDDR

Registradores especiais

Escrita + PDOR

set, reset, toggle

Leitura PDIR



Define velocidade, consumo de energia, A ou D pra cada pino

Cortex M0+

- GPIO Registradores especiais

  escrita set,

  reset,

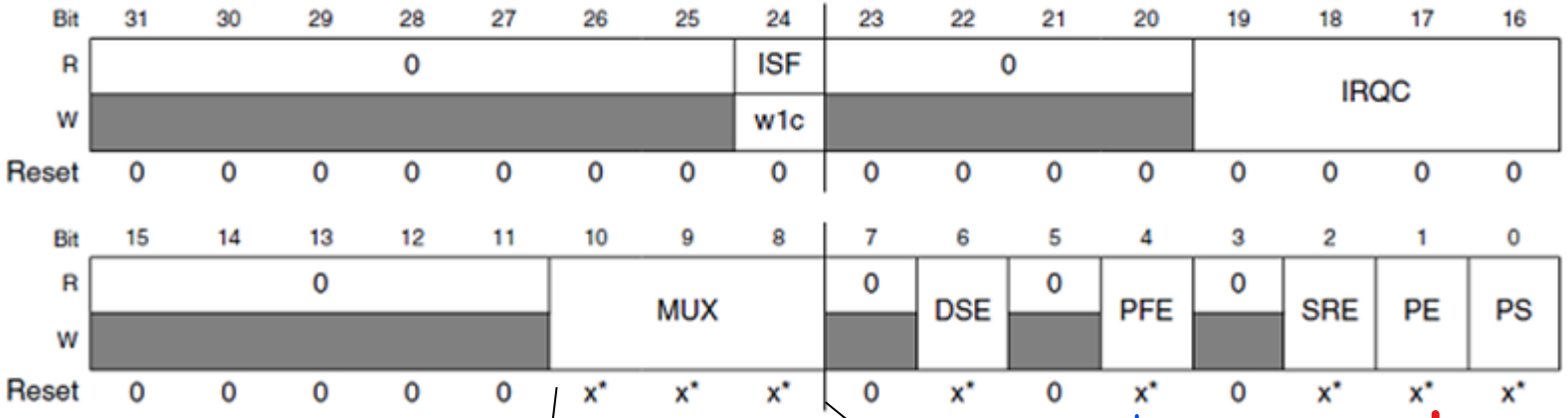
  toggle,
  leitura
  direção

Absolute address (hex)	Register name	Width (in bits)
400F_F000	Port Data Output Register (GPIOA_PDOR)	32
400F_F004	Port Set Output Register (GPIOA_PSOR)	32
400F_F008	Port Clear Output Register (GPIOA_PCOR)	32
400F_F00C	Port Toggle Output Register (GPIOA_PTOR)	32
400F_F010	Port Data Input Register (GPIOA_PDIR)	32
400F_F014	Port Data Direction Register (GPIOA_PDDR)	32

Cortex M0+

- GPIO – Configuração individual por pino

habilita interrupção



filtro passa baixa

velocidade pino

pull up (sim ou não)

pull up ou pull down

maneira como vai trabalhar

MUX (bits 10-8)	Configuration
000	Pin disabled (analog)
001	Alternative 1 – GPIO
010	Alternative 2
011	Alternative 3
100	Alternative 4
101	Alternative 5
110	Alternative 6
111	Alternative 7

Registrador PCR
Port Control
Register

Cortex M0+

- GPIOs
- Dois modos de acesso:
  - GPIO
    - Acesso normal
  - FGPIO
    - Acesso rápido

- Ambos atuam sobre a mesma porta, mas usam endereços diferentes (GPIOx vs FGPIOx)
  - Ex:

```
GPIOB_PTOR = 1;

FGPIOB_PTOR = 1;
```

Cortex M0+

- Controle de energia
- O módulo **SIM (system integration module)** provê controle do sistema e configuração do chip

Register name	Width (in bits)	Access	Reset value
System Options Register 1 (SIM_SOPT1)	32	R/W	See section
SOPT1 Configuration Register (SIM_SOPT1CFG)	32	R/W	0000_0000h
System Options Register 2 (SIM_SOPT2)	32	R/W	0000_0000h
System Options Register 4 (SIM_SOPT4)	32	R/W	0000_0000h
System Options Register 5 (SIM_SOPT5)	32	R/W	0000_0000h
System Options Register 7 (SIM_SOPT7)	32	R/W	0000_0000h
System Device Identification Register (SIM_SDID)	32	R	See section
System Clock Gating Control Register 4 (SIM_SCGC4)	32	R/W	F000_0030h
System Clock Gating Control Register 5 (SIM_SCGC5)	32	R/W	0000_0180h
System Clock Gating Control Register 6 (SIM_SCGC6)	32	R/W	0000_0001h
System Clock Gating Control Register 7 (SIM_SCGC7)	32	R/W	0000_0100h
System Clock Divider Register 1 (SIM_CLKDIV1)	32	R/W	See section
Flash Configuration Register 1 (SIM_FCFG1)	32	R/W	See section
Flash Configuration Register 2 (SIM_FCFG2)	32	R	See section
Unique Identification Register Mid-High (SIM_UIDMH)	32	R	See section
Unique Identification Register Mid Low (SIM_UIDML)	32	R	See section
Unique Identification Register Low (SIM_UIDL)	32	R	See section
COP Control Register (SIM_COPC)	32	R/W	0000_000Ch
Service COP Register (SIM_SRVCOP)	32	W	0000_0000h

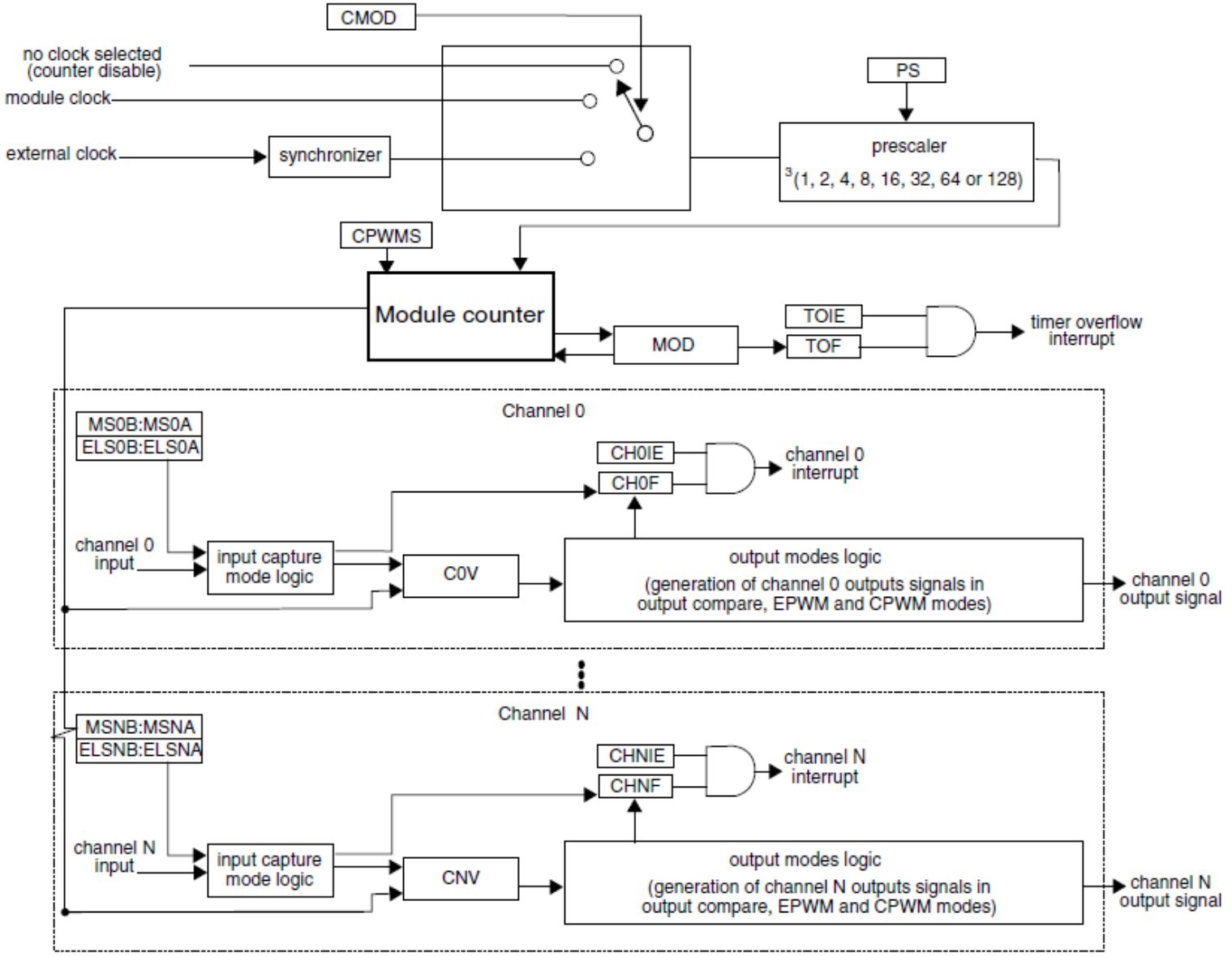
Cortex M0+

- TIMERS
- Arquitetura prevê modelos de timers voltados para diferentes aplicações, por isso disponibiliza diversas opções
  - TPM
  - PIT
  - LPTMR
  - Real-Time Clock

TPM – Timer/PWM Module

- TPM – Timer/PWM Module
  - Contador de 16 bits
  - Prescaler até 128
  - Se conecta a pinos de I/O
  - Suporta captura
  - Pode ser usado para gerar PWM
  - Modos:
    - Set
    - Clear
    - toogle
  - Pode ser usado para interrupções

TPM – Timer/PWM Module



TPM – Timer/PWM Module

- TPM - Timer/PWM Module

  - CMOD: seleciona clock interno ou externo
  - CPWMS: contador up (0) ou up / down (1)

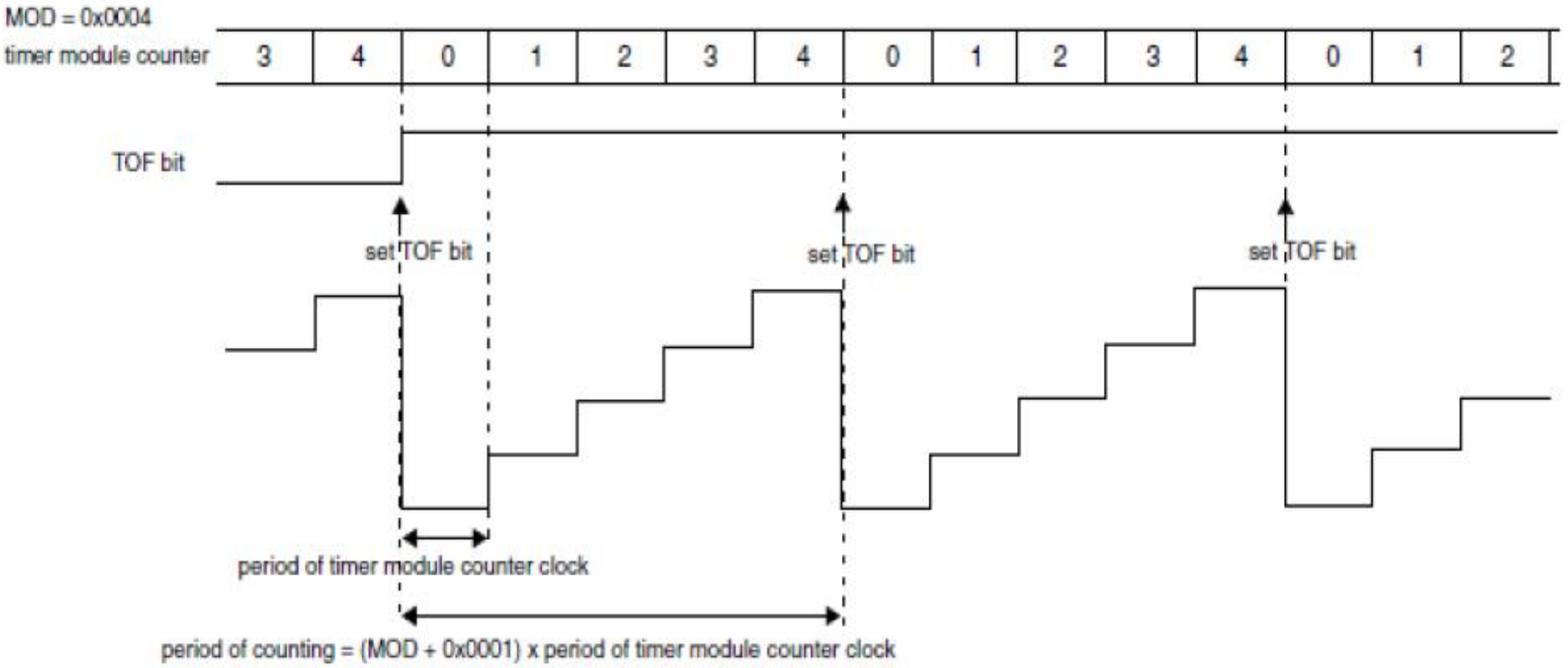
  Modo Up : 0, 1, 2, … MOD, 0/Overflow, 1, 2, … MOD
  Modo Up/down : 0, 1, 2, … MOD, MOD-1/Interrupt, MOD-2, … 2, 1, 0, 1, 2, …

  - MOD: valor de 16 bits (modulo)

  Overflow ao atingir MOD

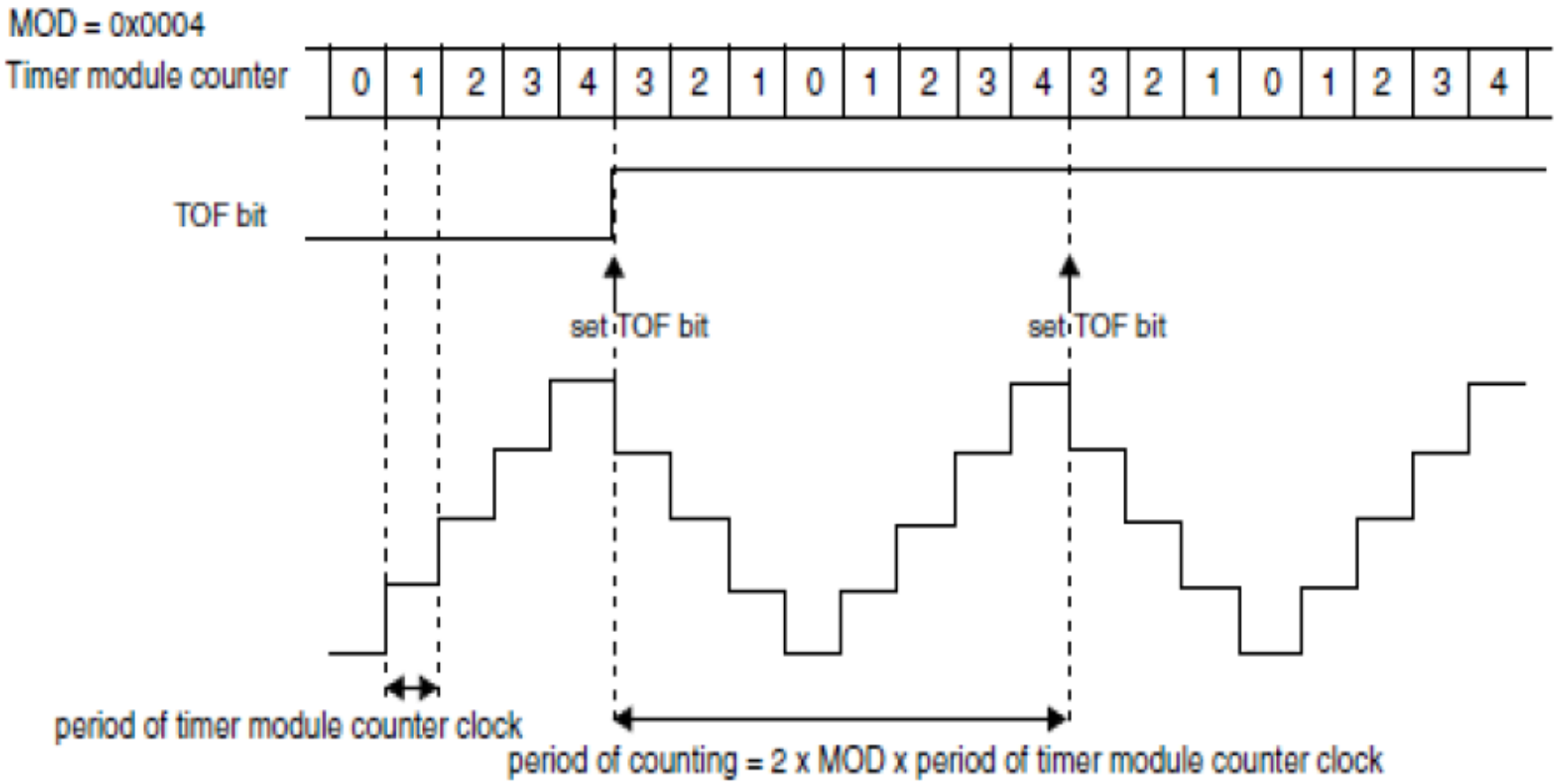
TPM – Timer/PWM Module

- Modo Up :



TPM – Timer/PWM Module

- Modo Up/down :



TPM – Timer/PWM Module

- Registradores por timer/canal

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value
4003_8000	Status and Control (TPM0_SC)	32	R/W	0000_0000h
4003_8004	Counter (TPM0_CNT)	32	R/W	0000_0000h
4003_8008	Modulo (TPM0_MOD)	32	R/W	0000_FFFFh
4003_800C	Channel (n) Status and Control (TPM0_C0SC)	32	R/W	0000_0000h
4003_8010	Channel (n) Value (TPM0_C0V)	32	R/W	0000_0000h
4003_8014	Channel (n) Status and Control (TPM0_C1SC)	32	R/W	0000_0000h
4003_8018	Channel (n) Value (TPM0_C1V)	32	R/W	0000_0000h
4003_801C	Channel (n) Status and Control (TPM0_C2SC)	32	R/W	0000_0000h
4003_8020	Channel (n) Value (TPM0_C2V)	32	R/W	0000_0000h
4003_8024	Channel (n) Status and Control (TPM0_C3SC)	32	R/W	0000_0000h
4003_8028	Channel (n) Value (TPM0_C3V)	32	R/W	0000_0000h
4003_802C	Channel (n) Status and Control (TPM0_C4SC)	32	R/W	0000_0000h
4003_8030	Channel (n) Value (TPM0_C4V)	32	R/W	0000_0000h
4003_8034	Channel (n) Status and Control (TPM0_C5SC)	32	R/W	0000_0000h
4003_8038	Channel (n) Value (TPM0_C5V)	32	R/W	0000_0000h
4003_8050	Capture and Compare Status (TPM0_STATUS)	32	R/W	0000_0000h
4003_8084	Configuration (TPM0_CONF)	32	R/W	0000_0000h

TPM – Timer/PWM Module

- Registrador de status e controle

TPMx_SC

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0							DMA	TOF	TOIE	CPWMS	CMOD		PS		
W									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DMA

0 Disables DMA transfers.
1 Enables DMA transfers.

TOF

0 LPTPM counter has not overflowed
1 LPTPM counter has overflowed.

TOIE

0 Disable TOF interrupts.
1 Enable TOF interrupts.

CPWMS

0 up counting mode.
1 up-down counting mode.

CMOD

00 LPTPM disabled
01 counter increments on LPTPM clock
10 counter increments on synchronized LPTPM_EXTCLK
11 Reserved

PS

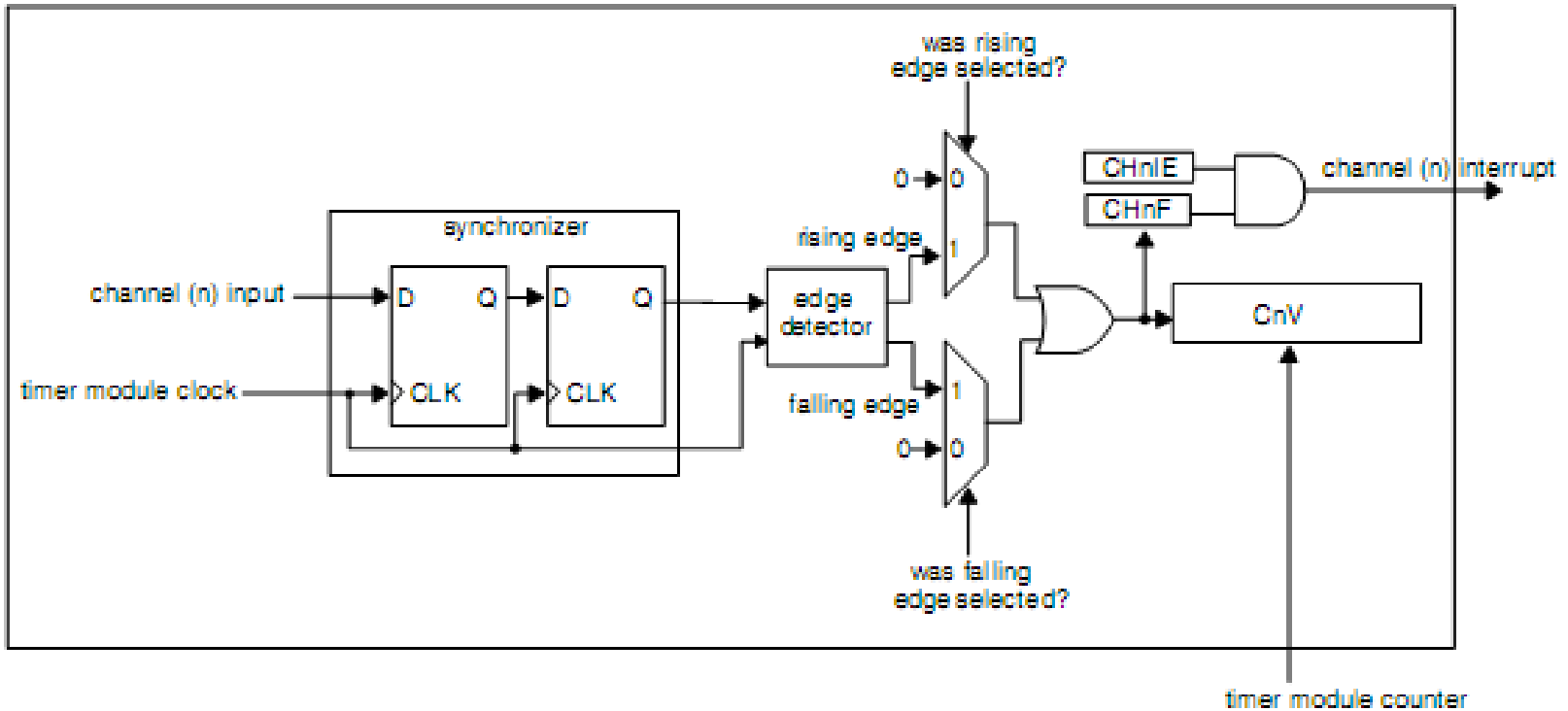
000 Divide by 1
001 Divide by 2
010 Divide by 4
011 Divide by 8
100 Divide by 16
101 Divide by 32
110 Divide by 64
111 Divide by 128

TPM – Timer/PWM Module

- TPM – Timer/PWM Module
  - No caso de captura o valor instantaneo do contador é armazenado no registrador CnV correspondente

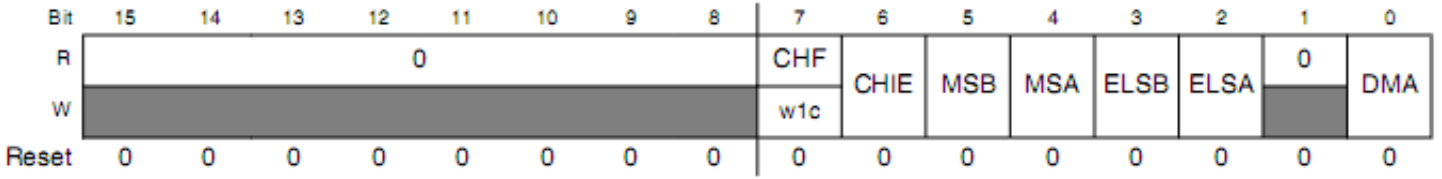
TPMx_CnV

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																VAL															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0



TPM – Timer/PWM Module

- Registrador de status e controle por canal



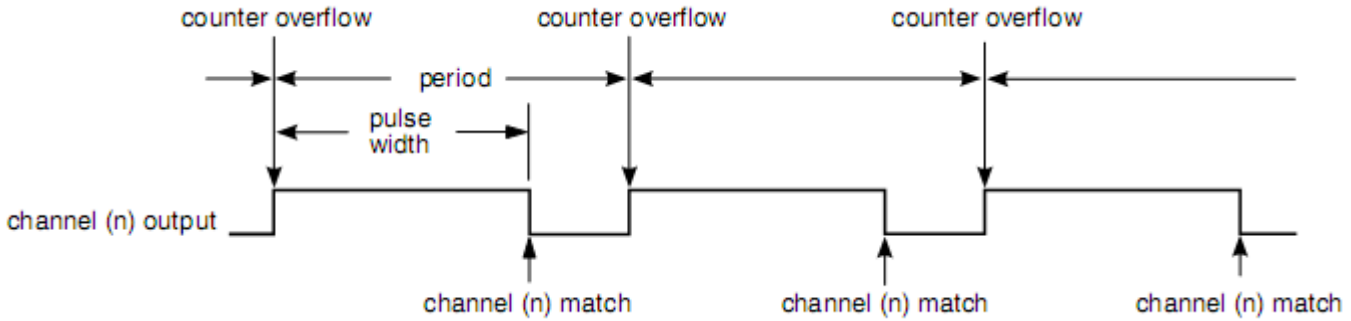
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0								CHF	CHIE	MSB	MSA	ELSB	ELSA	0	DMA
W									w1c							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

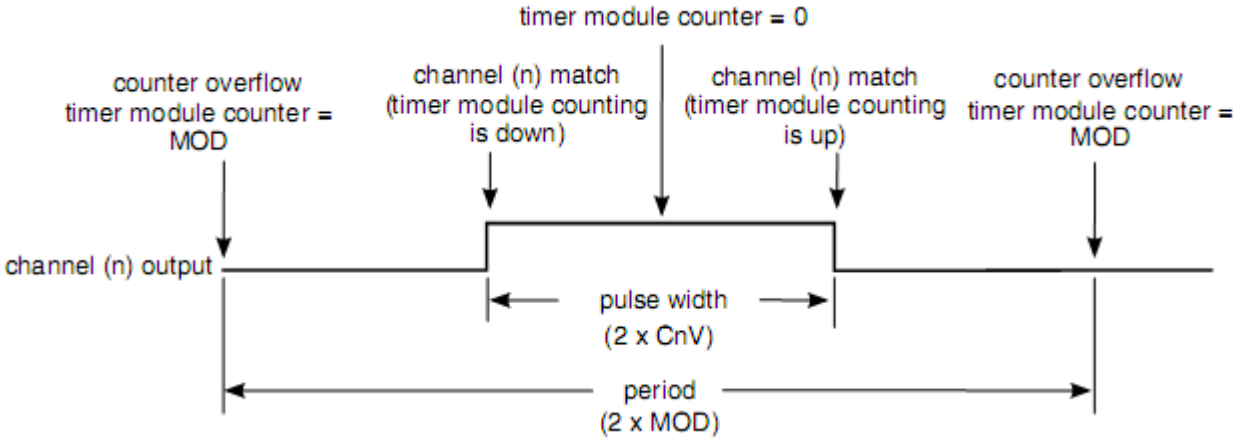
CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	00	00	None	Channel disabled
X	01/10/11	00	Software compare	Pin not used for LPTPM
0	00	01	Input capture	Capture on Rising Edge Only
		10		Capture on Falling Edge Only
		11		Capture on Rising or Falling Edge
	01	01	Output compare	Toggle Output on match
		10		Clear Output on match
		11		Set Output on match
	10	10	Edge-aligned PWM	High-true pulses (clear Output on match, set Output on reload)
		X1		Low-true pulses (set Output on match, clear Output on reload)
	11	10	Output compare	Pulse Output low on match
		X1		Pulse Output high on match
1	10	10	Center-aligned PWM	High-true pulses (clear Output on match-up, set Output on match-down)
		X1		Low-true pulses (set Output on match-up, clear Output on match-down)

TPM – Timer/PWM Module

- TPM – Timer/PWM Module
  - No caso de saida gera mudança de pino quando o valor do contador for igual ao registrador CnV

ex





TPM – Timer/PWM Module

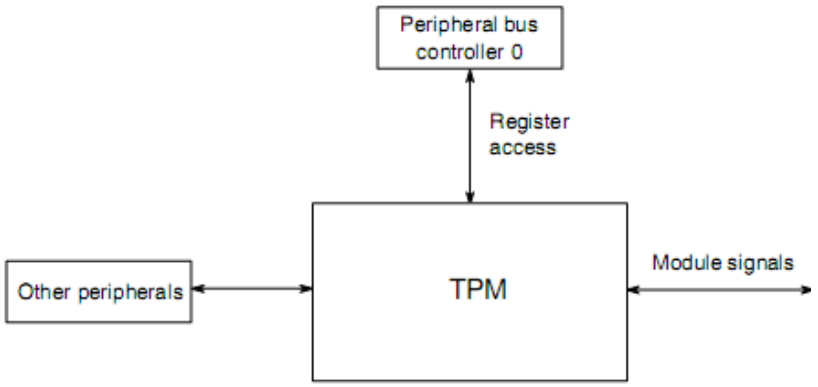
- Registrador de configuração

TPM = 8/3 freq da CPU

TPMx_CONF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0				TRGSEL				0					CROT	CSOO	CSOT
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0						GTBEEN	0	DBGMODE		DOZEEN	0				
W																
Reset	0	0	0	0	0	0	0	0								



TPMx_CONF[TRGSEL]	Selected source
0000	External trigger pin input (EXTRG_IN)
0001	CMP0 output
0010	Reserved
0011	Reserved
0100	PIT trigger 0
0101	PIT trigger 1
0110	Reserved
0111	Reserved
1000	TPM0 overflow
1001	TPM1 overflow
1010	TPM2 overflow
1011	Reserved
1100	RTC alarm
1101	RTC seconds
1110	LPTMR trigger
1111	Reserved

TPM – Timer/PWM Module

- TPM – Timer/PWM Module
  - Importante configurar pino

80 LQFP	64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
13	9	7	–	PTE20	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	UART0_TX			
14	10	8	–	PTE21	ADC0_DM0/ ADC0_SE4a	ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	UART0_RX			
15	11	–	–	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX			
16	12	–	–	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX			

Exemplo

- Desenvolver programa que pisque o LED vermelho da placa a uma frequencia de 4Hz
- Usar timer **TPM 0** para garantir temporização
- Detalhes da placa no manual