CSE – 5356

System On Chip

Project

REPORT

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INTRODUCTION:

Designing an I2C IP and its Linux Device Drivers on a DE1 -SoC Board is the goal of this project. The cyclone V chip, which is integrated with an FPGA and a dual core ARM processor, is part of the DE1 – Soc

Theory Of Operation:

This IP has Memory Mapped Avalon Interface. So, it can be controlled from processor by configuring the IP registers.

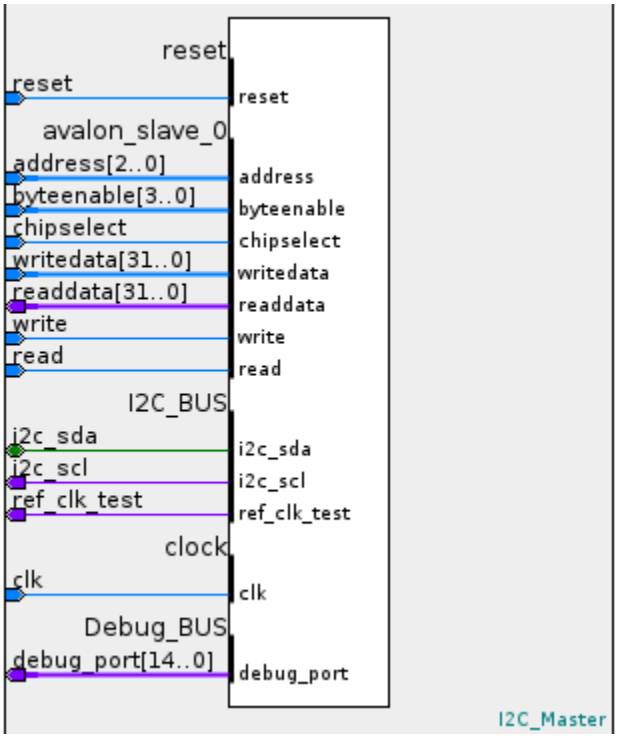
IP Registers:

Register	Reg Offset	Bits	Field	Function
ADDRESS (R/W)	0	6:0		7-bit address of the device
DATA (R/W)	4	7:0		Write: Write data to the TX FIFO Read: Reads data from the RX FIFO
STATUS (R/W1C)	8	0	RXFO	RX FIFO overflow (write 1 to clear)
		1	RXFF	RX FIFO full (auto clears when data is read)
		2	RXFE	RX FIFO empty (auto clears when data arrives)
		3	TXFO	TX FIFO overflow (write 1 to clear)
		4	TXFF	TX FIFO full (auto clears when data is sent)
		5	TXFE	TX FIFO empty (auto clears when data is written)
		6	ACK_ERROR	An ACK error occurred (write 1 to clear)
		7	BUSY	The module is busy transmitting or receiving
		31:8	DEBUG_IN	Debug interface (often used to peek at FSM)
CONTROL	12	0	R/~W	Direction of data on bus (read=1, write=0)

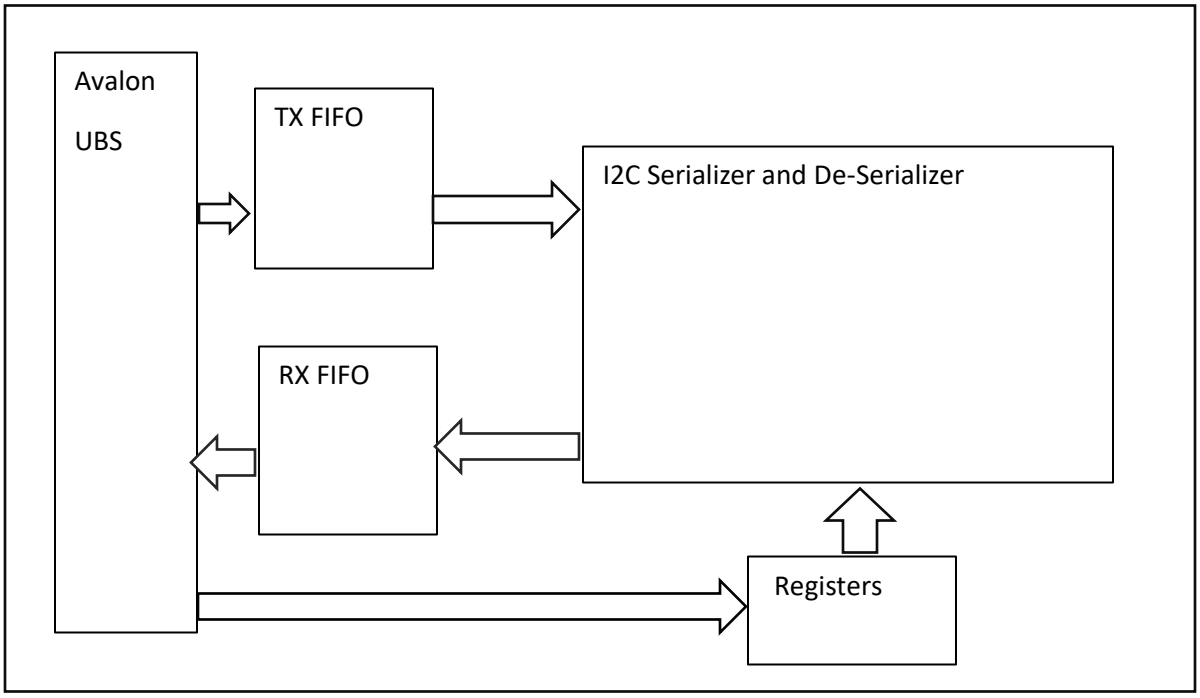
(R/W): reset 0		6:1	BYTE_COUNT	Number of bytes to be written or read
		7	USE_REGISTER	When reading and writing data from devices using internal registers, the register number should be sent after the address is sent.
		15:8	REGISTER	Register value to be sent
		16	USE_REPEATED_START	1 = use repeated start conditional on read, 0 = use stop followed by start condition on reads
		17	START	Write: 1 = start bus transaction, 0 = no effect Read: 0
		18	TEST_OUT	1 = enable test output, 0 = disable test output
		23:19	-	*reserved*
		31:24	DEBUG_OUT	Debug interface (can be used to drive GPO or LEDR ports)

(W = write, R = read, W1C = write 1 to clear)

IP Symbol:



IP Architecture:



Files Required:

Verilog:

1) I2C_Master.v

2) I2C_Serial_Interface.v

3) Sync_FIFO.v

Kernel Build Modules:

1)address_map.h

2)I2C_driver.c

3)I2C_Master_regs.h

Files Description:

1)Sync_FIFO.v : This is synchronous First in First Out module. This module is used two times (Transmitter FIFO and Receiver FIFO). During the write transaction, TX FIFO used, and RX FIFO is used during the read transaction.

2) I2C_Serial_Interface.v: This module takes the data from TX FIFO and serialize it and send it to the slave device as well as accept the data from slave device and send it to the RX FIFO.

3)I2C_Master.v: This module is the integration of above two modules with Avalon interface and register interface

4)address_map.h:Contains the base address of the IP

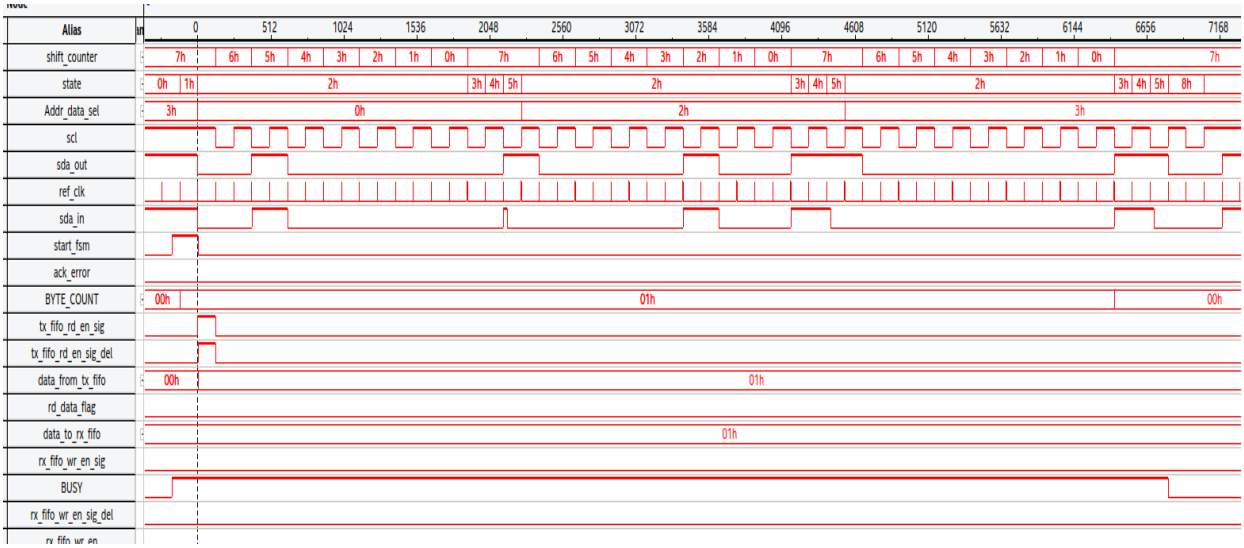
5)I2C_driver.c: Kernel code for the I2C IP and Kernel objects are as follows

File	Write value	Read value
/sys/kernel/i2c/mode	read or write	last written value
/sys/kernel/i2c/byte_count	0-63	last written value
/sys/kernel/i2c/register	0-255 or none	last written value
/sys/kernel/i2c/address	0-127	last written value
/sys/kernel/i2c/use_repeated_start	true or false	last written value
/sys/kernel/i2c/start	any value	current status
/sys/kernel/i2c/tx_data	value for TX_FIFO	N/A
/sys/kernel/i2c/rx_data	N/A	value in RX FIFO or -1 if empty

6)I2C_Master_regs.h: Contains all the register addresses

Tap Analyzer Results:

WRITE:



READ: