SDRAM Controller

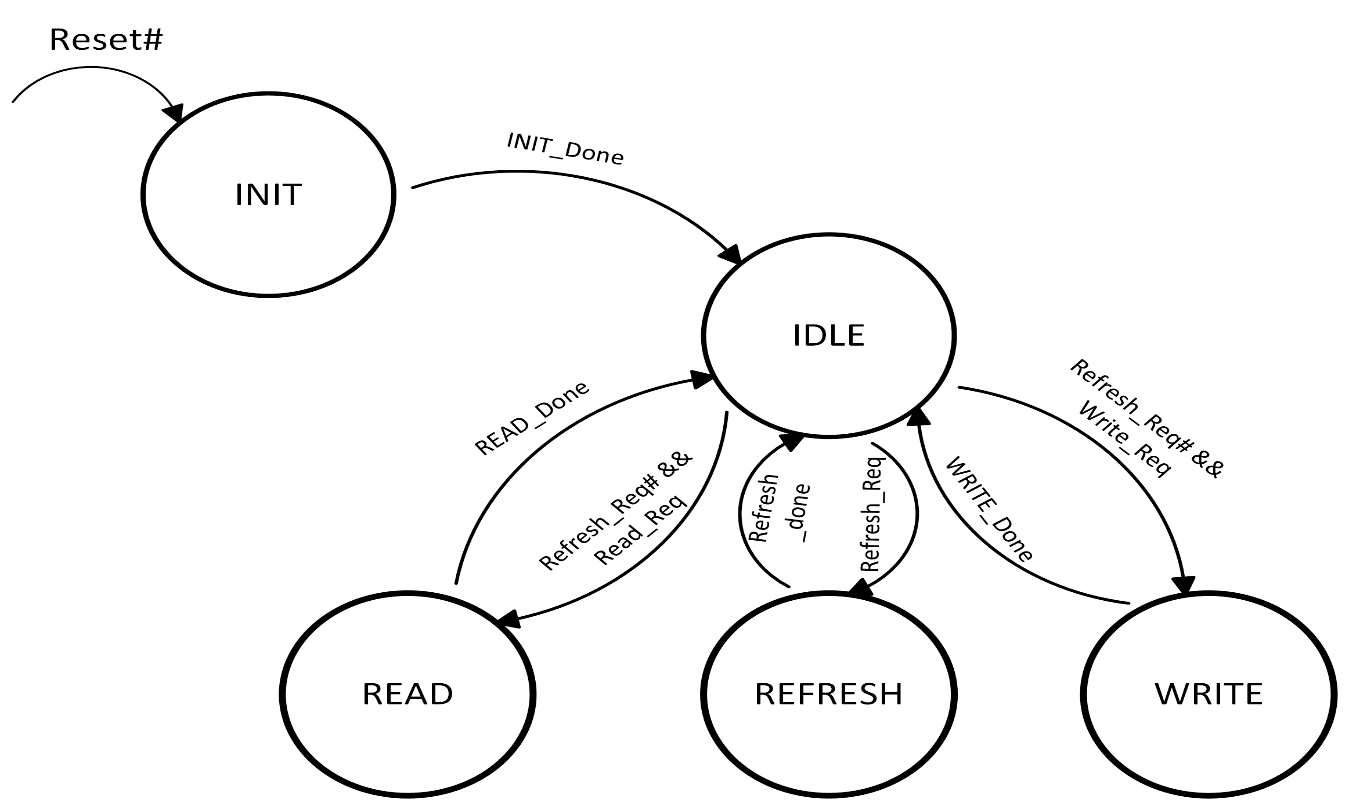
Introduction:

This SDRAM Controller is targeted for 80386DX i.e. to provide interface between asynchronous memory supported processor and SDR SDRAM(Single Data Rate Synchronous Dynamic Random Access Memory).

Theory Of Operation :

This Controller allows a single MT48LC16M4A2 to be connected to any CPU with a 32 bit asynchronous memory interface(In this paper we are targeting 80386DX).

The SDRAM controller’s top level Finite State Machine is shown below.



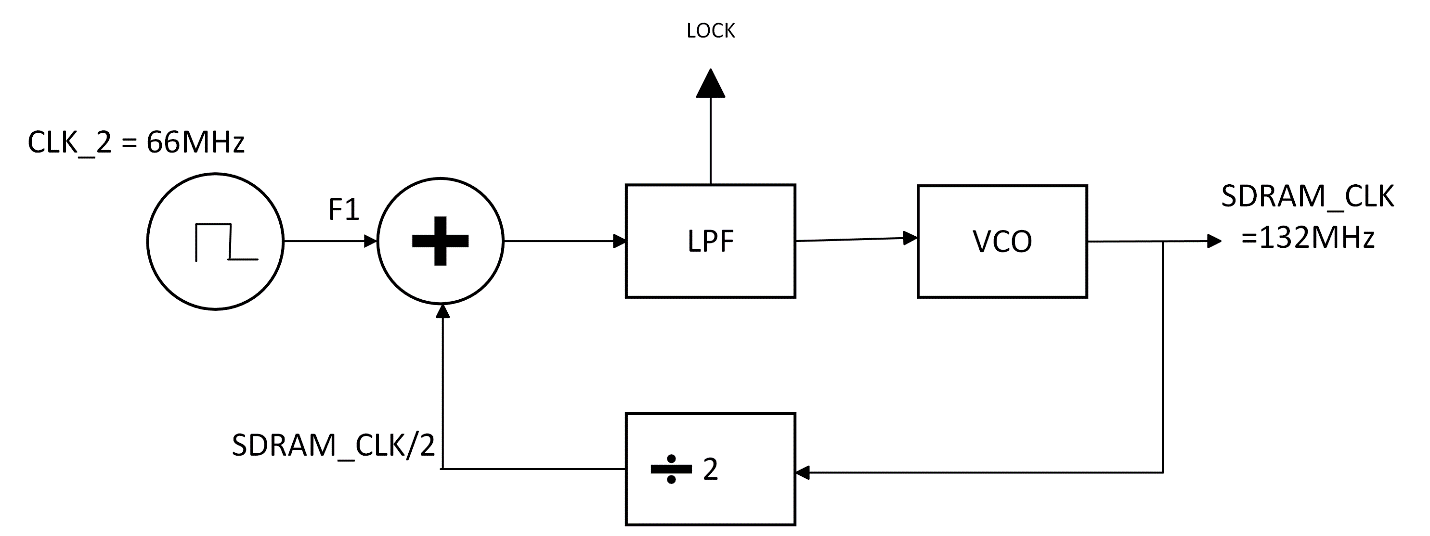
After coming out of reset, this controller will initialize the SDRAM in the INIT state and then enter the IDLE state . When a “Refresh\_Req” signal is received, the controller enters the REFRESH state and issue a “REFRESH” command to the SDRAM. “Refresh\_Req”is generated for every 15.625 μs by using a timer as all the SDRAM rows should be refreshed for every 64 ms (This value is specified by the memory chip vendor).If “Refresh\_Req” is generated when the controller is in READ state or WRITE state then the controller enters into REFRESH state after executing the READ state or WRITE state only .

Memory Chip Specifications:

1. Part Number : MT48LC16M4A2
2. Speed Grade : -7E
3. Clock Frequency : 132 MHz
4. Clock Period(tCK) : 7.5 ns
5. tRCD : 15 ns
6. tRP : 15 ns
7. tRFC : 66 ns

**SDRAM Clock Generation:**

SDRAM\_CLK(132 MHz) is generated using a PLL by taking CLK2 of 80386DX as reference for the PLL.Block Diagram for clock generation is shown below .



**Clock Cycles Calculations:**

Clock Cycles Calculation is done as below and all the clock cycles for required timing parameters are tabulated .

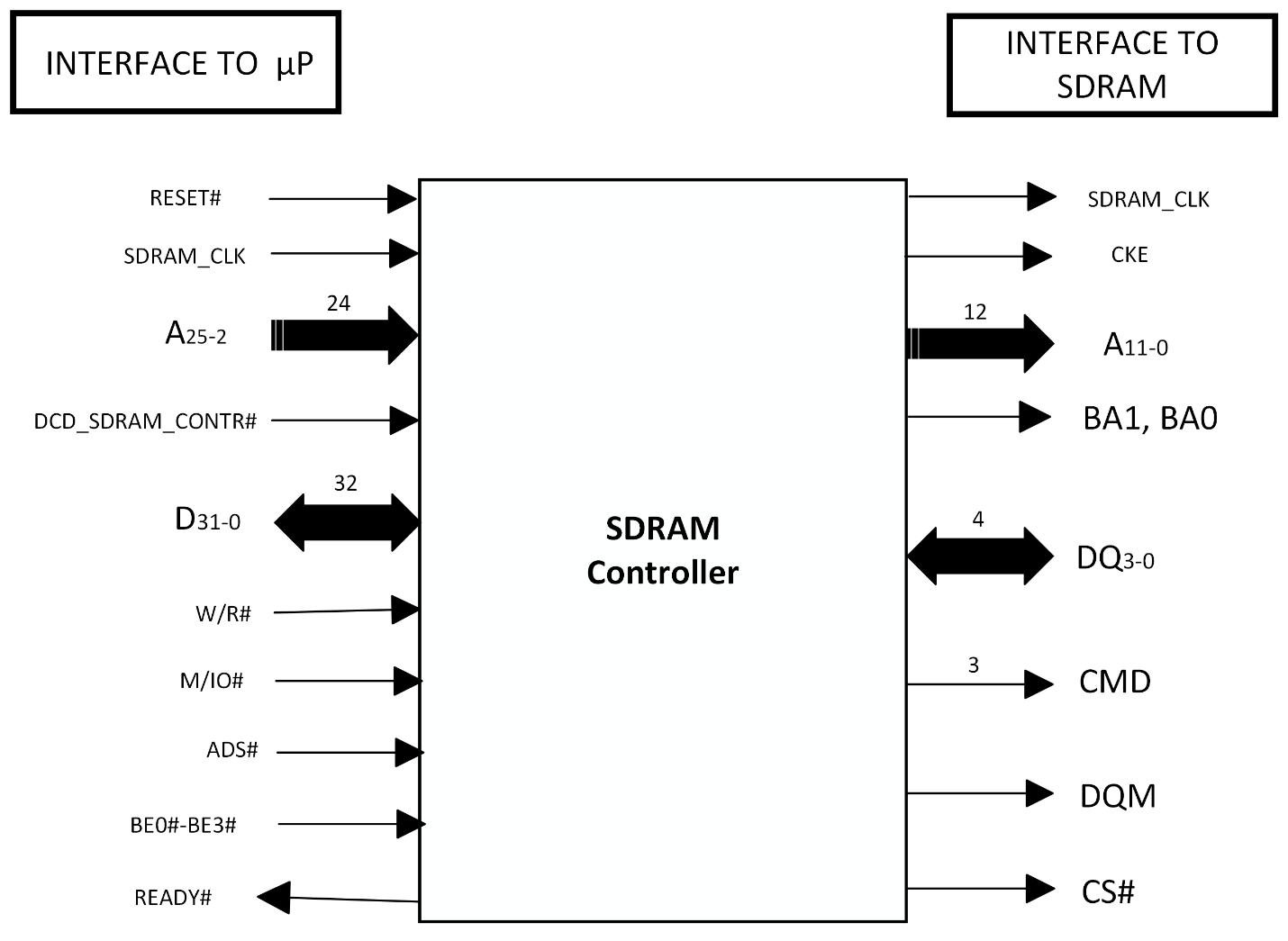
e.g: No.of Clock cycles required for tRCD = (tRCD/ tCK)

=(15 ns/7.5 ns)

=2 Clock Cycles

|  |  |  |
| --- | --- | --- |
| Timing Parameter | Required time | No.of Clock Cycles |
| tRCD | 15 ns | 2 |
| tRP | 15 ns | 2 |
| tRFC | 66 ns | 9 |
| Power\_up\_wait | 100 µs | 13333 |
| Refresh\_Req\_Rate | 15.625 µs | 2083 |

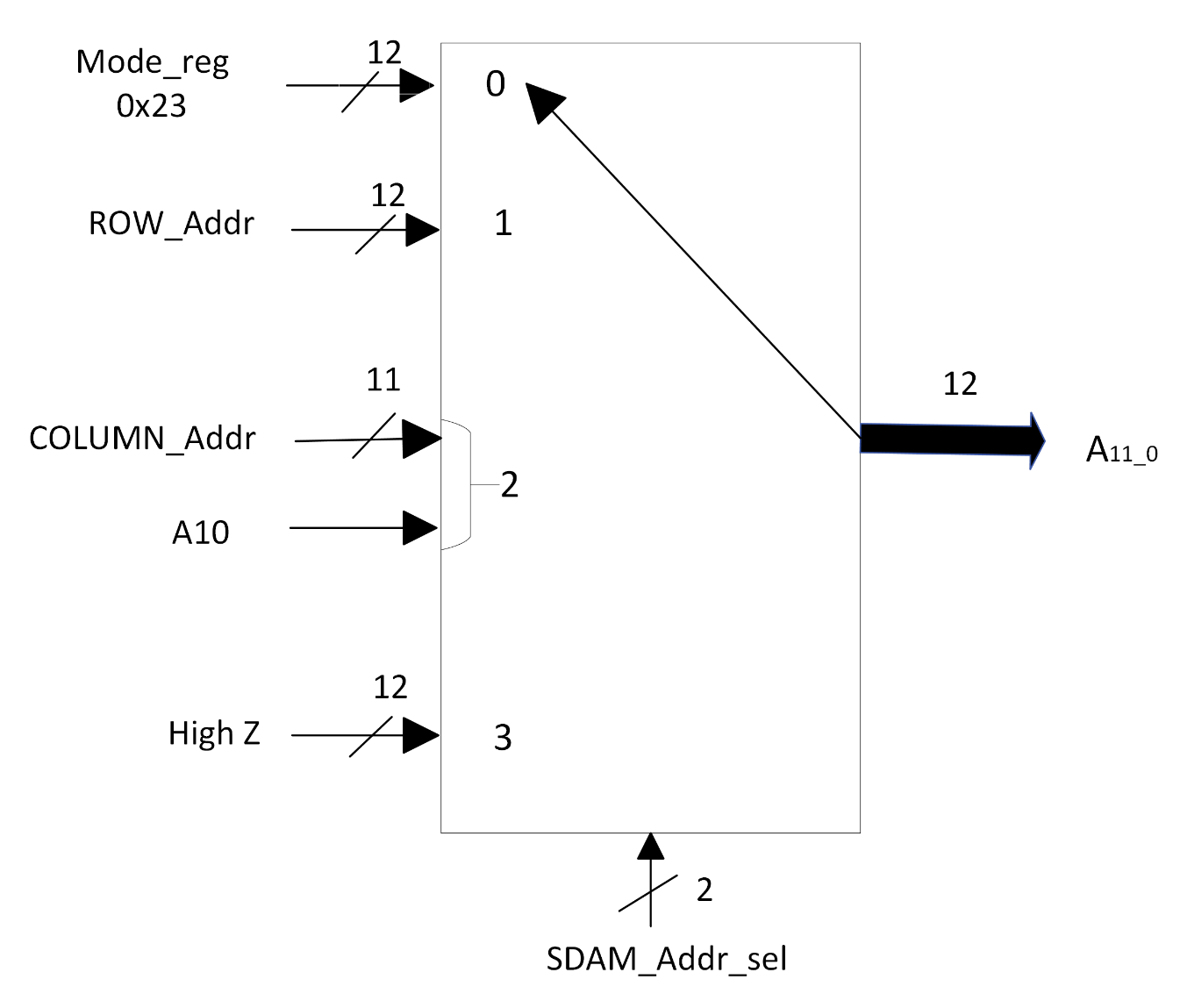
**SDRAM\_CONTROLLER INTERFACE:**



Decoder Logic:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Decoder Bits | Bank Enable Bits | Row Address Bits | Column Address Bits | Byte Enable Bits |
| A31-A26 | A25-A24 | A23-A12 | A11-A2 | A1-A0 |

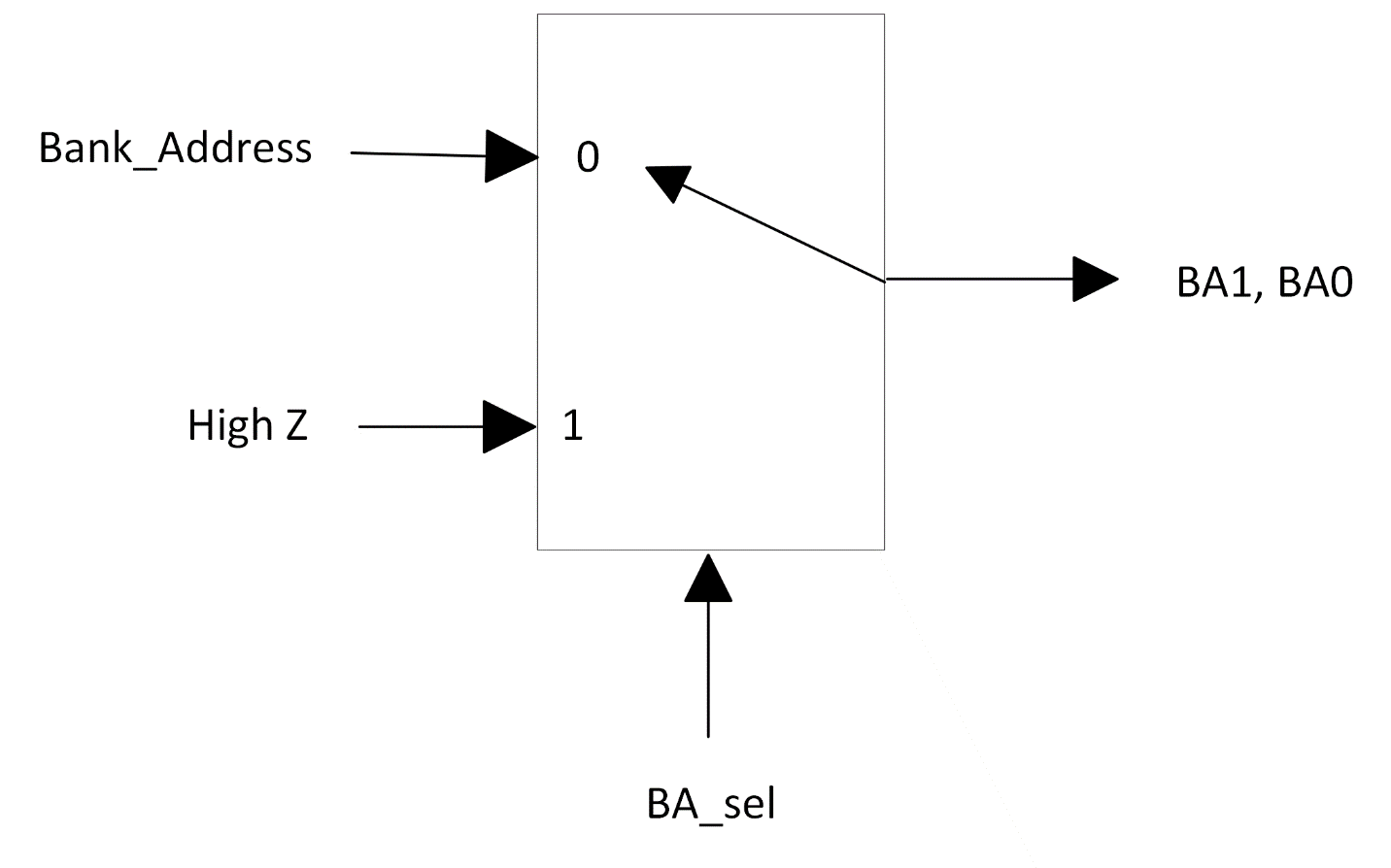
1. Decoder Bits : 6
2. Row Address Bits : 12
3. Column Address Bits : 10
4. Bank Enable bits : 2

SCEMATICS:

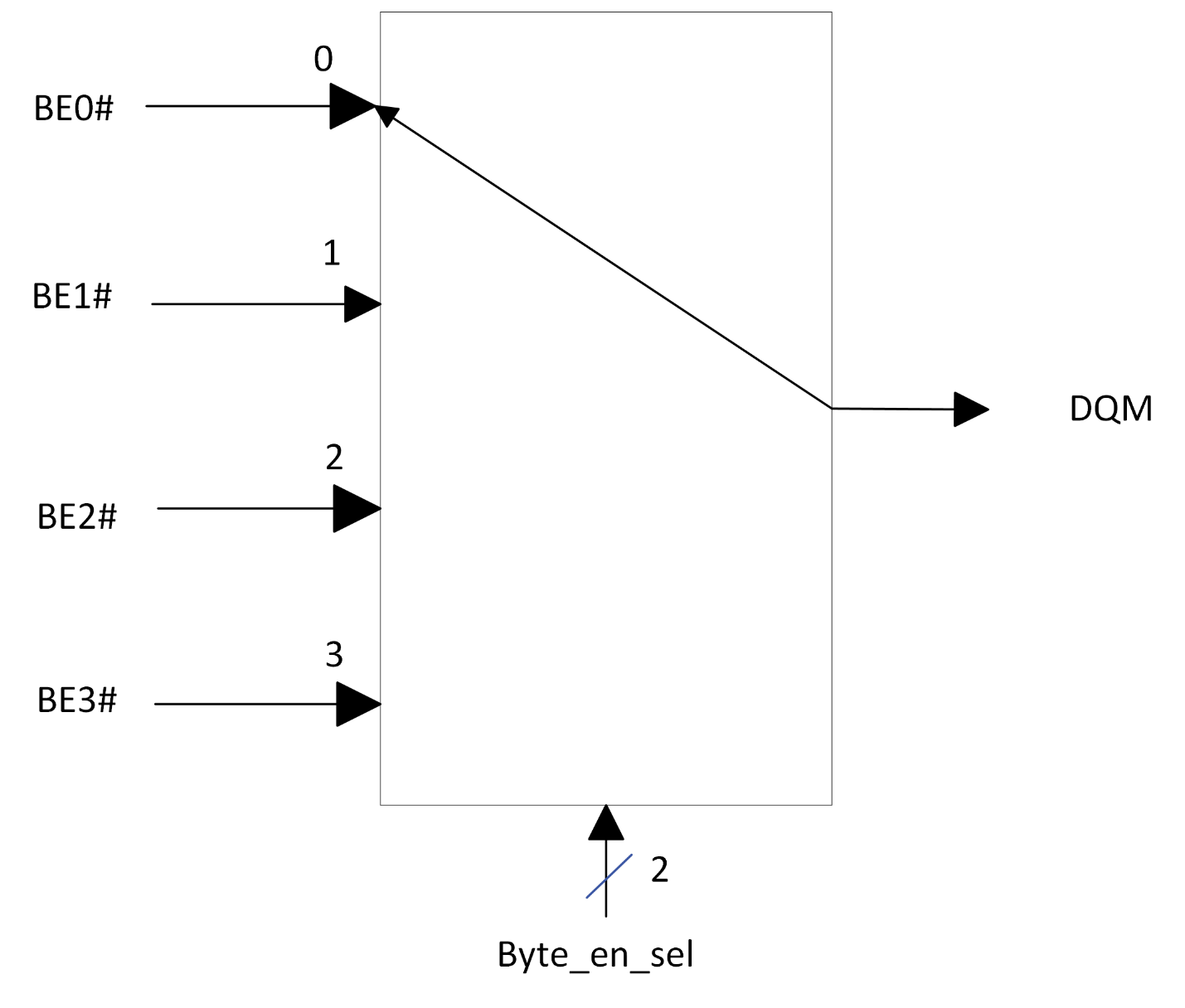
ADDRESS LINES CIRCUIT

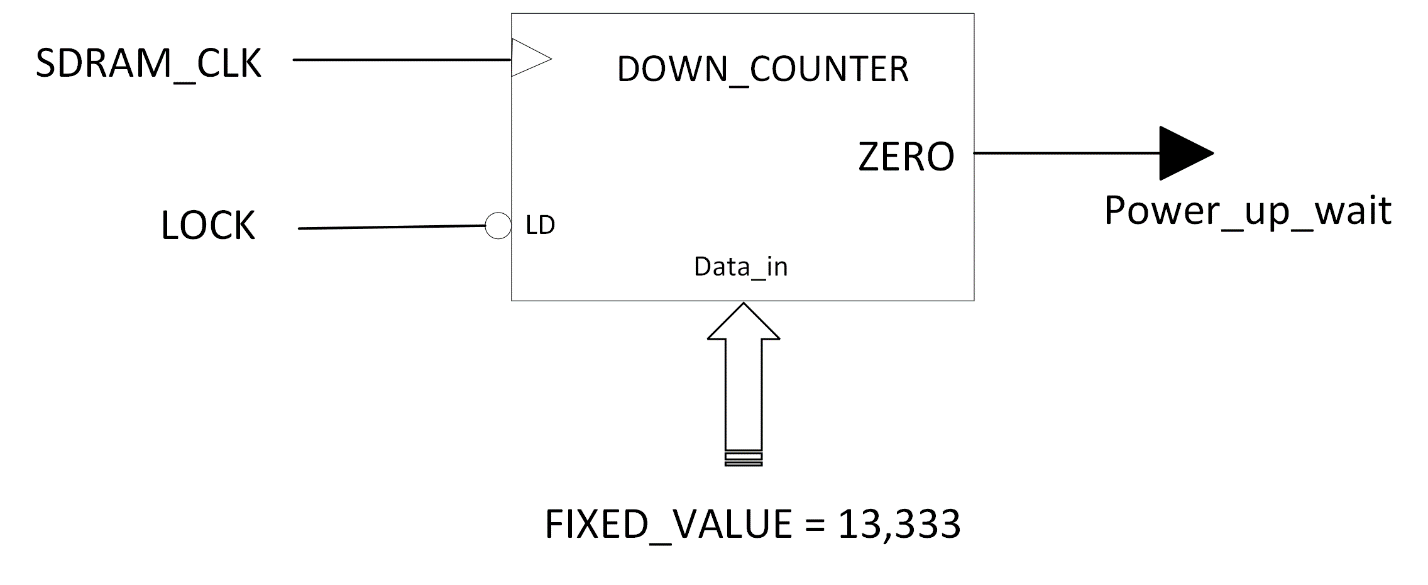
|  |  |  |
| --- | --- | --- |
| **Signal** | **Value** | **Condition** |
| Mode\_reg | 0X23 | State = send\_LMR |
| ROW\_Addr | A23-A12 | State = Active\_WRITE|Active\_READ |
| COLUMN\_Addr | {2’b00, A11-A2} | State=WRITE\_w\_D0\_3|READ |
| A10 | ‘1’ when Enable AUTO PRECHARGE else ‘0’ | State = WRITE|READ |

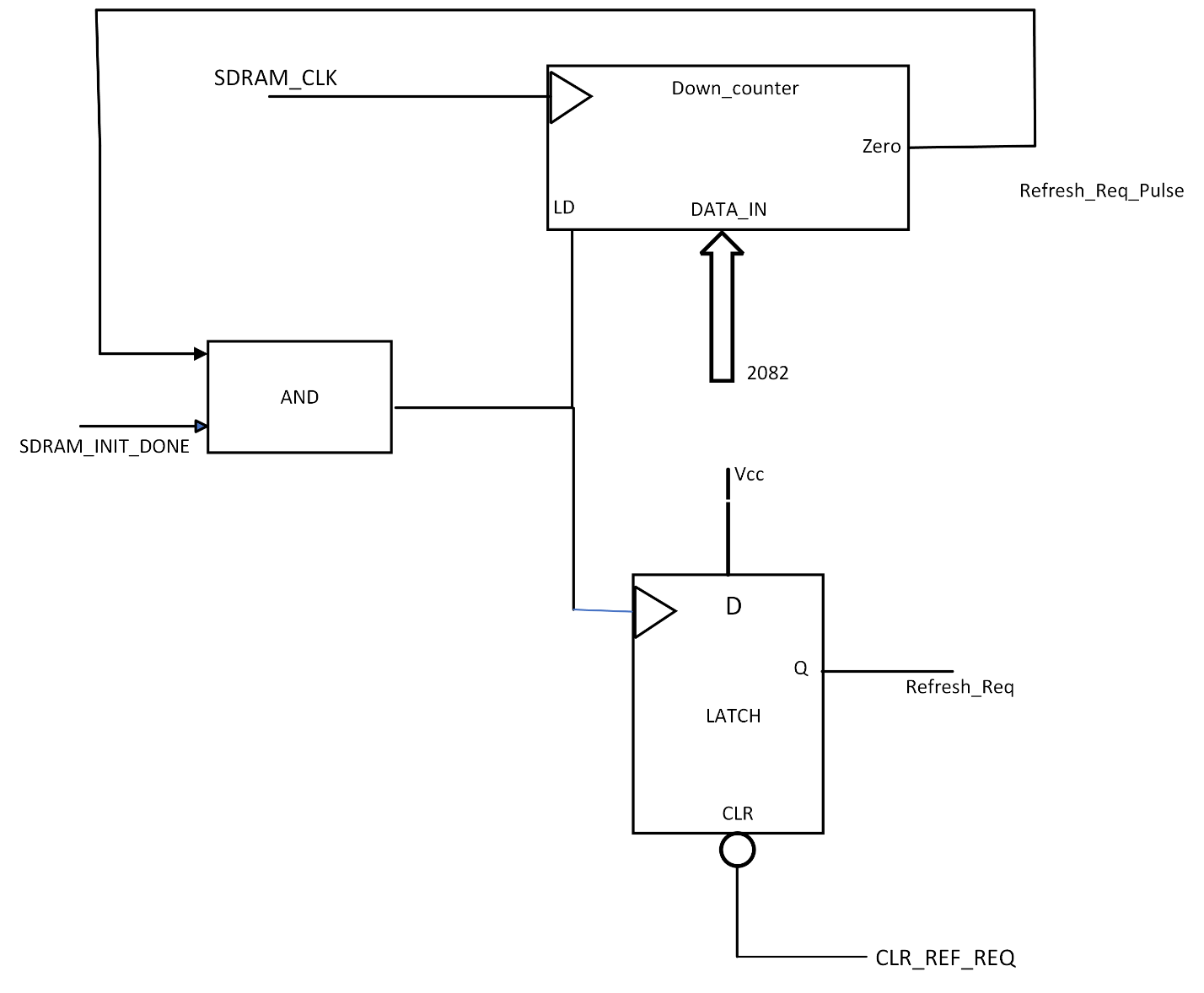
|  |  |  |
| --- | --- | --- |
| **Signal** | **Value** | **Condition** |
| SDRAM\_Addr\_sel | 2’b00 | State = send\_LMR |
|  | 2’b01 | State = Active\_WRITE|Active\_READ |
|  | 2’b10 | State=WRITE|READ |
|  | 2’b11 | State = High Z |

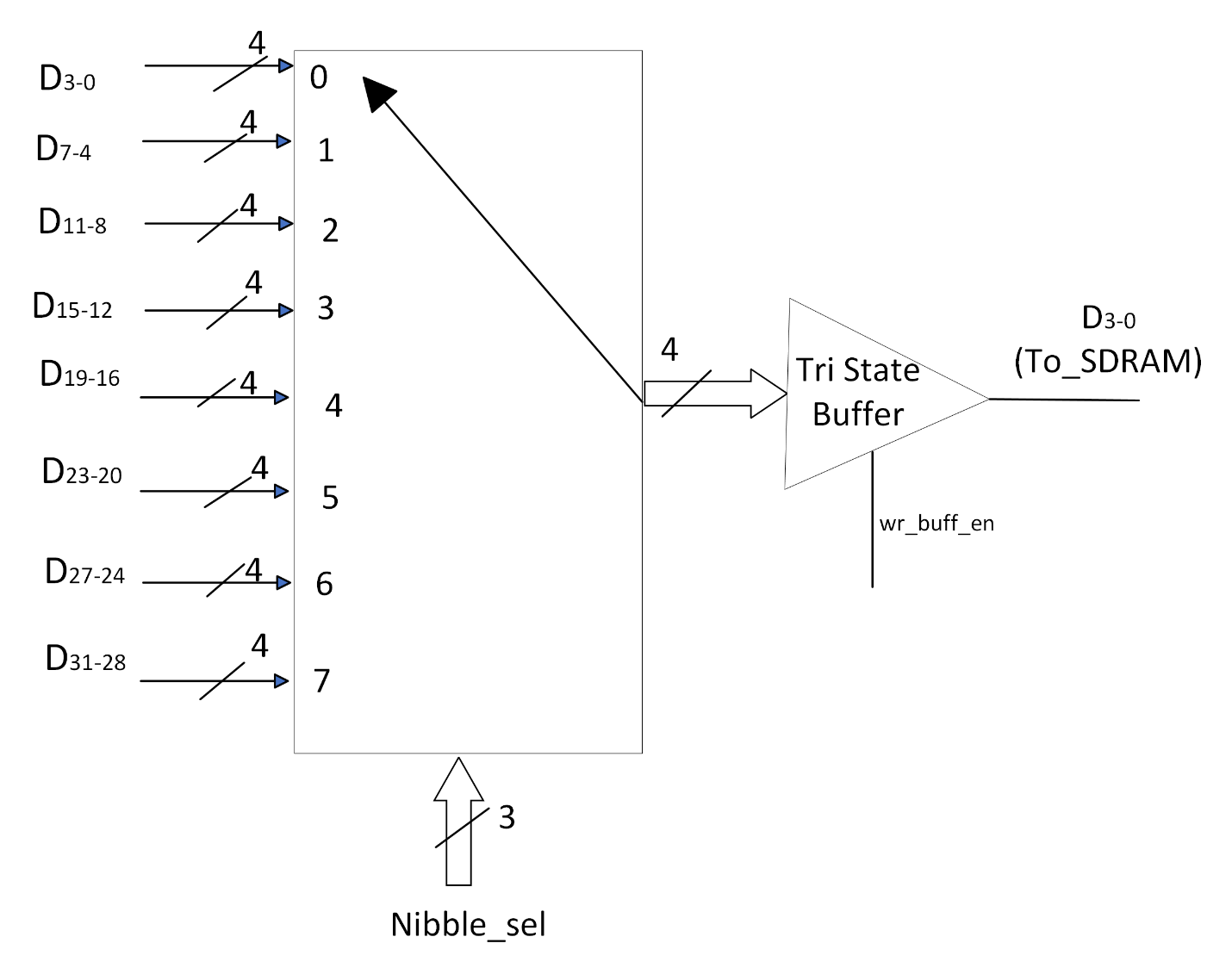


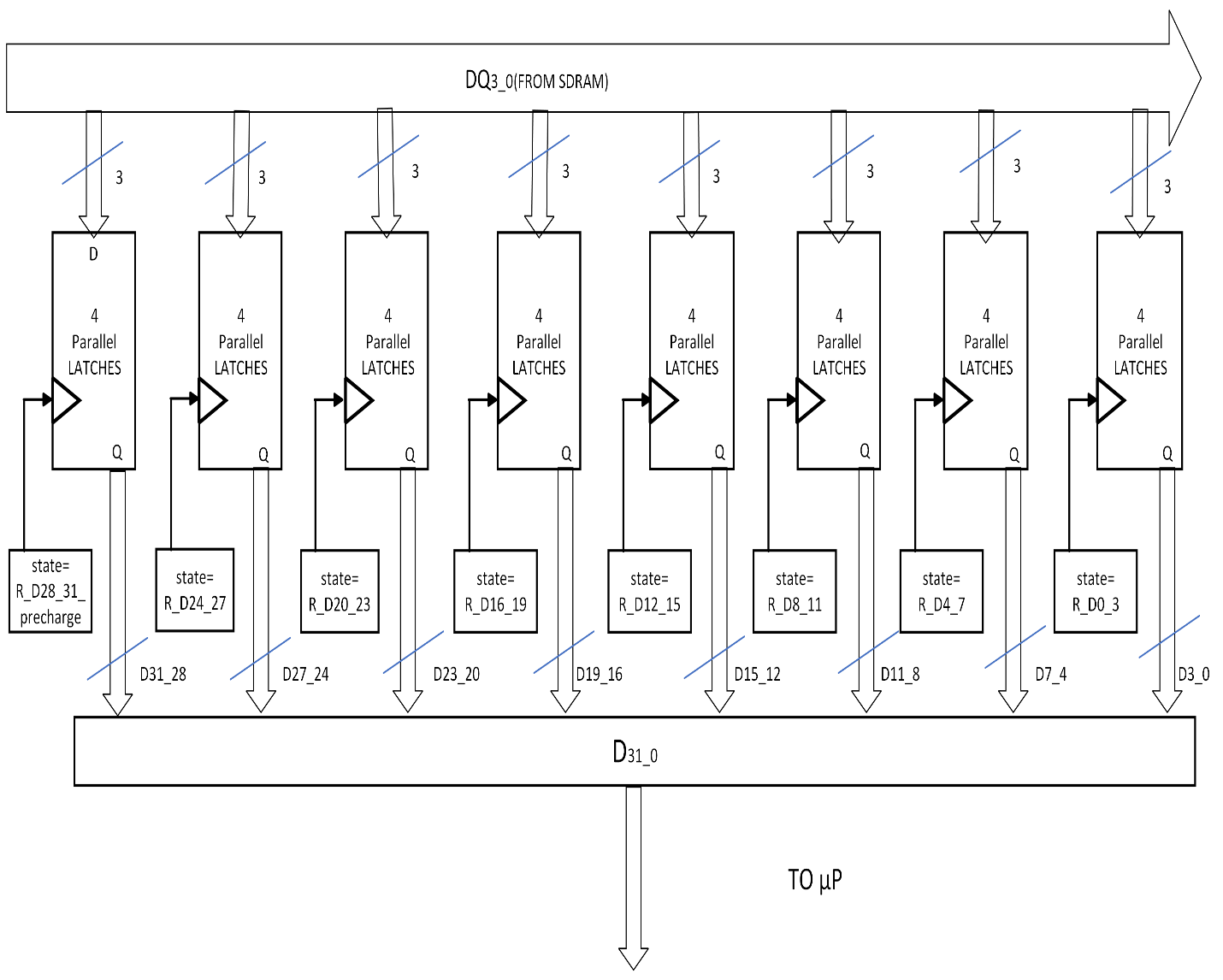
|  |  |  |
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| **Signal** | **Value** | **Condition** |
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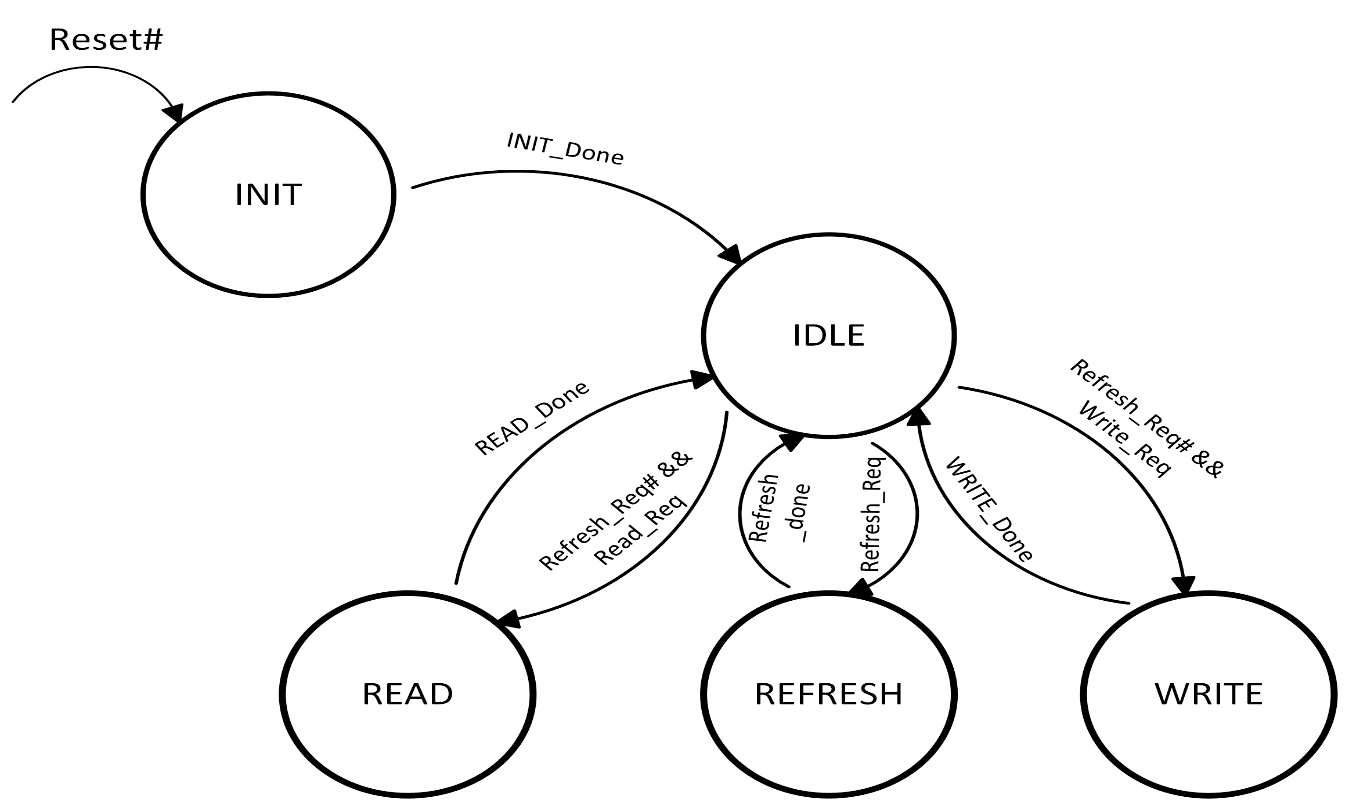








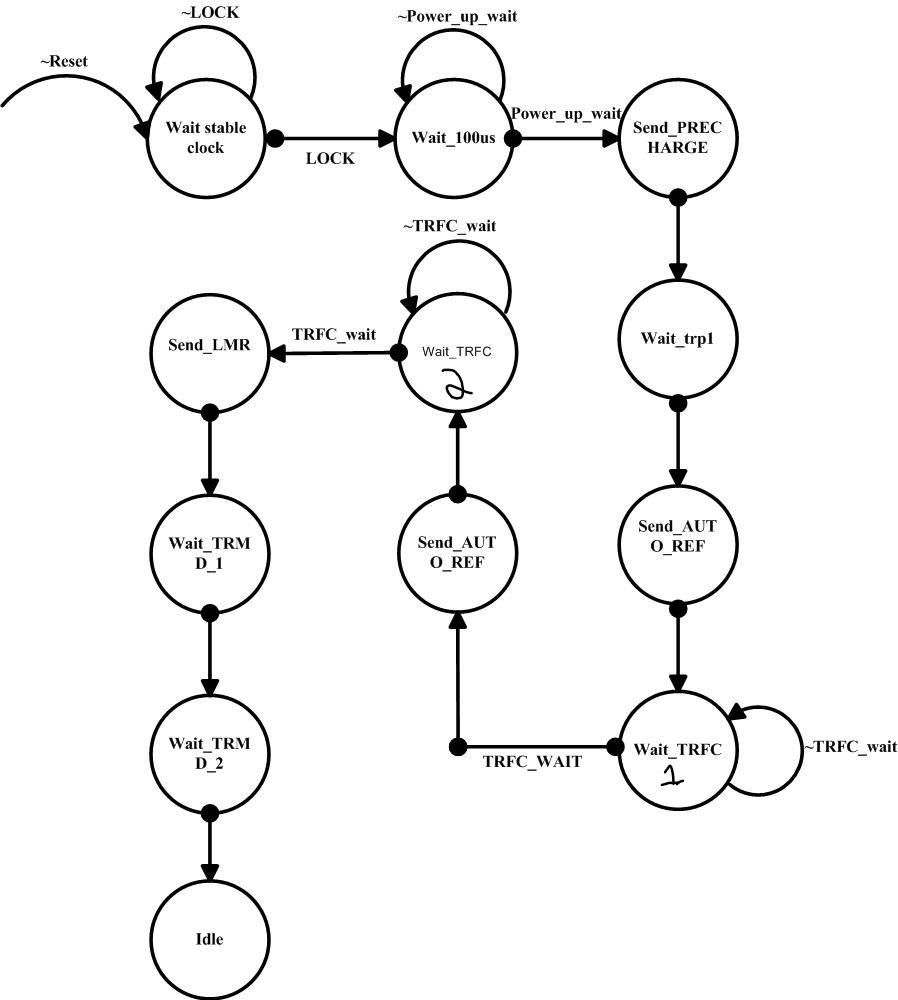
SDRAM\_Controller Top-Level FSM:



**STATE TRANSITION TABLE:**

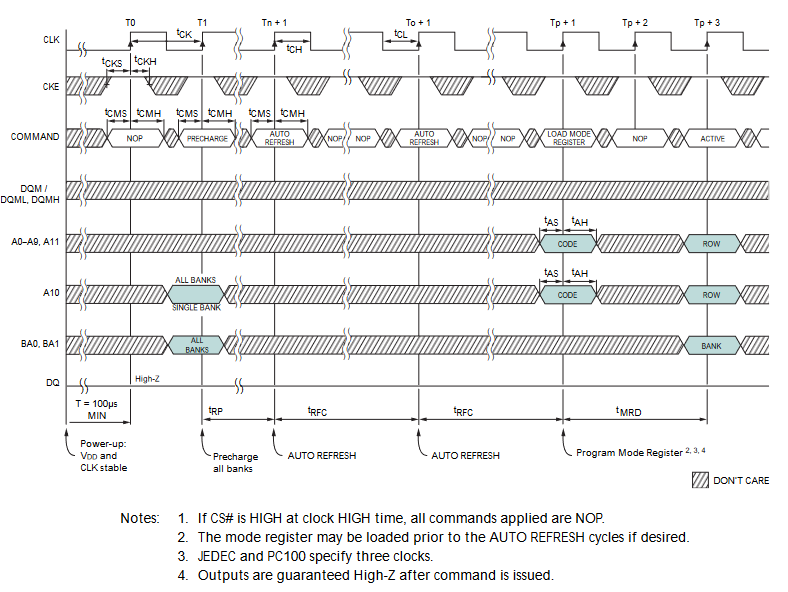
|  |  |  |
| --- | --- | --- |
| **Current State** | **Condition** | **Next\_State** |
| INIT | INIT\_Done | IDLE |
| IDLE | Refresh\_Req#&&Read\_Req | READ |
| READ | READ\_Done | IDLE |
| IDLE | Refresh\_Req | REFRESH |
| REFRESH | Refresh\_Done | IDLE |
| IDLE | Refresh\_Req#&&Write\_Req | WRITE |
| WRITE | WRITE\_Done | IDLE |

**INIT\_FSM:**

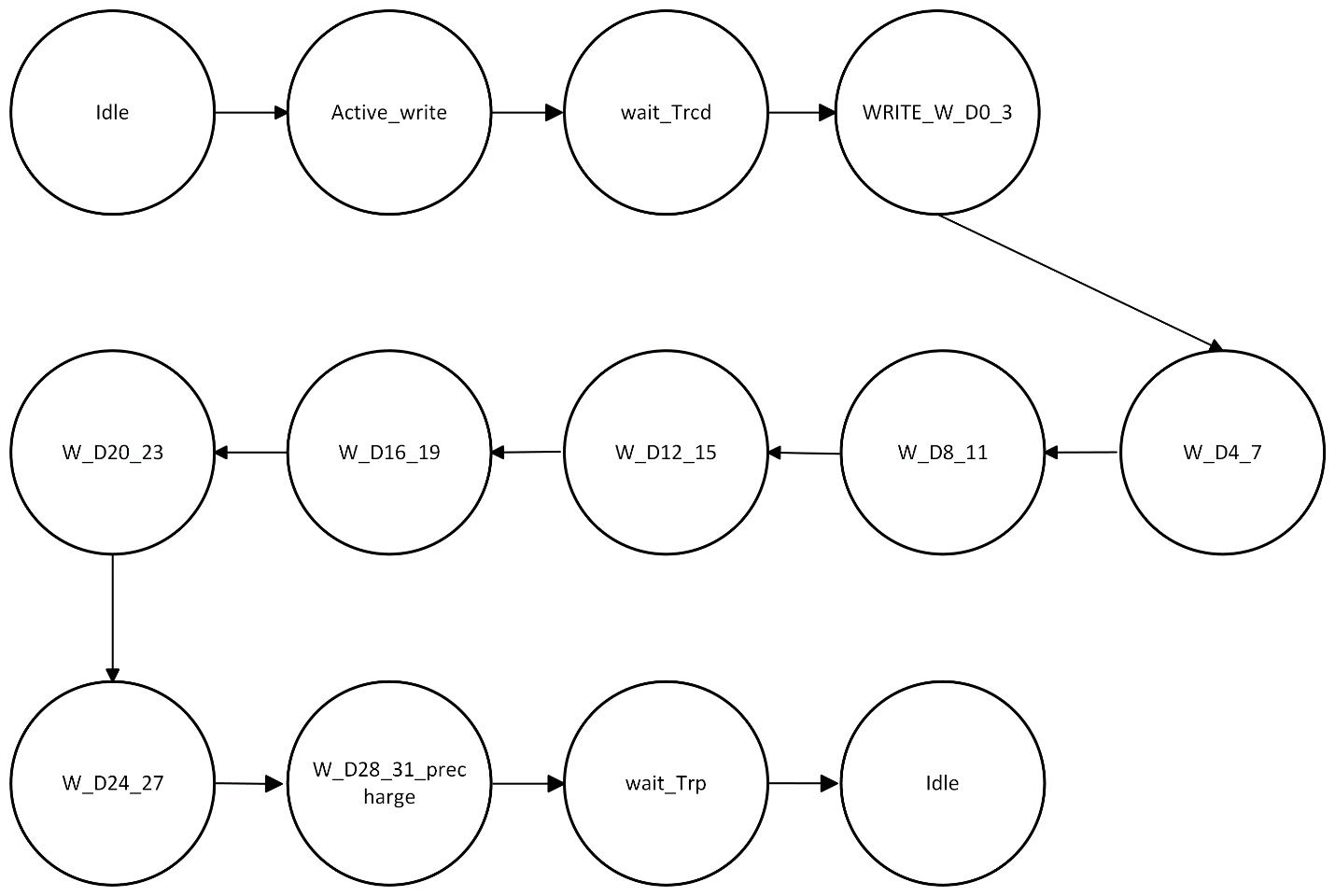


**State Transition Table :**

|  |  |  |
| --- | --- | --- |
| **Current State** | **Condition** | **Next\_State** |
| Wait\_stable\_clock | LOCK | Wait\_100µs |
| Wait\_100µs | Power\_up\_wait | Send\_PRECHARGE |
| Send\_PRECHARGE | X | Wait\_trp1 |
| Wait\_trp1 | X | Send\_AUTO\_REF |
| Wait\_TRFC1 | TRFC\_WAIT | Send\_AUTO\_REF |
| Wait\_TRFC1 | ~TRFC\_WAIT | Wait\_TRFC1 |
| Wait\_TRFC2 | TRFC\_WAIT | Send\_LMR |
| Wait\_TRFC2 | ~TRFC\_WAIT | Wait\_TRFC2 |
| Send\_LMR | X | Wait\_TRMD\_1 |
| Wait\_TRMD\_1 | X | Wait\_TRMD\_2 |
| Wait\_TRMD\_2 | X | IDLE |

**EQUATIONS for SDRAM\_CONTROLLER outputs :**

|  |  |  |
| --- | --- | --- |
| **Port** | **Value** | **Condition** |
| CKE | H | State != wait\_stable\_clock |
| CS# | L | State != wait\_stable\_clock |
| RAS# | L | State = send\_PRECHARGE|send\_AUTO\_REF|send\_LMR |
| CAS# | L | State = send\_AUTO\_REF|send\_LMR |
| WE# | L | State = send\_PRECHARGE|send\_LMR |
| A11-A0 | LMR value | State = send\_LMR |
| BA1-BA0 | Bank selection value | Sate = send\_PRECHARGE |
| DQS | HIGH Z | INIT\_DONE = 0 |
| DQM | HIGH Z | INIT\_DONE = 0 |

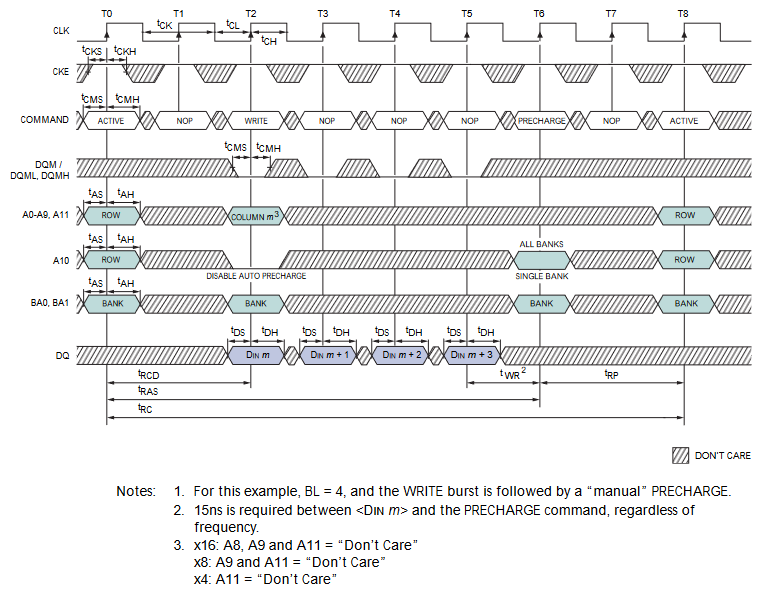
WRITE\_FSM:

State Transition Table :

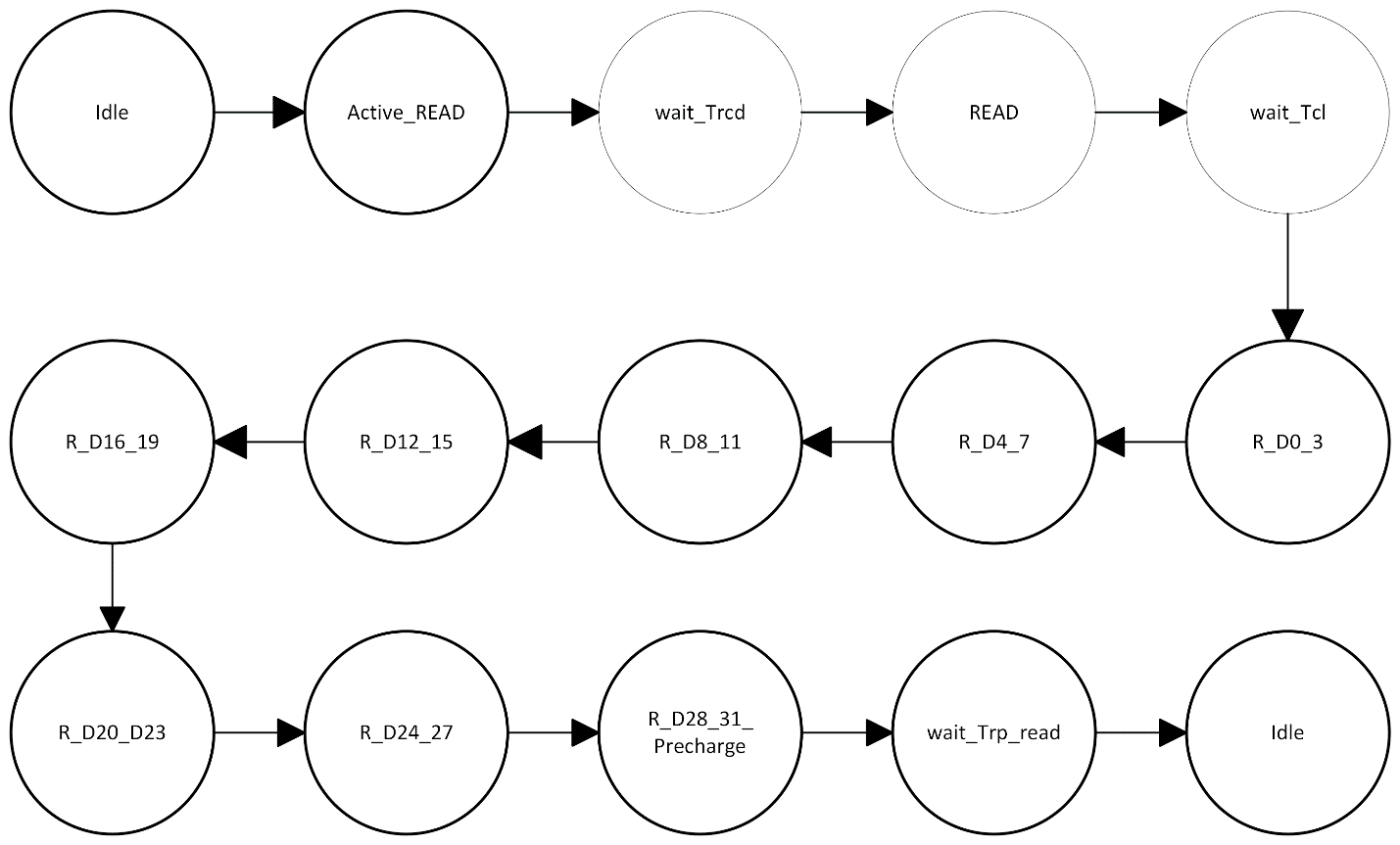
|  |  |  |
| --- | --- | --- |
| **Current State** | **Condition** | **Next State** |
| IDLE | X | ACTIVE\_WRITE |
| ACTIVE\_WRITE | X | Wait\_tRCD |
| Wait\_tRCD | X | WRITE\_W\_D0\_3 |
| WRITE\_W\_D0\_3 | X | W\_D4\_7 |
| W\_D4\_7 | X | W\_D8\_11 |
| W\_D8\_11 | X | W\_D12\_15 |
| W\_D12\_15 | X | W\_D16\_19 |
| W\_D16\_19 | X | W\_D20\_23 |
| W\_D20\_23 | X | W\_D24\_27 |
| W\_D24\_27 | X | W\_D28\_31\_PRECHARGE |
| W\_D28\_31\_PRECHARGE | X | Wait\_TRP |
| Wait\_TRP | X | IDLE |

**EQUATIONS FOR SDRAM CONTROLLER OUTPUTS:**

|  |  |  |
| --- | --- | --- |
| **Port** | **Value** | **Condition** |
| CKE | H | (State != wait\_stable\_clock)&&DCD\_SDRAM\_CONTR#=0 |
| CS# | L | (State != wait\_stable\_clock)&&DCD\_SDRAM\_CONTR#=0 |
| RAS# | L | State = Active\_WRITE| W\_D28\_31\_PRECHARGE |
| CAS# | L | State = WRITE\_W\_D0\_3 |
| WE# | L | State = W\_D28\_31\_PRECHARGE|WRITE\_W\_D0\_3 |
| A9-A0,A11 | ROW\_Address | State = Active\_WRITE |
| A9-A0,A11 | COL\_Address | State = WRITE |
| A10 | ROW\_Address | State = Active\_WRITE |
| A10 | EN\_AUTO\_PRECHARGE | State=WRITE |
| BA1-BA0 | Bank selection value | Sate = ACTIVE\_WRITE| WRITE\_W\_D0\_3|  W\_D28\_31\_PRECHARGE |
| DQS | DATA | Sate = WRITE\_W\_D0\_3|W\_D4\_7\_W\_D8\_11|W\_D12\_15|  W\_D16\_19|W\_D20\_23|W\_D24\_27|W\_D28\_31\_precharge |
| DQM | DQM\_value | Sate = WRITE\_W\_D0\_3|W\_D4\_7\_W\_D8\_11|W\_D12\_15|  W\_D16\_19|W\_D20\_23|W\_D24\_27|W\_D28\_31\_precharge |



**READ\_FSM:**

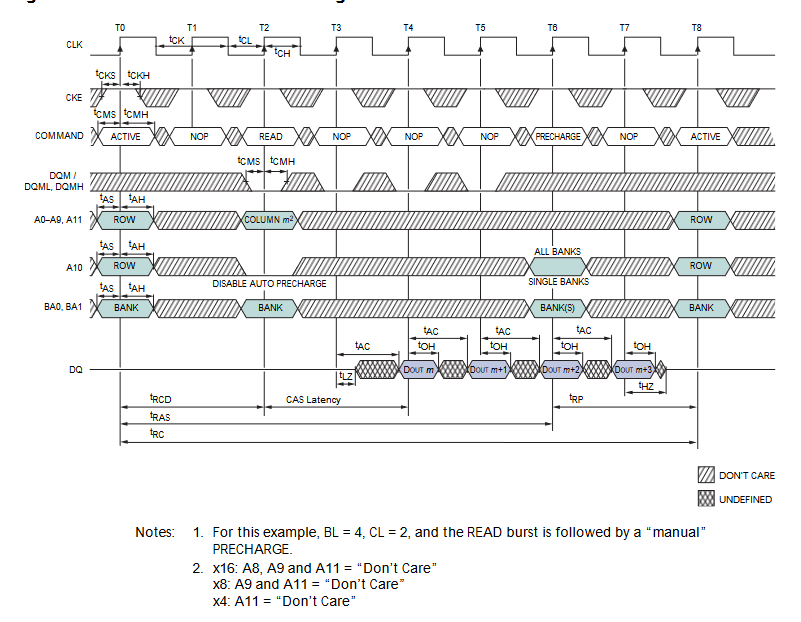


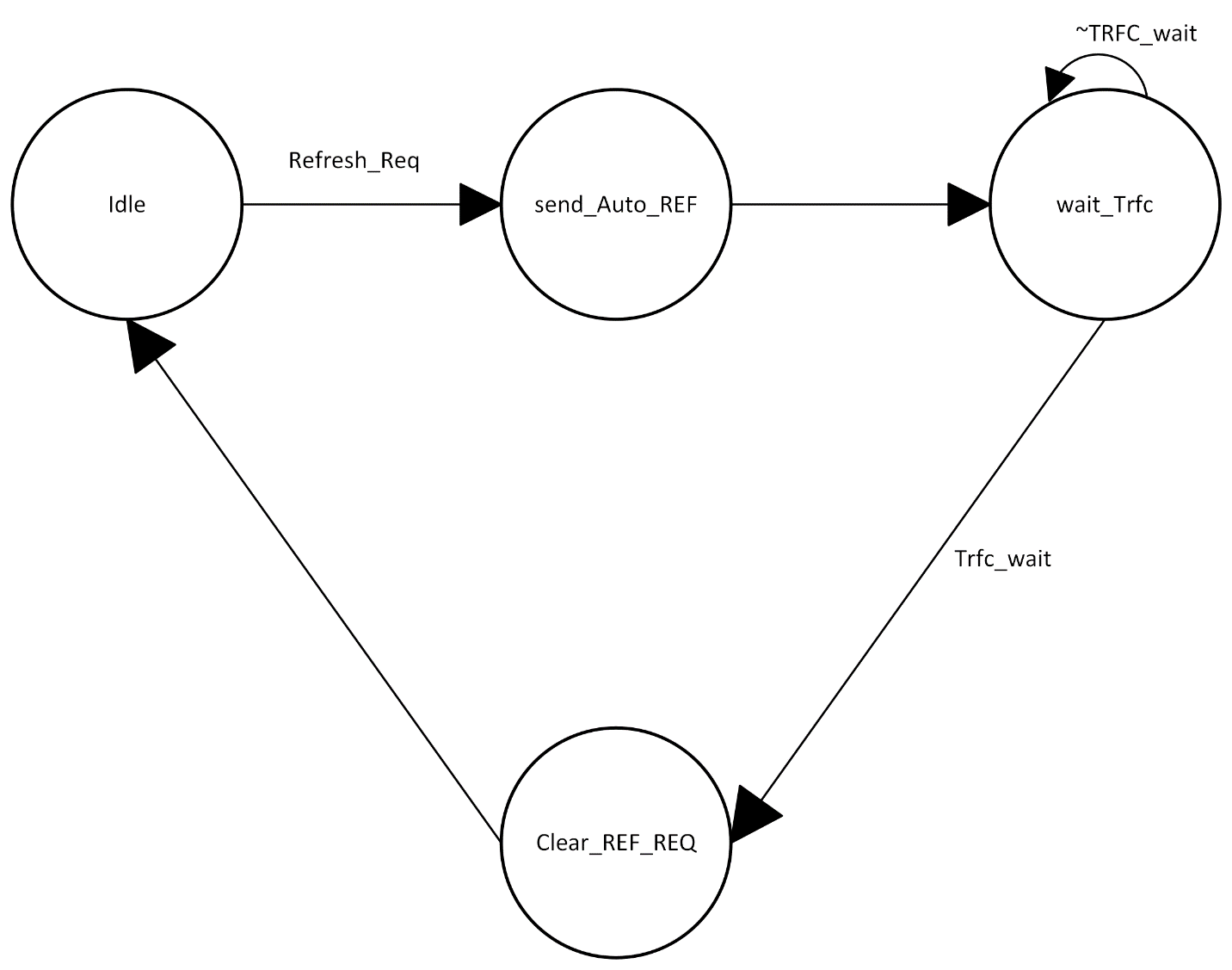
**State Transition Table :**

|  |  |  |
| --- | --- | --- |
| **Current State** | **Condition** | **Next State** |
| IDLE | X | ACTIVE\_WRITE |
| ACTIVE\_READ | X | Wait\_tRCD |
| Wait\_tRCD | X | READ |
| READ | X | Wait\_TCL |
| Wait\_TCL | X | R\_D0\_3 |
| R\_D0\_3 | X | R\_D4\_7 |
| R\_D4\_7 | X | R\_D8\_11 |
| R\_D8\_11 | X | R\_D12\_15 |
| R\_D12\_15 | X | R\_D16\_19 |
| R\_D16\_19 | X | R\_D20\_23 |
| R\_D20\_23 | X | R\_D24\_27 |
| R\_D24\_27 | X | R\_D28\_31\_PRECHARGE |
| R\_D28\_31\_PRECHARGE | X | Wait\_Trp\_read |
| Wait\_Trp\_read | X | IDLE |

**EQUATIONS FOR SDRAM CONTROLLER OUTPUTS:**

|  |  |  |
| --- | --- | --- |
| **Port** | **Value** | **Condition** |
| CKE | H | (State != wait\_stable\_clock)&&DCD\_SDRAM\_CONTR#=0 |
| CS# | L | (State != wait\_stable\_clock)&&DCD\_SDRAM\_CONTR#=0 |
| RAS# | L | State = Active\_READ| R\_D28\_31\_PRECHARGE |
| CAS# | L | State = READ |
| WE# | L | State = R\_D28\_31\_PRECHARGE |
| A9-A0,A11 | ROW\_Address | State = Active\_READ |
| A9-A0,A11 | COL\_Address | State = READ |
| A10 | ROW\_Address | State = Active\_READ |
| A10 | EN\_AUTO\_PRECHARGE | State=READ |
| BA1-BA0 | Bank selection value | Sate = ACTIVE\_READ| READ|  R\_D28\_31\_PRECHARGE |
| DQS | DATA | Sate = R\_D0\_3|R\_D4\_7\_W\_D8\_11|R\_D12\_15|  R\_D16\_19|R\_D20\_23|R\_D24\_27|R\_D28\_31\_precharge |
| DQM | DQM\_value | Sate = R\_D0\_3|R\_D4\_7\_W\_D8\_11|R\_D12\_15|  R\_D16\_19|R\_D20\_23|R\_D24\_27|R\_D28\_31\_precharge |
| READY# | L | State = R\_D28\_31\_precharge| Wait\_Trp\_read |



REFRESH FSM:

**State Transition Table:**

|  |  |  |
| --- | --- | --- |
| Current State | Condition | Next State |
| IDLE | Refresh\_req | Send\_Auto\_REF |
| Wait\_Trfc | ~TRFC\_wait | Wait\_Trfc |
| Wait\_Trfc | TRFC\_wait | Clear\_REF\_REQ |
| Clear\_REF\_REQ | X | IDLE |

**EQUATIONS FOR SDRAM CONTROLLER OUTPUTS:**

|  |  |  |
| --- | --- | --- |
| **Port** | **Value** | **Condition** |
| CKE | H | (State != wait\_stable\_clock)&&DCD\_SDRAM\_CONTR#=0 |
| CS# | L | (State != wait\_stable\_clock)&&DCD\_SDRAM\_CONTR#=0 |
| RAS# | L | State = send\_Auto\_REF |
| CAS# | L | State = send\_Auto\_REF |
| CLR\_REF\_REQ | L | State = clear\_ref\_request |