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1. Cover Sheet:

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CSE 4357/5357

Advanced Digital Logic Design

Spring Semester 2022

Assignment #4 - Registered Eight x Eight Signed Multiplier

Due Date - March 21, 2022 (11:59 PM)

Submit on Canvas Assignments

2. Design Requirements:

Eight bit Signed Multiplier should be Implemeted which should accept Multiplicand and Multiplier based on InM and InQ and a reset coontrol signal to perform the multiplication as well as out signal to register output .

To implement this design, we require the below mentioned verilog modules and hardware .

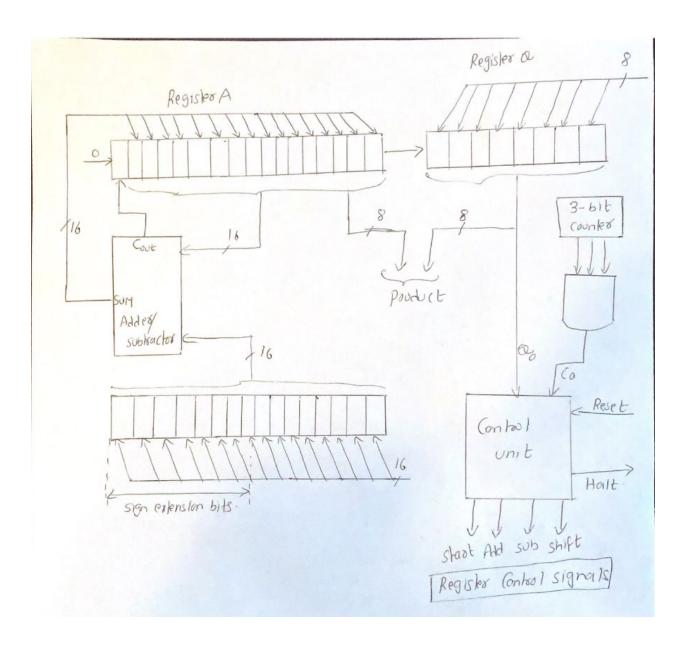
Verilog Modules:

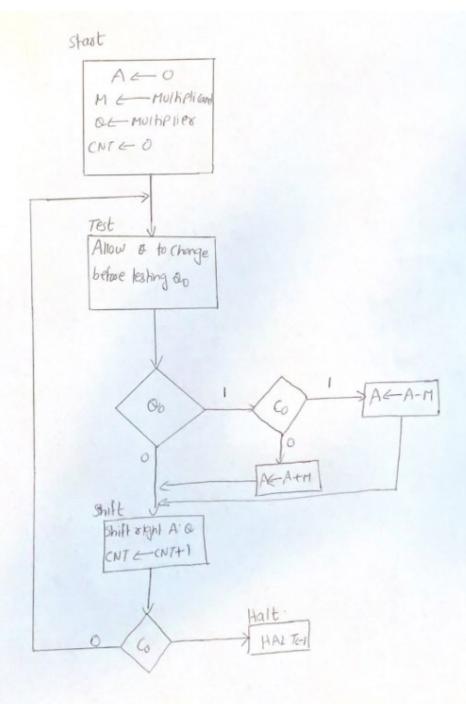
- 1. Eight_Bit_Multiplier
- 2. MultControl
- 3. Seven_segment_decoder_8_bit

Hardware:

- 1. Windows PC with Quartus Prime Lite edition
- 2. DE1-SoC board
- 3. JTAG CABLE
- 4. Power Supply

3. DATA PATH AND CONTROL PATH DIAGRAMS:





* For the last shift counter will move from "111" to "000". In the same clock cycle to also will be lested for entering into Hait state. So there will be no issue.

4. Verilog Codes:

```
//Multiplier. Verilog behavioral model.
module Eight Bit Multiplier
               input
                                       Clock
                                                                              ,//clk 50MHz
                                       Reset
                                                                              ,//pushbutton 2
               input
               input
                               [7:0]
                                       A_B_data
                                                                              ,//switch[7:0]
                                       InA
                                                                              ,//pushbutton 0
               input
               input
                                       InB
                                                                              ,//pushbutton 1
               input
                                       out
                                                                              ,//pushbutton 3
                                       Prod_nib_0
                                                                              ,//HEXO
               output
                               [0:6]
               output
                               [0:6]
                                       Prod nib 1
                                                                              ,//HEX1
               output
                               [0:6]
                                       Prod_nib_2
                                                                              ,//HEX2
                                       Prod nib 3
                                                                              ,//HEX3
               output
                               [0:6]
                                       multiplicand multiplier nib 0
                                                                              ,//HEX4
               output
                               [0:6]
                               [0:6]
                                       multiplicand multiplier nib 1
               output
                                                                              //HEX5
       );
               [7:0]
                       RegQ
                                                                               // Q register
       reg
                                                                      ;
               [16:0]
                       RegA
                                                                               // A register
        reg
               [16:0]
                       RegM
                                                                              // M register
       reg
        reg
               [2:0]
                       Count
                                                                           //3-bit iteration counter
               [15:0] Product
        reg
       wire
               CO, Start, Add, Shift, sub, sub flag
        reg [7:0] Multiplicand , Multiplier, input_disp_data
        always @(posedge Clock)
        begin
               if(lnA == 1'b0) begin
                                                       A_B_data
                       Multiplicand
                                               <=
                       input_disp_data
                                                       A_B_data
                                               <=
               end
               else if(lnB == 1'b0) begin
                       Multiplier
                                               <=
                                                       A_B_data
                       input disp data
                                                       A_B_data
                                               <=
               end
               else
               begin
                       Multiplicand
                                               <=
                                                       Multiplicand
                       Multiplier
                                                       Multiplier
                                               <=
                       input_disp_data
                                               <=
                                                       input_disp_data
               end
       end
```

```
always @(posedge Clock)
begin
       if(out == 1'b0 && Halt == 1'b1)
               Product <= {RegA[7:0],RegQ}
        else
               Product <= Product
end
// 3-bit counter for #iterations
always @(posedge Clock)
if (Start == 1)
        Count <= 3'b00
                                                    // clear in Start state
else if (Shift == 1)
       Count <= Count + 1
                                                    // increment in Shift state
assign C0 = Count[2] & Count[1] & Count[0] ; // detect count = 7
// Multiplicand register (load only)
always @(posedge Clock)
       if (Start == 1)
               RegM <= {{8{Multiplicand[7]}},Multiplicand}
// Multiplier register (load, shift)
always @(posedge Clock)
if (Start == 1)
        RegQ <= Multiplier ; // load in Start state
else if (Shift == 1)
       RegQ \le \{RegA[0], RegQ[7:1]\}; // shift in Shift state
// Accumulator register (clear, load, shift)
always @(posedge Clock)
if (Start == 1)
        RegA <=
                       16'd0
else if(sub == 1)
        RegA <=
                       RegA - RegM
                                                       //subtract sub stae
else if (Add == 1)
                                                       // load in Add state
        RegA <=
                       RegA + RegM
else if(Shift == 1)
                                                       // shift in Shift state
        RegA <=
                       RegA >> 1
```

```
// Instantiate controller module
       MultControl Ctrl
                .Clock(Clock)
                .Reset(~Reset) ,
                .Q0(RegQ[0]) ,
                .CO(CO)
                .Start(Start)
                .Add(Add)
                .sub(sub)
                .Shift(Shift)
                .Halt(Halt)
       );
       Seven_segment_decoder_8_bit Prod_nib_0_nib1
(
        .input data(Product[7:0]) ,
                                      // input [7:0] input_data_sig
        .DISP_VAL0(Prod_nib_0),
                                      // output [6:0] DISP_VALO_sig
                                      // output [6:0] DISP_VAL1_sig
        .DISP_VAL1(Prod_nib_1)
);
       Seven_segment_decoder_8_bit Prod_nib_2_nib3
        .input data(Product[15:8]),
                                      // input [7:0] input_data_sig
        .DISP_VAL0(Prod_nib_2),
                                      // output [6:0] DISP_VALO_sig
        .DISP_VAL1(Prod_nib_3)
                                      // output [6:0] DISP_VAL1_sig
);
       Seven_segment_decoder_8_bit multiplicand_multiplier_nib_0_nib1
(
        .input_data(input_disp_data)
                                                      // input [7:0] input_data_sig
        .DISP_VALO(multiplicand_multiplier_nib_0),
                                                      // output [6:0] DISP_VALO_sig
        .DISP_VAL1(multiplicand_multiplier_nib_1)
                                                      // output [6:0] DISP_VAL1_sig
);
```

endmodule

```
//Multiplier controller. Verilog behavioral model.
module MultControl
        (
                input Clock, Reset, Q0, C0,
                output Start, Add, sub, Shift, Halt
        );
        reg [5:0] state;
                               //five states (one hot –one flip-flop per state)
       //one-hot state assignments for five states
        parameter StartS=6'b000001, TestS=6'b000010, AddS=6'b000100, ShiftS=6'b001000,
                                HaltS=6'b010000,subS=6'b100000
       // State transitions on positive edge of Clock or Resets
        always @(posedge Clock, posedge Reset)
        if (Reset==1)
                state <= StartS
                                                                //enter StartS state on Reset
        else
       //change state on Clock
        case (state)
        StartS:
                state <= TestS
                                                                 // StartS to TestS
        TestS:
                if (Q0 == 1 && C0 == 1)
                                                                 //TestS to subS
                        state <= subS
                else if(Q0 == 1)
                        state <= AddS
                                                                 // TestS to AddS if Q0=1
                else
                        state <= ShiftS
                                                                 // TestS to ShiftS if Q0=0
        AddS:
                        state <= ShiftS
                                                                 // AddS to ShiftS
        subS:
                        state <= ShiftS
                                                                 // subS to ShiftS
        ShiftS:
                if (C0)
                                                                 // ShiftS to HaltS if CO=1
                        state <= HaltS
                else
                                                                 // ShiftS to TestS if C0=0
                        state <= TestS
        HaltS:
                        state <= HaltS
                                                                 // stay in HaltS
        endcase
```

```
// Moore model - activate one output per state
assign Start
                = state[0]
                                    // Start=1 in state StartS, else 0
                = state[2]
                                    // Add=1 in state AddS, else 0
assign Add
assign Shift
                = state[3]
                                    // Shift=1 in state ShiftS, else 0
                = state[4]
                                    // Halt=1 in state HaltS, else 0
assign Halt
assign sub
                = state[5]
                              ;
```

endmodule

module Seven_s (egment_decoder_	8_bit			
	input	[7:0]	input_data		,
	output reg [6:0] output reg [6:0]	DISP_VALU DISP_VAL1		,	
);					
	always @(input_ case(input_data)				
		8'h00: begin			
					DISP_VAL0 = 7'b0000001; //00 DISP_VAL1 = 7'b0000001;
		Olle Od . h t -		end	_
		8'h01: begin			DISP_VAL0 = 7'b1001111; //01
				end	DISP_VAL1 = 7'b0000001;
		8'h02: begin		ciid	
					DISP_VAL0 = 7'b0010010; //02 DISP_VAL1 = 7'b0000001;
				end	
		8'h03: begin			DISP_VAL0 = 7'b0000110; //03
				end	DISP_VAL1 = 7'b0000001;
		8'h04: begin		ciid	
					DISP_VAL0 = 7'b1001100; //04 DISP_VAL1 = 7'b0000001;
				end	
		8'h05: begin			DISP_VAL0 = 7'b0100100; //05
				end	DISP_VAL1 = 7'b0000001;
		8'h06: begin		enu	
					DISP_VAL0 = 7'b0100000; //06 DISP_VAL1 = 7'b0000001;
				end	DIST_VALT = 7 00000001,
		8'h07: begin			DISP_VAL0 = 7'b0001111; //07
					DISP_VAL1 = 7'b0000001;
		8'h08: begin		end	
					DISP_VAL0 = 7'b0000000; //08 DISP_VAL1 = 7'b0000001;
				end	
		8'h09: begin			DISP_VAL0 = 7'b0001100; //09
				end	DISP_VAL1 = 7'b0000001;
		8'h0A: begin		ciid	
					DISP_VAL0 = 7'b0001000; //0A DISP_VAL1 = 7'b0000001;
				end	
		8'h0B: begin			DISP_VAL0 = 7'b1100000; //0B
				end	DISP_VAL1 = 7'b0000001;
		8'h0C: begin			DISP_VAL0 = 7'b0110001; //0C
					DISP_VAL1 = 7'b0000001;
		8'h0D: begin		end	
		-			DISP_VAL0 = 7'b1000010; //0D DISP_VAL1 = 7'b0000001;
				end	DISI_VALI = 7 00000001,
		8'h0E: begin			DISP_VAL0 = 7'b0110000; //0E
					DISP_VAL1 = 7'b0000001;
		8'h0F: begin		end	
		-			DISP_VAL0 = 7'b0111000; //0F DISP_VAL1 = 7'b0000001;
				end	5.5VALT = / 50000001,
		8'h10: begin			
					DISP_VAL0 = 7'b0000001; //10
				end	DISP_VAL1 = 7'b1001111;
		8'h11: begin			DISP_VAL0 = 7'b1001111; //11
					DISP_VAL1 = 7'b1001111; //11
		8'h12: begin		end	
					DISP_VAL0 = 7'b0010010; //12
				end	DISP_VAL1 = 7'b1001111;
		8'h13: begin			DISP VAL0 = 7'b0000110; //13
					DISP_VAL1 = 7'b1001111;
		8'h14: begin		end	
		-			DISP_VAL0 = 7'b1001100; //14 DISP_VAL1 = 7'b1001111;
				end	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
		8'h15: begin			DISP_VAL0 = 7'b0100100; //15
				and	DISP_VAL1 = 7'b1001111;
		8'h16: begin		end	
					DISP_VAL0 = 7'b0100000; //16 DISP_VAL1 = 7'b1001111;
		011-47-7		end	
		8'h17: begin			DISP_VAL0 = 7'b0001111; //17
					DISP_VAL1 = 7'b1001111;

8'h18: begin	end	
	end	DISP_VAL0 = 7'b0000000; //18 DISP_VAL1 = 7'b1001111;
8'h19: begin		DISP_VAL0 = 7'b0001100; //19 DISP_VAL1 = 7'b1001111;
8'h1A: begin	end	DISP_VAL0 = 7'b0001000; //1A DISP_VAL1 = 7'b1001111;
8'h1B: begin	end	DISP_VAL0 = 7'b1100000; //1B
8'h1C: begin	end	DISP_VAL1 = 7'b1001111;
9/h4D, hagis	end	DISP_VAL0 = 7'b0110001; //1C DISP_VAL1 = 7'b1001111;
8'h1D: begin	end	DISP_VAL0 = 7'b1000010; //1D DISP_VAL1 = 7'b1001111;
8'h1E: begin		DISP_VAL0 = 7'b0110000; //1E DISP_VAL1 = 7'b1001111;
8'h1F: begin	end	DISP_VAL0 = 7'b0111000; //1F
8'h20: begin	end	DISP_VAL1 = 7'b1001111;
o nzu. begin	DISP_VAL1 = 7'bi	DISP_VAL0 = 7'b0000001; //20 0010010;
8'h21: begin	DISP_VAL1 = 7'bi	DISP_VAL0 = 7'b1001111; //21 0010010;
8'h22: begin	end DISP_VAL1 = 7'bl	DISP_VAL0 = 7'b0010010; //22
8'h23: begin	end	DISP_VAL0 = 7'b0000110; //23
8'h24: begin	DISP_VAL1 = 7'bi end	0010010;
Photo herin	DISP_VAL1 = 7'bi end	DISP_VAL0 = 7'b1001100; //24 0010010;
8'h25: begin	DISP_VAL1 = 7'bi	DISP_VAL0 = 7'b0100100; //25 0010010;
8'h26: begin	DISP_VAL1 = 7'bi	DISP_VAL0 = 7'b0100000; //26 0010010;
8'h27: begin	end DISP_VAL1 = 7'bl	DISP_VAL0 = 7'b0001111; //27
8'h28: begin	end	DISP_VAL0 = 7'b0000000; //28
8'h29: begin	DISP_VAL1 = 7'bi end	
8'h2A: begin	DISP_VAL1 = 7'bi end	DISP_VAL0 = 7'b0001100; //29 0010010;
	DISP_VAL1 = 7'bi	DISP_VAL0 = 7'b0001000; //2A 0010010;
8'h2B: begin	DISP_VAL1 = 7'bi	DISP_VAL0 = 7'b1100000; //2B 0010010;
8'h2C: begin	DISP VAL1 = 7'bi	DISP_VAL0 = 7'b0110001; //2C
8'h2D: begin	end	DISP_VAL0 = 7'b1000010; //2D
8'h2E: begin	DISP_VAL1 = 7'bi end	0010010; DISP_VAL0 = 7'b0110000; //2E
8'h2F: begin	DISP_VAL1 = 7'bl end	0010010;
	DISP_VAL1 = 7'bi	DISP_VAL0 = 7'b0111000; //2F 0010010;
8'h30: begin	DISP_VAL1 = 7'bi	DISP_VAL0 = 7'b0000001; //30
8'h31: begin	end	DISP_VAL0 = 7'b1001111; //31
	DISP_VAL1 = 7'bi	

end 8'h32: begin DISP_VAL0 = 7'b0010010; //32 DISP_VAL1 = 7'b0000110; 8'h33: begin DISP_VAL0 = 7'b0000110; //33 DISP_VAL1 = 7'b0000110; end DISP_VAL0 = 7'b1001100; //34
DISP_VAL1 = 7'b0000110;
end 8'h34: begin 8'h35: begin DISP_VAL0 = 7'b0100100; //35 DISP_VAL1 = 7'b0000110; 8'h36: begin DISP_VAL0 = 7'b0100000; //36 DISP_VAL1 = 7'b0000110; DISP_VAL0 = 7'b0001111; //37 DISP_VAL1 = 7'b0000110; end 8'h37: begin 8'h38: begin DISP_VAL0 = 7'b0000000; //38 DISP_VAL1 = 7'b0000110; end 8'h39: begin DISP_VAL0 = 7'b0001100; //39 DISP_VAL1 = 7'b0000110; 8'h3A: begin DISP_VAL0 = 7'b0001000; //3A DISP_VAL1 = 7'b0000110; DISP_VAL0 = 7'b1100000; //3B DISP_VAL1 = 7'b0000110; end 8'h3B: begin 8'h3C: begin DISP_VAL0 = 7'b0110001; //3C DISP_VAL1 = 7'b0000110; end 8'h3D: begin DISP_VAL0 = 7'b1000010; //3D DISP_VAL1 = 7'b0000110; 8'h3E: begin DISP_VAL0 = 7'b0110000; //3E DISP_VAL1 = 7'b0000110; DISP_VAL0 = 7'b0111000; //3F DISP_VAL1 = 7'b0000110; end 8'h3F: begin 8'h40: begin DISP_VAL0 = 7'b0000001; //40 DISP_VAL1 = 7'b1001100; 8'h41: begin DISP_VAL0 = 7'b1001111; //41 DISP_VAL1 = 7'b1001100; 8'h42: begin DISP_VAL0 = 7'b0010010; //42 DISP_VAL1 = 7'b1001100; end 8'h43: begin DISP_VAL0 = 7'b0000110; //43 DISP_VAL1 = 7'b1001100; end 8'h44: begin DISP_VAL0 = 7'b1001100; //44 DISP_VAL1 = 7'b1001100; 8'h45: begin DISP_VAL0 = 7'b0100100; //45 DISP_VAL1 = 7'b1001100; DISP_VAL0 = 7'b0100000; //46
DISP_VAL1 = 7'b1001100;
end 8'h46: begin
$$\label{eq:disp_val0} \begin{split} & \text{DISP_VAL0} = 7\text{'b00001111; //47} \\ & \text{DISP_VAL1} = 7\text{'b1001100;} \\ & \text{end} \end{split}$$
8'h47: begin

> DISP_VAL1 = 7'b1001100; DISP_VAL0 = 7'b1100000; //4B DISP_VAL1 = 7'b1001100;

DISP_VAL0 = 7'b0000000; //48 DISP_VAL1 = 7'b1001100;

DISP_VAL0 = 7'b0001100; //49 DISP_VAL1 = 7'b1001100;

DISP_VAL0 = 7'b0001000; //4A

8'h48: begin

8'h49: begin

8'h4A: begin

8'h4B: begin

8'h4C: begin DISP_VAL0 = 7'b0110001; //4C DISP_VAL1 = 7'b1001100; 8'h4D: begin DISP_VAL0 = 7'b1000010; //4D DISP_VAL1 = 7'b1001100; end 8'h4E: begin DISP_VAL0 = 7'b0110000; //4E DISP_VAL1 = 7'b1001100; end 8'h4F: begin DISP_VAL0 = 7'b0111000; //4F 8'h50: begin DISP_VAL0 = 7'b0000001; //50 DISP_VAL1 = 7'b0100100; DISP_VAL0 = 7'b1001111; //51 DISP_VAL1 = 7'b0100100; end 8'h51: begin 8'h52: begin DISP_VAL0 = 7'b0010010; //52 DISP_VAL1 = 7'b0100100; end 8'h53: begin DISP_VAL0 = 7'b0000110; //53 DISP_VAL1 = 7'b0100100; 8'h54: begin DISP_VAL0 = 7'b1001100; //54 DISP_VAL1 = 7'b0100100; DISP_VAL0 = 7'b0100100; //55
DISP_VAL1 = 7'b0100100; end 8'h55: begin 8'h56: begin DISP_VAL0 = 7'b0100000; //56 DISP_VAL1 = 7'b0100100; end 8'h57: begin DISP_VAL0 = 7'b0001111; //57 DISP_VAL1 = 7'b0100100; 8'h58: begin DISP_VAL0 = 7'b0000000; //58 DISP_VAL1 = 7'b0100100; DISP_VAL0 = 7'b0001100; //59 DISP_VAL1 = 7'b0100100; end 8'h59: begin DISP_VAL0 = 7'b0001000; //5A
DISP_VAL1 = 7'b0100100;
end 8'h5A: begin 8'h5B: begin DISP_VAL0 = 7'b1100000; //5B DISP_VAL1 = 7'b0100100; 8'h5C: begin DISP_VAL0 = 7'b0110001; //5C DISP_VAL1 = 7'b0100100; 8'h5D: begin DISP_VAL0 = 7'b1000010; //5D DISP_VAL1 = 7'b0100100; 8'h5E: begin DISP_VAL0 = 7'b0110000; //5E DISP_VAL1 = 7'b0100100; 8'h5F: begin DISP_VAL0 = 7'b0111000; //5F DISP_VAL1 = 7'b0100100; DISP_VAL0 = 7'b0000001; //60 DISP_VAL1 = 7'b0100000; end 8'h60: begin
$$\label{eq:disp_val0} \begin{split} & \text{DISP_VAL0} = 7\text{'b}1001111; \text{//61} \\ & \text{DISP_VAL1} = 7\text{'b}0100000; \\ & \text{end} \end{split}$$
8'h61: begin 8'h62: begin DISP_VAL0 = 7'b0010010; //62 DISP_VAL1 = 7'b0100000; 8'h63: begin DISP_VAL0 = 7'b0000110; //63 DISP_VAL1 = 7'b0100000; 8'h64: begin DISP_VAL0 = 7'b1001100; //64 DISP_VAL1 = 7'b0100000; 8'h65: begin

DISP_VAL0 = 7'b0100100; //65 DISP_VAL1 = 7'b0100000; 8'h66: begin DISP_VAL0 = 7'b0100000; //66 DISP_VAL1 = 7'b0100000; 8'h67: begin DISP_VAL0 = 7'b0001111; //67 DISP_VAL1 = 7'b0100000; end 8'h68: begin DISP_VAL0 = 7'b0000000; //68 DISP_VAL1 = 7'b0100000; end DISP_VAL0 = 7'b0001100; //69
DISP_VAL1 = 7'b0100000;
end 8'h69: begin 8'h6A: begin DISP_VAL0 = 7'b0001000; //6A DISP_VAL1 = 7'b0100000; 8'h6B: begin DISP_VAL0 = 7'b1100000; //6B DISP_VAL1 = 7'b0100000;
$$\label{eq:DISP_VALO} \begin{split} & \text{DISP_VALO} = 7'b0110001; //6C \\ & \text{DISP_VAL1} = 7'b0100000; \\ & \text{end} \end{split}$$
8'h6C: begin DISP_VAL0 = 7'b1000010; //6D DISP_VAL1 = 7'b0100000; end 8'h6D: begin 8'h6E: begin DISP_VAL0 = 7'b0110000; //6E DISP_VAL1 = 7'b0100000; 8'h6F: begin DISP_VAL0 = 7'b0111000; //6F DISP_VAL1 = 7'b0100000; 8'h70: begin DISP_VAL0 = 7'b0000001; //70 DISP_VAL1 = 7'b0001111; end 8'h71: begin DISP_VAL0 = 7'b1001111; //71
DISP_VAL1 = 7'b0001111; 8'h72: begin DISP_VAL0 = 7'b0010010; //72 DISP_VAL1 = 7'b0001111; DISP_VAL0 = 7'b0000110; //73
DISP_VAL1 = 7'b0001111;
end 8'h73: begin DISP_VAL0 = 7'b1001100; //74
DISP_VAL1 = 7'b0001111;
end 8'h74: begin 8'h75: begin DISP_VAL0 = 7'b0100100; //75 DISP_VAL1 = 7'b0001111; 8'h76: begin DISP_VAL0 = 7'b0100000; //76 DISP_VAL1 = 7'b0001111; 8'h77: begin DISP_VAL0 = 7'b0001111; //77
DISP_VAL1 = 7'b0001111; 8'h78: begin DISP_VAL0 = 7'b0000000; //78 DISP_VAL1 = 7'b0001111; 8'h79: begin DISP_VAL0 = 7'b0001100; //79
DISP_VAL1 = 7'b0001111; DISP_VAL0 = 7'b0001000; //7A
DISP_VAL1 = 7'b0001111;
end 8'h7A: begin DISP_VAL0 = 7'b1100000; //7B DISP_VAL1 = 7'b0001111; end 8'h7B: begin DISP_VAL0 = 7'b0110001; //7C DISP_VAL1 = 7'b0001111; end 8'h7C: begin 8'h7D: begin DISP_VAL0 = 7'b1000010; //7D DISP_VAL1 = 7'b0001111; 8'h7E: begin DISP_VAL0 = 7'b0110000; //7E DISP_VAL1 = 7'b0001111; 8'h7F: begin DISP_VAL0 = 7'b0111000; //7F DISP_VAL1 = 7'b0001111;

8'h80: begin		DISP_VAL0 = 7'b0000001; //80
ChC1, bosis	DISP_VAL1 end	= 7'b0000000;
8'h81: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001111; //81 = 7'b0000000;
8'h82: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0010010; //82 = 7'b0000000;
8'h83: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000110; //83 = 7'b0000000;
8'h84: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001100; //84 = 7'b0000000;
8'h85: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100100; //85 = 7'b0000000;
8'h86: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100000; //86 = 7'b0000000;
8'h87: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001111; //87 = 7'b0000000;
8'h88: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000000; //88 = 7'b0000000;
8'h89: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001100; //89 = 7'b0000000;
8'h8A: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001000; //8A = 7'b0000000;
8'h8B: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1100000; //8B = 7'b0000000;
8'h8C: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110001; //8C = 7'b0000000;
8'h8D: begin 8'h8E: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1000010; //8D = 7'b0000000;
o not. Degin	DISP_VAL1 end	DISP_VAL0 = 7'b0110000; //8E = 7'b0000000;
8'h8F: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0111000; //8F = 7'b0000000;
8'h90: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000001; //90 = 7'b0001100;
8'h91: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001111; //91 = 7'b0001100;
8'h92: begin	DISP_VAL1 end	DISP_VALO = 7'b0010010; //92 = 7'b0001100;
8'h93: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000110; //93 = 7'b0001100;
8'h94: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001100; //94 = 7'b0001100;
8'h95: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100100; //95 = 7'b0001100;
8'h96: begin		

	DISP_VAL1 end	DISP_VAL0 = 7'b0100000; //96 = 7'b0001100;
8'h97: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001111; //97 = 7'b0001100;
8'h98: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000000; //98 = 7'b0001100;
8'h99: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001100; //99 = 7'b0001100;
8'h9A: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001000; //9A = 7'b0001100;
8'h9B: begin	DISP_VAL1 end	DISP_VALO = 7'b1100000; //9B = 7'b0001100;
8'h9C: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110001; //9C = 7'b0001100;
8'h9D: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1000010; //9D = 7'b0001100;
8'h9E: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110000; //9E = 7'b0001100;
8'h9F: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0111000; //9F = 7'b0001100;
8'hA0: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000001; //A0 = 7'b0001000;
8'hA1: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001111; //A1 = 7'b0001000;
8'hA2: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0010010; //A2 = 7'b0001000;
8'hA3: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000110; //A3 = 7'b0001000;
8'hA4: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001100; //A4 = 7'b0001000;
8'hA5: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100100; //A5 = 7'b0001000;
8'hA6: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100000; //A6 = 7'b0001000;
8'hA7: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001111; //A7 = 7'b0001000;
8'hA8: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000000; //A8 = 7'b0001000;
8'hA9: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001100; //A9 = 7'b0001000;
8'hAA: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001000; //AA = 7'b0001000;
8'hAB: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1100000; //AB = 7'b0001000;
8'hAC: begin		

	DISP_VAL1 end	DISP_VAL0 = 7'b0110001; //AC = 7'b0001000;
8'hAD: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1000010; //AD = 7'b0001000;
8'hAE: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110000; //AE = 7'b0001000;
8'hAF: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0111000; //AF = 7'b0001000;
8'hB0: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000001; //B0 = 7'b1100000;
8'hB1: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001111; //B1 = 7'b1100000;
8'hB2: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0010010; //B2 = 7'b1100000;
8'hB3: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000110; //B3 = 7'b1100000;
8'hB4: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001100; //B4 = 7'b1100000;
8'hB5: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100100; //B5 = 7'b1100000;
8'hB6: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100000; //B6 = 7'b1100000;
8'hB7: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001111; //B7 = 7'b1100000;
8'hB8: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000000; //B8 = 7'b1100000;
8'hB9: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001100; //B9 = 7'b1100000;
8'hBA: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001000; //BA = 7'b1100000;
8'hBB: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1100000; //BB = 7'b1100000;
8'hBC: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110001; //BC = 7'b1100000;
8'hBD: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1000010; //BD = 7'b1100000;
	DISP_VAL1 end	DISP_VAL0 = 7'b0110000; //BE = 7'b1100000;
8'hBF: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0111000; //BF = 7'b1100000;
8'hCO: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000001; //C0 = 7'b0110001;
8'hC1: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001111; //C1 = 7'b0110001;
8'hC2: begin		DISP_VAL0 = 7'b0010010; //C2

	DISP_VAL1 end	= 7'b0110001;
8'hC3: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000110; //C3 = 7'b0110001;
8'hC4: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001100; //C4 = 7'b0110001;
8'hC5: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100100; //C5 = 7'b0110001;
8'hC6: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100000; //C6 = 7'b0110001;
8'hC7: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001111; //C7 = 7'b0110001;
8'hC8: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000000; //C8 = 7'b0110001;
8'hC9: begin	DISP_VAL1 end	DISP_VALO = 7'b0001100; //C9 = 7'b0110001;
8'hCA: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001000; //CA = 7'b0110001;
8'hCB: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1100000; //CB = 7'b0110001;
8'hCC: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110001; //CC = 7'b0110001;
8'hCD: begin	DISP_VAL1	DISP_VAL0 = 7'b1000010; //CD = 7'b0110001;
8'hCE: begin	end DISP_VAL1	DISP_VAL0 = 7'b0110000; //CE = 7'b0110001;
8'hCF: begin	end	
	DISP_VAL1 end	DISP_VALO = 7'b0111000; //CF = 7'b0110001;
8'hD0: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000001; //D0 = 7'b1000010;
8'hD1: begin 8'hD2: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001111; //D1 = 7'b1000010;
o noz. begin	DISP_VAL1 end	DISP_VAL0 = 7'b0010010; //D2 = 7'b1000010;
8'hD3: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000110; //D3 = 7'b1000010;
8'hD4: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001100; //D4 = 7'b1000010;
8'hD5: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100100; //D5 = 7'b1000010;
8'hD6: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100000; //D6 = 7'b1000010;
8'hD7: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001111; //D7 = 7'b1000010;
8'hD8: begin		DISP_VAL0 = 7'b0000000; //D8

	DISP_VAL1 end	= 7'b1000010;
8'hD9: begin		
	DISP_VAL1 end	DISP_VAL0 = 7'b0001100; //D9 = 7'b1000010;
8'hDA: begin		DISP_VAL0 = 7'b0001000; //DA = 7'b1000010;
8'hDB: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1100000; //DB = 7'b1000010;
8'hDC: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110001; //DC = 7'b1000010;
8'hDD: begin	DISP_VAL1	DISP_VAL0 = 7'b1000010; //DD = 7'b1000010;
8'hDE: begin	DISP_VAL1	DISP_VAL0 = 7'b0110000; //DE = 7'b1000010;
	enu	
8'hDF: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0111000; //DF = 7'b1000010;
8'hE0: begin	DISP_VAL1	DISP_VAL0 = 7'b0000001; //E0 = 7'b0110000;
8'hE1: begin		
8'hE2: begin		DISP_VAL0 = 7'b1001111; //E1 = 7'b0110000;
		DISP_VAL0 = 7'b0010010; //E2 = 7'b0110000;
8'hE3: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000110; //E3 = 7'b0110000;
8'hE4: begin	DISP_VAL1 end	DISP_VAL0 = 7'b1001100; //E4 = 7'b0110000;
8'hE5: begin		
8'hE6: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100100; //E5 = 7'b0110000;
		DISP_VAL0 = 7'b0100000; //E6 = 7'b0110000;
8'hE7: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001111; //E7 = 7'b0110000;
8'hE8: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0000000; //E8 = 7'b0110000;
8'hE9: begin		DISP_VALO = 7'b0001100; //E9 = 7'b0110000;
8'hEA: begin		DISP_VAL0 = 7'b0001000; //EA = 7'b0110000;
8'hEB: begin	DISP_VAL1 end	DISP_VALO = 7'b1100000; //EB = 7'b0110000;
8'hEC: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110001; //EC = 7'b0110000;
8'hED: begin	DISP_VAL1	DISP_VAL0 = 7'b1000010; //ED = 7'b0110000;
8'hEE: begin		DISP_VAL0 = 7'b0110000; //EE = 7'b0110000;

8'hEF: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0111000; //EF = 7'b0110000;
8'hF0: begin	DISP_VAL1 end	DISP_VALO = 7'b0000001; //F0 = 7'b0111000;
8'hF1: begin	DISP_VAL1	DISP_VAL0 = 7'b1001111; //F1 = 7'b0111000;
8'hF2: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0010010; //F2 = 7'b0111000;
8'hF3: begin	DISP_VAL1 end	DISP_VALO = 7'b0000110; //F3 = 7'b0111000;
8'hF4: begin	DISP_VAL1 end	DISP_VALO = 7'b1001100; //F4 = 7'b0111000;
8'hF5: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100100; //F5 = 7'b0111000;
8'hF6: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0100000; //F6 = 7'b0111000;
8'hF7: begin	DISP_VAL1 end	DISP_VALO = 7'b0001111; //F7 = 7'b0111000;
8'hF8: begin	DISP_VAL1 end	DISP_VALO = 7'b0000000; //F8 = 7'b0111000;
8'hF9: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001100; //F9 = 7'b0111000;
8'hFA: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0001000; //FA = 7'b0111000;
8'hFB: begin	DISP_VAL1 end	DISP_VALO = 7'b1100000; //FB = 7'b0111000;
8'hFC: begin	DISP_VAL1 end	DISP_VALO = 7'b0110001; //FC = 7'b0111000;
8'hFD: begin	DISP_VAL1	DISP_VALO = 7'b1000010; //FD = 7'b0111000;
8'hFE: begin	DISP_VAL1 end	DISP_VAL0 = 7'b0110000; //FE = 7'b0111000;
8'hFF: begin default:begin DISP_VAL0 = 7'b00	DISP_VAL1 end	DISP_VAL0 = 7'b0111000; //FF = 7'b0111000;

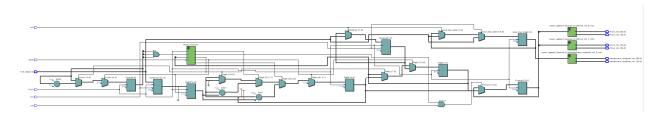
default:begin DISP_VAL0 = 7'b0000000; DISP_VAL1 = 7'b0000000; end//OFF

endcase

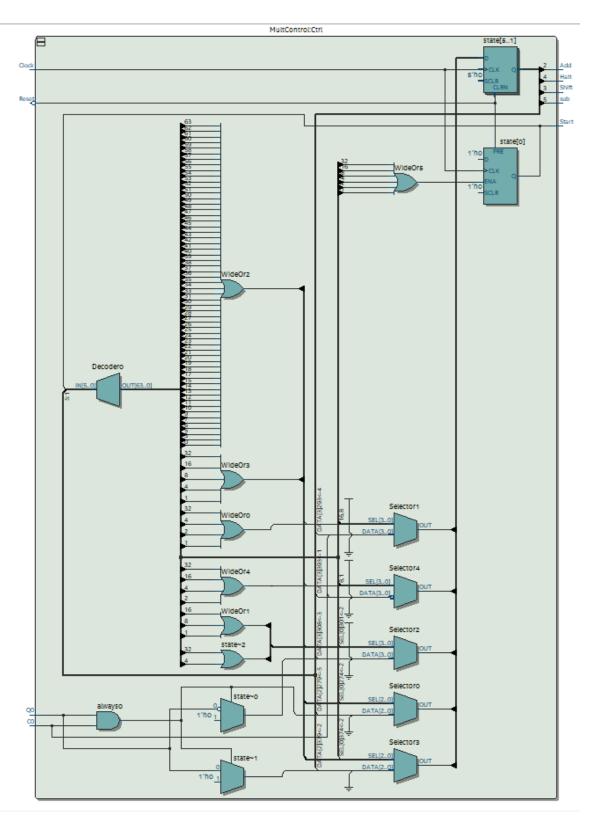
endmodule

5. RTL DIAGRAMS:

Eight_Bit_Multiplier:



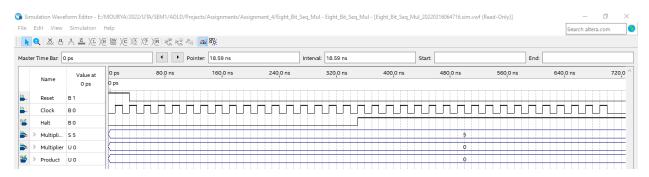
MultControl:



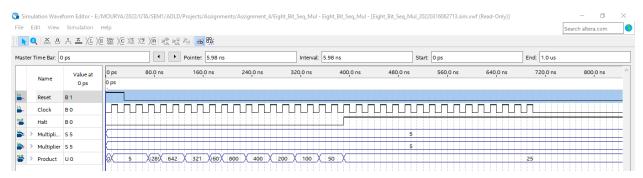
6. Simulation Results Wave Forms:

Unsigned Version Simulation Results:

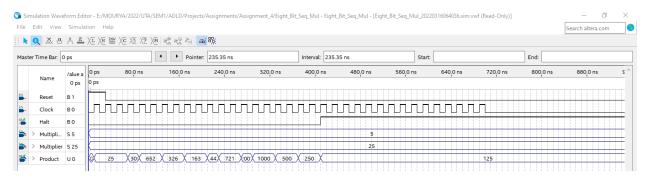
Multiplicand = 5, Multiplier = 0, Product = 0, Clock Cycles = 16



Multiplicand = 5, Multiplier = 5, Product = 25, Clock Cycles = 18

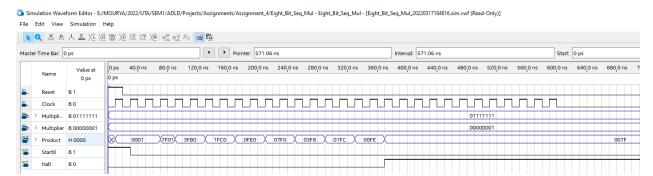


Multiplicand = 5, Multiplier = 25, Product = 125, Clock Cycles = 19

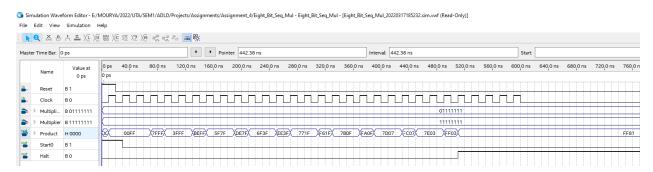


Signed Version Simulation Results:

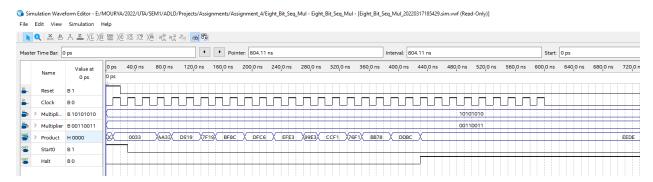
Multiplicand = 0x7F, Multiplier = 0x01, Product = 0x007F, Clock Cycles = 17



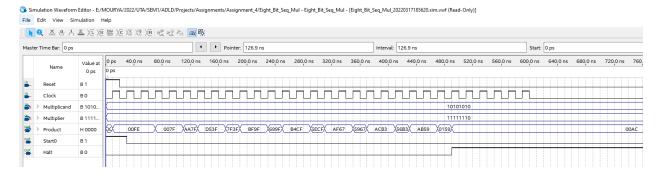
Multiplicand = 0x7F, Multiplier = 0xFF, Product = 0xFF81, Clock Cycles = 24



Multiplicand = 0xAA, Multiplier = 0x33, Product = 0xEEDE, Clock Cycles = 20



Multiplicand = 0xAA, Multiplier = 0xFE, Product = 0x00AC, Clock Cycles = 23



Multiplicand = 0xDD, Multiplier = 0xCD, Product = 0x06F9, Clock Cycles = 21



7. PIN ASSIGNMENTS:

71 11117 601011111211101	
set_location_assignment PIN_AC9	-to A_B_data[7]
set_location_assignment PIN_AE11	-to A_B_data[6]
set_location_assignment PIN_AD12	-to A_B_data[5]
set_location_assignment PIN_AD11	-to A_B_data[4]
set_location_assignment PIN_AF10	-to A_B_data[3]
set_location_assignment PIN_AF9	-to A_B_data[2]
set_location_assignment PIN_AC12	-to A_B_data[1]
set_location_assignment PIN_AB12	-to A_B_data[0]
set_location_assignment PIN_AF14	-to Clock
set_location_assignment PIN_AA14	-to InA
set_location_assignment PIN_AA15	-to lnB
set_location_assignment PIN_W15	-to Reset
set_location_assignment PIN_Y16	-to out
set_location_assignment PIN_AE26	-to Prod_nib_0[0]
set_location_assignment PIN_AE27	-to Prod nib 0[1]
set_location_assignment PIN_AE28	-to Prod_nib_0[2]
set location assignment PIN AG27	-to Prod_nib_0[3]
set_location_assignment PIN_AF28	-to Prod_nib_0[4]
set_location_assignment PIN_AG28	-to Prod_nib_0[5]
set_location_assignment PIN_AH28	-to Prod_nib_0[6]
set_location_assignment PIN_AJ29	-to Prod_nib_1[0]
set_location_assignment PIN_AH29	-to Prod_nib_1[1]
set_location_assignment PIN_AH30	-to Prod_nib_1[2]
set_location_assignment PIN_AG30	-to Prod_nib_1[3]
set_location_assignment PIN_AF29	-to Prod_nib_1[4]
set_location_assignment PIN_AF30	-to Prod_nib_1[5]
set_location_assignment PIN_AD27	-to Prod_nib_1[6]
set_location_assignment PIN_AB23	-to Prod_nib_2[0]
set_location_assignment PIN_AE29	-to Prod_nib_2[1]
set_location_assignment PIN_AD29	-to Prod_nib_2[2]
set_location_assignment PIN_AC28	-to Prod_nib_2[3]
set_location_assignment PIN_AD30	-to Prod_nib_2[4]
set_location_assignment PIN_AC29	-to Prod_nib_2[5]
set_location_assignment PIN_AC30	-to Prod_nib_2[6]
set location assignment PIN AD26	-to Prod_nib_3[0]
set_location_assignment PIN_AC27	-to Prod_nib_3[1]
set_location_assignment PIN_AD25	-to Prod_nib_3[2]
set_location_assignment PIN_AC25	-to Prod_nib_3[3]
set_location_assignment PIN_AB28	-to Prod_nib_3[4]
set_location_assignment PIN_AB25	-to Prod_nib_3[4] -to Prod_nib_3[5]
set_location_assignment PIN_AB22	-to Prod_nib_3[6]
set_location_assignment PIN_AA24	-to multiplicand_multiplier_nib_0[0]
set_location_assignment PIN_Y23	-to multiplicand_multiplier_nib_0[1]
set_location_assignment PIN_Y24	-to multiplicand_multiplier_nib_0[2]
set_location_assignment PIN_W22	-to multiplicand_multiplier_nib_0[3]
set_location_assignment PIN_W24	-to multiplicand_multiplier_nib_0[4]

set_location_assignment PIN_V23
set_location_assignment PIN_W25
set_location_assignment PIN_V25
set_location_assignment PIN_AA28
set_location_assignment PIN_Y27
set_location_assignment PIN_AB27
set_location_assignment PIN_AB26
set_location_assignment PIN_AA26
set_location_assignment PIN_AA25

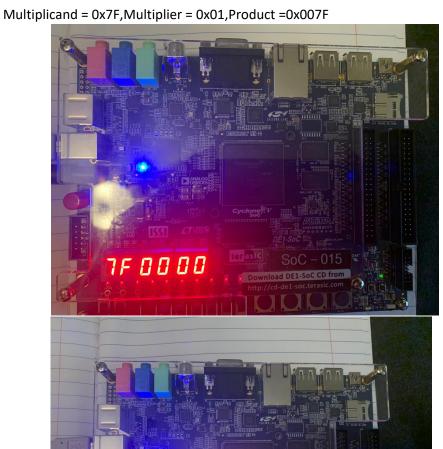
-to multiplicand_multiplier_nib_0[5]
-to multiplicand_multiplier_nib_0[6]
-to multiplicand_multiplier_nib_1[0]
-to multiplicand_multiplier_nib_1[1]
-to multiplicand_multiplier_nib_1[2]
-to multiplicand_multiplier_nib_1[3]
-to multiplicand_multiplier_nib_1[4]
-to multiplicand_multiplier_nib_1[5]
-to multiplicand_multiplier_nib_1[6]

8. TEST RESULTS:

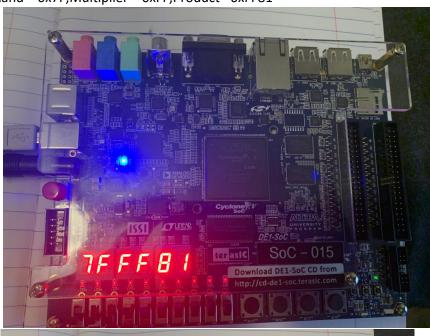
Multiplicand (HEX5,4)	Multiplier (HEX5,4)	Product (HEX3,2,1,0)	Clock Cycles Taken (Observed in Simulation)
0x7F	0x01	0x007F	17
0x7F	0xFF	0xFF81	24
0xAA	0x33	0xEEDE	20
0xAA	0xFE	0x00AC	23
0xDD	0xCD	0x06F9	21

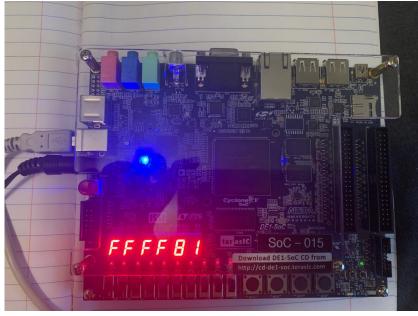
9.Photos Of Test Results

0 100 TF

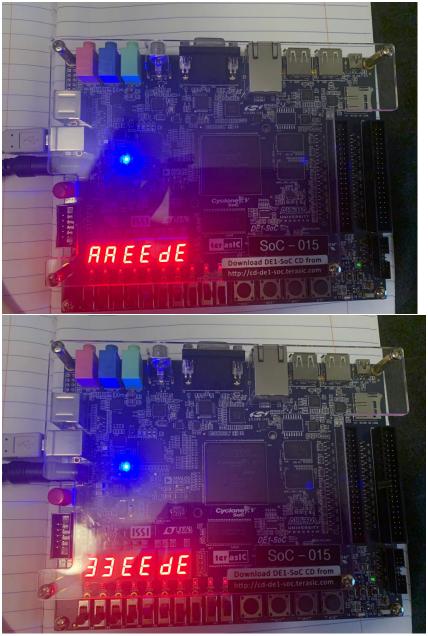


Multiplicand = 0x7F,Multiplier = 0xFF,Product =0xFF81





Multiplicand = 0xAA,Multiplier = 0x33,Product =0xEEDE



Multiplicand = 0xAA,Multiplier = 0xFE,Product =0x00AC





Multiplicand = 0xDD,Multiplier = 0xCD,Product =0x06F9

