Low-Voltage H-Bridge IC With LDO Voltage Regulator

FEATURES

- **H-Bridge Motor Driver**
  - **Drives a DC Motor, One Winding of a Stepper Motor, or Other Loads**
  - **Low MOSFET On-Resistance: 45 mΩ per FET**
- **5-A Continuous 8-A Peak-Drive Current**
- **Internal Current Sensing With Current Sense Output**
- **2 to 5.5-V Operating Supply Voltage Range**
- **Overvoltage and Undervoltage Lockout**
- **Low-Power Sleep Mode**
- **100-mA Isolated Low-Dropout (LDO) Voltage Regulator**
- **24-Pin QFN Package**
- **24-Pin HTSSOP Package**

APPLICATIONS

- **Battery-Operated Applications With High Startup Torque, such as:**
  - **Personal Hygiene (Electric Toothbrushes, Shavers)**
  - **Toys**
  - **RC Helicopters and Cars**
  - **Robotics**

DESCRIPTION

The DRV8850 device provides a motor driver plus LDO voltage regulator solution for consumer products, toys, and other low-voltage or battery-powered motion-control applications. The device has one H-bridge driver to drive a DC motor, a voice-coil actuator, one winding of a stepper motor, a solenoid, or other devices. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the load. An internal charge pump generates the needed gate-drive voltages.

The DRV8850 device supplies up to 5 A of continuous output current (with proper PCB heat sinking) and up to 8-A peak current. It operates on a supply voltage from 2.0 to 5.5 V.

A low-dropout linear voltage regulator is integrated with the motor driver to supply power to microcontrollers or other circuits. The LDO voltage regulator can be active in device sleep mode, so that the driver may be shut down without removing power to any devices powered by the LDO voltage regulator.

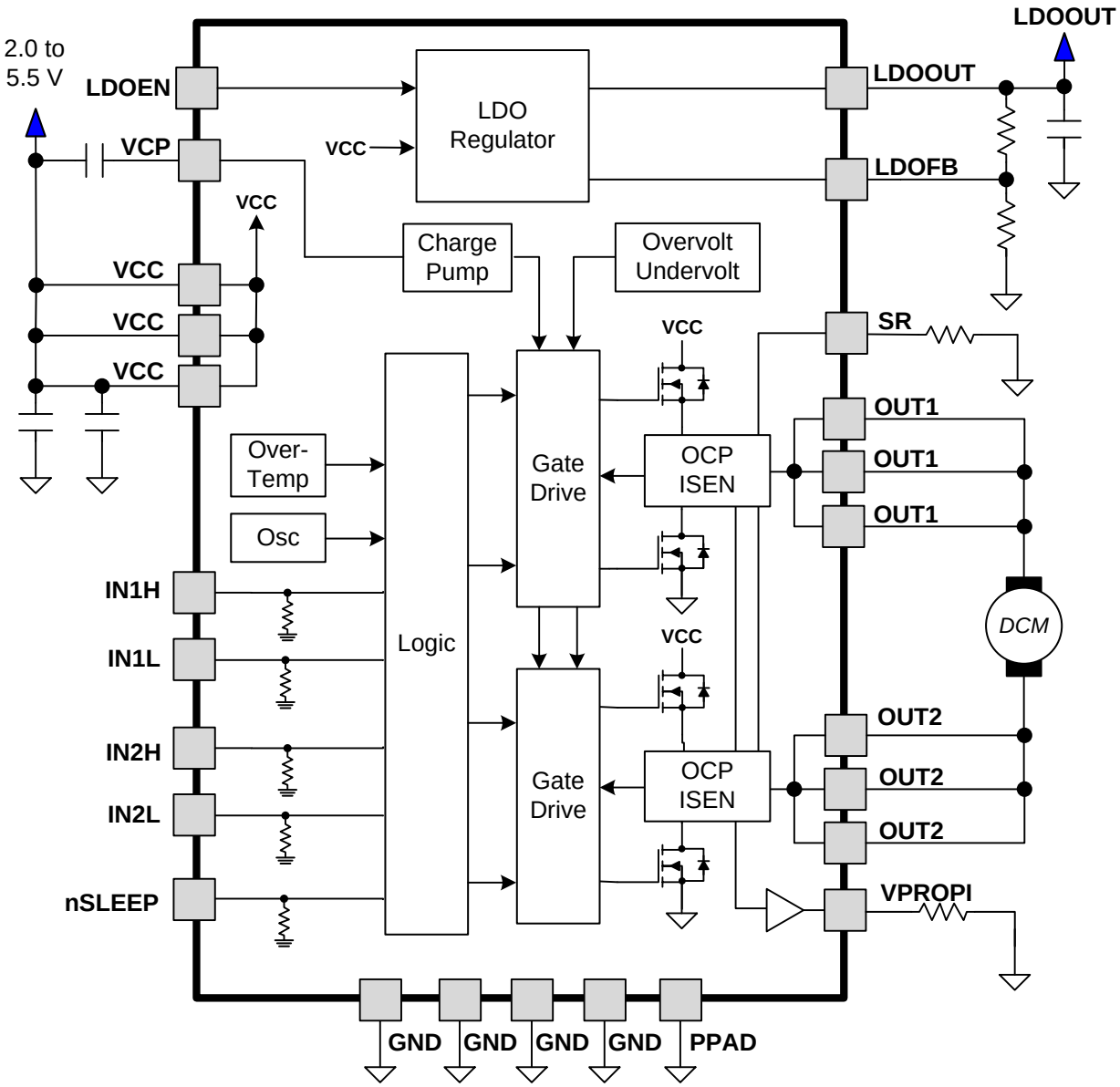
Internal shutdown functions provide overcurrent, short-circuit, undervoltage, overvoltage, and overtemperature protection. In addition, the device also has a built-in current sensing for accurate current measurement.

The DRV8850 device is packaged in a 24-pin HTSSOP (7.7 mm × 4.4 mm) or QFN (3.5-mm × 5.5-mm) package with PowerPAD™ (Eco-friendly: RoHS and no Sb/Br).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

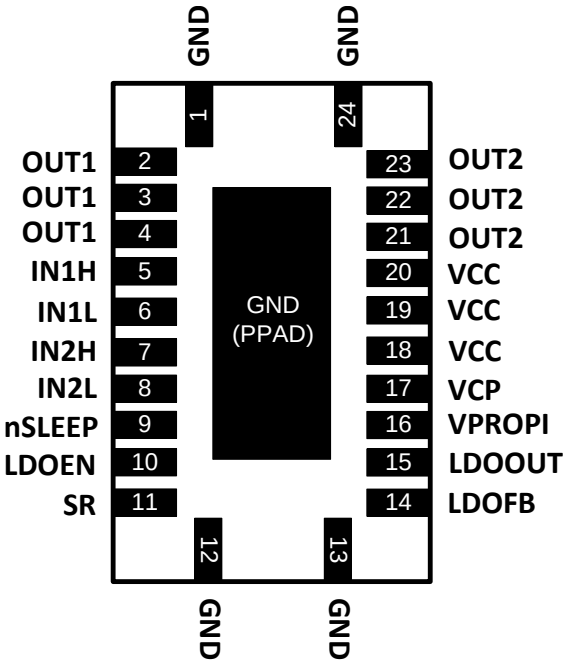
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



DEVICE INFORMATION

DRV8850RGY (QFN) PACKAGE
(TOP VIEW)



DRV8850PWP (HTSSOP) PACKAGE
(TOP VIEW)

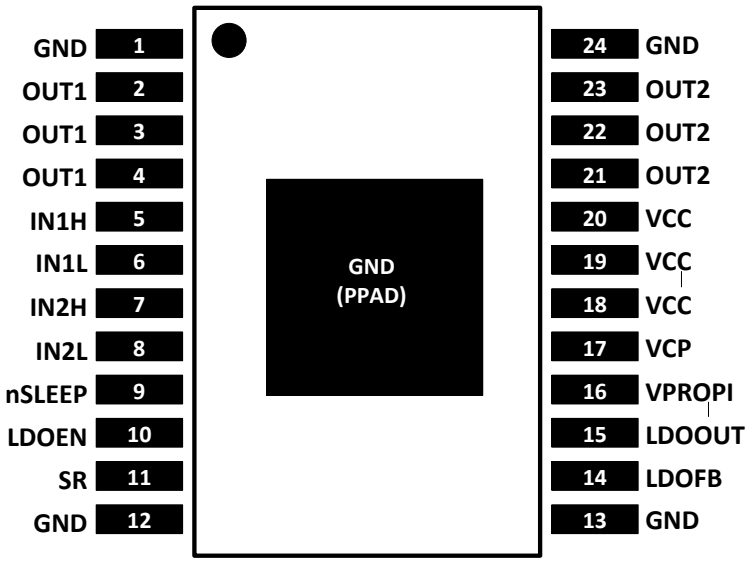


Table 1. Terminal Functions

PIN		I/O(1)	DESCRIPTION	
NAME	NO.			
POWER AND GROUND				
GND	1, 12, 13, 24, PPAD	–	Device ground	
LDOOUT	15	–	LDO regulator output	Bypass to GND with a 2.2-µF 6.3-V ceramic capacitor
VCC	21, 22, 23	–	Device supply	Bypass to GND with 0.1-µF and 10-µF 6.3-V ceramic capacitors
VCP	17	–	Charge pump	Connect a 0.1-µF 6.3-V ceramic capacitor to VCC
CONTROL				
LDOEN	10	I	LDO regulator enable	Logic low disables LDO regulator Logic high enables LDO regulator Internal pulldown resistor
LDOFB	14	I	LDO regulator feedback	Resistor divider from LDOOUT sets LDO output voltage May be connected to LDOIN to enable LDO
IN1H	5	I	Input 1 HS FET enable	Active high enables HS FET for output 1 Internal pulldown resistor
IN1L	6	I	Input 1 LS FET enable	Active high enables LS FET for output 1 Internal pulldown resistor
IN2H	7	I	Input 2 HS FET enable	Active high enables HS FET for output 2 Internal pulldown resistor
IN2L	8	I	Input 2 LS FET enable	Active high enables LS FET for output 2 Internal pulldown resistor
nSLEEP	9	I	Sleep mode input	Logic low puts device in low-power sleep mode Logic high for typical operation Internal pulldown resistor
SR	11	IO	Slew rate control	Resistor to ground sets output slew rate
OUTPUT				
OUT1	2, 3, 4	O	Output 1	Connect to motor winding
OUT2	18, 19, 20	O	Output 2	
VPROPI	16	O	Current sense output	Output current is proportional to H-bridge current. 1 kΩ, 1% resistor to GND for 2-A max current with VCC at 2 V. See text for equation if more current is required

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input or output

Table 2. External Components

PIN		DESCRIPTION	
NAME	NO.		
LDOFB	14	LDO regulator feedback	Resistor divider from LDOUT sets LDO output voltage.
LDOOUT	15	LDO regulator output	Bypass to GND with a 2.2-µF 6.3-V ceramic capacitor.
SR	11	Slew rate control	Resistor to ground sets output slew rate GND to 2.4 MΩ.
VCC	21, 22, 23	Device supply	Bypass to GND with 0.1-µF and 10-µF 6.3-V ceramic capacitors.
VCP	17	Charge pump	Connect a 0.1-µF 6.3-V ceramic capacitor to VCC
VPROPI	16	Current sense output	Output current is proportional to H-bridge current. 1 kΩ, 1% resistor to GND for 2-A max current with VCC at 2 V. See Equation 1 for if more current is required.

Absolute Maximum Ratings(1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VCC	Power supply voltage range	–0.3		7	V
VCP	Charge pump	–0.3		VCC + 7	
LDOEN, IN1H, IN1L, IN2H, IN2L, nSLEEP	Digital pin voltage range	–0.5		7	
OUT1, OUT2, SR, LDOUT, LDOFB, VPROPI	Other pins	–0.3		7	
OUT1, OUT2	Peak motor drive output current	Internally Limited			A
LDOOUT	LDO output current	Internally Limited			
T_J	Operating junction temperature range	–40		150	°C
T_{STG}	Storage temperature range	–60		150	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device power supply voltage range	2.0		5.5	V
I_{OUT}	H-bridge continuous output current(1)	0		5	A
I_{OUT}	H-bridge peak output current (1)	0		8	A
f_{PWM}	Externally applied PWM frequency	0		50	kHz
V_{IN}	Logic level input voltage	0		V_{CC}	V
T_A	Ambient temperature	–40		85	°C

(1) Power dissipation and thermal limits must be observed

Thermal Information

THERMAL METRIC(1)		DRV8850		UNIT
		PWP	RGY	
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	43.8	39.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	24.6	41.1	
θ_{JB}	Junction-to-board thermal resistance(4)	22.7	15.0	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.7	0.6	
ψ_{JB}	Junction-to-board characterization parameter(6)	22.5	14.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	4.1	3.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VCC)						
I_{VCC}	VCC operating supply current, LDO regulator and driver enabled	V_{CC} = 4.2 V, nSLEEP = LDOEN = V_{CC}		2.9		mA
I_{VCQ1}	VCC sleep mode supply current	V_{CC} = 4.2 V, nSLEEP = LDOEN = 0 V, INXH = INXL = 0 V			1	µA
I_{VCQ2}	VCC operating supply current, LDO regulator enabled, driver disabled(1)	V_{CC} = 4.2 V, nSLEEP = 0 V, LDOEN = V_{CC}, INXH = INXL = 0 V		40		µA
I_{VCQ3}	VCC operating supply current LDO voltage regulator disabled, driver enabled	V_{CC} = 4.2 V, nSLEEP = V_{CC}, LDOEN = 0 V		2.9		mA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			2	V
		V_{CC} falling			1.95	
V_{OVLO}	VCC overvoltage lockout voltage	V_{CC} rising	5.6			V
		V_{CC} falling	5.5			
LOGIC-LEVEL INPUTS (LDOEN, IN1H, IN1L, IN2H, IN2L, nSLEEP)						
V_{IL}	Input low voltage		0		0.2 × V_{CC}	V
V_{IH}	Input high voltage		0.5 × V_{CC}		V_{CC}	V
V_{HYS}	Input hysteresis			0.08 × V_{CC}		V
I_{IL}	Input low current	V_{IN} = 0	–1		1	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance	LDOEN		3.5		MΩ
		nSLEEP		400		kΩ
		INXH, INXL		200		kΩ
VPROPI OUTPUT (VPROPI)						
I_{VPROPI}	VPROPI output current	V_{CC} = 4.2 V, resistor chosen to keep VPROPI ≤ (V_{CC} – 1 V) / I_{OUT} 500 mA ≤ I_{OUT} ≤ 5 A		I_{OUT} / 2000		A
H-BRIDGE FETS (OUT1, OUT2)						
$R_{DS(ON)}$	HS FET on resistance	V_{CC} = 4.2 V, I_O = 2 A, T_A = 25°C		35		mΩ
	LS FET on resistance	V_{CC} = 4.2 V, I_O = 2 A, T_A = 25°C		30		mΩ
I_{OFF}	Off-state leakage current	VOUT = 0 V	–1		1	µA
LDO REGULATOR (LDOOUT)						
V_{FB}	LDO feedback (reference) voltage		0.76	0.8	0.84	V
V_{DO}	LDO regulator dropout voltage	V_{CC} = 4.2 V, IOUT = 100 mA, T_A = 25°C		150		mV
		V_{CC} = 4.2 V, IOUT = 100 mA, T_A = 85°C		175		mV
ΔV_{LINE}	LDO line regulation	V_{CC} from 4.2 to 5.5 V, VOUT = 3.3 V	–2.5		2.5	%
ΔV_{LOAD}	LDO load regulation	VOUT = 3.3 V, IOUT from 1 to 100 mA	–2.5		2.5	%
I_{CL}	LDO output current limit	V_{CC} = 4.2 V, VOUT = 3.3 V, T_A ≥ 25°C	275			mA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level	V_{CC} = 2.5 to 5.5 V	9.5			A
t_{OCP}	Overcurrent protection deglitch time			1		µs
t_{RETRY}	Overcurrent retry time			4		ms
t_{TSD}	Thermal shutdown temperature	Die temperature (rising)	150	160	180	°C
t_{HYS}	Thermal shutdown hysteresis	Temperature hysteresis		50		°C

(1) Does not include the current consumption from the feedback resistors.

Timing Requirements (1)

T_A = 25°C, VCC = 4.2 V, RL = 2 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_R, t_F	Rise and fall time (measured at OUTx)	RSR connected to GND			70		ns
		RSR = 24 kΩ			0.7		µs
		RSR = 2.4 MΩ			70		µs
t_{DELAY}	Propagation delay (measured as time between input edge to output change)	RSR connected to GND			500		ns
		RSR = 24 kΩ			750		ns
		RSR = 2.4 MΩ			50		µs
t_{DEAD}	Dead time (measured as time OUTx FET is Hi-Z)	Low-side slow decay LS OFF to HS ON	RSR short to GND		400		ns
			RSR = 24 kΩ		2.6		µs
			RSR = 2.4 MΩ		110		µs
		Low-side slow decay HS OFF to LS ON	RSR short to GND		400		ns
			RSR = 24 kΩ		2.6		µs
			RSR = 2.4 MΩ		110		µs
		High-side slow decay or fast decay HS OFF to LS ON	RSR short to GND		400		ns
			RSR = 24 kΩ		2.6		µs
			RSR = 2.4 MΩ		110		µs
		High-side slow decay or fast decay LS OFF to HS ON	RSR short to GND		600		ns
			RSR = 24 kΩ		3.9		µs
			RSR = 2.4 MΩ		165		µs

(1) Rise and fall time measured from 10 to 90% V_{CC}

TYPICAL PERFORMANCE GRAPHS

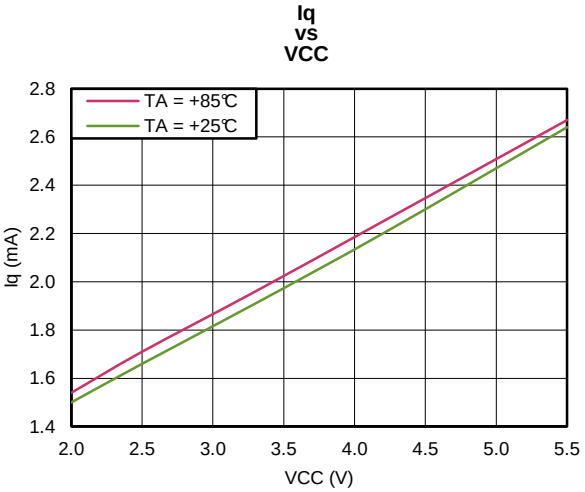


Figure 1. Quiescent Current With Motor Driver on and LDO On

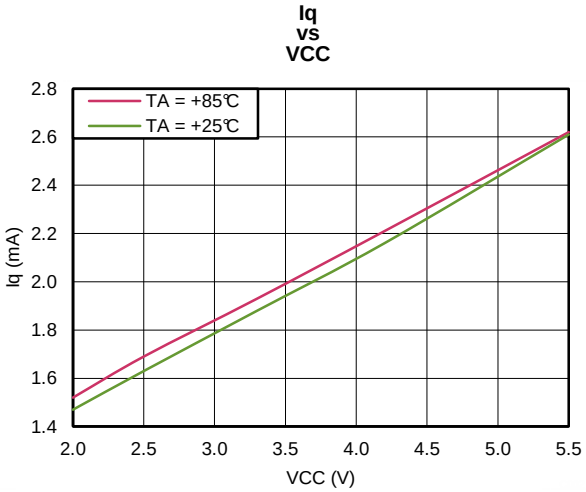


Figure 2. Quiescent Current With Motor Driver on and LDO Off

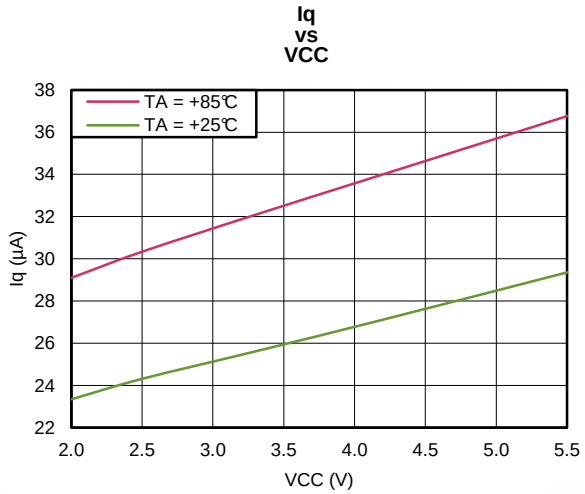


Figure 3. Quiescent Current With Motor Driver off and LDO On

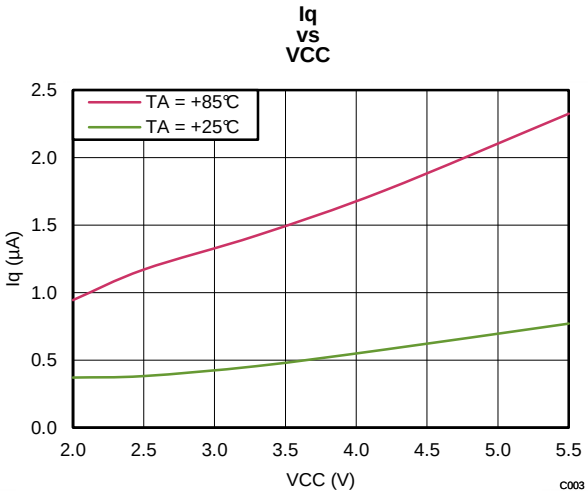


Figure 4. Quiescent Current With Motor Driver off and LDO off, Sleep Current

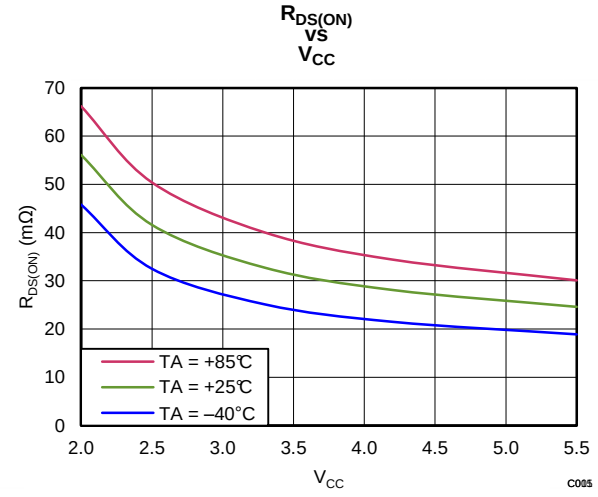


Figure 5. $R_{DS(ON)}$, HS – OUT1

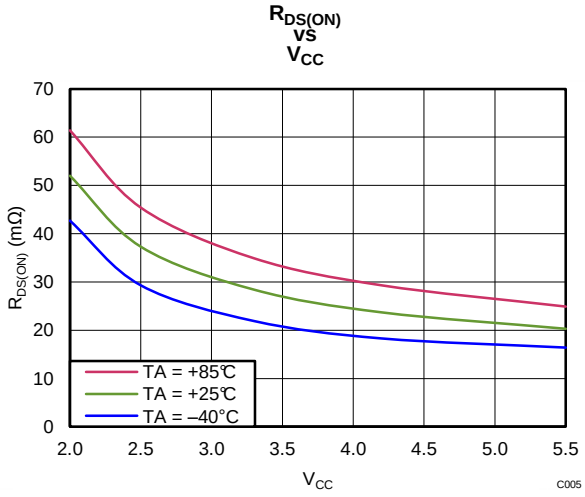


Figure 6. $R_{DS(ON)}$, HS – OUT2

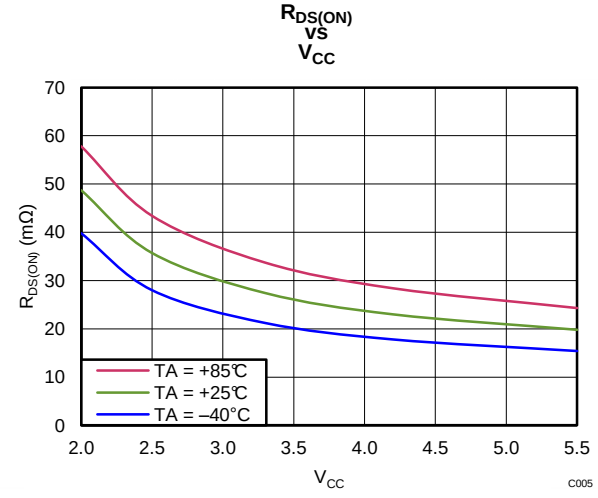


Figure 7. $R_{DS(ON)}$, LS – OUT1

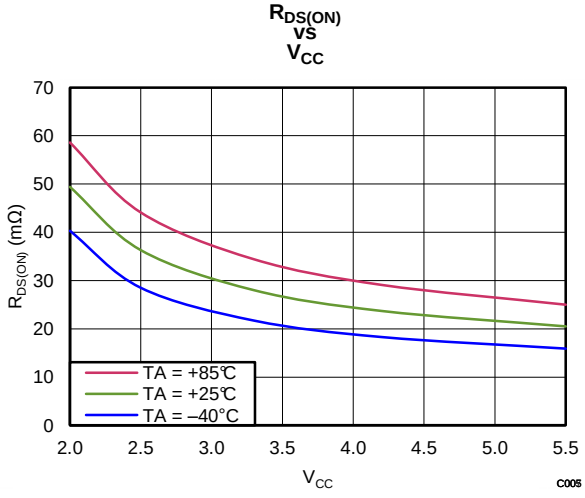


Figure 8. $R_{DS(ON)}$, LS – OUT2

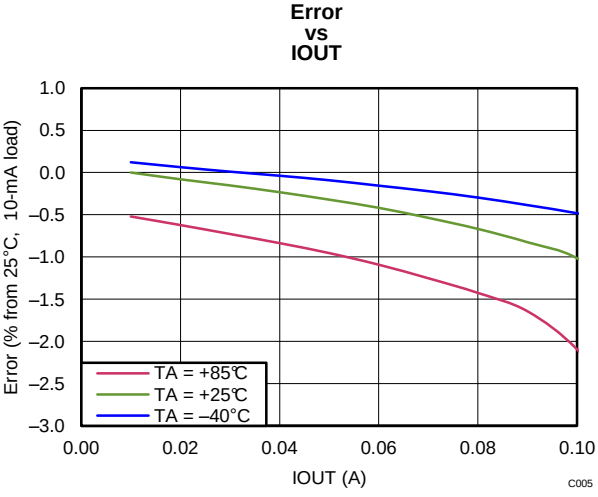


Figure 9. LDO Output, VCC = 3.5 V, LDOOUT = 3.3 V

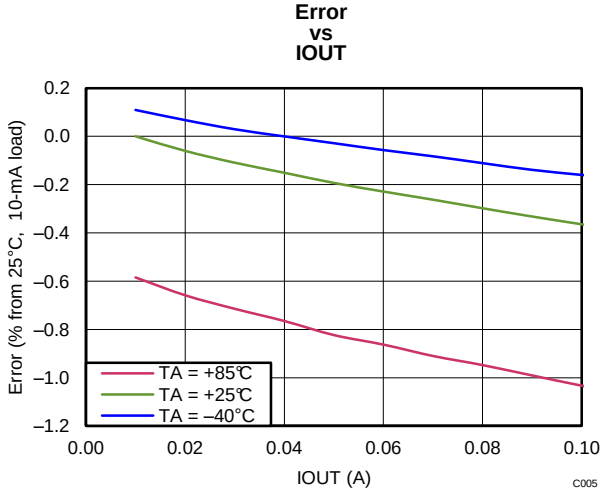


Figure 10. LDO Output, VCC = 4.2 V, LDOOUT = 3.3 V

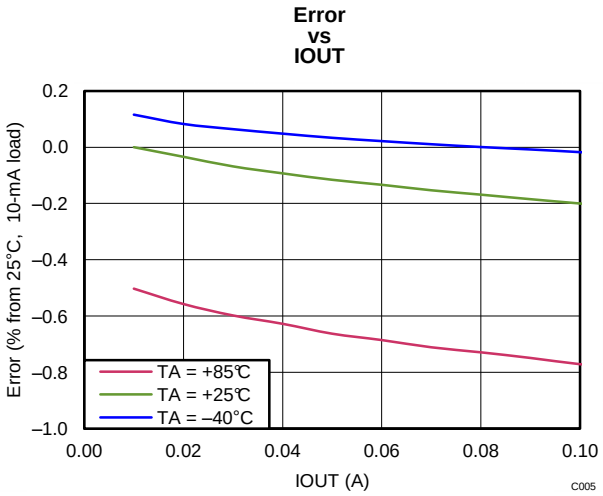


Figure 11. LDO Output, VCC = 5.5 V, LDOOUT = 3.3 V

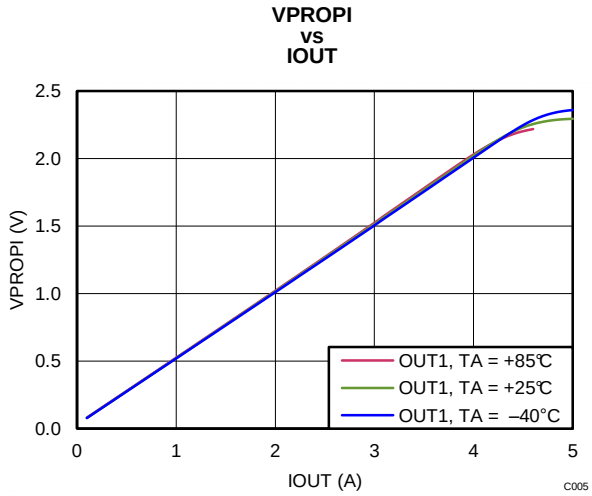


Figure 12. VPROPI Output, VCC = 4.2 V, OUT1 overtemperature, 1 kΩ

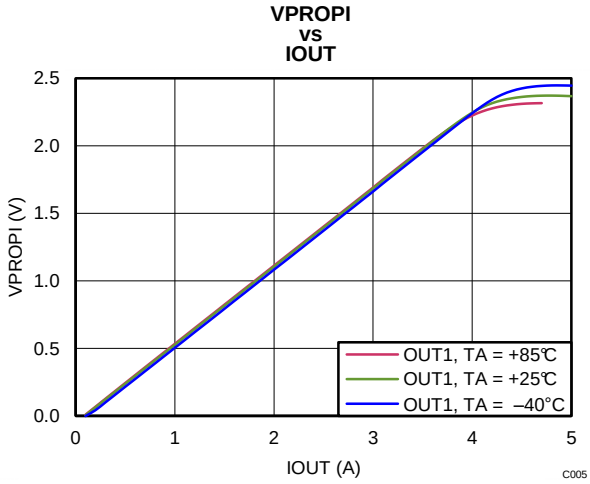


Figure 13. VPROPI Output, VCC = 4.2 V, OUT2 overtemperature, 1 kΩ

Functional Description

Power Supervisor

The LDO regulator can be active independent of the nSLEEP pin. This independence allows a microcontroller, or other device, to be powered by the LDO voltage regulator, while retaining the ability to put the DRV8850 device into sleep mode.

Because of this functionality, nSLEEP and LDOEN must both be brought logic low to minimize power consumption in sleep mode. If the LDO regulator remains active in sleep mode, a quiescent current of I_{VCQ2} (typically 50 µA plus current through the external feedback resistors) is drawn from the supply.

Table 3 shows the operation mode logic for the DRV8850 device:

Table 3. DRV8850 Device Operation Mode Logic(1)

nSLEEP	LDOEN	LDO Regulator	Driver
0	0	Off	Sleep
0	1	Active	Sleep
1	0	Off	Active
1	1	Active	Active

(1) A state must be active for a minimum of 1 ms before a new state is commanded.

Bridge Control

A corresponding input pin controls the individual FETs in the DRV8850 device. Shoot-through (the condition when both HS and LS FETs are turned on at the same time) is not allowed; with this input condition, both the HS and LS FETs turn off.

Table 4 shows the logic for the DRV8850 device:

Table 4. DRV8850 Device Logic

INxL	INxH	OUTx
0	0	Z
0	1	H
1	0	L
1	1	Z

Current Sensing – VPROPI

The VPROPI pin outputs an analog current that is proportional to the current flowing in the H-bridge. The output current is typically 1 / 2000 of the current in both high side FETs. VPROPI is derived from the current through either of the high side FETs. Because of this, VPROPI does not represent the H-bridge current when operating in a fast-decay mode or low-side slow-decay mode. VPROPI represents the H-bridge current under forward drive, reverse drive, and high-side slow decay. VPROPI output is delayed by roughly 2 µs after the high side FET is switched on and it has reached approximately VCC (including the deglitch on the HSon). Select the external resistor so that the voltage on VPROPI is less than (VCC – 1 V), so the resistor must be sized less than:

$$2000 \; x \; \left(VCC \; - \; 1\,V\right) \; / \; I_{OUT} \tag{1}$$

where I_{OUT} is the maximum drive current to be monitored

The range of current that can be monitored is 500 mA to 5 A, assuming the external resistor meets the prior equation.

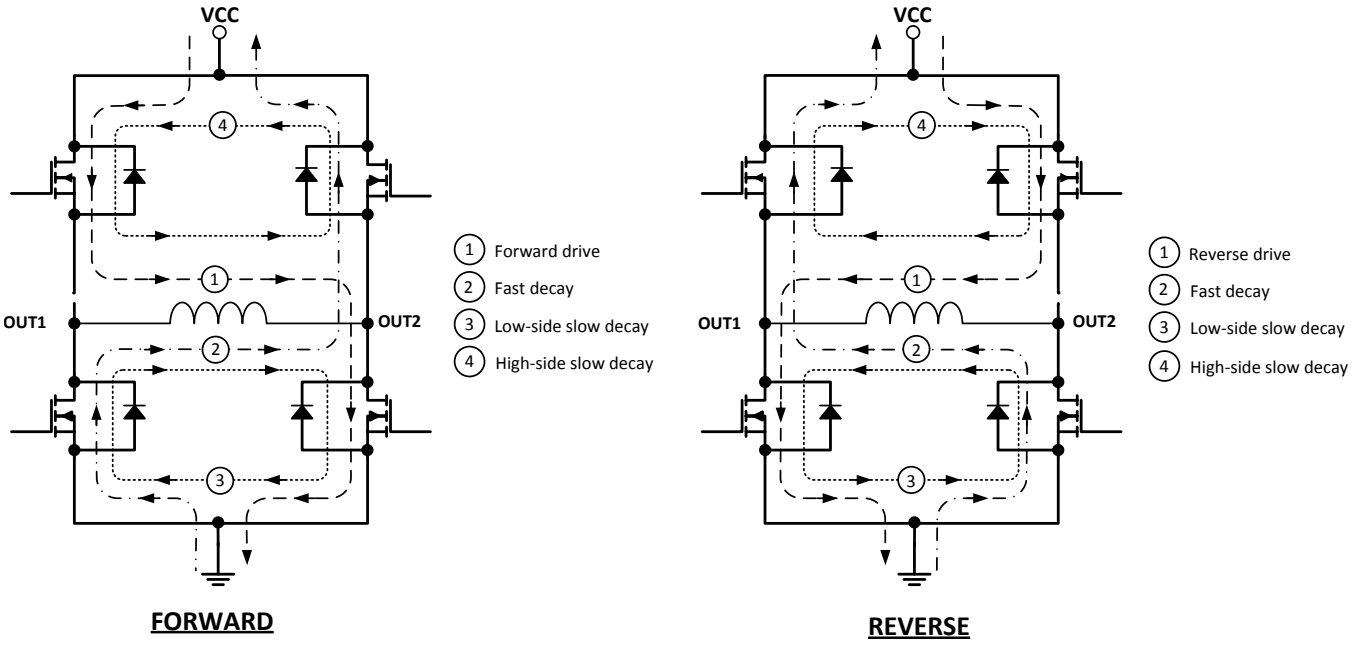


Figure 14. Forward and Reverse Operation

When using an independent half-bridge as a high-side driver, VPROPI does not output a current measurement during slow decay. During typical operation, VPROPI represents the total current flowing to loads connected to OUT1 and OUT2.

VPROPI is nonfunctional when implemented as a low-side driver.

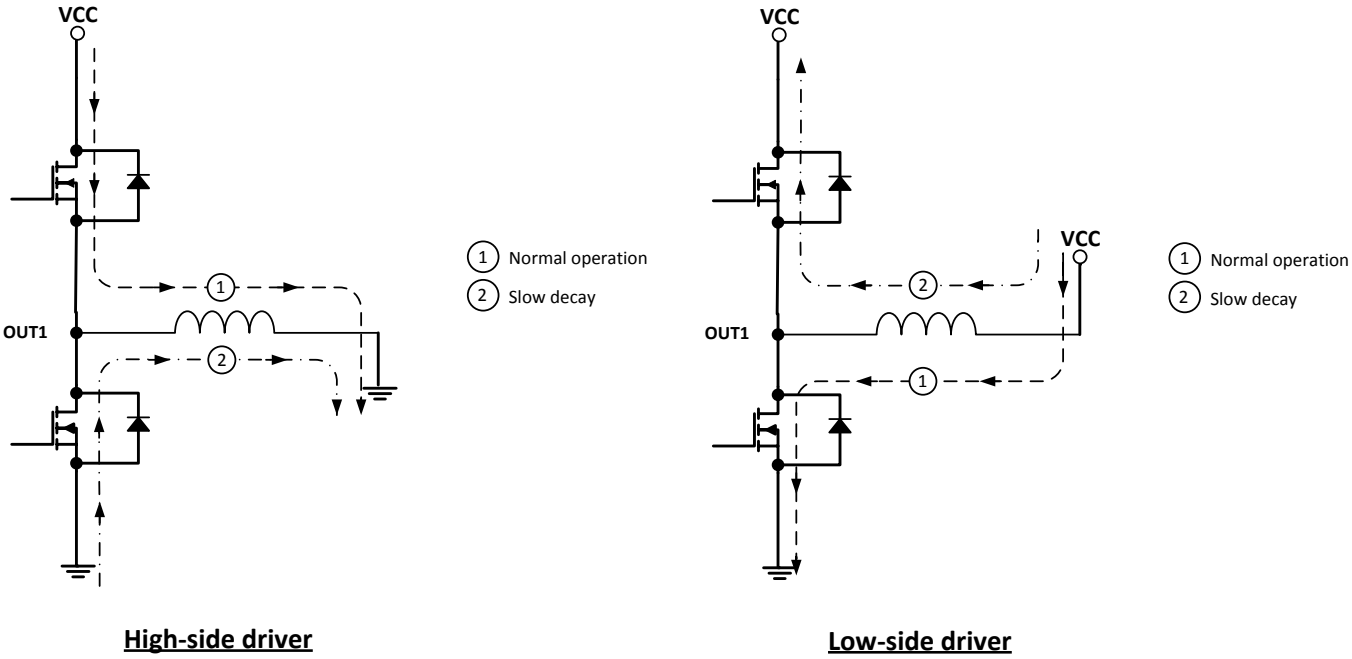


Figure 15. High-Side and Low-Side Drivers

Slew-Rate Control

The rise and fall times (t_R and t_F) of the outputs can be adjusted by the value of an external resistor connected from the SR pin to ground. The output slew rate is adjusted internally by the DRV8850 device by controlling the ramp rate of the driven FET gate.

The typical voltage on the SR pin is 0.6 V driven internally. Changing the resistor value monotonically increases the slew rates from approximately 100 ns to 100 µs. Recommended values for the external resistor are from GND to 2.4 MΩ. If the SR pin is grounded then the slew rate is 100 ns.

Dead Time

The dead time (t_{DEAD}) is measured as the time when OUTx is Hi-Z between turning off one of the H-bridge FETs and turning on the other. For example, the output is Hi-Z between turning off the high-side FET and turning on the low-side FET. When driving current out of the pin, the output is observed to fall to one diode drop below ground during dead time. When driving current into the pin, the output is observed to rise to one diode drop above VCC.

The DRV8850 has an analog dead time of approximately 100 ns. In addition to this analog dead time, the output is Hi-Z when the FET gate voltage is less than the threshold voltage. The total dead time depends on the SR resistor setting because a portion of the FET gate ramp includes the observable dead time.

Propagation Delay

The propagation delay time (t_{DELAY}) is measured as the time between an input edge to an output change. This time is composed of two parts: an input deglitcher and output slewing delay. The input deglitcher prevents noise on the input pins from affecting the output state.

The output slew rate also contributes to the delay time. For the output to change state during typical operation, first one FET must be turned off. The FET gate is ramped down according to the SR resistor selection, and the observed propagation delay ends when the FET gate falls to less than the threshold voltage.

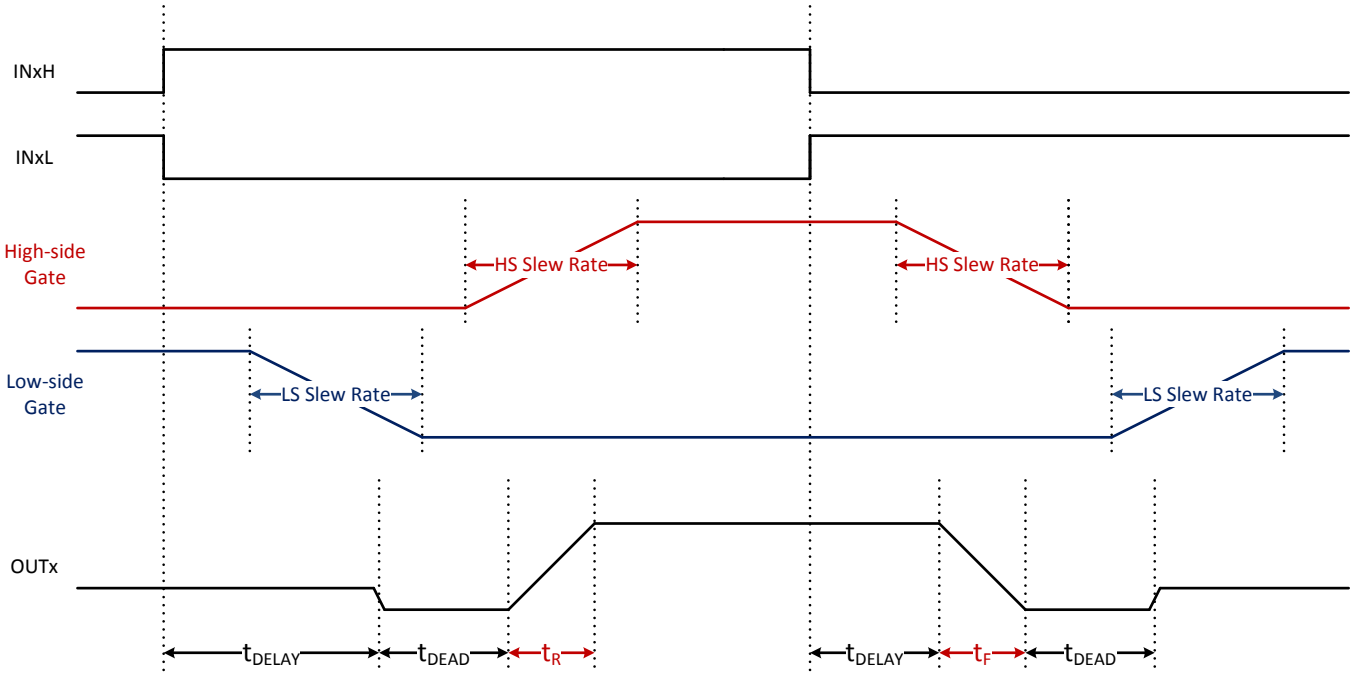


Figure 16. Low-Side Slow Decay Operation – Current Sourced from OUTx

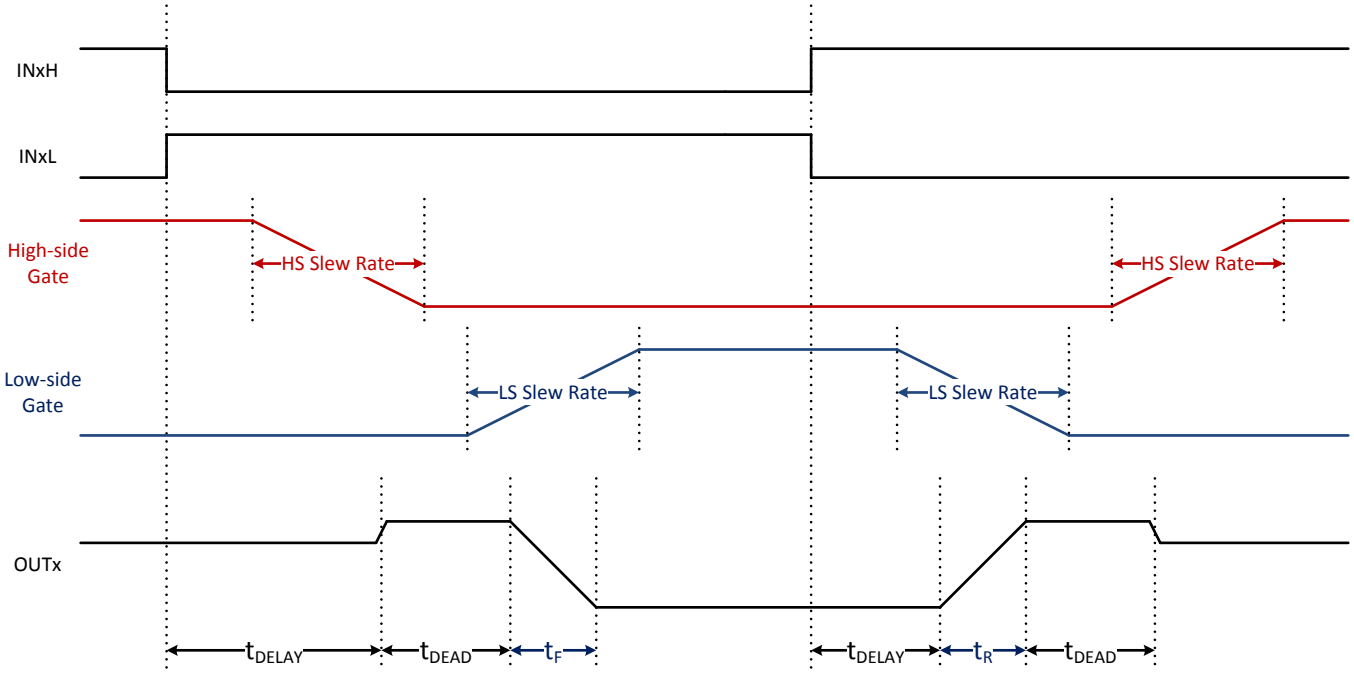


Figure 17. High-Side Slow Decay or Fast Decay Operation – Current Sunk into OUTx

Power Supplies and Input Pins

An internal charge pump generates a voltage greater than VCC that is used to drive the internal N-channel power MOSFETs. The charge pump requires a capacitor between the VCP and VCC pins. TI recommends to bypass VCC to ground with 0.1 and 10-µF ceramic capacitors, placed as close as possible to the IC. Each input pin has a weak pulldown resistor to ground (see Electrical Characteristics for more details).

The input pins should not be driven to more than 0.6 V without the VCC power supply removed.

LDO Voltage Regulator

An LDO regulator is integrated into the DRV8850 device. The LDO regulator is typically used to provide the supply voltage for a low-power microcontroller. For proper operation, bypass the LDOOUT pin to GND using a ceramic capacitor. The recommended value for this component is 2.2 µF.

Two external resistors are used to set the LDO voltage (V_{LDO}) by creating a voltage divider between LDOOUT and LDOFB. The LDO output voltage can be given by:

$$V_{LDO} = V_{FB} \times \left(1 + R1 / R2\right) V \quad (2)$$

where

- R1 is located between LDOOUT and LDOFB
- R2 is between LDOFB and GND

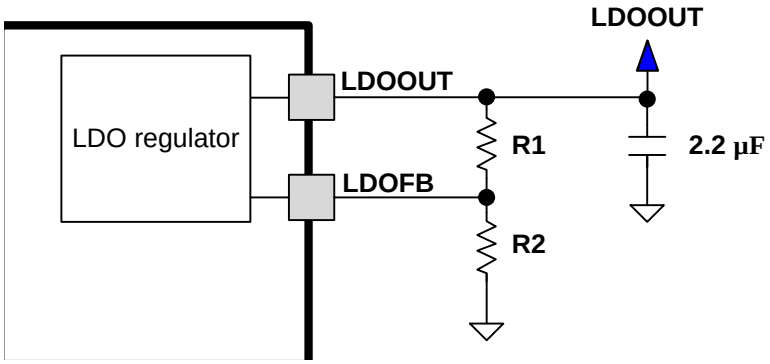


Figure 18. LDO Regulator Schematic

The output voltage is adjustable from 1.6 V to VCC – V_{LDO} using external resistors. The LDOEN pin is used to enable or disable the LDO regulator; when disabled, the output is turned off and the LDO regulator enters a very-low-power state.

When the LDO current load exceeds I_{CL}, the LDO regulator behaves like a constant current source. The LDO output voltage drops significantly with currents greater than I_{CL}.

Protection Circuits

The DRV8850 device is protected against undervoltage, overvoltage, overcurrent, and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{OCP}, all FETs in the H-bridge are disabled. After approximately t_{RETRY}, the bridge re-enables automatically.

Overcurrent conditions on both high and low-side devices, that is, a short to ground, supply, or across the motor winding result in an overcurrent shutdown.

Thermal Shutdown (TSD)

If the die temperature exceeds t_{TSD}, all FETs in the H-bridge are disabled. Once the die temperature has fallen below $t_{TSD} – t_{HYS}$, the H-bridge automatically re-enables.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pins falls to less than the undervoltage lockout threshold voltage, all circuitry in the device is disabled and internal logic resets. Operation resumes when VCC rises to greater than the UVLO threshold.

Overvoltage Lockout (OVLO)

If at any time the voltage on the VCC pins rises to more than V_{OVLO}, the output FETs are disabled (outputs are high-Z). Operation resumes when VCC falls below the V_{OVLO}.

CAUTION

VCC must remain less than the absolute maximum rating for the device, or damage to the device may occur.

Thermal Information

Thermal Protection

The DRV8850 device has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately t_{TSD}, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8850 device is the sum of the motor driver power dissipation and the LDO voltage regulator dissipation.

The LDO dissipation is calculated simply by $(V_{IN} – V_{OUT}) \times I_{OUT}$.

The power dissipation in the motor driver is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Power dissipation can be estimated by:

$$P_{TOT} = \left(LS\_R_{DS(ON)} + HS\_R_{DS(ON)}\right) x \left(I_{OUT(RMS)}\right)^2$$

where

- P_{TOT} is the total power dissipation
- $R_{DS(ON)}$ is the resistance of each FET
- $I_{OUT(RMS)}$ is the RMS output current being driven (3)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heat sinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

REVISION HISTORY

Changes from Original (November 2013) to Revision A	Page
• Removed product preview banner	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8850RGYR	ACTIVE	VQFN	RGY	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8850	Samples
DRV8850RGYT	ACTIVE	VQFN	RGY	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8850	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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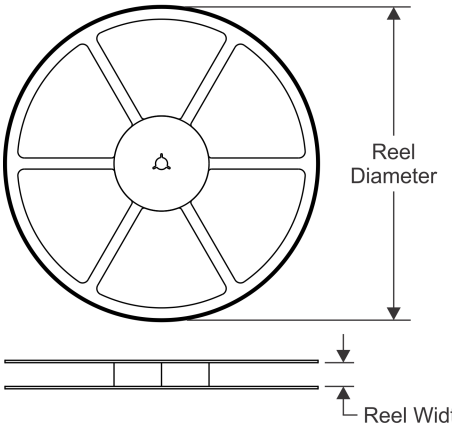
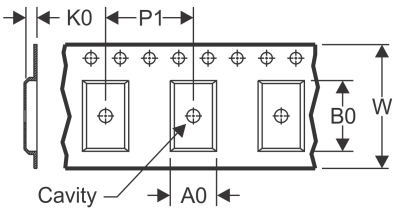
REEL DIMENSIONS

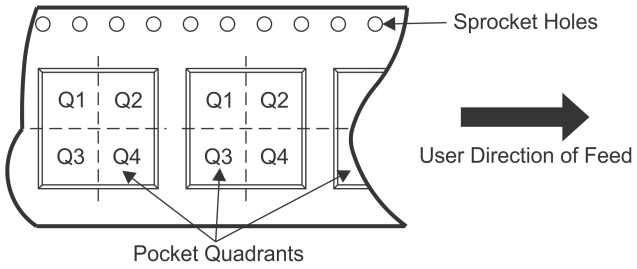


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

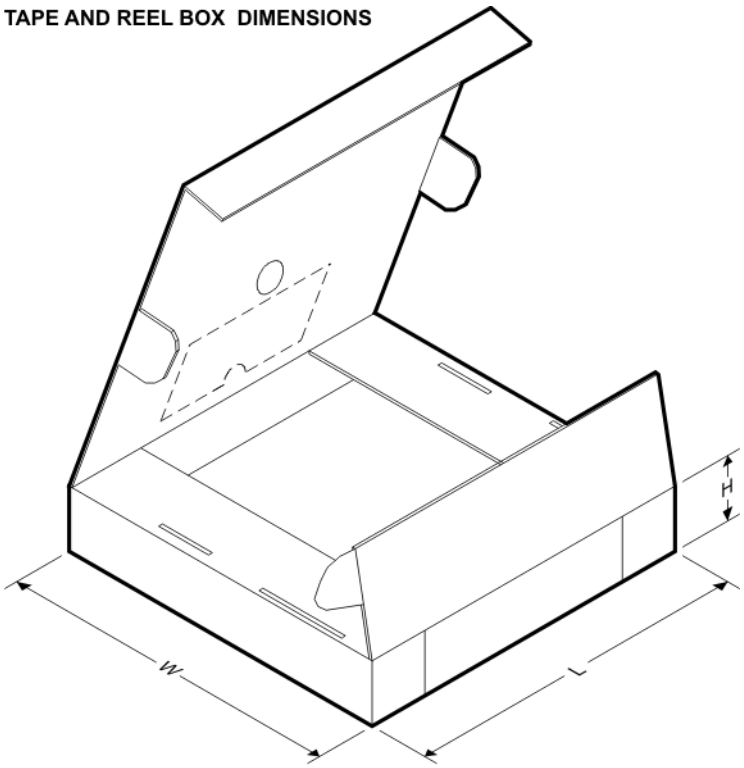
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8850RGYR	VQFN	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

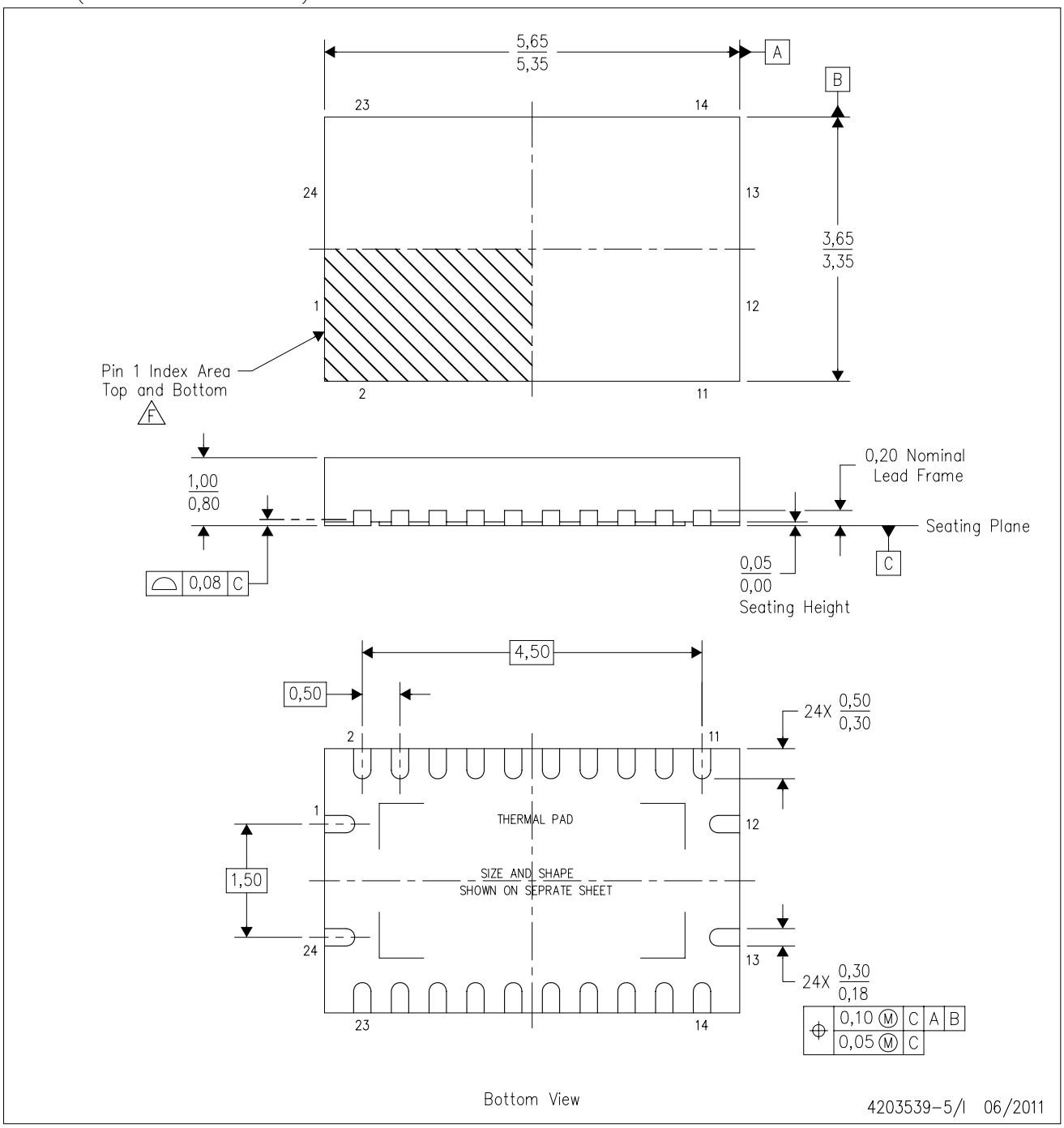
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8850RGYR	VQFN	RGY	24	3000	367.0	367.0	35.0

RGY (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

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