RELATED INFORMATION 1

NOTICE: This related information is not an official part of SEMI M13 and is not intended to modify or supercede the official standard. The standard should be referred to in all cases. SEMI makes no warranties or representations as to the suitability of the material set forth herein for any particular application. The determination of the suitability of the material is solely the responsibility of the user.

R1-1 Consideration for Reliable Automatic Reading of the Marking

R1-1.1 The following suggestions are offered to assist in assuring the most reliable automatic reading of the alphanumeric marking.

R1-1.2 *Character Stroke Thickness* — If a 5 × 9 dot matrix is chosen for marking, it is recommended that the minimum dot size be 0.100 mm. With a higher density dot matrix format, smaller dot diameters may be employed. Stroke thickness should be constant within 20% over the entire character set so that the reader settings may be optimized from the specific wafer run.

R1-1.3 *Contrast* — The character should have sufficient contrast to be legible. Contrast may be affected by depth and other conditions.

R1-1.4 *Clear Zone* — It is recommended that the area immediately beneath, and a minimum of 0.500 mm around, the marking characters be of uniform reflectivity and free of any lithography and process overlay edges.

NOTICE: SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copyrighted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI M14-89
SPECIFICATION FOR ION IMPLANTATION AND ACTIVATION PROCESS FOR SEMI-INSULATING GALLIUM ARSENIDE SINGLE CRYSTALS

1 Scope

The purpose of this document is to present a process for ion implantation, activation, and measurement of the resulting layers so that meaningful comparisons can be made between various lots of semi-insulating GaAs. This test will be performed by the supplier so that product may be represented in a standard way.

NOTE: This is intended to be an interim procedure for use until a standard test method is developed by ASTM.

2 Process

2.1 Candidate lots must pass SEMI GaAs specifications for resistivity, mobility, and thermal stability using standard ASTM referee techniques.

2.2 *Implantation Process*

2.2.1 *Surface Preparation* — The surface treatment shall be designed to remove residual oxide.

2.2.2 *Implant Angle Energy Species and Dose* — An energy of 150 keV using Si_{29} to a dose of $2 \times 10^{12}/cm^2$ and a tilt of 11° to 13° from the (100) toward the (110).

2.3 *Activation Process*

2.3.1 *Surface Preparation* — No chemical treatment should be performed prior to activation.

2.3.2 *Activation* — The samples shall be subjected to a temperature of 850°C for 10 minutes with a second proximity wafer directly in contact with the implanted surface. The proximity wafer shall be identical to the subject wafer except not subjected to ion implantation. The ambient of the furnace shall be a gas such as nitrogen or argon.

2.4 *Layer Evaluation*

2.4.1 Evaluation of the activated samples shall be based upon CV profiling, mobility, and resistivity as specified according to standard ASTM techniques.

SEMI M15-0298
POLISHED WAFER DEFECT LIMITS TABLE FOR SEMI-INSULATING GALLIUM ARSENIDE WAFERS

NOTE: This entire document was revised in 1998.

1 Purpose

1.1 This document defines the maximum number of defects, by type, that an acceptable polished Semi-Insulating Gallium Arsenide (GaAs) wafer may exhibit.

2 Scope

2.1 This document, established separately from SEMI M15, in accordance with the latest requirements for the material in advanced applications, covers polished semi-insulating GaAs wafers. The defect limits table can also be applied to conducting GaAs wafers, except for the specification of Light Point Defects (LPD) mentioned hereinafter. "Polished" shall refer to those wafers which have a specular chemical or chemical/mechanical finish applied to one side of the wafer, with the backside being as cut and etched, lapped and etched, ground and etched, or polished. The definition of defects is covered in ASTM Practices F 523 and F 154.

3 Referenced Documents

3.1 *ASTM Standards*[1]

F 154 — Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

F 523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

Table 1 Polished Wafer Defect Limits

Item #	*Characteristics — Front Surface*	*Maximum Defects Limits Prime Wafer*	*Maximum Defects Limits Test Wafer*	*Notes*
1	Scratches			
	Macroscratches	None		#1
	Maximum Number	----	3	
	Maximum Length	----	Radius/2	
	Microscratches	None	Not Specified	#1, 2
2	Pits			#1, 2
	2" Diameter Slices	None	5	
	3" Diameter Slices	None	15	
	4" Diameter Slices	None	30	
3	Haze	None	None	#1, 2
4	Cavity/Voids	None	None	#1
5	Contamination	None	None	#1, 2
6	Light Point Defects $\geq \phi$ 2.0 μm			
	2" Diameter Slices	10	20	#2, 3
	3" Diameter Slices	15	30	#2, 3
	4" Diameter Slices	20	40	#2, 3
	Light Point Defects $\geq \phi$ 3.0 μm			
	2" Diameter Slices	50	100	#2, 3
	3" Diameter Slices	100	200	#2, 3

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959

18				
	4" Diameter Slices	200	400	#2, 3
7	Chips (≥ 0.5 mm × 0.3 mm)	None	None	#1
8	Cracks	None	None	#1
9	Dimples	None	None	#1, 2
10	Gallium Inclusions/Precipitates	None	None	#1, 2
11	Orange Peel	None	None	#1, 2
12	Saw Marks	None	None	#1
13	Striations	None	None	#1, 2
14	Twins	None	None	#1, 2

Item #	*Characteristics – Back Surface*	*Maximum Defect LimitsPrime Wafer*	*Maximum Defect LimitsTest Wafer*	*Notes*
15	Stain	None	None	#2, 4
16	Saw Marks	None	None	#1, 5
17	Chips (≥ 0.5 mm × 0.3 mm)	None	None	#1
18	Cracks	None	None	#1
19	Listed Defects #10, 14	None	None	#1, 2
20	Listed Defects #1, 2, 6			#6

NOTES:

1. These defect limits are meant to apply only to those characteristics which can be seen with the unaided eye under high-intensity illumination according to ASTM Practice F 523. Limits for other defects listed and defined in this section which require the aid of a microscope, preferential etching, or other apparatus must be agreed upon between supplier and user.

2. Peripheral Edge Allowance — The outer edge exclusion for observation shall be determined from the following tabe:

Diameter	*Outer Edge Exclusion for Observation*
2 inch	2 mm
3 inch	3 mm
4 inch	3 mm

3. LPD shall be counted by measuring equipment designed for detecting laser light scatter. Selection of the measuring equipment and the requirement for the precision are to be agreed upon between supplier and user.

4. Back Surface Stain — An area of undercutting, texturing, or oxidation, common in waxless polished wafers.

5. The depth of allowed saw marks is to be no greater than 5 µm. The measuring method is to be agreed upon between supplier and user.

6. Item #20 — To be agreed upon between supplier and user.

SEMI M16-1103
SPECIFICATION FOR POLYCRYSTALLINE SILICON

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on September 16, 2003. Initially available at www.semi.org October 2003; to be published November 2003. Originally published in 1989; previously published December 1996.

NOTICE: This document was rewritten in its entirety in 2003, and is a replacement for the previous versions of both SEMI M16 and SEMI M16.1.

1 Purpose

1.1 This specification is intended for use in procurement of polycrystalline silicon for growth of electronic grade monocrystalline silicon ingots. Such ingots are sliced into wafers that are subsequently used for the production of semiconductor devices, integrated circuits, and other microelectronic components including microelectromechanical systems (MEMS).

2 Scope

2.1 This specification covers requirements for polycrystalline silicon (poly) used to produce single crystal silicon by either the modified Czochralski (Cz) or float zone (FZ) crystal growth technique for applications in the semiconductor device industry.

2.2 Form and dimensional characteristics are the only standardized properties set forth below. A purchase specification may include requirements for additional physical properties as listed in this specification, together with test methods suitable for determining their magnitudes.

NOTE 1: JEITA has also established a specification for polysilicon.[1] This specification also includes specification limits and specified measurement methods for purity and surface metal contamination. Similarities and differences between this standard and JEITA EM-3601 are discussed in Related Information 1.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI MF1708 — Practice for Evaluation of Granular Polysilicon by Melter-Zoner Techniques

SEMI MF1723 — Practice for Evaluation of Polycrystalline Silicon Rods by Float-Zone Crystal Growth and Spectroscopy

SEMI MF1724 — Test Method for Measuring Surface Metal Contamination of Polycrystalline Silicon by Acid Extraction-Atomic Absorption Spectroscopy

3.2 *ASTM Standards*[2]

E 122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

3.3 *Other Standard*

ANSI/ASQC Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes[3]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Definitions*

4.1.1 *etched polysilicon* — polysilicon that has been etched with acid to remove surface contamination.

4.1.2 *lot* — all of the material of nominally identical purity and characteristics contained in a single shipment, manufactured with similar processing conditions, and traceable to the manufacturing conditions. A lot may be further defined as the polysilicon produced from one reactor run.

4.1.3 *polycrystalline silicon* — silicon, formed by chemical vapor deposition from a silicon source gas, having a structure that contains large angle grain boundaries, twin boundaries, or both. Also known as *poly*, or *polysilicon*.

1 JEITA EM-3601, Standard specification for high purity polycrystalline silicon. Available in Japanese and English from Japan Electronics and Information Technology Industries Association, 3rd floor, Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan, Web site: www.jeita.or.jp

2 Volume 14.02 of the *Annual Book of ASTM Standards*, ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555, Web site: www.astm.org

3 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202, USA. Web site: www.asqc.org.

5 Ordering Information

5.1 Purchase orders for polysilicon furnished to this specification shall include the following items:

5.1.1 Form (nugget, granular, or rod)

5.1.2 Shape and size distribution (nugget form only)

5.1.3 Purity

5.1.4 Surface texture (nugget form only)

5.1.5 Surface condition

5.1.6 Optionally, surface metal contamination

5.1.7 Appearance

5.1.8 Lot acceptance procedures (see Section 8)

5.1.9 Certification (if required) (see Section 10)

5.1.10 Packing and marking (see Section 11)

6 Materials and Manufacture

6.1 The material shall consist of polysilicon with the form specified in the purchase order or contract.

7 Physical Requirements

7.1 The material shall conform to the properties specified in the purchase order or contract, as follows (see Table 1):

7.1.1 Shape and size distribution (nugget form only)

7.1.2 Purity

7.1.3 Surface texture (nugget form only)

7.1.4 Surface condition

7.1.5 Surface metal contamination, if specified

7.1.6 Appearance

8 Sampling

8.1 Unless otherwise specified, ASTM Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4-1993. Inspection levels shall be agreed upon between the supplier and the purchaser.

9 Test Methods

9.1 *Shape and Size Distribution (Nugget Form Only)* — Determine by methods agreed upon by the purchaser and the supplier.

9.2 *Purity* — For nugget and rod forms, determine in accordance with SEMI MF1723. For granular form, determine in accordance with SEMI MF1708.

9.3 *Surface Texture (Nugget Form Only)* — Determine by a method agreed upon by the purchaser and the supplier. Visual limit standards shall be used to describe acceptable limits.

9.4 *Surface Metal Contamination, if Specified* — Determine in accordance with SEMI MF1724.

9.5 *Surface Condition* — Identify as to whether or not the surface has been etched.

9.6 *Appearance* — Inspect visually for stains, discoloration, and visible contamination.

10 Certification

10.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with the specification shall be furnished at the time of shipment (Certificate of Compliance). Upon request, a report of the test results may also be required (Certificate of Analysis).

10.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate test in Section 9. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

11 Packing and Marking

11.1 Special packing requirements shall be subject to agreement between the supplier and purchaser. Otherwise all poly shall be handled, inspected, and packed in bags and boxes in such a manner as to minimize abrasion, chipping, and contamination, and in accordance with the best industry practices to provide ample protection against damage during shipment.

11.2 The poly supplied under the specification shall be identified by appropriately labeling the outside of each box and each bag therein. Identification shall include, as a minimum, the weight and lot number of the polysilicon. The lot number shall provide traceability to information concerning the manufacturing history of the particular poly in that lot. Such information shall be kept on file at the manufacturer's facility for at least three years after that particular lot has been accepted by the purchaser.

12 Related Documents

12.1 The following SEMI standards, cited in SEMI MF1708 and MF1723 are required to perform the tests described in those practices:

SEMI MF1389 — Test Methods for Photoluminescence Analysis of Single Crystal Silicon for III-V Impurities

SEMI MF1391 — Test Method for Substitutional Carbon Content of Silicon by Infrared Absorption

SEMI MF1630 — Test Method for Low Temperature FT-IR Analysis of Single Crystal Silicon for III-V Impurities

SEMI MF1725 — Guide for Analysis of Crystallographic Perfection of Silicon Ingots

Table 1 Requirements for Polysilicon

Property	*Nugget Form (previously SEMI M16.1)*	*Granular Form*	*Rod Form*
Shape	Irregular chunks, crushed from polysilicon rods, with maximum linear dimension of 150 mm.	As supplied; Polysilicon granules are nearly spherical in shape and range in size from 200 to 2500 μm with a mean size of about 900 μm.	Approximately cylindrical polycrystalline rods, with length equal to or greater than the diameter of the rod.
Size Distribution	As specified by customer.	Not applicable.	Not applicable.
Purity			
Acceptor concentration, max in parts per billion, atomic (ppba)	As specified by customer.	As specified by customer.	As specified by customer.
Donor concentration, max in parts per billion, atomic (ppba)	As specified by customer.	As specified by customer.	As specified by customer.
Carbon concentration, max in parts per million, atomic (ppma)	As specified by customer.	As specified by customer.	As specified by customer.
Evaluate in accordance with	SEMI MF1723	SEMI MF1708	SEMI MF1723
Surface Texture	Visual limit standards as agreed upon between supplier and purchaser.	Not applicable.	Not applicable.
Surface Condition	Identified as to whether or not the nuggets have been etched.	As agreed upon between supplier and purchaser.	Identified as to whether or not the rods have been etched.
Surface Metal Contamination, if specified	Sodium, Aluminum, Iron, Chromium, Copper, Nickel, Potassium, and Zinc, as specified, from thin surface layer on the sample, determined in parts per billion by weight (ppbw) in accordance with SEMI MF1724.		
Appearance	Clean with no stains, discoloration, or visible contamination.	As agreed upon between supplier and purchaser.	Clean with no stains, discoloration, or visible contamination.

RELATED INFORMATION 1
RELATIONSHIPS BETWEEN THE REQUIREMENTS OF SEMI M16 AND THE REQUIREMENTS OF JEITA EM-3601

NOTICE: This related information is not an official part of SEMI M16. It was developed during the revision of the document in May 2003. This related information was approved for publication by full letter ballot on September 19, 2003.

R1-1 Introduction

R1-1.1 SEMI M16 and JEITA EM-3601 both provide specification requirements for polycrystalline silicon (poly) in nugget (chunk), granular, and rod forms.

R1-1.2 This related information section provides comparisons between the two specifications with regard both to the specification requirements and to the test methods cited.

R1-2 Specification Requirements

R1-2.1 The philosophies of the two specifications are quite different in that JEITA EM-3601 spells out specific purity requirements, while SEMI M16 leaves these to be "as specified by the customer." The levels specified in JEITA EM-3601 may serve as a starting point for developing the necessary specifications.

R1-2.2 *Purity Requirements*

R1-2.2.1 JEITA EM-3601 lists the following bulk purity requirements for the nugget and rod forms:

R1-2.2.1.1 Acceptor concentration, maximum:

- B 0.05 ppba
- Al 0.05 ppba

R1-2.2.1.2 Donor concentration, maximum:

- P 0.3 ppba
- As 0.05 ppba

R1-2.2.1.3 Carbon concentration, maximum:

- C 0.3 ppma

R1-2.2.2 JEITA EM-3601 lists the following bulk purity requirements for the granular form:

- Total acceptors (B+ Al) 0.1 ppba, maximum
- Total donors (P+ As) 0.4 ppba, maximum
- Carbon 0.3 ppma, maximum

R1-2.2.3 JEITA EM-3601 lists the following surface metal contamination requirements for the nugget and granular forms (maximum surface metal contamination levels are not listed for the rod form):

- Fe, Cr, Ni, and Na 3.0 ppbw, maximum
- Zn 1.0 ppbw, maximum

NOTE 2: These surface metal concentrations correspond to 1.5 ppba for Fe, Cr, and Ni; 3.8 ppma for Na; and 0.5 ppba for Zn.

R1-2.3 *Size Distribution* — See Tables R1-1 through R1-3.

Table R1-1 Size Requirements for Nugget Form Poly

	JEITA EM-3601	*SEMI M16*
Maximum Dimension	120 mm	150 mm
Minimum Dimension	10 mm	not specified

Table R1-2 Size Requirements for Granular Form Poly

	JEITA EM-3601	*SEMI M16*
Maximum Size	3,500 μm	2,500 μm
Minimum Size	150 μm	200 μm
Mean Size	not specified	~ 900μm

Table R1-3 Size Requirements for Rod Form Poly

	JEITA EM-3601	*SEMI M16*
Minimum Length	not specified	rod diameter

R1-3 Test Method Requirements

R1-3.1 *Sample Preparation*

R1-3.1.1 JEITA EM-3601 contains instructions for preparing samples for photoluminescence, infrared absorption, and atomic absorption spectroscopy measurements. It cites the 1996 edition of JIS H 0615 for the preparation of samples from nugget and rod forms for photoluminescence measurements.

R1-3.1.2 SEMI M16 specifies that samples for photoluminescence and infrared measurements are to be prepared from nugget and rod forms in accordance with SEMI MF1723 and from granular form in accordance with SEMI MF1708. Samples for atomic absorption spectroscopy measurements are to be prepared in accordance with SEMI MF1724.

R1-3.1.3 The preparation procedures are generally similar, except that JIS H 0615 allows coring only perpendicular to the rod filament, but SEMI MF1723 permits coring parallel with the rod filament in addition to perpendicular to the rod filament.

R1-3.2 *Measurement Procedures*

R1-3.2.1 The photoluminescence technique is specified for measurement of donor and acceptor concentrations in both JEITA EM-3601 and in SEMI M16 (through reference to SEMI MF1723); the latter also allows this determination by low temperature FT-IR analysis. The photoluminescence technique is covered in SEMI MF1389 and in JIS H 0615. The latter, specified in JEITA EM-3601, allows only the high excitation condition for the photoluminescence analysis while the former allows either high or low excitation.

R1-3.2.2 The infrared absorption method is specified for the carbon determination in both SEMI M16 and JEITA EM-3601. The two cited test methods, SEMI MF1391, specified in SEMI M16 (through reference to SEMI MF1723), and JEITA EM-3503, cited in JEITA EM-3601, are essentially equivalent.

R1-3.2.3 Atomic absorption spectroscopy is specified for the surface metal contamination in both SEMI M16 and JEITA EM-3601. The two cited test methods, SEMI MF1724, specified in SEMI M16, and JIS K 0121, cited in JEITA EM-3601, are essentially equivalent insofar as the actual measurement is concerned, but SEMI MF1724 also standardizes the sampling procedures, etching solutions, and method of collecting the impurities in much greater detail.

SEMI M17-0704
GUIDE FOR A UNIVERSAL WAFER GRID

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on April 22, 2004. Initially available at www.semi.org May 2004; to be published July 2004. Originally published in 1990; previously published September 1998.

1 Purpose

1.1 Maximum allowable slip and other non-uniformly distributed defects are frequently specified when procuring polished and epitaxial silicon wafers. SEMI M2 specifies a maximum allowable fraction of the epitaxial wafer surface area that can contain slip.

1.2 This guide provides a design for and guidance for use of a wafer grid that facilitates the determination of the fraction of the wafer surface area covered by observed defects.

2 Scope

2.1 This document defines a grid pattern that is useful for quantifying surface defects on a nominally circular semiconductor wafer. The grid is defined such that it contains 1000 elements of approximately equal area. Each grid element thus contains 0.1 percent of the total quality area of the surface being inspected. Defects that are non-uniformly distributed (for example, slip) can be quantified in terms of the percent defective (or percent useful) area on the wafer surface.

2.2 The grid described is referenced to the center of the wafer. A concept of a "Fixed Quality Area" is used, based on nominal wafer diameter, such as is specified in SEMI M1.

2.3 Methods for observing these defects on silicon wafer surfaces are outside the scope of this guide. Such methods may be found in SEMI MF1725, SEMI MF1726, JIS H 0609, and DIN 50434.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M2 — Specifications for Silicon Epitaxial Wafers for Discrete Device Applications

SEMI MF154 —Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF1241 — Terminology of Silicon Technology

SEMI MF1725 — Practice for Analysis of Crystallographic Perfection of Silicon Ingots

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1809 — Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon

3.2 *Japan Industrial Standard*[1]

JIS H 0609 — Test methods of crystalline defects in silicon by preferential etch techniques

3.3 *DIN Standard*[2]

50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on { 111} and { 100} Surfaces

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions for many surface defects are given in SEMI MF1241. Additional information and illustrations of various surface defects are provided in SEMI MF154, SEMI MF1809, and JIS H 0609.

5 Grid Element Layout

5.1 *Grid Element Scheme*

5.1.1 Two types of grids are defined: one for wafers without a primary flat (for example, wafers where the primary fiducial is a notch), and one for wafers with a primary flat. The grid is divided by 18 concentric circles containing radial divisions which are assigned according to the diameter of each circle (see Table 1). The relative diameters of the concentric circles are established by the areas of each annulus. To find the

1 Available, in Japanese language edition only, through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp

2 Available from Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, website: www.din.de

actual diameter of any circle, multiply the relative diameter by the outer diameter of the grid.

5.1.2 The outer diameter of the grid is chosen to be the size appropriate for a particular application. This diameter would normally be chosen to be the nominal diameter of the fixed quality area to allow for such things as an edge exclusion, tolerance variations in the wafer diameter, and edge rounding. Table 2 shows the circle diameters for a series of grids which have a fixed quality area radius 3 or 4 mm smaller than the nominal radius of selected wafers specified in SEMI M1.

5.1.3 Identification of each grid element is done by referring to a circle number and a division number on that circle. Circles are numbered from the center out, with the center circle being number 01 and the outermost circle being number 18. The divisions are numbered starting with the first division counterclockwise from the horizontal line which starts at the center of the grid and extends to the right, when the primary fiducial (flat or notch) is placed at the bottom of the grid. Divisions are progressively numbered counterclockwise from 01 to *n*, where *n* equals the total number of divisions on the circle. An element's address is given by two sets of numbers separated by a comma: circle (0–18), division (01–*n*). Elements 18, 01 and 18, 100 are identified in Figure 1.

5.2 *Wafers without a Primary Flat*

5.2.1 The grid elements for wafers without a primary flat are illustrated in Figure 1. This pattern is generated by making concentric circles with relative diameters and radial divisions as specified in Table 1. In this table the circle number is given in the leftmost column. The number of divisions and the included angle of each division in the circle are given in the second and third columns. The total number of divisions (from the center outward) is given in the fourth column. The included area ratio, given in the fifth column, is the total number of divisions included within a circle divided by 1000, the total number of divisions in the grid. The relative diameter, given in the rightmost column, is the square root of the included area ratio.

5.3 *Wafers with a Primary Flat*

5.3.1 For wafers with a primary flat, a standard included angle of 43.2° is used for all wafer sizes. This angle was chosen because it lies between the maximum and minimum included angles of the primary flats specified in SEMI M1 for 100 mm, 125 mm, 150 mm, and 200 mm diameter wafers. In addition, if a fixed quality area of radius 3 mm less than the nominal wafer radius (or smaller) is used, the grid will not in any case extend beyond the edge of the wafer in the region of the primary flat.

5.3.2 This flat is propagated into the wafer as illustrated in Figure 2. The diameter of each circle is the same as for wafers without a primary flat. The flat is propagated vertically downward (starting with circle number 3) by the intersection of the circle with a horizontal chord which subtends 43.2° .

5.3.3 The areas of the grid elements within the propagated flat region are slightly smaller than the areas of the regular grid elements. This difference is ignored when counting grid elements for wafers with a primary flat. All grid elements are assumed to be 0.001 of the total fixed quality area.

5.4 *Secondary Flats*

5.4.1 The grid ignores secondary flats. These are shallow enough that the outer circle does not extend beyond the wafer edge if a fixed quality area of radius 3 mm less than the nominal wafer radius is used.

NOTE 1: In this sense, the fixed quality area used by the Universal Wafer Grid deviates somewhat from the formal definition in SEMI M1 which embodies an edge exclusion of constant width around the entire periphery of the wafer including the region of the secondary flat.

6 Use of the Grid

6.1 The quantification of defective area is done by overlaying a transparency of the grid onto a map of wafer defects or by mapping observed defects onto the grid. The number of grid elements which contain defects is counted. The element count divided by 10 corresponds to the percent of defective area. This grid could also be superimposed onto a CRT display, photograph, or computer generated map, where applicable. In use, grid pattern diameters must be scaled to the size of the map or image of the wafer to be overlaid.

Table 1 Grid Element Scheme

Circle Number	*Number of Divisions*	*Included Angle*	*Total Number of Divisions*	*Included Area Ratio*	*Relative Diameter*
01	4	90.0°	4	0.004	0.0632
02	8	45.0°	12	0.012	0.1095
03	16	22.5°	28	0.028	0.1673
04	24	15.0°	52	0.052	0.2280
05	30	12.0°	82	0.082	0.2864
06	36	10.0°	118	0.118	0.3435
07	40	9.0°	158	0.158	0.3975
08	48	7.5°	206	0.206	0.4539
09	50	7.2°	256	0.256	0.5060
10	60	6.0°	316	0.316	0.5621
11	72	5.0°	388	0.388	0.6229
12	72	5.0°	460	0.460	0.6782
13	80	4.5°	540	0.540	0.7348
14	80	4.5°	620	0.620	0.7874
15	90	4.0°	710	0.710	0.8426
16	90	4.0°	800	0.800	0.8944
17	100	3.6°	900	0.900	0.9487
18	100	3.6°	1000	1.000	1.0000

Table 2 Grid Circle Diameters (in mm) for Various Standard Wafer Sizes with Nominal Edge Exclusion, *E*.

Circle Number	*Relative Diameter*	*Nominal Wafer Diameter*					
		E = 3 mm				*E = 4 mm*	
		100 mm	*125 mm*	*150 mm*	*200 mm*	*150 mm*	*200 mm*
01	0.0632	5.94	7.52	9.10	12.26	8.97	12.13
02	0.1095	10.29	13.03	15.77	21.24	15.55	21.02
03	0.1673	15.73	19.91	24.09	32.46	23.76	32.12
04	0.2280	21.43	27.13	32.83	44.23	32.38	43.78
05	0.2864	26.92	34.08	41.24	55.56	40.67	54.99
06	0.3435	32.29	40.88	49.46	66.64	48.78	65.95
07	0.3975	37.37	47.30	57.24	77.12	56.45	76.32
08	0.4539	42.67	54.01	65.36	88.06	64.45	87.15
09	0.5060	47.56	60.21	72.86	98.16	71.85	97.15
10	0.5621	52.84	66.89	80.94	109.05	79.82	107.92
11	0.6229	58.55	74.13	89.70	120.84	88.45	119.60
12	0.6782	63.75	80.71	97.66	131.57	96.30	130.21
13	0.7348	69.07	87.44	105.81	142.55	104.34	141.08
14	0.7874	74.02	93.70	113.39	152.76	111.81	151.18
15	0.8426	79.20	100.27	121.33	163.46	119.65	161.78
16	0.8944	84.07	106.43	128.79	173.51	127.00	171.72
17	0.9487	89.18	112.90	136.61	184.05	134.72	182.15
18	1.0000	94.00	119.00	144.00	194.00	142.00	192.00

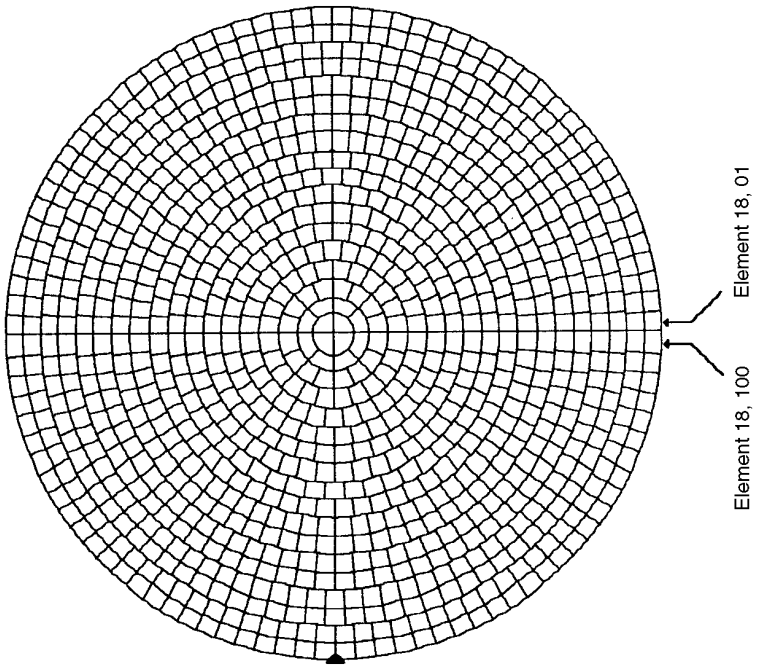

Figure 1
Grid Layout for Wafers Without a Primary Flat

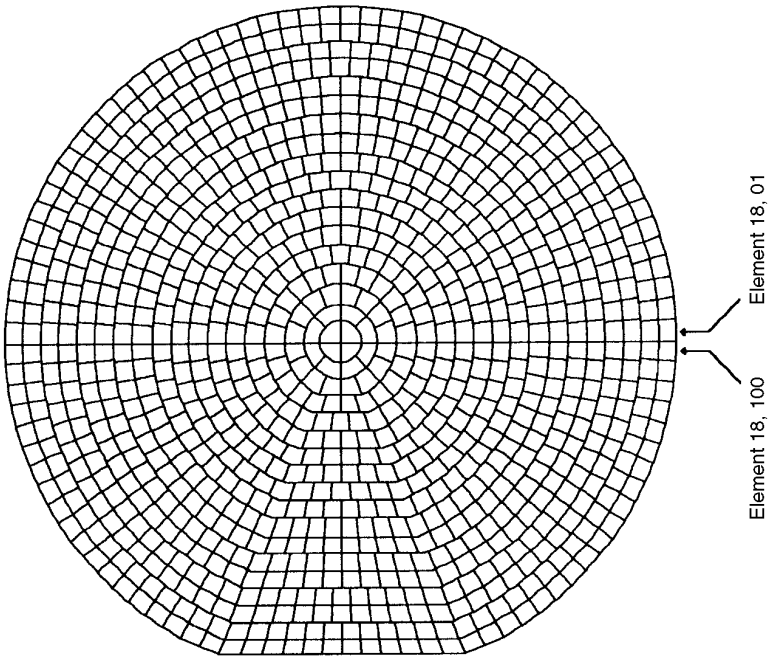

Figure 2
Grid Layout for Wafers With a Primary Flat

NOTICE: SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copyrighted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI M18-0704
FORMAT FOR SILICON WAFER SPECIFICATION FORM FOR ORDER ENTRY

This format was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved by the Japanese Regional Standards Committee on April 30, 2004. Initially available at www.semi.org June 2004; to be published July 2004. Originally published in 1990; last published March 2004.

1 Purpose

1.1 This format provides a standard form for specifying several classifications of silicon wafers, as follows:

1.1.1 Polished Silicon Wafers.

1.1.2 Epitaxial Silicon Wafers.

1.1.3 Epitaxial Silicon Wafers with Buried Layer.

1.1.4 Annealed Silicon Wafer.

1.1.5 SOI Wafers for CMOS Applications.

1.2 This format also lists the Electronic Data Interchange (EDI) codes used in SEMI T6 to identify the type of data being reported in the EDI message.

2 Scope

2.1 The form is designed to be used in conjunction with other SEMI specifications where details of the dimensional, physical, electrical, and chemical properties are defined or specified. However, the form includes many items that are not currently included in the SEMI specifications. Also, many items are not now commonly specified, but may find increased importance in the future. The intention is to provide for flexibility and expansion of the technology.

2.2 This format provides for specifying and ordering silicon wafers with varying levels of complexity. The minimum level of completeness is shown in each case, with additional options included to allow for customization of the wafer to the specific processing requirements of the user. If a particular item is not of interest, no entry is required. The only required entries are those marked as such for the purpose of minimal specification (diameter, orientation, dopant, resistivity, etc.).

2.3 Values for many items are listed either in the polished silicon wafer standards in SEMI M1 or in the defect limits tables in SEMI M1, SEMI M2, or SEMI M11. If these standard specifications are sufficient for defining the wafers, only a single entry is required in each section of the form.

2.4 This format also lists the codes required by SEMI T6 to identify the parameter being reported in the EDI message. Where necessary, secondary characteristics or identifier codes are listed within a generalized characteristic.

2.5 For referee purposes, U.S. Customary units shall be used for wafers of 2- and 3-inch diameters, and SI (System International, commonly called metric) units for 100 mm and larger diameter wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M2 — Specifications for Silicon Epitaxial Wafers for Discrete Device Applications

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Integrated Circuit (IC) Applications

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specifications for Alphanumeric Marking of Silicon Wafers

SEMI M20 — Specification for Establishing a Wafer Coordinate System

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M47 — Specification for Silicon-on-insulator (SOI) Wafers for CMOS LSI Applications

SEMI MF26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF28 — Test Method for Minority-Carrier Lifetime in Bulk Germanium and Silicon by Measurement of Photoconductive Decay

SEMI MF42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF81 — Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Probe Array

SEMI MF95 — Test Method for Thickness of Lightly Doped Silcon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

SEMI MF110 — Test Metod for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Standard Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-implanted Layers Using and In-Line Four-Point Probe

SEMI MF391 — Standard Test Methods for Minority-Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wave Number or Wavelength of the Plasma Resonance Minimum.

SEMI MF523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surface

SEMI MF525 — Test Method Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF533 — Standard Test Method for Thickness and Thickness of Variation of Silicon Wafers

SEMI MF534 — Standard Test Method for Bow of Silicon Wafers

SEMI MF657 — Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

SEMI MF671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Material

SEMI MF672 — Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe

SEMI MF673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

SEMI MF723 — Practice for Conversion Between Resisitivity and Dopant Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon.

SEMI MF847 — Standard Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF951 — Test Method for Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF978 — Standard Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

SEMI MF1049 — Standard Practice for Shallow Pit Detection on Silicon Wafers

SEMI MF1152 — Standard Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

SEMI MF1239 — Standard Test Methods for Oxygen Precipitation Characterization of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1241 — Standard Terminology of Silicon Technology

SEMI MF1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1388 — Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors

SEMI MF1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1391 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1393 — Test Metod for Determining Net Carrier Density Profile in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1451 — Standard Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1526 — Standard Test Method for Measuring Surface Metal Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy

SEMI MF1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1528 — Test Method for Measuring Boron Contamination in Heavily Doped N-Type Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1535 — Standard Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

SEMI MF1617 — Standard Test Method for Measuring Surface Sodium, Aluminum, and Potassium on Silicon and EPI Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1619 — Standard Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle

SEMI MF1620 — Standard Practice for Calibrating a Scanning Surface Inspection System Using Monodisperse Polystyrene Latex Spheres Deposited on Polished or Epitaxial Surfaces

SEMI MF1621 — Standard Practice for Determining Positional Accuracy Capabilities of a Scanning Surface Inspection System

SEMI MF1725 — Standard Guide for Analysis of Crystallographic Perfection of Silicon Ingots

SEMI MF1726 — Standard Guide for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

SEMI MF1810 — Test Method for Counting Preferentailly Etched or Decorated Structural Defects on Silicon Wafers

SEMI MF1982 — Test Method for Analyzing Organic Contamination on Silicon Wafers Surfaces by Thermal Desporption Gas Chromatography

SEMI T1 — Specification for Back Surface Bar Code Marking of Silicon Wafers

SEMI T2 — Specification for Marking of Wafers with a Two-Dimensional Matrix Code Symbol

SEMI T6 — Procedure and Format for Reporting of Test Results by Electronic Data Interchange (EDI)

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *ANSI Standard*[1]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standards*[2]

D 523 — Standard Test Method for Specular Gloss

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

F 416 — Standard Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers

F 419 — Test Method for Determining Carrier Density in Silicon Epitaxial Layers by Capacitance-Voltage Measurement on Fabricated Junction of Schottky Diodes

F 613 — Standard Test Method for Measuring Diameter of Semiconductor Wafers

3.4 *DIN Standards*[3]

NOTE 1: DIN Standards are available in both German and English editions. ASTM equivalents are given in square brackets following the title.

50431 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Colinear Four-Probe Array

50432 — Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot-Probe

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1 American National Standards Institute, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023 Website: www.ansi.org

2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

3 Available from Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, website: www.din.de

50433/1 — Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction

50433/2 — Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure

50433/3 — Determination of the Orientation of Single Crystals by Means of Laue Back Scattering

50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

50435 — Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four-Point-DC-Probe

50436 — Measurement of Metallurgical Thicknes of Epitaxial Layers of Silicon by the Stacking Fault Method

50437 — Measuring the Thickness of Silicon Epitaxial Layers of Silicon by Infrared Intereference Method [F95]

50438/1 — Determination of Impurity Content in Silicon by Infrared Absorption: Oxygen

50438/2 — Determination of Impurity Content in Silicon by Infrared Absorption: Carbon

50439 — Determination of the Dopant Concentration Profile of Single Crystalline Semiconductor Material by Means of the Capacitance-Voltage Method and Mercury Contact [F 1392, F 1393]

50438/3 — Determination of Impurity Content in Silicon by Infrared Absorption: Boron and Phosphorus

50440/1 — Measurement of Recombination Carrier Lifetime in Silicon Single Crystals by Means of Photoconductive Decay Method; Measurement on Bar-Shaped Test Samples [F28]

50441/1 — Determination of the Geometric Dimensions of Semiconductor Slices: Measurement of Thickness

50441/2 — Determination of the Geometric Dimensions of Semiconductor Slices: Testing of Edge Rounding

50441/3 — Measurement of the Geometric Dimensions of Semiconductor Slices; Determination of Flatness Deviation of Polished Slices by Means of Multiple Beam Interference

50441/4 — Determination of the Geometrical Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices

50443/1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-Ray Topography: Silicon

50444 — Conversion Between Resistivity and Dopant Density; Silicon [F723 (phosphorous and boron only)]

50445 — Contactless Determination of the Electrical Resistivity of Semiconductor Wafers with the Eddy Current Method

50446 — Determination of Defect Types and Defect Densities of Silicon Epitaxial Wafers [no direct ASTM equivalent, compare F 1726 and associated standards]

3.5 *ISO Standards*[4]

ISO 4287/1 — Surface Roughness – Terminology – Part 1: Surface and its Parameters

ISO 14644/1-7 — Clean Room and Associated Controlled Environments

3.6 *JEITA (formerly JEIDA) Standards*[5]

43 — Terminology of Silicon Wafer Flatness

53 — Test Method for Recombination Lifetime in Silicon Wafers by Measurement of Photoconductivity Decay by Microwave Reflectance

56 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

61— Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

EM-3602 — Determining the Orientation of a Semiconductor Silicon Single Crystal

EM-3501 — Standard Specification for Dimensional Properties of Silicon Wafers with Specular Surface

EM-3505 — Height calibration in 1nm order for AFM

3.7 *JIS Standards*[6]

NOTE 2: ASTM equivalents are given in square brackets following the title.

H 0602 — Testing Method of Resistivity for Silicon Crystals and Silicon Wafers with Four-Point Probe

H 0604 — Measurement of Minority Carrier Life Time in Silicon by Photoconductive Decay Method [F 28]

H 0607 — Testing Methods for Conductivity Type of Semiconductor Materials

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4 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch

5 Japanese Electronic and Information Technology Industries Association, Tokyo Chamber of Commerce and Industry Bldg. 2-2, Marunouchi 3-chome, Chiyoda-ku, Tokyo 100-0005, Japan. Website: www.jeita.or.jp

6 Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp

H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

H 0611 — Methods of Measurement of Thickness, Taper, and Bow of Silicon Wafers

H 0612 — Testing Method of Resistivity for Single Crystal Silicon Wafers (with Four Point Probe) [F 84]

H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

Z 8741 — Method of Measurement for Specular Glossiness

3.8 *Other Standard*[7]

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 The items listed in the form are referenced and defined in various documents. A reference for most items in Parts 2 and 3 of the form is listed in Table 1. The entries in the table are keyed to the form by item number. Because terms related to epitaxial wafers with buried layer are defined in this standard and because no standardized test methods for the buried layer parameters exist, Table 1 does not include line items from Part 4 of the form.

4.2 General term used in this standard:

4.2.1 *required (req. or req'd)* — when applied to a parameter listed in the order form, a user-supplied value is necessary to minimally define the material for manufacture.

4.3 Terms related to epitaxial wafers with buried layers:

4.3.1 *buried layer* — a diffused region in a substrate that is, or is intended to be, covered with an epitaxial layer.

4.3.2 *alignment precision* — pattern displacement in first mask photolithography process.

NOTE 3: Alignment precision is specified by maximum values of X and Y, the displacement of the center of the pattern from a reference position defined in the wafer specification in terms of the wafer coordinate system defined in SEMI M20, and the maximum value of θ, the angle between the x-axis of the pattern and the primary orientation flat (see Figure 1).

4.3.3 *pattern distortion ratio* — absolute magnitude of the quotient of the (1) difference between the width of the pattern on the substrate and the width of the pattern on the top surface of the epitaxial layer and (2) the thickness of the epitaxial layer.

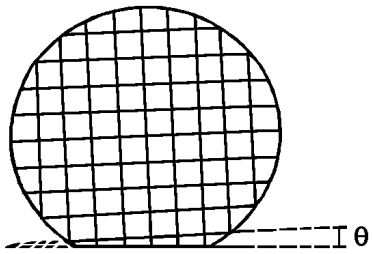

Figure 2
First Mask Showing Angular Displacement θ

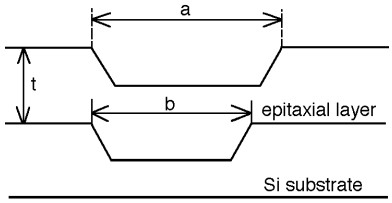

Figure 3
Cross-Section View of Epitaxial Layer Showing the Pattern Widths, *a*, at the Epi Surface, and *b*, at the Layer-Substrate Interface

4.3.4 *pattern shift ratio* — lateral distance between the center point of the pattern on the surface of the substrate and the center point of the pattern on the surface of the epitaxial layer divided by the epitaxial layer thickness.

NOTE 4: Pattern shift ratio, *d/t* (see Figure 4), is specified in terms of a nominal value, *X*, and a tolerance, ± *Y*, both of which are dimensionless because both *d* and *t* are in μm.

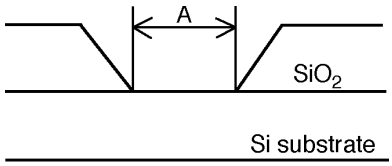

Figure 4
Schematic Diagram Showing Line Width, *A*, of Pattern on Substrate Wafer

7 The Amercan Society of Mechanical Engineers, United Engineering Center, 345 E. 47th St., New York, NY 10017.

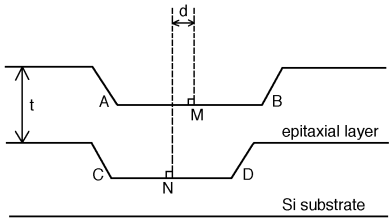

Figure 5
Cross-Section View of Epitaxial Wafer Showing the Pattern Shift, *d*. Not to scale: AM = MB and CN = ND

4.3.5 *pattern step height* — difference in vertical position of the diffused (buried layer) surface and the original substrate surface, after removal of oxide.

NOTE 5: Pattern step height, *A*, is specified as a nominal value, *X*, and a tolerance ± *Y*, both in nm. See Figure 5.

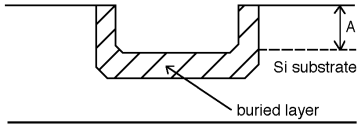

Figure 6
Cross-Sectional View of Epitaxial Substrate After Oxide Removal but Before Deposition of the Epitaxial Layer Showing the Pattern Step Height, *A*

4.4 *Terms Related to Annealed Wafers*

4.4.1 *annealed wafer* — wafer that has defects (COP) free zone near the surface produces by high temperature annealing.

4.4.1.1 *hydrogen annealed wafer* — annealed wafer produced under hydrogen atmosphere.

4.4.1.2 *argon annealed wafer* — annealed wafer produced under argon atmosphere.

4.5 *Terms Related to SOI Wafers*

4.5.1 *SOI wafer* — wafer that has a buried oxide layer (BOX).

4.5.1.1 *SIMOX wafer* — SOI wafer made by oxygen implantation and high temperature annealing technology.

4.5.1.2 *Bonded wafer* — SOI wafer made by bonding two silicon wafers with an insulating layer between them. The insulating layer is typically grown oxide.

5 Use of the Form

5.1 Different parts of the specification form are used for ordering different types of silicon wafers:

5.1.1 For polished wafers, complete Parts 1 and 2.

5.1.2 For epitaxial wafers, complete Parts 1, 2, and 3.

5.1.3 For epitaxial wafers with buried layer, complete Parts 1, 2, 3, and 4.

5.1.4 For annealed wafers, complete parts 1, 2, and 5.

5.1.5 For SOI wafers, complete Parts 1, 2, and 6. If necessary, complete Parts 3, 4, or 5.

5.2 In all cases, items listed as required must have a value or choice indicated to minimally specify the material.

5.3 Certain required dimensional items may be specified as a group according to the standard values presented in the applicable SEMI specification, or they may be specified individually.

5.4 Visual inspection criteria may be specified as a group according to the standard values listed in the applicable SEMI specification, or they may be specified individually.

5.5 For either dimensional values or visual inspection criteria, the appropriate SEMI specification may be marked and an optional line item (or items) marked as well. In this case, the value marked on each individual line item takes precedence over the standard value.

5.6 If the suggested form included in this format is not reproduced and used as a fill-out form, the items and responses must be adequately identified so that the information and requirements are clear to all parties.

6 Test Methods

6.1 Measurements shall be made or certifiable to the ASTM, JEITA, JIS, or DIN standard test method as cited in Table 1.

6.2 When standard test methods from different geographic regions are available, the default method shall be the method in common usage for the region of the purchaser of the wafer.

6.3 If several different standard test methods for an item are commonly used within a region, a specific entry must be made to identify which method of test is applicable.

6.4 If no standard test method for an item is available, the test procedure must be specified.

7 Testing Level and Certification

7.1 Material ordered using this format shall be tested and/or certified to the limits set forth in the individual criteria.

7.2 The actual testing level, whether the test is performed on all wafers, a sample of the wafers, special test pieces representing all portions of the material, or a sample of the test pieces, may be specified using this format.

7.3 In some cases, the material may be certified as "capable of meeting" certain requirements. In this context, the supplier is not required to perform the tests outlined in this format. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

8 EDI Codes and Sub-Parameter Codes

8.1 The EDI Codes for each parameter are listed in the following Table. Where necessary for clarity, additional sub-parameters are listed. These sub-parameter identify a specific measurement technique or method to be used.

8.2 If additional codes are required in the future, they will be added to the table, beginning with the next available EDI code identifier. This will allow the table to be rearranged for clarity while maintaining unique and consistent EDI codes for existing parameters. Table 2 provides a numerically sorted list of the EDI Codes.

SEMI Silicon Wafer Specification Form For Order Entry (Page 1)

Part 1 General Information

ITEMS	*INFORMATION*	*Date:*
Customer Name		
Purchase Order Number		
Line Number		
Item Number		
General Specification Number		
Revision Level		
Part Number/Revision		

Part 2 Polished Wafer

CUSTOMER:			*PART NUMBER:* *REVISION*	*DATE:*					
REQUIRED		*ITEM*	*SPECIFICATION*	*TESTING LEVEL*				*EDI*	*Sub*
				WAFER		*TEST PIECE*		*Code*	*Param*
				100%	*SAMPLE*	*100%*	*SAMPLE*	*ID*	*ID*
		1. GENERAL CHARACTERISTICS							
♦	1.1	Growth Method	[ ]Cz [ ]FZ [ ]MCz					100001	
♦	1.2	Crystal Orientation	[ ](100) [ ] (111) [ ] ( )					100002	
♦	1.3	Conductivity Type	[ ]p [ ]n					100003	
♦	1.4	Dopant	[ ]B [ ]Phos [ ]Sb [ ]As [ ]NTD					100004	
	1.5	Nominal Edge Exclusion Distance for Fixed Quality Area	Applies to Sections 6.10–6.14; 11 [ ]3 mm; [ ]5 mm; [ ]Other__mm Applies to Sections 7, 8, 12, 13 [ ]3 mm; [ ]5 mm; [ ]Other__mm (except edge defects)					100005	
		2. ELECTRICAL CHARACTERISTICS							
♦	2.1	Resistivity	Nominal [ ] ± Tolerance [ ] Ω–cm					100006	
		Measurement Position	[ ]Center Point; [ ]Other:						
		Measurement Method	[ ]SEMI MF81; [ ]SEMI MF673; [ ]JIS H 612; [ ]JEIDA 18; [ ]DIN 50431						
	2.2	Radial Resistivity Variation (RRG)	Not greater than [ ]%					100007	

		Measurement Position	SEMI MF81 Fig. 1 - [ ]A, [ ]B, [ ]C, [ ]D; [ ] JEIDA 18; [ ]DIN 50435							
		Calculation Method	[ ]SEMI MF81; [ ]JEIDA 18; [ ]DIN 50435; [ ]Other:							
	2.3	Resistivity Striations	Not greater than [ ]%					100008		
	2.4	Minority Carrier Lifetime	Greater than [ ]μs					100009		
		Test Method	SEMI MF28 [ ]A, [ ]B; SEMI MF391 [ ]A, [ ]B; [ ]SEMI MF1388; [ ]SEMI MF1535; [ ]JEIDA 53; [ ]JIS H604; [ ]DIN 50440; [ ]Other							
3. CHEMICAL CHARACTERISTICS										
	3.1	Oxygen Concentration	Nominal [ ] ± Tolerance [ ]; [ ] × 10^{17} cm^{-3}; [ ]ppma					100010		
		Calibration Factor	[ ]SEMI MF1188; [ ]ASTM F121(79); [ ]ASTM F121(83); [ ] JEIDA 61; [ ]DIN 50438/1; [ ]Other ____							
		Measurement Method	IR (Interstitial): [ ] SEMI MF1188; [ ] SEMI MF1619; [ ] JEIDA 61; [ ] DIN 50438-1 SIMS (Total): [ ]SEMI MF1366 [ ]GFA (Total)							
	3.2	Radial Oxygen Variation	Not greater than [ ]%					100011		
		Measurement Position	SEMI MF951 Plan [ ]A, [ ]B, [ ]B1, [ ]C, [ ]D; [ ]Other:__							
		Calculation Method	SEMI F951 Plan [ ]A, [ ]B, [ ]B1, [ ]C, [ ]D; [ ] Other:__							
	3.3	Carbon Concentration	Not greater than [ ] [ ]ppma; [ ] × $10^{16}$$cm^{-3}$					100012		
		Measurement Method	[ ]SEMI MF1391; JEIDA 56; [ ]DIN 50438/2; [ ]Other:____							
	3.4	Boron Concentration in Heavily Doped n-type Si	Not greater than [ ] ppba					100013		
4. STRUCTURAL CHARACTERISTICS										
	4.1	Dislocation Etch Pit Density	[ ]Not greater than [ ]/cm^2					100014		
	4.2	Slip	[ ]None [ ]Other ___					100015		
	4.3	Lineage	[ ]None [ ]Other ___					100016		
	4.4	Twin	[ ]None [ ]Other ___					100017		
	4.5	Swirl	[ ]Not greater than [ ]% of wafer area					100018		
	4.6	Shallow Pits	Not greater than [ ]/cm^2					100019		
	4.7	Oxidation Induced Stacking Faults (OSF)	Not greater than [ ]/cm^2					100020		
		Test Cycle	ASTM F 416 Cycle-[ ]1 [ ]2 [ ]3; [ ] SEMI MF 1727; [ ]Other:__							
	4.8	Oxide Precipitates (BMD)	Range: [ ] to [ ] Unit: [ ] cm^2 [ ] cm^3					100021		
		Test Cycle	SEMI MF1239 [ ]A, [ ]B; [ ] Other:_____							
	4.9	Interstitial Oxygen Reduction (ΔO_I)	Range: [ ] to [ ] [ ]ppma, [ ] × $10^{17}$$cm^{-3}$					100162		
		Test Cycle	SEMI MF1239 [ ]A, [ ]B; [ ] Other:_____							
5. WAFER PREPARATION CHARACTERISTICS										
	5.1	Wafer ID Marking	[ ]None; [ ]SEMI M12; [ ]SEMI M13; [ ]SEMI T1; [ ]SEMI T2; [ ] SEMI T7; [ ]Other:_____					100022		

	5.2	Front Surface Thin Film(s) Appl	[ ]None [ ]Description:					100023	
	5.3	Denuded Zone	[ ]None [ ]Description:					100024	
	5.4	Extrinsic Gettering Treatment	[ ]None [ ]Description:					100025	
	5.5	Backseal	[ ]None [ ]Description:					100026	
	5.6	Annealing	[ ]None [ ]Description:					100027	
6. MECHANICAL CHARACTERISTICS									
THE ITEMS LISTED IN THIS SECTION MAY BE									
	6.01	[ ] Specified According to SEMI M1_____						100028	
OR SPECIFIED INDIVIDUALLY									
♦	6.1	Diameter[1]	Nominal [ ] ± Tolerance [ ] mm					100029	
♦	6.2	Primary Flat Length/Diameter Notch Dimensions[1]	[ ]SEMI M1._____; [ ]Other:___mm					100030	
♦	6.3	Primary Flat/Notch Orientation[1]	[ ]SEMI M1._____; [ ]Other:					100031	
♦	6.4	Secondary Flat Length[1]	[ ]SEMI M1._____; [ ]Other:___mm; [ ]None					100032	
♦	6.5	Secondary Flat Location[1]	[ ]SEMI M1._____; [ ]Other:___; [ ]None					100033	
♦	6.6	Edge Profile[1]	[ ]SEMI Standard [ ]Other:_____					100034	
♦	6.7	Thickness[1]	Nominal [ ] ± Tolerance [ ] µm					100035	
		Method	[ ]SEMI MF533; [ ]SEMI MF1530; [ ]JIS H 611; [ ]DIN 50441/1; [ ]Other						
	6.8	Thickness Variation (TTV)[1]	[ ]SEMI M1._____; [ ]Other: [ ] µm					100036	
		Measurement Position	[ ]SEMI MF533; [ ]SEMI MF657; [ ]SEMI MF1530; [ ]JIS H 611; [ ]DIN 50441/1; [ ]Other:_____						
♦	6.9	Surface Orientation	[ ]0.00 ± 0.50; [ ]2.50 ± 0.50; [ ]4.00 ± 0.50; [ ] Other:_____					100037	
		Method	[ ]SEMI MF26; [ ]JEIDA 18; [ ]DIN 50433; [ ]Other:_____						
	6.10	Bow[1]	[ ]SEMI M1._____; [ ]Other:___ µm					100038	
		Method	[ ]SEMI MF534; [ ]JIS H 611; [ ]Other:_____						
	6.11	Warp[1]	[ ]SEMI M1._____; [ ]Other: ___ µm						
		Method	[ ]SEMI MF657; [ ]SEMI MF1390; [ ]Other:_____					100039 100040	SEMI MF657 SEMI MF1390
	6.12	Sori	[ ]_____µm					100041	
		Method	[ ] SEMI MF1451; [ ] JEIDA 43						
	6.13	Flatness/Global	Acronym:[2][ ] [ ] [ ] [ ] Value: [ ]µm					100042	
		Method	[ ]SEMI MF1530; [ ]DIN 50441/3; [ ]Other:_____						

	6.14	Flatness/Site	Acronym:[2] [ ] [ ] [ ] [ ] Value: [ ]µm Site Size ___×___ mm Total Sites___ % Usable Area___ [ ] Include partial sites [ ] Offset: x = [ ] mm, y = [ ] mm					100043 100044 100045 100046 100047 100048 100049 100050 100221	SF3R SF3D SFLR SFLD SFQR SFQD SBIR SBID SFSD
	6.15	Fixed Quality Area	Value: [ ]mm dia					100164	
7. FRONT SURFACE CHEMISTRY									
	7.1	Surface Metal Contamination							
		Sodium	[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100051	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other:_____						
		Aluminum	[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100052	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other:_____						
		Potassium	[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100053	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]Other:_____						
		Chromium	[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100054	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]SIMS; [ ]Other:_____						
		Iron	[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100055	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]SEMI MF1617 (SIMS); [ ]Other:_____						
		Nickel	[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100056	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]Other:_____						
		Copper	[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100057	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]Other:_____						
		Zinc	[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100058	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]Other:_____						
		Others (List Separately)							
			[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100059	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]SIMS; [ ]Other:_____						
			[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100060	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]SIMS; [ ]Other:_____						
			[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100061	
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]SIMS; [ ]Other:_____						
			[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100062	

		Method	[]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]SIMS; [ ]Other:_____							
			[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100063		
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]SIMS; [ ]Other:_____							
			[ ]Not greater than [ ]atoms/cm^2; [ ]Other					100064		
		Method	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1526 (TXRF); [ ]SEMI M33 (TXRF); [ ]SIMS; [ ]Other:_____							
	7.2	Surface Organics	[ ]Not greater than [ ]ngrams/cm^2					100065		
		Method	[ ]SEMI MF1982; [ ]Other:_____							
8. FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS										
THE ITEMS LISTED IN THIS SECTION MAY BE										
	8.01	[ ] Specified According to SEMI M1 Table 1						100066		
OR SPECIFIED INDIVIDUALLY										
	8.1	Scratches[3]	[ ]SEMI M1 Table 1 [ ]Other:					100067		
	8.2	Pits[3]	[ ]SEMI M1 Table 1 [ ]Other:					100068		
	8.3	Haze[3]	[ ]SEMI M1 Table 1 [ ]Other:					100069		
	8.4	Localized Light Scatterers (LLS)[3]	[ ]SEMI M1 Table 1 [ ]Other: Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ]					100070 100071 100072 100073 100074 100075 100076 100077 100078 100079 100080 100081 100082 100083 100084 100085 100086 100087 100088 100089 100090	≥0.50 µ ≥0.30 µ ≥0.20 µ ≥0.19 µ ≥0.18 µ ≥0.17 µ ≥0.16 µ ≥0.15 µ ≥0.14 µ ≥0.13 µ ≥0.12 µ ≥0.11 µ ≥0.10 µ ≥0.09 µ ≥0.08 µ ≥0.07 µ ≥0.06 µ ≥0.05 µ ≥0.04 µ ≥0.03 µ ≥0.02 µ
		Method	[ ]SEMI MF523; [ ]SEMI MF1620; [ ]JIS H 614; [ ]JEIDA 24; [ ]Other:_____							
	8.5	Contamination/Area[3]	[ ]SEMI M1 Table 1 [ ]Other:					100091		
	8.6	Edge Chips[3]	[ ]SEMI M1 Table 1 [ ]Other:					100092		
	8.7	Edge Cracks[3]	[ ]SEMI M1 Table 1 [ ]Other:					100093		
	8.8	Cracks, Crow's Feet[3]	[ ]SEMI M1 Table 1 [ ]Other:					100094		
	8.9	Craters[3]	[ ]SEMI M1 Table 1 [ ]Other:					100095		
	8.10	Dimples[3]	[ ]SEMI M1 Table 1 [ ]Other:					100096		
	8.11	Grooves[3]	[ ]SEMI M1 Table 1 [ ]Other:					100097		
	8.12	Mounds[3]	[ ]SEMI M1 Table 1 [ ]Other:					100098		
	8.13	Orange Peel[3]	[ ]SEMI M1 Table 1 [ ]Other:					100099		
	8.14	Saw Marks[3]	[ ]SEMI M1 Table 1 [ ]Other:					100100		
	8.15	Dopant Striation Rings	[ ]					100101		

	8.16	Stains	[ ]					100102	
9. BACK SURFACE VISUAL INSPECTION CHARACTERISTICS									
THE ITEMS LISTED IN THIS SECTION MAY BE									
	9.01	[ ] Specified According to SEMI M1 Table 1						100103	
OR SPECIFIED INDIVIDUALLY									
	9.1	Edge Chips[3]	[ ]SEMI M1 Table 1 [ ]Other:					100104	
	9.2	Cracks, Crow's Feet[3]	[ ]SEMI M1 Table 1 [ ]Other:					100105	
	9.3	Contamination/Area[3]	[ ]SEMI M1 Table 1 [ ]Other:					100106	
	9.4	Saw Marks[3]	[ ]SEMI M1 Table 1 [ ]Other:					100107	
	9.5	Stains	[ ]					100108	
	9.6	Roughness	[ ]					100109	
	9.7	Brightness	[ ]					100110	
	9.8	Scratches – macro	[ ]None; [ ]Cum Length =[ ]mm					100165	
	9.9	Scratches – micro	[ ]None; [ ]Cum Length =[ ]mm					100166	
	9.10	Localized Light Scatterers	Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ]					100167 100168	
10. OTHER CHARACTERISTICS									
	10.1	Bulk defects by X-ray topography	[ ]Value:_____					100169	
		Method	[ ]DIN 50443/1; [ ]Other:_____						

Part 3 Epitaxial Wafer

CUSTOMER:		*PART NUMBER:* *REVISION*	*DATE:*					
REQUIRED	*ITEM*	*SPECIFICATION*	*TESTING LEVEL*				*EDI*	*Sub*
			WAFER		*TEST PIECE*		*Code*	*Param*
			100%	*SAMPLE*	*100%*	*SAMPLE*	*ID*	*ID*
11. GENERAL EPITAXIAL WAFER AND LAYER CHARACTERISTICS								
THE ITEMS LISTED IN THIS TABLE MAY BE								
	11.01	[ ] Specified According to SEMI M11 Table [ ]					100170	
OR SPECIFIED INDIVIDUALLY								
♦	11.1	Conductivity Type/Structure	[ ]n/n+ [ ]p/p+ [ ]Other:_____				100111	
♦	11.2	Dopant	[ ]B [ ]Phos [ ]As				100112	
	11.3	Silicon Source Gas	[ ]SiH_4; [ ]SiH_2Cl_2; [ ]$SiHCl_3$; [ ]$SiCl_4$				100113	
	11.4	Growth Method	Reactor Type [ ] Pressure [ ]				100114	
♦	11.5	Net Carrier Density (Resistivity)	Nominal [ ] ± Tolerance [ ] (check unit below)				100115	
		Units	[ ]10[ ]atoms/cm^3; [ ]Ωcm					
		Test Method	[ ]ASTM F419 - [ ]Gated, [ ]Ungated, [ ]Schottky; [ ]SEMI MF374 (4-Pt); [ ]SEMI MF525 (SRP); [ ]SEMI MF1392 (Hg-CV); [ ] SEMI MF1393; [ ]DIN 50439; [ ]DIN 50444; [ ]DIN 50447; [ ]Other ____					
♦	11.6	Net Carrier Density Variation	[ ]Not greater than [ ]% [ ]SEMI M2; [ ]SEMI M11 Table [ ]				100116	
		Measurement Position	[ ]SEMI M2; [ ]SEMI M11; [ ]Other:_____					
		Calculation	[ ]SEMI M2; [ ]SEMI M11; [ ]Other:_____					

♦	11.7	Thickness	Nominal [ ] ± Tolerance [ ]µm					100117	
		Test Method	[ ]SEMI MF95; [ ]SEMI MF110; [ ]FT-IR; [ ]SEMI MF 672(SRP); [ ]DIN 50436; [ ]DIN 50437; [ ]Other:_____						
♦	11.8	Thickness Variation	[ ]Not greater than [ ]% [ ]SEMI M2; [ ]SEMI M11 Table [ ]					100118	
		Measurement Position	[ ]SEMI M2; [ ]SEMI M11; [ ]Other:_____						
		Calculation	[ ]SEMI M2; [ ]SEMI M11; [ ]Other:_____						
	11.9	Transition Width	Not greater than [ ]µm					100119	
		Measurement Position							
		Calculation							
	11.10	Flat Zone	Not less than [ ]µm					100120	
		Measurement Position							
		Calculation							
	11.11	Phantom Layer	[ ]None					100121	
12. MECHANICAL CHARACTERISTICS									
THE ITEMS LISTED IN THIS SECTION MAY BE									
	12.01	[ ] Specified According to SEMI M11 Table [ ]						100135	
OR SPECIFIED INDIVIDUALLY									
	12.1	Bow	Not greater than [ ] µm					100122	
		Method	[ ]SEMI MF534; [ ]JIS H 611; [ ]Other:_____						
	12.2	Warp	Not greater than [ ] µm						
		Method	[ ] SEMI MF657; [ ] SEMI MF1390; [ ]Other:_____					100123 100124	SEMI MF657 SEMI MF1390
	12.3	Sori	Not greater than [ ] µm					100125	
	12.4	Flatness/Global	Acronym[2]: [ ][ ][ ][ ] Value _____µm					100126	
		Method	[ ]SEMI MF1530 [ ]DIN 50441/3 [ ]Other						
	12.5	Flatness/Site	Acronym[2]:[ ][ ][ ][ ] Value ____µm Site Size __×__ mm Total Sites __ % Usable Area __ [ ] Include partial sites [ ] Offset: x = [ ] mm, y = [ ] mm					100127 100128 100129 100130 100131 100132 100134 100161 100222 100223	SF3R SF3D SFLR SFLD SFQR SFQD SBIR SFSR SFSD SBID
	12.6	Fixed Quality Area	Value: [ ]mm dia					100172	
13. FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS									
THE ITEMS LISTED IN THIS SECTION MAY BE									
	13.01	[ ] Specified According to [ ]SEMI M2 Table 1 or [ ]SEMI M11 Table [ ]						100135	
OR SPECIFIED INDIVIDUALLY									
	13.1	Stacking Faults[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100136	
		Method	[ ] ASTM F522 [ ] DIN 50446 [ ]Other						
	13.2	Slip[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100137	
		Method	[ ] ASTM F47 [ ] ASTM F80 [ ] SEMI MF523 [ ]DIN 50446 [ ]Other						

	13.3	Large Point Defects[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100138	
		Method	[ ] SEMI MF523 [ ] ASTM F815 [ ] DIN 50446 [ ] Other: _____						
	13.4	Total Points Defects[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100139	
		Method	[ ] SEMI MF523 [ ] ASTM F815 [ ] DIN 50446 [ ] Other: _____						
	13.5	Scratches[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100140	
		Method	[ ] SEMI MF523 [ ]Other						
	13.6	Dimples[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100141	
		Method	[ ] SEMI MF523 [ ]Other						
	13.7	Orange Peel[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100142	
		Method	[ ] SEMI MF523 [ ]Other						
	13.8	Cracks/Fractures[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100143	
		Method	[ ] SEMI MF523 [ ]Other						
	13.9	Crow's Feet[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100144	
		Method	[ ] SEMI MF523 [ ]Other						
	13.10	Edge Chips[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100145	
		Method	[ ] SEMI MF523 [ ]Other						
	13.11	Edge Crown[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100146	
		Method	[ ] DIN 50446 [ ]Other						
	13.12	Haze[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100147	
		Method	[ ] SEMI MF523 [ ]Other						
	13.13	Foreign Matter[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other: _____					100148	
		Method	[ ] SEMI MF523 [ ]Other						

	13.14	Localized Light Scatterers (LLS)[4]	[ ]SEMI M11 Table 1 [ ]Other: Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ]					100173 100174 100175 100176 100177 100178 100179 100180 100181 100182 100183 100184 100185 100186 100187 100188 100189 100190 100191 100192 100193	≥0.50 µ ≥0.30 µ ≥0.20 µ ≥0.19 µ ≥0.18 µ ≥0.17 µ ≥0.16 µ ≥0.15 µ ≥0.14 µ ≥0.13 µ ≥0.12 µ ≥0.11 µ ≥0.10 µ ≥0.09 µ ≥0.08 µ ≥0.07 µ ≥0.06 µ ≥0.05 µ ≥0.04 µ ≥0.03 µ ≥0.02 µ
		Method	[ ]SEMI MF523; [ ]SEMI MF1620; [ ]JIS H 614; [ ]JEIDA 24; [ ]Other:_____						
	13.15	Surface Edge Exclusion	[ ]2 mm; [ ]3 mm; [ ]4 mm; [ ]5 mm ; [ ]Other:____					100194	
14. BACK SURFACE VISUAL INSPECTION CHARACTERISTICS									
THE ITEMS LISTED IN THIS SECTION MAY BE									
	14.01	[ ] Specified According to SEMI M11 Table [ ]						100195	
OR SPECIFIED INDIVIDUALLY									
	14.1	Contamination[4]	[ ]SEMI M2 Table 1; [ ]SEMI M11 Table [ ]; [ ]Other:_____					100149	
	14.2	Scratches -- macro	[ ]None; [ ]Cum Length =[ ] mm					100196	
	14.3	Scratches -- micro	[ ]None; [ ]Cum Length =[ ] mm					100197	
	14.4	Localized Light Scatterers	[ ]SEMI M11 Table [ ]; [ ]Other:_____ Size: [ ] µm Count: ≤ [ ] Size: [ ] µm Count: ≤ [ ]					100198 100199	
15. OTHER CHARACTERISTICS									

Part 4 Epitaxial Wafer with Buried Layer

CUSTOMER:		*PART NUMBER: REVISION*	*DATE:*					
REQUIRED	*ITEM*	*SPECIFICATION*	*TESTING LEVEL*				*EDI*	*Sub*
			WAFER		*TEST PIECE*		*Code*	*Param*
			100%	*SAMPLE*	*100%*	*SAMPLE*	*ID*	*ID*
16. PHOTOLITHOGRAPHY CHARACTERISTICS								
	16.1	Mask ID	[ ] Number: [ ]; [ ]None					100150	

	16.2	Alignment Precision	X max [ ] µm, Y max [ ] µm, Θ max[ ]; Reference Point (Wafer Coordinate System): x [ ] mm, y [ ] mm					100151	
	16.3	Pattern Line Width Tolerance	Tolerance ± [ ] µm					100152	
		17. BURIED LAYER CHARACTERISTICS							
	17.1	Dopant	[ ]B; [ ]Phos; [ ]Sb; [ ]As					100153	
	17.2	Diffusion Depth (x_j)	Nominal [ ] ± Tolerance [ ] µm					100154	
	17.3	Sheet Resistance	Nominal [ ] ± Tolerance [ ] Ω/sq					100155	
	17.4	Pattern Step Height	Nominal [ ] ± Tolerance [ ] nm					100156	
	17.5	Defect Density (Before Epi)	Not greater than [ ]/cm^2					100157	
		18. BURIED LAYER PATTERN CHARACTERISTICS AFTER EPI							
	18.1	Pattern Shift Ratio	Nominal [ ] ± Tolerance [ ]					100158	
	18.2	Pattern Distortion Ratio	Max. [ ]					100159	
		19. OTHER CHARACTERISTICS							

Part 5 Annealed Wafer

CUSTOMER:			*PART NUMBER:* *REVISION*	*DATE:*					
REQUIRED	*ITEM*		*SPECIFICATION*	*TESTING LEVEL*				*EDI*	*Sub*
				WAFER		*TEST PIECE*		*Code*	*Param*
				100%	*SAMPLE*	*100%*	*SAMPLE*	*ID*	*ID*
		20. GENERAL ANNEALED WAFER CHARACTERISTICS							
♦	20.1	Annealing Atmosphere	[ ]Hydrogen [ ]Argon [ ]Other: _____					100200	
♦	20.2	Co-dopant in Crystal	[ ]N [ ]C [ ]Other:					100201	
		21. MECHANICAL CHARACTERISTICS							
	21.1	Bow	Not greater than [ ] µm					100202	
		Method	[ ]SEMI MF534; [ ]JIS H 611; [ ]Other:_____						
	21.2	Warp	Not greater than [ ] µm						
		Method	[ ] SEMI MF657; [ ] SEMI MF1390; [ ]Other:_____					100203 100204	SEMI MF657 SEMI MF1390
	21.3	Sori	Not greater than [ ] µm					100205	
	21.4	Flatness/Global	Acronym[2]: [ ][ ][ ][ ] Value _____µm					100206	
		Method	[ ]SEMI MF1530 [ ]DIN 50441/3 [ ]Other						

CUSTOMER:			PART NUMBER: REVISION	DATE:					
REQUIRED	ITEM		SPECIFICATION	TESTING LEVEL				EDI	Sub
				WAFER		TEST PIECE		Code	Param
				100%	SAMPLE	100%	SAMPLE	ID	ID
	21.5	Flatness/Site	Acronym[2]:[ ][ ][ ][ ] Value ____µm Site Size __×__ mm Total Sites __ % Usable Area __ [ ] Include partial sites [ ] Offset: x = [ ] mm, y = [ ] mm					100207 100208 100209 100210 100211 100212 100213 100214 100224 100225	SF3R SF3D SFLR SFLD SFQR SFQD SBIR SFSR SFSD SBID
	21.6	Fixed Quality Area	Value: [ ] mm					100215	
		22. FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS							
		THE ITEMS LISTED IN THIS SECTION MAY BE							
	22.01	[ ] Specified According to [ ]SEMI M2 Table 1 or [ ]SEMI M11 Table 1							
		OR SPECIFIED INDIVIDUALLY							
	22.1	Stacking Faults[4]	[ ]SEMI M( ) Table 1 [ ]Other:					100216	
	22.2	Slip[4]	[ ]SEMI M( ) Table 1 [ ]Other:					100217	
	22.3	Other Defect[5]	[ ]SEMI M( ) Table 1 [ ]Other:						
		23. BACK SURFACE VISUAL INSPECTION CHARACTERISTICS							
	23.1	Contamination[4]	[ ]SEMI M( ) Table 1; [ ]Other:_____					100218	
	23.2	Other[6]							
		24. OTHER CHARACTERISTICS							
	24.1	Depth of BMD Denuded Zone						100219	
	24.2	BMD Density						100220	
	24.3	Other[7]							

Part 6 SOI wafers for CMOS LSI Applications

CUSTOMER:			PART NUMBER: REVISION	DATE:					
REQUIRED	ITEM		SPECIFICATION	TESTING LEVEL				EDI	Sub
				WAFER		TEST PIECE		Code	Param
				100%	SAMPLE	100%	SAMPLE	ID	ID
	25. SOI LAYER CHARACTERISTICS								
♦	25.0	Type of SOI	[ ] SIMOX [ ] Bonded					100226	
	25.1	Starting silicon wafer for SOI	[ ] Polished [ ] Epitaxial [ ]Others					100227	
♦	25.2	Surface Silicon Thickness	[ ] (nm) See NOTE 8					100228	
		Test Method	[ ] Spectroscopic ellipsometry [ ] Spectroscopic reflectometry [ ] Others						
	25.3	Surface Silicon Thickness Mean Value Variation	≤ ± [ ] (nm) See NOTE 9					100229	
		Test Method	[ ] Spectroscopic ellipsometry [ ] Spectroscopic reflectometry [ ] Others						
♦	25.4	Surface Silicon Thickness Variation in Wafer	[ ] ≤ ± [ ] (%) [ ] ≤ ± [ ] (nm) See NOTE 9					100230	
	25.5	Crystal Orientation	(100) ± [ ] (degree)					100231	
		Test Method	[ ] X-ray diffraction, [ ] Others:						
	25.6	Rotation Misalignment	≤ ± [ ] (degree) for Bonded					100232	
		Test Method	[ ] Visual, [ ] Others:						
	25.7	Edge Exclusion, Nominal	[ ] (mm) See NOTE 10					100233	
	25.8	Non-SOI Edge Area	≤ [ ] (mm) for Bonded					100234	
		Test Method	[ ] Visual, [ ] Others:						
	25.9	Conductivity Type	[ ]P-type [ ]N-type					100235	
	25.10	Dopant	[ ]B [ ]P [ ]Others:					100236	
		Test Method	[ ] Secondary ion mass spectroscopy, [ ] Others						
	25.11	Dopant Concentration	[ ] (atoms /cm^3) See NOTE 8					100237	
		Test Method	[ ] Secondary ion mass spectroscopy, [ ] Others:						
	25.12	SOI Etch Pit	≤ [ ] (/cm^2)					100238	
		Test Method	[ ] Secco's Etching, [ ] Others:						
	25.13	Threading Dislocation	≤ [ ] (/cm^2) for SIMOX					100239	
		Test Method	[ ] Secco's Etching, [ ] Others:						
	25.14	HF Defect	≤ [ ] (/cm^2)					100240	
		Test Method	[ ] HF Etching, [ ] Others:						
	25.15	Void	≤ [ ] (/wafer) for Bonded					100241	
		Test Method	[ ] Automated particle counter, [ ] Visual, [ ] Others:						
	25.16	Roughness (Si surface) rms @ 2 × 2μm	≤ [ ] (nm)					100242	
		Test Method	[ ] Atomic force microscope, [ ] Others:						

		Roughness (Si surface) rms @ 10 × 10μm	≤ [ ] (nm)					100243	
		Test Method	[ ] Atomic force microscope, [ ] Others:						
		Roughness (Si surface) rms@ [ ] × [ ]μm	≤ [ ] (nm)					100244	
		Test Method	[ ] Atomic force microscope, [ ] Others:						
		Roughness (Si surface) rms@ [ ] × [ ]μm	≤ [ ] (nm)					100245	
		Test Method	[ ] Atomic force microscope, [ ] Others:						
	25.17	Surface Metal (Fe) Contamination	≤ [ ] (/cm^2)					100246	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal (Cr) Contamination	≤ [ ] (/cm^2)					100247	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal (Ni) Contamination	≤ [ ] (/cm^2)					100248	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal (Cu) Contamination	≤ [ ] (/cm^2)					100249	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal [ ] Contamination	≤ [ ] (/cm^2)					100250	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal [ ] Contamination	≤ [ ] (/cm^2)					100251	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal [ ] Contamination	≤ [ ] (/cm^2)					100252	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal [ ] Contamination	≤ [ ] (/cm^2)					100253	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal [ ] Contamination	≤ [ ] (/cm^2)					100254	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Surface Metal [ ] Contamination	≤ [ ] (/cm^2)					100255	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		26. BOX CHARACTERISTICS							
♦	26.1	BOX Thickness	[ ] (nm) See NOTE 8					100256	
		Test Method	[ ] Spectroscopic ellipsometry, [ ] Spectroscopic reflectometry, [ ] Others						
♦	26.2	BOX Thickness Variation	[ ] ≤ ± [ ] (nm), [ ] ≤ ± [ ] (%)					100257	
		Test Method	[ ] Spectroscopic ellipsometry, [ ] Spectroscopic reflectometry, [ ] Others:						

	26.3	Bonded Interface Location	[ ] at SOI/BOX interface [ ] within BOX layer [ ] at BOX/Substrate interface					100258	
	26.4	BOX Pinholes	≤ [ ] (/cm^2)					100259	
		Test Method	[ ] Cu plating, [ ] BOX capacitor, [ ] Others:						
	26.5	Dielectric Breakdown	> [ ] (MV/cm)					100260	
		Test Method	[ ] BOX capacitor, [ ] Others:						
27. MECHANICAL CHARACTERISTICS									
	27.1	Warp	≤ [ ] (μm)					100261	
		Test Method	[ ] Automated noncontact scanning [ ] Others:						
	27.2	Flatness-site	See NOTE 8					100262	
28. FRONT SURFACE INSPECTION CHARACTERISTICS									
	28.1	Scratch	None					100263	
		Test Method	[ ] Visual, [ ] Others:						
	28.2	Haze	None					100264	
		Test Method	[ ] Visual, [ ] Others:						
	28.3	LLS @particle size	≤ [ ] (/cm^2) @ ≥ [ ] (μm)					100265 100266	
		Test Method	[ ] Automated particle counter [ ] Others:						
	28.4	Slip	See NOTE 8					100267	
		Test Method	[ ] Visual, [ ] Others:						
	28.5	Edge Chip	[ ]SEMI M1, [ ]Others:					100268	
		Test Method	[ ] Visual, [ ] Others:						
	28.6	Edge Crack	[ ]SEMI M1, [ ]Others:					100269	
		Test Method	[ ] Visual, [ ] Others:						
	28.7	Foreign Matter	See NOTE 8					100270	
		Test Method	[ ] Visual, [ ] Others:						
29. BACK SURFACE CHARACTERISTICS									
	29.1	Backside Metal (Fe) Contamination	≤ [ ] (/cm^2) for each atom					100271	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Backside Metal (Cr) Contamination	≤ [ ] (/cm^2)					100272	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Backside Metal (Ni) Contamination	≤ [ ] (/cm^2)					100273	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Backside Metal (Cu) Contamination	≤ [ ] (/cm^2)					100274	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Backside Metal [ ] Contamination	≤ [ ] (/cm^2)					100275	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Backside Metal [ ] Contamination	≤ [ ] (/cm^2)					100276	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Backside Metal [ ] Contamination	≤ [ ] (/cm^2)					100277	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						

		Backside Metal [ ] Contamination	≤ [ ] (/cm^2)					100278	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Backside Metal [ ] Contamination	≤ [ ] (/cm^2)					100279	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						
		Backside Metal [ ] Contamination	≤ [ ] (/cm^2)					100280	
		Test Method	[ ] TXRF, [ ] AAS, [ ] ICP-MS						

1. Individual value is not required if wafer is specified according to SEMI M1. _____.

2. Flatness Acronyms are determined from the Flatness Decision Tree in SEMI M1, Appendix 1.

3. Individual value is not required if wafer is specified according to SEMI M1, Table 1.

4. Individual value is not required if wafer is specified according to Table 1 of SEMI M2 or SEMI M11.

5. Haze, Teracing, Surface micro-roughness, Nanotopography, and other attributes may be discussed between supplier and user.

6. Support-related backside defects may be discussed between supplier and user

7. Surface boron depletion, dissolved hydrogen in the case of hydrogen annealed wafer, Post-annealed oxygen, and Silicon nitride precipitates and defects in the case of nitrogen-doped silicon may be discussed between supplier and user.

8. To be specified or discussed between users and suppliers.

9. Thinner SOI is to be discussed between users and suppliers.

10. It is specified by a distance from the FQA boundary to the periphery of a base wafer of nominal dimensions. It is not a distance from an edge of an SOI layer.

Table 1 Industry Standard References

Polished Wafer

ITEM		*VALUE*		*STANDARD REFERENCE*[A]		*STANDARD TEST METHODS*			
		IS IN SEMI	*IS REQ'D*[B]	*SEMI*	*JEIDA*	*ASTM*	*SEMI*	*JIS JEIDA*	*DIN*
1.	GENERAL CHARACTERISTICS								
1.1	Growth Method	NO	YES	M1 Note 5			MF26		
1.2	Crystal Orientation	NO	YES				MF42	18	50433/1 50433/2 50433/3
1.3	Conductivity Type	NO	YES	M1 Note 5				H 607	50432
1.4	Dopant	NO	YES	M1 Note 5					50438/3
1.5	Nominal Edge Exclusion Distance for Fixed Quality Area	NO	NO	M1 Fig 1					
2.	ELECTRICAL CHARACTERISTICS								
2.1	Resistivity	NO	YES	M1 Sec 9			MF84, MF673	H 602 18 H 612	50431, 50447
2.2	Radial Resistivity Variation (RRG)	NO	NO	M1 Sec 9			MF81	18	50435
2.3	Resistivity Striations	NO	NO				MF154, MF525		
2.4	Minority Carrier Lifetime	NO	NO				MF28, MF391, MF1388, FM1535	H 604 53	50440
3.	CHEMICAL CHARACTERISTICS								
3.1	Oxygen Concentration	NO	NO				MF1188, MF1366, MF1619	61	50438/1
3.2	Radial Oxygen Variation	NO	NO				MF951		
3.3	Carbon Concentration	NO	NO				MF1391	56	50438/2

ITEM		VALUE		STANDARD REFERENCE[A]		STANDARD TEST METHODS			
		IS IN SEMI	IS REQ'D[B]	SEMI	JEIDA	ASTM	SEMI	JIS JEIDA	DIN
3.4	Boron Concentration in Heavily Doped n-type Si	NO	NO				MF1528		
4.	STRUCTURAL CHARACTERISTICS								
4.1	Dislocation Etch Pit Density	NO	NO			F 47		H 609	50434
4.2	Slip	NO	NO			F 47, F 416		H 609	50434
4.3	Lineage	NO	NO			F 47		H 609	50434
4.4	Twin	NO	NO			F 47		H 609	50434
4.5	Swirl	NO	NO			F 416		H 614 24	
4.6	Shallow Pits	NO	NO			F 416	MF1049	H 614 24	
4.7	Oxidation Induced Stacking Faults (OSF)	NO	NO			F 416	MF1727, MF1809, MF1810		
4.8	Oxide Precipitates (BMD) Interstitial Oxygen Reduction (ΔO_i)	NO NO	NO NO				MF1239, MF1809, MF1810		
5.	WAFER PREPARATION CHARACTERISTICS								
5.1	Wafer ID Marking	YES	NO	M12, M13					
5.2	Front Surface Thin Film(s) Applied	NO	NO						
5.3	Denuded Zone	NO	NO						
5.4	Extrinsic Gettering Treatment	NO	NO						
5.5	Backseal	NO	NO						
5.6	Annealing	NO	NO						
6.	MECHANICAL CHARACTERISTICS								
6.1	Diameter	YES	YES[C]	M1 Sec 9	27	F 613			50441/4
6.2	Primary Flat Length/Diameter Notch Dimensions	YES	YES[C]	M1	27		MF671, MF1152		50441/4
6.3	Primary Flat/Notch Orientation	YES	YES[C]	M1 Sec 9	27		MF847		
6.4	Secondary Flat Length	YES	YES[C]	M1 Sec 9			MF671		50441/4
6.5	Secondary Flat Location	YES	YES[C]	M1 Sec 9			MF847		
6.6	Edge Profile	YES	YES[C]	M1 Sec 5			MF928		50441/2
6.7	Thickness	YES	YES[C]	M1 Sec 9	27		MF533, MF1530	H 611	50441/1
6.8	Thickness Variation (TTV)	YES	NO	M1 Sec 9	27		MF533, MF657, MF1530	H 611	50441/1
6.9	Surface Orientation	YES	YES	M1 Sec 9	27		MF26	18	50433
6.10	Bow	YES	NO	M1 Sec 9			MF534	H 611	
6.11	Warp	YES	NO	M1 Sec 9			MF657, MF1390		
6.12	Sori	NO	NO	M1 Sec 9			MF1451	43	
6.13	Flatness	NO	NO	M1 Sec 9			MF1530		50441/3
7.	FRONT SURFACE CHEMISTRY								
7.1	Surface Metal Contamination								
	Sodium	NO	NO				MF1617		
	Aluminum	NO	NO				MF1617		
	Potassium	NO	NO	M33			MF1617		

ITEM		VALUE		STANDARD REFERENCE[A]		STANDARD TEST METHODS			
		IS IN SEMI	IS REQ'D[B]	SEMI	JEIDA	ASTM	SEMI	JIS JEIDA	DIN
	Chromium	NO	NO	M33			MF1526		
	Iron	NO	NO	M33			MF1526		
	Nickel	NO	NO	M33			MF1526		
	Copper	NO	NO	M33			MF1526		
	Zinc	NO	NO	M33			MF1526		
7.2	Surface Organics						MF1982		
8.	FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS[D]								
8.1	Scratches	YES	NO	M1 Table 1	26		MF523	H 614	
8.2	Pits	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.3	Haze	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.4	Light Scattering Defects(Particulate Contamination)	YES	NO	M1 Table 1	26		MF1620 MF523	H 614 24	
8.5	Contamination/Area	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.6	Edge Chips	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.7	Edge Cracks	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.8	Cracks, Crow's Feet	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.9	Craters	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.10	Dimples	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.11	Grooves	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.12	Mounds	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.13	Orange Peel	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.14	Saw Marks	YES	NO	M1 Table 1	26		MF523	H 614 24	
8.15	Dopant Striation Rings	NO	NO		26		MF523	H 614 24	
8.16	Stains	NO	NO		26		MF523	H 614 24	
9.	BACK SURFACE VISUAL INSPECTION CHARACTERISTICS								
9.1	Edge Chips	YES	NO	M1 Table 1			MF523		
9.2	Cracks, Crow's Feet	YES	NO	M1 Table 1			MF523		
9.3	Contamination/Area	YES	NO	M1 Table 1			MF523		
9.4	Saw Marks	YES	NO	M1 Table 1			MF523		
9.5	Stains	NO	NO						
9.6	Roughness	NO	NO						
9.7	Brightness	NO	NO						
10.	OTHER CHARACTERISTICS								
10.1	Bulk defects by X-ray topography								50443/1

Epitaxial Wafer

ITEM		*VALUE*			*STANDARD REFERENCE*[A]			*STANDARD TEST METHODS*			
		IS IN M2	*IS IN M11*	*IS REQ'D*[B]	*SEMI M2*	*SEMI M11*	*JEIDA*	*ASTM*	*SEMI*	*JIS JEIDA*	*DIN*
11.	GENERAL EPITAXIAL LAYER CHARACTERISTICS										
11.1	Conductivity Type/Structure	NO	NO	YES	Sec 3	Sec 3					
11.2	Dopant	NO	NO	YES	Sec 3	Sec 3					
11.3	Silicon Source Gas	NO	NO	NO	Sec 3	Sec 3					
11.4	Growth Method	NO	NO	NO	Sec 3	Sec 3					
11.5	Net Carrier Density (Resistivity)	NO	NO	YES	Sec 3	Sec 3		F 419	MF1392, MF1393 (MF374, MF398, MF525, MF723)		50439 (50444, 50447)
11.6	Net Carrier Density Variation (Resistivity Variation)	YES	NO	YES	Sec 3, 5	Sec 3, 5					50439
11.7	Thickness	NO	NO	YES	Sec 3	Sec 3			MF95, MF110, MF672		50436, 50437
11.8	Thickness Variation	YES	NO	YES	Sec 3, 5	Sec 3, 5					
11.9	Transition Width	NO	NO	NO							
11.10	Flat Zone	NO	NO	NO							
11.11	Phantom Layer	NO	NO	NO							
12.	MECHANICAL CHARACTERISTICS[D]										
12.1	Bow	NO	NO	NO	M1 Sec 9	M1 Sec 9			MF534	H 611	
12.2	Warp	NO	NO	NO	M1 Sec 9	M1 Sec 9			MF657, MF1390		
12.3	Sori	NO	NO	NO	M1 Sec 9	M1 Sec 9					
12.4	Flatness/Global	NO	NO	NO	M1 Sec 9	M1 Sec 9	DEF 43		MF1530		50441/3
12.5	Flatness/Site	NO	NO	NO	M1 Sec 9	M1 Sec 9			MF1530		
12.6	Fixed Quality Area	NO	NO	NO	M1 Sec 9	M1 Sec 9			MF1530		
13.	EPITAXIAL LAYER VISUAL INSPECTION CHARACTERISTICS[D]										
13.1	Stacking Faults	YES	YES	NO	Table 1	Table 1		F 522			50446
13.2	Slip	YES	YES	NO	Table 1	Table 1		F 47, F 80	MF523		50446
13.3	Large Point Defects	YES	YES	NO	Table 1	Table 1		F 815	MF523		50446
13.4	Total Point Defects	YES	YES	NO	Table 1	Table 1		F 815	MF523		50446
13.5	Scratches	YES	YES	NO	Table 1	Table 1			MF523		
13.6	Dimples	YES	YES	NO	Table 1	Table 1			MF523		
13.7	Orange Peel	YES	YES	NO	Table 1	Table 1			MF523		
13.8	Cracks/Fractures	YES	YES	NO	Table 1	Table 1			MF523		
13.9	Crow's Feet	YES	YES	NO	Table 1	Table 1			MF523		
13.10	Edge Chips	YES	YES	NO	Table 1	Table 1			MF523		
13.11	Edge Crown	YES	YES	NO	Table 1	Table 1					50446
13.12	Haze	YES	YES	NO	Table 1	Table 1			MF523		50446

ITEM		VALUE			STANDARD REFERENCE[A]			STANDARD TEST METHODS			
		IS IN M2	IS IN M11	IS REQ'D[B]	SEMI M2	SEMI M11	JEIDA	ASTM	SEMI	JIS JEIDA	DIN
13.13	Foreign Matter	YES	YES	NO	Table 1	Table 1			MF523		
14.	BACK SURFACE VISUAL INSPECTION CHARACTERISTICS										
14.1	Contamination	YES	YES	NO	Table 1	Table 1			MF523		
15.	OTHER CHARACTERISTICS										

Annealed Wafer

ITEM		VALUE		STANDARD REFERENCE[A]		STANDARD TEST METHODS			
		IS IN SEMI	IS REQ'D[B]	SEMI	JEIDA	ASTM	SEMI	JIS JEIDA	DIN
20.	GENERAL ANNEALED WAFER CHARACTERISTICS								
20.1	Annealing Atmosphere	NO	YES						
20.2	Co-Dopant in Crystal	NO	YES						
21.	MECHANICAL CHARACTERISTICS[D]								
21.1	Bow	YES	NO	M1 Sec 9			MF534	H 611	
21.2	Warp	YES	NO	M1 Sec 9			MF657, MF1390		
21.3	Sori	NO	NO	M1 Sec 9			MF1451	43	
21.4	Flatness/Global	NO	NO	M1 Sec 9			MF1530		50441/3
21.5	Flatness/Site	NO	NO	M1 Sec 9			MF1530		
21.6	Fixed Quality Area	NO	NO	M1 Sec 9			MF1530		
22.	FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS[D]								
22.1	Stacking Faults	YES	NO	M2 Table 1			MF1810		50446
22.2	Slip	YES	NO	M2 Table 1			MF523, MF1726		50446
22.3	Other Defect	YES	NO	M2 Table 1			MF523, MF1726		50446
23.	BACK SURFACE VISUAL INSPECTION CHARACTERISTICS								
23.1	Contamination	YES	NO	M1 Table 1			MF523		
23.2	Other								
24.	OTHER CHARACTERISTICS								
24.1	Depth of BMD Denuded Zone	NO	NO						
24.2	BMD Density	NO	NO				MF1239		
24.3	Other								

SOI Wafer

ITEM		*VALUE*		*STANDARD REFERENCE*[A]		*STANDARD TEST METHODS*		
		IS IN M47	*IS REQ'D*[B]	*SEMI M47*	*JEITA*	*SEMI*	*JIS JEITA*	*DIN*
25	SOI LAYER CHARACTERISTICS							
25.0	Type of SOI	YES	YES	Table 1				
25.1	Starting silicon wafer for SOI	YES	NO	Table 1				
25.2	Surface Silicon Thickness	YES	YES	Table 1				
25.3	Surface Silicon Thickness Mean Value Variation	YES	NO	Table 1				
25.4	Surface Silicon Thickness Variation in Wafer	YES	YES	Table 1				
25.5	Crystal Orientation	YES	NO	Table 1		SEMI MF26		
25.6	Rotation Misalignment	YES	NO	Table 1				
25.7	Edge Exclusion, Nominal	YES	NO	Table 1				
25.8	Non-SOI Edge Area	YES	NO	Table 1				
25.9	Conductivity Type	YES	NO	Table 1		SEMI MF42		
25.10	Dopant	YES	NO	Table 1				
25.11	Dopant Concentration	YES	NO	Table 1				
25.12	SOI Etch Pit	YES	NO	Table 1				
25.13	Threading Dislocation	YES	NO	Table 1				
25.14	HF Defect	YES	NO	Table 1				
25.15	Void	YES	NO	Table 1				
25.16	Roughness (Si surface) rms @ 2 × 2 µm	YES	NO	Table 1			EM-3505	
	Roughness (Si surface) rms @ 10 × 10 µm	YES	NO	Table 1			EM-3505	
	Roughness (Si surface) rms @ [ ] × [ ] µm	YES	NO	Table 1			EM-3505	
	Roughness (Si surface) rms @ [ ] × [ ] µm	YES	NO	Table 1			EM-3505	
25.17	Surface Metal Contamination (Fe)	YES	NO	Table 1		SEMI MF1526		
	Surface Metal Contamination (Cr)	YES	NO	Table 1		SEMI MF1526		
	Surface Metal Contamination (Ni)	YES	NO	Table 1		SEMI MF1526		
	Surface Metal Contamination (Cu)	YES	NO	Table 1		SEMI MF1526		
	Surface Metal Contamination [ ]	NO	NO			SEMI MF1526		
	Surface Metal Contamination [ ]	NO	NO			SEMI MF1526		
	Surface Metal Contamination [ ]	NO	NO			SEMI MF1526		
	Surface Metal Contamination [ ]	NO	NO			SEMI MF1526		
	Surface Metal Contamination [ ]	NO	NO			SEMI MF1526		
	Surface Metal Contamination [ ]	NO	NO			SEMI MF1526		
26	BOX CHARACTERISTICS							
26.1	BOX Thickness	YES	YES	Table 1				

ITEM		VALUE		STANDARD REFERENCE[A]		STANDARD TEST METHODS		
		IS IN M47	IS REQ'D[B]	SEMI M47	JEITA	SEMI	JIS JEITA	DIN
26.2	BOX Thickness Variation	YES	YES	Table 1				
26.3	Bonded Interface Location	YES	NO	Table 1				
26.4	BOX Pinholes	YES	NO	Table 1				
26.5	Dielectric Breakdown	YES	NO	Table 1				
27	MECHANICAL CHARACTERISTICS							
27.1	Warp	YES	NO	M1 Sec 9		SEMI MF1390		
27.2	Flatness-site	YES	NO	M1 Sec 9				
28	FRONT SURFACE INSPECTION CHARACTERISTICS							
28.1	Scratch	YES	NO	M1 Table 1		SEMI MF523		
28.2	Haze	YES	NO	M1 Table 1		SEMI MF523		
28.3	LLS @ particle size	YES	NO	M1 Table 1 M35				
28.4	Slip	YES	NO			SEMI MF523		
28.5	Edge Chip	YES	NO	M1 Table 1		SEMI MF523		
28.6	Edge Crack	YES	NO	M1 Table 1		SEMI MF523		
28.7	Foreign Matter	YES	NO	M35		SEMI MF523		
29	BACK SURFACE CHARACTERISTICS							
29.1	Backside Metal Contamination (Fe)	YES	NO	Table 1				
	Backside Metal Contamination (Cr)	YES	NO	Table 1				
	Backside Metal Contamination (Ni)	YES	NO	Table 1				
	Backside Metal Contamination (Cu)	YES	NO	Table 1				
	Backside Metal Contamination [ ]	NO	NO					
	Backside Metal Contamination [ ]	NO	NO					
	Backside Metal Contamination [ ]	NO	NO					
	Backside Metal Contamination [ ]	NO	NO					
	Backside Metal Contamination [ ]	NO	NO					
	Backside Metal Contamination [ ]	NO	NO					

[A] Item is defined or described and/or a test procedure applicable to the item is included in the cited reference.

[B] Value is/is not required to minimally specify a wafer.

[C] Individual value is not required if wafer is specified according to SEMI M1.

[D] In today's technology, it may be possible to inspect for some of these items using automated laser scanning systems; however, a standard test procedure has yet to be developed. Application of automated inspection must be agreed upon between supplier and user.

Table 2 EDI Code List

Line	Item	EDI Code ID	Sub Param ID
1.1	Growth Method	100001	
1.2	Crystal Orientation	100002	
1.3	Conductivity Type	100003	
1.4	Dopant	100004	
1.5	Nominal Edge Exclusion Distance for Fixed Quality Area	100005	
2.1	Resistivity	100006	

Line	*Item*	*EDI Code ID*	*Sub Param ID*
2.2	Radial Resistivity Variation (RRG)	100007	
2.3	Resistivity Striations	100008	
2.4	Minority Carrier Lifetime	100009	
3.1	Oxygen Concentration	100010	
3.2	Radial Oxygen Variation	100011	
3.3	Carbon Concentration	100012	
3.4	Boron Concentration in Heavily Doped n-type Si	100013	
4.1	Dislocation Etch Pit Density	100014	
4.2	Slip	100015	
4.3	Lineage	100016	
4.4	Twin	100017	
4.5	Swirl	100018	
4.6	Shallow Pits	100019	
4.7	Oxidation Induced Stacking Faults (OSF)	100020	
4.8	Oxide Precipitates (BMD)	100021	
5.1	Wafer ID Marking	100022	
5.2	Front Surface Thin Film(s) Appl	100023	
5.3	Denuded Zone	100024	
5.4	Extrinsic Gettering Treatment	100025	
5.5	Backseal	100026	
5.6	Annealing	100027	
6.01	Dimensions Specified According to SEMI M1.xx	100028	
6.1	Diameter	100029	
6.2	Primary Flat Length/Diameter Notch Dimensions	100030	
6.3	Primary Flat/Notch Orientation	100031	
6.4	Secondary Flat Length	100032	
6.5	Secondary Flat Location	100033	
6.6	Edge Profile	100034	
6.7	Thickness	100035	
6.8	Thickness Variation (TTV)	100036	
6.9	Surface Orientation	100037	
6.10	Bow	100038	
6.11	Warp Method	100039	SEMI MF657
6.11	Warp Method	100040	SEMI MF1390
6.12	Sori	100041	
6.13	Flatness/Global	100042	
6.14	Flatness/Site	100043	SF3R
6.14	Flatness/Site	100044	SF3D
6.14	Flatness/Site	100045	SFLR
6.14	Flatness/Site	100046	SFLD
6.14	Flatness/Site	100047	SFQR
6.14	Flatness/Site	100048	SFQD
6.14	Flatness/Site	100049	SBIR
6.14	Flatness/Site	100050	SBID
7.1	Surface Metal Contamination -- Sodium	100051	
7.1	Surface Metal Contamination -- Aluminum	100052	

Line	*Item*	*EDI Code ID*	*Sub Param ID*
7.1	Surface Metal Contamination -- Potassium	100053	
7.1	Surface Metal Contamination -- Chromium	100054	
7.1	Surface Metal Contamination -- Iron	100055	
7.1	Surface Metal Contamination -- Nickel	100056	
7.1	Surface Metal Contamination -- Copper	100057	
7.1	Surface Metal Contamination -- Zinc	100058	
7.1	Surface Metal Contamination -- (Producer-User Defined Metal)	100059	
7.1	Surface Metal Contamination -- (Producer-User Defined Metal)	100060	
7.1	Surface Metal Contamination -- (Producer-User Defined Metal)	100061	
7.1	Surface Metal Contamination -- (Producer-User Defined Metal)	100062	
7.1	Surface Metal Contamination -- (Producer-User Defined Metal)	100063	
7.1	Surface Metal Contamination -- (Producer-User Defined Metal)	100064	
7.2	Surface Organics	100065	
8.01	Front Surface Visual Inspection Specified According to SEMI M1 Table 1	100066	
8.1	Scratches	100067	
8.2	Pits	100068	
8.3	Haze	100069	
8.4	Localized Light Scatterers (LLS)	100070	$\geq 0.50\mu$
8.4	Localized Light Scatterers (LLS)	100071	$\geq 0.30\mu$
8.4	Localized Light Scatterers (LLS)	100072	$\geq 0.20\mu$
8.4	Localized Light Scatterers (LLS)	100073	$\geq 0.19\mu$
8.4	Localized Light Scatterers (LLS)	100074	$\geq 0.18\mu$
8.4	Localized Light Scatterers (LLS)	100075	$\geq 0.17\mu$
8.4	Localized Light Scatterers (LLS)	100076	$\geq 0.16\mu$
8.4	Localized Light Scatterers (LLS)	100077	$\geq 0.15\mu$
8.4	Localized Light Scatterers (LLS)	100078	$\geq 0.14\mu$
8.4	Localized Light Scatterers (LLS)	100079	$\geq 0.13\mu$
8.4	Localized Light Scatterers (LLS)	100080	$\geq 0.12\mu$
8.4	Localized Light Scatterers (LLS)	100081	$\geq 0.11\mu$
8.4	Localized Light Scatterers (LLS)	100082	$\geq 0.10\mu$
8.4	Localized Light Scatterers (LLS)	100083	$\geq 0.09\mu$
8.4	Localized Light Scatterers (LLS)	100084	$\geq 0.08\mu$
8.4	Localized Light Scatterers (LLS)	100085	$\geq 0.07\mu$
8.4	Localized Light Scatterers (LLS)	100086	$\geq 0.06\mu$
8.4	Localized Light Scatterers (LLS)	100087	$\geq 0.05\mu$
8.4	Localized Light Scatterers (LLS)	100088	$\geq 0.04\mu$
8.4	Localized Light Scatterers (LLS)	100089	$\geq 0.03\mu$
8.4	Localized Light Scatterers (LLS)	100090	$\geq 0.02\mu$
8.5	Contamination/Area	100091	
8.6	Edge Chips	100092	
8.7	Edge Cracks	100093	
8.8	Cracks, Crow's Feet	100094	
8.9	Craters	100095	
8.10	Dimples	100096	
8.11	Grooves	100097	
8.12	Mounds	100098	

Line	*Item*	*EDI Code ID*	*Sub Param ID*
8.13	Orange Peel	100099	
8.14	Saw Marks	100100	
8.15	Dopant Striation Rings	100101	
8.16	Stains	100102	
9.01	Back Surface Visual Inspection Specified According to SEMI M1 Table 1	100103	
9.1	Edge Chips	100104	
9.2	Cracks, Crow's Feet	100105	
9.3	Contamination/Area	100106	
9.4	Saw Marks	100107	
9.5	Stains	100108	
9.6	Roughness	100109	
9.7	Brightness	100110	
11.1	Conductivity Type/Structure	100111	
11.2	Dopant	100112	
11.3	Silicon Source Gas	100113	
11.4	Growth Method	100114	
11.5	Net Carrier Density (Resistivity)	100115	
11.6	Net Carrier Density Variation	100116	
11.7	Thickness	100117	
11.8	Thickness Variation	100118	
11.9	Transition Width	100119	
11.10	Flat Zone	100120	
11.11	Phantom Layer	100121	
12.1	Bow	100122	
12.2	Warp Method	100123	SEMI MF657
12.2	Warp Method	100124	SEMI MF1390
12.3	Sori	100125	
12.4	Flatness/Global	100126	
12.5	Flatness/Site	100127	SF3R
12.5	Flatness/Site	100128	SF3D
12.5	Flatness/Site	100129	SFLR
12.5	Flatness/Site	100130	SFLD
12.5	Flatness/Site	100131	SFQR
12.5	Flatness/Site	100132	SFQD
12.5	Flatness/Site	100134	SBIR
13.01	Epi Front Surface Visual Inspection Specified According to SEMI M2 Table 1 or SEMI M11 Table 1	100135	
13.1	Stacking Faults	100136	
13.2	Slip	100137	
13.3	Large Point Defects	100138	
13.4	Total Points Defects	100139	
13.5	Scratches	100140	
13.6	Dimples	100141	
13.7	Orange Peel	100142	
13.8	Cracks/Fractures	100143	
13.9	Crow's Feet	100144	

Line	*Item*	*EDI Code ID*	*Sub Param ID*
13.10	Edge Chips	100145	
13.11	Edge Crown	100146	
13.12	Haze	100147	
13.13	Foreign Matter	100148	
14.1	Contamination	100149	
16.1	Mask ID	100150	
16.2	Alignment Precision	100151	
16.3	Pattern Line Width Tolerance	100152	
17.1	Dopant	100153	
17.2	Diffusion Depth (xj)	100154	
17.3	Sheet Resistance	100155	
17.4	Pattern Step Height	100156	
17.5	Defect Density (Before Epi)	100157	
18.1	Pattern Shift Ratio	100158	
18.2	Pattern Distortion Ratio	100159	
6.14	Flatness/Site	100160	SFSR
12.5	Flatness/Site	100161	SFSR
4.9	Interstitial Oxygen Reduction (ΔOi)	100162	
6.15	Fixed Quality Area	100164	
10.1	Bulk defects by X-ray topography	100169	
12.6	Fixed Quality Area	100172	
9.8	Scratches – macro	100165	
9.9	Scratches – micro	100166	
9.10	Localized Light Scatterers (LLS)[4]	100167	
9.10	Localized Light Scatterers (LLS)[4]	100168	
11.01	[ ] Specified According to SEMI M11 Table [ ]	100170	
12.01	[ ] Specified According to SEMI M11 Table [ ]	100171	
13.14	Localized Light Scatterers (LLS)[4]	100173	≥ 0.50µ
13.14	Localized Light Scatterers (LLS)[4]	100174	≥ 0.30µ
13.14	Localized Light Scatterers (LLS)[4]	100175	≥ 0.20µ
13.14	Localized Light Scatterers (LLS)[4]	100176	≥ 0.19µ
13.14	Localized Light Scatterers (LLS)[4]	100177	≥ 0.18µ
13.14	Localized Light Scatterers (LLS)[4]	100178	≥ 0.17µ
13.14	Localized Light Scatterers (LLS)[4]	100179	≥ 0.16µ
13.14	Localized Light Scatterers (LLS)[4]	100180	≥ 0.15µ
13.14	Localized Light Scatterers (LLS)[4]	100181	≥ 0.14µ
13.14	Localized Light Scatterers (LLS)[4]	100182	≥ 0.13µ
13.14	Localized Light Scatterers (LLS)[4]	100183	≥ 0.12µ
13.14	Localized Light Scatterers (LLS)[4]	100184	≥ 0.11µ
13.14	Localized Light Scatterers (LLS)[4]	100185	≥ 0.10µ
13.14	Localized Light Scatterers (LLS)[4]	100186	≥ 0.09µ
13.14	Localized Light Scatterers (LLS)[4]	100187	≥ 0.08µ
13.14	Localized Light Scatterers (LLS)[4]	100188	≥ 0.07µ
13.14	Localized Light Scatterers (LLS)[4]	100189	≥ 0.06µ
13.14	Localized Light Scatterers (LLS)[4]	100190	≥ 0.05µ
13.14	Localized Light Scatterers (LLS)[4]	100191	≥ 0.04µ

Line	*Item*	*EDI Code ID*	*Sub Param ID*
13.14	Localized Light Scatterers (LLS)[4]	100192	≥ 0.03µ
13.14	Localized Light Scatterers (LLS)[4]	100193	≥ 0.02µ
13.15	Surface Edge Exclusion	100194	
14.01	[ ] Specified According to SEMI M11 Table [ ]	100195	
14.2	Scratches -- macro	100196	
14.3	Scratches -- micro	100197	
14.4	Localized Light Scatterers	100198 100199	
20.1	Annealing Atmosphere	100200	
20.2	Other Dopant in Crystal	100201	
21.1	Bow	100202	
21.2	Warp	100203	SEMI MF657
21.2	Warp	100204	SEMI MF1390
21.3	Sori	100205	
21.4	Flatness/Global	100206	
21.5	Flatness/Site	100207	SF3R
21.5	Flatnes/Site	100208	SF3D
21.5	Flatness/Site	100209	SFLR
21.5	Flatness/Site	100210	SFLD
21.5	Flatness/Site	100211	SFQR
21.5	Flatness/Site	100212	SFQD
21.5	Flatness/Site	100213	SBIR
21.5	Flatness/Site	100214	SFSR
21.6	Fixed Quality Area	100215	
22.1	Stacking Faults	100216	
22.2	Slip	100217	
23.1	Contamination	100218	
24.1	Depth of BMD Denuded Zone	100219	
24.2	BMD Density	100220	
6.14	Flatness/Site	100221	SFSD
12.5	Flatness/Site	100222	SFSD
12.5	Flatness/Site	100223	SBID
21.5	Flatness/Site	100224	SFSD
21.5	Flatness/Site	100225	SBID
25.0	Type of SOI	100226	
25.1	Starting silicon wafer for SOI	100227	
25.2	Surface Silicon Thickness	100228	
25.3	Surface Silicon Thickness Mean Value Variation	100229	
25.4	Surface Silicon Thickness Variation in Wafer	100230	
25.5	Crystal Orientation	100231	
25.6	Rotation Misalignment	100232	
25.7	Edge Exclusion, Nominal	100233	
25.8	Non-SOI Edge Area	100234	
25.9	Conductivity Type	100235	
25.10	Dopant	100236	
25.11	Dopant Concentration	100237	

Line	*Item*	*EDI Code ID*	*Sub Param ID*
25.12	SOI Etch Pit	100238	
25.13	Threading Dislocation	100239	
25.14	HF Defect	100240	
25.15	Void	100241	
25.16	Roughness (Si surface) rms @ 2 × 2μm	100242	
	Roughness (Si surface) rms @ 10 × 10μm	100243	
	Roughness (Si surface) rms @ [ ] × [ ]μm	100244	
	Roughness (Si surface) rms @ [ ] × [ ]μm	100245	
25.17	Surface Metal Contamination (Fe)	100246	
	Surface Metal Contamination (Cr)	100247	
	Surface Metal Contamination (Ni)	100248	
	Surface Metal Contamination (Cu)	100249	
	Surface Metal Contamination [ ]	100250	
	Surface Metal Contamination [ ]	100251	
	Surface Metal Contamination [ ]	100252	
	Surface Metal Contamination [ ]	100253	
	Surface Metal Contamination [ ]	100254	
	Surface Metal Contamination [ ]	100255	
26.1	BOX Thickness	100256	
26.2	BOX Thickness Variation	100267	
26.3	Bonded Interface Location	100258	
26.4	BOX Pinholes	100259	
26.5	Dielectric Breakdown	100260	
27.1	Warp	100261	
27.2	Flatness-site	100262	
28.1	Scratch	100263	
28.2	Haze	100264	
28.3	LLS @particle size	100265 100266	
28.4	Slip	100267	
28.5	Edge Chip	100268	
28.6	Edge Crack	100269	
28.7	Foreign Matter	100270	
29.1	Backside Metal Contamination (Fe)	100271	
	Backside Metal Contamination (Cr)	100272	
	Backside Metal Contamination (Ni)	100273	
	Backside Metal Contamination (Cu)	100274	
	Backside Metal Contamination [ ]	100275	
	Backside Metal Contamination [ ]	100276	
	Backside Metal Contamination [ ]	100277	
	Backside Metal Contamination [ ]	100278	
	Backside Metal Contamination [ ]	100279	
	Backside Metal Contamination [ ]	100280	

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SEMI M19-91
SPECIFICATION FOR ELECTRICAL PROPERTIES OF BULK GALLIUM ARSENIDE SINGLE CRYSTAL SUBSTRATES

1 Introduction

For the specification, three principal types of material were identified: semi-insulating, n-type, and p-type. This encompasses the full range of conductivity characteristics for Gallium Arsenide (GaAs). Section 3 considers subclasses of these characteristics defining the species which may be used for producing the conductivity type. For semi-insulating material, special cases have been isolated.

Undoped, Grade A1 represents those materials which are of high resistivity and stable following growth, without necessitating any additional annealing or processing. The Grade A2 material, "high purity", requires additional thermal processing following growth to bring the resistivity to a level > 10^7 Ω-cm. At this time, most producers have indicated that the majority of the Grade A2 ingots have resistivity characteristics which rise into the acceptable range after an appropriate thermal cycle. However, this phenomenon is sensitive to the details of the time-temperature cycle, and thus, such an increase cannot be guaranteed in every application. Thus, the label "Grade A2" is used to denote this material.

Chromium doping produces a high resistivity material. However, due to the rapid diffusion of Cr during processing and the propensity for surface accumulation, it is not as well suited to processing as grades 3.A.1 and 3.A.2, thus we assign this material "grade A".

Iso-electric dopant additions do not appear to affect the resistivity significantly, but rather, permit the reduction of dislocation generation in the final product. Thus, this material is classified Grade A. While In is the most effective hardening agent, Al, P, and Sb are also viable species. They are included for completeness and to reduce the likelihood of document revision at a later date. The Grade B specification encompasses those materials where the impurity and point defect densities are not quite in the proper balance, but the resistivity is suitable for less-stringent applications.

For conducting material, the best characterized, non-transition metal species have been included as n-type dopants; for p-type, a broader range of species has been included, as transition metals are useful acceptor impurities.

Section 4 defines the resistivity and stability of semi-insulating material as specified in Section 3. A stringent limit was placed on the Grade A2 material to minimize the likelihood that this material converts to low resistivity upon annealing. The issue of surface conversion in Cr-doped material was dealt with by eliminating a requirement for n-type characteristics following annealing.

The resistivity ranges for n-type conducting material were determined from the carrier concentration table (Section 5) and mobility values, using the analysis of Walukiewicz et al, J. Appl. Phys. 50 (1979) 899. This places a constraint on the permissible compensation ratio, selected to be in the range of approximately 0.0 to 0.7. The specification was designed then to exclude abnormally poor crystals. As limited data and demand exist for p-type material, there are no ranges specified at this writing. Should a significant body of data evolve, this specification may be designed and balloted as appropriate.

Section 5 deals with impurity concentrations, net electron yields and implicitly, with point defect concentrations. For semi-insulating material of high quality, the impurities are, at the present time, not reliably measurable (carbon is the notable exception). Thus the "unspecified" nomenclature. For types A-3 and A-4, the determination of the amount of the relevant impurity species is given to the appropriate party, the user, and producer, respectively.

For n-type materials, the ranges were selected to define a high purity regime ($n \leq 4 \times 10^{16}$ cm^{-3}), an intermediate regime where donor density is not more than ~10 times the typical deep level density; the transition region wherein deep levels are suppressed (range B-3); a highly doped range (> 10 ppm net electron concentration yield); and "saturation" doping range where the crystal growth process and thermodynamics determine the limits of impurity incorporation and electron yield.

In Section 6, the electron mobility values and ranges are stated. For semi-insulating materials, the values that have been determined by consensus are 5000 cm^2/V-s for Grade A1 and 6000 cm^2/V-s. In the interest of harmony, and to prevent further debilitating discussions, the authors and participants at the SEMI meetings, and responses from producers have been used to set this value at 5000 cm^2/V-s. The producers indicated that the Grade A2 material nearly always exceeds 6000 cm^2/V-s, and thus this value was adopted. For chromium doped materials, the mobility is less predictable and, therefore, is negotiated between the user and producer. In-doped materials have consistently lower mobilities, resulting from strain-effects,

scattering, and other related phenomena. Thus, based on producer experience, the minimum value was set at 3500 cm^2/V-s.

For n-type materials, the mobility ranges were selected to represent compensation ratios in the range of approximately 0.0 to 0.7 for a given net electron concentration. P-type material is not yet characterized sufficiently to warrant a specification.

2 Scope

This document specifies the characteristics and ranges of electrical properties for bulk GaAs crystals and substrate wafers. For high resistivity and n-type conducting materials, the permissible growth conditions or impurity species are stated; the electrical properties corresponding to the appropriate range(s) are noted. Due to the limited understanding, experience and demand for p-type materials only guidelines are provided in this specification at the present writing.

3 Conductivity Type

A. Semi-insulating, n-type

B. Conducting, n-type

C. Conducting, p-type

4 Dopant Species

A. 1. Undoped; Grade A1

2. Undoped; Grade A2

3. Chromium; Grade A

4. Isoelectronic impurity; Grade A Dopant specified by producer: In, Al, P, Sb

5. Undoped; Grade B

B. Dopant specified by user: Si, S, Se, Te, Sn

C. Dopant specified by user: Zn, Cd, Be, Mn, Fe, Co, Mg

NOTE See Sections 4 and 5 below for grade definition.

5 Resistivity at 300K

A. Semi-insulating, n-type*

B. 1. $\geq 1 \times 10^7$ Ω-cm, n-type before and after anneal

2. $\geq 5 \times 10^6$ Ω-cm becoming $\geq 1 \times 10^7$ Ω-cm after anneal n-type before and after anneal

3. $\geq 1 \times 10^7$ Ω-cm, n-type before anneal

4. $\geq 1 \times 10^7$ Ω-cm, n-type before and after anneal

5. $\geq 5 \times 10^6$ Ω-cm, n-type before and after anneal

1×10^7 Ω-cm = 1.6×10^8 Ω/❒; 5×10^6 Ω-cm = 8×10^7 Ω/❒;

* 1×10^6 Ω-cm = 1.6×10^7 Ω/❒ based on 625 μm wafer thickness

C. Conducting, n-type

D. 1. ≥ 0.0026 Ω-cm (at n – 4×10^{16} cm^{-3}; μ = 6000 cm^2/V-s

2. ≤ 0.06 Ω-cm

3. ≤ 0.042 Ω-cm

4. ≤ 0.012 Ω-cm

5. $< 5.2\ 10^{-3}$ Ω-cm

6. to be determined between user and producer

NOTE Ranges overlap due to the interrelationship of ρ, n, and μ.

E. Ranges to be determined between the user and producer.

6 Free Carrier or Impurity Concentration

A. 1. Unspecified impurity concentration

2. Unspecified impurity concentration

3. Cr concentration range in atomic ppm specified by user

4. Isoelectronic impurity concentration range in atomic ppm specified by producer

5. Unspecified impurity concentration

6. To be determined between user and producer

B. 1. $\leq 4 \times 10^{16}$ cm^{-3}

2. $> 4 \times 10^{16} – 1 \times 10^{17}$ cm^{-3}

3. $> 1 \times 10^7 – 5 \times 10^{17}$ cm^{-3}

4. $> 5 \times 10^7 – 3 \times 10^{18}$ cm^{-3}

5. $> 3 \times 10^{18}$ cm^{-3}

C. Carrier concentration agreed upon between user and producer

7 Electron Mobility, 300K (determined by Hall Effect)

A. 1 ≥ 5000 cm^2/V-s

2. ≥ 6000 cm^2/V-s