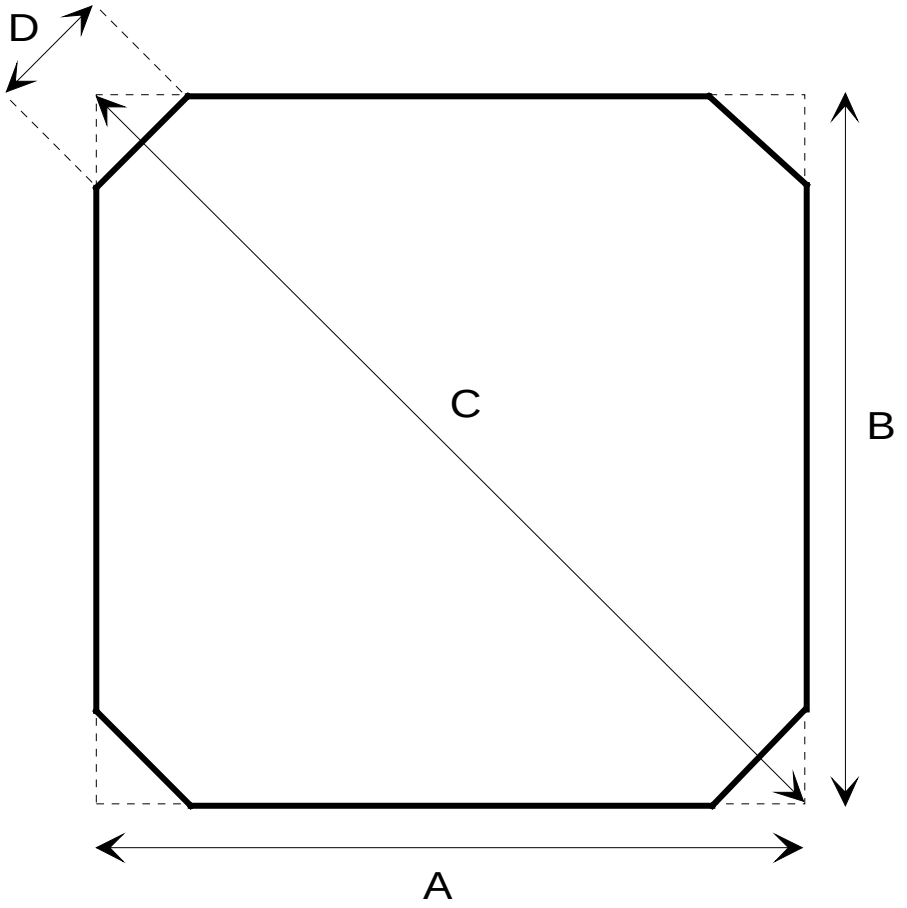

Figure 1
Rectangular Mainly Square Photovoltaic Solar Cell Silicon Wafer Dimensions

Table 2 Rectangular Mainly Square Photovoltaic Solar Cell Silicon Wafer Dimensions (letters as in Figure 1)

Nominal Size (mm)	*Dimensions (mm)*							
	A		*B*		*C*		*D*	
	Max.	*Min.*	*Max.*	*Min.*	*Max.*	*Min.*	*Max.*	*Min.*
100	101	99	101	99	142.8	140.0	2.0	0.5
125	126	124	126	124	187.2	175.4	2.0	0.5
150	151	149	151	149	213.5	210.7	2.0	0.5
200	201	199	201	199	284.3	281.4	2.0	0.5

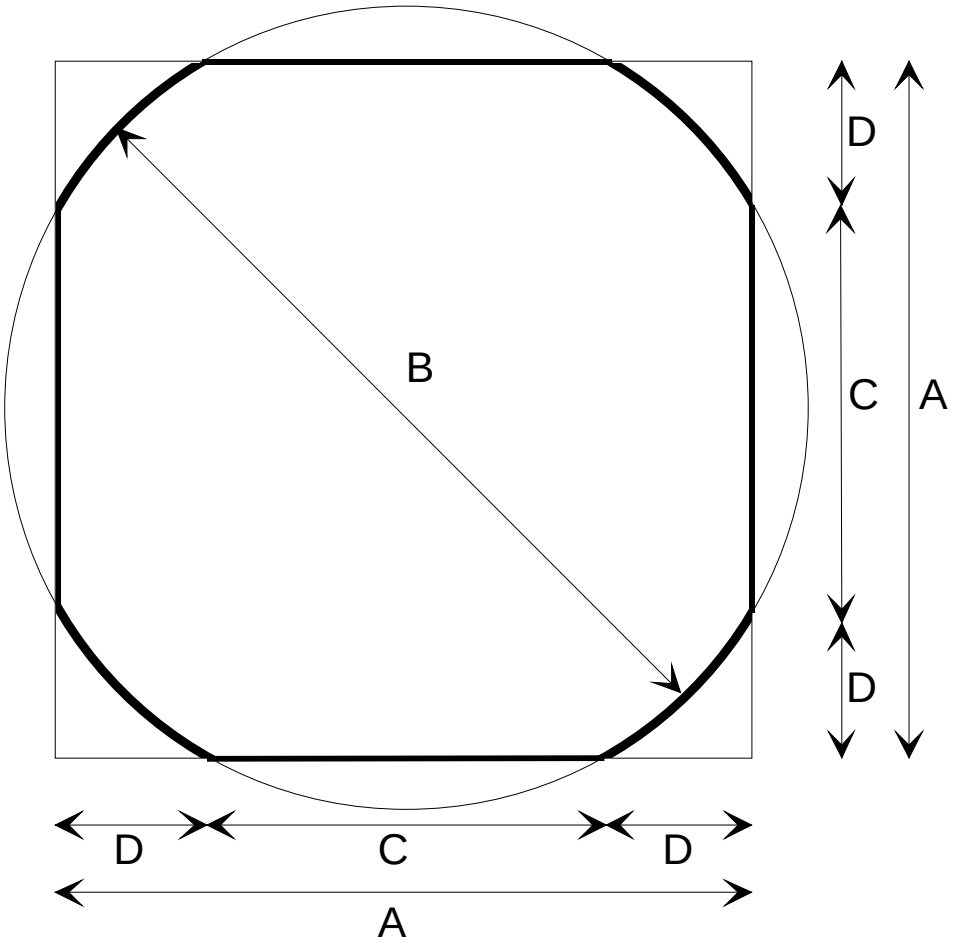

Figure 2
Pseudo-Square Monocrystalline Photovoltaic Solar Cell Silicon Wafer Dimensions

Table 3 Pseudo-Square Monocrystalline Photovoltaic Solar Cell Silicon Wafer Dimensions (letters as in Figure 2)

Nominal size (mm)	*Dimensions (mm)*							
	A		*B*		*C*		*D*	
	Min.	*Max.*	*Min.*	*Max.*	*Min.*	*Max.*	*Min.*	*Max.*
100	99	101	124	126	71.9	77.9	10.6	14.6
125	124	126	149	151	79.5	86.2	23.2	28.9
150	149	151	174	176	86.4	93.7	27.6	32.3

APPENDIX 1

NOTE: The material in this appendix is an official part of SEMI M6 and was approved by full letter ballot procedures on July 28, 2000 by the European Regional Standards Committee.

A1-1 *Crystal Orientation of Monocrystalline silicon wafers*

A1-1.1 A typical crystal orientation for monocrystalline silicon wafers is <100>.in the plane of the wafer.

A1-2 *Wafer resistivity*

A1-2.1 Typical wafer resistivity is between 0.5 Ω-cm and 2 Ω-cm.

A1-3 *Oxygen and Carbon Contents*

A1-3.1 Typical values.

A-1.3.1.1 Interstitial oxygen $< 1 \times 10^{18}$ at/cm^3 for CZ material and less than 8×10^{17} at/cm^3 for multicrystalline wafers.

A-1.3.1.2 Substitutional carbon $< 5 \times 10^{17}$ at/cm^3 for CZ and 1×10^{18} at/cm^3 for multicrystalline material.

A1-4 *Lifetime and Minority Carrier Diffusion Length*

A1-4.1 Typical minority carrier lifetime values for wafers used in the solar cell manufacturing process lie in a range between 1 μs and 20 μs.

SEMI M8-0703
SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON TEST WAFERS

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on April 11, 2003. Initially available at www.semi.org June 2003; to be published July 2003. Originally published in 1984; previously published March 2001.

NOTICE: This document was completely rewritten in 2003.

1 Purpose

1.1 This specification covers requirements for virgin silicon test wafers to be used for mechanical testing, and routine process monitoring in semiconductor manufacturing.

2 Scope

2.1 This specification covers dimensional and crystallographic properties of monocrystalline virgin silicon test wafers together with selected electrical and surface defect characteristic.

2.2 This specification covers virgin test wafers in all standard wafer diameters from 2 inch to 300 mm. It classifies test wafers according to the items specified. It provides three classes of smaller diameter test wafers (through 125 mm), and two classes of larger diameter test wafers (from 150 mm).

2.3 This specification does not cover test wafers intended for applications placing higher demands on silicon wafers, such as particle counting, measuring resolution in a photolithography process, or monitoring metallic contamination; for wafers to be used in these applications, the user should reference SEMI M24.

2.4 For referee purposes, U.S. customary units shall be used for wafers of 2- and 3-inch nominal diameter and SI (System International), commonly called metric units, for 100 mm and larger diameter wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standard*s

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

3.2 ASTM Standards[1]

F1241 — Standard Terminology of Silicon Technology

3.3 *Other Standards*

A comprehensive list of applicable standard test methods from a variety of sources is given in Table 1 of SEMI M18.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions of terms related to silicon wafer technology are given in ASTM Terminology F1241.

4.2 Definitions for some additional relevant terms are given in SEMI M1.

4.3 The following definitions apply in the context of this specification:

4.4 *Definitions*

4.4.1 *mechanical test wafer* — silicon wafer suitable for testing equipment with emphasis on dimensional and structural characteristics only.

4.4.2 *process test wafer* — silicon wafer suitable for process monitoring as well as some processing applications in semiconductor manufacturing. Also called *monitor wafer*.

4.4.3 *virgin test wafer* — test wafer that has not been used previously in semiconductor manufacturing.

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

5 Ordering Information

5.1 *Small Diameter Wafers*

5.1.1 Items that may be specified when ordering silicon wafers are listed in SEMI M18. Not all of these items are required for ordering small diameter (2 in., 3 in., 100 mm, and 125 mm) test wafers. The following items are included in the three specification groups shown in Table 1; numbers in square brackets following the item are the item numbers in SEMI M18:

5.1.1.1 *Group 1*, *General and Geometrical* — Growth method [1.1], diameter [6.1], surface orientation [6.9], thickness [6.7], orientation fiducials (flats and notches) [6.2–6.5], and edge profile [6.6].

5.1.1.2 *Group 2, Surface Characteristics* — Surface defects as listed in Tables 3 and 4 [7.1–7.2, 8.1–8.16].

5.1.1.3 *Group 3, Basic Intrinsic Properties* — Conductivity type [1.3], dopant [1.4], and resistivity [2.1].

Table 1 Classifications for Small Diameter Wafers

Classification	*Applicable Specification Groups*
A	1, 2, 3
B	1, 2
C	1

5.1.2 Not all of the above items must be specified explicitly; the specifications for many of the items are determined by the combination of wafer classification and nominal diameter. In all cases, the following must be specified on the purchase order for all classes of small diameter test wafers:

5.1.2.1 Wafer Classification (A, B or C),

5.1.2.2 Nominal diameter and surface orientation,

5.1.2.3 Growth method (see Section 7.1),

5.1.2.4 Lot acceptance procedures (see Section 9.1),

5.1.2.5 Certification (if required) (see Section 12),

5.1.2.6 Packing and Marking (see Section 13),

5.1.2.7 Any options listed in the table, and

5.1.2.8 Appropriate test methods when more than one is listed for the parameter in Table 1 of SEMI M18.

5.1.3 For Class A and B test wafers, that require controlled surface characteristics, certain surface defect limits (see Section 11), must be specified in addition to the items listed in Section 5.1.2, see Table 3, Sections 8.1–8.16.

5.1.4 For Class A wafers, the following must be specified in addition to the items listed in Sections 5.1.2 and 5.1.3 (see Section 8.1):

5.1.4.1 Conductivity type

5.1.4.2 Resistivity

5.2 *Large Diameter Wafers*

5.2.1 Items that may be specified when ordering silicon wafers are listed in SEMI M18. Not all of these items are required for ordering large diameter (150, 200, and 300 mm) test wafers. The following items are included in the two specification groups shown in Table 2; numbers in square brackets following the item are the item numbers in SEMI M18.

Table 2 Wafer Classifications for Large Diameter Wafers

Classifications	*Applicable Specification Groups*
Mechanical	1
Process	1, 2

5.2.1.1 *Group 1, General and Geometrical* — Growth method [1.1], diameter [6.1], surface orientation [6.9], thickness [6.7], orientation fiducials (flats and notches) [6.2–6.5], and edge profile [6.6].

5.2.1.2 *Group 2, Surface and Intrinsic Properties* — Surface defects as listed in Table 3 [7.1–7.2, 8.1–8.16], conductivity type [1.3], dopant [1.4], and resistivity [2.1].

5.2.2 Not all the specifications must be specified explicitly; the specifications for many of the items are determined by wafer classification and nominal diameter. In all cases the following must be specified on the purchase order for all classes of large diameter test wafers:

5.2.2.1 Wafer Classification (*Mechanical* or *Process),*

5.2.2.2 Nominal diameter and surface orientation,

5.2.2.3 Growth method (see Section 7.1),

5.2.2.4 Lot acceptance procedures (see Section 9.1),

5.2.2.5 Certification (if required) (see Section 12),

5.2.2.6 Packing and Marking (see Section 13),

5.2.2.7 Any options listed in the table, and

5.2.2.8 Appropriate test methods when more than one is listed for the parameter in Table 1 of SEMI M18.

6 Dimensions and Permissible Variations

6.1 The material shall conform to the parameters as specified in Table 3, 4, or 5.

6.2 If test wafers are specified to be edge contoured, the profile shall conform to the requirements in Section 5.2 of SEMI M1 and to the dimension C_y in the associated polished silicon wafer standard applicable to the same nominal diameter and thickness. If edge profiling is not specified explicitly, there is no specification for the geometrical dimensions of any profiles that may exist on the wafers.

6.3 The material shall conform to the crystallographic orientation details as listed in the tables.

7 Materials and Manufacture

7.1 The material shall consist of wafers from crystals grown by the process specified in the purchase order or contract.

8 Electrical Requirements

8.1 Class A test wafers and process test wafers (only) shall conform to the details specified in the purchase order or contract, as follows:

8.1.1 Conductivity type

8.1.2 Resistivity

9 Sampling

9.1 Unless otherwise specified, ASTM Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) and lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL and LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

10 Test Methods

NOTE 1: Silicon wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement methods.

NOTE 2: The crystal growth method (for example, Czochralski or Float Zone) and dopant (for example, boron, phosphorous or antimony) used are difficult to ascertain in finished wafers. Verification test procedures for certification of these characteristics shall be agreed upon between the supplier and the purchaser.

10.1 Use test methods for the specified quantities as listed in Table 1 of SEMI M18.

11 Surface Defect Criteria

11.1 *Minimal Conditions or Dimensions* — The minimal conditions or dimensions for defects stated below shall be used for determining wafer acceptability. Anomalies smaller than these limits shall not be considered defects.

11.2 *area contamination* — any foreign matter on the surface in localized areas which is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains, water spots, etc.

11.3 *crack* — any anomaly conforming to the definition and greater than 0.25 mm (0.010 inch) in total length.

11.4 *crow's foot* — any anomaly conforming to the definition and greater than 0.25 mm (0.010 inch) in total length.

11.5 *dimple* — any smooth surface depression greater than 3 mm in diameter.

11.6 *edge chip and indent* — any edge anomaly including saw exit marks conforming to the definition and greater than 0.25 mm (0.010 inch) in radial depth and peripheral length.

11.7 *hand scribe mark* — any mark such as that caused by a diamond scribe that is visible under diffuse illumination.

11.8 *haze* — haze is indicated when the image of a narrow beam tungsten lamp filament is detectable on the polished wafer surface. (Under some conditions contamination may appear as haze.)

11.9 *orange peel* — any roughened surface conforming to the definition that is observable under diffuse illumination.

11.10 *particulate contamination* — distinct particles resting on the surface, which is revealed under, collimated light as bright points.

11.11 *pit* — any individually distinguishable non-removable surface anomaly conforming to the definition and visible when viewed under high intensity illumination.

11.12 *saw marks* — any surface irregularities conforming to the definition that is observable under diffuse illumination.

11.13 *scratch* — any anomaly conforming to the definition and having a length-to-width ratio greater than 5:1.

11.14 *slip* — any pattern of short ridges aligned along <110> directions and visible under diffuse illumination.

11.15 *striations* — any helical features conforming to the definition and visible under diffuse illumination.

12 Certification

12.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

12.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 9. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

13 Packing and Marking

13.1 Special packing requirements shall be subject to agreement between the supplier and the purchaser. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices, to provide ample protection against damage during shipment.

13.2 The wafers supplied under this specification shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing.

Table 3 Specifications for Small Diameter Silicon Test Wafers

Item		*Specification*		
		CLASSIFICATION		
		A	**B**	**C**
1.0	**General Characteristics**			
1.1	Growth Method	User specified		
1.2	Crystal Orientation	User specified		
1.2.1	Crystal Orientation	User specified		
1.3	Conductivity Type	User specified		
1.4	Dopant	User specified		
1.5	Nominal Edge Exclusion Distance for FQA	Not specified		
2.0	**Electrical Characteristics**			
2.1	Resistivity	User specified		
2.2	Radial Resistivity Variation (RRG)	Optional		
2.3	Resistivity Striations	Unspecified		
2.4	Minority Carrier Lifetime	Unspecified		
3.0	**Chemical Characteristics**			
3.1	Oxygen Concentration	Unspecified		
3.2	Radial Oxygen Variation	Unspecified		
3.3	Carbon Concentration	Unspecified		
4.0	**Structural Characteristics**			
4.1	Dislocation Etch Pit Density	None	Optional	Unspecified
4.2	Slip	None	Optional	Unspecified
4.3	Lineage	None	Optional	Unspecified
4.4	Twins	None	Optional	Unspecified
4.5	Swirl	None	Optional	Unspecified
4.6	Shallow Pits	None	Optional	Unspecified
4.7	OISF	Optional	Optional	Unspecified
4.8	Oxide Precipitates	Unspecified		

Item		*Specification*		
		CLASSIFICATION		
		A	**B**	**C**
5.0	**Wafer Preparation Characteristics**			
5.1	Wafer ID Marking	Optional	Optional	Unspecified
5.2	Front Surface Thin Films	Optional	Optional	Unspecified
5.3	Denuded Zone	Optional	Optional	Unspecified
5.4	Extrinsic Gettering	Optional	Optional	Unspecified
5.5	Backseal	Optional	Optional	Unspecified
5.6	Annealing	Optional	Optional	Unspecified
6.0	**Mechanical Characteristics**			
6.1	Diameter			
	2.00 inch ±	0.015 in.	0.020 in.	0.030 in.
	3.00 inch ±	0.020 in.	0.025 in.	0.050 in.
	100 mm ±	0.20 mm	0.50 mm	1.00 mm
	125 mm ±	0.20 mm	0.50 mm	1.00 mm
6.2	Primary Flat Dimension			
	2.00 inch (flat length)	0.500–0.750 in.	0.500–0.750 in.	0.500–0.750 in.
	3.00 inch (flat length)	0.750–1.00 in.	0.750–1.00 in.	0.750–1.00 in.
	100 mm (flat length)	30–35 mm	28–37 mm	28–37 mm
	125 mm (flat length)	40–45 mm	38–47 mm	38–47 mm
6.3	Primary Flat Orientation		{110} ± 2°	
6.4	Secondary Flat Length		Unspecified	
6.5	Secondary Flat Location		Unspecified	
6.6	Edge Profile	5.2 of SEMI M1		Optional
6.7	Thickness			
	2 inch	0.0095–0.0125 in.	0.0090–0.013 in.	0.0080–0.0130 in.
	3 inch	0.0135–0.0165 in.	0.013–0.017 in.	0.012–0.018 in.
	100 mm (SEMI M1.5)	505–545 µm	500–550 µm	475–575 µm
	100 mm (SEMI M1.6)	605–645 µm	600–650 µm	575–675 µm
	125 mm	605–645 µm	600–650 µm	575–675 µm
6.8	Thickness Variation (TTV)		Unspecified	
6.9	Surface Orientation	User specified	Optional	Unspecified
6.10	Bow		Unspecified	
6.11	Warp		Unspecified	
6.12	Sori		Unspecified	
6.13	Flatness/Global		Unspecified	
6.14	Flatness/Site		Unspecified	
7.0	**Front Surface Chemistry**			
7.1	Surface Metal Contamination			
	Sodium	Optional	Unspecified	Unspecified
	Aluminum	Optional	Unspecified	Unspecified
	Potassium	Optional	Unspecified	Unspecified
	Chromium	Optional	Unspecified	Unspecified
	Iron	Optional	Unspecified	Unspecified
	Nickel	Optional	Unspecified	Unspecified
	Copper	Optional	Unspecified	Unspecified

Item		*Specification*		
		CLASSIFICATION		
		A	**B**	**C**
	Zinc	Optional	Unspecified	Unspecified
7.2	Surface Organics	Optional	Unspecified	Unspecified
8.0	**Front Surface Visual Characteristics**			
8.1	Scratches (# of)	Unspecified		
	(cumulative length)	R/5	R/2	Unspecified
8.2	Pits	None		Unspecified
8.3	Haze	None		Unspecified
8.4	Localized Light Scatterers	(Density per square meter with 4 mm edge exclusion)		
	2 inch	≤1900	≤5000	Unspecified
	3 inch	≤1900	≤5000	Unspecified
	100 mm	≤1900	≤5000	Unspecified
	125 mm	≤1900	≤5000	Unspecified
8.5	Contamination/area	None		Unspecified
8.6	Edge Chips	None		Unspecified
8.7	Edge Cracks	None		Unspecified
8.8	Cracks, Crow's feet	None		Unspecified
8.9	Craters	None		Unspecified
8.10	Dimples	None		Unspecified
8.11	Grooves	None		Unspecified
8.12	Mounds	None		Unspecified
8.13	Orange Peel	None		Unspecified
8.14	Saw Marks	None		Unspecified
8.15	Dopant Striation Rings	None		Unspecified
8.16	Stains	None		Unspecified
9.0	**Back Surface Characteristics**			
9.1	Edge Chips	None		Unspecified
9.2	Cracks, Crow's feet	None		Unspecified
9.3	Contamination/Area	None		Unspecified
9.4	Saw Marks	None		Unspecified
9.5	Stains	None		Unspecified
9.6	Roughness	Unspecified		
9.7	Brightness (gloss)	Unspecified		
TBD (NOTE 1)	Back Surface Finish	Unspecified		

NOTE 1: A revision to SEMI M18 to provide this item number is being developed. When this revision is completed, this specification will be revised to include the assigned item number from SEMI M18.

Table 4 Specifications for Large Diameter Silicon Test Wafers

	Item	*Specification*	
		CLASSIFICATION	
		MECHANICAL	**PROCESS**
1.0	**General Characteristics**		
1.1	Growth Method	CZ or MCZ	CZ or MCZ
1.2	Crystal Orientation	Unspecified	User specified
1.3	Conductivity Type	Unspecified	[ ]P or [ ]N
1.4	Dopant	Unspecified	[ ]Boron [ ]Phosphorus
1.5	Nominal Edge Exclusion Distance for FQA	3 mm	
2.0	**Electrical Characteristics**		
2.1	Resistivity	Unspecified	≥1 Ω·cm
2.2	Radial Resistivity Variation (RRG)	Unspecified	
2.3	Resistivity Striations	Unspecified	
2.4	Minority Carrier Lifetime	Unspecified	
3.0	**Chemical Characteristics**		
3.1	Oxygen Concentration	Unspecified	
3.2	Radial Oxygen Variation	Unspecified	
3.3	Carbon Concentration	Unspecified	
4.0	**Structural Characteristics**		
4.1	Dislocation Etch Pit Density	Unspecified	$\leq 500/cm^2$
4.2	Slip	Unspecified	None
4.3	Lineage	Unspecified	None
4.4	Twins	Unspecified	None
4.5	Swirl	Unspecified	
4.6	Shallow Pits	Unspecified	
4.7	OISF	Unspecified	
4.8	Oxide Precipitates	Unspecified	
5.0	**Wafer Preparation Characteristics**		
5.1	Wafer ID Marking	Optional	
5.2	Front Surface Thin Films	Unspecified	
5.3	Denuded Zone	Unspecified	
5.4	Extrinsic Gettering	Unspecified	
5.5	Backseal	Unspecified	
5.6	Annealing	Unspecified	
6.0	**Mechanical Characteristics**		
6.1	Diameter		
	150 mm ±	SEMI M1.8 or SEMI M1.13	
	200 mm ±	SEMI M1.9 or SEMI M1.10	
	300 mm ±	SEMI M1.15	
6.2	Primary Flat Dimension (or Notch Depth)		
	150 mm (flat length)	SEMI M1.8 or SEMI M1.13	

	Item	*Specification*	
		CLASSIFICATION	
		MECHANICAL	**PROCESS**
	200 mm (notch depth)	SEMI M1.9	
	200 mm (flat diameter)	SEMI M1.10	
	300 mm (notch depth)	SEMI M1.15	
6.3	Primary Flat/Notch Orientation	SEMI M1	
6.4	Secondary Flat Length	SEMI M1.8 or SEMI M1.13 (150 mm) or SEMI M1.10 (200 mm)	
	Secondary Flat Length (300 mm)	None	
6.5	Secondary Flat Location	SEMI M1	
6.6	Edge Profile	5.2 of SEMI M1	
6.7	Thickness		
	150 mm (SEMI M1)	SEMI M1.8 or SEMI M 1.13	
	200 mm (notched or flatted)	SEMI M1.9 or SEMI M1.10	
	300 mm	SEMI M1.15	
6.8	Thickness Variation (TTV)	Unspecified	
6.9	Surface Orientation (for all diameters up to 200 mm)	Unspecified	
	Surface Orientation (for 300 mm)	Unspecified	
6.10	Bow	Unspecified	
6.11	Warp	Unspecified	
6.12	Sori	Unspecified	
6.13	Flatness/Global	Unspecified	
6.14	Flatness/Site	Unspecified	
7.0	**Front Surface Chemistry**		
7.1	Surface Metal Concentration	Unspecified	See Note 1.
8.0	**Front Surface Visual Characteristics**		
8.1A	Scratches (macro) – total length	Unspecified	None
8.1B	Scratches (micro) – total length	Unspecified	≤ 0.10 × Diameter
8.2	Pits	Unspecified	None
8.3	Haze	Unspecified	None
8.4	Localized Light Scatterers	Unspecified	See Note 2.
	150 mm	Unspecified	≤ 0.20/cm^2 @ ≥ 0.20 µm
	200 mm	Unspecified	≤ 0.20/cm^2 @ ≥ 0.20 µm
	300 mm	Unspecified	≤ 0.20/cm^2 @ ≥ 0.20 µm
8.5	Contamination/area	Unspecified	None
8.6	Edge Chips	Unspecified	None
8.7	Edge Cracks	Unspecified	None
8.8	Cracks, Crow's feet	Unspecified	None
8.9	Craters	Unspecified	None
8.10	Dimples	Unspecified	None
8.11	Grooves	Unspecified	None
8.12	Mounds	Unspecified	None
8.13	Orange Peel	Unspecified	None
8.14	Saw Marks	Unspecified	None

	Item	*Specification*	
		CLASSIFICATION	
		MECHANICAL	**PROCESS**
9.0	**Back Surface Characteristics**		
9.1	Edge Chips	Unspecified	None
9.6	Roughness	Unspecified	
9.7	Brightness (gloss)		
	150 mm/200 mm	Unspecified	
	300 mm	≥ 80%	
9.8	Localized Light Scatterers (LLS's)	Unspecified	
9.9	Scratches (macro)	Unspecified	< 0.25 × Diameter
9.10	Scratches (micro)	Unspecified	
10.0	**Other Characteristics**		
TBD (See Note 3.)	150 mm/200 mm	Unspecified	
TBD (See Note 3.)	300 mm	Unspecified	Polished

NOTE 1: Test wafers are cleaned according to a defined prime wafer supplier process, with a stated capability for surface metals. Test wafer characteristics are defined to be the "unsorted" process capability for these parameters and accordingly, will not be sorted. Products needed special surface metal requirements should be described by SEMI M24 criteria.

NOTE 2: Test wafers are cleaned according to a defined prime wafer supplier process, with a stated capability for removable LLS. Test wafer characteristics are defined to be the "unsorted" process capability for these parameters and accordingly, will not be sorted. Products needing special LLS requirements should be described by SEMI M24 criteria.

NOTE 3: A revision to SEMI M18 to provide this item number is being developed. When this revision is completed, this specification will be revised to include the assigned item number from SEMI M18.

Table 5 Guide for Specifying 200 mm & 300 mm Polished Silicon Process Test Wafers for Advanced Applications

Item		*Process Test Wafers 0.18 µm or 0.13 µm Design Rule*
1.0	**GENERAL CHARACTERISTICS**	
1.1	Growth Method	CZ or MCZ
1.2	Crystal Orientation	<100>
1.3	Conductivity Type	*P*
1.4	Dopant	Boron
1.5	Nominal Edge Exclusion	3 mm
2.0	**ELECTRICAL CHARACTERISTICS**	
2.1	Resistivity	0.5– 50.0 Ω·cm
2.2	Radial Resistivity Variation	Unspecified
2.3	Resistivity Striations	Unspecified
2.4	Minority Carrier Recombination Lifetime	Unspecified
3.0	**CHEMICAL CHARACTERISTICS**	
3.1.1	Oxygen Concentration	Unspecified
3.2	Radial Oxygen Variation	Unspecified
3.3	Carbon Concentration	Unspecified
4.0	**STRUCTURAL CHARACTERISTICS**	
4.1	Dislocation Etch Pit Density	Unspecified
4.2	Slip	None
4.3	Lineage	None
4.4	Twins	None
4.5	Swirl	Unspecified
4.6	Shallow pits	Unspecified
4.7	Oxidation-Induced Stacking Faults (OSF)	Unspecified
4.8	Oxide Precipitates	Unspecified
5.0	**WAFER PREPARATION CHARACTERISTICS**	
5.1	Wafer ID Marking 200 mm 300 mm	 User Specified SEMI M1.15
5.2	Front Surface Thin Films	None
5.3	Denuded Zone	None
5.4	Extrinsic Gettering	None
5.5	Backseal	None
6.0	**MECHANICAL CHARACTERISTICS**	
6.1	Diameter	SEMI M1
6.2	Primary Fiducial Location	SEMI M1
6.3	Primary Fiducial Dimension	SEMI M1
6.6	Edge Profile	SEMI M1

Item		*Process Test Wafers* *0.18 µm or 0.13 µm Design Rule*
6.7	Thickness Target Tolerance	 SEMI M1 ± 25 µm
6.8	Thickness Variation (TTV)	Unspecified
6.9	Wafer Surface Orientation	{100} ± 1 deg
6.11	Warp	SEMI M1
6.12	Sori	Unspecified
6.14	Flatness/Site	Unspecified
7.0	**FRONT SURFACE CHEMISTRY**	
7.1	Surface Metal Concentration:	See Note 1.
8.0	**FRONT SURFACE CRITERIA**	
8.1 A	Scratches (macro) – total length	None
8.1 B	Scratches (micro) – total length	≤ 0.10 × Diameter
8.2	Pits	None
8.3	Haze	None by Bright Light Inspection
8.4	Localized Light Scatterers	See Note 2.
8.5	Contamination/Area	None
8.6	Edge Chips	None
8.7	Edge Cracks	None
8.8	Crack, crows feet	None
8.9	Craters	None
8.10	Dimples	None
8.11	Grooves	None
8.12	Mounds	None
8.13	Orange Peel	None
8.14	Saw Marks	None
9.0	**BACK SURFACE CRITERIA**	
9.1	Edge Chips	None
9.6	Roughness	Unspecified
9.7	Brightness (Gloss) 200 mm 300 mm	Unspecified SEMI M1.15
9.8	Scratches (macro) – total length	0.5 × diameter
9.9	Scratches (micro) – total length	Unspecified
9.10	Localized Light Scatters	Unspecified
10.0	**OTHER CHARACTERISTICS**	
TBD (See Note 3).	Edge Condition	Bright Etched or Polished

NOTE 1: Test wafers are cleaned according to a defined prime wafer supplier process, with a stated capability for removable LLS. Test wafer characteristics are defined to be the "unsorted" process capability for these parameters and accordingly, will not be sorted. Products needing special LLS requirements should be described by SEMI M24 criteria.

NOTE 2: Test wafers are cleaned according to a defined prime wafer supplier process, with a stated capability for surface metals. Test wafer characteristics are defined to be the "unsorted" process capability for these parameters and accordingly, will not be sorted. Products needed special surface metal requirements should be described by SEMI M24 criteria.

NOTE 3: The A revision to SEMI M18 to provide this designation item number is in process being developed. When the this revision to SEMI M18 is completed, this document specification will be revised to include the assigned item number from SEMI M18 designation.

NOTICE: SEMI makes no warranties or representations as to the suitability of the standard set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI M9-0999
SPECIFICATIONS FOR POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE SLICES

NOTE: This specification was modified in September 1999 to correct an editorial error present in Figure 4A. A Publication Improvement Proposal (PIP) form was submitted in August 1999.

1 Preface

1.1 These specifications cover two groups of substrate requirements for monocrystalline high-purity gallium arsenide wafers used in semiconductor and electronic device manufacture. Dimensional and crystallographic orientation characteristics and limits on surface defects are the only standardized properties set forth below.

1.2 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed, together with test methods suitable for determining their magnitude where such procedures are documented.

1.3 These specifications are directed specifically to gallium arsenide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

1.4 The material is Single Crystal Gallium Arsenide (GaAs) having a cubic zinc blende structure and having the following properties. The following properties are for use as guidelines:

Density	5.316 gm/cm^3
Melting Point	1238°C
Dielectric Constant	13.1
Lattice Parameter	5.654 Å
Energy Gap	1.42 eV

1.5 For reference purposes, SI (System International, commonly called metric) units shall be used.

2 Applicable Documents

2.1 *ASTM Standards*[1]

E 122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

F 26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

F 76 — Test Methods for Measuring Hall Mobility and Hall Coefficient in Extrinsic Semiconductor Single Crystals

F 154 — Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

F 523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

F 533 — Test Method for Thickness and Thickness Variation of Silicon Slices

F 534 — Test Method for Bow of Silicon Slices

F 613 — Test Method for Measuring Diameter of Silicon Slices and Wafers

F 657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Slices and Wafers by a Non-Contact Scanning Method

F 671 — Test Method for Measuring Fiducial Flat Length and Deviation

F 928 — Test Method for Edge Contour of Silicon Wafers

2.2 *Other Standard*[2]

ANSI/ASQC Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

3 Definitions

3.1 *Bow* — of a semiconductor slice or wafer, a measure of concave or convex deformation of the median surface of a slice or wafer, independent of any thickness variation which may be present. Bow is a bulk property of the test specimen, not a property of an exposed surface. Generally, bow is determined with a test specimen in a free, unclamped condition. Units of bow are generally micrometers or inches.

3.2 *Dopant* — a chemical element, usually from the second, fourth, or sixth columns of the periodic table for the case of III-V compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959 (All cited standards except for E 122 may be found in Volume 10.05 of the Annual Book of ASTM Standards; E 122 may be found in Volume 14.02.)

2 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

3.3 *Lot* — for the purpose of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

3.4 *Flat Diameter* — the linear dimension across the surface of a semiconductor wafer from the center of the flat through the wafer center to the circumference of the wafer on the opposite edge along the diameter perpendicular to the flat. (See Figure 6.)

NOTE 4 — The flat diameter may be associated with the primary orientation flat, with a secondary flat, if present, or with any other flat, if present. In such cases, the terms may be modified as primary orientation flat diameter, secondary flat diameter, etc.

3.5 *Orthogonal Misorientation* — in {100} wafers cut intentionally "off-orientation," the angle between the projection of the vector normal to the slice surface onto the {100} plane and the projection on that plane of the nearest direction. (See Figure 5.)

3.6 *Total Thickness Variation* — (TTV) the difference between the maximum and minimum thickness values of a slice or wafer encountered during a scan pattern or a series of point requirements. TTV is generally expressed in micrometers or mils (thousandths of an inch).

3.7 *Warp* — of a semiconductor slice or wafer, the difference between the maximum and minimum distances of the median surface of the slice or wafer from a reference plane, encountered during a scan pattern. Warp is a bulk property of the test specimen, not a property of an exposed surface. Warp is generally expressed in micrometers or mils (thousandths of an inch).

3.8 *Edge Contouring* — on slices whose edges have been shaped by mechanical and/or chemical means, a description of the profile of the boundary of the slice joining the front and back sides.

4 Ordering Information

4.1 Purchase orders for gallium arsenide wafers furnished to this specification shall include the following items:

4.1.1 Nominal diameter (see applicable SEMI Standard for polished GaAs wafers),

4.1.2 Thickness (see applicable SEMI Standard for polished GaAs wafers),

4.1.3 Total Thickness Variation (see applicable SEMI Standard for polished GaAs wafers),

4.1.4 Surface orientation (see applicable SEMI Standard for polished GaAs wafers). There are two options of flat location for 2" and 3" diameter polished mono-crystalline GaAs wafers for integrated circuit and optoelectronic applications. They are V-Groove (as illustrated in Figures 1 and 3) and Dove-Tail (as illustrated in Figures 2 and 4). These designations describe the shape of groove that can be etched perpendicular to the primary flat.

The following are the options of wafer surface orientation:

A. (100) ± 0.5° as shown in Figures 1 and 2

B. For V-Groove option:

(100) off 2° toward the (110) plane which is located between the primary and secondary flats as shown in Figure 3. Figure 5 illustrates orthogonal misorientation.

For Dove-Tail option:

(100) off 2° toward any of the nearest (110) planes as shown in Figure 4. Figure 5 illustrates orthogonal misorientation.

4.1.5 Lot Acceptance Procedures (see Section 8),

4.1.6 Certification (see Section 11),

4.1.7 Packing and Marking (see Section 12).

4.2 *Optional Criteria* — The following items may be specified optionally in addition to those listed above:

4.2.1 Crystal Growth Method,

4.2.2 Etch Pit Density (EPD) of Crystal,

4.2.3 Crystal Growth Perfection,

4.2.4 Impurity Type,

4.2.5 Surface Condition of Wafer,

4.2.6 Edge Contour,

4.2.7 Mobility,

4.2.8 Resistivity,

4.2.9 Carrier Concentration,

4.2.10 Thermal Conversion Characteristics.

5 Dimensions and Permissible Variations

5.1 The material shall conform to the dimensions and dimensional tolerances as specified in the applicable polished gallium arsenide slice standard.

5.2 If edge contoured wafers are specified on the purchase order, the profile shall conform to the following requirements at all points on the wafer periphery.

5.2.1 When the wafer is aligned with the SEMI Wafer Edge Profile Template (see Figure 6) so that the x-axis of the template is coincident with the wafer surface and the y-axis of the template is tangent with the outermost radial portion of the contour, the wafer edge profile must be contained within the clear region of the template. (See Figure 7 for example of acceptable and unacceptable contours.)

5.2.2 No sharp points or protrusions are permitted anywhere on the wafer edge contour.

5.2.3 Cosmetic attributes of the edge contour are not covered by this specification. They shall be agreed upon between supplier and purchaser.

6 Materials and Manufacture

6.1 The material shall consist of wafers from ingots grown to the material definition specified in the purchase order or contract.

7 Physical Requirements

7.1 The material shall conform to the crystallographic orientation details as specified in the applicable polished gallium arsenide slice standard.

7.2 The material shall conform to the details specified in the purchase order or contract as follows:

7.2.1 Conduction Type,

7.2.2 Dopant,

7.2.3 Carrier Concentration,

7.2.4 Resistivity,

7.2.5 Thermal Conversion Characteristics,

7.2.6 Etch Pit Density,

7.2.7 Mobility,

7.2.8 Surface Characteristics,

7.2.9 Growth Methods.

8 Sampling

8.1 Unless otherwise specified, Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

9 Test Methods

9.1 *Diameter* — Determine by ASTM Test Method F 613.

9.2 *Thickness, Center Point* — Determine by ASTM Test Method F 533.

NOTE 2 — GaAs wafers are extremely fragile. While the mechanical dimensions of a slice can be measured by use of tools such as a micrometer calipers and other conventional techniques, the slice may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement methods.

9.3 *Flat Length* — Determine by ASTM Test Method F 671.

9.4 *Flat Orientation* — Determine by etching method identified in the appropriate polished GaAs wafer standard.

9.5 *Bow and Warp* — Determine bow in accordance with ASTM Test Method F 534 and warp in accordance with ASTM Test Method F 657.

9.6 *Total Thickness Variation* — Determine by ASTM Test Method F 533 or F 657.

9.7 *Surface Orientation* — Determined by ASTM Test Methods F 26.

9.8 *Orthogonal Misorientation* — Determined by a method agreed upon between the supplier and purchaser.

9.9 *Surface Defects and Contamination* — Determined by a method agreed upon between the supplier and purchaser.

9.10 *Mobility* — Determined by ASTM Test Methods F 76.

9.11 *Crystal Perfection* — Determined by a method agreed upon between the supplier and purchaser.

10 Standard Defect Limits

10.1 Determined by agreement between supplier and purchaser as to limits.

11 Certification

11.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification together, with a report of the test results, shall be furnished at the time of shipment.

11.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material

shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 9. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

12 Packing and Marking

12.1 Special packing and marking requirements shall be subject to agreement between the supplier and the purchaser. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination in accordance with the best industry practices to provide ample protection against damage during shipment.

12.2 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductive dopant, orientation, resistivity range, and lot number.

12.3 The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to slice manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one month or as negotiated between vendor and user after that particular lot has been accepted by the purchaser.

Table 1. Equivalent Orientations — V-Groove Option

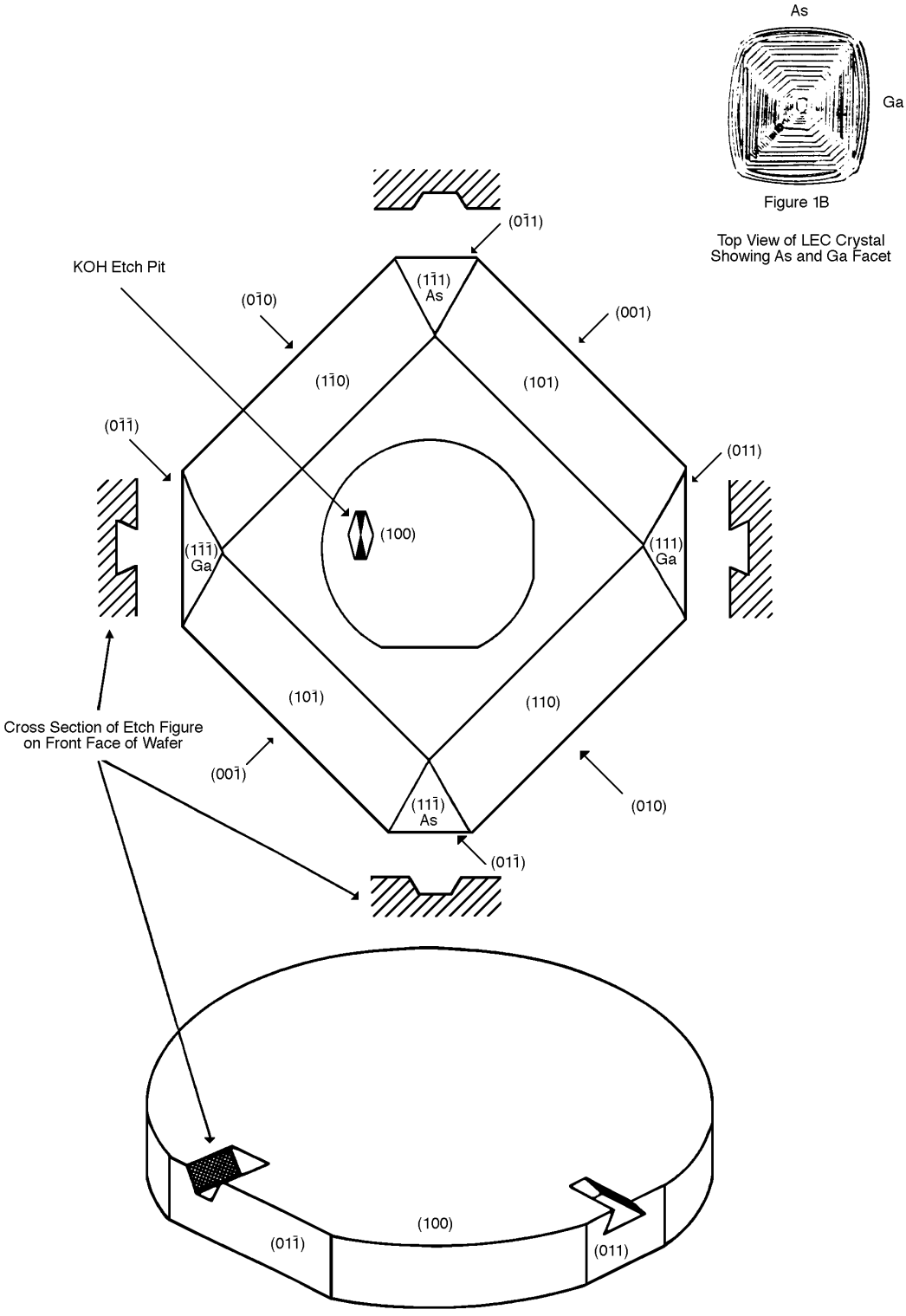
Surface orientation:	(100)	(100)	$(\bar{1}00)$	$(\bar{1}00)$
Primary flat location:	$(01\bar{1})$	$(0\bar{1}1)$	$(0\bar{1}\bar{1})$	(011)
Secondary flat location:	(011)	$(0\bar{1}\bar{1})$	$(0\bar{1}1)$	$(01\bar{1})$
For Surface orientation B, the off-orientation tilt direction is toward:	(110)	$(1\bar{1}0)$	$(\bar{1}\bar{1}0)$	$(\bar{1}10)$

Table 2. Equivalent Orientations — Dove-Tail Option

Surface orientation:	(100)	(100)	$(\bar{1}00)$	$(\bar{1}00)$
Primary flat location:	$(0\bar{1}\bar{1})$	(011)	$(01\bar{1})$	$(0\bar{1}1)$
Secondary flat location:	$(0\bar{1}1)$	$(01\bar{1})$	(011)	$(0\bar{1}\bar{1})$
For Surface orientation B, the off-orientation tilt direction is toward:	$(1\bar{1}0)$	(110)	$(\bar{1}10)$	$(\bar{1}\bar{1}0)$

The symmetry of GaAs crystal structure allows other Miller indices to be used for identifying surface and flat orientations. This table lists various possibilities which meet the requirements for the above two options.

NOTE: For V-Groove Option, the relative directions in a single column must be maintained. For Dove-Tail Option, any of the 110 tilt directions are considered equivalent.



Figures 1A and 1B
Both Diagrams Show a GaAs Wafer with Surface Orientation A and Flat Option V-Groove

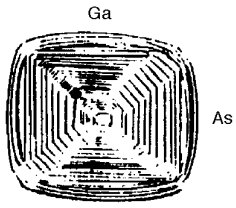
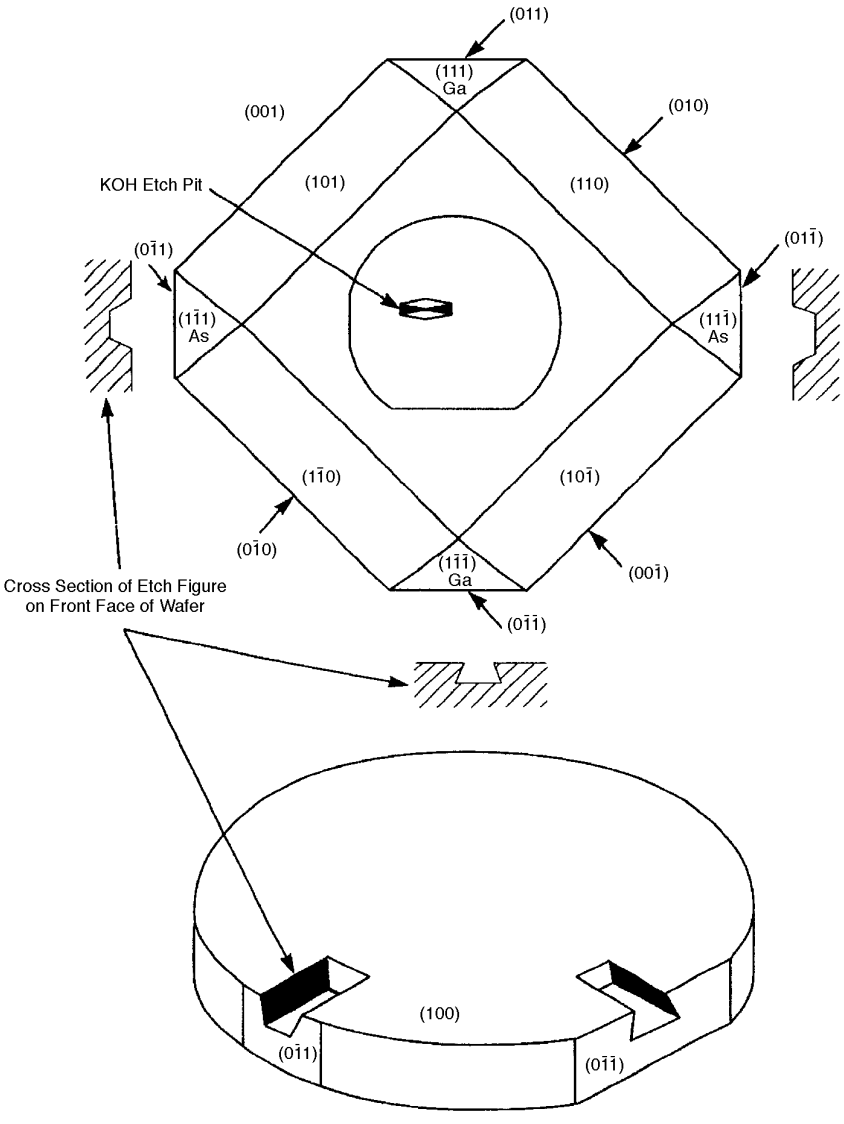
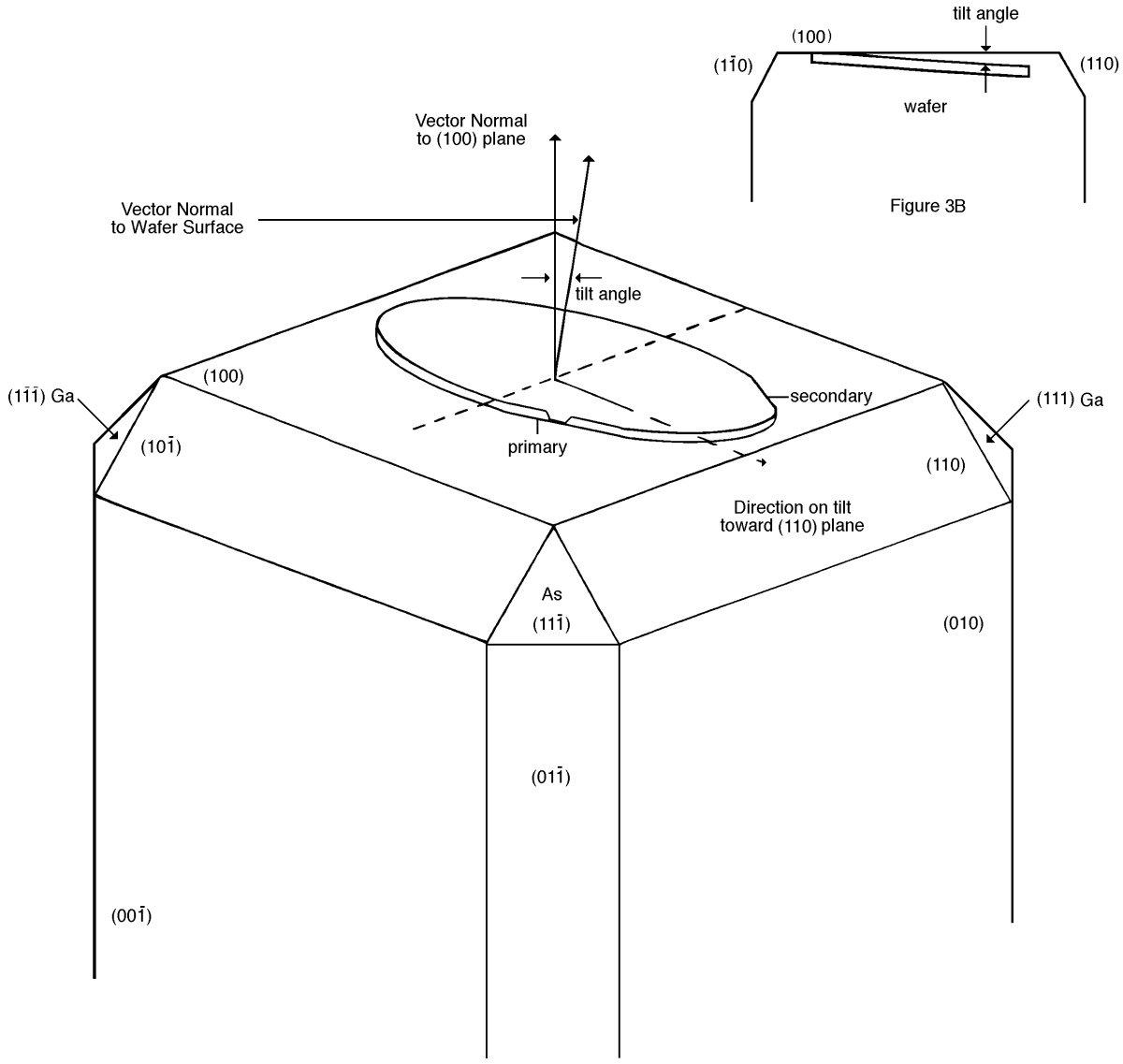


Figure 2B

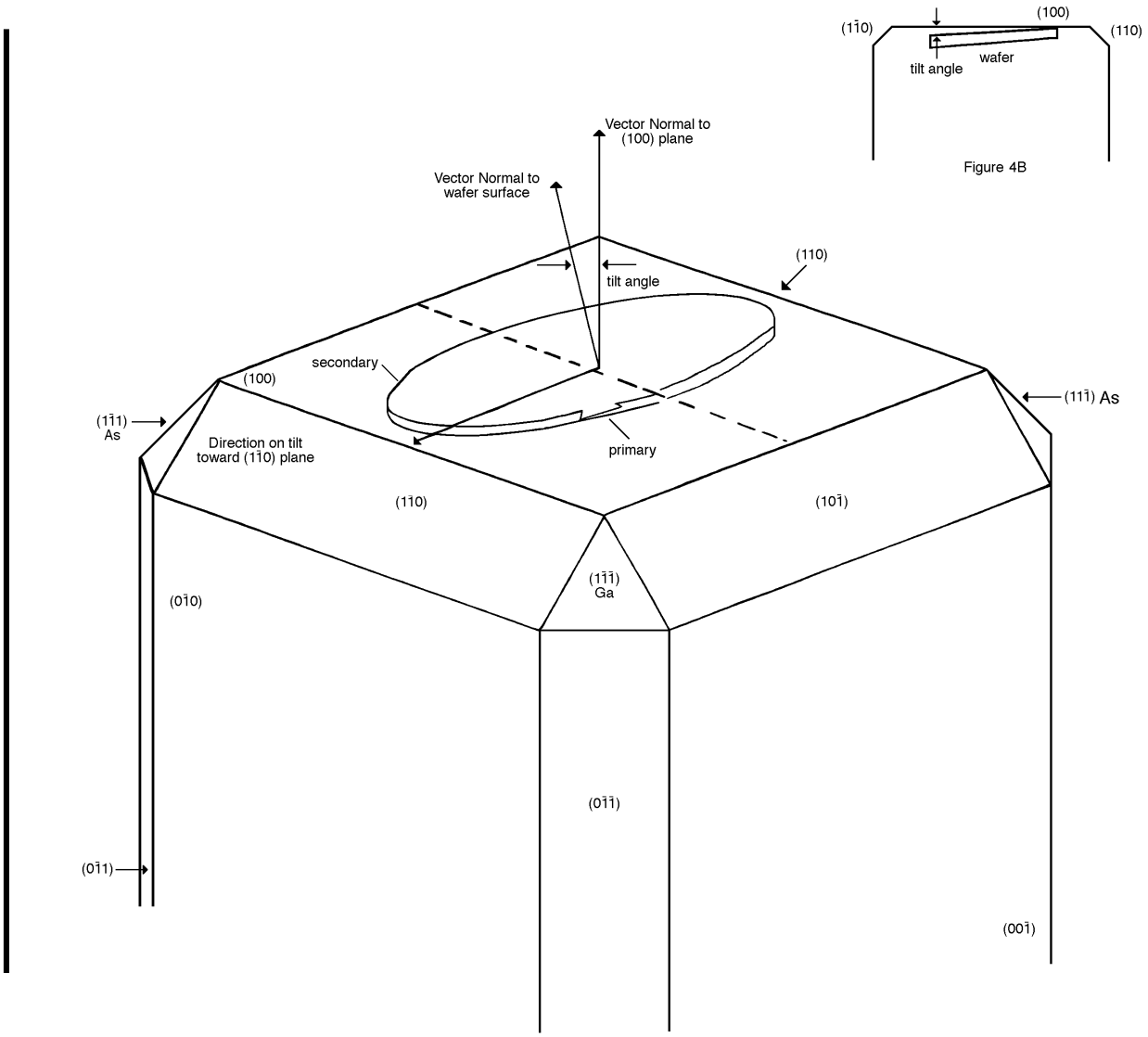
Top View of LEC Crystal
Showing Ga and As Facets



Figures 2A and 2B
Both Diagrams Show a GaAs Wafer with Surface Orientation A and Flat Option Dove-Tail



Figures 3A and 3B
Both Diagrams Show a GaAs Wafer with Surface Orientation B and Flat Option V-Groove



Figures 4A and 4B
Both Diagrams Show a GaAs Wafer with Surface Orientation B and Flat Option Dove-Tail

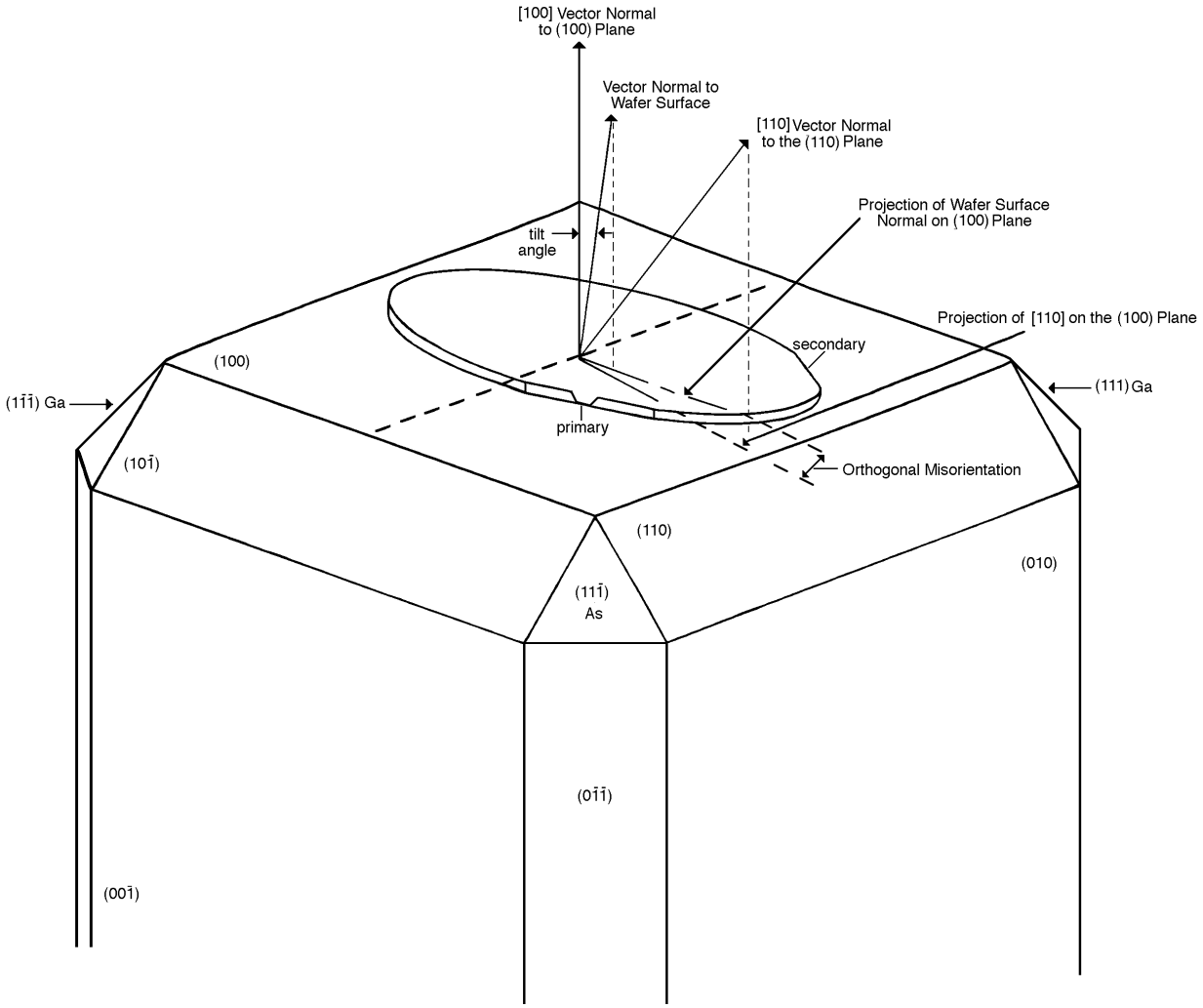


Figure 5
A GaAs Wafer with the Same Orientation as Figure 3, but with a Few Degrees of Orthogonal Misorientation

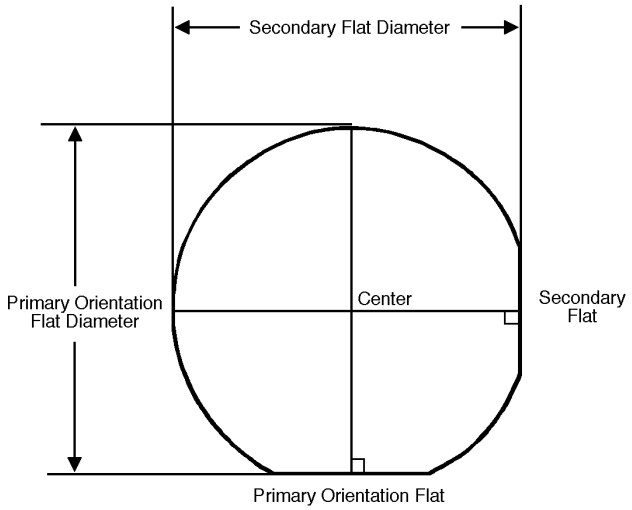


Figure 6
Flat Diameter on Wafer with Primary Orientation Flat and Secondary Flat

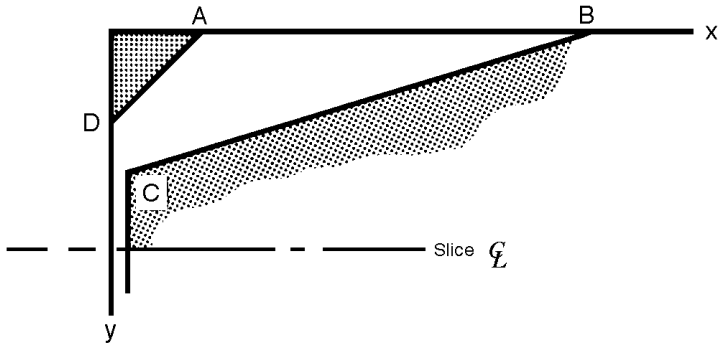


Figure 7
SEMI Wafer Edge Profile Template

Point	*x*		*y*	
	in.	*μm*	*in.*	*μm*
A	0.0030	76	0.00	0
B	0.0200	508	0.00	0
C	0.0020	51	(See Note 2)	(See Note 2)
D	0.00	0	0.0030	76

NOTE 1: For referee purposes, U.S. customary units are to be used for 2 and 3 in. diameter wafers and SI units otherwise.

NOTE 2: The y-coordinate of point C is 1/3 the nominal wafer thickness.

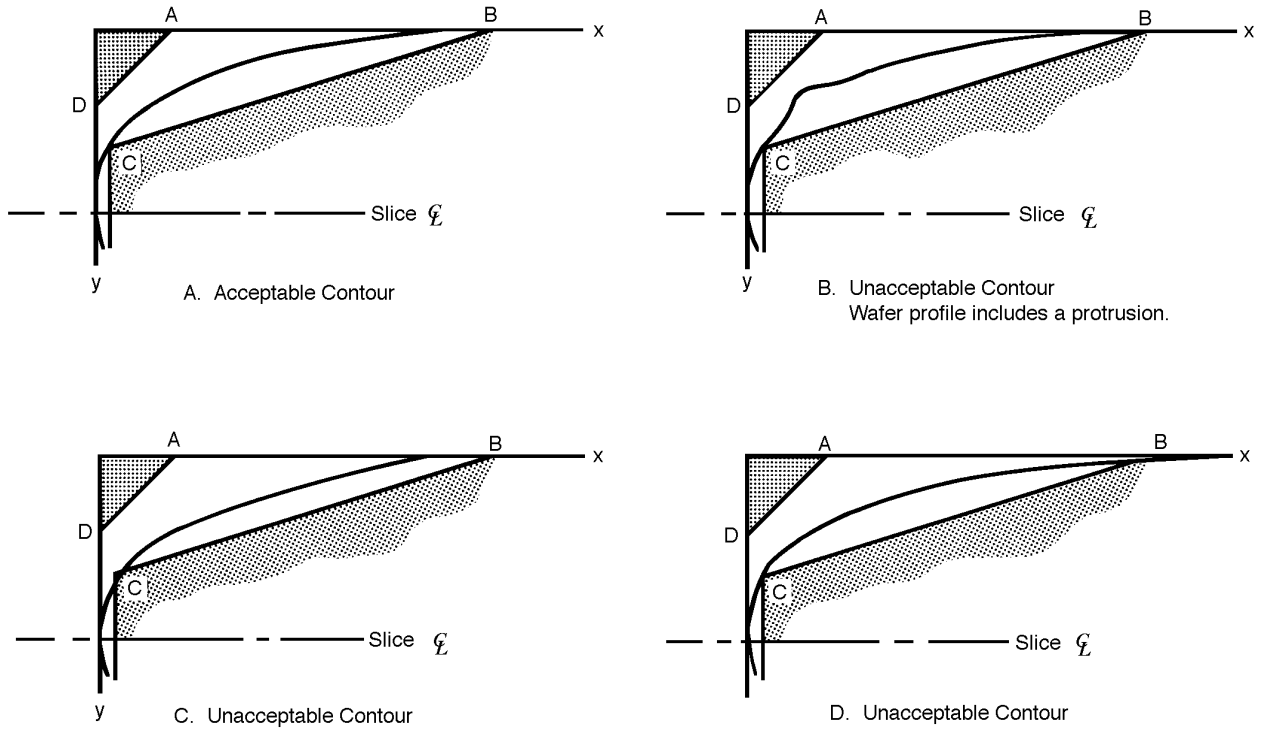


Figure 8
Examples of Acceptable and Unacceptable Wafer Edge Profiles

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SEMI M9.1-96
STANDARD FOR ROUND 50.8 mm POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE WAFERS FOR ELECTRONIC DEVICE APPLICATIONS

NOTE: This entire document was rewritten in 1995.

The complete specification for this product includes all general requirements of SEMI M9.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*
DIAMETER[A]	50.8	± 0.5	mm
THICKNESS, CENTER POINT	450	± 25	µm
PRIMARY FLAT LENGTH	16	± 2	mm
SECONDARY FLAT LENGTH	8	± 2	mm

[A] The diameter standard means that the dimension is centered to this value.

Table 2 Orientation and Flat Location Requirements

Property	*Requirement*
PRIMARY FLAT ORIENTATION	$(0\bar{1}1)$ ± 0.5° [A], under an Arsenic facet. The primary flat shall be perpendicular to the "V" etch figure.[B]
SECONDARY FLAT ORIENTATION	90° ± 5° counterclockwise from the primary flat.
SURFACE ORIENTATION[C]	(100) ± 0.5°
A.	(See Figure 1 in SEMI M9.)
B.	(100) off 2° ± 0.5° toward the (110) plane which is between the primary and secondary flats (see Figure 3 in SEMI M9.)
ORTHOGONAL MISORIENTATION	± 5° (See Figure 5 in SEMI M9.)

[A] See Table 1 in SEMI M9.

[B] Using A-B, bromine-methanol, ammonium hydroxide: hydrogen peroxide etch. See Figures 1 and 3 in SEMI M9. Figure 1 also shows the orientation of the V-groove figures relative to KOH etch pits.

[C] The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted toward the (110) plane of the crystal.

NOTICE: These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI M9.2-96
STANDARD FOR ROUND 76.2 mm POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE WAFERS FOR ELECTRONIC DEVICE APPLICATIONS

NOTE: This entire document was revised in 1995.

The complete specification for this product includes all general requirements of SEMI M9.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*
DIAMETER[A]	76.2	± 0.5	mm
THICKNESS, CENTER POINT	625	± 25	µm
PRIMARY FLAT LENGTH	22	± 2	mm
SECONDARY FLAT LENGTH	11	± 2	mm

[A] The diameter standard means that the dimension is centered to this value.

Table 2 Orientation and Flat Location Requirements

Property	*Requirement*
PRIMARY FLAT ORIENTATION	($(01\bar{1})$) ± 0.5° [A], under an Arsenic facet. The primary flat shall be perpendicular to the "V" etch figure.[B]
SECONDARY FLAT ORIENTATION	90° ± 5° counterclockwise from the primary flat.
SURFACE ORIENTATION[C]	(100) ± 0.5°
A.	(See Figure 1 in SEMI M9.)
B.	(100) off 2° ± 0.5° toward the (110) plane which is between the primary and secondary flats (see Figure 3 in SEMI M9.)
ORTHOGONAL MISORIENTATION	± 5° (See Figure 5 in SEMI M9.)

[A] See Table 1 in SEMI M9.

[B] Using A-B, bromine-methanol, ammonium hydroxide: hydrogen peroxide etch. See Figures 1 and 3 in SEMI M9. Figure 1 also shows the orientation of the V-groove figures relative to KOH etch pits.

[C] The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted toward the (110) plane of the crystal.

SEMI M9.3-89
STANDARD FOR ROUND 2 inch DIAMETER POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE SLICES FOR OPTOELECTRIC APPLICATIONS

The complete specification for this product includes all general requirements of SEMI M9.

Table 1 Dimension and Tolerance Requirements

Property	*Min*	*Max*	*Units*[A]
DIAMETER	50.42	51.18	mm
	1.985	2.015	in.
THICKNESS, CENTER POINT	350	400	mm
	0.0138	0.0158	in.
PRIMARY FLAT LENGTH	14.23	17.52	mm
	0.560	0.690	in.
SECONDARY FLAT LENGTH	6.35	9.65	mm
	0.250	0.380	In.
BOW		20	µm
		0.0008	in.
A.		50	µm
		0.0019	in.
B.		30	µm
		0.0011	in.
C.		10	µm
		0.0039	in.
TOTAL THICKNESS VARIATION SCHEDULE			
A.		24	µm
		0.0009	in.
B.		12	µm
		0.0005	in.
C.		8	µm
		0.0003	in.
D.		4	µm
		0.0002	in.

[A] For referee purposes, metric (SI) units apply.

Table 2 Orientation and Flat-Location Requirements

Property	*Requirement*	
Option	V-Groove (See Figures 1 and 3.)	Dove-Tail (See Figures 2 and 4.)
PRIMARY FLAT ORIENTATION	(011) ± 0.5° [B], under an Arsenic facet. The primary flat shall be perpendicular to the "V" etch figure.[C]	(011) ± 0.5° [B], under a Gallium facet. The primary flat shall be perpendicular to the "Dove-tail" etch figure.[C]
SECONDARY FLAT LOCATION	90° ± 5° counterclockwise from the primary flat.	90° ± 5° clockwise from the primary flat.
SURFACE ORIENTATION[A]		
A.	(100) ± 0.5° (See Figure 1.)	(100) ± 0.5° (See Figure 2.)
B.	(100) off 2° ± 0.5° towards the (110) plane which is between the primary and secondary flats (See Figure 3).	(100) off 2° ± 0.5° towards any (110) plane (See Figure 4).
ORTHOGONAL MISORIENTATION	± 5° (See Figure 5.)	± 5° (See Figure 5.)

[A] The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted towards the (110) plane of the crystal.

[B] See Table 1.

[C] Using A-B, bromine-methanol, ammonium hydroxide: hydrogen peroxide etch. See Figures 1 through 4. Figures 1 and 2 also show the orientation of the V-groove and Dove-tail figures relative to KOH etch pits.

SEMI M9.4-89
STANDARD FOR ROUND 3 inch DIAMETER POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE SLICES FOR OPTOELECTRIC APPLICATIONS

The complete specification for this product includes all general requirements of SEMI M9.

Table 1 Dimension and Tolerance Requirements

Property	*Min*	*Max*	*Units*[A]
DIAMETER	75.82	76.58	mm
	2.985	3.015	in.
THICKNESS, CENTER POINT	475	525	µm
	0.0187	0.0207	in.
PRIMARY FLAT LENGTH	19.05	25.40	mm in.
	0.750	1.000	mm
SECONDARY FLAT LENGTH	9.66	12.70	mm
	0.380	0.500	in.
BOW		20	µm
		0.0008	in.
A.		50	µm
		0.0019	in.
B.		30	µm
		0.0011	in.
C.		10	µm
		0.0039	in.
TOTAL THICKNESS VARIATION SCHEDULE:			
A.		24	µm
		0.0009	in.
B.		12	µm
		0.0005	in.
C.		8	µm
		0.0003	in.
D.		4	µm
		0.0002	in.

[A] For referee purposes, metric (SI) units apply.

Table 2 Orientation and Flat-Location Requirements

Property	*Requirement*	
Option	V-Groove (see Figures 1 and 3)	Dove-Tail (see Figures 2 and 4)
PRIMARY FLAT ORIENTATION	(011) ± 0.5° [B], under an Arsenic facet. The primary flat shall be perpendicular to the "V" etch figure.[C]	(011) ± 0.5° [B], under a Gallium facet. The primary flat shall be perpendicular to the "Dove-tail" etch figure.[C]
SECONDARY FLAT LOCATION	90° ± 5° counterclockwise from the primary flat.	90° ± 5° clockwise from the primary flat.
SURFACE ORIENTATION[A]		
A.	(100) ± 0.5° (see Figure 1.)	(100) ± 0.5° (see Figure 2.)
B.	(100) off 2° ± 0.5° towards the(110) plane which is between the primary and secondary flats (see Figure 3.)	(100) off 2° ± 0.5° towards any nearest (110) plane (see Figure 4.)
ORTHOGONAL MISORIENTATION	± 5° (see Figure 5.)	± 5° (see Figure 5.)

[A] The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted towards the (110) plane of the crystal.

[B] See Table 1.

[C] Using A-B, bromine-methanol, ammonium hydroxide: hydrogen peroxide etch. See Figures 1 through 4. Figures 1 and 2 also show the orientation of the V-groove and Dove-tail figures relative to KOH etch pits.

SEMI M9.5-96
STANDARD FOR ROUND 100 mm POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE WAFERS FOR ELECTRONIC DEVICE APPLICATIONS

NOTE: This entire document was revised in 1995.

The complete specification for this product includes all general requirements of SEMI M9.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*
DIAMETER[A]	100.0	± 0.5	mm
THICKNESS, CENTER POINT	625	± 25	µm
PRIMARY FLAT LENGTH	32.5	± 2	mm
SECONDARY FLAT LENGTH	18	± 2	mm

[A] The diameter standard means that the dimension is centered to this value.

Table 2 Orientation and Flat- Location Requirements

Property	*Requirement*
PRIMARY FLAT ORIENTATION	$(0\bar{1}1) \pm 0.5°$ [A], under an Arsenic facet. The primary flat shall be perpendicular to the "V" etch figure.[B]
SECONDARY FLAT ORIENTATION	90° ± 5° counterclockwise from the primary flat.
SURFACE ORIENTATION[C]	(100) ± 0.5°
A.	(See Figure 1 in SEMI M9.)
B.	(100) off 2° ± 0.5° toward the (110) plane which is between the primary and secondary flats (See Figure 3 in SEMI M9.)
ORTHOGONAL MISORIENTATION	± 5° (See Figure 5 in SEMI M9).

[A] See Table 1 in SEMI M9.

[B] Using A-B, bromine-methanol, ammonium hydroxide: hydrogen peroxide etch. See Figures 1 and 3 in SEMI M9. Figure 1 also shows the orientation of the V-groove figures relative to KOH etch pits.

[C] The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted toward the (110) plane of the crystal.

SEMI M9.6-95
STANDARD FOR ROUND 125 mm DIAMETER POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE WAFERS

The complete specification for this product includes all general requirements of SEMI M9.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*
DIAMETER	125.0	± 0.3	mm
THICKNESS, CENTER POINT	625	± 25	µm
PRIMARY ORIENTATION FLAT DIAMETER[A]	121.0	± 0.3	mm
SECONDARY FLAT DIAMETER[B]	123.5	± 0.3	mm

[A] Actual Primary Orientation Flat Length depends on allowed variation in the wafer diameter and the orientation flat diameter. Variation in Primary Orientation Flat Length is calculated assuming that the end points of Primary Orientation Flat will have curvature of a circle of radius R = 0 or R = 3 mm; this circle will be tangent to the orientation flat and also tangent to the wafer circumference. Calculated nominal linear length of Primary Orientation Flat (the straight part of the flat) are 44.00 mm in a case of R = 0 mm and 42.90 respectively on a case of R = 3 mm.

[B] Actual Secondary Flat Length also depends on allowed variation in the wafer diameter and the Secondary Flat Diameter. Variation in Secondary Flat Length is calculated. Calculated nominal linear lengths of the Secondary Flat (the straight part of the flat) are 27.22 mm in the case of R = 0 mm, and 26.25 mm, respectively, in the case of R = 3 mm.

Table 2 Orientation and Flat-Location Requirements

Property	*Requirement*
PRIMARY FLAT ORIENTATION	(011) ± 1.0°, under an Arsenic facet. The primary flat shall be perpendicular to the "V" etch figure.[C]
SECONDARY FLAT ORIENTATION	90° ± 5° counterclockwise from the primary flat.
SURFACE ORIENTATION	
A.	(100) ± 0.5° (see Figure 1 in M9.)
B.	(100) off 2° ± 0.5° towards the (110) plane which is between the primary and secondary flats (see Figure 3 in M9.)
ORTHOGONAL MISORIENTATION	± 5° (see Figure 5 in M9.)

[A] The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted towards the (110) plane of the crystal.

[B] See Table 1.

[C] Using A-B, bromine-methanol, ammonium hydroxide: hydrogen peroxide etch. See Figures 1 through 4. Figure 1 also shows the orientation of the V-groove figure relative to the KOH etch pits.

NOTICE: These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI M9.7-0200
SPECIFICATION FOR ROUND 150 mm POLISHED MONOCRYSTALLINE GALLIUM ARSENIDE WAFERS (NOTCHED)

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the North American Compound Semiconductor Committee. Current edition approved by the North American Regional Standards Committee on December 15, 1999. Initially available at www.semi.org January 2000; to be published February 2000. Originally published in 1995; previously published in 1996.

NOTE: This document was rewritten in its entirety in February 2000.

1 Purpose

1.1 This specification defines properties of 150 mm monocrystalline GaAs substrates, in agreement with presently established industry practice. It uniquely defines those mechanical parameters that do not need, for technical reasons, a choice of different values.

2 Scope

2.1 The parameters defined include the values and tolerances of wafer diameter, thickness and surface orientation. The position and depth of the notch and laser marking are also specified.

2.2 The complete specification of this product includes the requirements of SEMI M9, excluding those that are not relevant to this specification (e.g., flat positions).

2.3 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

4 Physical Requirements

Table 1 Physical Requirements

Property	*Specification*	*Tolerance*	*Unit*	*Reference*
WAFER				
Diameter	150.0	± 0.5	mm	
Thickness, center point	675	± 25	µm	
Surface orientation A	(100)	0.5 max.	degrees	Figure 2
Surface orientation B				
Tilt	2 off (100) towards (110)	± 0.5	degrees	Figure 3
Orthogonal misorientation	0	± 5 max.	degrees	Figure 4
NOTCH				
Orientation	[010]	± 2	degrees	Figure 1
Depth	1.0	+ 0.25, -0.0	mm	Figure 5
Opening angle	90	+ 5, -1	degrees	Figure 5
LASER MARKING				
Surface	front side			
Position	adjacent to notch			Figure 6
Mandatory content	check characters			SEMI M12

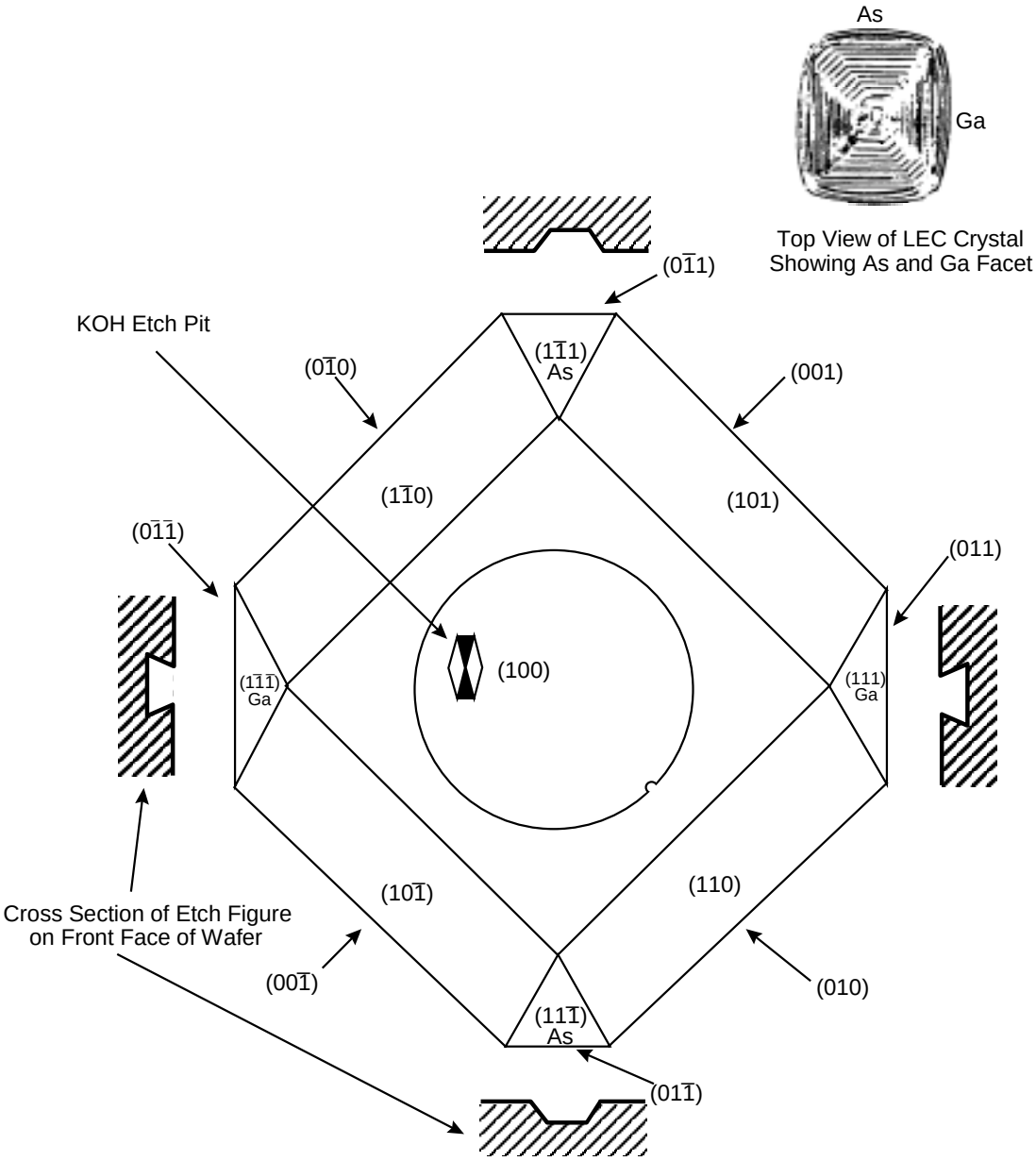

Figure 1
Diagram Shows a GaAs Wafer with Notch

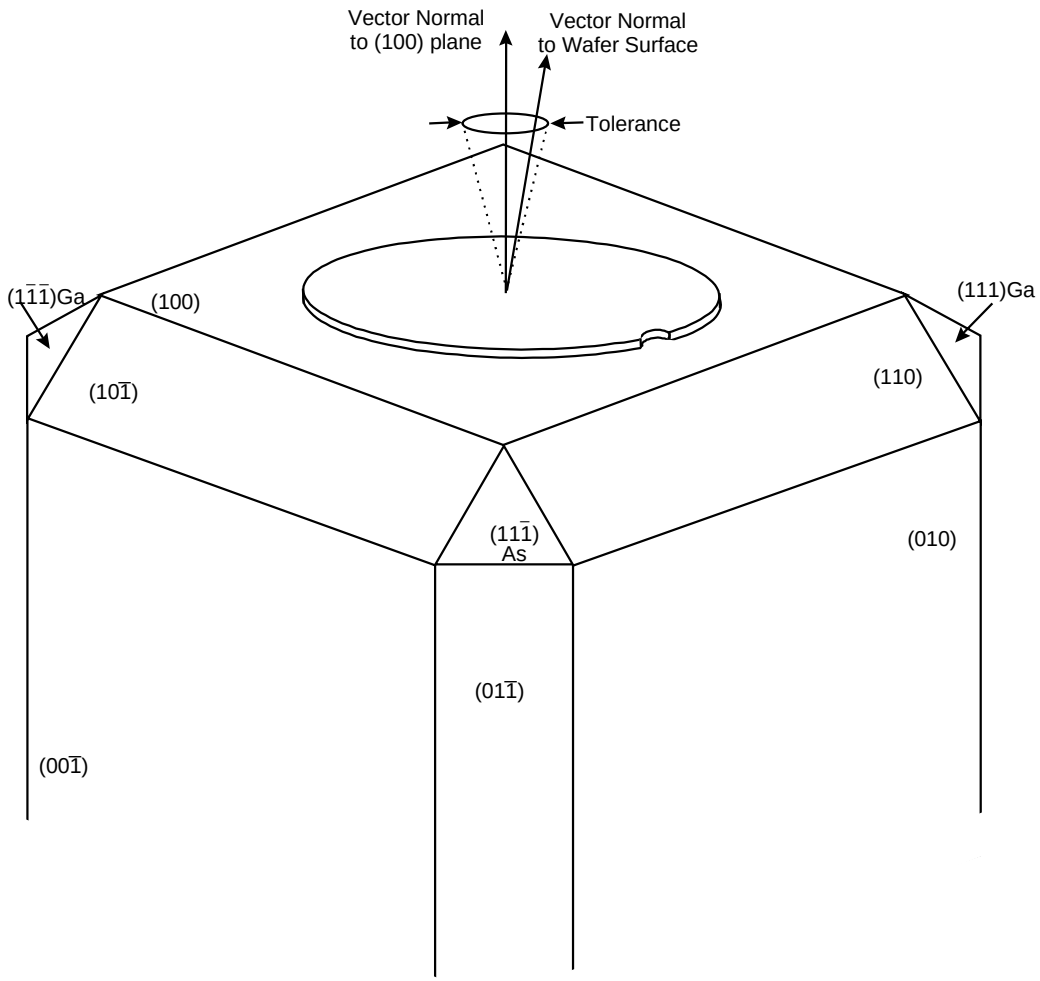

Figure 2
Notched GaAs Wafer Illustrating Surface Orientation A

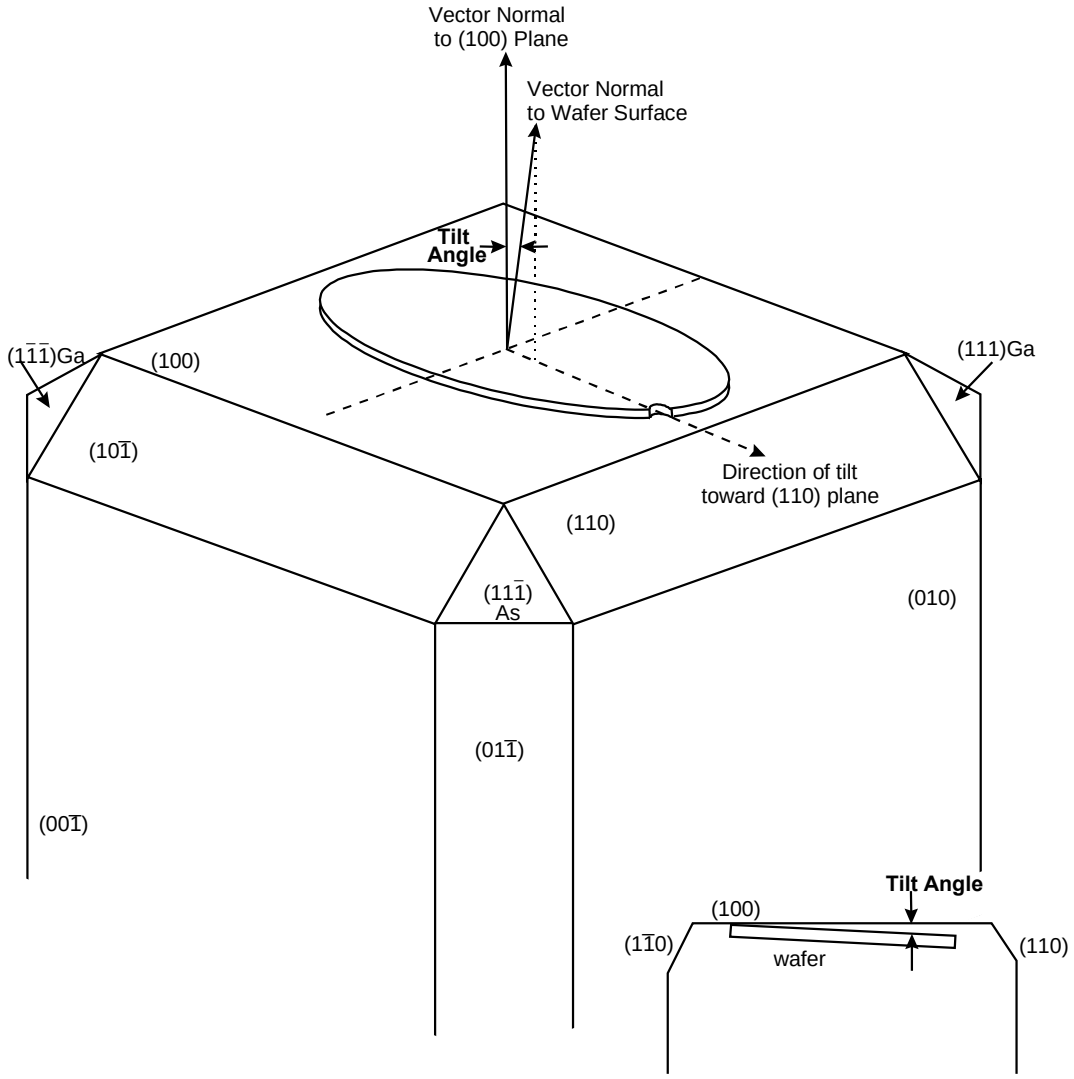

Figure 3
Notched GaAs Wafer Illustrating Surface Orientation B, with Tilt

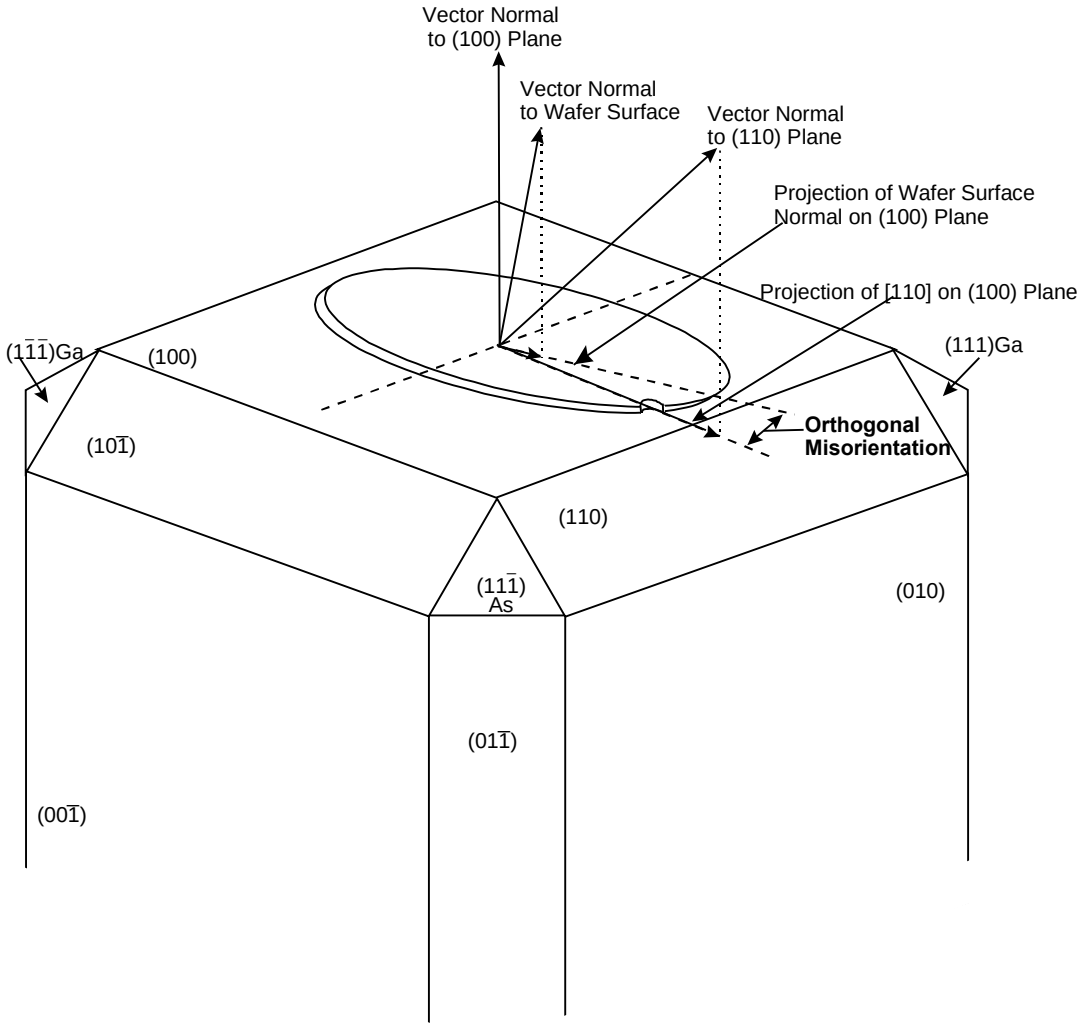

Figure 4
Notched GaAs Wafer Illustrating Surface Orientation B, with Tilt and Orthogonal Misorientation

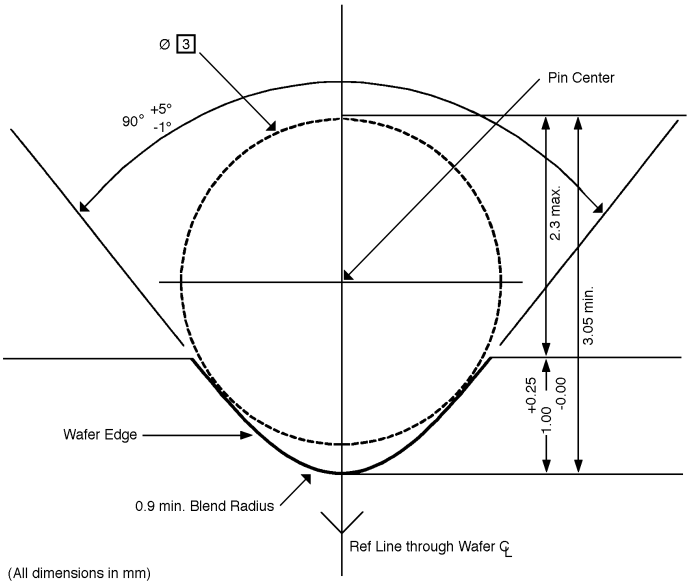

Figure 5
Notch Dimensions

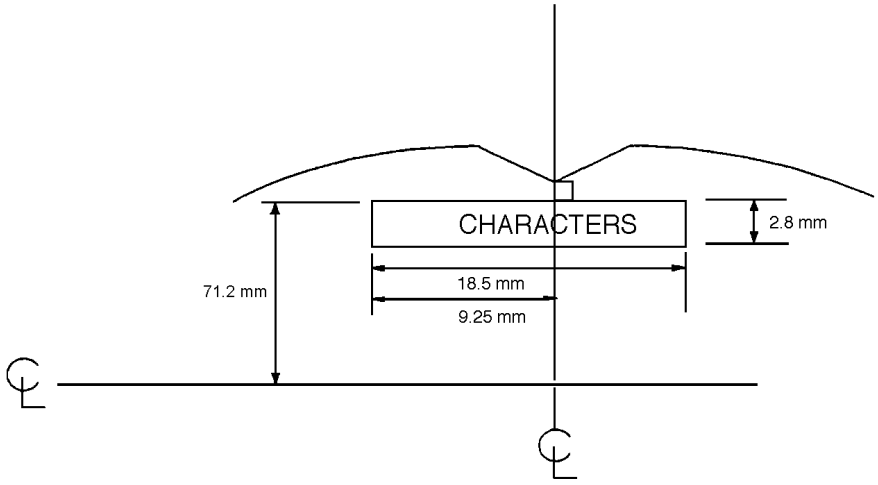

Figure 6
Character Window Location

NOTICE: SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copyrighted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI M10-1296
STANDARD NOMENCLATURE FOR IDENTIFICATION OF STRUCTURES AND FEATURES SEEN ON GALLIUM ARSENIDE WAFERS

1 Scope

1.1 The purpose of this document is to list, illustrate, and define various characters, features, and contaminants that are seen on highly polished GaAs wafers and present recommended practices for observation of these defects. These occurrences are frequently referred to as surface defects. The defects and common synonyms are arranged alphabetically in Section 4, and each structure is referred to by its most common name and, in some cases, probably origins.

1.2 Two cases of surface preparations are considered in this document: (1) surfaces after chemical polishing, and (2) mechanically and chemically polished surfaces.

1.3 This standard may involve hazardous materials, operations, and equipment. This standard does not purport to address all the safety problems associated with its use. It is the responsibility of whoever uses this standard to consult and establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

2 Applicable Documents

2.1 *SEMI Standard*

SEMI M9 — Specifications for Round Polished Monocrystalline Gallium Arsenide Slices

2.2 *ASTM Standard*[1]

F 47 — Crystallographic Perfection of Silicon by Preferential Etch Techniques

2.3 *Other Standard*[2]

ANSI/ASQC Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

3 Significance and Use

3.1 This document contains a compilation of the most commonly observed singularly discernable structures on polished GaAs surfaces. Ambiguities and uncertainties regarding surface defects may be resolved by reference to this document.

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959 (The cited standard may be found in Volume 10.05 of the Annual Book of ASTM Standards.)

2 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

4 Definitions and Descriptions of Terms

cell structure — (block structure): Malformations attributable to crystal inhomogeneities and that have their origins in the crystal growth process.

chips — (edge chips, peripheral chips, peripheral indents, surface chips): Areas of material mechanically removed from the surface or edge of a wafer.

> Chips indicate crystallographic damage in the adjacent material. The origins of some chips are in the handling of wafers arising from the physical transfer or placement of the specimen for process, measurement, or inspection purposes. The size of a chip is defined by its maximum radial depth and peripheral chord length as measurable on an orthographic shadow projection of the specimen outline.

apex chip —Any material missing from the edge of a wafer having at least 2 distinct interior boundaries which form one or more distinct intersections.

chuck marks — Any physical mark on either surface of a wafer caused by a chuck or wand.

contaminant — (solvent residue, wax residue, film, mottled surface, smudge): Surface feature that cannot be removed by the pre-inspection (non-etching) cleaning.

NOTE Contaminant may be foreign matter on the surface such as localized areas which are smudged, stained, discolored, mottled, etc., or larger areas exhibiting a hazy or cloudy appearance resulting from a film of foreign material.

> Solvent residue: type of film found on wafer surfaces after solvent evaporation from the surface. Note: The residue comes from either the solvent itself or material that the solvent has removed from the surface and redeposited. Wax residue: film of wax that migrated onto the wafer surface from several possible sources.

NOTE The wax originally may have been used to hold the crystal in place during slicing or polishing. Excessive heat used in mounting or demounting, during lapping or polishing processes, may cause the wax to polymerize.

crack — Cleavage or fracture that extends to the surface of a slice. It may or may not pass through the entire

thickness of the slice. Often cracks are caused by the improper handling of wafers.

NOTE Some crack-defect structures can be traced to process related events.

cavity — (void) A vacancy or hole in the wafer.

NOTE Usually left by dissolved precipitates and Ga inclusions, As disassociation or created by excess vapor pressure.

Dimple — Deformation appearing in mechanically polished GaAs wafers.

NOTE This surface texture can be induced by floating the wafers during the initial stages of polishing.

Dislocation — See *slip, lineage, pit.*

edge chip — See *chip*.

Embedded — abrasive grains Abrasive particles mechanically forced into the surface of the wafer.

etch pi t — See *pit.*

film — See *contaminant.*

flake — Material missing from one, but not the other, side of a wafer, whose sole interior boundary is one distinct line or arc not exceeding 2 mm in length, nor projecting into the wafer beyond the specified edge exclusion.

gallium inclusion — A segregated Ga-rich droplet incorporated into the surface structure.

NOTE Normally caused by insufficient As vapor pressure at the termination of the crystal growth process or by Ga complexing with some dopants near saturation.

grain boundary — See *lineage*.

haze — (cloud, nebula): Attributable to light scattering by concentrations of microscopic surface irregularities such as pits, oxides, small ridges or scratches, particles, etc. The light reflection from an individual irregularity probably could not be readily detected by the unaided eye, so haze is a mass effect. It is seen as a high density of tiny reflections.

NOTE This type of contamination may occur during slicing, lapping, or polishing.

lamella — A special case of the twin. A multiple twin, extremely thin and relatively long, which may intersect more than one plane.

lineage — (dislocation pits, grain boundary): Low-angle grain boundary resulting from an array of dislocations. This angle may vary from a fraction of a second to a minute of arc difference in orientation from one part of the crystal to another. The array of dislocations will appear as rows of pits on a preferentially etched surface.

NOTE Lineage can be induced into the material in crystal growth or in subsequent thermal or epitaxial processes. Lineage will be visible to the unaided eye only after preferential etching.

macroscratch —See *scratch*.

microscratch — See *scratch*.

microtwin — See *twin*.

orange peel — (roughness, texture): Large featured roughened type of surface visible to the unaided eye, occasionally seen on all types of polished wafers.

NOTE Orange peel is usually symptomatic of a process control problem. In the case of chemical polishing for instance, an excessively fast polishing rate, or nonuniform flow of oxidizer during polishing, can result in orange peel. Conversely, it can also be caused by insufficient stock removal.

particulate — (dust): Discrete particle of material which can usually be removed by (non-etching) cleaning.

pit — (dislocation, etch pit): Depression in the wafer surface which has a definite and distinguishable shape, that is, a place where the sloped sides of the pit meet the wafer surface.

NOTE Pits can be caused by the various growths or polishing processes.

Preferential etch pits result where dislocations intersect the wafer surface after treatment with a preferential etch. These pits so formed usually have a characteristic shape related to the surface and bulk crystallographic orientation.

polycrystalline — (poly): Body of semiconductor materials that contain large-angle grain boundaries, twin boundaries, or both.

precipitates — A localized concentration of dopant at its solubility limit formed during crystal growth.

probe damage — Any damage to the wafer surface caused by mechanical probing or measurement.

roughness — see *orange peel*.

saw blade defects —A depression in the wafer surface made by the blade, which may not be visible before polishing.

saw exit chip —A particular kind of edge chip, found at the point where the saw blade completed its cut of the wafer. It is typically flat or arc shaped instead of irregular in shape, and can sometimes be confused with the orientation flats.

scratch — (macroscratch, microscratch): Long, narrow, shallow groove or cut below the established plane of the surface, seen either before or after etching. The ratio of the length of the figure to the width of the figure must be greater than 5:1 in order to be defined as a scratch.

Macroscratches are visible to the unaided eye under high intensity illumination.

Microscratches are not visible to the unaided eye under high intensity illumination.

slip — (dislocation pit, preferential etch pits, stress effect) (see also *pit*): Process of plastic deformation in which one part of a crystal undergoes a shear displacement relative to another in a fashion which preserves the crystallinity of the material. Slip is evidenced by a pattern of one or more straight lines of 10 or more dislocation etch pits per millimeter which do not necessarily touch each other.

striations — Striations appear in Czochralski grown crystals regardless of their resistivity.

tweezer mark — Any mark on the wafer caused by handling with tweezers.

twin — A body of crystal within the wafer in which the lattice is of two parts, related to each other in orientation as mirror images, across a coherent planar interface known as the twinning plane or twin boundary.

SEMI M11-0704
SPECIFICATIONS FOR SILICON EPITAXIAL WAFERS FOR INTEGRATED CIRCUIT (IC) APPLICATIONS

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on April 22, 2004. Initially available at www.semi.org June 2004; to be published July 2004. Originally published in 1988; previously published November 2003.

1 Purpose

1.1 This specification defines and provides examples of silicon epitaxial wafer requirements for integrated circuit device manufacture. It is restricted to wafers of diameter 100 mm or greater with epitaxial layer thickness less than or equal to 25 μm. By defining inspection procedures and acceptance criteria, both suppliers and consumers may uniformly define product characteristics and quality requirements.

2 Scope

2.1 This specification covers characteristics of both the substrate (as specified in SEMI M1) and the epitaxial layer, in-cluding handling and packaging. The primary standard-ized properties set forth in this specification relate to physical, electrical, and surface defect parameters.

2.2 The primary standard-ized properties set forth in this specification relate to physical, electrical, and surface defect parameters.

2.3 A complete purchase specification requires that additional physical properties be specified along with suitable test methods for their measurements. SEMI M18 may be used for this purpose.

2.4 These specifications are specifically directed to silicon homoepitaxial deposits on homogeneous silicon substrates only, for which more stringent uniformity and surface defect criteria are required than specified in SEMI M2.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Mono-crystalline Silicon Wafers

SEMI M2 — Specification for Silicon Epitaxial Wafers for Discrete Device Applications

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI M44 — Guide for Conversion Factors for Interstitial Oxygen in Silicon

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems using Certified Depositions of Monodisperse Polystyrene Latex Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI MF95 — Test Method for Thickness of Epitaxial Layers of Silicon on Substrates of the Same Type by Infrared Reflectance

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial Layers Using an Inline Four-Point Probe with the Single Configuration

SEMI MF398 — Test Method for Majority Carrier Con-centration in Semiconductors by Measurement of Wavelength of the Plasma Resonance Minimum

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

SEMI MF525 — Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF672 — Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe

SEMI MF723 — Practice for Conversion between Resistivity and Dopant Density for Boron-Doped and Phosphorus-Doped Silicon

SEMI MF951 — Test Method for Determination of Radial Interstitial Oxygen Concentration Variation in Silicon

SEMI MF1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption With Short Baseline

SEMI MF1239 — Test Methods for Oxygen Precipitation Characterization of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1241 — Terminology of Silicon Technology

SEMI MF1366 — Test Method for Measuring Oxygen Concentration in Heavily Doped Silicon Substrates by Secondary Ion Mass Spectrometry

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1393 — Test Method for Determining Net Carrier Density in Silicon Wafers by Miller Feedback Profiler Measurements with a Mercury Probe

SEMI MF1726 — Guide for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

3.2 *Other Standards*

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes[1]

ISO 14644-1 — Cleanrooms and associated controlled environments — Part 1: Classification of airborne particulates[2]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Many terms relating to silicon technology are defined in SEMI MF1241.

4.2 Descriptions of other epitaxial wafer defects covered in Table 1 are given in SEMI MF154.

4.3 Definitions of selected epi wafer defects, extended to consider automatic surface inspection are given below.

4.3.1 *mound (epi)* — a rounded protrusion on a semiconductor wafer surface, which may have one or more partially developed facets (see Figure 1).

NOTE 1: Scattering event size reported by SSIS will differ from the physical size of the object. The figure captions in the examples highlight this fact. No useful method exists at the present time to quantify this relationship (see Section 7.3.3.3)

4.3.1.1 *Discussion* — Related characteristics include the following:

- *Device characteristics that may be affected* — critical feature dimensions, lithographic equipment focus, gate oxide integrity.
- *Detection characteristics used for characterization* — mound height, diameter at 50% height.
- *Discrimination characteristics used for characterization* — positive height: 10–100 nm, or approximately 20% of the epi layer thickness; diameter: 0.1–6 μm; circular symmetry.
- *Specification characteristics used for wafer qualification* — number per wafer, mound height, height to diameter.

4.3.2 *epi stacking fault* — a two dimensional effect that results from a deviation from the normal stacking sequence of atoms in a crystal. [SEMI MF154, SEMI MF1727]

NOTE 2: Discrimination and specification characteristics are given in this section to facilitate equipment development (see Section 7.3.3.3) and are not intended for use in commercial wafer specifications.

4.3.2.1 *Discussion* — Epi stacking faults are typically linked together into squares in the case of {100} oriented wafers, and triangles in the case of {111} oriented wafers. Most stacking faults are nucleated at the epi layer substrate boundary, though some have been observed being nucleated further into the epi growth process. Faults are aligned along specific crystallographic directions. For {100} wafer the sides of the faults are aligned along <110> directions. The length of a side is typically proportional to the epi layer thickness and related to the crystallographic orientation. In order to minimize the strain around a stacking fault contaminants may diffuse to these defects. Some stacking faults may have an effect on the local growth rate giving the stacking fault a three dimension aspect. This three dimensional aspect changes their light scattering cross section when observed by an SSIS (see Figures 3 through 7). Still more complicated are overlapping stacking faults which scatter even more than a single stacking fault of the same size (see figure 4). Other types of defects may be composites of stacking faults and polysilicon growth which can also appear larger than a single stacking fault of the same lateral dimensions (see Figures 5 and 6). Related characteristics include the following:

1 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202. Website: www.asqc.org.

2 ISO Central Secretariat, C. P. 56, CH-1211 Genève 20, Switzerland; Website: www.iso.ch; available in the U.S. from American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036 Website: www.ansi.org.

- *Device characteristics that may be affected* — leakage and gate oxide integrity, from crystallographic changes.
- *Detection characteristics used for characterization* — side length and depth, orientation parallel to a <110> direction.
- *Discrimination characteristics used for characterization* — shape, length ~ epi layer thickness: 1–10 µm. Stacking faults may cluster (see Figure 7) and scatter more than a single stacking fault.
- *Specification characteristics used for wafer qualification* — Number per wafer. Since certain types of epi stacking faults have no observed impact on device performance while others are killer defects no number can be assigned without a clear identification of the type of epi stacking fault that is involved.

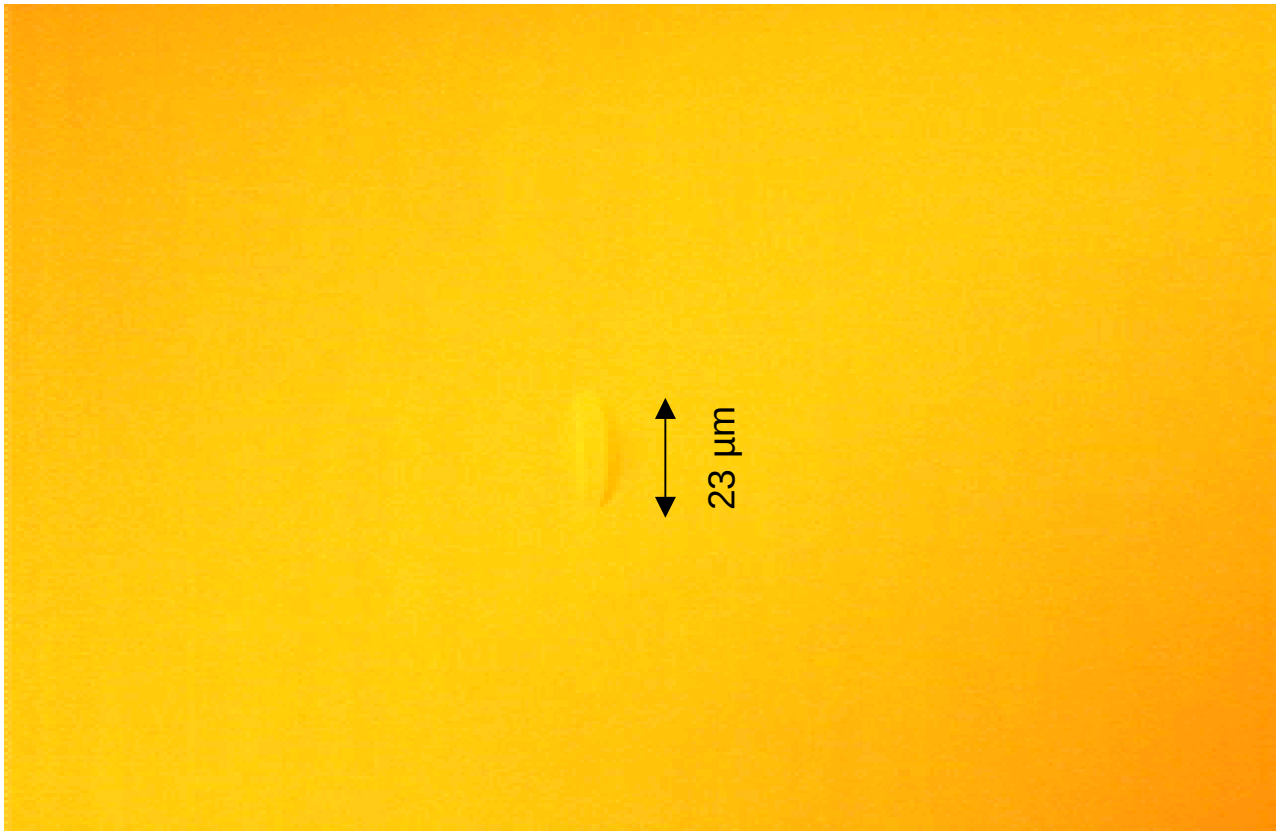

Figure 1
A Mound. Magnification 1000 times using Nomarksi Interference Microscopy. Approximate SSIS scattering event size 0.22 µm.

Figure 2
This is a mound that does not have the sharp edges of an Epitaxial Stacking Fault, but is not as high as a Bump. They are typically sized much smaller in a SSIS than their actual size, but some have facets that scatter enough light to be more easily detected. Some people refer to this feature as a hillock which is a type of mound. The shape can be either circular or square. Magnification 500 times using Nomarski Interference Microscopy. Approximate SSIS event size: 0.15 µm

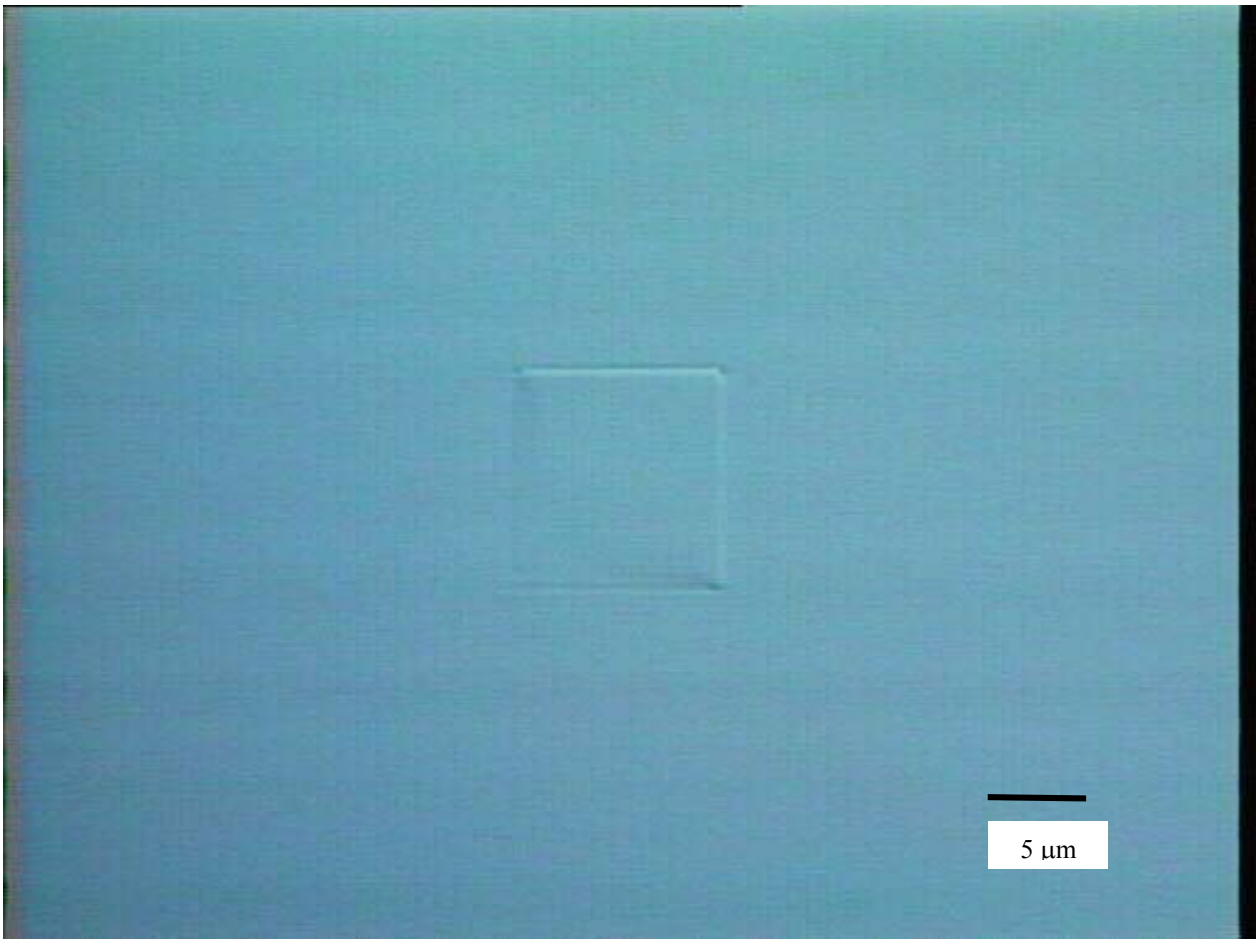

Figure 3
The Epi Stacking Fault (ESF) defect is a grown-in defect with 1 to 4 sides of a square visible. Magnification 1500 times using Nomarski Interference Microscopy. Approximate SSIS event size: 0.165 µm

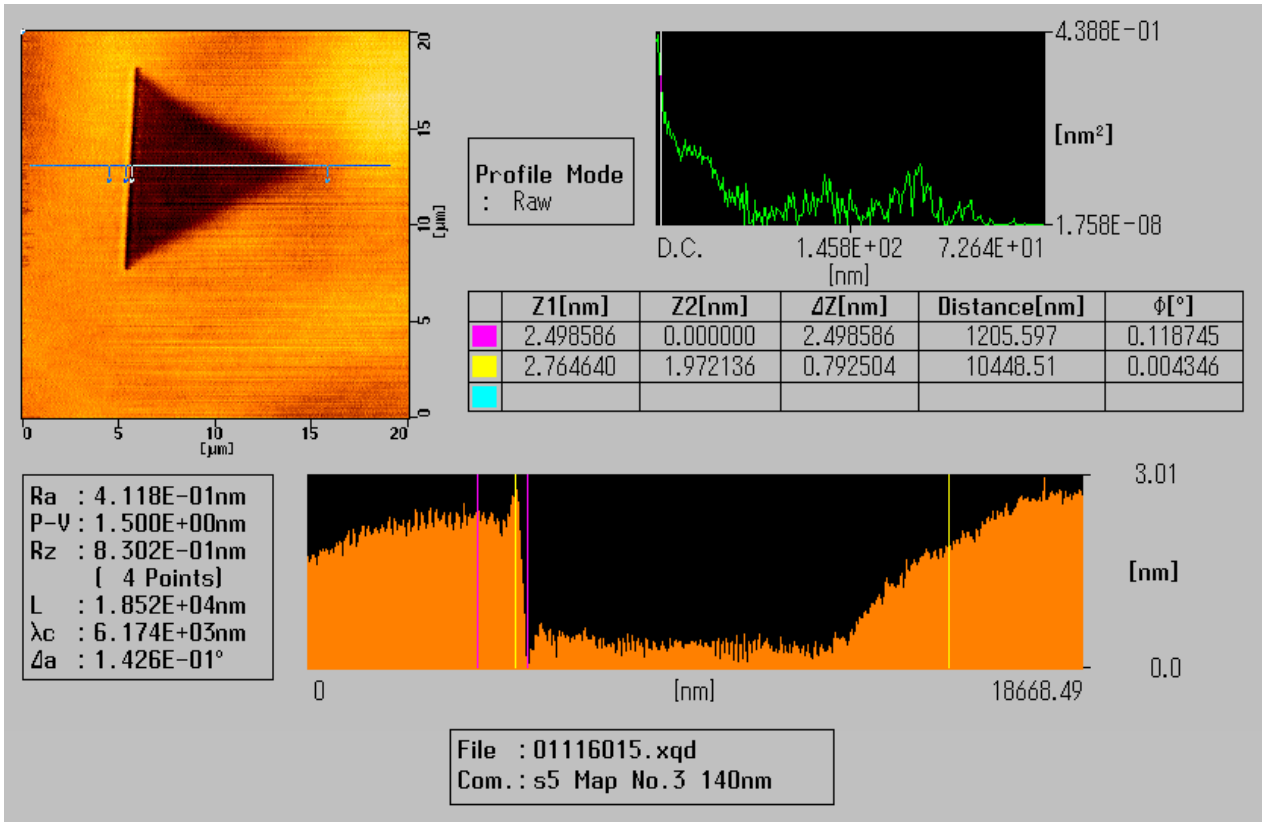

Figure 4
Epitaxial Stacking Fault. Atomic Force Microscope (AFM) Image. Approximate SSIS scattering event size 0.12 µm.

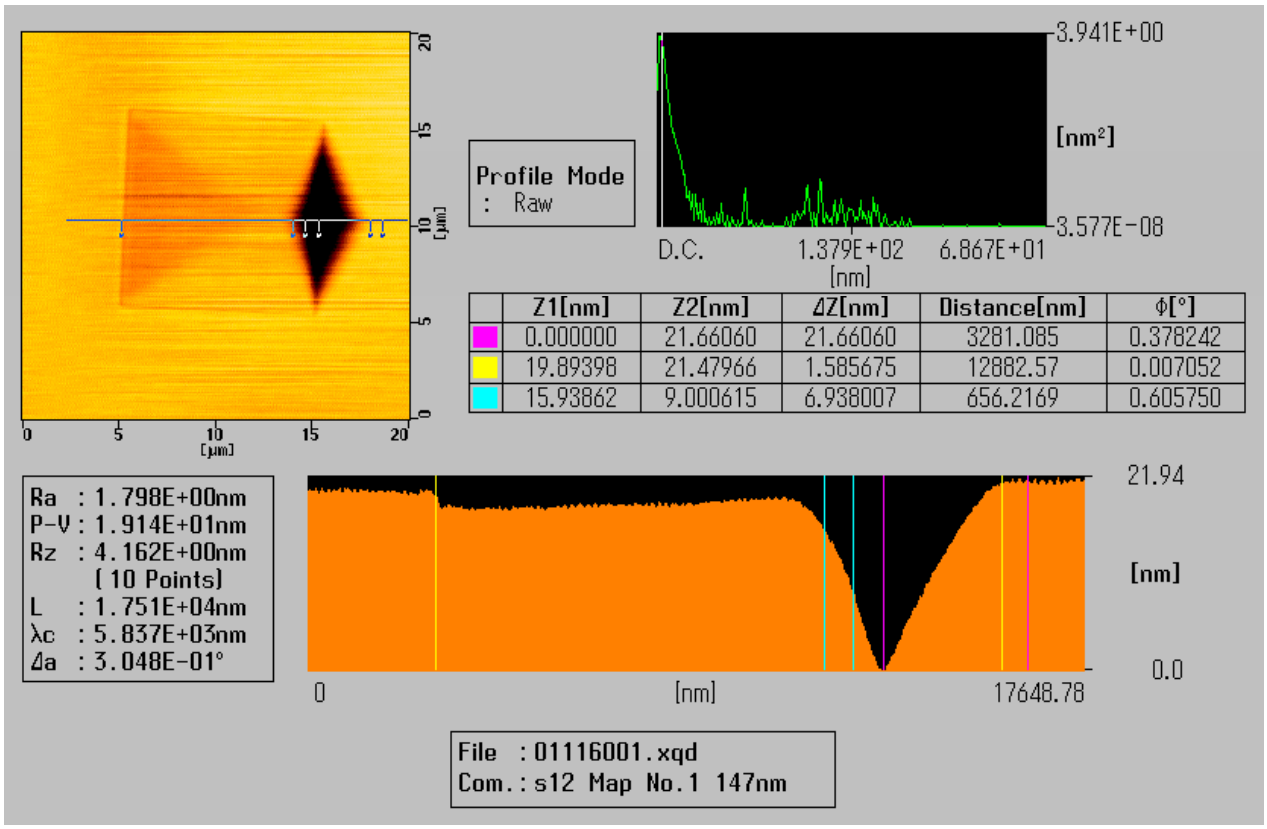

Figure 5
Epitaxial Stacking Fault showing four sides and a deep depression on on side of about 20 nm. Atomic Force Microscope Image. Approximate SSIS scattering event size, 0.30 µm.