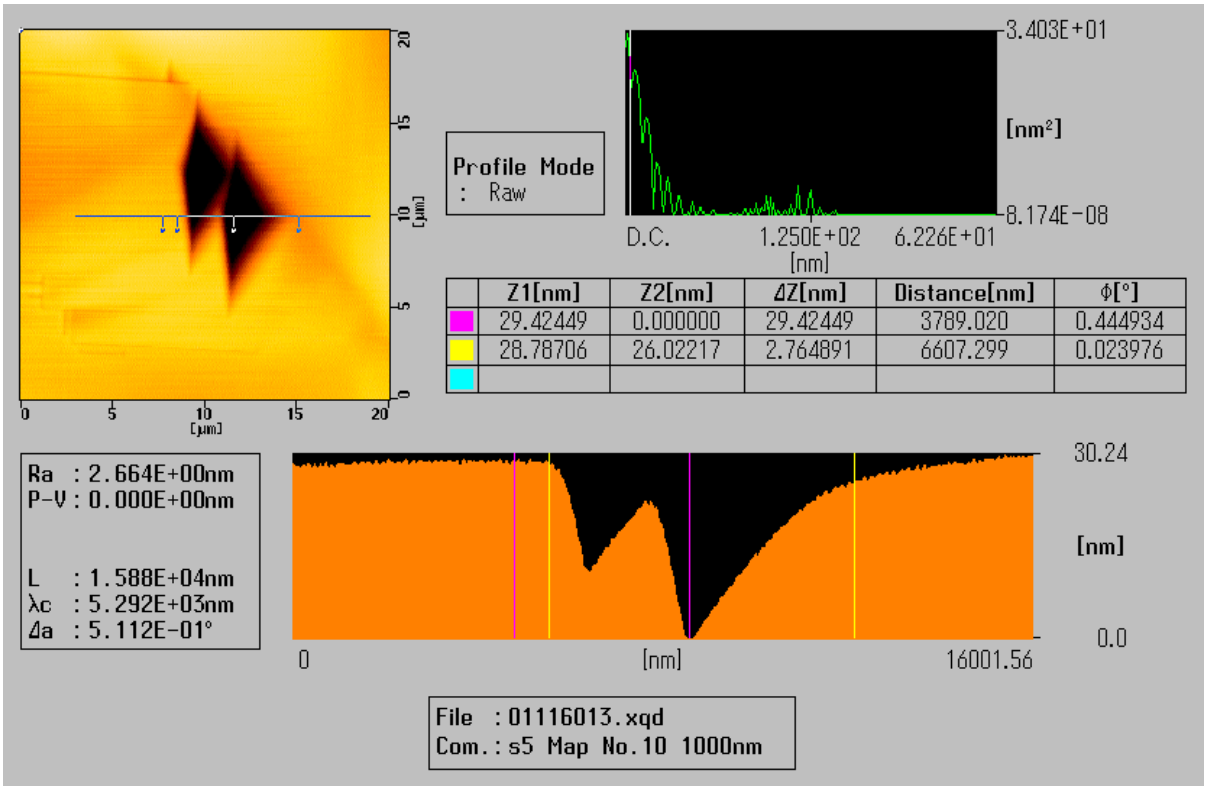

Figure 6
Double Epi taxial Stacking Fault. Atomic Force Microscope image. Approximate SSIS event scattering size 1.05 µm

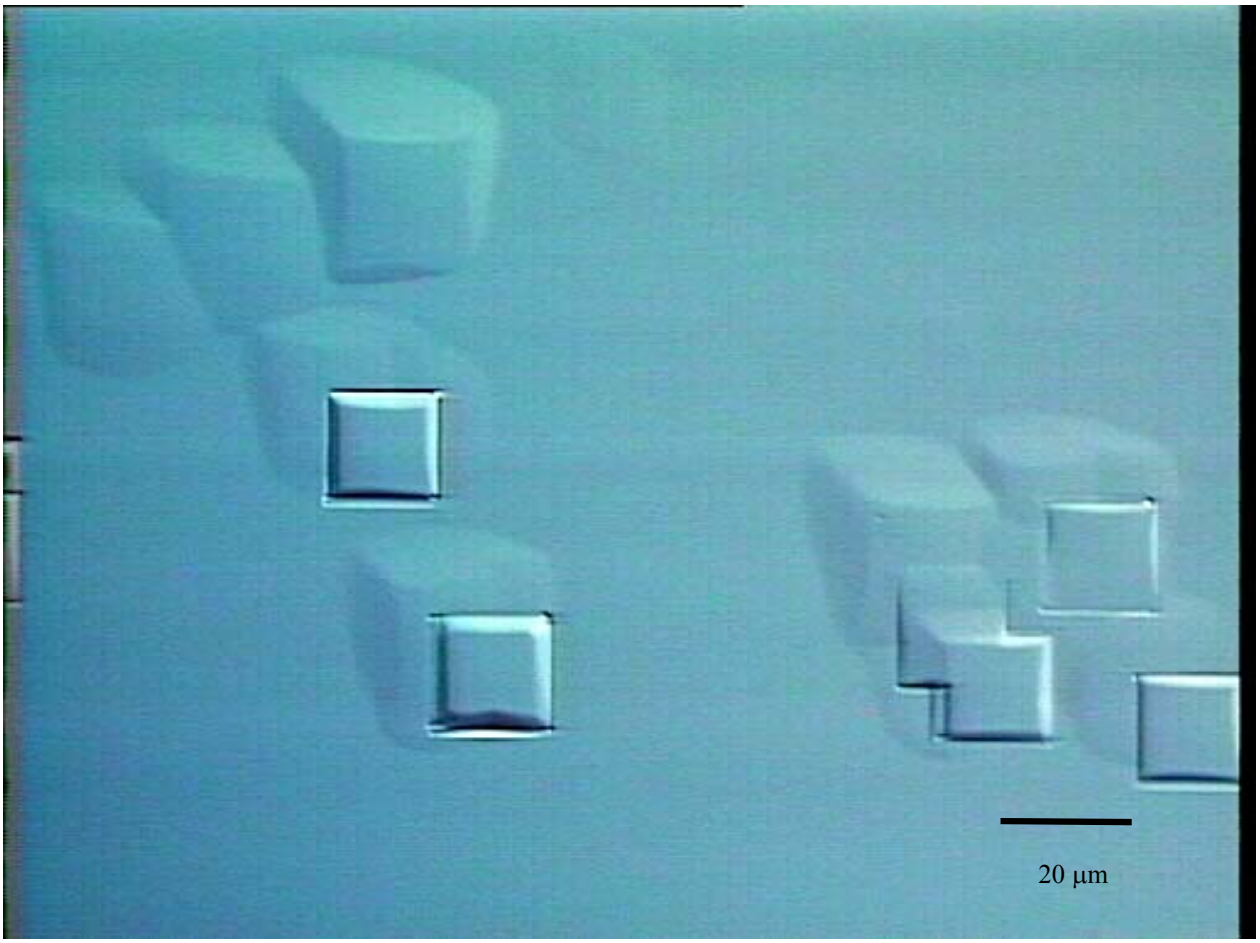

Figure 7
The Epitaxial Stacking Fault Cluster classification is used to define a group of ESFs in close proximity on the wafer surface. The group can either be overlapping or in a line (except when the line appears to be part of a Pre-Epi Scratch). Magnification 500 times using Nomarski Interference Microscopy. Approximate SSIS event size, 0.20 µm

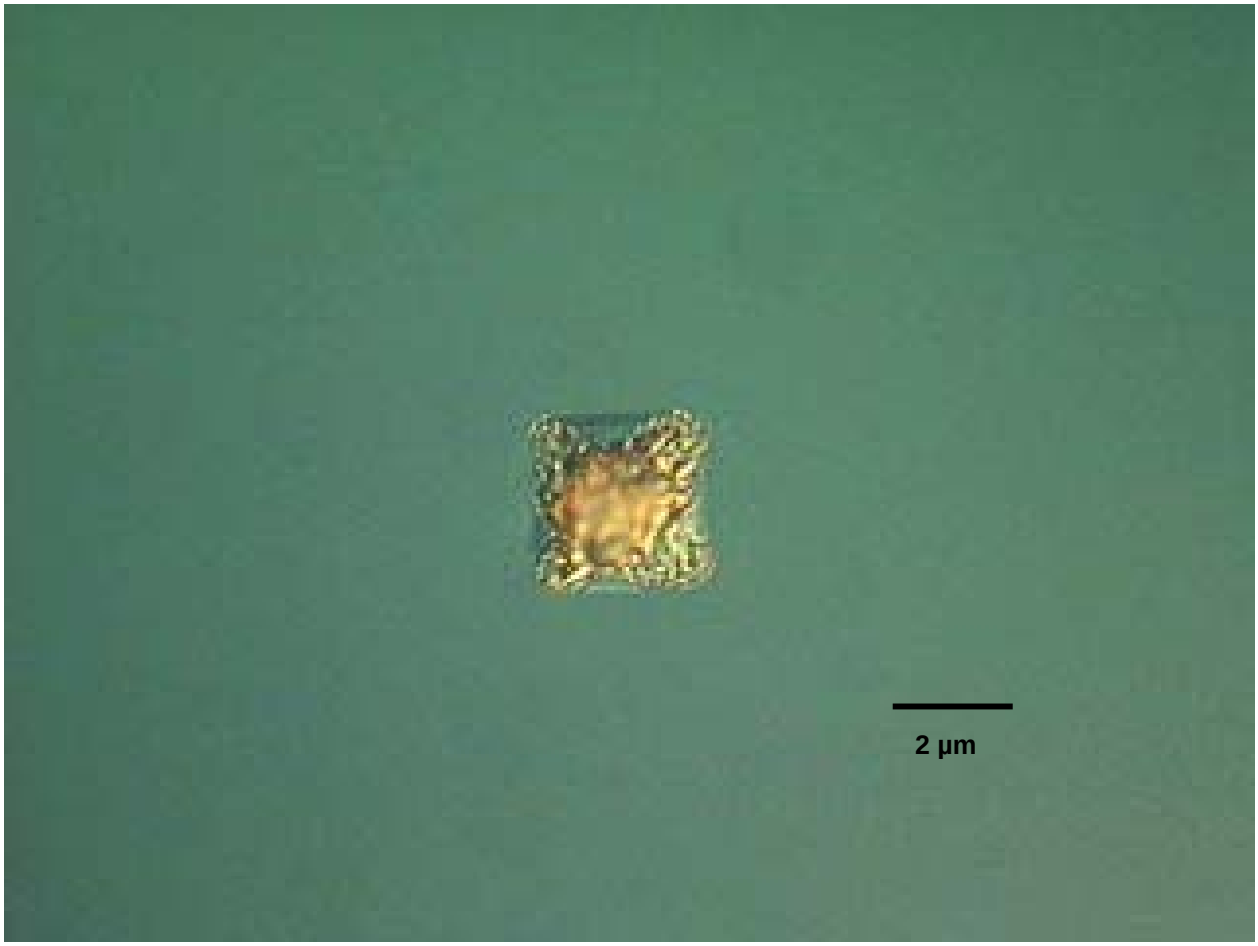

Figure 8
Composite Defect of polysilicon growth and stacking faults. Magnification 1000 times by Nomarksi Interference Microscopy. Approximate SSIS image event size >>1.0 µm

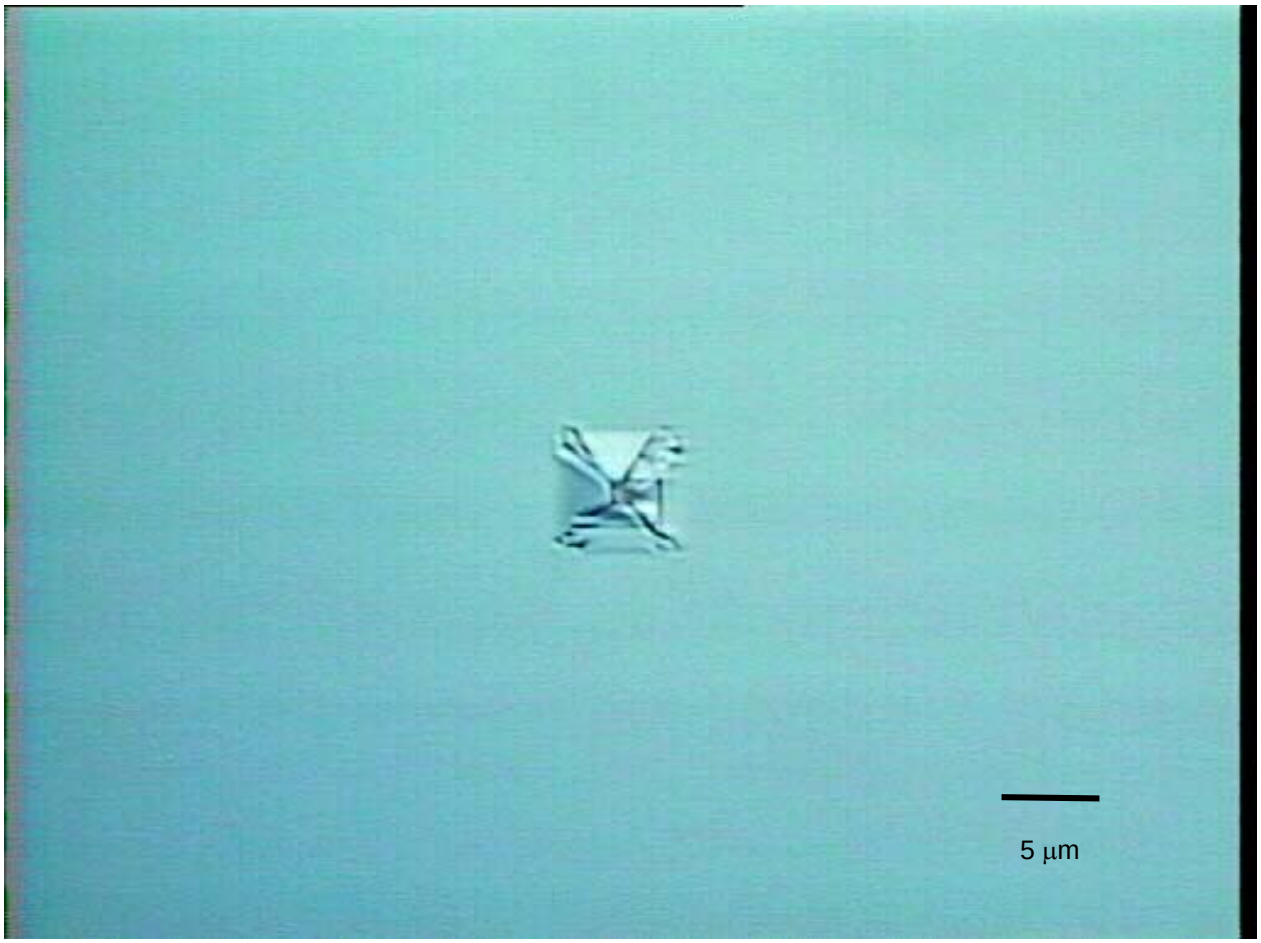

Figure 9
The Compound ESF defect is an epi stacking fault that has a broken surface, but maintains the square shape of an ESF. It typically scatters more light than a normal ESF because of the extra facets, so it is sized larger in a SSIS. Magnification 500 times using Nomarski Interference Microscopy. Approximate SSIS event size: 280 μm

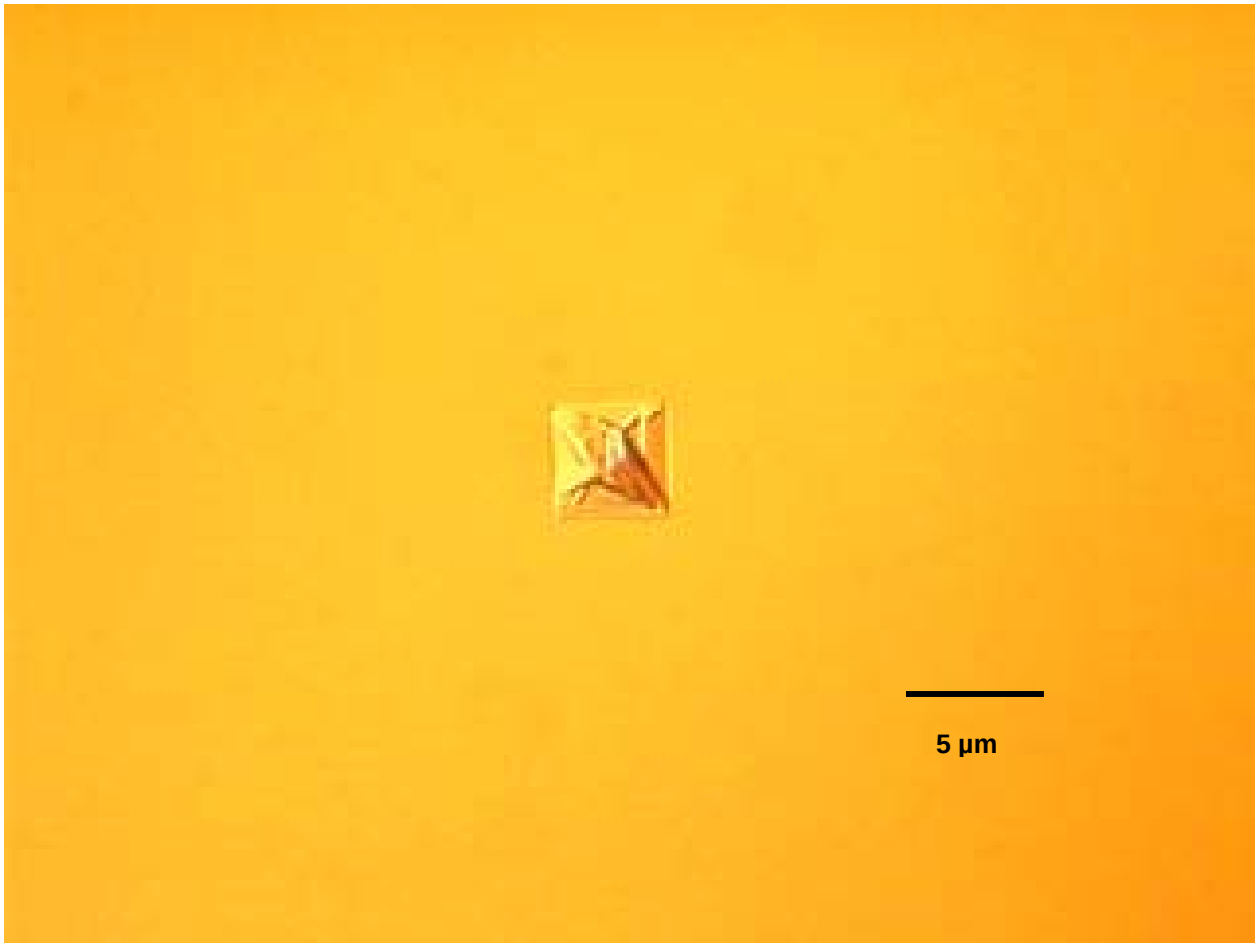

Figure 10
Composite Defect of polysilicon growth and stacking faults. Magnification 500 times by Nomarksi Interference Microscopy. Approximate SSIS image event size >>1.0 µm

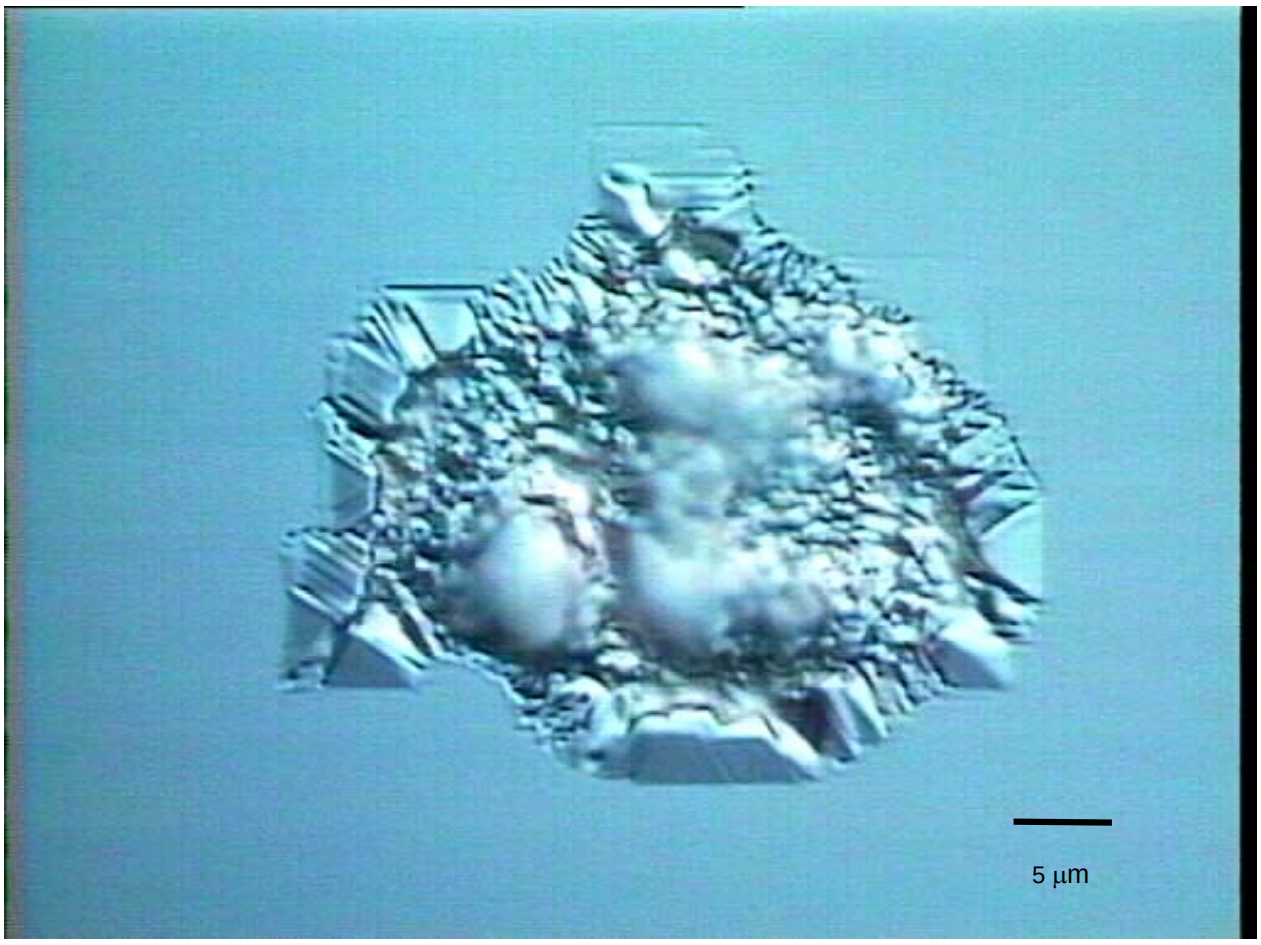

Figure 11
A Polysilicon Epitaxial Stacking Fault is a defect that covers a large area and is covered or surrounded by ESFs. This classification is used when the surface appears to be poly-crystalline rather than single crystal. It is almost always a Large Area Defect and is caused by a large particle that may still be visible (see Buried Particle). Magnification 1500 times using Nomarski Interference Microscopy. Approximate SSIS event size, 440 µm

4.4 Other terms are defined as follows:

4.4.1 *autodoping, of an epitaxial layer* — incorporation of dopant originating from the substrate into the epitaxial layer. Also called *self-doping*.

NOTE 3: Sources of autodoping can be the back and front surfaces and edges of the substrate, other substrates in the reactor, the susceptor, or other parts of the deposition assembly.

4.4.2 *chemical vapor deposition, in semiconductor technology* — a process in which a controlled chemical reaction produces a thin surface film.

NOTE 4: Epitaxial growth is an example of a special case of chemical vapor deposition (CVD).

4.4.3 *edge crown* — the difference between the surface elevation 1/8 inch (3.2 mm) from the edge of the wafer and the elevation at the wafer edge.

4.4.4 *effective layer thickness, of an epitaxial layer* — the depth from the front surface in which the net carrier density is within the specified limits.

4.4.5 *epi profile slope, of an epitaxial layer* — the difference between the net carrier density at 0.75 of the layer thickness and the net carrier density at 0.25 of the layer thickness divided by one-half the layer thickness:

$$\text{epi profile slope} = \frac{N_{0.75t} - N_{0.25t}}{0.5t}$$

where :

N = net carrier density, cm^{-3}, and

t = layer thickness, μm.

4.4.6 *epitaxial layer* — a layer of single crystal semiconductor material grown on a host substrate which determines its orientation.

4.4.7 *epitaxy* — the growth of a single crystal layer on a substrate of the same material, homoepitaxy; or on a substrate of different material with a compatible crystal structure, heteroepitaxy.

4.4.8 *flat zone, of an epitaxial layer* — the depth from the front surface to the point where the net carrier density is 20% greater than or less than the average net carrier density (see Section 7.3.2) of the region between 0.25 and 0.75 of the layer thickness.

4.4.9 *laser light scattering event* — a signal pulse that exceeds a preset threshold, generated by the interaction of a laser beam with a discrete scatterer at a wafer surface as sensed by a detector.

4.4.10 *thickness, of an epitaxial layer* — the distance from the surface of the wafer to the layer-substrate interface.

4.4.11 *transition width, of an epitaxial layer deposited on a more heavily doped substrate of the same conductivity type* — the difference between the layer thickness as determined by infrared reflectance (see Section 7.3.1) and the flat zone based on the same thickness measurement.

5 Ordering Information

5.1 Purchase orders for the epitaxial layer on substrates furnished to this specification shall include the following items:

5.1.1 *Substrate Characteristics*

5.1.2 *Epitaxial Layer Characteristics*

5.1.2.1 Silicon Source for Epitaxial Growth (if required) (see Note 3.)

5.1.2.2 Epitaxial Layer Conductivity Type and Doping Source (see Note 3.)

5.1.2.3 Etch Removal (if required)

5.1.2.4 Epitaxial Layer Center Point Thickness and Thickness Tolerances

5.1.2.5 Epitaxial Layer Thickness Variation Range

5.1.2.6 Epitaxial Layer Centerpoint Net Carrier Density and Net Carrier Density Tolerances (see Note 4.)

5.1.2.7 Epitaxial Layer Net Carrier Density Variation Range

5.1.2.8 Epitaxial Layer Defect Limits

5.1.3 Methods of Test and Measurements (see Section 7.)

5.1.4 Lot Acceptance Procedures (see Section 8.)

5.1.5 Certification (if required) (see Section 9.)

5.1.6 Packing and Marking (see Section 10.)

NOTE 5: The dopant, doping method, and growth method are difficult to ascertain in the finished wafers. Verification test procedures or certification of these characteristics shall be agreed upon between the supplier and the purchaser. (See Section 9.)

NOTE 6: Care should be taken in converting between carrier density and resistivity using SEMI MF723. Multiple conversions may introduce differences in values. For example, converting from carrier density (C_i) to resistivity and back to carrier density (C_f), may result in C_i not equaling C_f.

6 Requirements

6.1 As a minimum, the substrate shall conform to SEMI M1 and the appropriate individual polished monocrystalline silicon wafer standard.

6.2 Epitaxial wafer defects shall not exceed the limit as given in Table 1.

6.2.1 Limits for slip, which may require destructive testing, shall be specified in a purchase order together with an appropriate test method. In the absence of another specification, the wafer will contain no slip lines within the quality area. (See Table 1, Note 1.)

NOTE 7: When an unetched wafer is observed for slip it is impossible to differentiate between slip and linear misfit lines.

6.3 *Layer Thickness Variation* — Unless otherwise specified, the thickness variation shall be determined from value measured at the center and locations centered 12 mm ± 1 mm from the periphery, on diameters both parallel and perpendicular to the primary flat,

$$\text{Variation}(\%) = \frac{t_{max} - t_{min}}{t_{max} + t_{min}} \times 100$$

where t_{max} and t_{min} denote the maximum and minimum thickness values measured. The 12 mm locations have been defined based on instrument processing and fixturing considerations.

6.4 *Layer Net Carrier Density Variation* — The net carrier density variation shall be determined from values measured at the center and locations with center of the probe at 12 mm ± 1 mm from the periphery, on diameters both parallel and perpendicular to the primary flat,

$$\text{Variation}(\%) = \frac{N_{max} - N_{min}}{N_{max} + N_{min}} \times 100$$

where N_{max} and N_{min} denote the maximum and minimum values measured. The 12 mm locations have been defined based on instrument processing and fixturing considerations.

7 Test Methods and Measurements

7.1 Measurements shall be carried out in conformance with the specified SEMI Test Methods. Where no methods are specified or where choices are given, the supplier and purchaser shall agree in advance on the means for making the measurement.

7.2 *Substrates* — Determine in accordance with methods specified in SEMI M1.

7.3 *Epitaxial Layer*

7.3.1 *Thickness* — Determine in accordance with SEMI MF95 or SEMI MF110.

NOTE 8: In the case of thin layers and graded doping transitions, SEMI MF95 and SEMI MF110 may not be suitable. See the scopes of these test methods to determine their limitations. In all cases, there is a possibility that various types of infrared reflectance instrumentation may result in different values of epitaxial layer thickness. Therefore, the instrumentation used shall be agreed upon between supplier and purchaser.

7.3.2 *Net Carrier Density* — Determine by method(s) agreed upon between supplier and purchaser.

NOTE 9: SEMI MF1392 and SEMI MF1393 are methods for measuring net carrier density using a mercury probe contact. If resistivity is measured, as by SEMI MF374 or SEMI MF525, conversion to dopant density shall be made using SEMI MF723. Net carrier density of very heavily doped layers (or substrates) may be found using SEMI MF398. Net carrier density profiles may be determined directly in accordance with SEMI MF1392 or SEMI MF1393 or indirectly in accordance with SEMI MF672, with conversion from resistivity to net carrier density in accordance with SEMI MF723. If the method used for determining the net carrier density profile is not the same as that used to determine the center-point net carrier density, correlation between the two methods used shall be established.

7.3.3 *Epitaxial Wafer Defects* — Determine in accordance with the methods given in Table 1.

7.3.3.1 Surface inspection shall be performed before any other testing. Wafers may be cleaned prior to inspection to minimize difficulty in the visual inspection of defects other than foreign matter.

7.3.3.2 *Slip* — Determine by methods agreed upon between supplier and purchaser.

7.3.3.3 Automatic surface inspection technology is being developed to detect and discriminate surface defects. The extended definitions in Section 4.3 are intended to facilitate this development.

NOTE 10: For observation of gross slip, examination of the epitaxial layer under the illumination conditions specified in Section 12.2 of SEMI MF523 may suffice. For more demanding applications, it may be desirable to etch the surface in accordance with SEMI MF1726 prior to the visual inspection.

7.4 If substrates of different type and net carrier density than the product substrates are to be used for deposition control, their type, resistivity, and quantity per run or lot shall be agreed upon between supplier and purchaser.

Table 1 IC Epitaxial Wafers - Basic Surface Criteria

Item	*Characteristics*	*Maximum Acceptability Limits*	*Test Method*	*Notes and Reference Documents*
1	Stacking Faults	1 per cm^2	SEMI MF1726	1
2	Slip	None	SEMI MF523 or SEMI MF1726	1, 5, 6
3	Dislocations	None	SEMI MF1726	1
4	Total Localized Light Scatterers	2000 per m^2	≥ 0.5 μm LSE, based on calibration of surface scanning inspection systems with latex spheres, 90% capture rate	1, 7 Table 2
5	Haze	None	SEMI MF523 Section 12.2	4, 7
6	Scratches	None	SEMI MF523 Section 12.2	2, 7
7	Edge Chips	None	SEMI MF523 Section 12.2	
8	Foreign Matter	None	SEMI MF523 Section 12.3	4
9	Back Surface Contamination	None	SEMI MF523 Section 12.4	4

NOTE 1: Defect limits shall apply to quality area, which is defined as the entire wafer surface except a defined outer annulus of 4 mm and any area included in a window where there is a laser identification mark.

NOTE 2: The cumulative AQL for both front surface and back surface of wafer is 2.5.

NOTE 3: The cumulative AQL for both front surface and back surface of wafer is 1.0.

NOTE 4: Any adherent contaminants, such as stains, glovemarks, dirt, smudges, warps, and solvent residues. This characteristic does not include point defects. Any nonadherent contamination or particulate matter easily removed by industry-accepted cleaning techniques shall not constitute foreign matter or haze.

NOTE 5: Test method(s) to be agreed upon between supplier and purchaser.

NOTE 6: For observation of gross slip, examine the epitaxial layer under illumination conditions specified in Section 12.2 of SEMI MF523. For more demanding applications, it may be desirable to etch the surface in accordance with SEMI MF1726.

NOTE 7: In today's technology, it may be possible to do this inspection using automated laser scanning systems; however, a standard test procedure has yet to be developed. Application of automated inspection must be agreed upon between supplier and user.

8 Sampling

8.1 Unless otherwise specified, appropriate sample sizes shall be selected from each lot according to ANSI/ASQC Z1.4-1993. Quality characteristics shall be assigned an acceptable quality level (AQL) in accordance with ANSI/ASQC Z1.4-1993. Inspection levels shall be agreed upon between supplier and purchaser. Accept and reject criteria are to be based on defective wafers, not on defective characteristics.

8.2 Unless otherwise specified, the following AQL's shall be assigned:

8.2.1 Epitaxial Layer Center-point Thickness and Variation, 1%;

8.2.2 Epitaxial Layer Center Net Carrier Density and Variation, 1%;

8.2.3 Epitaxial Wafer Defects, Cumulative, 2.5%.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 The supplier and purchaser may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 7; however, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Packing and Marking

10.1 Special packing requirements shall be subject to agreement between the supplier and the purchaser. Otherwise all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices to provide protection against damage during shipment.

10.2 The wafers supplied under this specification shall be identified by appropriately labeling the outside of each box or container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include supplier's name and reference number, purchaser's p.o. number, quantity, dopant, orientation, conductivity type of substrates and epitaxial layers, carrier density, and thickness of the epitaxial layer. The reference number assigned by the supplier shall provide ready access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one year after that particular lot has been shipped.

11 Guides

11.1 The specifications in the epitaxial guides are examples which were formed by a consensus of viewpoints. They may or may not be used as a foundation to specify an epitaxial wafer for use in device manufacture. Their usefulness can be increased by considering the guides prior to developing a device design or process. The required specification is deter-mined by the device and the process design, the guides are suggestions from which a specification can evolve.

11.2 An epitaxial guide can be viewed as a generic epitaxial wafer specification or as an example of a specification. These tables provide common epitaxial wafer characteristics which describe starting wafers useful for the manufacture of some twin tub CMOS devices.

11.3 The guides in Tables 3, 4, 5, 6, 7, 8, 9, and 10 provide a series of options intended to increase the awareness of epitaxial specifications and to provide information from which a specification can be formulated.

11.4 SEMI M18 was used as a template for formulating these tables. When suitable to the application, the guides can be used intact, reducing the proliferation of specifications and formats.

11.4.1 Table 3 is representative of 1.0 µm design rule epitaxial wafer criteria.

11.4.2 Table 4 is typical of an epitaxial wafer criteria for custom twin tub CMOS, 0.35 µm design rule devices, such as, but not limited to ASIC's, FPGA's, linears, DSP's, and microprocessors.

11.4.3 Table 5 is typical of an epitaxial wafer criteria for 0.35 µm design rule devices such as 64 megabit DRAM's.

11.4.4 Table 6 is typical of epitaxial wafer criteria for twin tub CMOS, 0.25 µm design rule devices, such as, but not limited to ASIC's, FPGA's, linears, DSP's, and microprocessors.

11.4.5 Table 7 is typical of epitaxial wafer criteria for twin tub CMOS, 0.18 µm design rule devices.

11.4.6 Table 8 is typical of epitaxial wafer substrate criteria for a wafer pre-epitaxial that will be used in twin tub CMOS, 0.25 µm design rule devices.

11.4.7 Table 9 is typical of epi wafer criteria for twin tub CMOS, 0.13 µm design rule devices.

11.4.8 Table 10 is typical of epi wafer criteria that can be used to develop a wafer specification for 90 nm Design Rule CMOS devices.

Table 2 Equivalent Units for Localized Light Scatterers

Diameter[1]						
Density per m^2	*100*	*125*	*150*	*200*	*300*	*Density per cm^2*
	Localized Light Scatterers per Wafer					
100	1	1	2	3	7	0.01
200	1	2	3	6	13	0.02
300	2	3	5	9	20	0.03
400	3	4	6	12	27	0.04
500	3	5	8	14	33	0.05
600	4	6	10	17	40	0.06
700	5	8	11	20	47	0.07
800	5	9	13	23	54	0.08

Diameter[1]						
Density per m²	*100*	*125*	*150*	*200*	*300*	*Density per cm²*
	Localized Light Scatterers per Wafer					
900	6	10	14	26	60	0.09
1000	7	11	16	29	67	0.10
1100	7	12	17	32	74	0.11
1200	8	13	19	35	80	0.12
1300	9	14	21	38	87	0.13
1400	9	15	22	41	94	0.14
1500	10	16	24	43	100	0.15
1600	11	17	25	46	107	0.16
1700	11	18	27	49	114	0.17
1800	12	19	29	52	121	0.18
1900	13	20	30	55	127	0.19
2000	13	22	32	58	134	0.20
2100	14	23	33	61	141	0.21
2200	15	24	35	64	147	0.22
2300	15	25	36	67	154	0.23
2400	16	26	38	69	161	0.24
2500	17	27	40	72	167	0.25
2600	17	28	41	75	174	0.26
2700	18	29	43	78	181	0.27
2800	19	30	44	81	188	0.28
2900	19	31	46	84	194	0.29
3000	20	32	48	87	201	0.30
3100	21	33	49	90	208	0.31
3200	21	34	51	93	214	0.32
3300	22	35	52	96	221	0.33
3400	23	37	54	98	228	0.34
3500	23	38	55	101	234	0.35
3600	24	39	57	104	241	0.36
3700	25	40	59	107	248	0.37
3800	25	41	60	110	254	0.38
3900	26	42	62	113	261	0.39
4000	27	43	63	116	268	0.40
4100	27	44	65	119	275	0.41
4200	28	45	67	122	281	0.42
4300	29	46	68	124	288	0.43
4400	29	47	70	127	295	0.44
4500	30	48	71	130	301	0.45
4600	31	49	73	133	308	0.46
4700	31	51	74	136	315	0.47
4800	32	52	76	139	321	0.48
4900	33	53	78	142	328	0.49
5000	33	54	79	145	335	0.50

Table 3 Guide for Specification of 1.0 µm Design Rule, Twin-Tub CMOS, Epitaxial Wafers

CUSTOMER:		*PART NUMBER:* *REVISION:*	*DATE:*			
M18 ITEM #		*SPECIFICATION*	*TESTING LEVEL*			
			WAFER		*TEST PIECE*	
			100%	*SAMPLE*	*100%*	*SAMPLE*
11. GENERAL EPITAXIAL WAFER AND LAYER CHARACTERISTICS						
11.1	Conductivity Type/ Structure	*p/p+*				
11.2	Primary Dopant	Boron				
11.3	Silicon Source Gas	Fixed				
11.4	Reactor Type	Fixed				
11.5	Carrier Density (Center)	$2.00 \pm 1.0 \times 10^{15}$				
	Units	carriers per cm^3				
	Test Method	Mercury Probe SEMI MF1392				
11.6	Carrier Density Variation	10% max per SEMI M11				
11.7	Thickness (Center)	Target ± 10%				
11.8	Thickness Variation	10% per SEMI M11				
11.11	Phantom Layer	none				
12. MECHANICAL CHARACTERISTICS: POST EPI						
12.5	Flatness/Site	95% of the 18 mm × 18 mm sites ≤ 0.5 µm (SFQD) includes partial sites				
13. FRONT SURFACE CHARACTERISTICS						
13.1	Stacking Faults	1 per cm^2 maximum				
13.2	Slip/Dislocations	none per SEMI MF1726				
13.14	Localized Light Scatterers	2000 per m^2 max. ≥ 0.5 µm LSE, based on calibration of surface scanning inspection systems with latex spheres, 90% capture rate				
13.5	Scratches	none per SEMI MF523, Section 12.2				
13.6	Dimples	none per SEMI MF523, Section 12.3				
13.7	Orange Peel	none per SEMI MF523, Section 12.3				
13.8	Cracks/Fractures	none per SEMI MF523, Section 12.3				
13.9	Crow's Feet	none per SEMI MF523, Section 12.3				
13.10	Edge Chips	none per SEMI MF 523, Section 12.3				
13.12	Haze	none per SEMI MF523, Section 12.2				
12.13	Foreign Matter	none per SEMI MF523, Section 12.3				
13.15	Nominal Edge Exclusion	4 mm				
	Surface Metals	≤ 1×10^{12} per cm^2 for Zn, Al, Ni ≤ 2×10^{11} per cm^2 for each element: Na, Cr, K, Fe, Cu				
14. BACK SURFACE CHARACTERISTICS						
14.1	Contamination	none per SEMI MF523, Section 12.4				
15. OTHER CHARACTERISTICS - POLISHED WAFER: EPITAXIAL SUBSTRATE — MEETS SEMI M1						
15.1	Resistivity	0.005–0.020 Ω·cm				
15.2	Back Seal	polysilicon [ ], silicon oxide [ ], silicon nitride [ ], combination and thickness as required, none [ ]				
15.3	Nominal Diameter	125 mm [ ], 150 mm [ ], 200 mm [ ], 300 mm [ ]				

Table 4 Guide for the Specification of 0.35 µm Design Rule, Twin-Tub CMOS, Epitaxial Wafers

CUSTOMER:		*PART NUMBER:* *REVISION:*	*DATE:*			
M18 ITEM #		*SPECIFICATION*	*TESTING LEVEL*			
			WAFER		*TEST PIECE*	
			100%	*SAMPLE*	*100%*	*SAMPLE*
11. GENERAL EPITAXIAL WAFER AND LAYER CHARACTERISTICS						
11.1	Conductivity Type/ Structure	*p/p+*				
11.2	Primary Dopant	Boron				
11.3	Silicon Source Gas	Fixed				
11.4	Reactor Type	Fixed				
11.5	Net Carrier Density (Center)	$2.00 \pm 0.5 \times 10^{15}$				
	Units	carriers per cm^3				
	Test Method	Mercury Probe SEMI MF1392 or SEMI MF1393				
11.6	Net Carrier DensityVariation	10% max per SEMI M11				
11.7	Thickness (Center)	Target ± 5% (1σ)				
11.8	Thickness Variation	10% per SEMI M11				
11.11	Phantom Layer	none				
12. MECHANICAL CHARACTERISTICS: POST EPI						
12.5	Flatness/Site	95% of the 22 mm × 22 mm ≤ 0.23 um (SFQD) includes partial sites				
13. FRONT SURFACE CHARACTERISTICS						
13.1	Stacking Faults	0.1 per cm^2 maximum				
13.2	Slip/Dislocations	none per SEMI MF1726				
13.5	Scratches	none per SEMI MF523, Section 12.2				
13.6	Dimples	none per SEMI MF523, Section 12.3				
13.7	Orange Peel	none per SEMI MF523, Section 12.3				
13.8	Cracks/Fractures	none per SEMI MF523, Section 12.3				
13.9	Crow's Feet	none per SEMI MF523, Section 12.3				
13.10	Edge Chips	none per SEMI MF523, Section 12.3				
13.12	Haze	none per SEMI MF523, Section 12.2				
13.13	Foreign Matter	none per SEMI MF523, Section 12.3				
TBD	Localized Light Scatterers	2000 per m^2 max. ≥ 0.2 µm size, based on calibration of surface scanning inspection systems with latex spheres, 90% capture rate				
13.15	Nominal Edge Exclusion	4 mm for all front surface characteristics except cracks/fractures, edge chips, crow's feet, and foreign matter				
7.1	Surface Metals	$\leq 1 \times 10^{11}$ atoms per cm^2 for each element: Na, Al, Cr, K, Fe, Ni, Cu, Zn				
14. BACK SURFACE CHARACTERISTICS						
14.1	Contamination	none per SEMI MF523, Section 13.4				
TBD	Back Seal	user specified				
15. OTHER CHARACTERISTICS: POLISHED WAFER-EPITAXIAL SUBSTRATE — MUST MEET SEMI M1 EXCEPT AS NOTED						
2.1	Resistivity	0.005–0.010 Ω·cm				
TBD	Bulk Micro Defects	user specified				

CUSTOMER:		PART NUMBER: REVISION:	DATE:			
M18 ITEM #		SPECIFICATION	TESTING LEVEL			
			WAFER		TEST PIECE	
			100%	SAMPLE	100%	SAMPLE
TBD	Denuded Zone	user specified				
TBD	Back Seal	polysilicon [ ], silicon oxide [ ], silicon nitride [ ], combination and thickness as required, none [ ]				
6.1	Diameter	125 mm [ ], 150 mm [ ], 200 mm [ ], 300 mm [ ]				

Table 5 Guide for the Specification of 0.35 μm Design Rule Epitaxial Wafers for DRAM Applications

CUSTOMER:		PART NUMBER: REVISION:	DATE:			
M18 ITEM #		SPECIFICATION	TESTING LEVEL			
			WAFER		TEST PIECE	
			100%	SAMPLE	100%	SAMPLE
11. GENERAL EPITAXIAL WAFER AND LAYER CHARACTERISTICS						
11.1	Conductivity Type/ Structure	*p/p+*				
11.2	Primary Dopant	Boron				
11.3	Silicon Source Gas	not specified				
11.4	Growth Method	not specified				
11.5	Net Carrier Density(Center)	Target must be $\geq 1.34 \times 10^{15}$ Tolerance ± 25% of target				
	Units	Carriers per cm^3				
	Test Method	SEMI MF1392 or SEMI MF1393				
11.6	Net Carrier DensityVariation	± 20% per SEMI M11				
11.7	Thickness (Center)	Target must be ≤ 5 μm, Tolerance ± 5 % (1σ) or target				
11.8	Thickness Variation	10% per SEMI M11				
11.9	Transition Width	user specified				
11.11	Phantom Layer	none				
6. MECHANICAL CHARACTERISTICS: PRE EPI						
6.11	Warp	user specified				
6.13	Global Flatness	3 μm max. (GFLR)				
6.8	Total Thickness Variation (TTV)	5 μm max. (GBIR)				
6.14	Flatness/Site	95% of the 22 mm × 22 mm sites ≤ 0.35 μm (SFQD), partial sites not included, substrate form				
13. FRONT SURFACE CHARACTERISTICS						
13.1	Stacking Faults	0.1 per cm^2 maximum				
13.2	Slip/Dislocations	total length ≤ diameter/2 per SEMI MF1726				
13.10	Edge Chips	none per SEMI MF523, Section 12.3				
13.14	Localized Light Scatters including haze, stacking faults and scratches	2000 per m^2 max. ≥ 0.16 μm size, based on calibration of surface scanning inspection systems with latex spheres, 90% capture rate				
13.15	Nominal Edge Exclusion	4 mm for all front surface characteristics except cracks/fractures, edge chips, crow's feet, and foreign matter				

CUSTOMER:		PART NUMBER: REVISION:		DATE:			
M18 ITEM #		SPECIFICATION		TESTING LEVEL			
				WAFER		TEST PIECE	
				100%	SAMPLE	100%	SAMPLE
7.1	Surface Metals	$\leq 1 \times 10^{11}$ atoms per cm^2 for each element: Na, Al, Cr, K, Fe, Ni, Cu, Zn					
14. BACK SURFACE CHARACTERISTICS							
14.1	Contamination	none per SEMI MF523, Section 12.4					
14.2	Back Seal	Silicon Oxide [ ], None [ ]					
15. OTHER CHARACTERISTICS: POLISHED WAFER, EPITAXIAL - SUBSTRATE - MUST MEET SEMI M1 EXCEPT AS NOTED							
2.1	Resistivity	0.005–0.010 Ω·cm or 0.010–0.020 Ω·cm					
		Substrate Resistivity	Backseal Required				
		0.005–0.010 Ω·cm	yes				
		0.010–0.020 Ω·cm	user specified				
TBD	Bulk Micro Defects	user-specified					
TBD	Denuded Zone	user-specified					
6.1	Nominal Diameter	200 mm only					
6.3	Primary Flat/Notch	Notch Only					
TBD	Extrinsic Getter	user-specified					
5.1	Laser Mark Identification	SEMI M13					
3.1	Oxygen Concentration	$\leq 1.5 \times 10^{18}$ atoms/cm^3 (per in-process monitoring only) correlated to SEMI MF121-79 equivalent					
TBD	Inspection Sheet	Certificate required in a standard format to be determined					

NOTE 1: TBD - Number to be determined by M18 Task Force, which will also develop EDI coding.

Table 6 Guide for the Specification of 0.25 Micron Design Rule, Twin-Tub CMOS, Epitaxial Wafers

CUSTOMER:		PART NUMBER: REVISION:	DATE:			
M18 ITEM #		SPECIFICATION	TESTING LEVEL			
			WAFER		TEST PIECE	
			100%	SAMPLE	100%	SAMPLE
11. GENERAL EPITAXIAL WAFER AND LAYER CHARACTERISTICS						
11.1	Conductivity Type/ Structure	*p/p+*				
11.2	Primary Dopant	Boron				
11.3	Silicon Source Gas	fixed by agreement				
11.4	Reactor Type	fixed by agreement				
11.5	Net Carrier Density (Center)	2.00×10^{15} target ± 25% (2σ) tolerance 1.34×10^{15} minimum				
	Units	carriers per cm^3				
	Test Method	Mercury Probe SEMI MF1392 or SEMI MF1393				
11.6	Net Carrier DensityVariation	10% maximum per SEMI M11				

CUSTOMER:		PART NUMBER: REVISION:	DATE:			
M18 ITEM #		SPECIFICATION	TESTING LEVEL			
			WAFER		TEST PIECE	
			100%	SAMPLE	100%	SAMPLE
11.7	Thickness (Center)	target by agreement within 2–5 μm range ± 5% (1σ) tolerance				
11.8	Thickness Variation	10% per SEMI M11				
11.11	Phantom Layer	none				
12. MECHANICAL CHARACTERISTICS: POST EPI						
12.5	Flatness/Site	≤ 0.25 um (SFQR), site size 22 mm × 22 mm including partial sites, PUA to be negotiated (See NOTE 1.)				
13. FRONT SURFACE CHARACTERISTICS						
13.1	Stacking Faults	0.03/cm^2 maximum (See NOTE 2.)				
13.2	Slip/Dislocations	none per SEMI MF1726, slip with a depth < 0.1 μm acceptable				
13.5	Scratches	none per SEMI MF523, Section 12.2				
13.6	Dimples	none per SEMI MF523, Section 12.3				
13.7	Orange Peel	none per SEMI MF523, Section 12.3				
13.8	Cracks/Fractures	none per SEMI MF523, Section 12.3				
13.9	Crow's Feet	none per SEMI MF523, Section 12.3				
13.10	Edge Chips	none per SEMI MF523, Section 12.3				
13.12	Haze	none per SEMI MF523, Section 12.2				
13.13	Foreign Matter	none per SEMI MF523, Section 12.3				
TBD	Localized Light Scatterers	0.36 per cm^2 maximum ≥ 0.16 μm LSE (See NOTE 3.)				
		calibrate using SEMI M53				
13.15	Nominal Edge Exclusion	4 mm for all front surface characteristics except cracks/fractures, edge chips, crow's feet, and foreign matter.				
7.1	Surface Metals	≤ 5 × 10^{10} atoms per cm^2 for each of the following elements: Ca, Cr, Co, Cu, Fe, K, Mn, Mo, Na, Ni, Ti.				
		≤ 1 × 10^{11} atoms per cm^2 for each of the following elements: Al, V, Zn.				
14. BACK SURFACE CHARACTERISTICS						
14.1	Contamination	none per SEMI MF523, Section 13.4				
TBD	Back Seal	user specified				
15. OTHER CHARACTERISTICS: POLISHED WAFER-EPITAXIAL SUBSTRATE – MUST MEET SEMI M1 (except when noted)						
2.1	Resistivity	0.005–0.010 Ω·cm [ ], 0.010–0.020 Ω·cm [ ]				
TBD	Bulk Micro Defects	by agreement				
TBD	Denuded Zone	by agreement				
TBD	Back Seal	polysilicon [ ], silicon oxide [ ], combinations and thickness by agreement, none [ ]				
6.1	Diameter	125 mm [ ], 150 mm [ ], 200 mm [ ], 300 mm [ ]				

NOTE 1: Based on 1997 process capability. PUA is estimated to be 90%.

NOTE 2: Based on 1997 process capability.

NOTE 3: This requirement is mathematically consistent with the SIA Roadmap value of 0.6 per cm^2 maximum ≥ 0.12 μm LSE. The SIA Roadmap value was transformed using draft international standard ISO/DIS 14644-1 which follows the equation: 0.36 per cm^2 = 0.60 per cm^2 /(0.16 μm /0.125 μm)$^{2.1}$.

NOTE 4: TBD — Number to be determined by M-18 Task Force which will also develop EDI coding.

Table 7 Guide For The Specification Of 0.18 Micron Design Rule

ITEM		*p/p^- EPITAXIAL CIRCUIT WAFER (DRAM)*	*p/p^+ EPITAXIAL CIRCUIT WAFER (Logic/DRAM)*	*p/p^{++} EPIAXIAL CIRCUIT WAFER (Logic)*
1.0 GENERAL CHARACTERISTICS				
1.1	Growth Method	Cz or MCz *	Cz or MCz *	Cz or MCz *
1.2	Crystal Orientation/Tolerance	{100} ± 1°	{100} ± 1°	{100} ± 1°
1.3	Conductivity Type	p/p^-	p/p^+	p/p^{++}
1.4	Dopant	Boron	Boron	Boron
1.5	Nominal Edge Exclusion	3 mm	3 mm	3 mm
2.0 ELECTRICAL CHARACTERISTICS				
2.1.1	Resistivity (Center Point)	0.8–15 Ω·cm* (match epi layer)	0.01–0.02 Ω·cm*	0.005–0.010 Ω·cm*
2.1.2	Resistivity (Tolerance)	(see row 2.1.1)	(see row 2.1.1)	(see row 2.1.1)
2.2	Radial Resistivity Variation (RRG)	< 20% *	< 20% *	< 20% *
2.3	Resistivity Striations	NS * (See Note 2.)	NS * (See Note 2.)	NS * (See Note 2.)
2.4	Minority Carrier Recombination Lifetime	NS * (See Note 2.)	NS * (See Note 2.)	NS * (See Note 2.)
3.0 CHEMICAL CHARACTERISTICS				
3.1.1	Oxygen Concentration (Nominal)	user/supplier	user/supplier	user/supplier
3.1.2	Oxygen Concentration (Tolerance: within shipment variation)	± 1.5 ppma *	± 2.0 ppma * (See Note 3.)	± 2.0 ppma * (See Note 3.)
3.2	Radial Oxygen Variation	≤ 10% * 10 mm from Edge	≤ 10% * 10 mm from Edge	≤ 10% * 10 mm from Edge
3.3	Carbon Concentration	≤ 0.5 ppma *	See Note 3	See Note 3
4.0 STRUCTURAL CHARACTERISTICS				
4.1	Dislocation Etch Pit Density	NS (See Note 2.)	NS (See Note 2.)	NS (See Note 2.)
4.2	Slip	none	none	none
4.3	Lineage	none	none	none
4.4	Twin	none	none	none
4.5	Swirl	none	none	none
4.6	Shallow Pits	none	none	none
4.7	Oxidation-Induced Stacking Faults (OSF)	NS * (See Note 2.)	NS * (See Note 2.)	NS * (See Note 2.)
4.8	Oxide Precipitates (BMD) O_i Reduction (ΔO_i)	user/supplier	user/supplier	user/supplier
5.0 WAFER PREPARATION CHARACTERISTICS				
5.1	Wafer ID Marking	Per SEMI M1	Per SEMI M1	Per SEMI M1
5.2	Front Surface Thin Film(s)			
5.3	Denuded Zone	user/supplier	user/supplier	user/supplier
5.4	Extrinsic Gettering Treatment	user/supplier	user/supplier	user/supplier
5.5	Backseal	none	None or as user/ supplier agreement	None or as user/ supplier agreement
5.6	Annealing	None or as user/ supplier agreement	None or as user/ supplier agreement	None or as user/ supplier agreement
6.0 MECHANICAL CHARACTERISTICS				
6.1	Diameter	300 ± 0.2 mm or 200 ± 0.2 mm	300 ± 0.2 mm or 200 ± 0.2 mm	300 ± 0.2 mm or 200 ± 0.2 mm
6.2	Diameter Notch Dimensions	Per SEMI M1	Per SEMI M1	Per SEMI M1
6.2.1	Notch Depth	1 + 0.25, -0.00 mm	1 + 0.25, -0.00 mm	1 + 0.25, -0.00 mm

ITEM		*p/p⁻ EPITAXIAL CIRCUIT WAFER (DRAM)*	*p/p⁺ EPITAXIAL CIRCUIT WAFER (Logic/DRAM)*	*p/p⁺⁺ EPIAXIAL CIRCUIT WAFER (Logic)*
6.2.2	Notch Angle	90 +5, -1 degrees	90 +5, -1 degrees	90 +5, -1 degrees
6.3	Notch Orientation	<110> ± 1°	<110> ± 1°	<110> ± 1°
6.6	Edge Profile*	Per SEMI M1	Per SEMI M1	Per SEMI M1
6.6.1	Edge Surface Finish	Polished *	Polished *	Polished *
6.7	Thickness	300 mm per SEMI M1	300 mm per SEMI M1	300 mm per SEMI M1
6.7.1	Thickness Variation (9-Point TTV)	NS (See Note 2.)	NS (See Note 2.)	NS (See Note 2.)
6.7.2	Thickness Variation (GBIR)	≤ 3 µm	≤ 3 µm	≤ 3 µm
6.10	Bow	NS (See Note 2.)	NS (See Note 2.)	NS (See Note 2.)
6.11	Warp (only process control data required)	≤ 50 µm	≤ 50 µm for wafers without backseal ≤ 100 µm for wafers with backseal	≤ 50 µm for wafers without backseal ≤ 100 µm for wafers with backseal
6.12	Sori	NS (See Note 2.)	NS (See Note 2.)	NS (See Note 2.)
6.13	Flatness/Global	NS (See Note 2.)	NS (See Note 2.)	NS (See Note 2.)
6.14 B	Flatness/Site (See NOTE 4)	SFSR ≤ 0.18 µm	SFSR ≤ 0.18 µm	SFSR ≤ 0.18 µm
7.0 FRONT SURFACE CHEMISTRY				
7.1	Surface Metal Contamination			
	Sodium	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Aluminum	$\leq 1 \times 10^{11}/cm^2$	$\leq 1 \times 10^{11}/cm^2$	$\leq 1 \times 10^{11}/cm^2$
	Potassium	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Chromium	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Iron	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Nickel	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Copper	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Zinc	$\leq 1 \times 10^{11}/cm^2$	$\leq 1 \times 10^{11}/cm^2$	$\leq 1 \times 10^{11}/cm^2$
	Calcium	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
8.0 FRONT SURFACE CRITERIA				
8.1A	Scratches (macro)	none	none	none
8.1B	Scratches (micro)	≤ 10 mm (total length)	≤ 10 mm (total length)	≤ 10 mm (total length)
8.3	Localized Light Scatterers – Only particles for epitaxial wafers – Sizes are PSL equivalents	≤ 60 @ ≥ 0.09 µm (300 mm) ≤ 27 @ ≥ 0.09 µm (200 mm) or (See NOTE 5) ≤ 34 @ ≥ 0.12 µm (300 mm) ≤ 15 @ ≥ 0.12 µm (200 mm)	≤ 60 @ ≥ 0.09 µm (300 mm) ≤ 27 @ ≥ 0.09 µm (200 mm) or (See NOTE 5) ≤ 34 @ ≥ 0.12 µm (300 mm) ≤ 15 @ ≥ 0.12 µm (200 mm)	≤ 60 @ ≥ 0.09 µm (300 mm) ≤ 27 @ ≥ 0.09 µm (200 mm) or (See NOTE 5) ≤ 34 @ ≥ 0.12 µm (300 mm) ≤ 15 @ ≥ 0.12 µm (200 mm)
8.4	Edge Chips	none	none	none
8.5-8.16	OTHER	none	none	none
9.0 BACK SURFACE CRITERIA				
9.1	Edge Chips	none	none	none

	ITEM	*p/p^- EPITAXIAL CIRCUIT WAFER (DRAM)*	*p/p^+ EPITAXIAL CIRCUIT WAFER (Logic/DRAM)*	*p/p^{++} EPIAXIAL CIRCUIT WAFER (Logic)*
9.2-9.5	OTHER	none	none	none
9.6	Roughness	NS (See Note 2.)	NS (See Note 2.)	NS (See Note 2.)
9.7	Brightness (Gloss) 60° angle of incidence, referenced to a mirror polished wafer. NOTE: Double-side polish process preferred	≥ 80%	≥ 80% Applies to wafers without backseal only.	≥ 80% Applies to wafers without backseal only.
9.X	Localized Light Scatterers (See Note 6)	NS (See Note 2.)	NS (See Note 2.)	NS (See Note 2.)
9.YA	Scratches (Macro)	none	none	none
9.YB	Scratches (Micro)	≤ 25 mm (total length)	≤ 25 mm (total length)	≤ 25 mm (total length)
11.0 ADDITIONAL EPITAXIAL LAYER CHARACTERISTICS				
11.1	Conductivity Type/Structure	*p/p^-*	*p/p^+*	*p/p^{++}*
11.2	Primary Dopant	Boron	Boron	Boron
11.3	Silicon Source Gas	NS (See Note 2.)	NS (See Note 2.)	NS (See Note 2.)
11.4	Epitaxial Growth Method	NS (See Note 2.) (see Item 5.3)	NS (See Note 2.) (see Item 5.3)	NS (See Note 2.) (see Item 5.3)
11.5	Net Carrier Density Target Variation (Center of wafer)	user/supplier	user/supplier	user/supplier
11.6	Net Carrier Density Variation	± 5%	± 5% with backseal ± 10% without backseal	± 5% with backseal ± 10% without backseal
11.7	Thickness Target Variation	± 5%	± 5%	± 5%
11.8	Thickness Variation	± 10%	± 10%	± 10%
11.9	Transition Width	user/supplier	user/supplier	user/supplier
11.X	Layer Flat Zone	user/supplier	user/supplier	user/supplier
13.1	Stacking Faults (See Note 7)	< 2 per wafer	< 2 per wafer	< 2 per wafer
13.2	Slip/Dislocations (See Note 8)	none	none	none
13.5-13.13	OTHER	(see Item 13.1)	(see Item 13.1)	(see Item 13.1)

NOTE 1: * indicates substrate specification.

NOTE 2: NS is the abbreviation for Not Specified.

NOTE 3: Practical non-destructive metrology did not exist at the time this document was approved.

NOTE 4: The site size is 32 mm × 25 mm. Partial sites are included. The metrology was being developed at the time this document was being balloted.

NOTE 5: These values are mathematically consistent. The 0.09 μm count limit was transformed using draft international standard: ISO/DIS 14644-1 which follows the equation: 34 counts per wafer = 60 counts per wafer /(0.12 μm/ 0.09 μm)2.

NOTE 6: The process control capability is expected to be: ≤ 500 @ ≥ 0.25 μm.

NOTE 7: The lot average density is < 0.0029/cm2.

NOTE 8: Tested per SEMI MF1726; a depth < 100 nm is acceptable.

Table 8 Guide for the Specification of Polished Wafer, P+ Substrate for 0.25 μm Design Rule Epitaxial

CUSTOMER			*PART NUMBER:* *REVISION*		*DATE:*			
REQ.	*M18 ITEM #*		*SPECIFICATION*		*TESTING LEVEL*			
					WAFER		*TEST PIECE*	
					100%	*SAMPLE*	*100%*	*SAMPLE*
POLISHED WAFER, EPITAXIAL SUBSTRATE - MUST MEET SEMI M1								
	15.1	Resistivity	0.005-0.010 Ω·cm or 0.010-0.020 Ω·cm					
			Substrate Resistivity	**Backseal Required**				
			0.005–0.010 Ω·cm	yes				
			0.010–0.020 Ω·cm	user specified				
	15.2	Bulk Micro Defects	user specified					
		Dopant	Boron					
	15.4	Nominal Diameter	150 mm [ ] 200 mm [ ]					
	15.5	Primary Flat/ Notch	User specified per SEMI M1					
	15.6	Extrinsic Getter	User specified					
		Intrinsic Getter	User specified					
	15.7	Laser Mark Identification	SEMI M13 [ ] SEMI M12 [ ] SEMI T1 [ ]					
	15.8	Oxygen Concentration	maximum 30 ppma, Old ASTM					
		Inspection Sheet	Certificate required in a standard format to be determined.					
		SQC Data Sheet	SQC required in a standard format to be determined.					
12. MECHANICAL CHARACTERISTICS: PRE EPITAXIAL								
		Total Thickness Variation (TTV)	5 μm (GBIR)					
	12.5	Flatness/Site	≤ 0.25 μm (SFQR), site size 22 mm × 22 mm including partial sites, PUA to be negotiated					
13. FRONT SURFACE CHARACTERISTICS								
	13.2	Slip/Dislocations	none					
	13.10	Edge Chips	none per SEMI MF523, Section 12.3					
	13.14	Localized Light Scatterers and	0.23 per cm^2 maximum ≥ 0.12 μm LSE and 0.0 per cm^2 ≥ 1 μm LSE, calibrate using SEMI M53					
		Scratches	none					
	13.15	Nominal Edge Exclusion	3 mm for all front surface characteristics except cracks/fractures, edge chips, crow's feet, and foreign matter					
		Surface Metals	≤ 1×10^{11} atoms per cm^2 for each element: Na, Al, Cr, K , Fe, Ni, Cu, Zn					
14. BACK SURFACE CHARACTERISTICS								
	14.1	Contamination	none per SEMI MF523, Section 12.4					

CUSTOMER			*PART NUMBER:* *REVISION*	*DATE:*
	14.2	Back Seal	[ ] Silicon Oxide: 5000 ± 1000 Angstroms, [ ] Polysilicon: 10,000 ± 2000 Angstroms, [ ] Backside Damage, [ ] None, [ ] Combination of: 3000 ± 1000 Angstroms Silicon Oxide on top of 8000 ± 2000 Angstroms Polysilicon	

Table 9 Guide For The Specification Of 0.13 Micron Design Rule Silicon Epitaxial Wafers

ITEM		*p/p⁻ EPITAXIAL CIRCUIT WAFER (DRAM)*	*p/p⁺ EPITAXIAL CIRCUIT WAFER (Logic/DRAM)*	*p/p⁺⁺ EPITAXIAL CIRCUIT WAFER (Logic)*
1.0 GENERAL CHARACTERISTICS				
1.1	Growth Method	Cz or MCz *	Cz or MCz *	Cz or MCz *
1.2	Crystal Orientation	{100}	{100}	{100}
1.3	Crystal Orientation/Tolerance	± 1°	± 1°	± 1°
1.4	Conductivity type	*p/p-*	*p/p+*	*p/p++*
1.5	Dopant	Boron	Boron	Boron
1.6	Nominal Edge Exclusion	3 mm	3 mm	3 mm
2.0 ELECTRICAL CHARACTERISTICS				
2.1.1	Resistivity (Center Point)	0.8–15 Ω·cm *	0.01–0.02 Ω·cm *	0.005–0.010 Ω·cm *
2.2	Radial Resistivity Variation (See Note 9.)	< 20% *	< 20% *	< 20% *
2.3	Resistivity Striations	NS *	NS *	NS *
3.0 CHEMICAL CHARACTERISTICS				
3.1.1	Nominal Oxygen Concentration (Center)	user/supplier	user/supplier	user/supplier
3.1.2	Oxygen Concentration Tolerance Per old ASTM calibration factor (See SEMI M44.)	± 2.0 ppma *	± 2.0 ppma * (See Note 3.)	± 2.0 ppma * (See Note 3.)
3.2	Radial Oxygen Variation Per SEMI MF951	≤ 10% * 10 mm from Edge	≤ 10% * 10 mm from Edge (See Note 3.)	≤ 10% * 10 mm from Edge (See Note 3.)
3.3	Carbon Concentration (See Note 9.)	≤ 0.5 ppma *	≤ 0.5 ppma (See Note 3.) *	≤ 0.5 ppma (See Note 3.) *
4.0 STRUCTURAL CHARACTERISTICS				
4.1	Dislocation Etch Pit Density	NS	NS	NS
4.2	Slip	none	none	none
4.3	Lineage	none	none	none
4.4	Twin	none	none	none
4.5	Swirl	none	none	none
4.6	Shallow pits	none	none	none
4.7	Oxidation-Induced Stacking Faults (OSF)	NS *	NS *	NS *
4.8	Oxide Precipitates (BMD) O_i Reduction (ΔO_i)	user/supplier	user/supplier	user/supplier
5.0 WAFER PREPARATION CHARACTERISTICS				
5.1	Wafer ID Marking	per M1	per M1	per M1
5.2	Front Surface Thin Film(s)	NS	NS	NS
5.3	Denuded Zone	user/supplier	user/supplier	user/supplier

ITEM		*p/p⁻ EPITAXIAL CIRCUIT WAFER (DRAM)*	*p/p⁺ EPITAXIAL CIRCUIT WAFER (Logic/DRAM)*	*p/p⁺⁺ EPITAXIAL CIRCUIT WAFER (Logic)*
5.4	Extrinsic Gettering Treatment	user/supplier	user/supplier	user/supplier
5.5	Backseal	none	None or as user/supplier agreement	None or as user/supplier agreement
5.6	Annealing	None or as user/supplier agreement	None or as user/supplier agreement	None or as user/supplier agreement
6.0 MECHANICAL CHARACTERISTICS				
6.1	Diameter	300 ± 0.2 mm or 200 ± 0.2 mm	300 ± 0.2 mm or 200 ± 0.2 mm	300 ± 0.2 mm or 200 ± 0.2 mm
6.2	Diameter Notch Dimensions			
6.2.1	Notch Depth	1 +0.25,-0.00 mm	1 +0.25,-0.00 mm	1 +0.25,-0.00 mm
6.2.2	Notch Angle	90 +5,-1 degrees	90 +5,-1 degrees	90 +5,-1 degrees
6.3	Notch Orientation	<110> ± 1°	<110> ± 1°	<110> ± 1°
6.61	Edge Profile*	per SEMI M1	per SEMI M1	per SEMI M1
6.6.2	Edge Surface Finish	Polished *	Polished *	Polished *
6.7	Thickness	775 ± 25 µm* [300 mm diameter] or 725 ± 20 µm* [200 mm diameter]	775 ± 25 µm* [300 mm diameter] or 725 ± 20 µm* [200 mm diameter]	775 ± 25 µm* [300 mm diameter] or 725 ± 20 µm* [200 mm diameter]
6.7.1	Thickness Variation (9-Point TTV)	NS	NS	NS
6.72	Thickness Variation (GBIR)	≤ 3 µm	≤ 3 µm	≤ 3 µm
6.9	Surface Orientation	100	100	100
6.10	Bow	NS	NS	NS
6.11	Warp (only process control data required)	≤ 50 µm	≤ 50 µm for wafers without backseal ≤ 100 µm for wafers with backseal	≤ 50 µm for wafers without backseal ≤ 100 µm for wafers with backseal
6.12	Sori	NS	NS	NS
6.13	Flatness/Global	NS	NS	NS
6.14B	Flatness/Site (See Note 4)	SFSR ≤ 0.13 µm	SFSR ≤ 0.13 µm	SFSR ≤ 0.13 µm
7.0 FRONT SURFACE CHEMISTRY				
7.1	Surface Metal Contamination See Note 9			
	Sodium	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Aluminum	$\leq 1 \times 10^{11}/cm^2$	$\leq 1 \times 10^{11}/cm^2$	$\leq 1 \times 10^{11}/cm^2$
	Potassium	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Chromium	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Iron	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Nickel	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Copper	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
	Zinc	$\leq 1 \times 10^{11}/cm^2$	$\leq 1 \times 10^{11}/cm^2$	$\leq 1 \times 10^{11}/cm^2$
	Calcium	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$	$\leq 1.3 \times 10^{10}/cm^2$
8.0 FRONT SURFACE CRITERIA				
8.1A	Scratches (macro)	none	none	none
8.1B	Scratches (micro)	≤ 10 mm (total length)	≤ 10 mm (total length)	≤ 10 mm (total length)

ITEM		*p/p⁻ EPITAXIAL CIRCUIT WAFER (DRAM)*	*p/p⁺ EPITAXIAL CIRCUIT WAFER (Logic/DRAM)*	*p/p⁺⁺ EPITAXIAL CIRCUIT WAFER (Logic)*
8.3	Localized Light Scatterers - Only particles for epitaxial wafers - Sizes are PSL equivalents	300 mm: ≤ 200 @ ≥ 0.09 µm or ≤ 112 @ ≥ 0.12 µm (See note 5.)	300 mm: ≤ 200 @ ≥ 0.09 µm or ≤ 112 @ ≥ 0.12 µm (See note 5.)	300 mm: ≤ 200 @ ≥ 0.09 µm or ≤ 112 @ ≥ 0.12 µm (See note 5.)
		200 mm: ≤ 89 @ ≥ 0.09 µm or ≤ 50 @ ≥ 0.12 µm (See note 5.)	200 mm: ≤ 89 @ ≥ 0.09 µm or ≤ 50 @ ≥ 0.12 µm (See note 5.)	200 mm: ≤ 89 @ ≥ 0.09 µm or ≤ 50 @ ≥ 0.12 µm (See note 5.)
8.4	Edge Chips	none	none	none
8.5-8.16	OTHER	none	none	none
9.0 BACK SURFACE CRITERIA				
9.1	Edge Chips	none	none	none
9.2-9.5	OTHER	none	none	none
9.6	Roughness	NS	NS	NS
9.7	Brightness (Gloss) 60° angle of incidence, referenced to a mirror polished wafer. NOTE: Double-side polish process preferred	≥ 80%.	≥ 80% Applies to wafers without backseal only.	≥ 80% Applies to wafers without backseal only.
TBD	Localized Light Scatterers (See Note 6.)	NS	NS	NS
TBD	Scratches (Macro)	none	none	none
TBD	Scratches (Micro)	Cumulative Length ≤ 10% of the Wafer Diameter	Cumulative Length ≤ 10% of the Wafer Diameter	Cumulative Length ≤ 10% of the Wafer Diameter
11.0 ADDITIONAL EPITAXIAL LAYER CHARACTERISTICS				
11.1	Conductivity Type/Structure	*p/p-*	*p/p+*	*p/p++*
11.2	Primary Dopant	Boron	Boron	Boron
11.3	Silicon Source Gas	NS	NS	NS
11.4	Epi Growth Method	NS (see item 5.3)	NS (see item 5.3)	NS (see item 5.3)
11.5	Carrier Density Range - Must be met at all points on the wafer surface inside the edge exclusion (See Note 11.)	User/supplier agreement	User/supplier agreement	User/supplier agreement
11.6	Layer Thickness (Target Value at Wafer Center and Tolerance)	Target: user/supplier agreement Tolerance: ± 5%	Target: user/supplier agreement Tolerance: ± 5%	Target: user/supplier agreement Tolerance: ± 5%
11.7	Thickness Variation (within wafer per SEMI M11)	10%	10%	10%
11.8	Transition Width	User/supplier agreement	User/supplier agreement	User/supplier agreement
11.9	Layer Flat Zone	User/supplier agreement	User/supplier agreement	User/supplier agreement
13.1	Stacking Faults (See Note 7.)	< 0.012/cm^2	< 0.012/cm^2	< 0.012/cm^2
TBD	Large Area Defects (LAD's) (See Note 7.)	< 0.006/cm^2	< 0.006/cm^2	< 0.006/cm^2
13.2	Slip/Dislocations (See Note 8.)	none	none	none
13.5 - 13.13	OTHER	(see 13.1)	(see 13.1)	(see 13.1)

NOTE 1: * indicates substrate specification.

NOTE 2: NS is the abbreviation for Not Specified.

NOTE 3: Non-destructive metrology did not exist at the time this document was approved.

NOTE 4: The site size is 25 mm × 32 mm. Partial sites are included. The metrology was being developed at the time this document was being balloted.

NOTE 5: These values are mathematically consistent. The 0.09 µm count limit was transformed using draft international standard: ISO 14644-1 which follows the equation: 112 counts per wafer = 200 counts per wafer /(0.12 µm /0.09 µm)^2.

NOTE 6: The process control capability is expected to be: ≤ 500 @ ≥ 0.25 µm.

NOTE 7: Large Area Defects (LAD's) are surface imperfections or particles that have geometry with at least one side or diameter that is a minimum of 1 micron in length .

NOTE 8: Tested per SEMI MF1726; a depth < 100 nm is acceptable.

NOTE 9: Only process control data is required. Data not required on Certificate of Compliance.

NOTE 10: The first column under item references SEMI M18. M18 was in the process of substantial revision at the time this documented was balloted. Many M18 line references remain to be determined. TBD is the abbreviation for "to be determined".

NOTE 11: The intent in specifying carrier density using a range, rather than the center nominal with tolerance accompanied by a wafer variation limit, is to minimize the importance of edge variations and to emphasize meeting the range of carrier density as it is allowed by the process and the designers.

Table 10 Guide for the Specification of 90 nm Design Rule Silicon Epitaxial Wafers with DSP Substrates

ITEM (See Note 1)		*p/p⁻ EPITAXIAL WAFER*	*p/p⁺ EPITAXIAL WAFER*	*p/p⁺⁺ EPITAXIAL WAFER*
1.0	**SUBSTRATE GENERAL CHARACTERISTICS (See Note 1)**			
1.1	Growth Method	Cz or MCz		
1.2	Crystal Orientation	{100}		
1.3	Crystal Orientation/Tolerance	±1°		
1.4	Substrate Conductivity Type	p^-	p^+	p^{++}
1.5	Dopant	Boron		
1.6	Nominal Edge Exclusion (Note 2)	2 mm (300 mm) or 3 mm (200 mm)		
2.0	**SUBSTRATE ELECTRICAL CHARACTERISTICS**			
2.1	Substrate Resistivity (Center Point)	0.8–15 Ω·cm	0.01–0.02 Ω·cm	0.005–0.010 Ω·cm
2.2	Substrate Radial Resistivity Variation (See Note 3.)	≤ 20%		
3.0	**CHEMICAL CHARACTERISTICS**			
3.1	Oxygen Concentration (Center)	supplier-purchaser agreement (See Notes 4 & 5)	supplier-purchaser agreement (See Notes 4 & 6) supplier-purchaser	
TBD	Oxygen Concentration Tolerance (Center)	supplier-purchaser agreement		
3.2	Radial Oxygen Variation	supplier-purchaser agreement 10 mm from Edge (See Note 7)		
3.3	Carbon Concentration	≤ 0.5 ppma (Background, See Notes 3 & 4)	≤ 0.5 ppma (Background, See Notes 3, 4 & 8)	
4.0	**STRUCTURAL CHARACTERISTICS**			
4.1	Dislocation Etch Pit Density	supplier-purchaser agreement		
4.2	Slip			
4.3	Lineage			

ITEM (See Note 1)		*p/p⁻ EPITAXIAL WAFER*	*p/p⁺ EPITAXIAL WAFER*	*p/p⁺⁺ EPITAXIAL WAFER*
4.4	Twin			
4.5	Swirl			
4.6	Shallow pits			
4.7	Oxidation-Induced Stacking Faults (OSF)			
5.0	**WAFER PREPARATION CHARACTERISTICS**			
5.1	Wafer ID Marking	per SEMI M1		
5.4	Extrinsic Gettering Treatment	supplier-purchaser agreement		
5.5	Backseal			
5.6	Annealing			
6.0	**SUBSTRATE MECHANICAL CHARACTERISTICS (**Per SEMI M1 Unless Otherwise Specified)			
6.1	Diameter	300 or 200		
6.2	Notch Dimensions	per SEMI M1		
6.3	Notch Orientation	<110> ± 1°		
6.61	Edge Profile	per SEMI M1		
6.6.2	Edge Surface Finish	Polished		
6.7	Substrate Thickness	775 ± 20 µm [300 mm diameter] or 725 ± 20 µm [200 mm diameter]		
6.8	Thickness Variation (GBIR)	≤ 3 µm		
6.9	Surface Orientation and Tolerance	(100) ± (0.2 – 1)°		

EPITAXIAL WAFER（Epitaxial Layer and Substrate）

11.0	**EPITAXIAL LAYER CHARACTERISTICS**			
11.1	Conductivity Type	*p/p⁻*	*p/p⁺*	*p/p⁺⁺*
11.2	Primary Dopant	Boron		
11.3	Silicon Source Gas	supplier-purchaser agreement		
11.4	Epi Growth Method			
11.5	Carrier Density Range - Must be met at all points on the wafer surface inside the edge exclusion (See Note 13)			
11.6	Net Carrier Density Variation	≤ 15%		
11.7	Layer Thickness (Target Value at Wafer Center and Tolerance)	Target: supplier-purchaser agreement		
11.8	Thickness Variation (within wafer, per SEMI M11, Section 6.3)	≤ 10%		
11.9	Flat Zone	supplier-purchaser agreement		
11.10	Transition Width	supplier-purchaser agreement		
12.0	**MECHANICAL CHARACTERISTICS**			
12.1	Bow	supplier-purchaser agreement		
12.2	Warp	≤ 50 µm (See Note 3)		
12.3	Sori	supplier-purchaser agreement		
12.4a	Total Thickness Variation (GBIR or TTV, see NOTE 9.)	≤ 4 µm		

	ITEM (See Note 1)	*p/p⁻ EPITAXIAL WAFER*	*p/p⁺ EPITAXIAL WAFER*	*p/p⁺⁺ EPITAXIAL WAFER*
12.4b	Global Flatness (GFLR or TIR)	≤ 3 µm		
12.5	Flatness/Site (See Note 10)	SFQR ≤ 90 nm Site Size 26 mm x 8 mm Percent Usable Area ≥ 95% Partial Sites Included Or Percent Usable Area 100% Full Sites Only X-offset = 0 and Y-offset = 0		
12.7	Nanotopography for each analysis area at a specified percentage defective (See SEMI M43)	supplier-purchaser agreement		
12.8	Misfit Dislocations	supplier-purchaser agreement		
13.0	**FRONT SURFACE CHARACTERISTICS**			
13.2	Slip (Note 15)	none		
TBD	Dislocation Density			
TBD	Contamination/Area			
TBD	Edge Cracks			
13.5a	Scratches – macro			
13.5b	Scratches – micro			
13.6	Dimples			
13.7	Orange Peel			
13.8	Cracks/Fractures			
13.9	Crow's Feet			
13.10	Edge Chips			
13.11	Edge Crown			
13.12	Haze			
13.13	Foreign Matter			
TBD	Saw Marks			
TBD	Dopant Striation Rings			
TBD	Stains			
13.14	Localized Light Scatters (LLS) (300 mm diameter, scale for 200 mm)	Size ≥ 90 nm Count ≤ 238 (Note 11, 16, 17) Size ≥ 300 nm Count ≤10 (Note 17) Size ≥ 2,000 nm Count ≤ 5 (See Note 14)		
TDB	Surface Metal Contamination (See Note 3)			
TDB	Sodium	$\leq 1 \times 10^{10}/cm^2$		
TDB	Aluminum	$\leq 1 \times 10^{10}/cm^2$		
TDB	Potassium	$\leq 1 \times 10^{10}/cm^2$		
TDB	Chromium	$\leq 1 \times 10^{10}/cm^2$		
TDB	Iron	$\leq 1 \times 10^{10}/cm^2$		
TDB	Nickel	$\leq 1 \times 10^{10}/cm^2$		
TDB	Copper	$\leq 1 \times 10^{10}/cm^2$		
TDB	Zinc	$\leq 1 \times 10^{10}/cm^2$		

	ITEM (See Note 1)	*p/p⁻ EPITAXIAL WAFER*	*p/p⁺ EPITAXIAL WAFER*	*p/p⁺⁺ EPITAXIAL WAFER*
TDB	Calcium	$\leq 1 \times 10^{10}/cm^2$		
14.0	**BACK SURFACE CRITERIA**			
14.1	Contamination/Area	none		
14.2	Scratches – macro	supplier-purchaser agreement		
14.3	Scratches – micro			
14.4	Localized Light Scatterers			
TBD	Edge Chips	none		
TBD	Cracks, Crow's Feet			
TBD	Saw Marks			
TBD	Stains			
TBD	Roughness	Polished		
TBD	Brightness (Gloss) 60° angle of incidence, referenced to a mirror polished wafer.	≥ 80% (See Note 12)		
15.0	**OTHER CHARACTERISTICS**			
TBD	Denuded Zone Free of Bulk Micro-defects (BMD)	supplier-purchaser agreement		
TBD	BMD（Bulk Micro-defect Density) Thermal Cycle per SEMI MF1239）			

NOTE 1: The first column under item references SEMI Standard M18. M18 was in the process of substantial revision at the time this documented was balloted. Many M18 line references remain to be determined. TBD is the abbreviation for "**to be determined**".

NOTE 2: Unless otherwise agreed upon for a specific characteristic or test method.

NOTE 3: Only process control data is required. Data not required on Certificate of Compliance. A larger warp value may be appropriate if a oxide layer is deposited on the back of the substrate.

NOTE 4: Oxygen level in itself should not be specified but rather is only a control parameter that may give an indication of the amount of precipitation that will occur after some thermal process that nucleates and grows Bulk Micro-defects generated at precipitates. Addition of nitrogen or carbon (above the background level) to the crystal can enhance the growth of these precipitates.

NOTE 5: Test in accordance with SEMI MF1188, JEIDA 61, or DIN 50438/1. Also see SEMI M44.

NOTE 6: Test in accordance with SEMI MF1366 or Gas Fusion Analysis, as agreed between supplier and purchaser. Non-destructive metrology did not exist at the time this document was approved.

NOTE 7: Test in accordance with SEMI MF951, Plan A1, A2, or A3, as agreed between supplier and purchaser.

NOTE 8: Non-destructive metrology did not exist at the time this document was approved.

NOTE 9: The 9-point TTV parameter has been replaced by GBIR. See 12.4a.

NOTE 10: SFQR with a site size of 26 mm × 8 mm is approximately equal to SFSR with a site size of 26 mm x 32 mm at the 90 nm technology level. The smaller site allows more coverage of the FQA than the larger site. The value of site flatness of 90 nm is taken from the ITRS Starting Materials Table.

NOTE 11: The 90 nm count, 238, may be transformed to another maximum LLS count using draft international standard: ISO/DIS 14644-1 which uses the equation: count per wafer at 65 nm (new minimum size) = (count per wafer at 90 nm) *(90 nm / 65 nm) ^{2}. For example converting from a 90 nm minimum size to a 65 nm minimum size yields a count of 456.

NOTE 12: This specification implies a polished back surface.

NOTE 13: The intent in specifying carrier density using a range, rather than the center nominal with tolerance accompanied by a wafer variation limit, is to minimize the importance of edge variations and to emphasize meeting the range of carrier density as it is allowed by the process and the designers.

NOTE 14: Large Area Defects (LADs) are surface imperfections or particles that have geometry with at least one side or diameter that is equal to or greater than the layer thickness. Their actual size cannot be currently implied from the output of an SSIS.

NOTE 15: Slip tested in accordance with SEMI MF1726; an etch depth < 100 nm is acceptable. The metrology used for slip determination is a major factor in determining the presence or absence of slip lines. X-ray Topography is much more sensitive than the ASTM etching and microscopic inspection method given here but no Standard Test Method currently exists. X-ray Topography will detect slip that may not penetrate to the near surface region where the device is fabricated. Use of SSIS equipment set at less ≤90 nm can also reveal slip lines on epi wafers but again no Standard Test Method currently exists. Surface roughness may interfere with SSIS measurements. With the thermal cycles employed in 90 nm technology thermal processes, slip propagation should not be a problem.

NOTE 16: Value from the 2003 ITRS 90 nm node.

NOTE 17: May include stacking faults of different scattering intensities and other structural epitaxial defects which are not correctly sized by current generation SSISs.

NOTICE: SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI M12-1103
SPECIFICATION FOR SERIAL ALPHANUMERIC MARKING OF THE FRONT SURFACE OF WAFERS

This specification was technically approved by the Global Traceability Committee and is the direct responsibility of the North American Traceability Committee. Current edition approved by the North American Regional Standards Committee on July 27, 2003. Initially available at www.semi.org October 2003; to be published November 2003. Originally published in 1988; previously published March 2003.

1 Purpose

1.1 This specification provides a serial alphanumeric marking of silicon or other semiconductor wafers. The wafer serial number links the properties of the wafer stored in an appropriate database system to each individual wafer for purposes of tracking and control during wafer and device manufacture.

1.2 By defining the basic code used for the mark, this specification ensures the consistency of wafer marking performed by wafer manufacturers. Thus, it allows simplification of the performance requirements of automatic optical character reading (OCR) equipment, provides for unassisted and immediate human readability without wafer handling, and facilitates resolution of wafer level process variations.

1.3 The marking code is intended to be valid for a broad range of wafer products (i.e., epi, SOI, processed polished wafers, etc.).

2 Scope

2.1 This specification defines the geometric and spatial limits of the alphanumeric code, specifically for serial identification of flatted and notched silicon wafers.

2.2 This specification does NOT address the marking techniques that may be employed when complying with this standard.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Definitions*

4.1.1 *adjacent character misalignment, R_{adj}* — the vertical distance between the character baselines of two adjacent characters on the same line.

4.1.2 *character separation* — the horizontal distance between the adjacent boundaries of any two adjacent characters.

4.1.3 *character spacing* — the horizontal distance between the character centerlines of any two adjacent characters.

4.1.4 *character window* — the rectangular window within which all characters must be contained.

4.1.5 *front surface of the wafer* — the exposed surface upon which active semiconductor devices have been or will be fabricated.

4.1.6 *line character misalignment, R_{line}* — the vertical distance between the character baselines of the highest and the lowest characters on the same line.

5 Shape and Size of Marking

5.1 Solid line or dot matrix method may be used to write characters. The minimum matrix shall be 5 dots horizontal and 9 dots vertical. More dots may be used, up to and including a solid line. Higher density is recommended to achieve improved read reliability (see Related Information 1).

5.2 *Character Dimensions and Spacing* — (see Table 1 and Figure 1)

Table 1 Character Dimensions

Character	*mm*
Height	1.624 ± 0.025
Width	0.812 ± 0.025
Thickness (See NOTE 1)	0.200 + 0.050/-0.150
Spacing	1.420 ± 0.025

NOTE 1: The thickness of the diagonal in the letter " N" is 0.138 ± 0.05 mm for single density dot matrix.

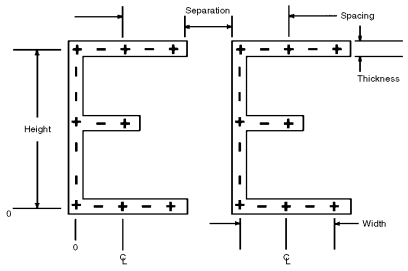


Figure 1
Character Outline

Table 2 Code

Character Location	*CharacterStyle*	*Parameter*	*Code*	*Definition*
1	Alpha/Numeric	IDENTIFICATION NUMBER	A through Z and 0 through 9	Supplier-Assigned (see Note 1)
2	Alpha/Numeric			
3	Alpha/Numeric			
4	Alpha/Numeric			
5	Alpha/Numeric			
6	Alpha/Numeric			
7	Alpha/Numeric			
8	Numeric Only		0 through 9	
9	Alpha Only	WAFER SUPPLIER IDENTIFICATION	A through Z	(see SEMI AUX001[1] and Note 1)
10	Alpha Only			
11	Alpha Only	CHECK CHARACTER A_{11}	A through H	Error-Detecting Method (see Section 9)
12	Numeric Only	CHECK CHARACTER A_{12}	0 through 7	

NOTE 1: In the absence of information at any assigned location, a dash (–) must be used.

6 Alphanumeric Code

6.1 The code consists of one line of 12 characters. The first eight characters are an identification number which is unique to the wafer for a given vendor. These characters may be alphanumeric except character 8 which must be numeric (see Table 2). Characters 9 and 10 comprise the supplier identification code (see SEMI AUX001[1]). Characters 11 and 12 are check characters (see Section 9). These check characters are machine generated for code acceptance and reading verification.

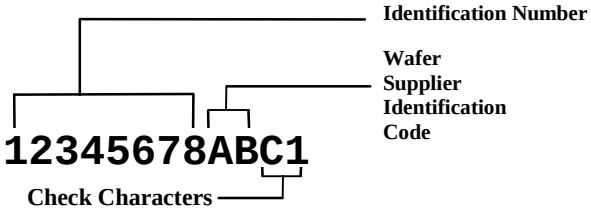


Figure 2
Example of Code

6.2 In the absence of a character at any assigned location, a dash (–) must be used.

1 SEMI AUX001, List of Wafer Supplier Identification Codes, available from SEMI web site: www.semi.org.

6.3 An example of the code is given in Figure 2.

6.4 *SEMI-OCR Standard Character Set* — This character set contains capital letters from A to Z, numerals from 0 to 9, a dash, and a period (see Appendix 1). The period is NOT used in the code symbols defined in this specification (see Tables 2 and 3), although it is required for use in the code symbols defined in SEMI M13.

Table 3 SEMI OCR Character Set Modified for Use in this Specification

ABCDEFGHIJKLMNO
PQRSTUVWXYZ-
0123456789

7 Character Window

7.1 The character window must be located on the front surface of the wafers.

7.2 All characters must be contained within the character window dimensions specified in Figures 3 (for flatted wafers) or Figure 4 (for notched wafers).

7.3 The top of the characters is toward the side of the character window nearest to the flat or notch.

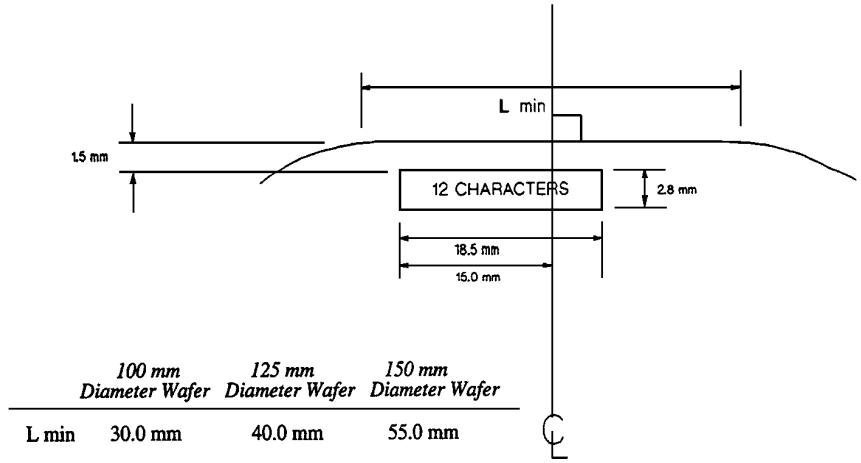


Figure 3
Character Window Location for Flatted Wafers

NOTE: The vertical center line referenced in Figure 3 is the bisector of the primary fiducial (flat).

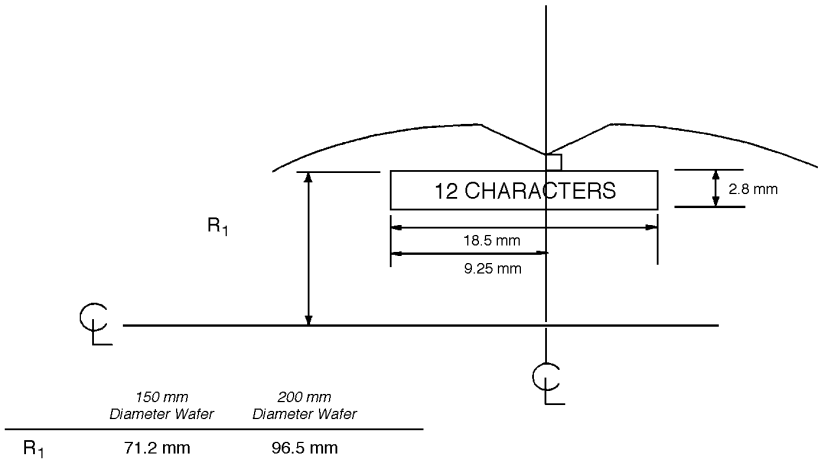


Figure 4
Character Window Location for Notched Wafers

NOTE: The vertical center line referenced in Figure 4 is the bisector of the primary fiducial (notch).

8 Character Alignment

8.1 *Character Skew* — the maximum allowable angle between the character baseline and a line parallel with the bottom of the character window shall be 3 degrees (see Figure 5).

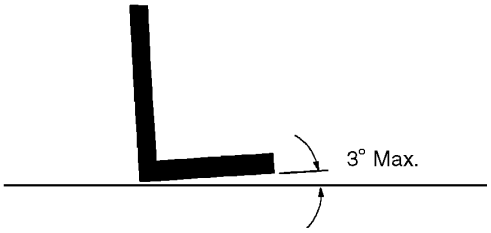


Figure 5
Character Skew

NOTE: This line is parallel to the bottom of the character window.

8.2 *Maximum Character Misalignment* — the maximum adjacent character misalignment, R_{adj} shall be 0.23 mm (see Figure 6), and the maximum line character misalignment, R_{line}, shall be 0.46 mm (see Figure 7).

Figure 6
Adjacent Character Misalignment

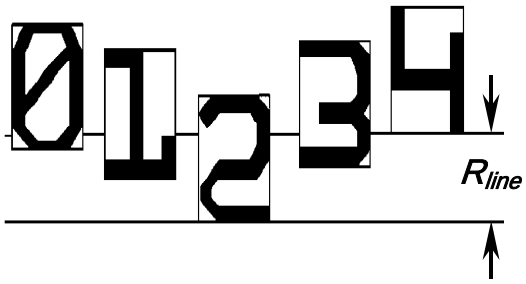


Figure 7
Line Character Misalignment

9 Alphanumeric Error-Detecting Method

9.1 The alphanumeric check characters in character locations 11 and 12 are a required part of the Code defined in this specification.

9.2 All single-character substitution errors are detected.

9.3 All two-character transposition errors are detected for any message up to 58 characters in length.

9.4 The character set may be expanded to include the first 59 characters of the ASCII 64-character set.

9.5 There exist simple recursive algorithms for error detection and check character generation that do not require the use of multiplication or division.

9.6 *Definition of the Error-Detecting Method*

9.6.1 For the purpose of describing the error-detecting method, we define the following symbols:

- A_i represents the ith ASCII character.
- a_i represents the numerical value assigned to A_i.

9.6.2 The characters are numbered from left to right, so that the message is given by

$$A_1A_2A_3 \ldots A_{12}$$

9.6.3 A complete description of the error-detecting method is given by the following seven rules:

9.6.3.1 The numerical value a_i is found by subtracting 32 from the ASCII decimal representation of A_i (refer to Table 4 — Character Values).

9.6.3.2 An ASCII character A_i is allowed only if its numerical value a_i is one of

$$0,1,2,\ldots 58.$$

9.6.3.3 The check character A_{11} must be one of the ASCII characters A,B,C,D,E,F,G,H.

9.6.3.4 The check character A_{12} must be one of the ASCII characters 0,1,2,3,4,5,6,7.

9.6.3.5 The check character pair $A_{11}A_{12}$ may not be one of the combinations H3, H4, H5, H6, H7.

9.6.3.6 When the message is written, the check characters A_{11} and A_{12} are chosen such that 59 divides the expression

$$8^{11}a_1 + 8^{10}a_2 \ldots + 8^2a_{10} + 8a_{11} + a_{12}$$

without a remainder.

9.6.3.7 If, on reading the message, 59 does not evenly divide the expression given above, an error has occurred.

Table 4 Character Values

ASCII Character	*ASCII Decimal Value*	*Numerical Value*
–	45	13
.(Note 1)	46	14
0	48	16
1	49	17
2	50	18
3	51	19
4	52	20
5	53	21
6	54	22
7	55	23
8	56	24
9	57	25
A	65	33
B	66	34
C	67	35
D	68	36
E	69	37
F	70	38
G	71	39
H	72	40
I	73	41
J	74	42
K	75	43
L	76	44
M	77	45
N	78	46
O	79	47
P	80	48
Q	81	49
R	82	50
S	83	51
T	84	52
U	85	53
V	86	54
W	87	55
X	88	56
Y	89	57
Z	90	58

Note 1: This character is not used in the code symbol covered by this specification.

9.7 *Suggestions for Implementation* — The error-detecting method can be implemented directly by calculating the expression given above, and the check characters can be found by exhaustive search. However, this approach is unnecessarily complex; a decrease in complexity can be made by taking advantage of three simple observations.

9.7.1 First, since we are interested only in the remainder of the final expression after dividing it by 59, we can avoid working with large numbers by subtracting 59 repeatedly after each operation until the result is less than 59.

9.7.2 Second, we can rearrange the error-detecting expression, using Horner's Rule, to form

$$a_{12} + 8\left(a_{11} + \ldots 8\left(a_3 + 8\left(a_2 + 8a_1\right)\right)\ldots\right)$$

which can be calculated recursively from the inside out by successive multiplication and addition.

9.7.3 Third, multiplication by eight can be accomplished by adding a quantity to itself three times in succession.

9.8 *An Algorithm for Error Detection*

9.8.1 When implementing error detection, it is convenient to imagine a checksum for each individual character position. This partial checksum forms a check on all preceding characters, as well as the present character. Then using Horner's Rule, one can calculate a running checksum (that is, calculate each partial checksum in order). This leads to the following algorithm.

9.8.2 Add the checksum (or the previous character position to itself. (For the first character position, the value of the previous checksum is zero.) If the result is 59 or greater, subtract 59. This leaves a value in the range 0–58.

9.8.3 Add the result of step 1 to itself. If the result is 59 or greater, subtract 59.

9.8.4 Add the result of step 2 to itself. If the result is 59 or greater, subtract 59. The result of this step is eight times the previous position checksum, modulo 59.

9.8.5 Add the result of step 3 to the numerical value of the character in the present position. If the result is 59 or greater, subtract 59. The result of this step is the checksum for the present character position.

9.8.6 Repeat steps 1 through 4 for each character position. If the checksum for the final character position is nonzero, an error has occurred.

9.9 *An Algorithm for Generating the Check Characters* — The check characters can be generated as follows:

9.9.1 Initially, assume that the check characters are A0 (the first check character is the letter A, the second is the numeral 0).

9.9.2 Calculate the final checksum in the manner described above for error detection. If the result is zero, the check characters are correct, and the algorithm terminates.

9.9.3 If the result of step 2 is nonzero, subtract it from 59, yielding a number in the range 1–58.

9.9.4 Convert the result of step 3 to binary.

9.9.5 Add the least significant three bits of the binary number to the numerical value of the second assumed check character 0 (numeral zero). This will yield a value that corresponds to an ASCII character in the range 0–7.

9.9.6 Add the next higher three bits of the binary number to the numerical value of the first assumed check character A. This will yield a numerical value that corresponds to an ASCII character in the range A–H.

9.10 *An Illustrative Example* — For the purpose of illustrating the check character generating algorithm, assume that the message consists of only two characters, the numerals 2 and 3.

9.10.1 Initially, assume that the check characters are A and 0 (zero) yielding the composite message 23A0.

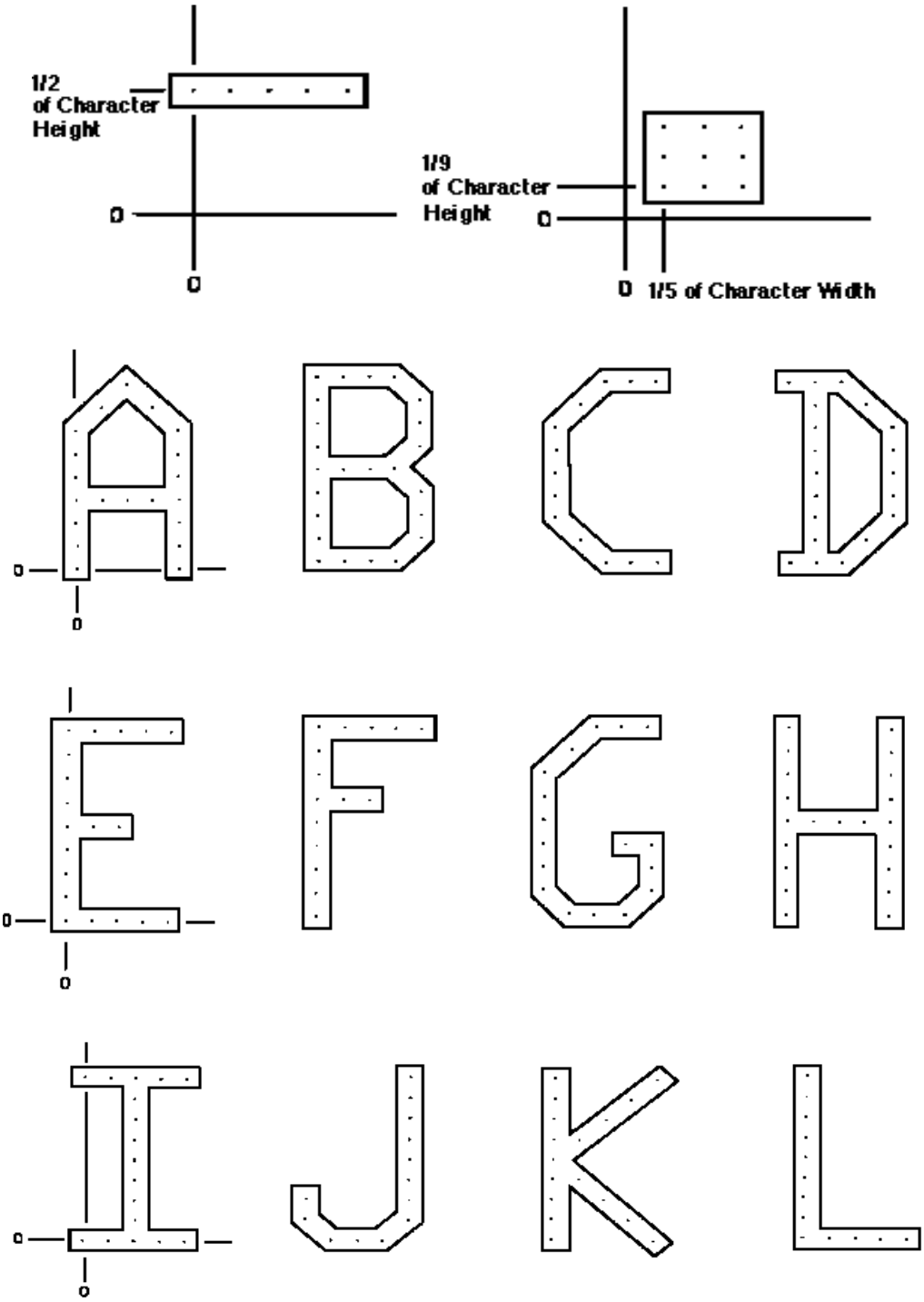
9.10.2 Using the algorithm described above, the final checksum is found to be 33. Since this is nonzero, it is subtracted from 59, yielding 26 in decimal, or 011010 in binary.

9.10.3 The least significant three bits 010 (decimal value 2) added to the numerical value of the ASCII character 0 (numeral zero), which is 16, yields 18 (the numerical value of the ASCII character 2).

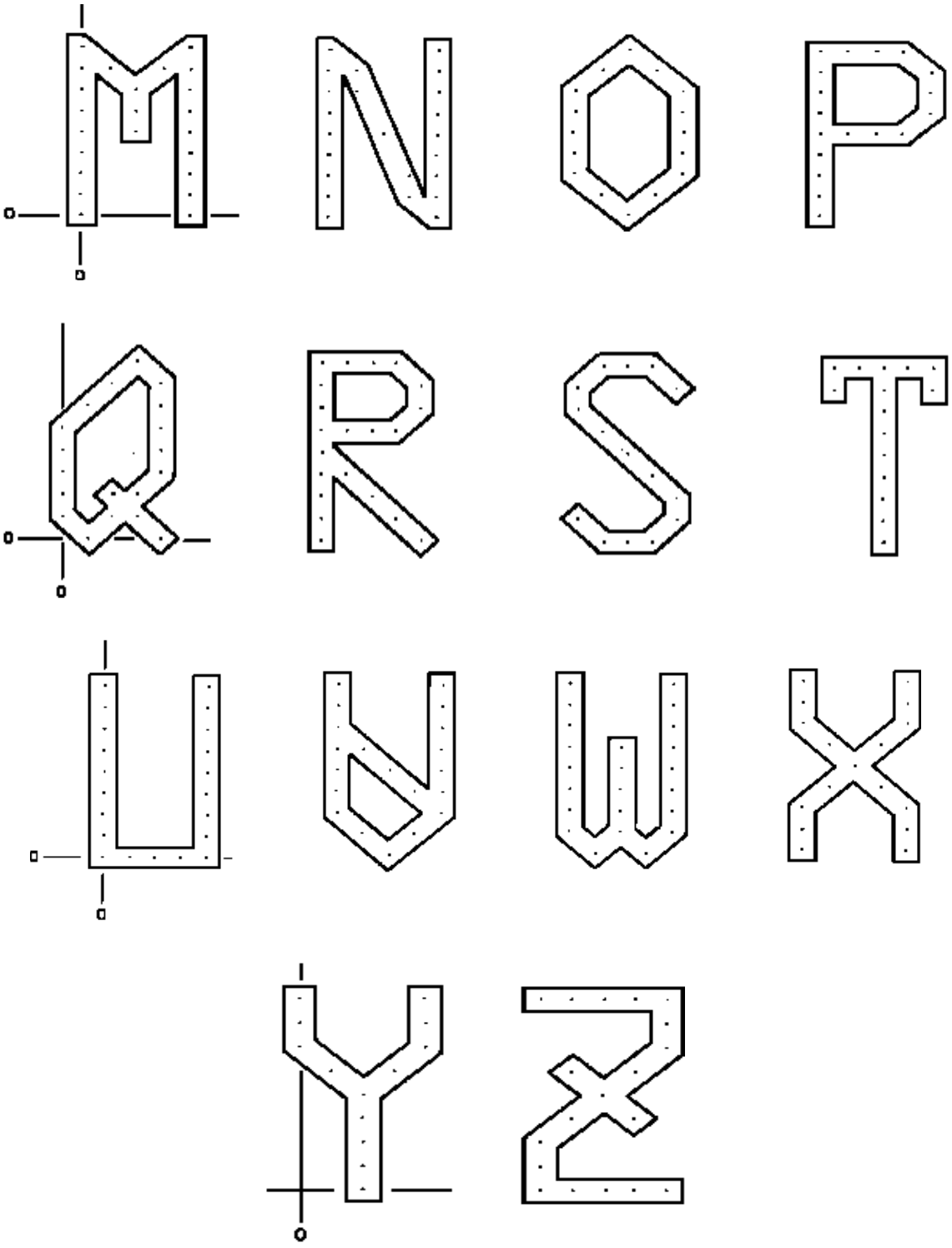
9.10.4 The next higher three bits 011 (decimal value 3) added to the numerical value of the ASCII character A, which is 33, yields 36 (the numerical value of the ASCII character D). The final composite message is 23D2.

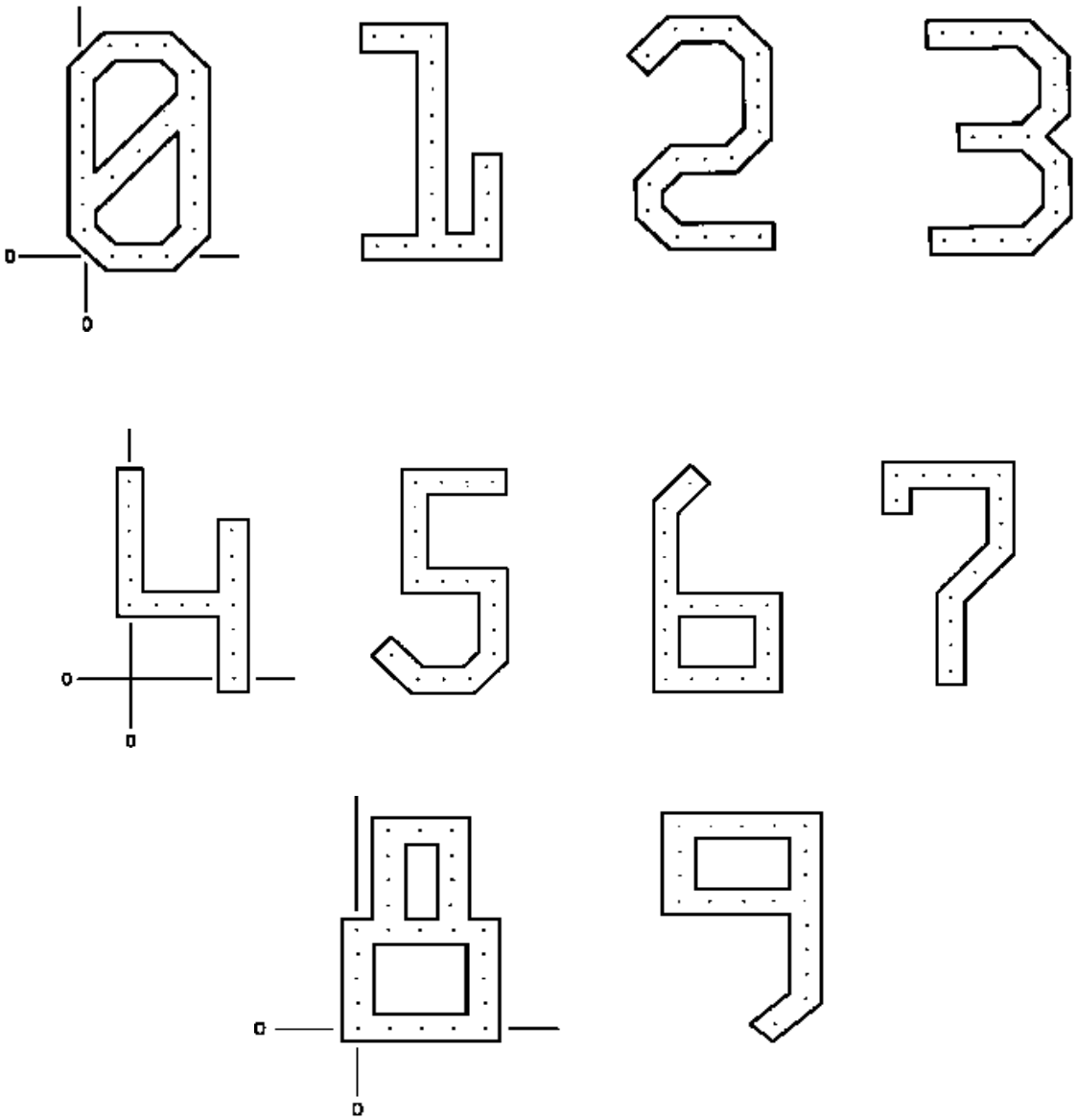
APPENDIX 1
SEMI OCR CHARACTER OUTLINES

NOTICE: The material in this appendix is an official part of SEMI M12 and was approved by full letter ballot procedures on July 12, 1998.



NOTE 1: The character shown above for "period" [.] is not used in this specification (SEMI M12).





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RELATED INFORMATION 1

NOTICE: This related information is not an official part of SEMI M12 but was approved for publication on July 12, 1998.

R1-1 Considerations for Reliable Automatic Reading of the Marking

R1-1.1 The following suggestions are offered to assist in assuring the most reliable automatic reading of the alphanumeric marking.

R1-1.2 *Character Stroke Thickness* — If a 5 × 9 dot matrix is chosen for marking, it is recommended that the minimum dot size be 0.100 mm. Double or higher density dot matrix is recommended — when used, smaller dot diameters may be employed. Stroke thickness should be constant within 20% over the entire character set so that the reader settings may be optimized for the specific wafer run.

R1-1.3 *Contrast* — The character should have sufficient contrast to be legible. Contrast may be affected by depth and other conditions.

R1-1.4 *Clear Zone* — It is recommended that the area immediately beneath and a minimum of 0.500 mm around the marking characters be of uniform reflectivity and free of any lithography and process overlay edges.

R1-2 Considerations for the Use of Front Surface Markings

R1-2.1 Marks can impinge upon areas where devices may be printed. Since mask geometries are varied, considerations of the mark area should be made in mask design and also when applying the mark specifications to existing mask designs.

R1-2.2 When the mark is applied prior to epitaxial deposition, a crown or epi may grow along the mark edge. The height of this crown will depend upon the epi thickness and the deposition process.

SEMI M13-1103
SPECIFICATION FOR ALPHANUMERIC MARKING OF SILICON WAFERS

This specification was technically approved by the Global Traceability Committee and is the direct responsibility of the North American Traceability Committee. Current edition approved by the North American Silicon Wafer Committee on July 27, 2003. Initially available at www.semi.org October 2003; to be published November 2003. Originally published in 1988; previously published in September 1998.

1 Purpose

1.1 This specification describes an alphanumeric marking system for silicon wafers. The marking code includes information on the origin, approximate resistivity, dopant species, and crystal growth orientation in addition to a wafer identification number. Use of this specification ensures the consistency of all wafer marking performed by silicon manufacturers. This consistency allows simplification of the performance requirements of Automatic Optical Character Reading (OCR) equipment.

1.2 By defining the basic code used to characterize the individual wafer, this specification provides the information needed for practical operator interpretation.

2 Scope

2.1 This specification defines the character set, location, and associated dimensions and tolerances of an alphanumeric code, specifically for identification of flatted and notched silicon wafers.

2.2 This specification does not address the marking techniques that may be employed when complying with this standard.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 None.

4 Terminology

4.1 *Definitions*

4.1.1 *adjacent character misalignment, R_{adj}* — the vertical distance between the character baselines of two adjacent characters on the same line.

4.1.2 *character separation* — the horizontal distance between the adjacent boundaries of any characters.

4.1.3 *character spacing* — the horizontal distance between the character spacing reference lines of the adjacent characters.

4.1.4 *line character misalignment, R_{line}* — the vertical distance between the character baselines of the highest and lowest characters on the same line.

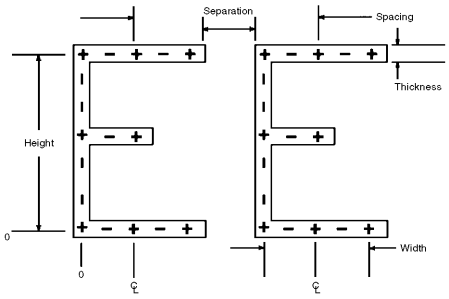


Figure 1
Character Outline

5 Shape and Size of Marking

5.1 Solid line or dot matrix method may be used to write characters. The minimum matrix shall be 5 dots horizontal and 9 dots vertical as shown in Figure 1. More dots may be used, up to and including a solid line. Higher density is recommended, especially for use with the larger code size applicable to notched wafers, to achieve improved read reliability (see Related Information 1).

5.2 *Character Dimensions and Spacing* — See Table 1 and Figure 1.

5.3 *SEMI OCR Standard Character Set* — See Table 2 and Appendix 1.

6 Alphanumeric Code

6.1 *Message Content* — The code consists of one line of 18 characters. The first eight characters are an identification number that is unique to the wafer for a given supplier. These characters may be alphanumeric except character 8, which must be numeric (see Table 3). Characters 9 and 10 are the supplier

identification code (see SEMI AUX001[1]) (See Figure 2 and Table 3.)

NOTE 1: In the absence of a character at any assigned location, a dash (-) must be used.

6.2 *Code Field Location and Dimensions* — The alphanumeric code field shall be located on the front surface of the wafers (see Figures 3 and 4 for location and dimensions of the alphanumeric code field for flatted and notched wafers, respectively).

6.3 *Character Alignment*

6.3.1 *Character Skew* — the maximum allowable angle between the character baseline and a line parallel with the bottom of the character window shall be 3 degrees (see Figure 5).

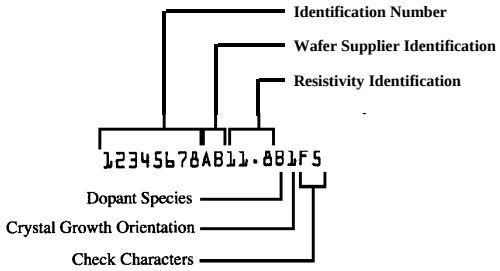
6.3.2 *Maximum Character Misalignment* — the maximum adjacent character misalignment, R_{adj}, shall be 0.23 mm (see Figure 6), and the maximum line character misalignment, R_{line}, shall be 0.46 mm (see Figure 7).

Table 1 Character Dimensions

Character	*100 mm, 125 mm, and 150 mm Flatted Wafers, mm*	*150 mm and 200 mm Notched Wafers, mm*
Height	0.812 ± 0.025	1.624 ± 0.025
Width	0.406 ± 0.025	0.812 ± 0.025
Thickness	0.100 ± 0.050	0.200 + 0.025 or – 0.150
Spacing	0.710 ± 0.025	1.420 ± 0.025
Minimum Separation	0.104	0.308

NOTE 1: The diagonal thickness of the letter "N" is 0.138 ± 0.05 mm.

Table 2 Standard Character Set



Identification Number	**12345678**
Wafer Supplier Identification	**See SEMI AUX001[2]**
Resistivity Identification	**11.8 Ω·cm**
Dopant Species	**Boron**
Crystal Growth Orientation	**[111]**
Check Characters (F5)	**Machine input for code acceptance**

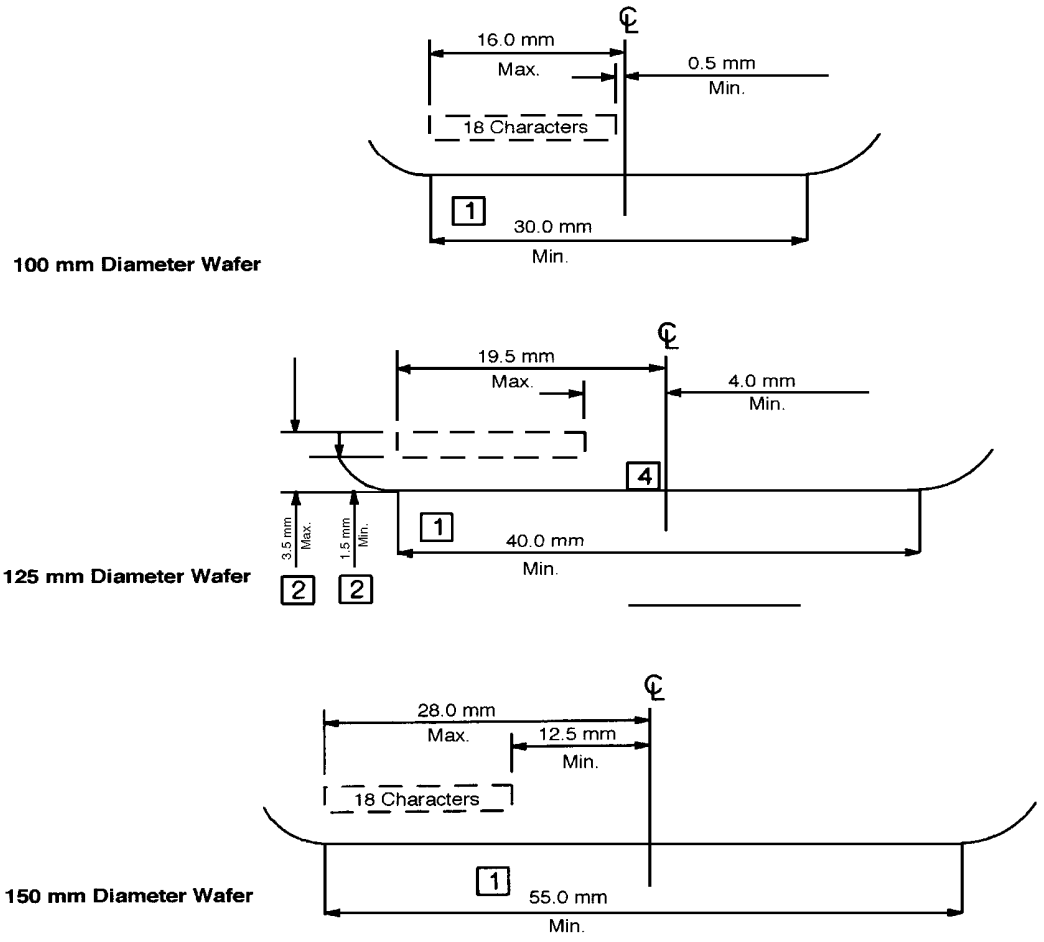
Figure 2
Example of Code

[1] SEMI AUX001, List of Wafer Supplier Identification Codes, available from SEMI web site: www.semi.org.

Table 3 Code

Character Location	*CharacterStyle*	*Parameter*	*Code*	*Definition*
1	Alpha/Numeric	IDENTIFICATION NUMBER	A through Z and 0 through 9	Supplier-Assigned (See NOTE 1.)
2	Alpha/Numeric			
3	Alpha/Numeric			
4	Alpha/Numeric			
5	Alpha/Numeric			
6	Alpha/Numeric			
7	Alpha/Numeric			
8	Numeric Only		0 through 9	
9	Alpha Only	SUPPLIER IDENTIFICATION	A through Z	(see SEMI AUX001 and NOTE 1.)
10	Alpha Only			
11	Numeric Only	RESISTIVITY IDENTIFICATION	0 through 9 and .(period)	Resistivity (Ω·cm) identification is assigned by supplier, expressed as a whole number or as a mixed number with a decimal fraction. No accuracy is implied. (See NOTE 1.)
12	Numeric Only			
13	Numeric Only			
14	Numeric Only			
15	Alpha Only	DOPANT SPECIES	B	Boron
			F	Phosphorous
			A	Arsenic
			S	Antimony
			–	not identified
16	Numeric Only	CRYSTAL GROWTH ORIENTATION	0	[100]
			1	[111]
			2	[110]
			3	[011]
			5	[511]
			–	not identified
17	Alpha Only	CHECK CHARACTER A_{17}	A through H	Error-Detecting Method (see Section 7)
18	Numeric Only	CHECK CHARACTER A_{18}	0 through 7	

NOTE 1: In the absence of information at any assigned location, a dash (–) must be used.



1 Minimum flat length shown for 100 mm, 125 mm, and 150 mm diameter wafers.

2 This dimension applies to 100 mm, 125 mm, and 150 mm diameter wafers.

Figure 3
Code Field Location for Flatted Wafers

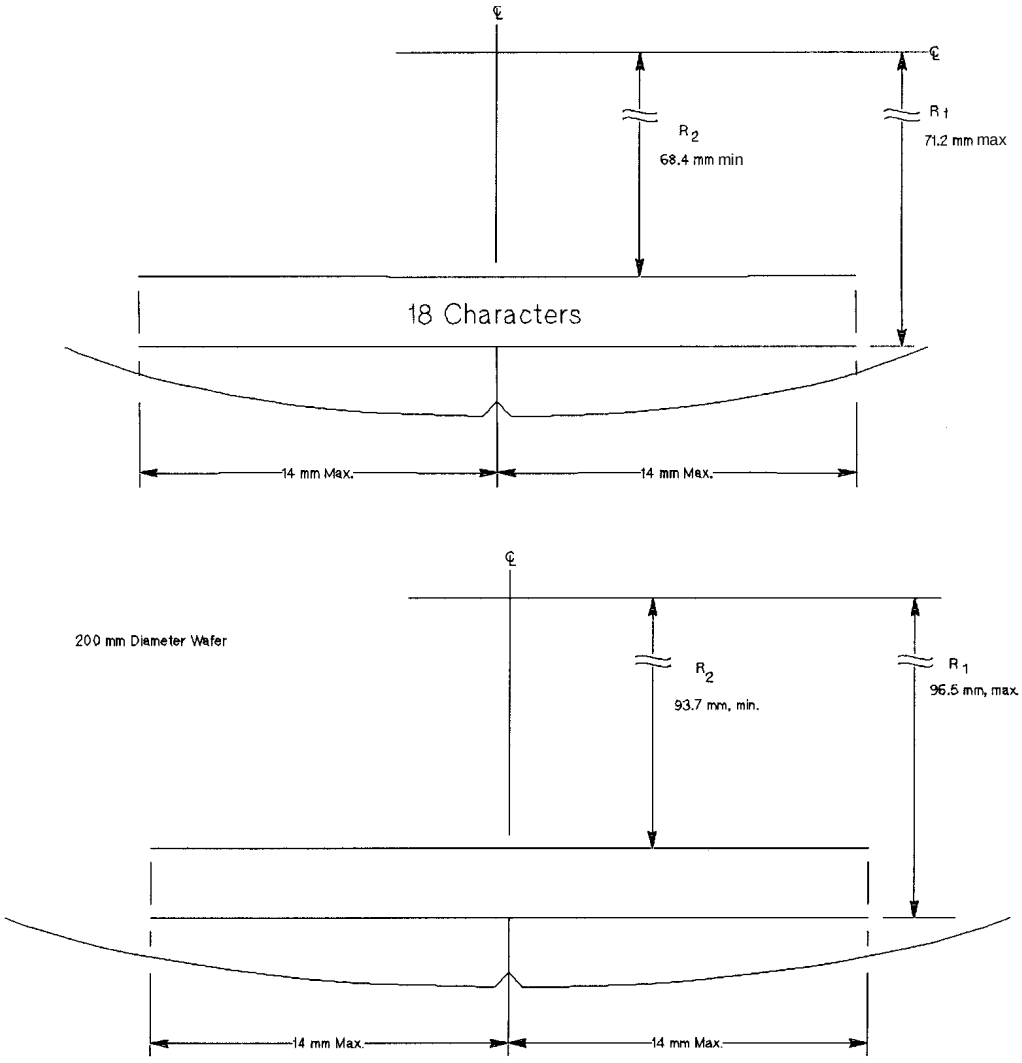


Figure 4
Field Location for Notched Wafers

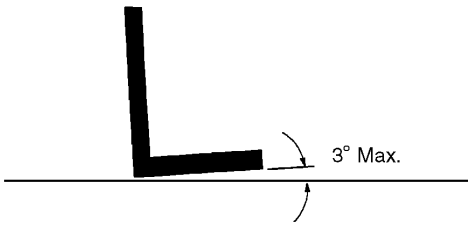


Figure 5
Character Skew

NOTE: This line is parallel to the bottom of the code field window.

Figure 6
Adjacent Character Misalignment

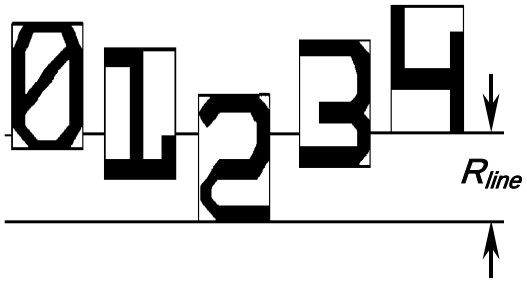


Figure 7
Line Character Misalignment

7 Alphanumeric Error-Detecting Method

7.1 The alphanumeric check characters in character locations 17 and 18 are a required part of the Code defined in this specification.

7.2 All single-character substitution errors are detected.

7.3 All two-character transposition errors are detected for any message up to 58 characters in length.

7.4 The character set may be expanded into the first 59 characters of the ASCII 64-character set.

7.5 There exist simple recursive algorithms for error detection and check character generation that do not require the use of multiplication or division.

7.6 *Definition of the Error-Detecting Method*

7.6.1 For the purpose of describing the error-detecting method, we define the following symbols:

- A_i represents the i^{th} ASCII character.
- a_i represents the numerical value assigned to A_i.

7.6.2 The characters are numbered from left to right, so that the message is given by

$$A_1A_2A_3...A_{18}.$$

7.6.3 A complete description of the error-detecting method is given by the following seven rules:

7.6.3.1 The numerical value a_i is found by subtracting 32 from the ASCII decimal representation of A_i (refer to Table 4).

7.6.3.2 An ASCII character A_i is allowed only if its numerical value a_i is one of

$$0, 1, 2, ..., 58.$$

7.6.3.3 The check character A_{17} must be one of the ASCII characters A,B,C,D,E,F,G,H.

7.6.3.4 The check character A_{18} must be one of the ASCII characters 0,1,2,3,4,5,6,7.

7.6.3.5 The check character pair A_{17} A_{18} may not be one of the combinations H3, H4, H5, H6, H7.

7.6.3.6 When the message is written, the check characters A_{17} and A_{18} are chosen such that 59 divides the expression

$$8^{17}a_1 + 8^{16}a_2... + 8^2a_{16} + 8a_{17} + a_{18}$$

without a remainder.

7.6.3.7 If, on reading the message, 59 does not evenly divide the expression given above, an error has occurred.

7.7 *Suggestions for Implementation* — The error-detecting method can be implemented directly by calculating the expression given above, and the check characters can be found by exhaustive search. However, this approach is unnecessarily complex; a decrease in complexity can be made by taking advantage of three simple observations.

7.7.1 First, since we are interested only in the remainder of the final expression after dividing it by 59, we can avoid working with large numbers by subtracting 59 repeatedly after each operation until the result is less than 59.

7.7.2 Second, we can rearrange the error-detecting expression, using Horner' s Rule, to form

$$a_{18} + 8(a_{16} + ...8(a_3 + 8(a_2 + 8a_1))...)$$

which can be calculated recursively from the inside out by successive multiplication and addition.

7.7.3 Third, multiplication by eight can be accomplished by adding a quantity to itself three times in succession.

7.8 *An Algorithm for Error Detection*

7.8.1 When implementing error detection, it is convenient to imaging a checksum for each individual character position. This partial checksum forms a check on all preceding characters, as well as the present character. Then, using Horner' s Rule, one can calculate a " running" checksum (that is, calculate each partial checksum in order). This leads to the following algorithm.

7.8.2 Add the checksum for the previous character position to itself. (For the first character position, the value of the previous checksum is zero.) If the result is 59 or greater, subtract 59. This leaves a value in the range 0-58.

7.8.3 Add the result of Step 1 to itself. If the result is 59 or greater, subtract 59.

7.8.4 Add the result of Step 2 to itself. If the result is 59 or greater, subtract 59. The result of this step is eight times the previous position checksum, modulo 59.

7.8.5 Add the result of Step 3 to the numerical value of the character in the present position. If the result is 59 or greater, subtract 59. The result of this step is the checksum for the present character position.

7.8.6 Repeat Steps 1 through 4 for each character position. If the checksum for the final character position is nonzero, an error has occurred.

7.9 *An Algorithm for Generating the Check Characters* — The check characters may be generated as follows:

7.9.1 Initially, assume that the check characters are A0 (the first check character is the letter A, the second is the numeral 0).

7.9.2 Calculate the final checksum in the manner described above for error detection. If the result is zero, the check characters are correct, and the algorithm terminates.

7.9.3 If the result of Step 2 is nonzero, subtract it from 59, yielding a number in the range 1–58.

7.9.4 Convert the result of Step 3 to binary.

7.9.5 Add the least significant three bits of the binary number to the numerical value of the second assumed check character 0 (zero). This will yield a value that corresponds to an ASCII character in the range 0–7.

7.9.6 Add the next higher three bits of the binary number to the numerical value of the first assumed check character A. This will yield a numerical value that corresponds to an ASCII character in the range A–H.

7.10 *An Illustrative Example* — For the purpose of illustrating the check character generating algorithm, assume that the message consists of only two characters, the digits 2 and 3. Initially, assume that the check characters are A and 0 (zero) yielding the composite message 23A0.

7.10.1 Initially, assume that the check characters are A and 0 (zero) yielding the composite message 23A0.

7.10.2 Using the algorithm described above, the final checksum is found to be 33. Since this is nonzero, it is subtracted from 59, yielding 26 in decimal, or 011010 in binary.

7.10.3 The least significant three bits 010 (decimal value 2) added to the numerical value of the ASCII character 0 (zero), which is 16, yields 18 (the numerical value of the ASCII character 2).

7.10.4 The final composite message is 23D2. The next higher three bits (011) (decimal value 3) added to the numerical value of the ASCII character A, which is 33, yields 36 (the numerical value of the ASCII character D).

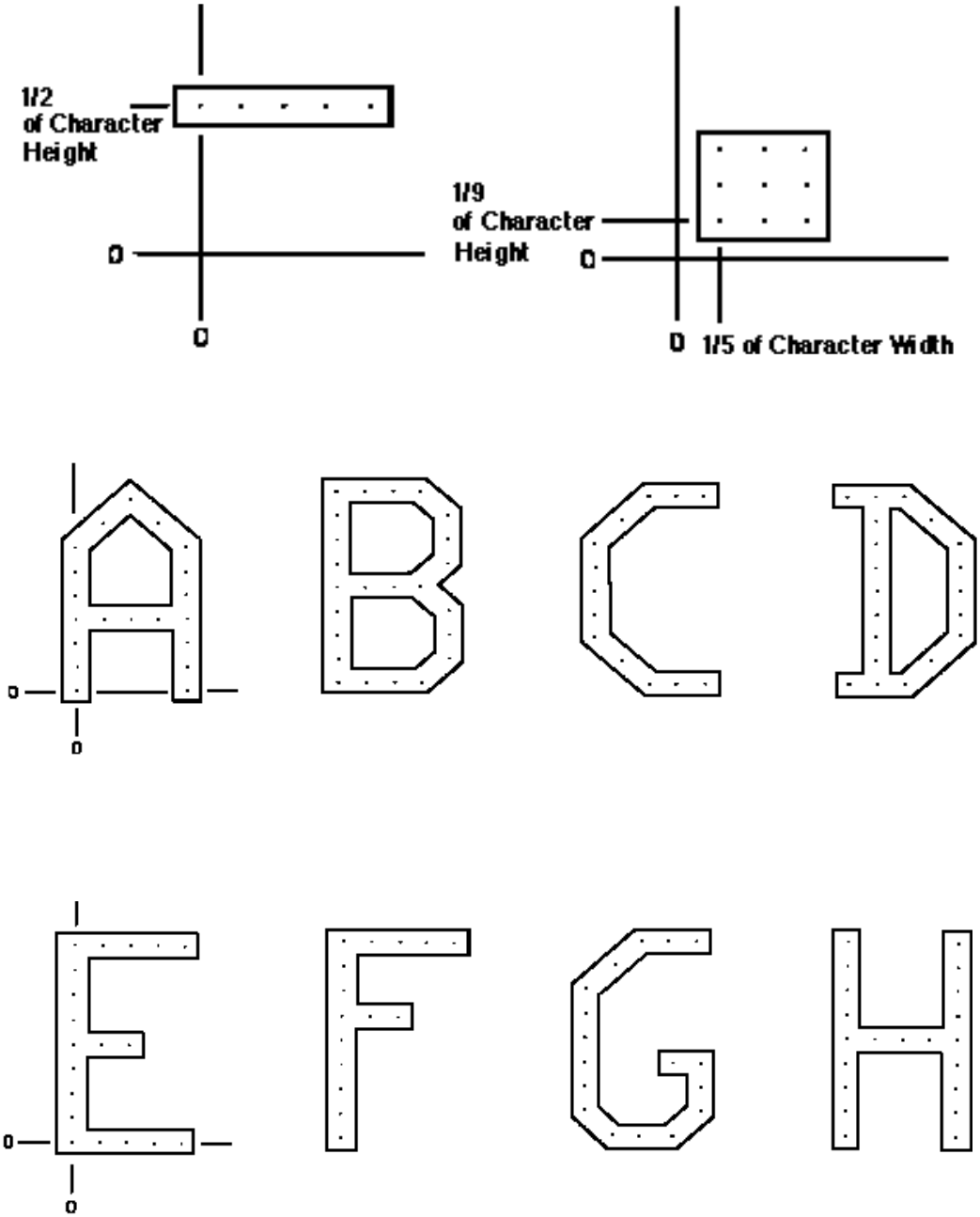
Table 4 Character Values

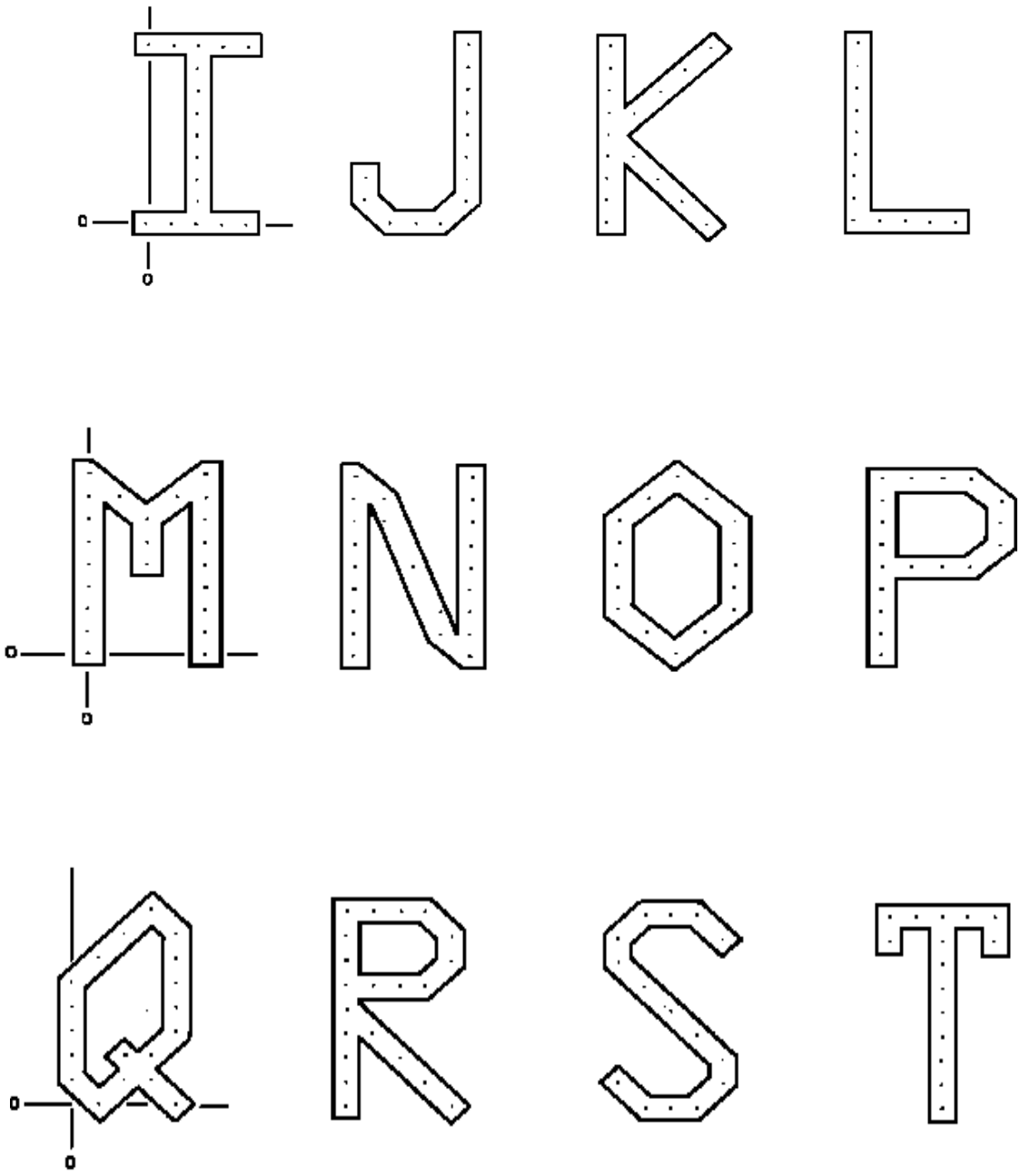
ASCII Character	*ASCII Decimal Value*	*Numerical Value*
–	45	13
.	46	14
0	48	16
1	49	17
2	50	18
3	51	19
4	52	20
5	53	21
6	54	22
7	55	23
8	56	24
9	57	25
A	65	33
B	66	34
C	67	35
D	68	36
E	69	37
F	70	38
G	71	39
H	72	40
I	73	41
J	74	42

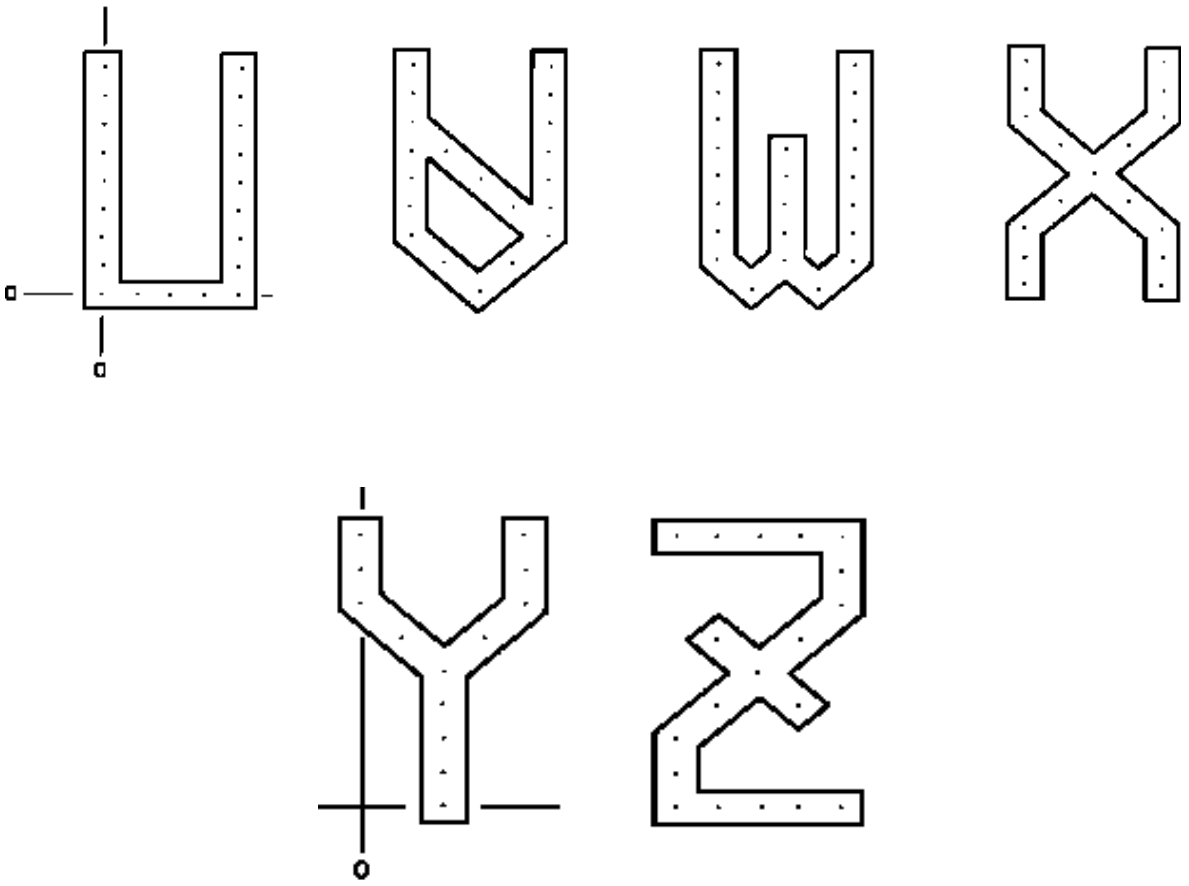
ASCII Character	*ASCII Decimal Value*	*Numerical Value*
K	75	43
L	76	44
M	77	45
N	78	46
O	79	47
P	80	48
Q	81	49
R	82	50
S	83	51
T	84	52
U	85	53
V	86	54
W	87	55
X	88	56
Y	89	57
Z	90	58

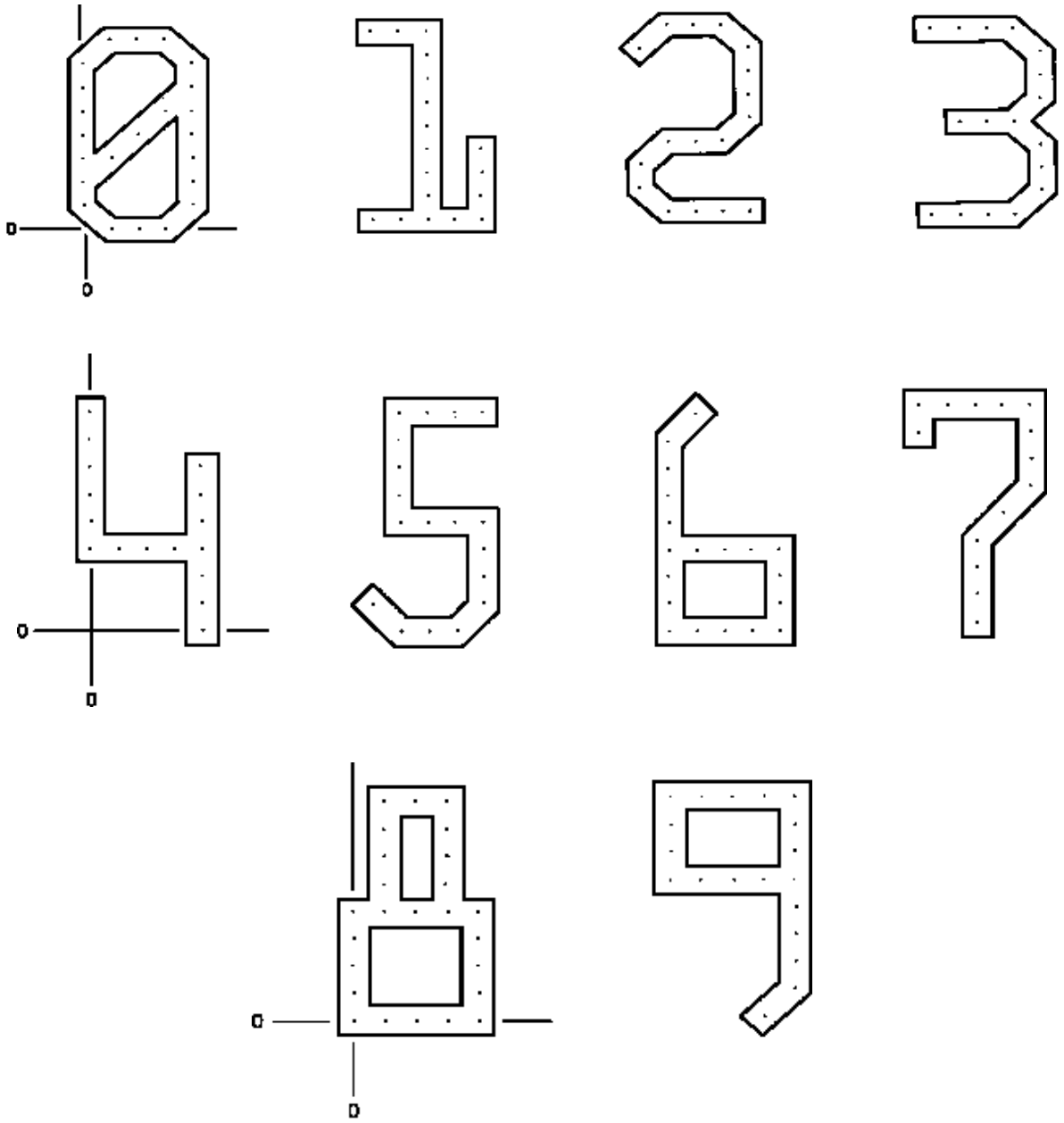
APPENDIX 1
SEMI OCR CHARACTER OUTLINES

NOTICE: The material in this appendix is an official part of SEMI M13 and was approved by full letter ballot procedures on July 12, 1998.









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