SEMI G20-96
SPECIFICATION FOR LEAD FINISHES FOR PLASTIC PACKAGES (ACTIVE DEVICES ONLY)

1 Purpose

This specification defines lead finishes for plastic packages (e.g., single-in-line, dual-in-line, quad-in-line) utilizing leadframes with SEMI specified leadframe materials.

2 Scope

This specification defines the composition, properties, and limits and refers to the appropriate tests for utility.

3 Referenced Documents

Unless otherwise specified, the following standards and specifications, with appropriate issue letter at time of order entry, form a part of this specification to the extent, and for the purpose, specified herein.

3.1 *SEMI Specifications*

SEMI G4 — Specification for Integrated Circuit Leadframe Materials Used in the Production of Stamped Leadframes

SEMI G18 — Specification for Integrated Circuit Leadframe Material Used in the Production of Etched Leadframes

SEMI G55 — Test Method Measurement of Silver Plating Brightness

SEMI G56 — Test Method Measurement of Silver Plating Thickness

3.2 *ASTM Specifications*[1]

B 487 — Measuring Metal and Oxide Coating Thickness by Microscopical Examination of Cross Section

B 545 — Standard Specification for Electrodeposited Coatings of Tin

B 567 — Measurement of Coating Thickness by the Beta Backscatter Principle

B 568 — Measurement of Coating Thickness by X-Ray Spectrometry

E 1B 571 — Adhesion of Metallic Coatings

E 10 — Standard Test Method for Brinell Hardness for Metallic Materials

E 384 — Standard Test Methods for Microhardness of Materials

3.3 *Federal Specifications*[2]

QQ-S-365 — Silver Plating, Electrodeposited, General Requirements for

QQ-S-571 — Solder, Tin Alloy: Tin Lead Alloy, and Lead Alloy

3.4 *Military Specifications*[2]

MIL-G-45204 — Gold Plating, Electrodeposited

MIL-P-81728 — Plating, Tin Lead, Electrodeposited

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-T-10727 — Tin Plating; Electrodeposits or Hot-Dipped, for Ferrous and Non-Ferrous Metals

4 Application

4.1 Table 1 lists recommended finishes for copper and nickel/iron alloys.

4.1.1 Silver is approved as a lead finish for all alloys but only for internal processing. When shipped to a customer, silver must be removed and replaced by tin lead.

4.1.2 Gold plate is usable in socketed applications as well as in soldered applications. Hardness, grain size, and other properties shall be specified on the procurement drawing.

4.1.3 Solder, as used in this specification, refers to tin lead as 63/37 or 60/40 unless otherwise specified and agreed upon between user and supplier, and stated on procurement drawings.

4.1.4 "Tinning" is a generic term (primarily used in user industries) and means hot solder dip (near 60/40 tin lead) and not an application of tin.

4.2 Composition, limits, mechanical and physical properties, and dimensions and tolerances for leadframes are stated in SEMI G4 and SEMI G18.

4.3 Lead finish details are stated in Section 5.

1 American Society for Testing Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959

2 Military Standards, Naval Publications and Forms Center, 5801 Tabor Ave., Philadelphia, PA 19120

5 Lead Finish

5.1 Tin Electroplate

5.1.1 *Composition* — The tin shall not be less than 99.8% pure tin and shall not contain more than 0.1% carbon. The deposit is Type I as defined in MIL-T-10727.

Table 1 Alloys

	Finish Iron Alloys	*Finish Copper Alloys*
Tin MIL-T-10727		
Tin (over base metal)	X	X
Acceptable Undercoats		
1. Copper	X	X
2. Nickel	X	X
Tin Lead (Sn/Pb)		
MIL-P-81728		
Tin Lead (over base metal)	X	X
Sn/Pb		
Acceptable Undercoats		
1. Copper	X	X
2. Nickel	X	X
Solder Dip (Sn/Pb)		
QQ-S-571		
Solder Dip (over base metal)	X	X
Acceptable Undercoats		
1. Copper	X	X
2. Nickel	X	X
3. Silver	X	X
Gold MIL-G-45204		
Gold (over base metal)		X
Acceptable Undercoats		
1. Nickel	X	X
2. Copper Flash	X	
Silver QQ-S-365		
Silver (over base metal)	X	X
Acceptable Undercoats		
1. Copper	X	
2. Gold		X

5.1.2 *Characteristics* — The procedure used for evaluating the tin coating and the general requirements for the coating shall comply with ASTM B 545 or the latest current revision, except where noted below.

5.1.3 *Thickness* — The plated coating as measured on the major flat of the leads shall be a minimum of 5 micrometers (200 microinches).

5.1.4 *Appearance* — The surface texture of the tin shall be non-reflective matte finish.

5.1.5 *Hardness* — None specified.

5.1.6 *Preservation* — Preservation coating, if desired and agreed upon by user and supplier, is acceptable. (Example: Stearic acid solution in xylol as defined in MIL-T-10727.)

5.2 *Tin Lead (SnPb) Electroplate*

5.2.1 *Composition* — Major constituents shall be tin lead with minor impurities. Range of major constituents shall be:

Tin	60%—95%
Lead	5%—40%

5.2.2 *Purity and Application* — Per MIL-P-81728.

5.2.3 *Thickness* — Shall be a minimum of 5 micrometers (200 microinches) measured on the major flat of the leads.

5.2.4 The surface of the tin lead shall be non-reflective matte finish.

5.2.5 *Hardness* — None specified.

5.3 *Tin Lead Solder-Dip*

5.3.1 *Composition* — 60/40 or 63/37.

5.3.2 *Purity* — As per Federal Specification QQ-S-571.

5.3.3 *Thickness* — Shall be a minimum of 5 micrometers (200 microinches) as measured on the major flat of the leads.

5.3.4 *Process Conformance* — Solder coating is applicable as shown in Table 1. In addition, the coating is acceptable as follows:

1. Over the electroplated tin or tin lead as per Section 5.1 or 5.2.
2. Over the electroplated silver as per Section 5.4.
3. Over the electroplated gold as per Section 5.5.

5.3.5 *Appearance* — Surface shall be smooth and continuous.

5.3.6 *Hardness* — None specified.

5.4 *Silver Electroplate*

5.4.1 *Composition* — Silver electroplate shall be semi-bright, Type II as per Federal Specification QQ-S-365, Grade B, (without supplementary tarnish resistant treatment).

5.4.2 *Thickness* — Shall be a minimum of 1.25 micrometers (50 microinches) as measured on the major flat of the leads, in accordance with SEMI G56.

5.4.3 *Appearance* — Smooth and continuous and semi-bright with minimum discoloration as measured, in accordance with SEMI G55.

5.4.4 *Hardness* — Hardness shall be between 90 and 135 on the Brinell Hardness Scale, in accordance with ASTM E 10.

5.4.5 *Additional Processing*

5.4.5.1 Due to chemical reactions, silver electroplated surfaces should be protected from sulfur and sulfur bearing materials such as note paper, cardboard, and other like materials. Sulfur-free papers shall be used for packing.

5.4.5.2 Prior to shipment to a user, devices with silver electroplated leads shall have the silver removed and replaced with tin lead coated leads, unless accepted by contract.

5.5 *Gold Electroplate*

5.5.1 *Composition* — Gold plating shall be applied in accordance with MIL-G-45204 in any and all of the following grades depending on application.

Type I	- 99.7 Percent minimum
Type II	- 99.0 Percent minimum
Type III	- 99.9 Percent minimum

NOTE 1: Type II is suitable for socketing application only.

5.5.2 *Thickness* — Shall be a minimum of 1.25 micrometers (50 microinches) as measured on the major flat of the leads.

5.5.3 *Appearance* — Appearance of surface shall be smooth and continuous. Attributes and defects are specified in MIL-G-45204 (workmanship paragraph).

5.5.4 *Purity* — Composition limits are as specified in Section 5.5.1 above. Individual metallics in the deposit shall not exceed 0.1%. Metallic hardening agents, purposely added to adjust a plating bath to specified hardness, are not considered as impurities.

5.5.5 *Hardness* — Depending on Type and Application, hardness is specified, using Knoop indenter in the following categories (testing shall be in accordance with ASTM E 384):

Type	*Grade*	*Hardness (Knoop)*
I	A	90 max
	B	91—129
	C	130—200
II	B	91—129
	C	130—200
	D	201 and over
III	A	90 max

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SEMI G21-94
SPECIFICATION FOR PLATING INTEGRATED CIRCUIT LEADFRAMES

1 Preface

1.1 *Purpose* — This specification details the requirements for plating layers on leadframes intended for use in platic semiconductor packages. It is intended as a design guideline.

1.2 *Scope* — The specifications and test procedures detailed in this document apply to all plating applied to the internal section of leadframes. External leadframe finishes are not included.

1.3 *Units* — U.S. Customary (inch-pound) or SI units may be used at the customer's discretion. This specification uses U.S. Customary units as the prime unit.

2 Referenced Documents

2.1 *Applicable Documents* — To avoid conflicts, the order of precedence when ordering plated leadframes shall be as follows:

Purchase Order

Customer's Leadframe Drawing

This Specification

Referenced Documents

Related Documents

2.2 *Referenced Documents*

2.2.1 *SEMI Specifications*

SEMI G4 — Integrated Circuit Leadframe Materials used in the Production of Stamped Leadframes

SEMI G18 — Materials Used in the Production of Etched Leadframes for Semiconductor Devices

SEMI — All leadframe specifications

2.2.2 *ASTM Specifications*[1]

B 847 — Test Method for Measurement of Metal and Oxide Coating Thicknesses by Microscopic Examination of a Cross-Section

B 567 — Method for Measurement of Coating Thickness by the Beta Backscatter Method

B 568 — Method for Measuring Coating Thickness by X-Ray Spectrometry

E 384 — Standard Test Method for Microhardness of Materials

F 1269 — Test Methods for Destructive Shear Testing of Ball Bonds

2.2.3 *Military and Federal Specifications*[2]

MIL-C-14550 — Copper Plating, Electrodeposited

MIL-G-45204 — Gold Plating, Electrodeposited

MIL-T-10727 — Tin Plating, Electrdeposits or Hot Dipped, for Ferrous and Non-Ferrous Metals

MIL-STD-883 — Test Methods and Procedures for Microelectronics

QQ-N-290 — Nickel Plating, Electrodeposited

QQ-S-3651 — General Requirements for Electrodeposited Silver Plating

2.3 *Related Documents*

2.3.1 *Military and Federal Specifications*

MIL-P-81728 — Plating Tin/Lead (Sn/Pb) Electrodeposited

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-202 — Test Methods for Electronic and Electrical Component Parts

MIL-S-19500 — General Specification for Semiconductor Devices

2.3.2 *ISO Standards*[3]

ISO-3497 — Metallic Coating Measurement of Coating Thickness, X-Ray Spectrometry Method

3 Terminology

3.1 *finish (plating)* — The final plating layer.

3.2 *resin bleed-out (die attach)* — The surface creep of a resin used for die attach beyond the outer perimeter of the bulk of the resin (filler). For a given resin formulation, the resin creep may be exacerbated by the micro-structure and cleanliness of the die attach surface.

1 American Society of Testing and Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959

2 Military Standards, Naval Publications and Form Center, 5801 Tabor Ave., Philadelphia, PA 19120

3 ANSI, 1430 Broadway, New York, NY 10018

4 Ordering Information

Purchase orders for material furnished to this specification shall include the following information:

4.1 Leadframe drawing showing the areas to be plated and tolerances for the location.

4.2 *Plating Metal, Type, and Grade* — Underplate and finish plate.

4.3 Plating(s) thickness and tolerance.

4.4 Certification or Test Report requirements.

4.5 Reference to this specification.

4.6 Any additions to or variations from this specification.

5 Materials

5.1 *Base Material* — See SEMI G4 and G18 for leadframe base metal specifications.

5.2 *Underplates* — When underplates are specified, the materials specified in Table 1 shall be used.

Table 1 Underplates

Platings	*Type Grade*	*Specifications*	*Specifications*
Nickel			QQN-290
Copper			MIL-C-14550
Gold	III	A	MIL-G-45204
Silver	I, II, III	B	QQ-S-365

5.3 *Finish/Underplates* — The recommended finish plating options for copper and nickel-iron alloys and the suggested underplates are show in Table 2.

Table 2 Undercoat Finishes

Finish	*Copper Alloys*	*Nickel/Iron Alloy*
Gold MIL-G-45204		
Over Base Material		X
Acceptable Underplate		
Nickel*	X	X
Silver QQ-S-365		
Over Base Material	X	
Acceptable Underplate		
Gold		X
Copper	X	X
Tin MIL-T-10727		
Over Base Material	X	X
Acceptable Underplate		
Nickel	X	X
Copper	X	X
Copper MIL-C-14550		
Over Base Material	X	X
Acceptable Underplate		
Nickel QQN-290		
Over Base Material	X	X
Acceptable Underplate		
Palladium		
Over Base Material		
Acceptable Underplate Nickel	X	X
Copper	X	X

*Copper strike may be used under nickel.

6 Sampling

6.1 The sampling plan shall be agreed between user and supplier.

7 Equipment

7.1 Beta Backscatter system.

7.2 Die Attach equipment.

7.3 Eutectic Die Attach heater block or hot plate capable of 450°C ± 10°C.

7.4 Microscope 10–30× magnification with 45° lighting.

7.5 Micro Cross-Section equipment.

7.6 Toolmaker's Microscope

7.7 Wire Bond equipment

7.8 X-ray Fluorescence system

7.9 Solderability equipment

8 Incoming Inspection

If incoming inspection is performed, materials shall be inspected in the following sequence:

8.1 Visual Inspection

8.2 Surface Finish

8.3 Plating Area and Thickness

8.4 *Plating Quality* — Heat Test and Adhesion Test

8.5 Functional Tests

8.5.1 Die Attach

8.5.2 Wire Bond

8.5.3 Solderability

8.6 Plating Hardness

9 Test Methods

9.1 Visual Inspection

9.1.1 Visually inspect the plated area using a binocular microscope, at 10×–30× magnification for the following rejectable conditions.

9.1.1.1 Any bare spots or missing plating in critical areas as defined by the coined areas or minimum flat wire bond area in the appropriate leadframe specification.

9.1.1.2 Any peeling or blistered plating.

9.1.1.3 Any nodules in critical area as defined in 9.1.1.1.

Note 1: Nodules not exceeding 0.0005" (0.0381 mm) in a surface dimension and 0.0005" (0.0127 mm) in height in non-critical areas are allowed providing there are no more than one per internal lead finger or six (6) per leadframe.

9.1.1.4 Any pits which exceed 0.0003" (0.008 mm) in depth or 0.0005" (0.0127 mm) in a surface dimension in critical areas or 0.001" (0.0254 mm) in depth or 0.002" (0.051 mm) in a surface dimension in non-critical areas.

9.1.1.5 Any scratches or scrapes in the metallization plating which expose underplate or base material.

9.1.1.6 Any scratches or scrapes in critical areas which cause a build up of material in excess of 0.0005" (0.0127 mm) in height.

9.1.1.7 Any foreign material, contamination, oxidation or tarnish.

9.2 *Surface Finish*

9.2.1 The surface finish or brightness shall be inspected according to procedures agreed upon between vendor and customer.

9.3 *Plating Area and Thickness*

9.3.1 *Plating Area*

9.3.1.1 Using a toolmaker's microscope determine if spot plated areas meet the requirements of the leadframe drawing for position and size tolerance.

9.3.2 *Thickness*

9.3.2.1 Plating thickness shall be measured at locations agreed between vendor and customer according to procedures detailed in ASTM B 487, ASTM B 567, or ASTM B 568.

Note 2: Only use ASTM B 487 for thicknesses greater than 100 micro-inches (0.0025 mm).

9.4 *Plating Quality* — Heat Test and Adhesion Test.

9.4.1 *Copper Plate* — Test according to procedures agreed between vendor and customer.

9.4.2 *Gold and Silver Plate*

9.4.2.1 Submit gold plated samples to 450°C + 10°C for two (2) minutes in air on a die attach heater block or hot plate and silver plated samples to 300° C + 10° C with the same conditions.

Note 3: For silver plating thicknesses less than 100 micro-inches (0.0025 mm), heat testing is not valid unless an alternate time and temperature is agreed upon between the vendor and the customer.

9.4.2.2 Visually inspect the plating under the microscope set at 10× magnification for blistering, peeling, and discoloration.

Note 4: For gold plating, discoloration after the heat testing is only allowable if the fold plate thickness is less than 20 micro-inches (508 microns) by design.

Note 5: 30× magnification may be used for confirmation.

9.4.2.3 Place a strip of tape across the plated area. Press firmly with fingertips or another smooth object.

9.4.2.4 Peel the tape quickly off the plated surface. If there is any plating on the tape the component shall be rejected.

9.4.3 *Nickel Plate* — Test according to procedures agreed between vendor and customer.

9.4.4 *Palladium Plate* — Test according to procedures agreed between vendor and customer.

9.4.5 *Tin Plate* — Test according to procedures agreed between vendor and customer.

9.5 *Functional Tests*

9.5.1 *Die Attach*

9.5.1.1 Sample die, using a resin agreed between vendor and customer, shall be attached to plated leadframes.

9.5.1.2 Die shear tests shall be performed per MIL-STD-883, Method 2019 or to a method agreed between vendor and customer.

9.5.1.3 Resin bleed-out shall not exceed 0.010" (0.254 mm).

Note 6: Control samples from a previously accepted leadframe lot shall be tested at the same time, using the same resin batch, for comparison.

9.5.2 *Wire Bond*

9.5.3 Sample leadframes shall be bonded using wire and procedures agreed between vendor and customer.

9.5.3.1 Wires and bonds shall be tested according to MIL-STD-883, Method 2011, and/or ASTM F 1269 by agreement between vendor and customer.

9.5.4 Tin Plate Solderability

9.5.5 The solderability or alloying capability of the tin plate shall be evaluated per procedures agreed between vendor and customer.

9.6 *Plating Hardness*

9.6.1 Where required for verification of results obtained in other tests, the plating hardness shall be measured per ASTM E 384.

10 Certification

10.1 Upon request by the customer in the purchase order, a vendor's certification that the plating was performed and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment. This certification does not remove the vendor's responsibility for discrepant product subsequently found by the customer.

10.2 When certification is requested, the following information shall be supplied as a minimum requirement:

10.2.1 Vendor Name

10.2.2 Purchase Order Number

10.2.3 Vendor Lot Number

10.2.4 Customer Part Number

10.2.5 Plating Type, Grade and Measured Thickness for Under and Finsh Plates

10.2.6 Plating hardness if agreed between vendor and user.

11 Packaging and Marking

11.1 *Packaging*

11.1.1 Shipping containers and materials shall be suitably selected to provide the material with protection from normal transportation damage risks which include crushing, abrasion, spillage, and exposure to moisture and other corrosive gases. The inner packing materials may be further specified by the customer for cleanliness and non-tarnishing issues.

11.2 *Marking*

11.2.1 *Internal Packages* — Each internal package shall be marked as follows:

Vendor's Name

Customer's Part Number

Customer's Order Number

Vendor's Specification Number and Customer's, if appropriate

Manufacturing Lot Number

Quantity

Date of Manufacture

11.2.2 *External Packages*

Customer's Specification Number

Customer's Order Number

Quantity

Shipping Date

Any specific instructions for receiving dock personnel if requested on the purchase order

12 Discrepancy Material

12.1 Material rejected at incoming inspection shall be segregated and tagged as rejectable.

12.2 The vendor shall be informed and the returned goods policy activated.

Note 7: Samples showing the defects shall be identified for the vendor. If the vendor wishes to see the samples before return of the complete shipment, the material shall be stored by the customer in a manner to prevent further damage or deterioration.

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SEMI G22-1296
SPECIFICATION FOR CERAMIC PIN GRID ARRAY PACKAGES

1 Purpose

This specification defines the acceptance criteria for cofired ceramic pin grid array packages.

2 Scope

This specification includes the visual, dimensional, and functional requirements for the ceramics PGA package.

3 Referenced Documents

3.1 *Military Standards*[1]

MIL-G-45204 — Gold Plating, Electrodeposited

MIL-I-23011 — Iron Nickel Alloys for Sealing to Glasses and Ceramics

MIL-PRF-38535 — Integrated Circuits (Microcircuits) Manufacturing, General Specification for

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-STD-1835 — Interface Standard for Microcircuit Case Outlines

MIL-STD-7883 — Brazing

QQ-N-290A — Nickel Plating

3.2 *Other Documents*

ANSI Y14.5[2] — Dimensioning and Tolerancing

JEDEC Pub. No. 95[3] — Registered and Standard Outlines for Semiconductor Devices

4 Terminology

4.1 *blister (bubble) ceramic* — Any separation within the ceramic which does not expose underlying ceramic material.

4.2 *blister (bubble) metal* — Any localized separation within the metallized or between the metallization and ceramic which does not expose underlying metal or ceramic material.

4.3 *braze* — An alloy with a melting point equal to or greater than 450°C.

4.4 *burr* — An adherent fragment of excess parent material, either horizontal or vertical, adhering to the component surface.

4.5 *chip* — A region of ceramic missing from the surface or edge of a package which does not go completely through the package. Chip size is given by its length, width, and depth from a projection of design plan form (Figure 1).

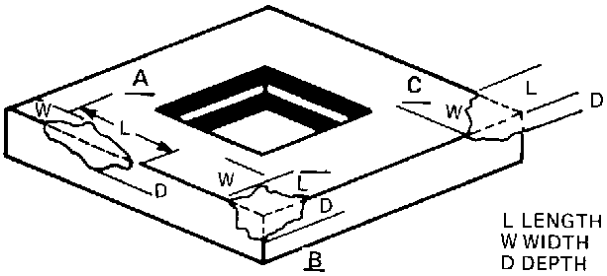

Figure 1
Chip Illustration

4.6 *cofired* — A process or technology for manufacturing products in which the ceramic and refractory metallizations are fired simultaneously.

4.7 *contact pad* — That metallized pattern that provides mechanical or electrical connection to the external circuitry.

4.8 *crack* — A cleavage or fracture that extends to the surface of a package. It may or may not pass through the entire thickness of the package.

4.9 *delamination* — The separation of the individual layers of the ceramic.

4.10 *die attach area* — A dimensional outline designated for die attach.

4.11 *discoloration* — Any change in the color of the package plating or metallization as detected by the unaided eye which normally appears after the application of heat per Section 8.7.1.

4.12 *flatness* — The allowable deviation of a surface from a reference plane. The tolerance zone is defined by two parallel planes within which the surface must lie.

4.13 *footprint* — Pin pattern.

4.14 *foreign material* — An adherent particle other than parent material of that component.

1 Military Standards, Naval Publications and Form Center, 5801 Tabor Ave., Philadelphia, PA 19120

2 ANSI, 1430 Broadway, New York, NY 10018

3 JEDEC, 2500 Wilson Blvd., Arlington, VA 22201-3834

4.15 *isolation gap* — Metal-free space between conductive areas.

4.16 *layer* — A dielectric sheet with or without metallization that performs a discrete function as part of the package.

4.17 *peeling (flaking)* — Any separation of metallization from the base material that exposes the base material.

4.18 *pit* — Any unspecified depression in the package.

4.19 *projection* — An adherent fragment of excess parent material on the component surface.

4.20 *pullback* — A dimension covering the linear distance between the edge of the ceramic and the first measurable metallization (see Figure 2).

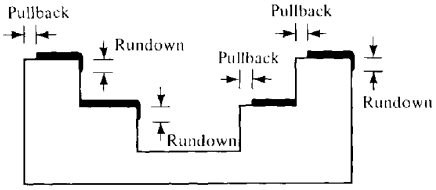

Figure 2
Metallization Misalignment

4.21 *rundown* — The linear distance down a vertical surface from the top to the point of maximum metallization overhang (see Figure 2).

4.22 *seal area* — A dimensional outline area designated for either metallization or bare ceramic to provide a surface area for sealing.

4.23 *seating plane* — As defined by the standoff features or the package base plane if no standoff is used (see Figure 3).

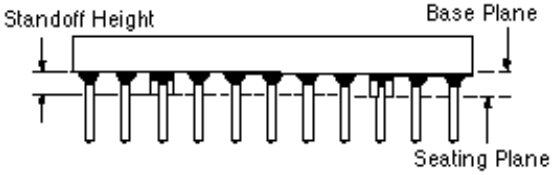

Figure 3
Seating Plane

4.24 *standoff* — The designed separation between the base plane and the seating plane created by a physical feature. Standoff use, configuration, and placement is optional (see Figure 3).

4.25 *terminal* — Metallization at the point of electrical contact to package internal circuitry.

4.26 *TIR* — Total indicator reading.

4.27 *voids* — An absence of refractory metallization, braze, or plating material from a designated area greater than 0.002" (0.051 mm) in diameter.

5 Ordering Information

Purchase orders for pin grid array packages furnished to this specification shall include the following items:

1. Drawing number and revision level
2. Certification requirements
3. Quantity
4. Reference to this document
5. Any exceptions to print or specifications

6 Dimensions and Permissible Variations

The dimensions of the pin grid array package shall conform to the SEMI Standards or to the customer drawing and be within the outline of the appropriate JEDEC standard. Refer to MIL-PRF-38535 and MIL-STD-1835.

7 Material Parameters

The definitions, defects, and functional testing described in this specification relate directly to a nominal package made with the following materials. They may also be applicable to similar pin grid array packages made with other materials.

7.1 *Ceramic Properties*

7.1.1 *Materials* — Alumina content 90% minimum. Beryllia content to be determined.

7.1.2 *Color* — Dark or white.

7.2 *Metal Properties*

7.2.1 Metallized circuits and areas shall be refractory metal tungsten, molybdenum, or an approved equivalent, 0.0003" (0.00762 mm) minimum thickness.

7.2.2 Finish shall be per MIL-PRF-38535 and MIL-STD-1835; Nickel Plating (if designated) shall be per QQ-N-290A, 50 µ"–350 µ" (0.0013 mm–0.00889 mm). Gold plating shall conform to MIL-G-45204, Type III and 50 µ"–225 µ" (0.0013 mm–0.00508 mm).

7.2.3 Braze shall be per MIL-STD-7883.

7.2.4 *Pin Material* — Iron nickel cobalt alloy per MIL-PRF-38535 and MIL-STD-1835, Type A (Kovar). Iron nickel alloy per MIL-PRF-38535 and MIL-STD-1835, Type B (Alloy 42). Phosphor bronze per ASTM B159.

8 Defect Limits

A magnification of 10× to 30× shall be used to inspect the packages unless otherwise specified.

8.1 *Ceramic*

8.1.1 *Cracks* — Per MIL-STD-883, Method 2009.

8.1.2 *Chips* — (See Figure 1.)

8.1.2.1 *Edge* — 0.100" (2.54 mm) length × 0.030" (0.762 mm) width × 0.020" (0.508 mm) (see Figure 1, A).

8.1.2.2 *Corner* — 0.030" (0.762 mm) length × 0.030" (0.762 mm) width × 0.030" (0.762 mm) (see Figure 1, B).

8.1.2.3 Chips cannot encroach upon contact pad or expose any buried metallization.

8.1.2.4 *Seal Area* — 0.060" (1.52 mm) length × 0.020" (0.508 mm) width × 0.020" (0.508 mm) depth maximum.

8.1.2.5 Chips cannot reduce the seal width by more than 1/3 of the design width.

8.2 *Package Flatness* — 0.004 inch/inch (0.004 mm/mm) maximum.

8.2.1 *Seal Area Flatness*

Seal Area Size	*Seal Area Flatness (TIR)*
0.000" – 0.500" (0 – 12.7 mm)	0.002" (0.51 mm) Maximum
0.501" – 0.750" (12.72 – 19.05 mm)	0.003" (0.076 mm) Maximum
0.751" & greater (19.07 mm)	0.004" (0.101 mm) Maximum

8.2.2 *Die Attach Area Flatness*

Die Attach Area Flatness	*Die Attach Area Flatness (TIR)*
0.000" – 0.500" (0 – 12.7 mm)	0.002" (0.051 mm) Maximum
0.501" – 0.750" (12.72 – 19.05 mm)	0.0035" (0.088 mm) Maximum

8.3 *Metallization Voids* — (Voids greater than 0.003" (0.075 mm) should be considered.)

8.3.1 *Seal Area* — Maximum number of three (3) voids per seal ring allowed. The maximum void dimension is 0.010" (0.254 mm) and voids must be separated by a minimum of 0.030" (0.762 mm).

8.3.2 *Wire Bond Finger* — Be free of voids or bare spots in the bonding area as defined by customer drawing.

8.3.3 *Die Attach Area* — Three (3) voids allowed, maximum 0.010" (0.254 mm) diameter voids separated by a distance greater than 0.010" (0.254 mm). Voids within 0.015" (0.381 mm) of die attach cavity wall shall not be considered as the basis for rejection.

8.3.4 *Braze Metallization* — A 0.010" (0.254 mm) maximum diameter void is acceptable, one (1) void per pad.

8.4 *Metallization Misalignment* — (See Figure 2.)

8.4.1 *Metallization Rundown* — Internal cavity not to exceed 0.010" (0.254 mm) maximum.

8.4.2 *Wire Bond Finger Pullback* — 0.010" (0.254 mm) maximum.

8.4.3 *Wire Bond Finger Rundown* — Metallization rundown not to exceed 0.010" (0.254 mm) maximum.

8.4.4 *Pattern Isolation* — Minimum shall not be reduced by more than 50% of the design.

8.5 *Pins*

8.5.1 *Pin Attachment* — The pin must be within the area of the braze pad (fillet seen on all sides). The pin must be located within 0.010" (0.254 mm) radius of true location with respect to all other pins.

8.5.2 Pins that are broken, missing, twisted, or bent more than 30 °.

8.5.3 Pin burrs greater than 0.005" (0.125 mm) in any direction.

8.6 *Plating*

8.6.1 Any visual evidence of plating defects such as blistering, peeling, voids, or stains.

8.6.2 Any plating damage such as scratches or marred areas that expose underlying base metal.

8.7 *Components (General)*

8.7.1 Any visual evidence of corrosion, contamination, or chemical stains on the package component.

8.7.2 Any protrusion, conductive, or non-conductive, that is more than 0.005" (0.125 mm) in height.

9 Sampling

Sampling size must meet the requirements of MIL-STD-105 or MIL-PRF-38535 and MIL-STD-1835, or as agreed to between vendor and customer. Single, double or multiple samples may be used per vendor and customer agreement.

10 Test Methods

10.1 *Mechanical, Electrical, and Thermal Test Methods* — Per MIL-STD-883 unless otherwise noted.

10.1.1 Gold plating and bake test of gold plated package shall be tested by placing parts on a calibrated heater per MIL-STD-883, Method 1008 (excluding temperature).

10.1.1.1 *Condition A* — 450 ± 10°C for two minutes in air, or

10.1.1.2 *Condition B* — 470 ± 10°C for one minute in nitrogen.

10.1.1.3 After cooling at room temperature the packages will be examined for the following criteria:

1. *Blisters* — None allowed at 10× magnification.
2. Any non-uniform color change of the gold at die attach pad. Discolorations within edges up to 0.015" (.381 mm) from the cavity wall is acceptable.
3. Any non-uniform color change of the bonding fingers, seal ring surface, or external pins is not acceptable.
4. There shall be no flaking or peeling of the package plating when viewed at 10x magnification.
5. Superficial stains left during drying or prior operations is not cause for rejection.
6. Plating adhesion tape test.

10.1.2 *Lead Pull* — Under the test condition of five (5) pounds ± one-quarter (1/4) pound pull at an angle of 20° or less from the pins vertical line, measured perpendicular to the package, there shall be no visible separation of the braze joint under 10x magnification. This excludes plating.

10.1.3 *Lead Fatigue* — Test per MIL-STD-883, Method 2004, Test Condition B2, Section 3.1.

10.2 *Functional Test Methods*

10.2.1 *Die Attach Quality* — Destructive die shear test post environmental testing per MIL-STD-883, Method 2019, Paragraph 3.2C.

10.2.2 *Wire Bond Quality* — Minimum pre-seal and post-seal bond strength test per MIL-STD-883, Method 2011, Test Condition D. Reject for bonds which cause plating to lift from the base metal of the bonding fingers or fail to meet minimum strength requirement.

10.2.3 *Solderability* — Test per MIL-STD-883, Method 2003 (omit aging).

10.2.4 *Insulation Resistance* — Test per MIL-STD-883, Method 1003, Condition D.

10.2.5 Hermetic and Environmental Testing per MIL-STD-883.

10.2.5.1 The hermetic integrity of the package must be maintained after all environmental testing. Hermetic checks shall comply with MIL-STD-883, Method 1014, Test Conditions A, B, C, or D.

10.2.5.2 Environmental testing shall include but not be limited to the following:

1. *Temperature Cycle* — MIL-STD-883, Method 1010, Condition C without heat sink; Condition B with heat sink.
2. *Thermal Shock* — MIL-STD-883, Method 1011, Condition C without heat sink; Condition B with heat sink.
3. *Centrifuge* — MIL-STD-883, Method 2001, Condition E. Y1 axis only — cavity up; Y2 axis only — cavity down (optional).
4. *Mechanical Shock* — MIL-STD-883, Method 2002, Condition B.
5. *Vibration* — MIL-STD-883, Method 2007, Condition A.

NOTE 1: Package applications requiring a heat sink attach will require the environmental test requirements (temp. cycle, shock, etc.) to be evaluated on an individual basis. The material, form factor, and method of attach used for heat sinks may result in severe stresses being induced on the package assembly during environmental testing. Actual accelerated test requirements should be based on the expected product application environment and may be less rigorous than those tests for packages without heat sinks.

11 Sequence of Events and Incoming Testing

During incoming inspection the sequence of testing shall be:

A. Visual

B. Dimensional

C. Functional (typical functional tests which may be applied):

Die Attach

Wire Bond

Pre-seal wire pull

Seal

Heat sink attach (if applicable)

Environmental Test

Fine Leak — MIL-STD-883, Method 1014, Condition B

Gross Leak — MIL-STD-883, Method 1014, Condition C

Post-Seal Bond Pull

Radiography

Die Shear — MIL-STD-883, Method 2019

Solderability — MIL-STD-883, Method 2003

NOTE 2: An initial vendor qualification may be performed on the thermal and electrical characteristics of the package. The characteristics tested will be:

Insulation Resistance — MIL-STD-883, Method 1003, Test Condition D.

Thermal Dissipation — MIL-STD-883, Method 1012.

12 Packaging and Marking

12.1 *Packaging* — Containers selected shall be strong enough and suitably designed to provide maximum protection against crushing, spillage, and other forms of damage to the container or its contents to contamination from exposure to excessive moisture or oxidation by gases. Packaging materials shall be so selected to prevent any contamination of the ceramic components parts with fibers or organic particles.

12.2 *Marking* — The outer containers shall be clearly marked identifying the customer part number, customer purchase order number, drawing number (optional), quantity, date, and vendor lot number (optional).

SEMI G23-0996
TEST METHOD FOR INDUCTANCE OF INTERNAL TRACES OF SEMICONDUCTOR PACKAGES

NOTE: This entire document was revised in 1996.

1 Purpose

This test method describes the measurement method for the inductance of internal traces of semiconductor packages.

2 Scope

2.1 This test method is applicable for the measurement of package inductance that is greater than 0.5 nH.

2.2 This document describes the measurement of a pin grid array, one of the package types, as a sample.

2.3 This test method is also applicable to other types of packages.

2.4 The inductance in this document is limited to that of internal traces only and does not contain the portions contributed by the exposed areas such as pins and wires.

2.5 This document uses SI units.

3 Limitation

It is not practical to apply this test method for fine-pitch packages where traces or pads (point A of Figure 1) cannot be connected to with two probes.

4 Referenced Documents

None.

5 Terminology

5.1 *internal inductance (of packages)* — Inductance of the circuit that comprises the signal path starts from the shoulder or in the center of the outside lead (point A of Figure 1) and ends at the end of the lead on the cavity side of the lead (point B of Figure 1). The return path is made by tying all other traces (except for the target trace in the same electric potential) together. The target trace is tied to the return path at the bonding finger (see Figure 2).

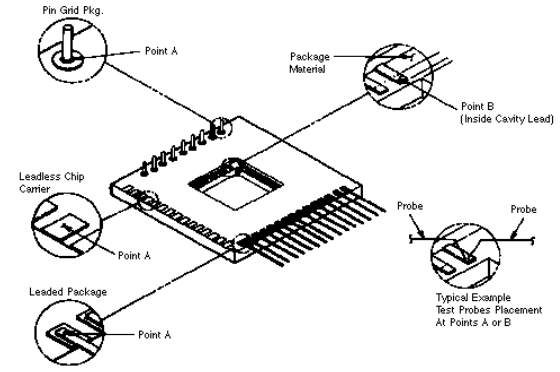

Figure 1
Internal Inductance Measurement

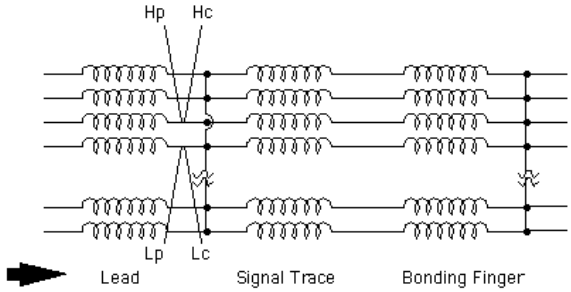

Figure 2
Concept of Internal Inductance

5.2 *four-point probe* — The probe consists of four coaxial measuring terminals, H_c (current high), H_p (potential high), L_c (current low) and L_p (potential low), to measure impedance. Independent coaxial cables are used between the package being measured and the measurement instrument to minimize the effect caused by mutual inductance (between terminals) and/or interferences from the measured signals (see Figures 3 and 6).

6 Summary of Method

Fabricate the package to be measured. Then measure the inductance of internal traces using the four terminal probe method.

7 Interference

7.1 It is desirable that an operator who is familiar with the measuring system, measuring method, and

principles, conduct the actual measurement to get the best result.

7.2 To get an accurate measurement, maintain equal probe angle and distance.

8 Apparatus

8.1 *LCR Meter*

8.1.1 Four terminal probe attachment capability

8.1.2 Capable of measuring at the frequency of 10 MHz or higher

8.1.3 Measurement error of less than 0.1 nH for the measurement range more than 1 nH at the measurement frequency

8.2 *Four Terminal Probe* — See Figure 3.

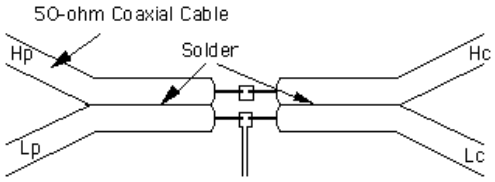

Figure 3
Configuration of Four Terminal Probe

8.2.1 *Residual Inductance* — less than 1 nH

9 Material

9.1 *Copper Plate*

9.1.1 *Plating* — gold

9.1.2 *Thickness* — 2 mm or thicker

9.2 *Insulator* — such as Teflon

9.3 *Silver Foil*

9.3.1 *Thickness* — around 50 µm

9.4 Solder or Conductive Paste

9.4.1 *Resistivity* — 10^{-4} Ω · m or less

10 Test Specimens

10.1 *Preparation of Sample* — Conduct the circuit by measuring the trace as a signal path and the rest, which has a different potential from this signal path, will be the return path, as follows:

10.1.1 All the bonding fingers shall be soldered or pasted together at the bond finger area to form a short circuit.

NOTE 1: The short circuit area shall be 0.5 mm from the tip of the bond fingers. The entire bond fingers shall not be short circuited (see Figure 4).

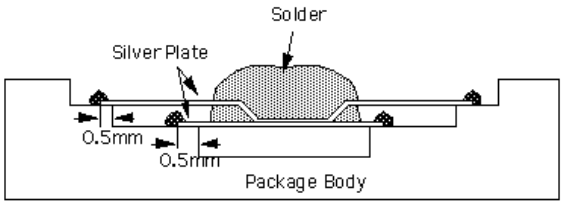

Figure 4
Sample Preparation (Part of Bonding Finger)

10.1.2 Short all pins or leads except for the ones with the same potential as the trace being measured.

NOTE 2: The location for the short circuit shall be as close as possible to the bottom of the pins or the braze pad of the leads to minimize the inductance caused by the pins or leads.

NOTE 3: In case of Pin Grid Array packages, it is recommended to press 50 µm thickness silver foil, which is the same size of package, through the pins. In case of Flat Packages, it is recommended to solder silver foil (or a copper foil) at the braze pads of the leads.

11 Preparation of Apparatus

Before starting the measurement, warm up the instruments as specified in the manual.

12 Calibration

Before starting the measurement, calibrate the instruments as specified in the manual.

13 Procedures

13.1 *Measurement of Residual Inductance*

13.1.1 Set the LCR meter to the inductance measurement mode.

13.1.2 Measure the inductance by conducting the four terminal probe on the gold plated copper plate as shown in Figure 5.

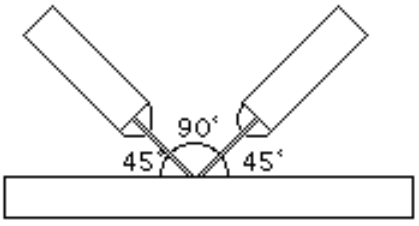

Figure 5
Measurement of Residual Inductance

NOTE 4: The angle between the potential terminal probe and the current terminal probe has to be maintained at a right angle (90°). This is to nullify the mutual interference caused by the magnetic flux.

13.2 *Measurement of the Resultant Inductance*

13.2.1 Place the sample on the insulator such as Teflon.

13.2.2 Set the probe at the bottom of the pin of the trace being measured and at the closest traces belonging to the short circuit as shown in Figure 6.

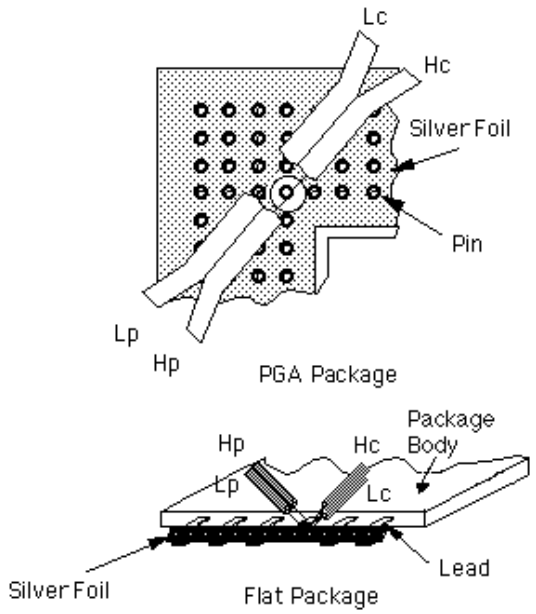

Figure 6
Probing Method

NOTE 5: The probes H_p and H_c are attached/placed onto the pins to be measured and the probes L_p and L_c are attached/placed onto the short circuit.

14 Calculation

14.1 The inductance of the internal trace is calculated as follows:

Internal Inductance (nH) = Measured Inductance — Residual Inductance

14.2 Round the second digit after the decimal point to the unit of 0.1 nH.

15 Report

The following information shall be reported:

- Brief description of the package
- Measurement instrument or system
- Measurement frequency
- Measurement pin numbers
- *Inductance* — Raw data as well as the average in case of multiple measurements.

16 Accuracy

Using the same samples, four different packaging manufactures were tested. The following results were obtained:

Repeatability — ± 0.2 nH

Reproductibility — ± 0.5 nH

17 Related Documents

SEMI G24 — Test Method for Measuring the Lead-to-Lead and Loading Capacitance of Package Leads

SEMI G25 — Test Method for Measuring the Resistance of Package Leads

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SEMI G24-89
TEST METHOD FOR MEASURING THE LEAD-TO-LEAD AND LOADING CAPACITANCE OF PACKAGE LEADS[1]

1 Purpose

This document defines the equipment, materials, and procedures used to measure the lead-to-lead and loading capacitance of package leads. Semiconductor packages are shown as examples; however, other packaging elements can be measured by this method.

2 Equipment and Materials

2.1 Capacitance meter which uses a two probe plus guard method with two coax cables, or a meter which utilizes a four probe plus guard method. The four probe method requires four cables to be modified to connect to two probes at the probe end of the cables. Both methods require an 18 awg. or larger insulated wire for the guard connection. Keep cables at minimum length (1 meter) unless specified by individual equipment. Coaxial cables must be used to connect the probes to the meter. Meter accuracy ± 2%. The probe shields must be connected together. This connection should be short, approximately one to two inches.

2.2 Probe station with two coax probes and one regular probe. Recommendation: Micromanipulator, two (2) each coax probe model 44-FPC-6000 with #5 collet, and one each OON-FPC-6000 with #3 collet, or equivalent.

3 Procedure: Lead-to-Lead Capacitance(See Figure 1)

3.1 Set the instrument to measure at 1 Mhz. If the equipment has a cable length selection switch, adjust the switch to the appropriate coax cable length.

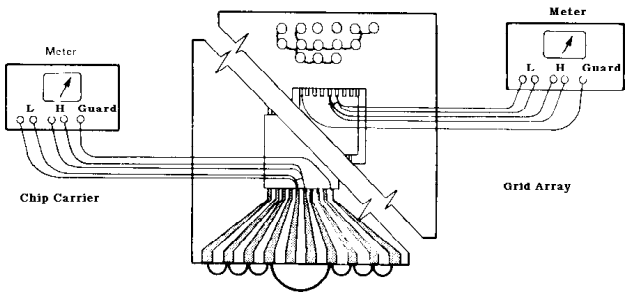

Figure 1
Lead-to-Lead Capacitance

3.2 Connect together all the pins in close proximity to those being measured, for multi-layer ceramic package pins should be chosen to connect all traces adjacent to traces being measured. Example: Eight surrounding pins are connected for the 68 lead pin grid; twelve surrounding pins are connected together for the 124 pin grid; eight surrounding pins are connected together for all flat packs (see Figure 1). If there are power planes and/or large power buses in the package, their pins must be connected together with the eight or 12 surrounding pins discussed above.

3.3 Place the guard probe down on the cavity side of any one of the eight or 12 leads discussed in Section 3.2, to ensure that they will not affect the measurement.

3.4 Place one coaxial probe approximately 1/8 inch above the cavity side of one of the leads to be measured.

3.5 Place the other coaxial probe approximately 1/8 inch above the cavity side of the other lead to be measured.

3.6 *Nulling Procedure* — If using an instrument that auto-zeros, such as the H.P.4275A, follow the instrument instructions for capacitance measurement. If this type of instrument is not being used, take the reading on the instrument at this point.

---

1 This test method applies to measurements in the range of 1 to 100 pico farands.

3.7 Place the probes down on the leads to be measured. This should be a vertical movement only.

3.8 Take the capacitance reading. If using auto-zeroing equipment, this capacitance measurement will be used. If not, take the reading from 3.6 and subtract it from the reading in 3.8 to derive the capacitance measurement of interest. (See Table 1.)

Table 1 Capacitance Nulling Procedurefor Non-Zeroing Equipment

Pins to be Measured	*Capacitance Reading at 3.6*	*Capacitance Reading at 3.8*	*Subtraction Step to Derive Desired Capacitance at 3.9*
1 & 2	C_1	C_2	$C_2–C_1 = C_3$
3 & 4	0.050 pf	2.130 pf	2.130–0.050 = 2.080 pf

For Auto-Zeroing Equipment:

Pins to be Measured	*Capacitance Reading at 3.6*	*Capacitance Reading at 3.8*	*Subtraction Step to Derive Desired Capacitance at 3.9*
5 & 6	C_1	C_2	$C_2–C_1 = C_3$
7 & 8	0.00 pf*	2.08 pf	2.080–0.000 = 2.080 pf

*Follow instrument instructions to read 0.00 pf

3.9 Repeat the procedure as required.

4 Procedure: Loading Capacitance (See Figure 2)

4.1 Omit guard terminal. Connect together all the pins in close proximity to the one to be measured. Example: Eight surrounding pins are connected together for the 68 pin grid; twelve surrounding pins are connected together for the 124 pin grid; eight surrounding pins are connected together for all flat packs (see Figure 2). If there are power planes and/or large power buses in the package, their pins must be connected together with the eight or 12 surrounding pins discussed above.

4.2 Place one coaxial probe approximately 1/8 inch above the cavity side of any one of the eight or 12 leads discussed in Section 4.1.

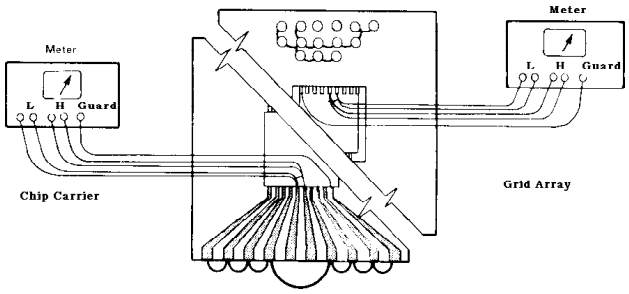

Figure 2
Loading Capacitance

4.3 Place the other coaxial probe approximately 1/8 inch above the cavity side of the lead to be measured.

4.4 Continue as in Steps 3.6 to 3.9.

4.5 Overall accuracy with this method is ± 5%.

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SEMI G25-89
TEST METHOD FOR MEASURING THE RESISTANCE OF PACKAGE LEADS

1 Purpose

This document defines the equipment, materials, and procedure used to measure the resistance of leads in packaging elements. This document uses a pin grid (cavity down) package as one example of the type of packaging element that can be measured with the method described herein; however, this measurement technique can be applied to other geometrics with proper consideration.

2 Equipment and Materials

2.1 D.C. Ohmmeter which uses the four point probe (Kelvin) method with four cables. Minimum accuracy should be ± 4 mΩ.

2.2 Probe station with four probes. Probes should be such that the taper of the probe and the diameter of its point allow two probes to come together within a 5 mil. square without touching each other elsewhere. Recommendation: Micromanipulator, four each, probe number OON-FPC-6000 with #3 collet or equivalent.

3 Procedure

3.1 Place both probes of the low side of the meter as close together as possible on the shoulder or in the center of the outside lead (see Figure 1, Point A).

3.2 Place both probes of the high side of the meter within 5 mils of the end of the lead on the cavity side of the lead (see Figure 1, Point B).

3.3 Set the ohmmeter scale to the lowest setting possible without putting meter in an "over range" mode.

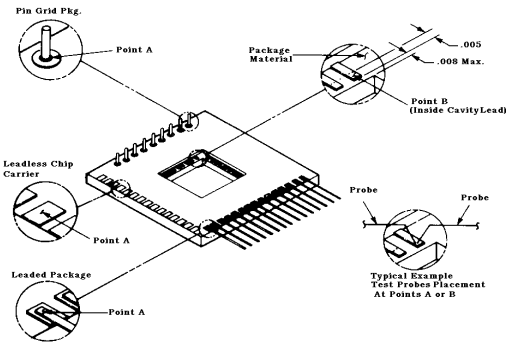

Figure 1
Resistance Measurement

3.4 Take resistance reading. Overall accuracy with this method is ± 20 mΩ. This accuracy estimate includes basic instrumentation error, probe placement repeatability, and typical package construction (printed pattern accuracy).

4 Application Note

Readings below 100 mΩ can be made with acceptable reeatability if considerable care in pleacement is taken. For example, in measuring a conductor made of tungsten 0.010" wide, a 0.010" variation in the distance between the two sets of probes will result in a 15 mΩ change in the measured reading. The same variation in a gold conductor would result in a 3–5 mΩ error.

SEMI G26-90
SPECIFICATION FOR HERMETIC SLAM CHIP CARRIER LIDS

1 Preface

This specification covers the ceramic piece part commonly referred to as a lid, used in the construction of a hermetic SLAM package with a .050" pad centerline. The SLAM package is covered separately in the SEMI G5 Specification for Ceramic Chip Carriers.

2 Applicable Documents

MIL-STD-883[1] — Test Methods and Procedures for Microelectronics

MIL-M-38510 — General Specification for Microcircuits

MIL-I-23011 — Iron Nickel Alloys for Sealing to Glass and Ceramic

3 Selected Definitions

burr — A fragment of excess material or foreign particle adhering to the surface.

chip — Region of ceramic missing from the surface or edge of a package which does not go completely through the package. Chip size is given by its length, width and depth from a projection of the design plan-form (see Figure 1).

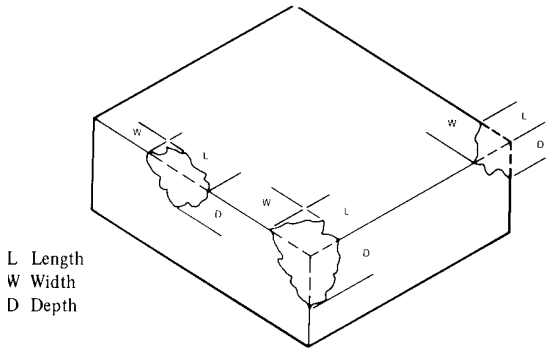

Figure 1
Chip Illustration

crack — A cleavage or fracture that extends to the surface of a package. It may or may not pass through the entire thickness of the package.

fin — A fine, feathery-edged projection on the edge or corner of the ceramic.

glass flow — Heated just sufficiently to remove all screen mesh marks visible at 10× magnification.

overhang — Horizontal extension of glass from the ceramic.

projection — Raised portion of the surface indigenous with the parent material.

pullback — Defines a dimension covering the linear distance between the edge of the ceramic and the first measurable glass interface excluding any glass spatter (see Figure 2).

rundown — Vertical extension of glass from the ceramic (see Figure 2).

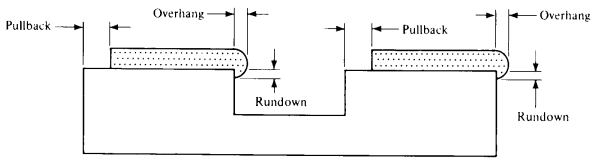

Figure 2
Glass Misalignment

seal area — A dimensional outline area designated for sealing the lid and package together.

terminal — Case outline at point of entry or exit of an electrical contact.

void —An absence of glass from a designated glassed area on the ceramic surface.

4 Ordering Information

Purchase orders for SLAM lids furnished to this specification shall include the following items:

1. Drawing number and revision level
2. Type and color of ceramic
3. Type and thickness of sealing material
4. Length, width, thickness and sealing area
5. Certification
6. Method of test and measurements (see Section 9)
7. Lot acceptance procedures (see Section 8)
8. Packaging and marking (see Section 10)

1 Military Standards, Naval Publications and Form Center, 5801 Tabor Ave., Philadelphia, PA 19120

5 Dimensions and Permissible Variations

The lid dimensions shall conform as specified in Figure 3 and Table 1.

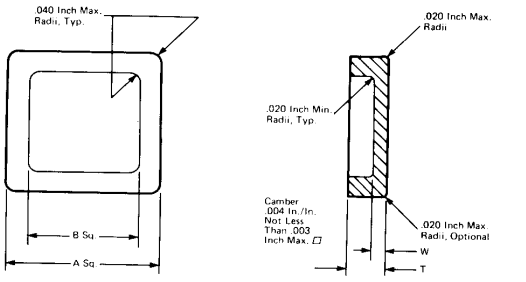

Figure 3
Dimensions

Table 1 Lid Dimensions for 0.050" Pad Centerline

Terminals	*Chip Carrier Base Thickness (Reference)*	*DIM A*	*DIM B*	*DIM T*	*DIM W*	*S/R, WIDTH*
20	0.020	0.310	0.230	0.060	0.020	0.040
28	0.025	0.410	0.330	0.060	0.025	0.040
44	0.040	0.500	0.420	0.065	0.025	0.040
68	0.040	0.700	0.560	0.065	0.022	0.070

6 Materials

6.1 Ceramic

6.1.1 Alumina content 90% minimum or Beryllia content 94% minimum.

6.1.2 Dark or white.

6.2 *Sealing Material* — As specified in the ordering information.

7 Defect Limits

7.1 *Ceramic*

7.1.1 *Cracks* — Cracks are not allowed.

7.1.2 *Chips*

7.1.2.1 *Corner* — 0.762 mm × 0.762 mm × 0.762 mm (0.030" × 0.030" × 0.030").

7.1.2.2 *Edge* — 0.762 mm × 0.762 mm × 0.762 mm (0.030" × 0.030" × 0.030").

7.1.2.3 Chips cannot reduce the seal path by more than 0.381 mm (0.015") or 10%, whichever is smaller.

7.1.3 *Burrs, Projections, and Fins* — Lids — 0.127 mm (0.005") maximum.

7.1.4 *Camber* — 0.004 inch/inch. For sizes below one inch the maximum camber shall be 0.076 mm (0.003").

7.2 *Glass*

7.2.1 *Chips or Voids* — There shall be no chips or voids after glass flow test.

7.2.2 Glass Misalignment — (As received.)

7.2.2.1 *External Overhang* — 0.254 mm (0.010") maximum.

7.2.2.2 *External Rundown* — 30% of ceramic thickness maximum at maximum material condition.

7.2.2.3 *Glass Pullback* — 0.254 mm (0.010") maximum.

7.2.2.4 Regardless of maximum allowable criteria stated above, the seal area must not be reduced by greater than 20% of the nominal design width.

7.2.3 Glass thickness shall be measured in four locations. Measurement shall be made on glass and base total thickness. Base reference thickness shall be measured on the same part by removal of a portion of the glass.

7.2.4 Glass splatter in all areas may not exceed 0.052 mm (0.002") in height, 0.127 mm (0.005") in diameter, with a maximum of three per 0.1" square area on the cavity surface.

8 Sampling

Sampling will be determined between supplier and purchaser.

9 Test Methods

9.1 *Sequence of Events and Functional Testing* — During functional testing, the sequence of testing shall be:

1. Seal
2. Vapor Content
3. Environmental Testing
4. Fine Leak
5. Gross Leak
6. Torque Test

9.2 *Hermetic and Environmental Testing*

9.2.1 The hermetic integrity of the package must be maintained after all environmental testing. Hermetic checks shall comply with MIL-STD-883, Method 1014, Test Conditions A_1, or B and C.

9.2.2 Environmental testing shall include: Temp Cycle, MIL-STD-883, Method 1010, Condition C.

10 Packaging and Marking

10.1 *Packaging* — Containers selected shall be strong enough and suitably designed to provide maximum protection against crushing, spillage and other forms of damage to the container or its contents. Containers shall afford protection of the contents to contamination from exposure to excessive moisture or oxidation by gases. Packaging materials shall be so selected to prevent any contamination of the ceramic component parts with paper fibers or organic particles.

10.2 *Marking* — The outer containers shall be clearly marked to identify the user stock number, user purchase order number, drawing number, quantity, vendor lot number, and solder glass type.

SEMI G27-89
SPECIFICATION FOR LEADFRAMES FOR PLASTIC LEADED CHIP CARRIER (PLCC) PACKAGES

1 Preface

This specification is a guideline for high volume production of leadframes for plastic leaded chip carrier semiconductor packages. It is a design guideline for packaging engineers, leadframe stampers and mold manufacturers, and has been developed to meet the requirements of automatic assemblers.

2 Applicable Documents

2.1 *Order of Precedence* — To avoid conflicts, the order of precedence when ordering leadframes to this specification shall be as follows:

Purchase Order

This Specification

Referenced Documents

2.2 *SEMI Specifications*

SEMI G4 — Specification for Integrated Circuit Leadframe Material

SEMI G10 — Standard Method of Mechanical Measurement for Leadframes

SEMI G18 — Specification, Integrated Circuit Leadframe Materials Used in the Production of Etched Leadframes

SEMI G21 — Specification, Plating Integrated Circuit Leadframes

2.3 *Military and Federal Specifications*[1]

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

2.4 *ANSI Specification*[2]

Y14.5M — Dimensioning and Tolerancing

2.5 *JEDEC Publication*[3]

Publication 9b — Registered and Standard Outlines for Semiconductor Devices

1 Military Standards, Naval Publications and Form Center, 5801 Tabor Avenue, Philadelphia, PA 19120

2 ANSI, 1430 Broadway, New York, NY 10018

3 JEDEC, 20001 Eye Street N.W., Washington, D.C. 20006

3 Selected Definitions

burr — a fragment of excess material either horizontal or vertical attached to the leadframe.

camber — curvature of the leadframe strip edge (see Figure 1).

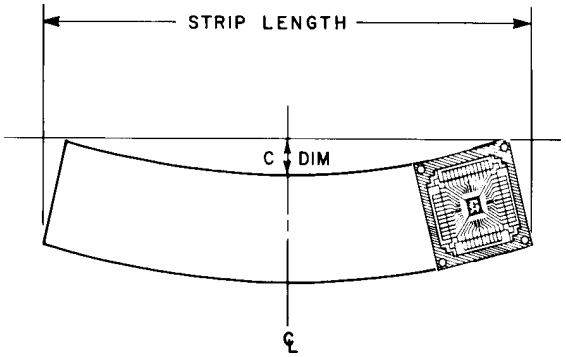

Figure 1
Camber

coil set — longitudinal bowing of the leadframe (see Figure 2).

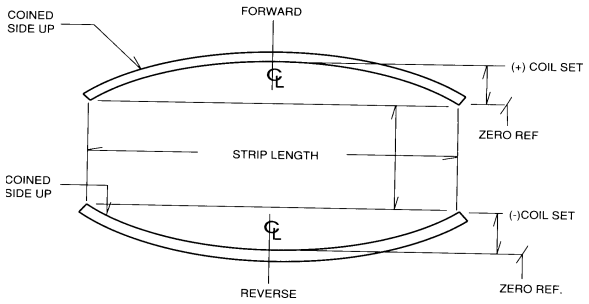

Figure 2
Coil Set

coined area — that area at the tip end of the bond fingers coined to produce a flattened area for functional use (see Figure 3).

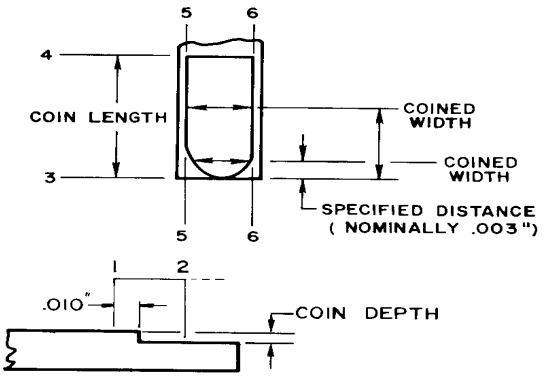

Figure 3
Coined Area

crossbow — transverse bowing of the leadframe (see Figure 4).

functional area — the die attach pad and the lead tips.

lead twist — angular rotation of bonding fingers (see Figure 5).

pits — shallow surface depression or craters in the leadframe material.

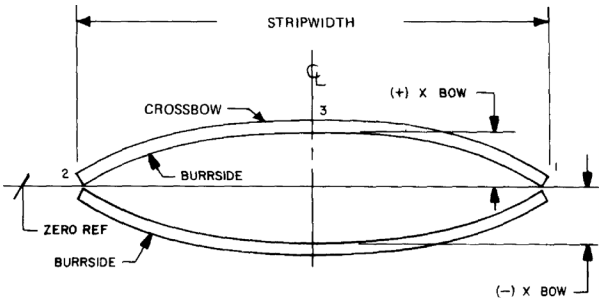

Figure 4
Crossbow

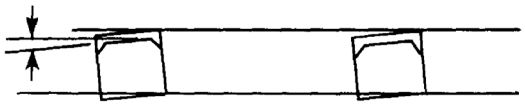

Figure 5
Lead Twist

slug marks — random dents in the leadframe caused by foreign material in the stamping die.

stamped leadframe terminology — (See Figure 6.)

true position circle — the circle with its center positioned at the center of the coined lead which defines the design position of the lead tip.

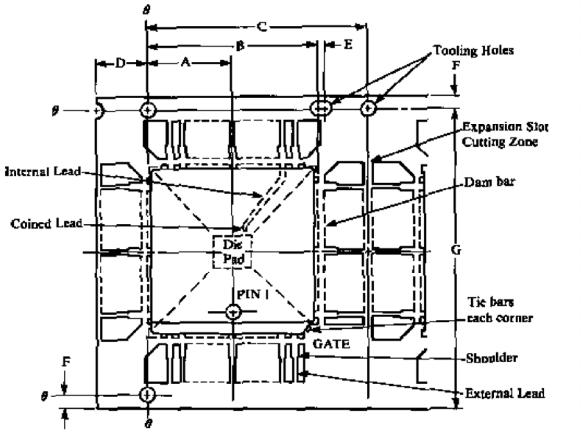

Figure 6
Plastic Leaded Chip Carrier Leadframe

4 Ordering Information

4.1 Purchase orders for leadframes furnished to this specification shall include the following information:

4.1.1 Current revision of the leadframe drawing detailing the base material and the plating type(s), thickness(es) and area(s).

4.1.2 Reference to this specification.

4.1.3 Vendor certification requirements.

5 Dimensions

See Table 1.

6 Defect Limits and Parameters

Note: Measurement methods are described in SEMI G10. Alternate methods may be used as agreed to between vendor and customer. The methods described in SEMI G10 are considered to be standard for the purpose of solving differences.

6.1 *Dimensional Tolerances* — See Figure 6.

6.2 *Minimum Flat Wire Bonding Area* — 80% of nominal lead width and 0.635 mm (0.025") in length.

6.3 *Coined Depth* — 0.013 mm (0.0005") min. to 30% of material thickness maximum.

6.4 *Horizontal Lead Spacing and Location (Lead Tips)*

6.4.1 The lead spacing and lead location that can be maintained is a function of the designed lead spacing and lead width.

Design Lead Width	*Design Lead Space*	*Minimum Lead Sapce*	*Minimum True Position Circle Dia.*
≥ 0.011"	≥ 0.011"	0.006"	0.007"
0.010"	0.010"	0.005"	0.006"

Tolerances for lead designs smaller than .010" should be negotiated between vendor and user.

6.4.2 *18 - 100 Pin Lead Frames* — Leads to be located so that a 0.007" diameter circle centered on the nominal center of the coined lead in width and 0.152 mm (0.006") back from lead tip in length shall be totally encompassed by the coined area.

Table 1 Plastic Leaded Chip Carrier Leadframe Standard Dimensions (all dimensions in inches)

LEAD COUNT	*18 LD*	*18 LD*	*20 LD*	*28 LD*	*28 LD*	*32 LD*	*44 LD*	*52 LD*	*68 LD*	*84 LD*	*100 LD*	*100 LD*
PACKAGE SHAPE	Rect.	Rect. Stretch	Square	Square	Rect.	Rect.	Square	Square	Square	Square	Square	Square
JEDEC PACKAGEDESIGNATION	AA	AB	AA	AB	AD	AE	AC	AD	AE	AF		
Nominal Pkg. Width	0.290	0.290	0.350	0.450	0.350	0.450	0.650	0.750	0.950	1.150	1.350	1.150
Length	0.425	0.490	0.350	0.450	0.550	0.550	0.650	0.750	0.950	1.150	1.350	1.150
PROGRESSION	0.720	0.720	0.780	0.880	0.780	0.880	1.080	1.180	1.400	1.600	1.800	1.600
STRIP WIDTH	0.970	1.230	0.970	1.070	1.230	1.230	1.230	1.430	1.670	1.870	2.070	1.870
TOOLING DIMENSIONS (See Figure 6)												
A	0.170	0.170	0.200	0.250	0.200	0.250	0.350	0.400	0.500	0.600	0.700	0.600
B	0.340	0.340	0.400	0.500	0.400	0.500	0.700	0.800	1.000	1.200	1.400	1.200
C	0.530	0.530	0.590	0.690	0.590	0.690	0.890	0.990	1.200	1.400	1.600	1.400
D	0.190	0.190	0.190	0.190	0.190	0.190	0.190	0.190	0.200	0.200	0.200	0.200
E	0.020	0.020	0.020	0.020	0.020	0.020	0.020	9.020	0.020	0.020	0.020	0.020
F	0.050	0.050	0.050	0.050	0.050	0.050	0.050	0.050	0.050	0.050	0.050	0.050
G	0.920	1.180	0.920	1.020	1.180	1.180	1.180	1.380	1.620	1.820	2.020	1.820
Diameter	0.060	0.060	0.060	0.060	0.060	0.060	0.060	0.060	0.060	0.060	0.060	0.060
Metal Thickness	0.010	0.010	0.010	0.010	0.010	0.010	0.010	0.010	0.008	0.008	0.008	0.008

Note 1: Gate — All packages; gate on the corner counter-clockwise from pin one.

Note 2: Dam Bar — Recommend 0.025 wide with 0.025 space between package and dam bar.

Note 3: Lead shall meet the JEDEC Quad Package requirements.

6.5 *Horizontal Die Attach Pad Location* — Die attach pad shall be located within 0.051 mm (± 0.002") on 18-100 pin leads.

6.6 *Lead Twist* — Shall not exceed 3° 30' or 0.015 mm (0.0006") per 0.254 mm (0.010") of lead width.

6.7 *Die Attach Pad Tilt and Flatness*

6.7.1 *Tilt* — 0.025 mm (0.001") maximum per 2.54 mm (0.100") of length or width in the undepressed state. 0.051 mm (0.002") maximum per 2.54 mm (0.100") of length or width in the depressed conditions when measuring from corner to corner.

6.7.2 *Flatness* — 0.005 mm (0.0002") per 0.100" pad length on 18-100 pin leadframes when measuring from the center to the average of the four corners. The corners are defined at 0.127 mm (0.005") from each edge.

6.8 *Die Attach Pad Downset or Depression* — The nominal downset recommended is 0.015" (0.381 mm) ± 0.002".

6.9 *Lead and Die Attach Pad Coplanarity*

6.9.1 *Lead Planarity* — The lead tips shall be within the following tolerances of the Z plane in the taped or untaped condition.

Table 2 Taped or Untaped Condition

No. of Leads	*Strip Width*	*Lead Tip Coplanarity*
18 Rect.	1.070" - 1.230" (27.18 mm - 31.24 mm)	± 0.003" (0.76 mm)
20 Square	0.970" (24.64 mm)	± 0.003" (0.076 mm)
28-52	1.070" - 1.470" (27.18 mm - 37.34 mm)	± 0.004" (0.120 mm)
64-84	1.670" - 1.870" (42.42 mm - 47.50 mm)	± 0.005" (0.127 mm)

6.9.2 *Die Attach Pad Planarity* — The die attach pad shall be within the following tolerances of the Z plane.

6.10 *Material*

6.10.1 0.203 mm (0.008") material thickness recommended for greater than 52 leads.

6.10.2 0.254 mm (0.010") material thickness recommended for 52 lead and below.

6.10.3 Nominal thickness tolerances for both Alloy 42 and copper materials of 0.203 mm (0.008") and 0.254 mm (0.010") shall be 0.008 mm (± 0.0003").

6.10.4 *Width Tolerance* — 0.051 mm (± 0.002") for both Alloy 42 and copper.

6.11 *Coil Set* — Maximum of 0.508 mm (0.020") over the nominal strip length. Does not include material thickness.

6.12 *Crossbow* — Crossbow shall not exceed the following dimensions:

No. of Leads	*Maximum Crossbow*
18—20	± 0.005" (0.127 mm)
28 - 52	± 0.006" (0.152 mm)
68 - 84	± 0.010" (0.254 mm)

6.13 *Camber* — Shall not exceed 0.002" over nominal strip lengths of 8 ± 2 inches.

The relationship to determine maximum camber for other lengths is approximated as follows:

$$\frac{C_1}{C_2} = \frac{L_1^2}{L_2^2}$$

6.14 *Progression* — The progression over the nominal strip length shall be within 0.051 mm (± 0.002") and noncumulative.

6.15 *Burrs* — Shall be firmly attached and able to withstand a probe force of 10 grams. Vertical burrs inside the dambar shall not exceed 0.025 mm (0.001"). Vertical burrs outside the dambar and horizontal burrs in any location shall not exceed 0.051 mm (0.002").

6.16 *Pits and Slugmarks*

6.16.1 Within functional area and on external leads, there shall be no slugmarks. Pits shall not exceed 0.008 mm (0.0003") in depth and 0.013 mm (0.0005") in largest surface dimension in these areas.

APPLICATION NOTE: There is a question regarding the ability of material suppliers to meet this specification. Revision of this specification is under review.

6.16.2 In other areas, pits and imperfections shall not affect leadframe strength regardless of size and shall not exceed 0.051 mm (0.002") in depth and 0.127 mm (0.005") in largest surface dimension.

6.17 *Strip Cut Off Location* — Strip cut off shall be within 0.076 mm (± 0.003") of basic strip length (see Figure 6).

6.18 *Coining and Metal Clearance*

6.18.1 Dimensions shown on drawings are before coin dimensions.

6.18.2 Maximum coining bulge shall not exceed 0.051 mm (0.002") per edge and shall be governed by metal to metal clearance requirements (lead to lead and lead to pad).

6.18.3 *Metal to Metal Clearance* — Shall be as agreed to between vendor and customer.

7 Sampling

7.1 The sampling plan shall be agreed upon between vendor and customer.

8 Packaging and Marking

8.1 *Packaging* — Containers and packaging materials shall be selected to provide protection against normal transportation damage risks and spillage. They will also offer protection from contamination, exposure to moisture, oxidation, and tarnishing.

8.2 *Marking*

8.2.1 The following details shall be noted on the packing slip attached to the outside of the shipping package:

Vendor Part Number

Customer Part Number

Quantity

Date

Vendor Lot Number

User PO Number

Drawing Number

NOTICE: These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI G28-0997
SPECIFICATION FOR LEADFRAMES FOR PLASTIC MOLDED S.O. PACKAGES

1 Purpose

This specification defines the acceptance criteria for stamped leadframes for plastic molded S.O. packages.

2 Scope

This specification is a guideline for production of stamped S.O. Leadframes to be used in plastic molded S.O. packages.

3 Referenced Documents

3.1 *SEMI Specifications*

SEMI G4 — Specification for Integrated Circuit Leadframe Materials used in the Production of Stamped Leadframes

SEMI G9 — Specification for Stamped Leadframes for Plastic Molded Dual-In-Line Semiconductor Packages

SEMI G10 — Standard Method for Mechanical Measurement for Plastic Package Leadframes

SEMI G21 — Specification for Plating Integrated Circuit Leadframes

3.2 *ANSI/ASQC Specifications*[1]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ANSI Specifications*[2]

ANSI Y14.5M — Dimensioning and Tolerancing

4 Terminology

4.1 *burr* — A fragment of excess material either horizontal or vertical adhering to the component surface.

4.2 *camber* — Curvature of the leadframe strip edge in the horizontal plane (see Figure 1).

4.3 *coil set* — Longitudinal bowing of the leadframe (see Figure 2).

4.4 *coined area* — That area at the tip of the bond fingers flattened to produce an acceptable surface for wire bonding (see Figure 3).

4.5 *crossbow* — Transverse bowing of the leadframe (see Figure 4).

4.6 *functional area* — The die attach pad and the wire bond (lead tips) area.

4.7 *lead twist* — Angular rotation of bonding fingers (see Figure 5).

4.8 *pit* — A shallow surface depression or crater in the leadframe material.

4.9 *slugmarks* — Random dents in the leadframe caused by foreign material in the stamping die.

4.10 *stamped leadframe terminology* — (See Figure 6.)

5 Ordering Information

Purchase orders for leadframes for plastic molded S.O. packages furnished to this specification shall include the following items:

a. Current leadframe specification drawing.

b. All dimensions and tolerances per ANSI Y14.5 practices.

c. Material type and physical characteristics (see SEMI G4).

d. Type hardness and thickness of any required plating (see SEMI G21).

6 Dimensions

See Table 1 and Figure 7 for standard dimensions. Tolerances shall be agreed between vendor and customer.

7 Defect Limits and Parameters (see SEMI G10 for measurement methods)

7.1 *Internal Frame Area*

7.1.1 *Minimum Flat Wire Bonding Area* — 80% of nominal lead width and .015" (.381 mm) in length.

7.1.2 *Coin Depth*

7.1.2.1 0.008" (0.20 mm) material: 0.0005" (0.013 mm) minimum/0.001" (0.02 mm) maximum.

7.1.2.2 0.010" (0.25 mm) material: 0.0005" (0.013 mm) minimum/0.002" (0.05 mm) maximum.

1 ASQC, 611 East Wisconsin Avenue, Milwaukee, WI 53202

2 ANSI, 1430 Broadway, New York, NY 10018

NOTE: Maximum coin depth may also be constrained by minimum lead spacing requirement given in Section 7.1.3.1. Minimum coin depth may also be constrained by minimum bond area requirement given in Section 7.1.1.

7.1.3 *X-Y Plane Lead Spacing and Location*

7.1.3.1 Spacing between leads to be 0.004" (0.100 mm) minimum.

7.1.3.2 Leads to be located so that a 0.007" diameter circle centered on the nominal center of the coined lead in width and 0.006" (0.152 mm) back from lead tip in length shall be totally encompassed by the coined area.

7.1.4 *X-Y Plane Die Attach Pad Location* — Die attach pad to be located within ± 0.002" (0.051 mm) as measured from the centerline of the reference hole in the side rail.

7.1.5 *Lead Twist* — Shall not exceed 3°30' or 0.0006" (0.015 mm) per 0.010" (0.254 mm) of lead width.

7.1.6 *Die Attach Pad Tilt and Flatness*

7.1.6.1 *Tilt* — 0.001" (0.025 mm) maximum per 0.100" (2.54 mm) in the undepressed state. 0.002" (0.015 mm) maximum per 0.100" (2.54 mm) in the depressed condition.

7.1.6.2 *Flatness* — To be within 0.002" (0.051 mm) T.I.R. per 0.100" (2.54 mm) when measured from the center to each of the four corners. The corners are defined at 0.005" (0.127 mm) from each edge.

7.1.7 *Die Attach Pad Downset* — ± 0.002" (0.051 mm) as measured from the center of the pad to a point on the bar pad support strip. The nominal downset recommended is 0.012" (0.30 mm) for 0.010" (0.25 mm) thick material and 0.008" (0.20 mm) for 0.008" (0.20 mm) thick material.

7.1.8 *Lead and Die Attach Pad Coplanarity*

7.1.8.1 The coplanarity relationship is based on reference to the Z plane (see SEMI G10).

7.1.8.2 *Lead Planarity* — The lead tips as measured in the center of the back, uncoined surface of the lead tip shall be located within the following tolerances of the Z plane:

Lead Planarity: ± 0.004"

7.1.8.3 *Die Attach Pad Planarity* — The die attach pad when measured at the center must be within the following tolerances of the Z plane:

Pad Planarity: + 0.003"/-0.005"

7.2 *External Area and Strip*

7.2.1 *Material*

7.2.1.1 0.008" (0.20 mm) material thickness recommended for 0.150" wide packages.

7.2.1.2 0.010" (0.25 mm) material thickness recommended for 0.300" wide packages.

7.2.1.3 *Nominal Thickness* — Tolerances shall be ± 0.0003" (0.008 mm).

7.2.1.4 *Width Tolerance* — ± 0.002" (0.051 mm).

7.2.2 *Coil Set* — Maximum of 0.125" (3.175 mm) measured in a free standing state over strip length.

7.2.3 *Crossbow* — Crossbow shall not exceed the following dimensions:

Maximum Crossbow: ± 0.005" (0.127 mm)

7.2.4 *Camber* — Shall not exceed 0.002" (0.05 mm) over a gage length of 6.00" (150 mm). (See SEMI G10.)

7.2.5 *Progression* — Should be specified along with tolerances on the drawing.

7.2.6 *Burrs* — Burrs shall be firmly attached and able to withstand a probe force of 10 grams. Vertical burrs inside the dambar shall not exceed 0.001" (0.02 mm). Vertical burrs outside the dambar and horizontal burrs in any location shall not exceed 0.002" (0.05 mm).

7.2.7 *Pits and Slugmarks*

7.2.7.1 Within functional area and on external leads there shall be no slugmarks. Pits shall not exceed 0.0003" (0.008 mm) in depth and 0.0005" (0.013 mm) in largest surface dimension in these areas.

7.2.7.2 *Areas Other than 7.2.7.1* — Pits and imperfections shall not affect leadframe strength regardless of size and shall not exceed 0.002" (0.05 mm) in depth and 0.005" (0.127 mm) in largest surface dimension.

7.2.8 *Strip Length Cutoff* — (See SEMI G10.)

7.2.8.1 Strip cutoff location and tolerance shall be detailed on the drawing.

7.2.8.2 Overall strip length and tolerance shall be detailed on the drawing.

8 Functional Testing

Functional testing shall be agreed upon between vendor and customer.

9 Sampling

Sampling based on ANSI/ASQC Z1.4 shall be agreed between supplier and purchaser.

10 Packaging, Marking, and Packing List

10.1 *Packaging* — The shipping containers and materials shall be suitably designed to provide the leadframes with protection against normal transportation damage risks which include crushing and spillage, and exposure to moisture and other corrosive gases.

10.1.1 The inner packaging materials for cut strips must not cause particulate contamination on the leadframes and shall be clean room compatible as defined by the customer. The leadframes boxes shall be vacuum sealed in a bag with a desiccant. If the leadframes are to be delivered in coil form, the coil diameter shall be set in the purchase order (see SEMI G9).

10.2 *Marking*

10.2.1 *Internal Packages* — Each internal package shall be clearly marked with the following information, as appropriate:

a. Customer's part number

b. Customer's purchase order number

c. Drawing number (customer's and/or vendor's, as requested by customer)

d. Vendor's shipping lot number

e. Quantity

f. Date of Manufacture

g. Any agreed upon certification data

10.2.2 *External Packages* — The packing list on the outside of the external package shall contain the following information:

a. Customer's part number

b. Customer's purchase order number

c. Quantity

d. Shipping Date

e. Any specific instructions for receiving dock personnel

11 Certification

11.1 Upon request of the customer in the contract or purchase order, a vendor's certification that the product was manufactured and tested in accordance with this specification, together with a report of the test results shall be furnished at the time of shipment. However, if the customer does perform inspection and test on a certified shipment and the product fails to meet the requirements, the product shall be subject to rejection.

11.2 If the customer and vendor agree, the product may be certified as capable of meeting this specification. In this context, capable of meeting signifies that the vendor is not required to perform all the inspections and tests. However, if the customer does perform inspection and test on a certified shipment and the product fails to meet the requirements, the product shall be subject to rejection.

Table 1

		0.150 WIDE			*0.30 WIDE (J-COMPATIBLE)*					
		8	14	16	14	16	18	20	24	28
	MATERIAL GAGE	0.008" (0.200 mm)	0.008 (0.200)	0.008 (0.200)	0.010 (0.250)	0.010 (0.250)	0.010 (0.250)	0.010 (0.250)	0.010 (0.250)	0.010 (0.250)
A	STRIP WIDTH	0.600 (15.2)	0.600 (15.2)	0.600 (15.2)	0.720 (18.30)	0.720 (18.30)	0.720 (18.30)	0.970 (24.60)	0.970 (24.60)	0.970 (24.60)
B	PROGRESSION	0.336 (8.53)	0.336 (8.53)	0.336 (8.53)	0.674 (17.12)	0.674 (17.12)	0.674 (17.12)	0.674 (17.12)	0.674 (17.12)	0.674 (17.12)
C	TOOLING HOLE				0.060 (1.52)	0.060 (1.52)	0.060 (1.52)	0.060 (1.52)	0.060 (1.52)	0.060 (1.52)
D	DAMBAR WIDTH 0				0.010 (.250)	0.010 (.250)	0.010 (.250)	0.010 (.250)	0.010 (.250)	0.010 (.250)
E	DAMBAR DISTANCE FROM CL	0.079 (2.00)	0.079 (2.00)	0.079 (2.00)	0.156 (4.00)	0.156 (4.00)	0.156 (4.00)	0.156 (4.00)	0.156 (4.00)	0.156 (4.00)
F	LEAD LENGTH CL TO LEAD RAIL	0.167 (4.24)	0.167 (4.24)	0.167 (4.24)	0.322 (8.18)	0.322 (8.18)	0.322 (8.18)	0.322 (8.18)	0.322 (8.18)	0.322 (8.18)
G	PKG. LENGTH BOUNDARY	0.098 (2.49)	0.172 (4.37)	0.198 (5.03)	0.181 (4.60)	0.198 (5.03)	0.231 (5.87)	0.255 (6.48)	0.307 (7.80)	0.356 (9.04)
H	PARTS PER STRIP (STRIP LENGTH)	24 (8.064)	24 (8.064)	24 (8.064)	12 (8.088)	12 (8.088)	12 (8.088)	12 (8.088)	12 (8.088)	12 (8.088)
I	PAD DOWNSET	0.008 (0.200)	0.008 (0.200)	0.008 (0.200)	0.012 (0.305)	0.012 (0.305)	0.012 (0.305)	0.012 (0.305)	0.012 (0.305)	0.012 (0.305)

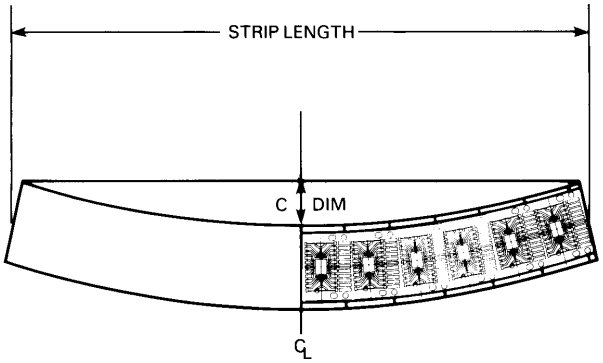

Figure 1
Camber

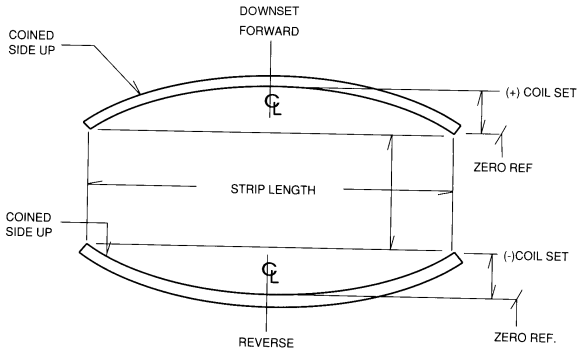

Figure 2
Coil Set

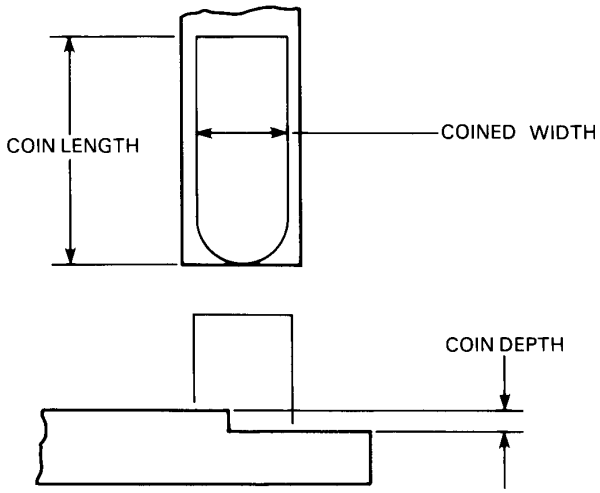

Figure 3
Coined Area

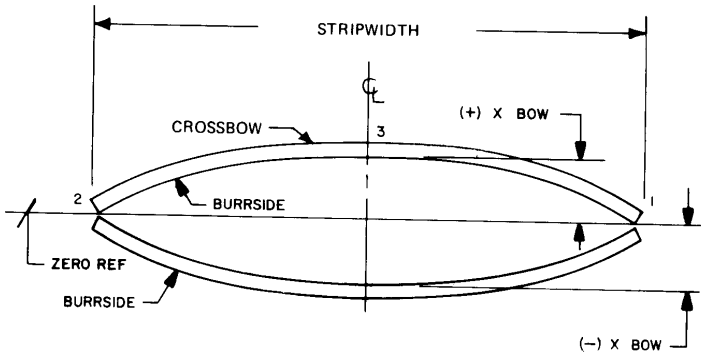

Figure 4
Crossbow

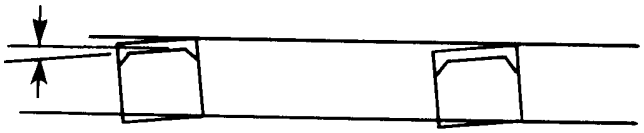

Figure 5
Lead Twist

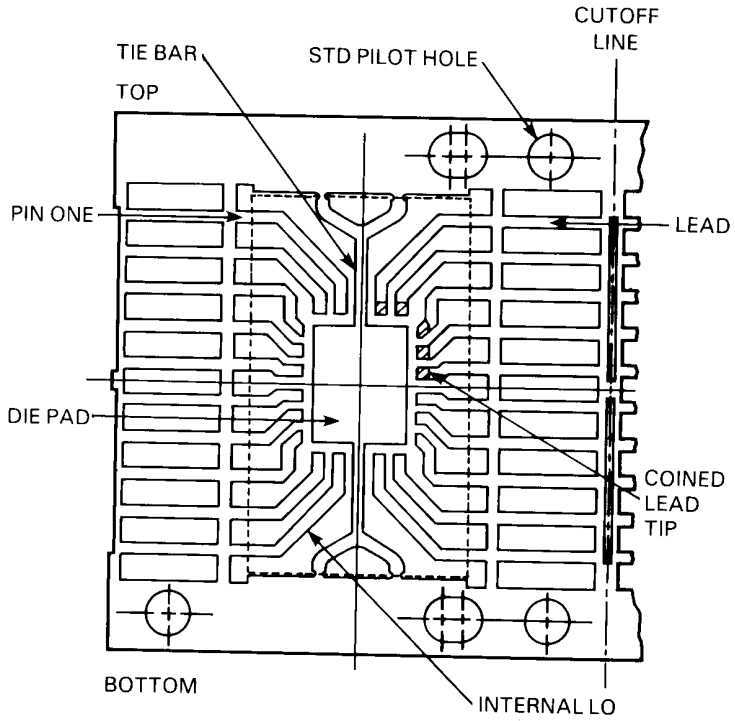

Figure 6
Stamped Leadframe Terminology

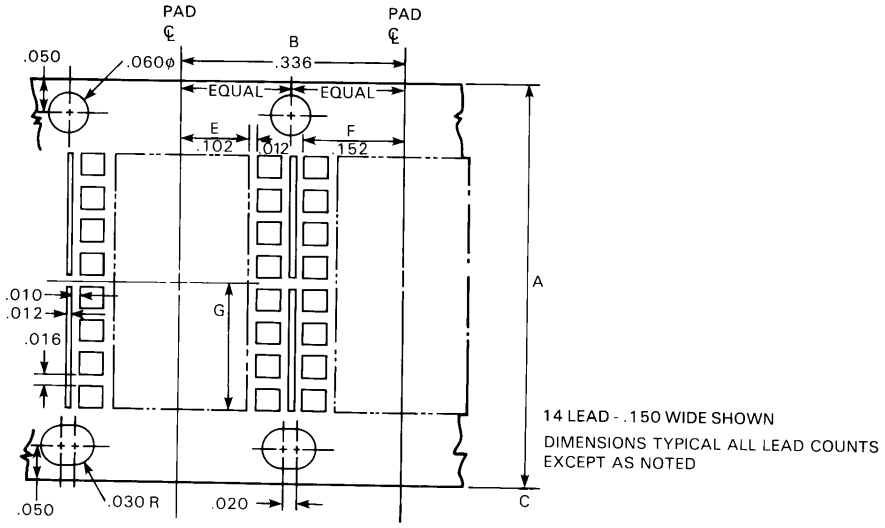

Figure 7
S.O. Leadframe Standard

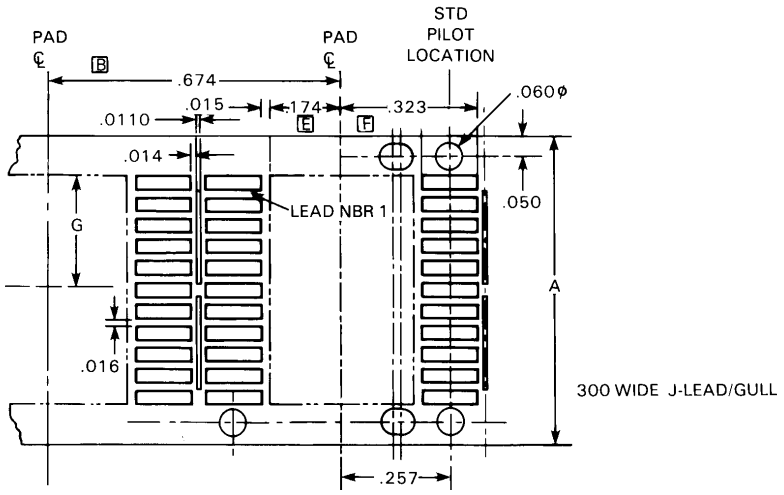

Figure 8
S.O. Leadframe

NOTICE: These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI G29-1296[E]
TEST METHOD FOR TRACE CONTAMINANTS IN MOLDING COMPOUNDS

[E] This document was editorially modified in September 2002. Changes were made to Section 5.4 to correct a typographical error.

1 Purpose

1.1 This specification defines the test method for determination of extractable trace contaminants in molding compound.

2 Scope

2.1 This test method is suitable for all molding compound materials and may be used by supplier and customers to determine the trace contaminants in molding compound.

2.2 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability or regulatory limitations prior to use.

3 Referenced Documents

3.1 *ASTM Documents*[1]

ASTM D 1193 — Specification for Reagent Water

ASTM D 4327 — Anions in Water by Ion Chromatography

4 Method Summary

4.1 Plastic molding compound material is molded, ground to a defined mesh size, and placed into a sealed extraction vessel with de-ionized water. Extraction is carried out at 120 ± 2° C for 48 hours. The extract is analyzed for both anionic and cationic impurities.

5 Sample Preparation

5.1 Samples of molding compound materials may be obtained from either standard molding operations, or prepared in the laboratory.

5.1.1 Samples from molding operations may include mold runners post-cured according to manufacturer's recommendations.

5.1.2 To secure a sample in the laboratory, spread a thin layer of uncured compound in a dedicated clean teflon-coated container. Cure and post-cure the compound material according to manufacturer's recommendations.

5.2 Crush the cured material using a suitable grinding apparatus, such as Spex mixer-mill No. 8000, or equivalent.

NOTE 1: The grinder used must not generate excess localized heat, or else sample decomposition and erroneous results may be generated.

NOTE 2: Addition of liquid nitrogen is a suitable method for eliminating undesirable thermal decomposition during grinding.

5.3 Remove the ground compound and sieve it. Collect for analysis the portion which passes through a 40 mesh size, but is retained on a 100 mesh size screen. This particle size is best suited for adequate extraction of impurities.

5.4 Weigh 10 ± 0.1 grams of the powdered material and place in an extraction vessel. Parr bombs with teflon liners are suitable extraction vessels. Add 100 ml de-ionized water. Prepare blank extraction vessel by processing it in the same manner as your sample. Weigh the sealed bombs and record their weights. Place the sealed bottles on their sides in an oven at 120 ± 2° C for forty-eight (48) hours.

NOTE 3: Certain compounds may require addition of reagent grade methanol 10% (V:V) to enhance wetting.

5.5 At the completion of forty-eight (48) hours of extraction, allow the bombs to cool to room temperature and reweigh. If the weight loss exceeds 0.5 grams the sample should not be used for analysis. Portion of this extract may be used to generate pH and conductivity data. Anion analysis may be performed using ion chromatography or specific ion electrodes. Cation analysis may be conducted using atomic absorption, plasma spectrometry, or ion chromatography.

NOTE 4: It is important to avoid contamination with particulate matter in the extract used for the analysis by AA, ICAP, or IC. This procedure addresses determination of extractive species only.

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

6 Instrumentation Techniques

6.1 *Measurement of Conductivity*

6.1.1 *Apparatus* — Conductivity Meter Model RC1682 with microconductivity cell, industrial instruments, or equivalent.

6.1.2 *Measurement* — Measure conductivity of the sample and black solutions. Calculate the specific conductance of sample using the following equation:

$L_s = (L_e - L_b) K$

L_s - Specific conductance, S cm^{-1}

L_e - Conductance of extract, S

L_b - Conductance of the blank

K - Conductivity cell constant

6.2 *Measurement of pH*

6.2.1 *Apparatus*

6.2.1.1 pH meter (Orion, Model 601, or equivalent)

6.2.1.2 pH standard solutions

6.2.2 *Measurement* — Adjust pH meter indicator by using standard solutions. Remove the electrodes with de-ionized water and dry with clean filter paper. Place the electrodes into the molding compound extract. Allow the meter to equilibrate. Record the pH value.

6.3 *Ion Specific Electrodes* — Ion-specific electrodes may be used for the determination of chloride, bromide, sulfate, and phosphate. A separate specific electrode for each ion is required and, in some instances, a reference electrode may be necessary to complete the test. Individual standards are needed for each ion tested. Methodology recommended by the manufacturer for each ion specific electrode should be closely followed. Measured concentrations corrected for blank value should be compared to the known standards in the range 0.1–100 ppm. Chloride and bromide are usually determined, using a solid state single electrode. Determination of sulfate and phosphate ions may require use of additional buffers and a titration.

6.4 *Determination of Sodium, Potassium, and Antimony Using Atomic Absorption*

6.4.1 *Apparatus* — Atomic absorption spectrophotometer.

6.4.2 *Standard Solutions*

6.4.2.1 Sodium standard solutions 0.1, 0.2, 0.4, 0.6, 0.8, 1.0 ppm.

6.4.2.2 Potassium standard solutions 0.1, 0.2, 0.4, 0.6, 0.8, 1.0 ppm.

6.4.2.3 Antimony standard solution 0.1, 0.2, 0.4, 0.6, 0.8, 1.0 ppm.

6.4.3 *Measurement* — Set up instrument according to manufacturer's recommendation. Analyze water extract based on the calibration curve prepared using standard solutions to obtain concentration of ion of interest.

6.4.4 *Calculation*

6.5 Determination of Chloride, Bromide, Phosphate, Sulfate, Sodium, and Potassium by Ion Chromatography

6.5.1 *Method Principle* — Ion chromatography is a form of liquid chromatography used in the separation and quantitation of ions. A filtered aliquot of sample is injected into an Ion chromatograph. The sample is pumped by the eluent stream through two (2) different ion exchange columns: a guard column, which serves to protect the separator column from residual particulate matter and retain certain organics, and the separator column, the primary function of which is to separate analyzed ions based on their affinity for the exchange sites of the resin. Both guard column and the separator column are packed with identical low capacity anion exchanger (anion analysis) or cation exchange (cation analysis). The separated ionic species then pass to a detector module consisting of a chemical suppressor device and a conductivity cell. The suppressor device is used to reduce background conductivity of the eluent to a low, or negligible level, and convert analyte anions into their acid form or analyte cations into their hydroxide form. Thus, separated and modified ionic species are detected using an electrical conductivity cell. Anions are identified based on their retention time compared to the known standards. Quantitation is accomplished by measuring the peak height or area, and comparing it to a calibration curve generated from known standards.

NOTE 5: For recommended practice for ion chromatography analyses, see instrument manufacturer's literature and ASTM D 4327.

6.5.2 *Interferences*

6.5.2.1 High levels of organic acids may be present in molding compound extracts. This may interfere with inorganic anion analysis. Two (2) common species, formate and acetate, elute between fluoride and chloride. This may be minimized by modifying instrument set-up.

6.5.2.2 Certain amines may interfere with the determination of sodium or potassium. This may be minimized by using different instrument set-ups.

6.5.3 *Apparatus*

6.5.3.1 Ion chromatograph (Dionex or equivalent). The chromatograph shall be equipped with an injection valve, a 50–100 µl sample loop, and shall be set up with the following:

1. Guard Column
2. Separator Column
3. Chemical Suppressor Device
4. Conductivity Detector

6.5.4 *Reagents*

6.5.4.1 *Water Purity* — Water used in the preparation of eluents, standards, and sample extraction shall conform to ASTM D 1193.

6.5.4.2 *Reagent Purity* — Reagent grade chemicals should be used in all tests.

6.5.4.3 *Eluent/Regenerant Solutions* — Should be prepared in accordance with instrument manufacturer's instructions recommended for each column set.

6.5.4.4 *Stock Solutions* — Stock solutions (1 ml - 1 mg - 1 ppm ion of interest) should be prepared according to accepted practice, and as described in the instrument manufacturer's instructions.

6.5.4.5 *Calibration Standards* — Prepare a blank and at least three (3) different calibration solutions containing combination of anion/cations. These solutions must be prepared in volumeric flasks (see Table 1).

6.5.4.5.1 Prepare a standard solution I by diluting the volume of each anion/cation stock solution as specified in Table 1 together with 1 litre of water.

6.5.4.5.2 Prepare a standard solution II by diluting 20 ml of standard solution II to 100 ml with water (see Table 1).

NOTE 6: If the concentrations of the sample ions are known, or estimated, the concentration of calibration standard solutions may be varied to better approximate or bracket concentration range of interest.

6.5.5 *Calibration*

6.5.5.1 Analyze the blank and each of the prepared calibration solutions described in Section 6.5.4.5.

6.5.5.2 Prepare analytical curves for each anion/cation of interest by plotting on linear graph paper peak height or peak area versus nominal concentrations of the anion/cation calibration standard.

NOTE 7: Each analytical curve should be established using only one (1) scale setting.

6.5.6 *Procedure*

6.5.6.1 Set-up the ion chromatograph according to the manufacturer's instructions.

NOTE 8: The range setting required for the analysis will depend on the concentration of ions in the sample and should be chosen accordingly. For these types of samples, operating range from 30 to 30µ S/cm, fullscale is most frqurntly used.

6.5.6.2 Equilibriate the system by pumping eluent through the analytical system until a stable baseline is obtained (approximately twenty (20) minutes).

6.5.6.3 Filter samples through a pre-washed 0.22 µm filter prior to analysis.

NOTE 9: Several types of syringe-tip filters are available (Millipore or equivalent).

6.5.6.4 Load 2–3 ml of sample into the injection part using a syringe. Inject the sample into the eluent stream and record the ion chromatogram.

6.5.7 *Calculations*

6.5.7.1 Refer to the peak height or area for the anions/cations of interest to the appropriate analytical curves to determine the anion concentration.

6.6 *Inductivity Coupled Argon Plasma Spectrometry/ICP*

6.6.1 *Method Principle* — Inductivity coupled Argon Plasma (ICP) uses high frequency Argon Plasma to excite sample constituents to 8000° K. Because the plasma ionizes most atomic species, background interferences are vastly reduced and linear response over several orders of magnitude can be observed for most elements. The sample extract is aspirated into the plasma by means of a high purity argon carrier gas. The resulting emissions are directed into the spectrometer and signal strengths are read by photomultiplier tubes placed at emission points in a focal curve. A computer is used to scan each elemental channel many times a second, and this output is sent to a printer in numerical form. The cycle or time of analysis is usually about seven (7) seconds. With this instrument, very little of the extracted sample is consumed.

6.6.2 *Instrument Conditions*

Typical operating conditions are:

Excitation source	27 MHz plasma
Carrier gas	99.999% Argon
Sample flow	1 ml/min
Power output	1000 watts
Plasma temperature	8000° K
Slit width of Spectrometer	30 µ m

6.6.3 *Measurement of Sodium, Potassium, and Antimony* — A standard solution of ten (10) ppm of sodium, potassium, and antimony should be prepared and cycled through the ICP instrument. The blank extract sample and the unknown molding compound extracts are then run through the ICP. The values obtained for sample are corrected by subtracting values obtained for the blank. With the ICP, sodium, potassium, and antimony can be analyzed with sensitivities to the ten (10) PPB levels. Any additional elements present may be obtained on the same cycle with no additional preparation.

Table 1 Preparation of Standard Solutions for Instrument Calibration

Anion	*Standard Solution*		*Standard Solution II*	*Standard Solution III*
	ml of Stock Soln. Diluted to 1000 ml	*Anion Conc. mg/1*		
Chloride (Cl)	5	5	1	0.2
Phosphate (HPO_4^{2-})	25	25	5	1.0
Bromide (Br^-)	10	10	2	0.4
Nitrate (NO_3	30	30	6	1.2
Sulfate (SO_4^{2-})	25	25	5	1.0
Cation				
Sodium (NA^+)	5	5	1	0.2
Ammonium (NH_4^+)	5	5	1	0.2
Potassium (K^+)	10	10	2	0.4

SEMI G30-88
TEST METHOD FOR JUNCTION-TO-CASE THERMAL RESISTANCE MEASUREMENTS OF CERAMIC PACKAGES

1 Purpose

The purpose of this test is to determine the thermal resistance of ceramic packages using thermal test chips. This test method deals only with junction-to-case or mounting surface measurements of thermal resistance and limits itself to heat sink and fluid bath testing environments. Following the guidelines outlined in this test method, junction-to-case thermal resistance measurements of ceramic packages using the heat sink and fluid bath methods should give the same results only under certain limited conditions (i.e., under conditions that approximate unidirectional heat flow through the chip and substrate to the preferred heat removal surface). If discrepancies occur, the heat sink mounting technique shall be considered as the referee test method. The heat sink mounting method for measuring junction-to-case thermal resistance will be a conservative measure of the package's ability to transfer heat to the ambient environment because heat sinking is provided only on one side of the package, whereas the fluid bath mounting method has the potential for equally cooling both sides of the package.

1.1 *Definitions* — The following definitions and symbols shall apply for the purpose of this test:

a. *case temperature,* T_C, in degrees Celsius. The case temperature is the temperature at a specified accessible reference point on the package in which the microelectronic chip is mounted.

b. *mounting surface temperature,* T_M, in degrees Celsius. The mounting surface temperature is the temperature of a specified point at the device-heat sink mounting interface (or primary heat removal surface).

c. *junction temperature,* T_J, in degrees Celsius. The term is used to denote the temperature of the semiconductor junction in the microcircuit in which the major part of the heat is generated. For purposes of this test, the measured junction temperature is only indicative of the temperature in the immediate vicinity of the element used to sense the temperature.

d. *power dissipation,* P_H, in watts, is the heating power applied to the device causing a junction-to-reference point temperature difference.

e. *thermal resistance, junction-to-specified reference point,* $R_{\Theta JR}$, in degrees Celsius/watt. The thermal resistance of the microcircuit is the temperature difference from the junction to some reference point on the package divided by the power dissipation P_H.

f. *temperature-sensitive parameter,* TSP, is the temperature-dependent electrical characteristic of the junction under test which can be calibrated with respect to temperature and subsequently used to detect the junction temperature of interest.

2 Apparatus

2.1 The apparatus required for these tests shall include the following as applicable to the specified test procedures.

a. Thermocouple material shall be copper-constantan (type T) or equivalent, for the temperature range -100 to +300°C. The wire size shall be no larger than AWG size 30. The junction of the thermocouple shall be welded to form a bead rather than soldered or twisted. The accuracy of the thermocouple and associated measuring system shall be ± 0.5°C.

b. Suitable electrical equipment as required to provide controlled levels of conditioning power and to make the specified measurements. The instrument used to electrically measure the temperature-sensitive parameter shall be capable of resolving a voltage change of 0.5 mV.

c. Controlled temperature chamber, fluid bath, or heat sink capable of maintaining the specified reference point temperature to within ± 0.5°C of the preset (measured) value. Typical temperature-controlled heat sink and fluid bath assemblies are presented for illustrative purposes only.

2.2 *Heat Sink Assembly* — A typical heat sink assembly for mounting the microelectronic device under test is shown in Figure 1. The primary heat sink is water cooled using a temperature-controlled fluid circulator bath. An adapter socket/heat sink is fastened to the heat removal surface of the primary heat sink, and has a special geometry to handle specific size packages (e.g., flat packs, dual-in-line packages, chip carriers). This adapter provides a repeatable and

efficient interface between the package and the primary heat sink. The mounting surface temperature is determined with a thermocouple attached from the side or bottom of the adapter with a thermal conducting adhesive or grease at or near the interface between the adapter and the package. It is at this point that the device-under-test temperature is specified and controlled. The adapter also contains the socket or other electrical interconnection scheme. A thin coating (about 25 – 50 mm thick) of a thermal heat-sinking compound, such as zinc-oxide-loaded silicone thermal grease, is used at the interface to provide a reliable thermal contact.

2.3 *Fluid Bath Assembly* — A typical temperature-controlled fluid bath for thermally characterizing the microelectronic device under test is shown in Figure 2. In this figure, the package is mounted in a fluid bath separate from the fluid circulator, although it can be immersed directly in an integrated fluid circulator/bath unit. The fluid in the bath should be continuously stirred or agitated to ensure the required temperature stability. Since this working fluid is being used as an infinite heat sink, the case-to-fluid (ambient) temperature difference at the case temperature reference point of interest should be minimized, i.e., less than or equal to 20°C. For case-to-fluid temperature differences greater than 20°C, accuracy and repeatability difficulties may occur due to a large variable temperature gradient in the fluid film boundary layer at the package-fluid interface. The case-to-fluid temperature difference can be minimized by increasing the fluid velocity and by decreasing the power density seen by the fluid. The device under test should be mounted such that heat transfer to the fluid is not impeded. For leaded devices, the leads should be oriented in such a manner so as not to interfere with the heat transfer to the fluid and provide freedom to any thermal currents caused by the power dissipation within the package. The case temperature of the device under test should be measured with a thermocouple that is attached to the package and should not be assumed to be at the fluid temperature. Care should be taken to minimize exposure of the thermocouple bead to the high temperature gradient in the fluid film boundary layer at the package-fluid interface. The working fluid should have a thermal conductivity at 25°C of at least 0.0006 W/cm°C. Working fluids such as inert fluorocarbon liquids and silicone oils are suitable as a cooling media.

3 Procedure

3.1 *Direct Measurement of Reference Point Temperature* — T_C. For the purpose of measuring a microelectronic device thermal resistance, the reference point temperature shall be measured at the package location of highest temperature which is accessible outside the package. This reference point location is determined with the device operating in free air and with no external heat-sinking. In general, this reference point is found to be on the outside surface of the package substrate directly underneath the chip in the major path of heat flow from the chip to the heat sink or ambient. Examples of the reference point location for both cavity-up and cavity-down ceramic packages are depicted in Figure 3. The package surface may be altered to facilitate this measurement, provided that such alteration does not affect the original heat transfer paths and, hence, the thermal resistance, within the package by more than a few percent. For packages with an integral heat dissipater attached to the outside surface of the package substrate, the case temperature reference point shall be on the surface of the heat dissipater at a point opposite the backside of the chip as indicated in Figure 4.

3.1.1 Case temperature, T_C. The microelectronic device under test shall be mounted under specified conditions so that the case temperature can be held at the specified value. A thermocouple shall be attached on the surface of the device package directly under the chip. A conducting epoxy may be used for this purpose. The thermocouple bead should be in direct mechanical contact with the case of the microelectronic device under test. For devices which, in their normal application, are intimately connected (by pressure contact, adhesive, soldering, or other means) to an external heat sink, the mounting surface temperature, as measured directly below the primary heat removal surface of the case, may be used as the equivalent case temperature.

If it is found that attaching the thermocouple directly to the case is impractical, an alternate approach utilizing a thermocouple welded to one side of a thin metal disk should be used. This can be accomplished by parallel gap welding the crossed thermocouple wires to one side of a 0.25 cm (0.094 in) diameter, 0.02 cm (0.008 in) thick beryllium-copper disk and then, with a thin layer of adhesive, bonding the other side of the disk to the case at the point of interest.

3.1.1.1 Mounting surface temperature, T_M. The mounting surface temperature is measured directly below the primary heat removal surface of the case. It is measured with a thermocouple at or near the mounting surface of the heat sink. A typical mounting arrangement is shown in Figure 5. The surface of the copper mounting base shall be nickel plated and free of oxides.

The thermocouple hole shall be drilled into the mounting base such that the thermocouple lead is directly below the area on the case of interest. It is

recommended that the thermocouple be secured into the mounting base with a thermal conducting adhesive (or solder) and that particular attention be paid to minimizing air voids around the ball or the thermocouple. A thermal conducting compound (or adhesive) should be used at the interfaces of the mounting base and the device under test. The mounting surface technique is application oriented in that it takes into account the mounting surface interface.

3.2 *Thermal Resistance, Junction-to-Specified Reference point, $R_{\Theta JR}$*

3.2.1 *General Considerations* — The thermal resistance of a semiconductor device is a measure of the ability of its carrier or package and mounting technique to provide for heat removal from the semiconductor junction. The thermal resistance of a microelectronic device can be calculated when the case/mounting surface temperature and power dissipation in the device and a measurement of the junction temperature are known.

When making the indicated measurements, the package shall be considered to have achieved thermal equilibrium when halving the time between the application of power and the taking of the reading causes no error in the indicated results within the required accuracy of measurement.

3.2.2 *Indirect Measurement of Junction Temperature for the Determination of $R_{\Theta JR}$* — The purpose of the test is to measure the thermal resistance of integrated circuits by using particular semiconductor elements on the chip to indicate the device junction temperature. In order to obtain a realistic estimate of the operating junction temperature, the whole chip in the package should be powered in order to provide the proper internal temperature distribution. During measurement of the junction temperature the chip heating power (constant voltage source) shall remain constant while the junction calibration current remains stable. It is assumed that the calibration current will not be affected by the circuit operation during the application of heating power.

The temperature-sensitive device parameter is used as an indicator of an average (weighted) junction temperature of the semiconductor element for calculations of thermal resistance. The measured junction temperature is indicative of the temperature only in the immediate vicinity of the element used to sense the temperature.

The temperature-sensitive electrical parameters generally used to indirectly measure the junction temperature are the forward voltage of diodes and the emitter-base voltage of bipolar transistors. Other appropriate temperature-sensitive parameters may be used for indirectly measuring junction temperature for fabrication technologies that do not lend themselves to sensing the active junction voltages.

3.2.2.1 Steady-state technique for measuring T_J. The following symbols shall apply for the purpose of these measurements:

I_M	Measuring current in milliamperes.
V_{MH}	Value of temperature-sensitive parameter in millivolts, measured at I_M, and corresponding to the temperature of the junction heated by P_H.
T_{MC}	Calibration temperature in degrees Celsius, measured at the reference point.
V_{MC}	Value of temperature-sensitive parameter in millivolts, measured at I_M, and specific value of T_{MC}.

The measurement of T_J using junction forward voltage as the TSP is made in the following manner:

Step 1 — Measurement of the temperature coefficient of the TSP (calibration).

The coefficient of the temperature-sensitive parameter is generated by measuring the TSP as a function of the reference point temperature, for a specified constant measuring current, IM, by externally heating the device under test in an oven or in a fluid bath. The reference-point temperature range used during calibration shall encompass the temperature range encountered in the power application test (see Step 2). The measuring current is generally chosen such that the TSP decreases linearly with increasing temperature over the range of interest, and that negligible internal heating occurs in the silicon and metal traces. For determining the optimum TSP calibration or measuring current, V_{MC} vs. log I_M curves for two temperature levels that encompass the calibration temperature range of interest should be plotted. The optimum measuring current, I_M, is then selected such that it resides on the linear portion of the two V_{MC} vs. log I_M curves that were generated. A measuring current ranging from 0.05 to 5 mA is generally used, depending on the specifications and operating conditions of the device under test, for measuring the TSP. The value of the TSP temperature coefficient, V_{MC}/T_{MC}, for the particular measuring current used in the test, is calculated from the calibration curve, V_{MC} vs. T_{MC}. At least three points should be used to generate the voltage vs. temperature curve for the determination of the TSP temperature coefficient.

Step 2 — Power application test.

The power application test is performed in two parts. For both portions of the test, the reference point temperature is held constant at a preset value. The first

measurement to be made is that of the temperature-sensitive parameter, i.e., V_{MC}, under operating conditions with the measuring current, I_M, used during the calibration procedure. The microelectronic device under test shall then be operated with heating power (P_H) applied. The temperature-sensitive parameter, V_{MH}, shall be measured with constant measuring current, I_M, that was applied during the calibration procedure (See Step 1).

The heating power, P_H, shall be chosen such that the calculated junction-to-reference point temperature difference as measured at V_{MH} is greater than or equal to 20°C. In accomplishing this, the device under test should not be operated at such a high heating power level that the on-chip temperature-sensing and heating circuitry is no longer electrically isolated. Care should also be taken not to exceed the design ratings of the package-interconnect system, as this may lead to an overestimation of the power being dissipated in the active area of the chip due to excessive power losses in the package leads and wire bonds. The values of V_{MH}, V_{MC}, and P_H are recorded during the power application test.

The following data shall be recorded for these test conditions:

a. Temperature-sensitive electrical parameters (V_F, V_{EB}, or other appropriate TSP).

b. Junction temperature, T_J, is calculated from the equation:

$$T_J = T_R + \left(V_{MH} - V_{MC}\right)\left|\frac{\Delta V_{MC}}{\Delta T_{MC}}\right|^{-1}$$

where $T_R = T_C$ or T_M

c. Case or mounting surface temperature, T_C or T_M.

d. Power dissipation, P_H.

e. Mounting arrangement (including package mounting force).

3.3 Calculations of $R_{\Theta JR}$

3.3.1 *Calculations of Package Thermal Resistance* — The thermal resistance of a microelectronic device can be calculated when the junction temperature, T_J, has been measured in accordance with procedures outlined in Sections 3.1 and 3.2.

With the data recorded from each test, the thermal resistance shall be determined from:

$$R_{\Theta JR} = \frac{T_J - T_R}{P_{H(package)}}, \text{ junction - to reference point,}$$

where $R_{QJR} = R_{QJC}$ or R_{QJM} and $T_R = T_C$ or T_M, respectively.

4 Summary Report

The following details shall be specified as appropriate:

a. Description of package, including thermal test chip, location of case or chip carrier temperature measurement(s), and heat sinking arrangement.

b. Test condition(s), as applicable (see Section 3).

c. Test voltage(s), current(s), and power dissipation of test chip.

d. Recorded data for each test condition, as applicable.

e. Symbol(s) with subscript designation(s) of the thermal characteristics determined.

f. Accept or reject criteria.

RELATED REFERENCES

1. Unencapsulated Thermal Test Chip, SEMI G32-86 Guideline, Book of SEMI Standards, Packaging Volume.

2. Accepted Practices for Making Microelectronic Device Thermal Characteristics Test — A User's Guide. JEDEC Engrg. Bull. No. 20, Jan. 1975 (Electronic Industries Assoc., Washington, D.C.).

3. Thermal Characteristics, Method 1012.1, MIL-STD-883C Test Methods and Procedures for Microelectronics, Nov. 4, 1980 (Rev. Aug. 15, 1984).

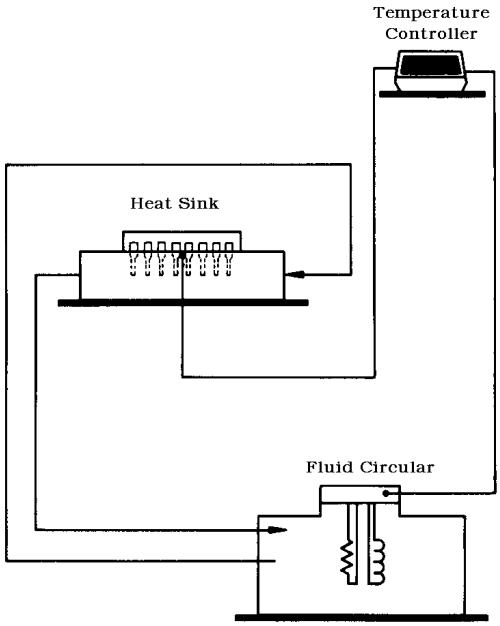

Figure 1
Temperature-Controlled Heat Sink Assembly

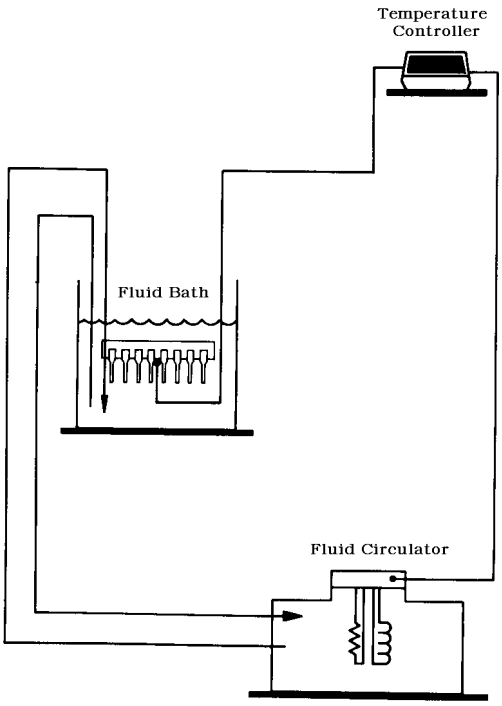

Figure 2
Temperature-Controlled Fluid Bath Assembly

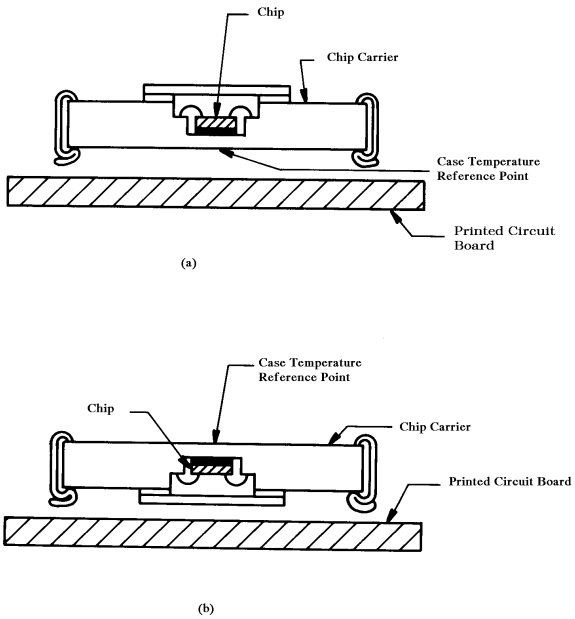

Figure 3
Reference Point Location for Case Temperture Measurement of A) Cavity-Up and B) Cavity—Down Ceramic Packages

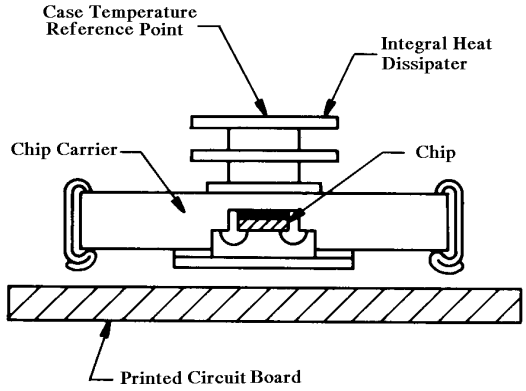

Figure 4
Reference Point Location for Case Temperature Measurement of a Ceramic Package with an Integral Head Dissipater

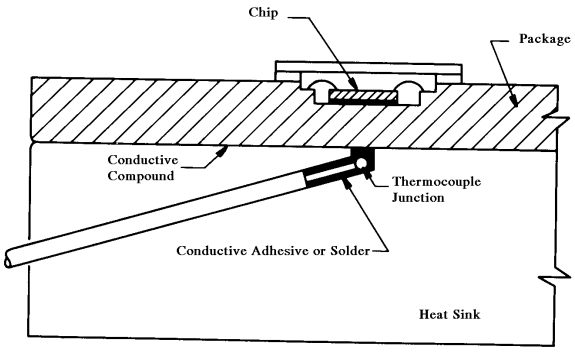

Figure 5
Mounting Surface Temperature Measurements

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SEMI G31-0997
TEST METHOD FOR DETERMINING THE ABRASIVE CHARACTERISTICS OF MOLDING COMPOUNDS

1 Purpose

This document describes the method to measure the abrasive characteristics of molding compounds by measuring mold orifice weight loss as a function of molded volume.

2 Scope

2.1 All thermoset molding compounds used for microelectronic device encapsulation contain filler materials, typically 60–90% — which contribute to mold wear. Mold wear, typically at gates, is a major reason for mold rework. This test method may be used by suppliers to evaluate new molding materials or control current materials or by customers to evaluate the use of new materials. This test method provides a comparison of abrasiveness between materials.

2.2 This procedure can be used to determine the abrasive character of a given molding compound. Knowing the conditions of test, the results of the test, and the mold life experience (within one's own company) in the field, it is possible to judge if a molding compound is more or less abrasive to current compound in use.

3 Referenced Documents

3.1 Operational manuals for all equipment listed within this document.

3.2 Mold compound data sheets

4 Method

This procedure determines the abrasive character of a given filled molding compound by measuring orifice weight loss as a function of extruded volume.

5 Interferences

5.1 Care must be taken to avoid orifice weight loss by mishandling during placing and removing the orifice from the mold base.

5.2 Before the orifice is re-weighed after molding, carefully remove all contamination.

6 Equipment

6.1 Transfer molding press, 50 tons clamp minimum

6.2 Dielectric preheater

6.3 Orifice insert and mold assembly (See Figures 2–6.)

6.4 Mold base with pot diameter 1.75 to 2.00 inches

6.5 Photoelectric safety light screen

6.6 Stop watch

6.7 Pyrometer

6.8 Force gauge

6.9 Asbestos gloves

7 Procedure

7.1 *Equipment Set-Up* — Orifice Mold Installation (see Figure 1).

7.1.1 Place mold assembly on mold base and align orifice retainer opening with center of transfer pot.

7.1.2 Clamp bottom plate of mold assembly to bottom mold platen.

7.1.3 Set press limit switch to ensure clamp slow close is initiated 1" from completion of mold closing.

7.2 *Process Parameters*

7.2.1 Set up the molding parameters according to the material data sheet recommendations or expected use conditions, if known. These conditions include:

- Mold temperature
- Pre-heat temperature or pre-heat time
- Transfer speed
- Transfer pressure
- Clamp pressure
- Cure time

NOTE: The charge weight to be determined by trial molding shots to achieve a cull thickness between 0.060–0.120" and a suitable weight of extrudate.

7.3 *Operating Procedure*

7.3.1 Weigh orifice to one ten-thousandth of a gram. Record weight.

7.3.2 Verify process parameter settings.

7.3.3 Place orifice in orifice retainer and clamp mold assembly.

7.3.4 Preheat preformed material to the required temperature.

7.3.5 Insert preheated material into transfer pot and activate transfer ram (semi-automatic mode).

7.3.6 Start stopwatch when extrudate first appears. Record total extrusion time.

7.3.7 Collect and weigh extrudate to nearest one tenth of a gram. Record extrudate weight.

7.3.8 At the end of cure cycle, remove orifice from retainer. Loosen set-screws to split orifice and, with compressed air, blow out cured slug.

7.3.9 Ensure mating orifice halves are clean, realign the halves and tighten set screws.

7.3.10 Place orifice in retainer and repeat steps 7.3.4 through 7.3.9.

7.3.11 Repeat steps 7.3.4 through 7.3.10 until a minimum of 40 shots are run.

7.3.12 Record the following:

1. Original orifice weight
2. Shot number
3. Extruded weight per shot in grams
4. Cumulative extruded weight in grams
5. Orifice weight in grams
6. Orifice percent weight loss
7. Extrusion rate

8 Calculation

8.1 *Orifice Weight Loss*

$$\frac{I_O - I_N}{I_O}(100\%) = \%\ \text{wt. loss}$$

I_O = Initial orifice weight to ten thousandth of a gram

I_N = Orifice weight after "N" number of shots to ten thousandth of a gram

8.2 Plot on linear graph paper the orifice weight loss vs. cumulative extruded weight.

8.3 Convert cumulative weight extruded to cumulative volume extruded.

Example: Molding compound density 2.0 g/cm^3 cumulative weight = 2000 g

$$2000\ g \times \frac{cm^3}{2.0g} = 1000\ \ cm^3$$

8.4 Convert cumulative volume extruded to equivalent production mold shots.

Example: 28 mm × 28 mm × 3.4 mm - 208 Id PQFP

Package Volume:

$$28\,\text{mm} \times 28\ \text{mm} \times 3.4\ \text{mm}\,\text{x}\ \frac{\text{cm}^3}{1000\ \text{mm}^3} = 2.6656\ \text{cm}^3$$

Volume to shots:

$$1000\ \ \text{cm}^3 \times \frac{\text{shot}}{2.6656\ \text{cm}^3} = \ 375\ \text{shots}$$

8.5 Plot on linear graph paper the orifice weight loss vs. equivalent production mold shots.

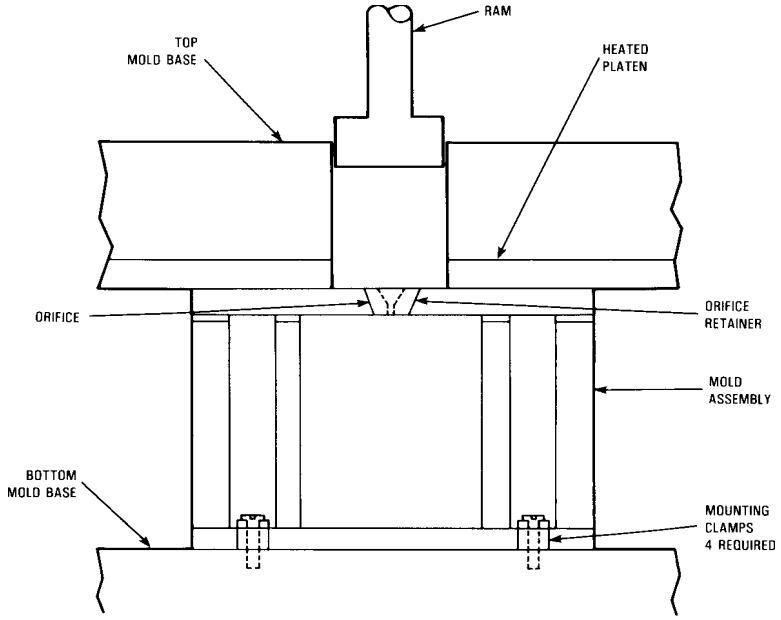
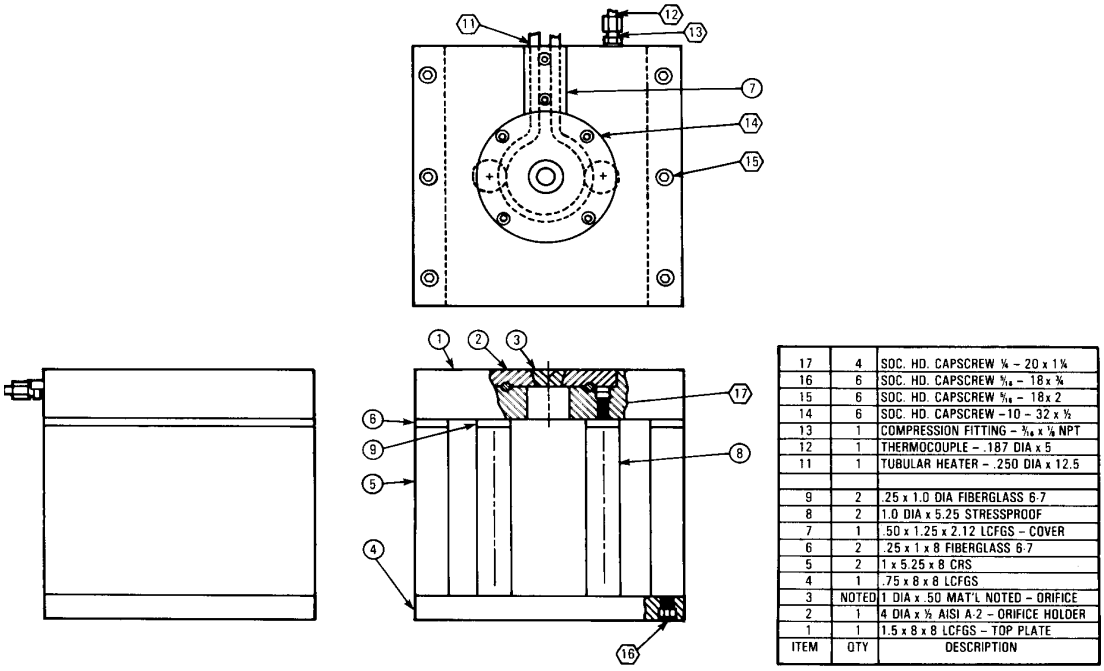


Figure 1
Orifice Abrasion



ITEM	QTY	DESCRIPTION
17	4	SOC. HD. CAPSCREW ¼ – 20 x 1¼
16	6	SOC. HD. CAPSCREW 5/16 – 18 x ¾
15	6	SOC. HD. CAPSCREW 5/16 – 18 x 2
14	6	SOC. HD. CAPSCREW –10 – 32 x ½
13	1	COMPRESSION FITTING – 3/16 x ⅛ NPT
12	1	THERMOCOUPLE – .187 DIA x 5
11	1	TUBULAR HEATER – .250 DIA x 12.5
9	2	.25 x 1.0 DIA FIBERGLASS 6:7
8	2	1.0 DIA x 5.25 STRESSPROOF
7	1	.50 x 1.25 x 2.12 LCFGS – COVER
6	2	.25 x 1 x 8 FIBERGLASS 6:7
5	2	1 x 5.25 x 8 CRS
4	1	.75 x 8 x 8 LCFGS
3	NOTED	1 DIA x .50 MAT'L NOTED – ORIFICE
2	1	4 DIA x ½ AISI A-2 – ORIFICE HOLDER
1	1	1.5 x 8 x 8 LCFGS – TOP PLATE

Figure 2
Orifice Mold

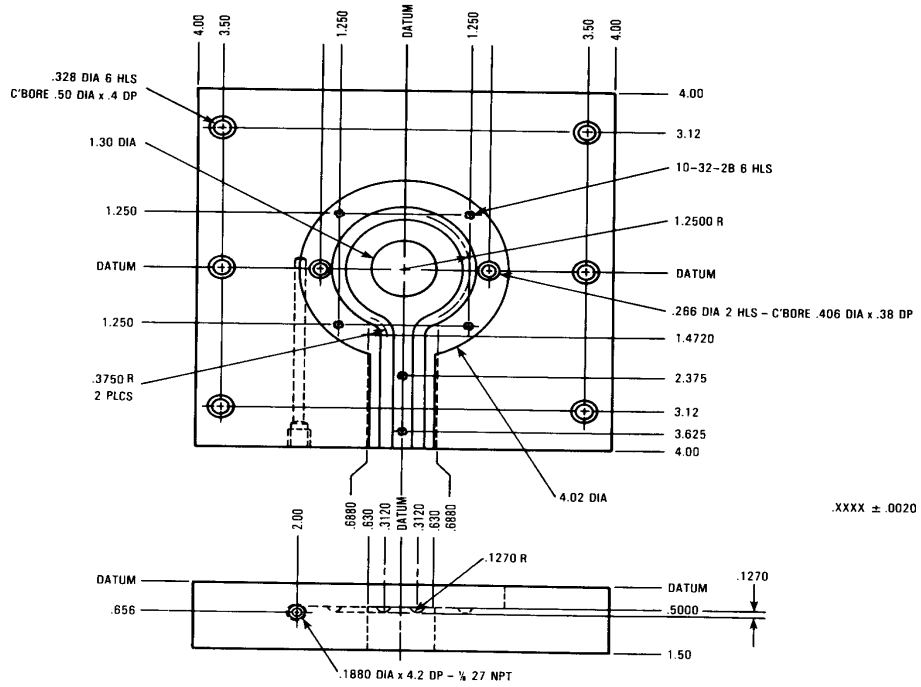


Figure 3
Top Plate

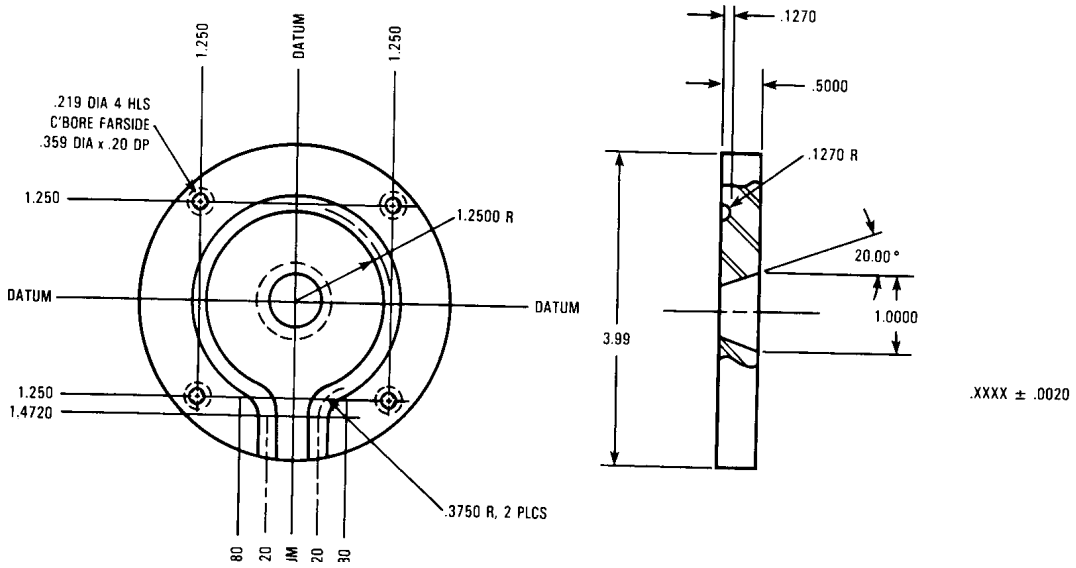


Figure 4
Orifice Holder