interaction using a generic measurement method. The signal measurement should be made with the driver loaded with reference load A (500 ohms in parallel with 2.5pF ± 0.5pF of capacitance). The following nested loop outline describes the test flow:

```
for amplitude = 1V, 3V, 5V (optional)
  for pin = 1 to n
    for edge = rising to falling
        measure the 20% to 80% transition time of a
        NR driver signal with test cycle = 10*min,
        delay = 0s  using oscilloscope (averaging = 8)
        error = maximum transition time - minimum
                transition time
    end edge
  end pin
end amplitude
```

10.4.3.2 The transition time measurements are to be made between the measured 20% and 80% points of both positive and negative signal edges, i.e., the 20% and 80% points on the signal transition edge relative to a 0% or 100% steady state level displayed on the oscilloscope. Ideally, measurement points chosen should be referenced to a steady state level that results after all aberrations in the transition have expired. Use the lowest tester pin as a reference channel when setting the measurement points for these measurements.

10.4.3.3 ATE systems may use a focused calibration routine for driver pins. That routine is intended to correct edge error due to transition time variations. In the context of executing this method for a machine that has this capability, the user of this method is advised to: 1) Execute the Drive Input Transition Time Variation test regardless, and 2) Enter the test results to the method data summary, Table 2. The entry in Table 2 for transition variation will be a reference parameter. This method as defined is incapable of making drive edge error measurements that exclude transition variation and jitter.

10.4.4 *Driver Input Timing Cycle Jitter Test*[12] — Since driver input timing jitter cannot be determined from Level 1 tests, an external instrument must be used to measure short term, cycle to cycle (or period) instability. This can be done by making period measurements of the driver-input channel under test, with a high bandwidth, digital sampling oscilloscope. A 50-ohm probe should be used to minimize measurement jitter. The tolerance for this test is ± 20ps[13] (min-max) due to the tester/instrument interaction using a generic measurement method. The measurement results are expressed as RMS. This measurement depends on the jitter distribution being Gaussian. Reference Appendix 4 for additional detail regarding this measurement. If in the application of this method it is determined that the jitter is non-Gaussian, skip this test and make the appropriate notation on the exceptions page (Appendix 3).

10.4.4.1 The following nested loop outline describes the test flow:

```
for pin = 1 to n
  for amplitude = 3V
    for test_cycle =  2*min
      for format = RTZ
          for format_delay = 50%
            for pulse_width = 50%
              for i = 1 to 1000
  meas(i) = measure the period of the pin under test
              end i
  measured signal  jitter = RMS spread of meas(1)
              through meas(1000)
            end pulse_width
          end format_delay
      end format
    end test_cycle
  end amplitude
end pin
measured instrumentation jitter = RMS spread of
      oscilloscope trigger
     (method described further in  Appendix 4)
actual RMS signal jitter = measured signal jitter -
      measured instrumentation jitter
(via sum of squares - reference Appendix 4)
```

Reference load B (50 ohms to ground) should be used for this measurement.

10.4.5 *High Speed Clock Self-trigger Cycle Jitter Test* — If the ATE is configured with dedicated high speed clock pins, an external instrument must be used to measure short term, cycle to cycle (or period) instability.

12 Trigger off the scope probe for this and the subsequent jitter test. Use a high persistence display to show signal jitter. Use of a high bandwidth-sampling oscilloscope with statistical capability is recommended. Instrumentation jitter should be extracted from the measured signal jitter, as explained in Appendix 4.

13 When recording measurement data, log all measurements as they are taken from the measurement equipment and show the associated equipment tolerances as a separate entity.

10.4.5.1 This can be done by making period measurements of the high speed clock channel under test, with a high bandwidth, digital sampling oscilloscope. A 50-ohm probe should be used to minimize measurement jitter. The tolerance for this test is ± 20ps (min-max) due to the tester/instrument interaction using a generic measurement method. The measurement results are expressed as RMS. This measurement depends on the jitter distribution being Gaussian. Reference Appendix 4 for additional detail regarding this measurement. If in the application of this method it is determined that the jitter is non-Gaussian, skip this test and make the appropriate notation on the exceptions page (Appendix 3). The following nested loop outline describes the test flow:

```
for pin = (all high speed clock pins)
 for amplitude = 3V
 for test_cycle = 10*min to min by min
     for clock_delay = 50%
       for i = 1 to 1000
meas(i) = measure the period of the clock pin under
test
       end i
measured signal jitter = RMS spread of meas(1)
      through meas(1000)
     end format_delay
   end test_cycle
  end amplitude
end pin
measured instrumentation jitter = RMS spread of
       oscilloscope trigger
      (method described further in  Appendix 4)
actual RMS signal jitter = measured signal jitter -
       measured instrumentation jitter
(via sum of squares - reference Appendix 4)
```

Reference load B (50 ohms to ground) should be used for this measurement.

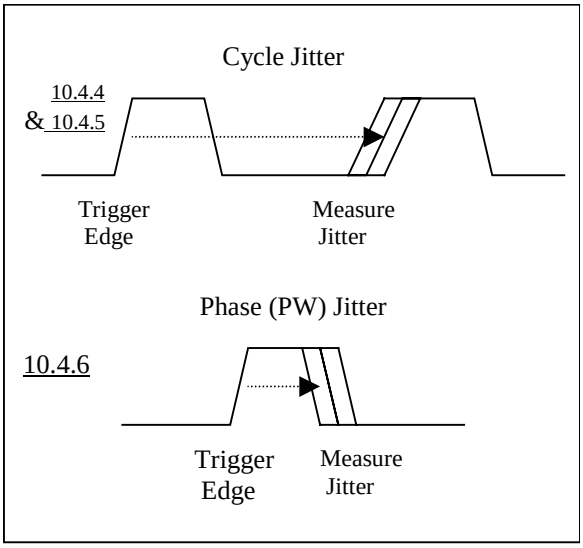


Figure 5
Jitter Tests – Sections 10.4.4, 10.4.5 and 10.4.6

10.4.6 *High Speed Clock Self-trigger Phase Jitter Test* — If the ATE is configured with dedicated high speed clock pins, an external instrument must be used to measure short term, phase (or duty cycle) instability. This can be done by making pulse width measurements of the high speed clock channel under test, using a high bandwidth, digital-sampling oscilloscope. A 50-ohm probe should be used to minimize measurement jitter. The tolerance for this test is ± 20ps[14] (min-max) due to the tester/instrument interaction using a generic measurement method. The results are expressed as RMS.

10.4.6.1 This measurement depends on the jitter distribution being Gaussian. Reference Appendix 4 for additional detail regarding this measurement. If in the application of this method it is determined that the jitter is non-Gaussian, skip this test and make the appropriate notation on the exceptions page (Appendix 3). The following nested loop outline describes the test flow:

```
for pin = (all high speed clock pins)
  for amplitude = 3V
    for test_cycle = 10*min to min by min
      for clock_delay = 50%
        for i = 1 to 1000
meas(i) = measure the pulse width of the clock pin
under test
       end i
measured signal jitter = RMS spread of meas(1)
through meas(1000)
     end format_delay
```

14 When recording measurement data, log all measurements as they are taken from the measurement equipment and show the associated equipment tolerance as a separate entity.

```
    end test_cycle
  end amplitude
end pin
measured instrumentation jitter = RMS spread of
      oscilloscope trigger
     (method described further in  Appendix 4)
actual RMS signal jitter = measured signal jitter -
      measured instrumentation jitter
(via sum of squares - reference Appendix 4)
```

Reference load B (50 ohms to ground) should be used for this measurement.

11 Data Collection Tables

11.1 Table 1 is the data collection table. Data can be manually or automatically entered to this table as this procedure is executed, depending upon how the user chooses to implement data collection.

11.2 Table 2 is intended to contain the final conclusions or analysis results of this procedure. Data for this table is taken from Table 1. Instructions for entering data to Table 2 will be described in Section 12, Reporting and Interpretation of Results, of this procedure. Examples of OTA calculations and data entry to Table 2 are contained in Appendix 2.

NOTE 4: A blank version of Table 2 is contained in Appendix 1.

12 Reporting and Interpretation of Results

12.1 *Reporting Results* — A large amount of data will be gathered when this Test Method is executed per the requirements of this method. A subset of this data should be collected into Table 1. This table contains the minimum and maximum values for the various tests contained in this Test Method.

12.1.1 Table 2 is a summary revealing the results of this Test Method. Table 2 entries will be determined from values taken out of Table 1 as well as summations of various entries occurring in Table 2. The following is a guide to making entries to Table 2:

12.1.2 *Driver Input Timing Delay Error (Section 10.4.1)* — This value is taken from Table 1. It is the difference between the minimum and maximum values shown in Table 1 for this parameter.

12.1.3 *Driver Input Timing Cycle Jitter (Section 10.4.4)* — This value is taken from Table 1. This is the RMS values shown in Table 1 for this parameter.

12.1.4 *Driver Input Transition Time Variation (Section 10.4.3)* — This value is taken from Table 1. It is the difference between the minimum and maximum values shown in Table 1 for this parameter.

12.1.5 *Driver Input Edge Placement Accuracy* — Driver Input Edge Placement by definition is the summation of Driver Input Timing Delay Error (Section 10.4.1), Driver Input Timing Cycle Jitter (Section 10.4.4), and Driver Input Transition Time Variation (Section 10.4.3). Regardless, since Drive Input Timing Delay Error measurements defined in this method do not exclude edge transition variation and jitter this entry is simply the measurements results obtained for Drive Input Timing Delay Error Level 2 (Section 10.4.1). Enter this value into Table 2 as Driver Input Edge Placement.

12.1.6 *Compare Output Time Delay Error (Section 10.4.2)* — This value is taken from Table 1. It is the difference between the minimum and maximum values shown in Table 1 for this parameter.

12.1.7 *Compare Output Edge Placement Accuracy* — Compare Output Edge Placement will be entered into Table 2 as the same entry made for Compare Output Time Delay Error (Section 10.4.2).

12.1.8 *Drive Input to Compare Output Timing Accuracy* — Data taken from Table 1 for Section 10.3.1 results: Drive Input To Compare Output Timing Accuracy = Reference – [(Min Value + Max Value)/2]. Refer to examples in Appendix 2.

12.1.9 *Overall Timing Accuracy (OTA)* — By definition and in the general case, the OTA value is the sum of Driver Input Edge Placement Accuracy, Compare Output Edge Placement Accuracy, and Driver Input to Compare Output Timing Accuracy. Examples are provided in Appendix 2 for making this entry into Table 2.

NOTE 5: For all High Speed Clock parameters shown in Table 2: High Speed Clock Delay and High Speed Clock Transition are parameters that use the same procedures as Drive Input Timing Delay and Drive Input Transition Time Variation. High Speed Clock Delay and High Speed Clock Transition are parameters provided in this procedure to accommodate those systems that have different pin electronics for the High Speed Clock function. If the system under evaluation doesn't have a High Speed Clock function, then the steps in this procedure for all High Speed Clock Accuracy are not required. High Speed Clock Cycle Jitter and High Speed Clock Phase Jitter are reference parameters with their respective test provided in this procedure to reveal accuracy for the High Speed Clock function when that function is present.

12.1.10 *High Speed Clock Delay Error (Section 10.4.1)* — This value is taken from Table 1. It is the difference between the minimum and maximum values shown in Table 1 for this parameter.

12.1.11 *High Speed Clock Cycle Jitter (Section 10.4.5)* — This value is taken from Table 1. This is the RMS values shown in Table 1 for this parameter.

12.1.12 *High Speed Clock Transition Time Variation (Section 10.4.3)* — This value is taken from Table 1. It is the difference between the minimum and maximum values shown in Table 1 for this parameter.

12.1.13 *High Speed Clock Phase Jitter (Section 10.4.6)* — This value is taken from Table 1. This is the RMS values shown in Table 1 for this parameter.

12.1.14 *High Speed Clock Accuracy* — This parameter is for systems that have a High Speed Clock function. High Speed Clock Accuracy is simply the same entry made for High Speed Clock Delay Error. High Speed Clock Transition Time Variation, High Speed Clock Cycle Jitter, and High Speed Clock Phase Jitter are reference parameters and should be entered to the appropriate location in Table 2.

12.1.15 *Driver Input Z Timing Errors (Section 10.3.5)* — There are four Drive Input Z Timing Errors. Each value is determined in the same way and is to be entered into Table 2. This value is taken from Table 1. Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1, Appendix 2.

12.1.16 *Timing Linearity (Section 10.3.1)* — This value is established from Table 1. Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1, Appendix 2. These two values should be entered at the appropriate place in Table 2.

12.1.17 *Extended Delay (Section 10.3.4)* — This value is taken from Table 1. Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1, Appendix 2.

12.1.18 *Multiple Period (Section 10.3.6)* — This parameter is optional. The test method for this parameter was defined for those systems with Timing On the Fly (OTF). If the system under evaluation does not have OTF timing data entry for this parameter is not required. Else, this value is taken from Table 1. Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1, Appendix 2.

12.2 *Interpreting Results* — Table 2 will contain summarized data, results of the Overall Digital Timing Accuracy Analysis Method for automated test systems.

12.2.1 This dialog is intended to explain the Level 1 and Level 2 results for OTA contained in Table 2 and require reference to Figure 6, Figure 7[15], and Table 2.

12.2.2 Level 1 analysis is meant to determine a test system's net conformance to the OTA specification in an efficient manner.

12.2.3 Level 2 employs external equipment to isolate parameters that contribute to OTA. That data reveals a more detailed and accurate representation to OTA conformance. Regardless, there is a limitation at getting to OTA entirely through Level 2 data collection.

12.2.4 Level 1 and Level 2 parameters are contained in Table 2 to represent OTA (Overall Timing Accuracy). Level 1 Timing Linearity (Section 10.3.1) provides analysis for all pins under comprehensive conditions and is used to acquire the drive input to compare output error parameter. Extended Delay (Section 10.3.4) complements Timing Linearity by verifying accuracy for timing generator delays beyond the length of the test cycle, and can be (optionally) used in lieu of Section 10.3.1. These two Level 1 elements represent in part OTA. Thus, this method produces a single point representation of system OTA, per the methodology defined in this method and consistent with the definition of OTA. This is done by summing Level 2 Drive Input Edge Placement Accuracy and Compare Output Edge Placement Accuracy with Level 1 Drive Input to Compare Output Timing Accuracy.

12.2.4.1 Compare side error in this method is not fully characterized or broken out into its constituent components, per the defintion of Compare Output Edge Placement Error. This method does establish Output Timing Delay Error, and its measurement contains the jitter component. But the method does not contain a way for determining Output Compare Timing Jitter by itself.

12.2.5 Establishing OTA using only Level 2 data is not possible. Only two of the three components per the standard definition of OTA can be determined. The OTA definition states: OTA is the sum of Drive Input Edge Placement, Compare Output Edge Placement, and Drive Input to Compare Output Accuracy. Level 2 analysis will collect data for the first two error components. The Level 2 parameter not achievable is Drive Input to Compare Output Accuracy. Level 1 will determine that value.

12.2.5.1 The Drive Input to Compare Output Accuracy by definition is the difference between the average of min & max drive input delay timing and the average of min & max compare output delay timing. Values for those components are in the Level 2 data, but because there is no common reference point for these two components when the data is taken, their difference cannot be established from the data at-hand.

12.2.5.2 In summary Level 2 analysis is capable of independently determining and isolating drive input timing error and compare output timing error. But, Level 2 drive input to compare output-timing error can not be established. Analysis done in Level 1 is required

15 Additional information related to Figure 7 is contained in Appendix 2.

to establish Drive Input to Compare Output timing error. Reference Figure 6.

12.2.6 As noted, Level 1 analysis does establish drive input to compare output-timing error. But, Level 1 cannot independently determine and isolate drive input timing error from compare output timing error, as was accomplished in Level 2. What this means is if the minimum to maximum drive input to compare output timing error is established as 1ns (Level 1), the method cannot create a break down such that so much of that 1ns is input error, with the remaining part of that 1ns being the output error.

12.2.7 Table 2 data also contains other valuable components of ATE error that will assist in establishing ATE timing integrity. Tests that establish the various components of Input Z Timing error, Multiple Period Tests for on the fly timing, and for systems with a High Speed Clock function tests to determine various delay, jitter and time variation errors.

12.3 A brief word on Drive Input to Compare Output Timing Accuracy will be made. Drive Input to Compare Output Timing can be described in different ways. It is easy to think of this parameter, per the definition of this aspect of OTA (reference Figure 6), as simply the relative time difference (skew) between drive input delay timing (see SEMI G79) and compare output delay timing (see SEMI G79), for a particular machine.[16] But this parameter, once established, is not necessarily constant. For example, this parameter can change from one calibration of a machine at a particular time, to something different, as a result of a subsequent calibration of that same machine. As well, Drive Input to Compare Output error can also be considered as a machine to machine accuracy parameter, not necessarily having the same value between any two machines of the same kind.

12.3.1 Thus, on each machine and at different points in time for the same machine the Drive Input to Compare Output Timing skew can be uniquely different per machine. That difference being influenced by the various machine anomalies that contribute to machine error including the not so perfect results of a periodic edge calibration.

12.3.2 In the general case drive input to compare output as shown in Figure 6 should be thought of in the context of drive/compare edges having time variance across multiple machines or as representing edges for the same machine but having variance across multiple time intervals associated with different calibrations.

12.3.3 Examination of the OTA definition in the context of Figure 6, that being the general case and not a single point timing evaluation, reveals that the overall timing accuracy time value is the time line indicated by "A" and the time line indicated by "B". In a single point AC timing evaluation, OTA is determined as a distribution of edges associated with time line "A" or time line "B", depending upon the relationship between the drive edge values and compare edge values (see SEMI G79) at that point in time.

13 Precision, Accuracy, and Precautions

13.1 *Precision and Accuracy* — Tolerances called-out in the various steps of this procedure are consistent with the required supplemental equipment specifications called for in this Test Procedure.

13.2 *Precautions* — A precaution is advised when executing this procedure to the letter. Unreliable execution or failures may occur as a result of ATE specification tradeoff that typically exists between minimum pulse width and drive signal amplitude. This can be especially true when operation is in conjunction with complex formats such as SBC. This condition is a result of specification limitations inherent in the system under evaluation. Be advised that failure conditions can occur for systems with inadequate minimum pulse width and/or inadequate comparator bandwidth characteristics operating this procedure at high frequencies with complex formats.

13.3 It is necessary to note that data in Table 1 for any particular test represents minimum and maximum values taken for all conditions specified for each test. Examples of these conditions are parameters such as frequency, formats, and different voltages. Thus the precaution lies in how the user interprets the minimum to maximum deltas. As an example, a minimum value can occur at a lower frequency whereas a maximum value for that test may occur at a higher (different) frequency. Be aware, deltas under broad conditions may be greater than deltas for a focused condition. This specification is defined to provide results for the broad case.

13.4 When entering your analysis results to Table 2 Single Point Overall Timing Accuracy (OTA), be advised that the Single Point OTA Result is represented only as indicated in Table 2, the sum of Drive Input to Compare Output Timing, Drive Input Timing Delay Error, and Compare Output Time Delay Error. This appears to deviate from the absolute definition of OTA in that Drive Input Transition and Drive Input Timing Cycle Jitter are not included. The method does not lend itself to making Drive Input Timing Delay Error measurements that exclude these two components. Per this method when the Drive Input Timing Delay Error

16 Both drive input delay timing and compare output delay timing values taken at center of spread. By definition center of spread is the average of min & max: (minerr + maxerr)/2.

measurements are made they include these two parameters. Thus, because of the measurement if included per the definition, they would be double counted.

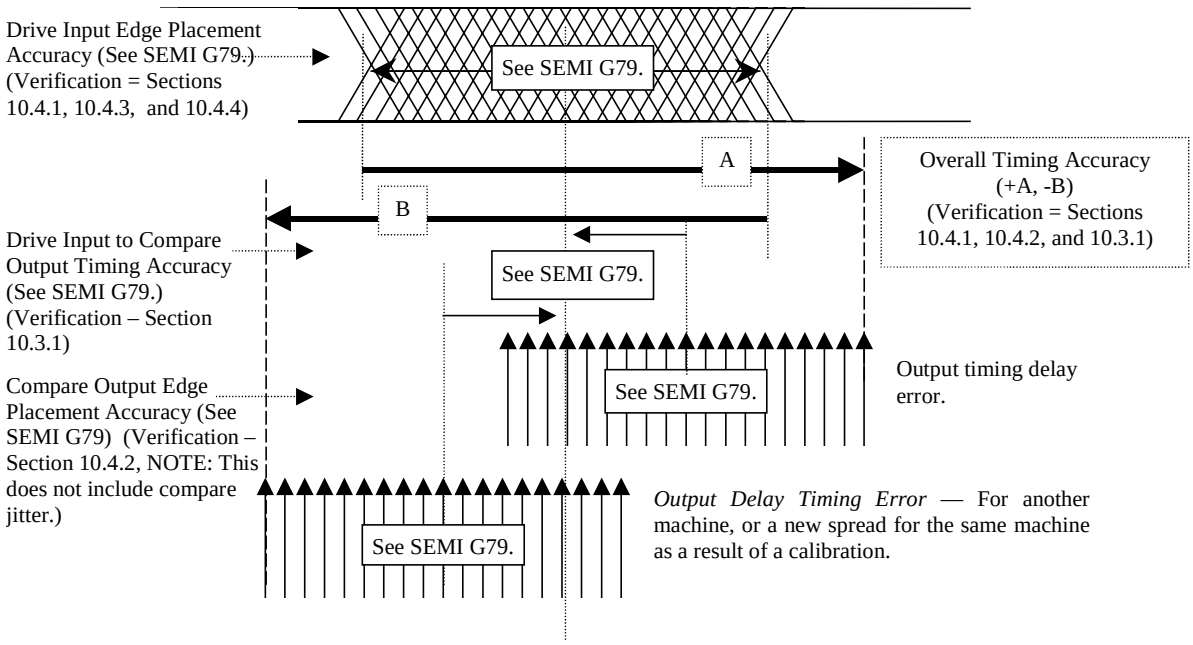
13.5 The OTA definition used in this method does not include reference parameters shown in Table 2 such as Drive Input Z Timing Error, Extended Delay, Multiple Period (timing on the fly), and High Speed Clock measurements. These are strictly reference timing parameters. This method is not defined such that they are to be included as part of OTA. Thus the user is advised not to sum any of those items as part of the OTA value entered into Table 2.

13.6 Table 2 is labeled Single Point Overall Timing Accuracy (OTA) Results. The term “single point” is used as a reminder for the user of this document that one execution of this method on a particular ATE system does not in itself constitute an overall timing accuracy conclusion for that system. It is simply a sample of the ATE's performance at some point in time. A true assessment of an ATE's performance for overall timing accuracy requires a comprehensive analysis involving data collection over an extended period of time that goes well beyond what this method provides in one pass.

13.7 In general, regarding these precautions, the user is free to adjust the procedure and data collection according to conditions consistent with the desired objective. Regardless, if the procedure is performed under anything other than full-up broad conditions, the results must be identified as a subset or partial interoperation of a single point overall timing accuracy assessment.

14 Related Documents

None.



For reference see the following definitions taken from SEMI G79:

7.1.1 *Input Edge Placement Accuracy* — DUT input timing error comprised of input timing delay error, input timing jitter and input transition time variation.

7.1.2 *Output Edge Placement Accuracy* — DUT output compare timing error comprised of output timing delay error and output compare timing jitter.

Output Timing Delay Error — time delay error at the detected midpoint of a 5V transition, with respect to an ideal delay (NIST traceable reference), using any pin, any delay value, any compare timing edge, window or strobe compare mode, expect H or L, positive or negative transition and any test cycle length.

Conditions:

- measured with load circuit "off" or high impedance
- delays normalized to rising edge detected by pin 1, using strobe compare format, expect H, @ 0ns
- error normalized to the average of min & max of the error distribution
- input signal: 50-ohm source, 0–5V step, > 1V/ns, inserted at a zero length interconnect on the DUT side of a standard performance board

Output Compare Timing Jitter — short term (cycle to cycle) instability using any pin, any compare timing edge, window or strobe compare mode, expect H or L. (NOTE: This document does not define a method for Output Compare Timing Jitter.)

Conditions:

- error expressed as RMS value
- physical reference point is a zero length interconnect on the DUT side of a standard performance board
- jitter referenced to an independent synchronous trigger

7.1.3 *Input to Output Timing Accuracy* — relative time difference between the input delay timing and output delay timing.

Figure 6
Overall Timing Accuracy (OTA)

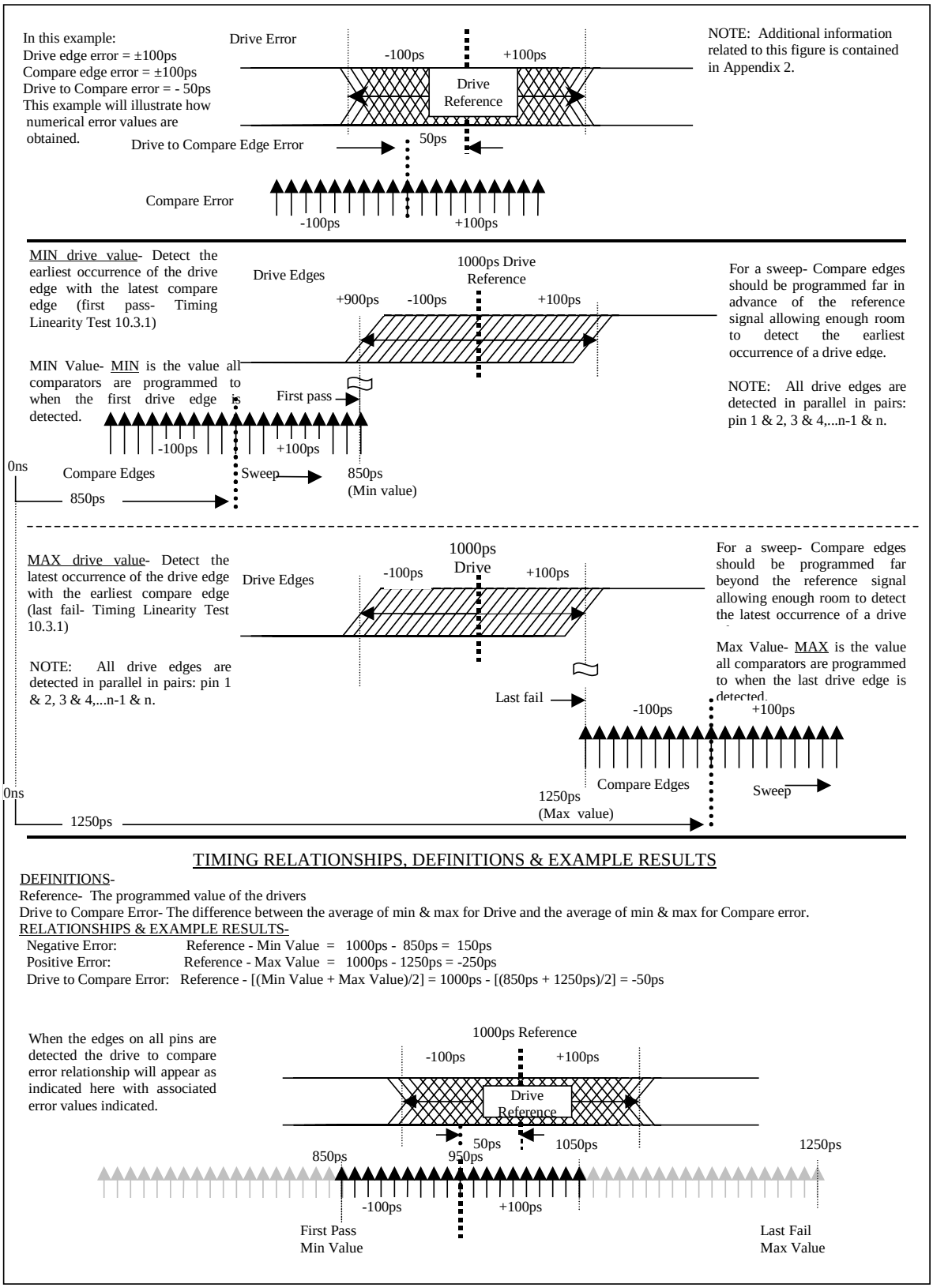


Figure 7
Level 1 Drive Edge Error = Compare Error

Table 1 Data Collection Table for Levels 1 and 2

	Test Number	*Channel Number*	*Min. Value*	*Max. Value*
LEVEL ONE	Section 10.3.1 Timing Linearity Test (Drive Input Edge Placement)	m to n		
	Section 10.3.4 Extended Delay Test (Compare Output Edge Placement)	m to n		
	Section 10.3.5 Drive Input Z Timing Error (Z to 0 (Low))	m to n		
	Section 10.3.5 Drive Input Z Timing Error (Z to 1 (High))	m to n		
	Section 10.3.5 Drive Input Z Timing Error (0 (Low) to Z)	m to n		
	Section 10.3.5 Drive Input Z Timing Error (1 (High) to Z)	m to n		
	Section 10.3.6 Multiple Period Test (Optional- for on the fly timing)	m to n		
LEVEL TWO	Section 10.4.1 Drive Input Time Delay Error (Drive Input Edge Placement)	m to n		
	Section 10.4.2 Compare Output Time Delay Error (Compare Output Edge Placement)	m to n		
	Section 10.4.3 Drive Input Transition Time Variation	m to n		
	Section 10.4.4 Drive Input Timing Cycle Jitter (Short term cycle to cycle period jitter)	m to n	*Enter RMS value only*	
	Section 10.4.5 High Speed Clock Self Trigger Cycle Jitter (Short term cycle to cycle period jitter/clocks)	m to n	*Enter RMS value only*	
	Section 10.4.6 High Speed Clock Self Trigger Phase Jitter (Short term phase /duty cycle jitter/clocks)	m to n	*Enter RMS value only*	

NOTE 6: This is a generic example of the data table needed to gather the data values for this timing analysis procedure. The actual number of table entries will depend upon the number of tester pins under evaluation. The pins to be tested are represented by the designation “m” to “n”. For Level 1 the application program is expected to fill in the minimum and maximum measurements made for each pin and specified condition. For Level 2 the user will fill-in these data values via manual entry, unless the application and implementation method employ automated/robotic operation.

Table 2 Test Method Summary Table for Establishing Overall Timing Accuracy (OTA)

LEVEL 1		LEVEL 2			
		Single Point Overall Timing Accuracy (OTA) Results *Data to enter here is: A = Dr (item 2) + Cmp (item 3) + Dr-Cmp (item 1)* *-B = -Dr (item 2) - Cmp (item 3) + Dr-Cmp (item 1).*			
Drive Z Timing *Data below represents Level 1 Z- state timing results*	**Timing Linearity Extended Delay Multiple Period** *Data below represents Level 1edge-delay results*	**1) Drive Input To Compare Output Timing** *Data to enter here is Drive Input to Compare Output (value below)*	**2) Drive Input Edge Placement** *Data to enter here = "a" below:*	**3) Compare Output Edge Placement** *Data to enter here = a) Compare Output Time Delay Error*	**High Speed Clock Accuracy** *Data to enter here = "a" below:*
Drive Input Z Timing Error Level 1 (Section 10.3.5) Z to 0 (Low)- Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1 Appendix 2.	Timing Linearity Level 1 (Sec.10.3.1) Data to enter here is Positive Error & Negative Error per the data in Table 1 and the 2 equations: Positive Error = Reference - Max Value Negative Error = Reference -Min Value	Drive Input to Compare Out put Timing Accuracy calculated from 10.3.1 data as: Reference - [(MinValue+Max Value)/2]. Refer to examples in Appendix 2.	a) Drive Input Timing Delay Error Level 2 (Section 10.4.1)- Data to enter here = the delta between the min and max values in Table 1.	a) Compare Output Time Delay Error Level 2 (Section 10.4.2) Data to enter here = the delta between the min and max values in Table 1.	a) High Speed Clock Delay Error (Section 10.4.1- same as Drive Input Timing Delay but for clock pins) Data taken and entered for these pins equivalent to Drive Input Timing
Drive Input Z Timing Error Level 1 (Section 10.3.5) Z to 1 (High)- Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1 Appendix 2.	Extended Delay Level 1 (Sec. 10.3.4)- Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1 Appendix 2.		b) Drive Input Transition Time Variation Level 2 (Section 10.4.3) - Data to enter here = the delta between the min and max values in Table 1.	b) Compare Output Timing Jitter (Note: no method exists for this test)	b) High Speed Clock Transition time variation (Section 10.4.3- same as drive input transition time but for clock pins) Data entry equivalent to Drive Input Transition Time.
Drive Input Z Timing Error Level 1 (Section 10.3.5) 0 (Low) to Z - Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1 Appendix 2.	Multiple Period Level 1 Optional (Sec. 10.3.6) Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1 Appendix 2.		c) Drive Input Timing Cycle Jitter Level 2 (Section 10.4.4) Data to enter here = the RMS value in Table 1.		c) High Speed Clock Self Trigger Cycle Jitter Level 2 (Section 10.4.5) Data to enter here = the RMS value in Table 1.
Drive Input Z Timing Error Level 1 (Section 10.3.5) 1 (High) to Z- Data to enter here is Positive Error and Negative Error per the data in Table 1 and Equation 1 Appendix 2.					d) High Speed Clock Self Trigger Phase Jitter Level 2 (Section 10.4.6)- Data to enter here = the RMS value in Table 1.

The user of the method is advised to read Section 13, Precautions before filling in this table.

Table 2 (cont.) Test Method Summary - Non Data Analysis Aspects Associated with This Method

1. Level 1 — Procedure Start Date and Time:	
2. Level 1 — Procedure Finish Date and Time:	
3. Level 2 — Procedure Start Date and Time:	
4. Level 2 — Procedure Finish Data and Time:	
5. Specify the Ambient Temperature when this method was executed.	
6. Manufacturer's model number and/or name for this system analyzed.	
7. System Serial Number:	
8. Date & Time of Last System Calibration:	
9. Specify PARTIAL or Full-Up execution of this method. Exceptions noted in Appendix 3.	
10. Specify Number of Test Heads & Number of Pins analyzed using this method.	

APPENDIX 1

NOTE: The material in this appendix is an official part of SEMI G80 and was approved by fulll letter ballot procedures on September 3, 1999 by the North Amerian Regional Standards Committee.

Table A1-1 Test Method Summary Table for Establishing Overall Timing Accuracy (OTA)

LEVEL 1		LEVEL 2			
		Single Point Overall Timing Accuracy (OTA) Results *Data to enter here is: A = Dr (item 2) + Cmp (item 3) + Dr-Cmp (item 1)* *-B = -Dr (item 2) - Cmp (item 3) + Dr-Cmp (item 1).*			
Drive Z Timing *Data below represents Level 1 Z-state timing results*	**Timing Linearity Extended Delay Multiple Period** *Data below represents Level 1 edge-delay results*	**1) Drive Input To Compare Output Timing** _____	**2) Drive Input Edge Placement** _____	**3) Compare Output Edge Placement** _____	**High Speed Clock Accuracy** _____
Drive Input Z Timing Error Level 1 (Section 10.3.5) Z to 0 (Low) _____ _____	Timing Linearity Level 1 (Sec.10.3.1) Positive Error: _____ Negative Error: _____	Drive Input to Compare Out put Timing Accuracy calculated from the 10.3.1 entry. _____	a) Drive Input Timing Delay Error Level 2 (Section 10.4.1) _____	a) Compare Output Time Delay Error Level 2 (Section 10.4.2) _____	a) High Speed Clock Delay Error Level 2 (Section 10.4.1- Drive Input Timing Delay for clock function) _____
Drive Input Z Timing Error Level 1 (Section 10.3.5) Z to 1 (High) _____ _____	Extended Delay Level 1 (Sec. 10.3.4) Positive Error: _____ Negative Error: _____		b) Drive Input Transition Time Variation Level 2 (Section 10.4.3) _____		b) High Speed Clock Transition Time Variation Level 2 (Section 10.4.3- Drive Input Transition Time for clock function) _____
Drive Input Z Timing Error Level 1 (Section 10.3.5) 0 (Low) to Z _____ _____	Multiple Period Level 1 Optional (Sec. 10.3.6) Positive Error: _____ Negative Error: _____		c) Drive Input Timing Cycle Jitter Level 2 (Section 10.4.4) _____		c) High Speed Clock Cycle Jitter Level 2 (Section 10.4.5) _____
Drive Input Z Timing Error Level 1 (Section 10.3.5) 1 (High) to Z _____ _____					d) High Speed Clock Phase Jitter Level 2 (Section 10.4.6) _____

The user of the method is advised to read Section 13, Precautions before filling in this table.

Table A1-1 (cont.) Test Method Summary - Non Data Analysis Aspects Associated with This Method

1. Level 1 — Procedure Start Date and Time:	
2. Level 1 — Procedure Finish Date and Time:	
3. Level 2 — Procedure Start Date and Time:	
4. Level 2 — Procedure Finish Data and Time:	
5. Specify the ambient temperature when this method was executed.	
6. Manufacturer's model number and/or name for this system analyzed.	
7. System Serial Number:	
8. Date and Time of Last System Calibration:	
9. Specify PARTIAL or Full-Up execution of this method. Exceptions noted in Appendix 3.	
10. Specify number of Test Heads and number of Pins analyzed using this method.	

APPENDIX 2

NOTE: The material in this appendix is an official part of SEMI G80 and was approved by fulll letter ballot procedures on September 3, 1999 by the North Amerian Regional Standards Committee.

A2-1 Examples

NOTE 1: This appendix contains Figures A2-1, A2-2, A2-3, and A2-4 created for this method as examples. The purpose of these examples is to show that Drive Input To Compare Output Error (Accuracy) can be determined. Establishing this value requires that two edge timing values be detected: MIN DRIVE VALUE: the earliest occurrence the drive edges with the latest compare edge. That is also referred to here as FIRST PASS. MAX DRIVE VALUE: the latest occurrence of the drive edges with the earliest compare edge. That is also referred to here as LAST FAIL.

NOTE 2: Timing Linearity Test 10.3.1 can provide these values. Examples in this appendix will also show data entry to Table 2 for OTA calculation.

A2-1.1 *Maximum Drive Value and Minimum Drive Value* — To follow this analysis you can refer to the example in Figure 7. In this example drive error and compare error are each 100ps.

NOTE 3: Figures A2-1, A2-2, A2-3, and A2-4 are equivalent and represent complementary examples for the cases where drive error does not have the same error value as compare error.

A2-1.2 Minimum Drive Value is determined by first assuming that all compare edges are programmed at 0ns. You must then take into account the drive to compare error, in this example that value is –50ps (note the sign indicating the shift is in the negative direction). Add the drive to compare error to the compare programming value. That means that the average (mean) compare edge can be thought of as actually occurring at –50ps (versus the programmed value of 0ns). Per this example the compare error is ± 100ps, which means the latest compare edge would occur at + 50ps (–50ps + 100ps). Since the driver edge error is also ± 100ps and is programmed to the reference value of 1000ps, the earliest drive edge occurs at 900ps (1000ps minus 100ps). The MIN DRIVE VALUE is then whatever programming value is needed to get the latest compare edge (at + 50ps) to line up with the earliest drive edge (at 900ps). In this case that's 850ps (the difference between 50ps and 900ps). This value of 850ps is also referred to at the FIRST PASS.

A2-1.3 The same analysis applies when determining Max Drive Value. First assume all compare edges are programmed to 0ns. The drive to compare error must be added-in, in this case –50ps. That puts the mean programmed compare edge at –50ps. Taking into account the compare edge error of 100ps the earliest compare edge would occur at –150ps. The drive edges are programmed to 1000ps. Thus the latest drive edge occurs at 1100ps when the 100ps drive edge error is taken onto account. To get the earliest compare edge to line up with the latest drive edge 1250ps of delay would need to be programmed (the difference between 1100ps and –150ps). This value of 1250ps is referred to as the LAST FAIL.

A2-1.4 *Drive to Compare Edge Error* — By definition DRIVE TO COMPARE EDGE ERROR is the relative time difference between the drive (input) edge error and compare (output) edge error distributions. All drive edges in Level 1 are detected in parallel in pairs. Once the minimum and maximum values of drive edge are determined per procedure 10.3.1 (illustrated in Figures A2-1 through A2-4) determination of drive to compare edge error can be established. As per these examples (Figures 7 and A2-1 through A2-4) the drive to compare edge error is calculated as the reference value minus the average of min and max error values:

Drive to Compare Error =
Reference-[Min Value + Max Value)/2]

A2-1.5 *Distinguishing Drive and Compare Edge Error Uniquely Is Not Possible with Level 1 Tests* — The user is cautioned that even though drive to compare edge error is known, per this method it is still not possible to distinguish Level 1 drive input error from compare output error. The key to this shortcoming lies in observation of examples shown in Figures A2-1 thorough A2-4. These examples have drive and compare edge error values that are not the same value. That is, drive error is either much greater that compare edge error, or vice versa. In each example drive to compare edge error is established. To establish the point that drive input error cannot be distinguished from compare output error per level 1, the user is asked to look at Figures A2-1 and A2-2. In these two examples it is assumed that the drive error and compare error are different by a factor of two. Because of limited visibility per the level 1 approach it is not possible to determine that the drive error is ± 100ps and the compare error is ± 50ps (example in Figure A2-1), or vice versa. All that can be established is that the positive error is 200ps and the negative error is 100ps. Level 2 tests are required to determine drive input timing error and compare output timing error.

A2-1.6 The same rationale applies for the examples in Figure A2-3 and A2-4 where one component of error is assumed to be 200ps and the other is 100ps, with a 50ps drive to compare error. The drive to compare edge error is determined, but again establishing a unique value for drive or a unique value compare error is not

possible in Level 1. All that is known per Level 1 analysis is that the positive error is 350ps and the negative error is 250ps.

A2-1.4 *Positive and Negative Error* — EQUATION 1: Per the examples in this Appendix and data taken out of Table 1:

Positive Error = Reference - Max Value
Negative Error = Reference - Min Value

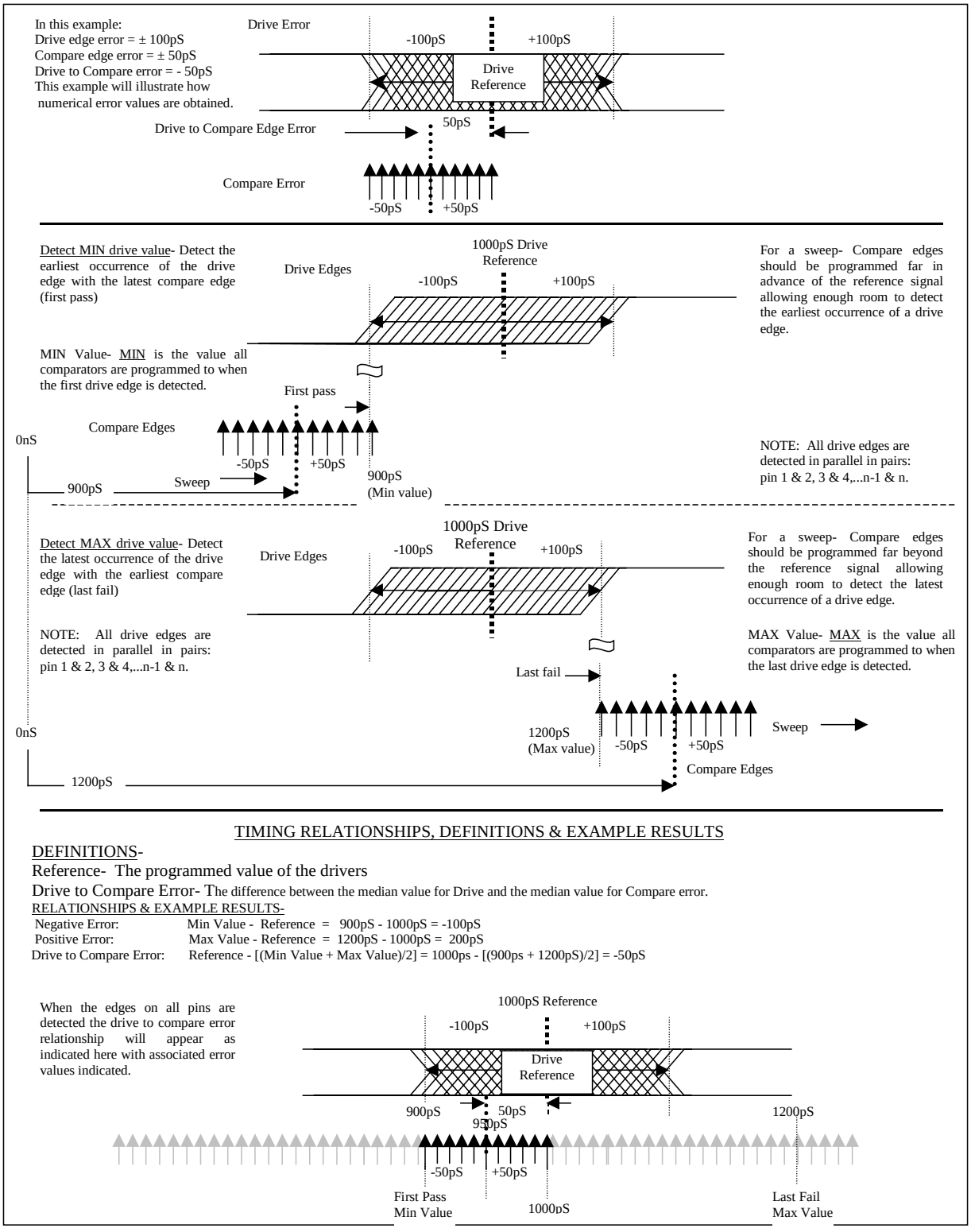


Figure A2-1
Level 1 Compare Edge Error << Drive Edge

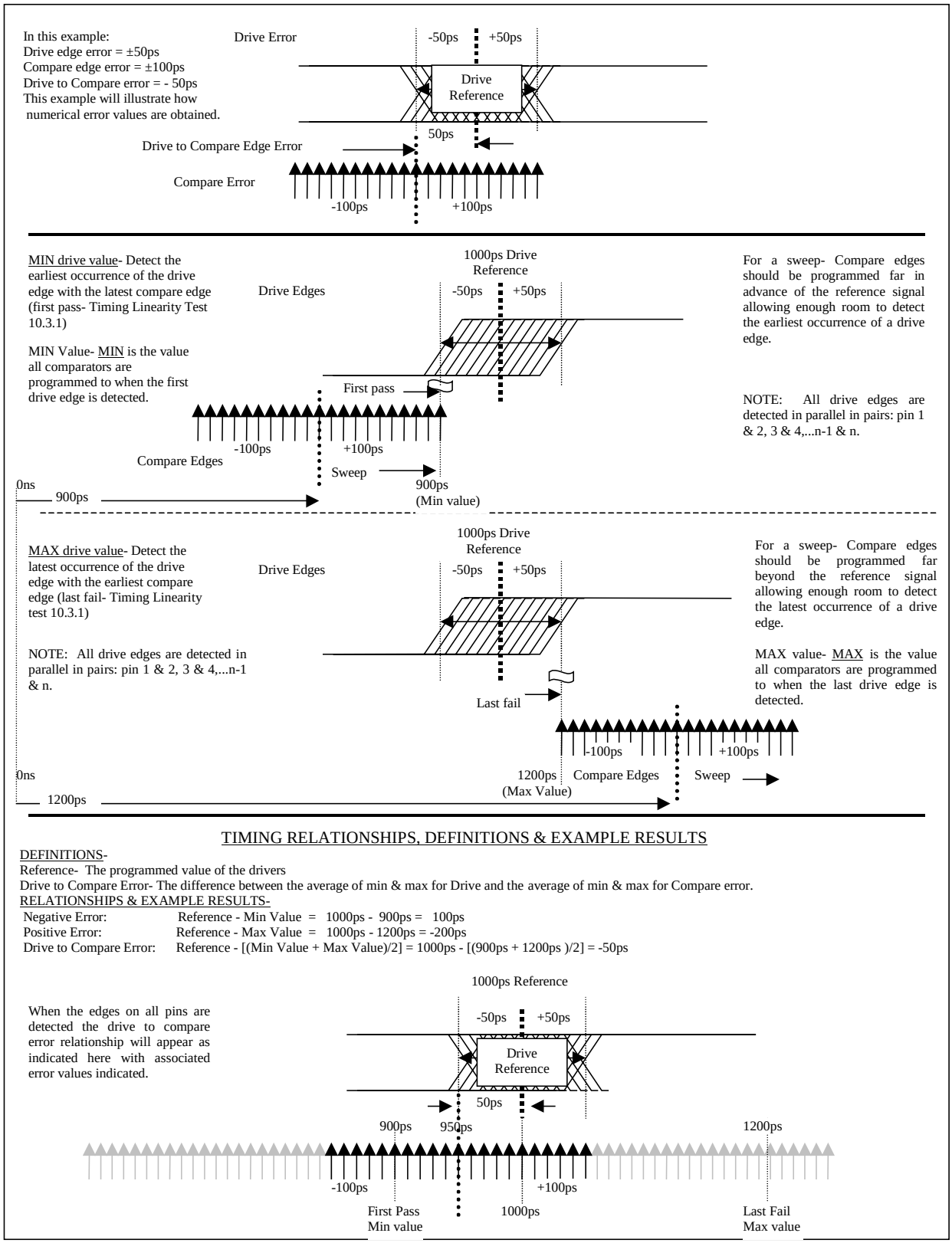


Figure A2-2
Level 1 Drive Edge Error << Compare Edge Error

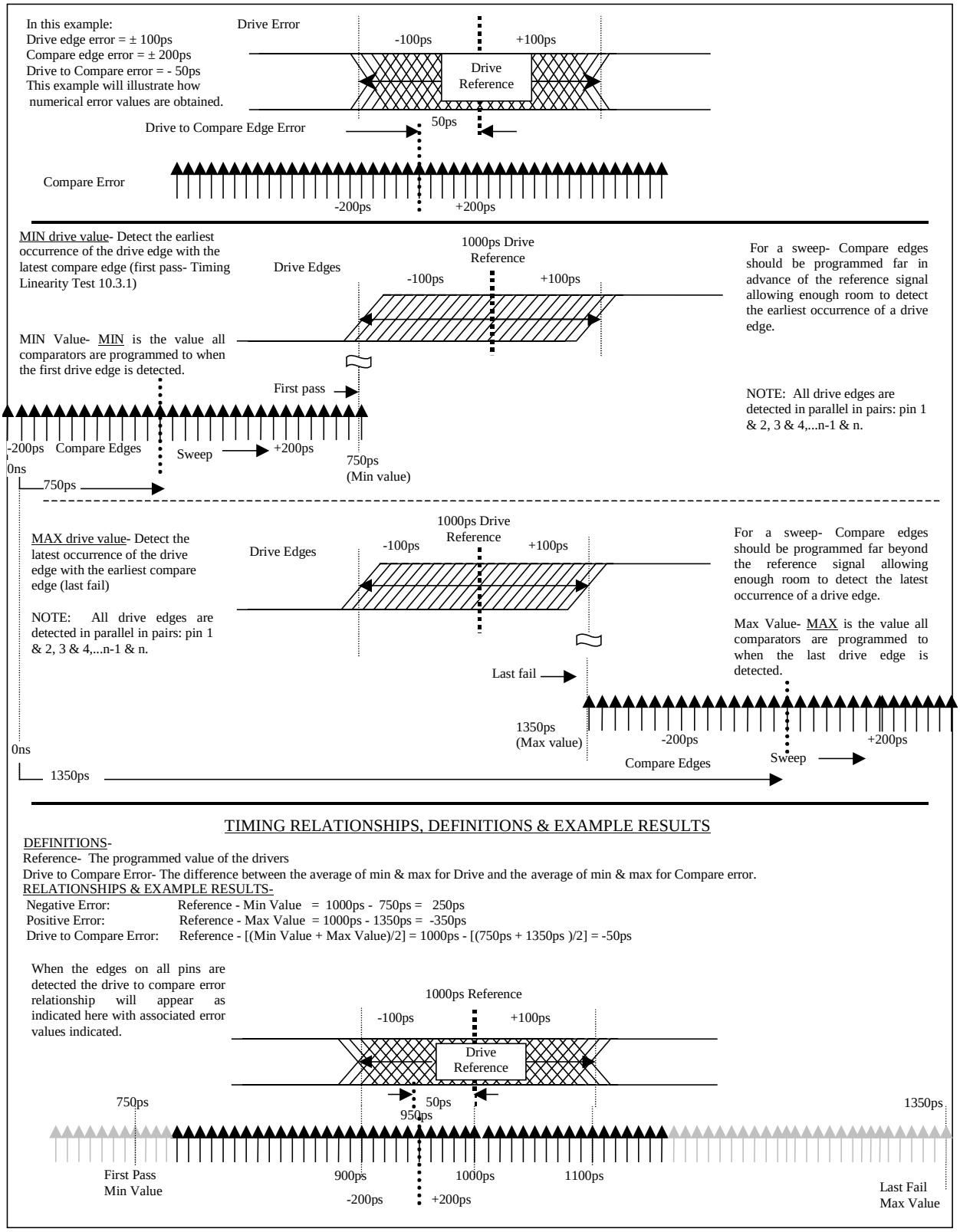


Figure A2-3
Level 1 Compare Edge Error >> Drive Edge Error

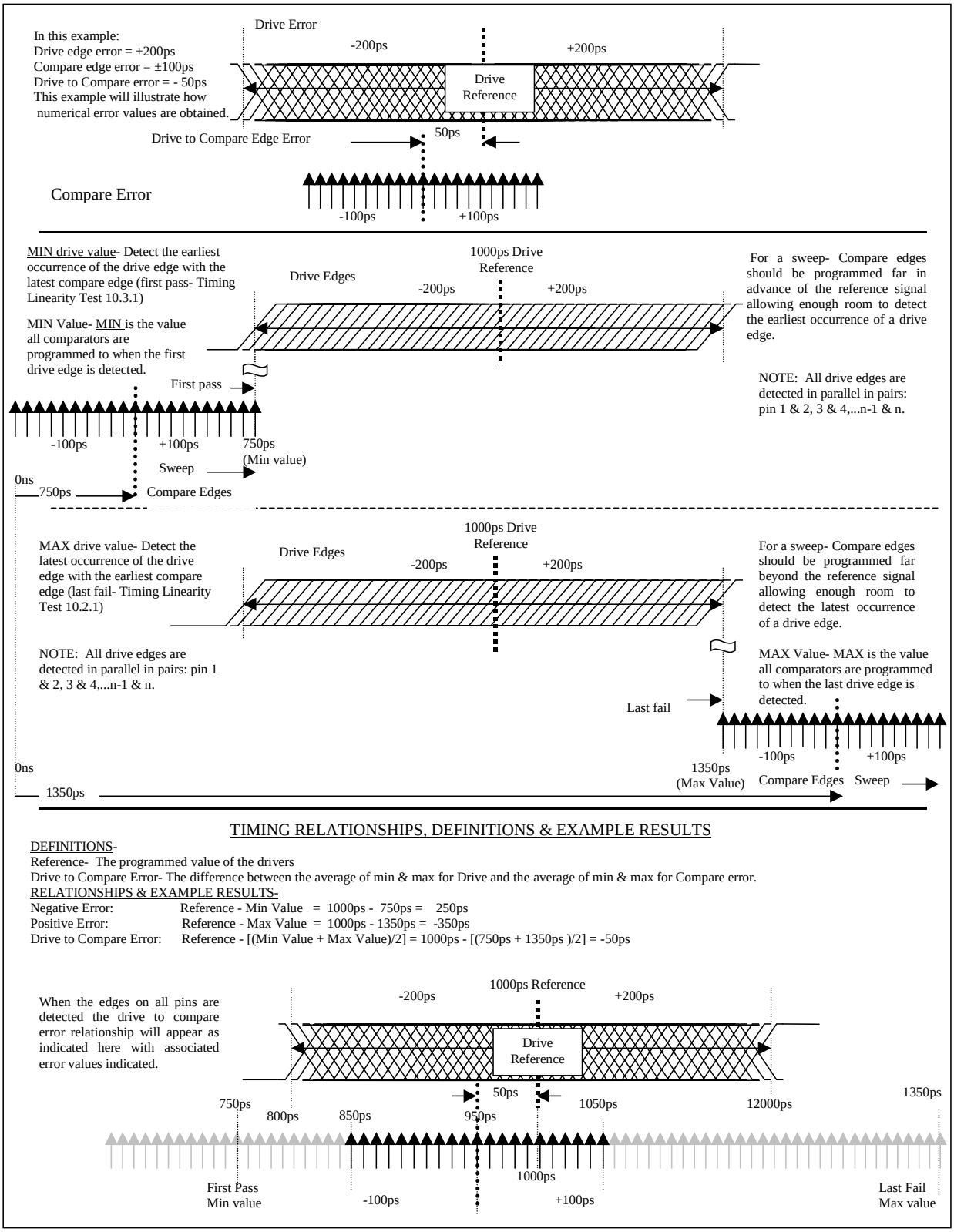


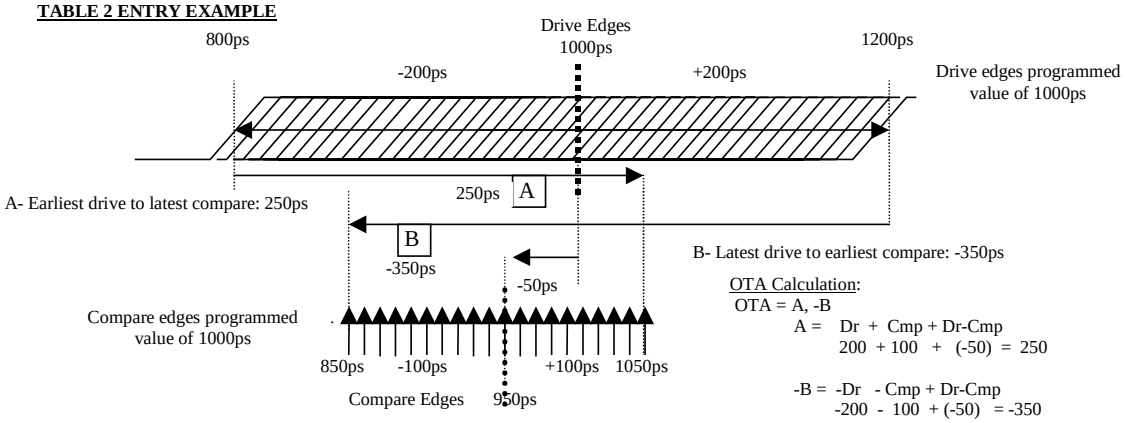
Figure A2-4
Drive Edge Error >> Compare Edge Error

Example A2-5 Test Method Summary for Showing Data Entry to Table 2 for OTA Calculation

LEVEL 1		Single Point Overall Timing Accuracy (OTA) Results *Data to enter here is: A = Dr (item 2) + Cmp (item 3) + Dr-Cmp (item 1)* *-B = -Dr (item 2) - Cmp (item 3) + Dr-Cmp (item 1).* **+250ps, –350ps**			LEVEL 2
Drive Z Timing *Data below represents Level 1 Z-state timing results*	**Timing Linearity Ext. Dly. / Mult Period** *Data below represents Level 1 edge-delay results*	**1) Drive Input To Compare Output Timing** –50	**2) Drive Input Edge Placement** ±200	**3) Compare Output Edge Placement** ±100	**High Speed Clock Accuracy** _____
Drive Input Z Timing Error Level 1 (Section 10.3.5) Z to 0 (Low)	Timing Linearity Level 1 (Sec.10.3.1) Positive Error: **+250** Negative Error: **–350**	Drive Input to Compare Out put Timing Accuracy Taken from 10.3.1 **–50**	a) Drive Input Timing Delay Error Level 2 (Section 10.4.1) **±200**	a) Compare Output Time Delay Error Level 2 (Section 10.4.2) **±100**	a) High Speed Clock Delay Error Level 2 (Section 10.4.1- Drive Input Timing Delay for clock function)
Drive Input Z Timing Error Level 1 (Section 10.3.5) Z to 1 (High)	Extended Delay Level 1 (Sec. 10.3.4) Positive Error: Negative Error:		b) Drive Input Transition Time Variation Level 2 (Section 10.4.3)		b) High Speed Clock Transition Time Variation Level 2 (Section 10.4.3- Drive Input Transition Time for clock function)
Drive Input Z Timing Error Level 1 (Section 10.3.5) 0 (Low) to Z	Multiple Period Level 1 Optional (Sec. 10.3.6) Positive Error: Negative Error:		c) Drive Input Timing Cycle Jitter Level 2 (Section 10.4.4)		c) High Speed Clock Cycle Jitter Level 2 (Section 10.4.5)
Drive Input Z Timing Error Level 1 (Section 10.3.5) 1 (High) to Z					d) High Speed Clock Phase Jitter Level 2 (Section 10.4.6)

The user of the method is advised to read Section 13, Precautions before filling in this table.

OTA DATA CALCULATION and TABLE 2 ENTRY EXAMPLE



OTA Calculation:

OTA = A, -B

A = Dr + Cmp + Dr-Cmp

200 + 100 + (-50) = 250

-B = -Dr - Cmp + Dr-Cmp

-200 - 100 + (-50) = -350

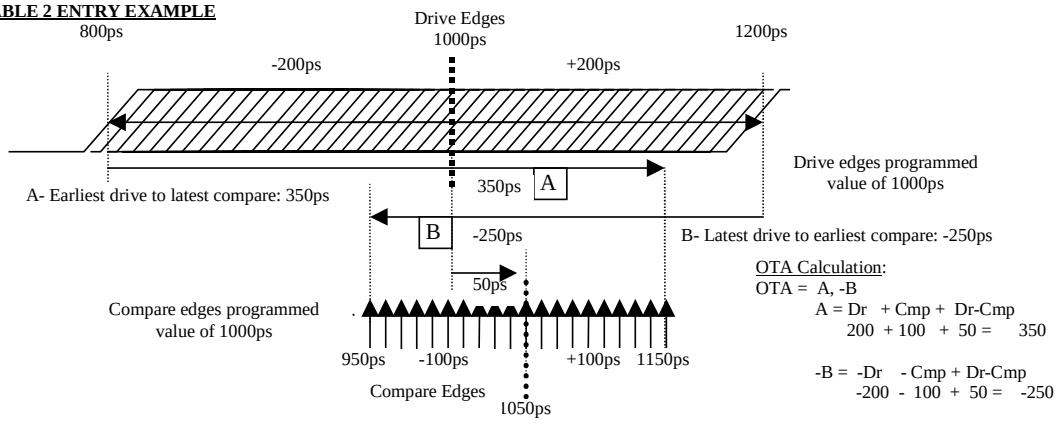
OTA = 250ps, -350ps

Example A2-6 Test Method Summary for Showing Data Entry to Table 2 for OTA Calculation

LEVEL 1		Single Point Overall Timing Accuracy (OTA) Results *Data to enter here is: A = Dr (item 2) + Cmp (item 3) + Dr-Cmp (item 1)* *-B = -Dr (item 2) - Cmp (item 3) + Dr-Cmp (item 1).* **+350ps, –250ps**			LEVEL 2
Drive Z Timing *Data below represents Level 1 Z-state timing results*	**Timing Linearity Ext. Dly. / Mult Period** *Data below represents Level 1 edge-delay results*	**1) Drive Input To Compare Output Timing** **+50**	**2) Drive Input Edge Placement** **± 200**	**3) Compare Output Edge Placement** **±100**	**High Speed Clock Accuracy** _____
Drive Input Z Timing Error Level 1 (Section 10.3.5) Z to 0 (Low)	Timing Linearity Level 1 (Sec.10.3.1) Positive Error: **+350** Negative Error: **–250**	Drive Input to Compare Out put Timing Accuracy Taken from Section 10.3.1 **+50**	a) Drive Input Timing Delay Error Level 2 (Section 10.4.1) **± 200**	a) Compare Output Time Delay Error Level 2 (Section 10.4.2) **± 100**	a) High Speed Clock Delay Error Level 2 (Section 10.4.1- Drive Input Timing Delay for clock function)
Drive Input Z Timing Error Level 1 (Section 10.3.5) Z to 1 (High)	Extended Delay Level 1 (Sec. 10.3.4) Positive Error: Negative Error:		b) Drive Input Transition Time Variation Level 2 (Section 10.4.3)		b) High Speed Clock Transition Time Variation Level 2 (Section 10.4.3- Drive Input Transition Time for clock function)
Drive Input Z Timing Error Level 1 (Section 10.3.5) 0 (Low) to Z	Multiple Period Level 1 Optional (Sec. 10.3.6) Positive Error: Negative Error:		c) Drive Input Timing Cycle Jitter Level 2 (Section 10.4.4)		c) High Speed Clock Cycle Jitter Level 2 (Section 10.4.5)
Drive Input Z Timing Error Level 1 (Section 10.3.5) 1 (High) to Z					d) High Speed Clock Phase Jitter Level 2 (Section 10.4.6)

The user of the method is advised to read Section 13, Precautions before filling in this table.

OTA DATA CALCULATION and TABLE 2 ENTRY EXAMPLE



OTA Calculation:
OTA = A, -B
A = Dr + Cmp + Dr-Cmp
200 + 100 + 50 = 350

-B = -Dr - Cmp + Dr-Cmp
-200 - 100 + 50 = -250

OTA = 350, –250

APPENDIX 3
EXCEPTIONS PAGE

NOTE: The material in this appendix is an official part of SEMI G80 and was approved by fulll letter ballot procedures on September 3, 1999 by the North Amerian Regional Standards Committee.

NOTE 2: This page is intended to capture any Digital Timing Accuracy Analysis Method exceptions the user has chosen to make.

Test Number		*NOTE 3: MAKE ATTACHMENTS AS NEEDED*
LEVEL ONE	Section 10.3.1 Timing Linearity Test (Drive Input Edge Placement)	
	Section 10.3.4 Extended Delay Test (Compare Output Edge Placement)	
	Section 10.3.5 Drive Input Z Timing Error (Z to 0 (Low))	
	Section 10.3.5 Drive Input Z Timing Error (Z to 1 (High))	
	Section 10.3.5 Drive Input Z Timing Error (0 (Low) to Z)	
	Section 10.3.5 Drive Input Z Timing Error (1 (High) to Z)	
	Section 10.3.6 Multiple Period Test (Optional- for on the fly timing)	
LEVEL TWO	Section 10.4.1 Drive Input Time Delay Error (Drive Input Edge Placement)	
	Section 10.4.2 Compare Output Time Delay Error (Compare Output Edge Placement)	
	Section 10.4.3 Drive Input Transition Time Variation	
	Section 10.4.4 Drive Input Timing Cycle Jitter (Short term cycle to cycle period jitter)	
	Section 10.4.5 High Speed Clock Self Trigger Cycle Jitter (Short term cycle to cycle period jitter/clocks)	
	Section 10.4.6 High Speed Clock Self Trigger Phase Jitter (Short term phase/duty cycle jitter/clocks)	

APPENDIX 4

NOTE: The material in this appendix is an official part of SEMI G80 and was approved by fulll letter ballot procedures on September 3, 1999 by the North Amerian Regional Standards Committee.

A4-1 Jitter Measurement

A4-1.1 If a jitter measurement described here is to be statistically correct the jitter variation in the signal being measured must be Gausian. The measured jitter in this method will be represented as one standard deviation (sigma) of the Gausian distribution, referred to here as the RMS jitter value.

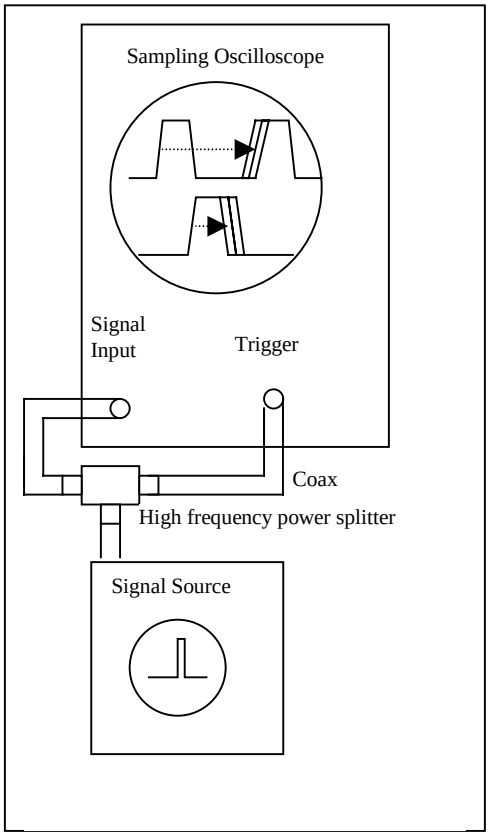


Figure A4-1
Signal Jitter Measurement

A4-1.2 The signal being measured will have some amount of jitter. The instrumentation used to measure the jitter will also have some amount of jitter. To accurately measure the jitter of a periodic signal the jitter component of the instrumentation must be accounted for and subtracted from the signal being measured.

A4-1.3 Two jitter measurements are required. A jitter measurement will be made on the signal of interest. A second jitter measurement will be made to determine the instrumentation jitter. Instrumentation jitter will be subtracted from the signal measurement to obtain the most accurate representation of signal jitter.

A4-1.4 A sampling oscilloscope will have an inherent delay, typically on the order of 20ns. This represents the time difference from the time the oscilloscope is triggered to the time when an input signal can be viewed. The key to extracting the jitter of the measurement instrumentation is providing a setup that allows viewing the trigger on the oscilloscope display. This is accomplished by delaying the oscilloscope trigger to an input channel.

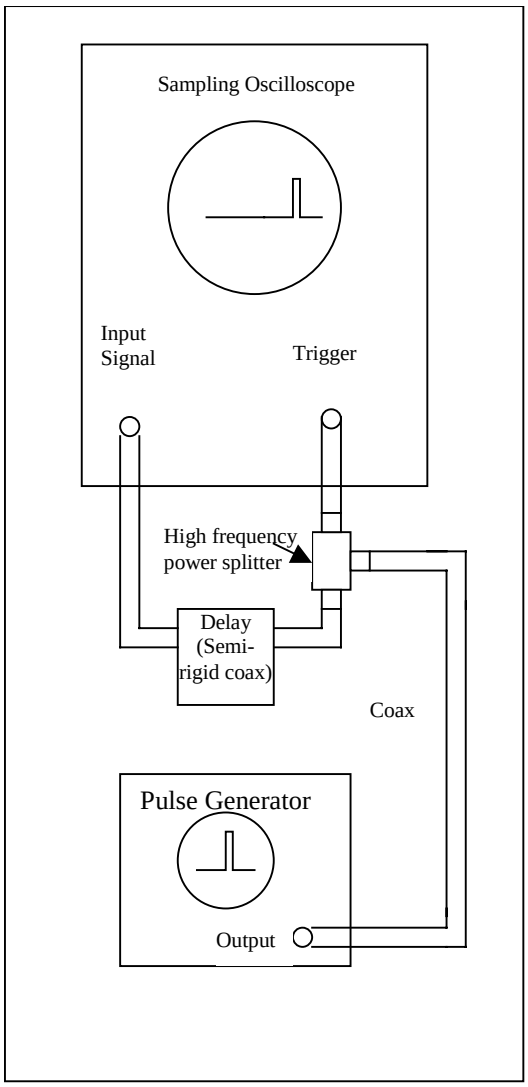


Figure A4-2
Measuring Instrumentation Jitter

A4-1.4.1 The amount of delay to the input channel must be greater than the inherent delay of the oscilloscope.

A4-1.5 A high bandwidth-sampling oscilloscope with statistical calculation capability is recommended. In addition, when making low jitter measurements high quality RF connectors and cables will be required. A setup similar to that shown in Figure A4-2 is adequate for extracting instrumentation jitter.

A4-1.6 Using semi-rigid coax for the delay will minimize loss of signal. The pulse generator should be set to low frequency to maximize the pulse width. A period of 10MHz with a 50ns pulse width is adequate for an oscilloscope with an inherent delay of 20ns . The semi-rigid coax length should be chosen to have a delay slightly larger than the inherent delay of the oscilloscope. The proper amount of delay allows viewing the trigger signal with minimal oscilloscope horizontal delay.

A4-2 *Procedure*

A4-2.1 A signal measurement will be made as indicated in Figure A4-1. The semi-rigid coax (delay) is not used, but the power splitter output will be connected to the oscilloscope input. As well, the input to the power splitter is connected to the signal being measured. The scope is triggered from the input signal, and the signal being viewed is delayed from the trigger by an amount equal to the inherent delay of the oscilloscope. This measurement step provides a value referred to here as MEASURED RMS SIGNAL JITTER, MS.[17]

A4-2.2 An instrumentation jitter measurement is then made as indicated in Figure A4-2. Per this arrangement the signal being displayed is the same signal that triggered the oscilloscope. That connection scheme cannot produce any signal jitter between the trigger and the signal being viewed; thus any jitter shown on the oscilloscope display represents instrumentation jitter. This measurement step provides a value referred to here as MEASURED RMS INSTRUMENTATION JITTER, MI.

A4-2.3 Since the signal jitter being measured is Gausian, the sum of squares relationship is used to subtract out the instrumentation jitter, and thus obtain ACTUAL RMS SIGNAL JITTER, AS.

$$MS = (MI^2 + AS^2)^{1/2}$$

MS- Measured RMS signal jitter.

MI- Measured RMS instrumentation jitter.

AS- Actual RMS signal jitter.

17 Use of a loop-through sampling head is an alternative method for making this measurement.

A4-3 *Example*

A4-3.1 Measured RMS signal jitter MS, the signal being measured, results in a 10ps measurement.

A4-3.2 Measured RMS instrumentation jitter MI, the jitter of the measurement setup, results in a 5ps measurement.

A4-3.3 The actual RMS signal jitter AS is determined from the relationship:

$$MS = MI^2 + AS^2)^{1/2}$$

and calculates to be:

$$10^2 = 5^2 + AS^2$$

$$100 = 25 + AS^2$$

$$75 = AS^2$$

$$75^{1/2} = AS$$

8.66ps = AS (actual RMS signal jitter)

Since the jitter is Gaussian, the max value of jitter is approximately equal to 5 or 6 times the RMS value of the jitter.

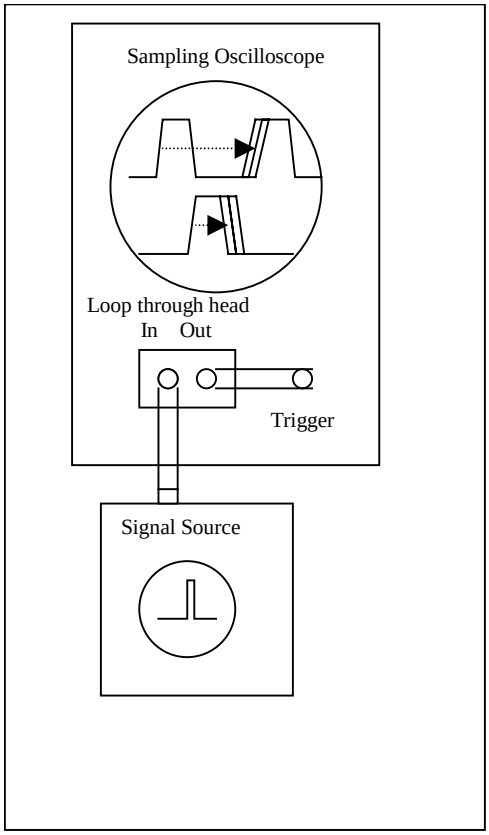


Figure A4-3
Use of a Loop-Through Sampling Head

A4.4 *Use of a Loop-Through Sampling Head*

A4-4.1 This is an alternate approach to measured RMS signal jitter. The input signal is routed through the loop-through sampling head where it is sampled and sent to the output of the sampling head. The head output is connected to the oscilloscope trigger. (See Figure A4-3.)

A4-4.2 *What is Observed When Making MS And MI Measurements* — This dialog is meant to provide further clarification for making jitter measurements. This is an example that applies to a jitter measurement using an oscilloscope with an inherent oscilloscope delay of 20ns. The signal frequency is 100MHz (period of 10ns). The semi-rigid coax delay is set to the inherent oscilloscope delay of 20ns.

A4-4.3 *Measured RMS Signal Jitter, MS* — For the MS measurement the observed edge occurs subsequent to the edge that triggered the oscilloscope:

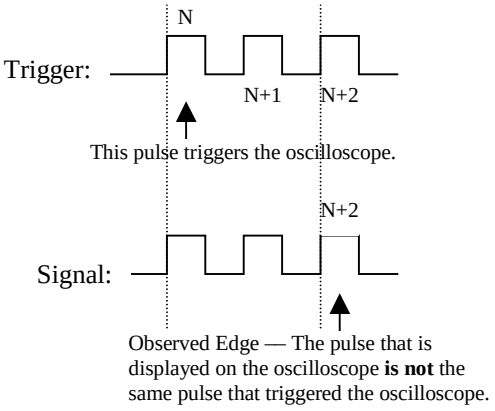


Figure A4-4
Measured RMS Signal Jitter, MS

A4-4.4 The observed edge depends upon the signal frequency; thus what is displayed is subsequent to the trigger pulse permitting signal jitter to be observed.

A4-4.5 *Measured RMS Instrumentation Jitter, MI* — For the MI measurement the observed edge is the same edge that triggered the oscilloscope.

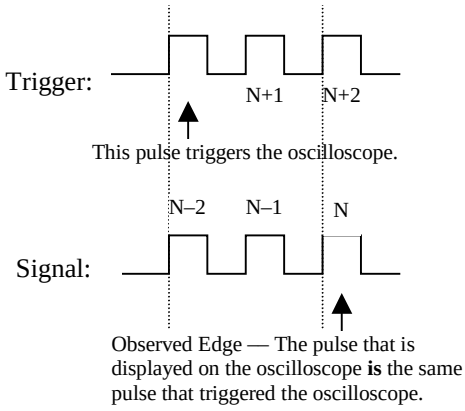


Figure A4-5
Measured RMS Instrumentation Jitter, MI

A4-4.6 There is no repetitive aspect of the signal, thus whatever jitter you observe is strictly instrumentation jitter.

A4-4.7 *Summary* — Jitter is only observable for a periodic signal or repetitive edge. Thus when MS measurements are made signal jitter is observed because a subsequent or repetitive signal is displayed (in addition to instrumentation jitter). When MI measurements are made the input signal is delayed such that you see the same edge that trigger the oscilloscope. That creates a non-repetitive or non-periodic occurrence of the observed signal, thus the jitter observed is strictly due to the instrumentation.

SEMI G81-0703
SPECIFICATION FOR MAP DATA ITEMS

This specification was technically approved by the Global Automated Test Equipment Committee and is the direct responsibility of the North American Automated Test Equipment Committee. Current edition approved by the North American Regional Standards Committee on March 12, 2003. Initially available at www.semi.org May 2003; to be published July 2003. Originally published October 2000; previously published March 2003.

1 Purpose

1.1 This document describes the data items that relate to electronic substrate mapping.

2 Scope

2.1 This document applies only to substrate map data items.

2.2 This document does not address the transmission, file naming conventions, storage or archiving of substrate maps.

2.3 The specification of which data items are optional and which are required is not specified in this document.

2.4 The size of each data item described in this document is maximum size. The actual size may be further restricted by an application document.

2.5 The order of the data items is not restricted in this document. The order of the data items may be restricted by an application document.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 There are no known limitations within the defined scope.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E5 — SEMI Equipment Communications Standard 2 Message Content (SECS-II)

SEMI T9 — Specification for Marking of Metal Lead-Frame Strips with a Two-Dimensional Data Matrix Code Symbol

4.2 *IEEE Standards*[1]

IEEE 754-1985 — IEEE Standard for Binary Floating–Point Arithmetic

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Definitions*

5.1.1 *bottom side* — the bottom side of the substrate as defined in the corresponding Appendix (Appendix 1, 2, or 3).

5.1.2 *device* — the unit to which the device status code in the map is assigned including, but not limited to: die, multi-chip modules and packages.

5.1.3 *map* — a two-dimensional array of bin codes derived from electrical test data of a substrate including, but not limited to: wafer, tray, strip, or tape.

5.1.4 *substrate* — any carrier of a two-dimensional array of devices including, but not limited to: wafers, trays, strips, tape, panels, or boards.

5.1.5 *top side* — the top side of the substrate as defined in the corresponding Appendix for that substrate (Appendix 1, 2, or 3).

6 Requirements

6.1 This document does not define format of each data item specified in the following chapter. In order to implement this specification, it requires standardized and/or specific format definition documents. Standardized format definition documents are those generic, application specific or equipment specific specification, supplied by SEMI. They may be format specification, static file specification or communication specification, e.g. SEMI E5. Specific format definition documents may de defined by supplier and user.

1 Institute of Electrical and Electronics Engineers, IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331, USA. Telephone: 732.981.0060; Fax: 732.981.1721. Website www.ieee.org.

6.2 Also this document does not define communication protocol at all. If an implementation requires transfer data items defined in the following chapter, it is necessary to prepare a custom communication protocol document or to comply with the appropriate SEMI communication standards.

6.3 This document places no special requirements on the transmission, file naming conventions, storage, or archiving of substrate maps.

7 Description

7.1 The substrate map data item specifications defined in this document are shown in Table 2. The columns in this table are described in the following sections.

7.1.1 *Item Name Column* — the name by which the data item is referenced.

7.1.2 *Data Type Column* — the type of the data as defined in Table 1.

Table 1 Data Types and Sizes

Type	*Size*	*Definition*
String	0–32767	A string of ASCII characters from zero to "Size" characters in length.
Integer	1,2,4	An integer value that may be represented by "Size" bytes. E.g., if Size = 2 then the value may be –32768 to 32767.
Float	4	IEEE single-precision 32-bit floating point type [IEEE 754-1985]

7.1.2.1 Generic data type definitions are used so that the data item definitions may be shared by several other standards, which may have their own distinct data type representations.

7.1.3 *Size Column* — the maximum number of characters that may be used to represent the data.

7.1.4 *Description Column* — describes what the data item is and what value restrictions it has.

7.2 *Coordinate System Conventions*

7.2.1 Whenever reference is made to rows, columns, X or Y they are defined as follows.

7.2.2 The X axis is the horizontal axis from left to right when the substrate is rotated according to [Orientation] in Table 2. Columns increase along the X axis. Column zero is the column just before the left (or right, depending on OriginLocation) column containing measured devices.

7.2.3 The Y axis is the vertical axis from bottom to top when the substrate is rotated according to [Orientation] in Table 2. Rows increase along the Y axis. Row zero is the row just before the extreme top (or bottom depending on OriginLocation) row containing measured devices.

7.2.4 Columns increase along the X-axis. Rows increase along the Y-axis.

Table 2 Substrate Map Data Items

Item Name	*Data Type*	*Size*	*Description*
FormatRevision	String	256	Specifies the exact name and revision of the format used to represent substrate map data. This field can be used by a parser to automatically determine the format of the remaining substrate map data.
ProductId	String	256	Product identifier
LotId	String	32	Production lot identifier for this data.
Orientation	Integer	2	The orientation of the substrate in relation to the map data. This variable will increase in the right (clockwise) direction from 0° . This item may be used to specify that the map data be rotated. Since the map data is rectangular, only the values 0, 90, 180, and 270 are allowed in that case.
WaferSize	Integer	2	Diameter of Wafer in millimeters.
DeviceSizeX	Float	4	Device size on X axis in microns
DeviceSizeY	Float	4	Device size on Y axis in microns

Item Name	*Data Type*	*Size*	*Description*
StepSizeX	Float	4	The distance in microns from a reference point on one device to the same reference point on the adjacent device in the X direction. StepSizeX – DeviceSizeX is equal to the “street” width between device in the X direction.
StepSizeY	Float	4	The distance in microns from a reference point on one device to the same reference point on the adjacent device in the Y direction. StepSizeY – DeviceSizeY is equal to the “street” width between device in the Y direction.
FrameId	String	32	A character code that may be printed or encoded on the substrate, which uniquely identifies the substrate, and can be used to correlate the map with physical substrate.
Rows	Integer	2	The number of rows of (measured) device matrix on substrate, that is the number of devices on the Y-axis of the map data. It is required if the type of the map data is simple array structure.
Columns	Integer	2	The number of columns of (measured) device matrix on substrate, that is the number of devices on the X-axis of the map data. It is required if the type of the map data is simple array structure.
MapType	String	16	Possible variations of data structure, one of which is to be chosen for passing map data. This document allows formats of the three types shown below. [MapType] = ‘Row’: Row/Column Format Expression using the coordinate showing the head of a row as well as the number of devices in the row and the bin data of the relevant row. Each bin data is attached in succession to each row. Example: X, Y, N, BIN, BIN, BIN, ..., BIN (N: Number of devices) [MapType] = ‘Array’: Array Format All of a substrate’s bin data is expressed in a one-dimensional array form. Left to right and top down substrate map data will be set in a one-dimensional array. Example: BIN, BIN, BIN, ... [MapType] = ‘Device’: Coordinate Format Expressed by XY coordinates of each device on a substrate as well as bin data. Even when using this format, to prevent omission of data, it is best to set bin data for all devices tested in front end processing. Example: X, Y, BIN, ..., X, Y, BIN The MAP coordinates set here are values for the state with the substrate orientation flat rotated to the angle given by [Orientation]. Appendix 1 contains diagrams that illustrate each [MapType]. NOTE: MAP coordinates can also be negative values.
HeadingDeviceX	Integer	2	X coordinate of the heading device of a row in the map data. This item is used when [MapType] = ‘Row’.
HeadingDeviceY	Integer	2	Y coordinate of the heading device of a row in the map data. This item is used when [MapType] = ‘Row’.
DeviceRow	Integer	2	Number of the devices on a row in the map data. This item is used when [MapType] = ‘Row’.
DeviceX	Integer	2	X coordinate of the device in the map data. This item is used when [MapType] = ‘Device’.
DeviceY	Integer	2	Y coordinate of the device in the map data. This item is used when [MapType] = ‘Device’.

Item Name	*Data Type*	*Size*	*Description*
BinType	String	16	The format in which the bin code for each device will be represented in the [Map]. The choices are as follows: [BinType] = 'Ascii': Single ASCII character (1 byte per device) [BinType] = 'Decimal': 3 digit integer from 000 to 255 (1 byte per device) [BinType] = 'HexaDecimal': 2 digit Hexadecimal value from 00 to FF (1 byte per device) [BinType] = 'Integer2': 4 digit Hexadecimal value from 0000 to FFFF (2 bytes per device) NOTE 1: For readability when [BinType] = 'Decimal' there must be spaces added between each device and each row of devices should be on a new line. NOTE 2: When [BinType] = 'Ascii' or 'Hexadecimal' or 'Integer2' there must not be spaces between each device and for readability, each row should be on a new line.
ReferenceDeviceX	Integer	2	X coordinate of the reference device to align device matrix on physical substrate with the map data.
ReferenceDeviceY	Integer	2	Y coordinate of the reference device to align device matrix on physical substrate with the map data.
RefDevicePosX	Float	4	Offset in µ m of the center of a reference devicein the X-direction from the center of substrate.
RefDevicePosY	Float	4	Offset in µ m of the center of a reference devicein the Y-direction from the center of substrate.
MapName	String	32	A name that describes the purpose of the bin codes in the map. Possible examples include: "CellStatus", "DefectCode", "MarkGrade", "PackageGrade", "SortGrade".
MapVersion	String	32	The version is used to distinguish between multiple versions of maps for the same substrate with the same MapName.
BinCode	Integer	1	A bin category from 0 to 255, other that the value assigned to [NullBin], that may be assigned to a device. It should be represented according to [BinType]. NOTE: BinCode and NullBin may take on values from 0 to 255 is represented as Ascii, Decimal, Hexadecimal, or Binary, according to BinType. See definition of BinType for more information.
BinCount	Integer	4	The number of devices on the substrate with the specified [BinCode].
BinQuality	String	16	Describes the quality of the specified [BinCode]. The following values are reserved for the data item: "Pass" – Indicates a quality that has commercial value "Fail" – Indicates a quality that does not have commercial value Other values defined by an application.
BinDescription	String	256	A description of the specified [BinCode], e.g. "100MHz".
NullBin	Integer	1	Code to indicate no device or not measured device in [Data]. It should be represented according to [BinType].
SupplierName	String	256	Name of the supplier of the substrate.
OriginLocation	Integer	1	Coordinate system on substrate to address devices. Location of the datum point or the origin of the coordinates shall be one of the following: 0 = Center device* – top side 1 = Upper right – top side 2 = Upper left – top side 3 = Lower left – top side** 4 = Lower right – top side 5 = Center device* – bottom side 6 = Upper right – bottom side 7 = Upper left – bottom side 8 = Lower left – bottom side 9 = Lower right – bottom side * Center device is X = (row count + 1), Y = (column count + 1)/2. ** Default value is 3 (= Lower left – top side) if this item is not present.

Item Name	*Data Type*	*Size*	*Description*
CreateDate	String	16	Date and time when the map data is acquired: formatted as YYYYMMDDhhmmsscc (year-month-date-hour-minute-second-centisecond).
Status	String	16	Status of map data supplying process or preceding process.
Label	String	256	Name of a special parameter.
SupplierValue	String	256	Value of a special parameter.
SlotNumber	Integer	2	This identifies the slot in the carrier in which the substrate is placed.
SubstrateNumber	Integer	2	Identifies the substrate within a lot.
GoodDevices	Integer	4	The total number of “good” devices on the substrate. The definition of “good” is beyond the scope of this document.
SubstrateType	String	16	The type of substrate. The choices are as follows: [SubstrateType] = ‘Wafer’ [SubstrateType] = ‘Strip’ [SubstrateType] = ‘Tray’
SubstrateId	String	32	A character code that may be printed or encoded on the substrate, which uniquely identifies the substrate, and can be used to correlate the map with the physical substrate.
CarrierType	String	16	The type of substrate carrier. The choices are as follows: [CarrierType] = ‘Cassette’ [CarrierType] = ‘Magazine’
CarrierId	String	32	A character code that may be printed or encoded on the substrate carrier, which uniquely identifies the substrate carrier.
LastModified	String	16	Date and time when the map data was last modified: formatted as YYYYMMDDhhmmsscc (year-month-date-hour-minute-second-centisecond)

NOTE 1: A set of above items is prepared for each single substrate to make it possible to consolidate more than one lot in a cassette.

7.3 *Example*

```
<?xml version="1.0"?>
<Map xmlns=”http://www.semi.org” SubstrateType=”Wafer”
SubstrateId="ZSDGS88DF" FormatRevision="SEMI G85-0703">
  <Device
    ProductId="854CS1C"
    LotId="wksfd87dcj37"
    Orientation="0"
    DeviceSizeX="343.8"
    DeviceSizeY="373.1"
    Rows="6"
    Columns="6"
    BinType="HexaDecimal"
    FrameId="KJKSDFK45"
    NullBin="FF"
    SupplierName="Company X"
    OriginLocation="1"
    CreateDate="2002110112000000"
    LastModified="2003010612000000"
    Status="Product">
    <ReferenceDevice
      ReferenceDeviceX="2"
      ReferenceDeviceY="-3"
      RefDevicePosX="2"
      RefDevicePosY="2"
    />
    <ReferenceDevice
```

```
      ReferenceDeviceX="4"
      ReferenceDeviceY="-5"
      RefDevicePosX="2"
      RefDevicePosY="2"
    />
    <Bin
      BinCode="02"
      BinQuality="Pass"
      BinDescription="500MHz"
    />
    <Data MapName="SortGrade" Version="1">
      <Row><![CDATA[FFFF020CFFFF]]></Row>
      <Row><![CDATA[FF14020C02FF]]></Row>
      <Row><![CDATA[0202020C0116]]></Row>
      <Row><![CDATA[0201140C0202]]></Row>
      <Row><![CDATA[FF14020C02FF]]></Row>
      <Row><![CDATA[FFFF020CFFFF]]></Row>
    </Data>
  </Device>
</Map>
```

APPENDIX 1
WAFER MAP

NOTICE: The material in this appendix is an official part of SEMI G81 and was approved by full letter ballot procedures on August 27, 2001.

A1-1 This appendix shows how the map data items may be applied to wafers as well as some additional information specific to this substrate type. See Figures A1-1 through A1-8.

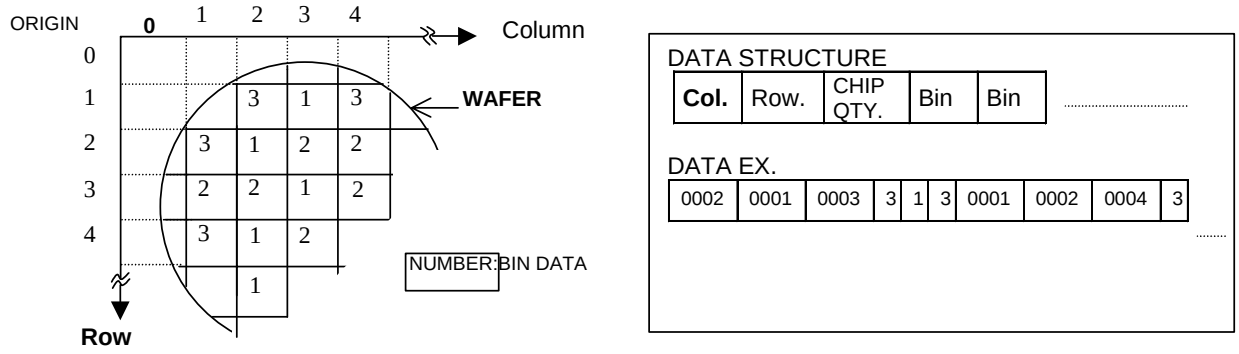


Figure A1-1a
Row/Column Format (MapType = "Row")

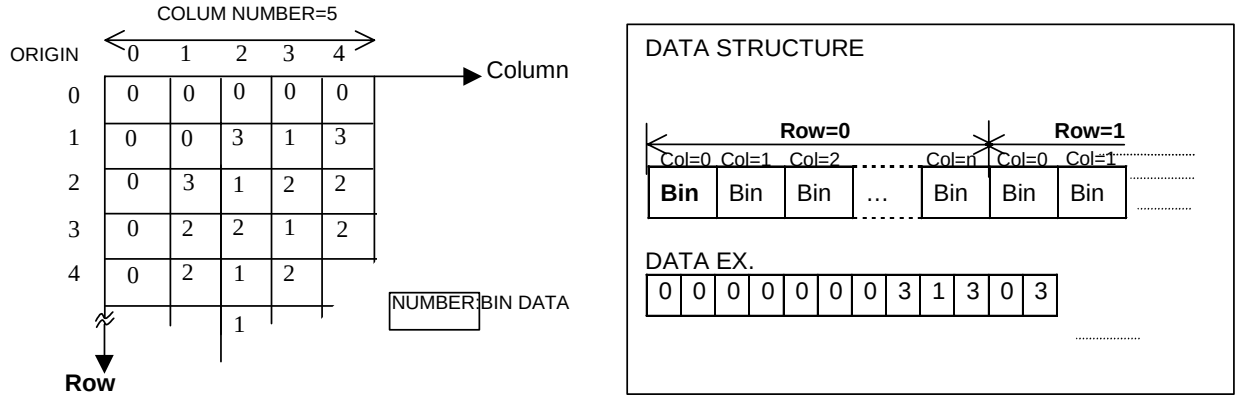


Figure A1-1b
Array Format (MapType = "Array")

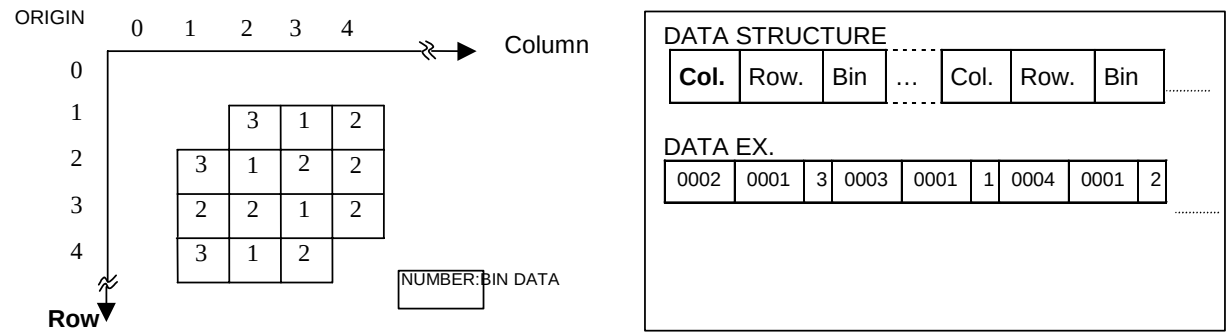


Figure A1-1c
Coordinate Format (MapType = "Device")

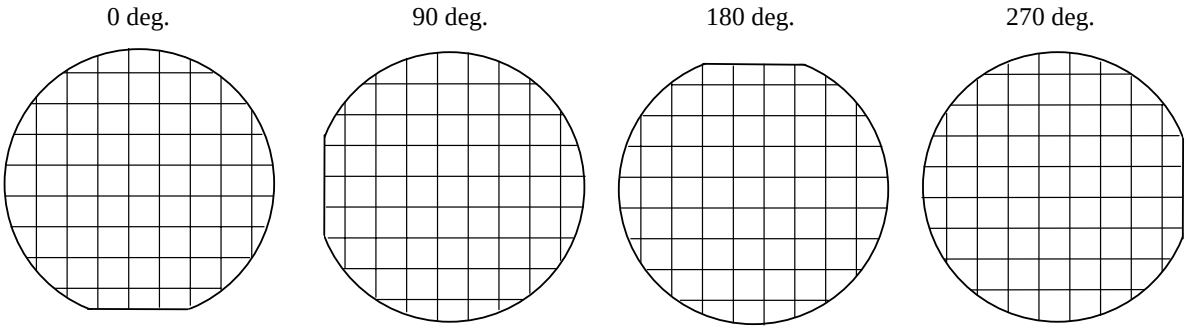


Figure A1-2
Orientation of the Wafer Flat or Notch (Orientation)

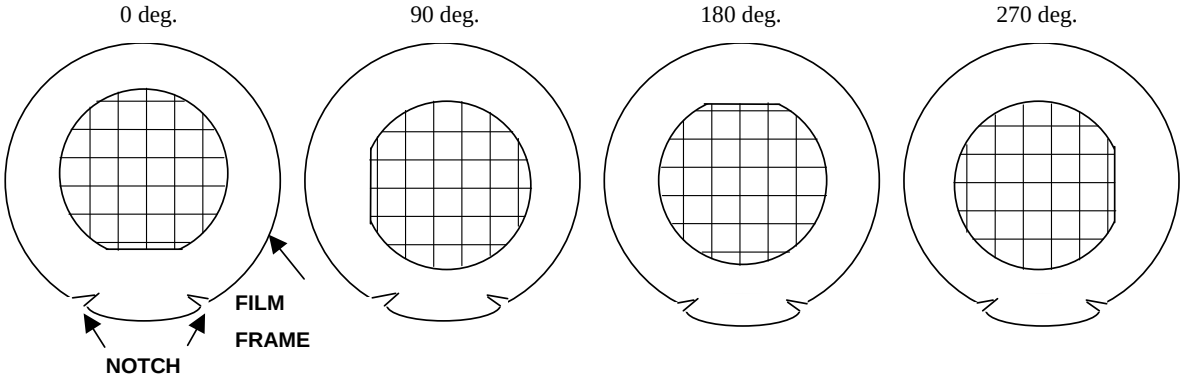


Figure A1-3
Orientation of the Wafer Flat or Notch on the Film Frame

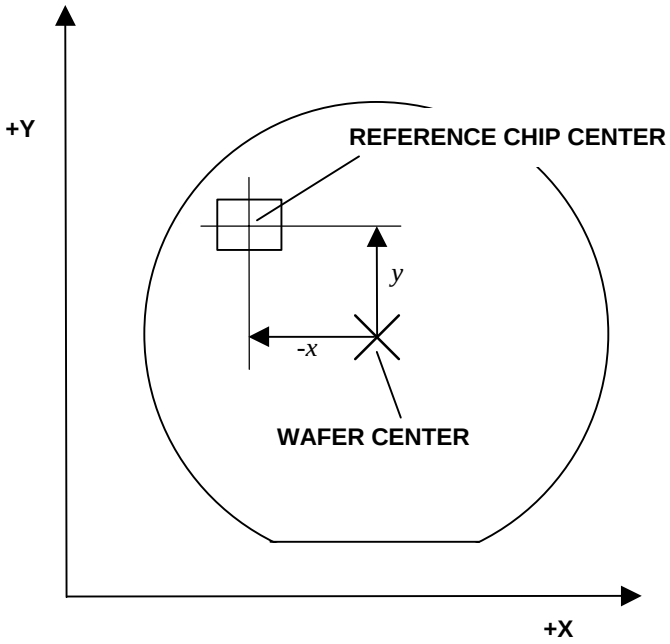


Figure A1-4
Reference Device Position (RefDevicePosX and RefDevicePosY)

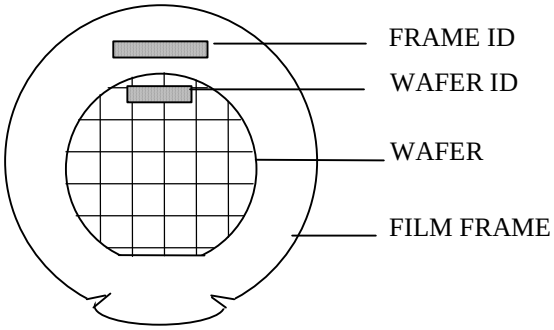


Figure A1-5
Example of WaferID and FrameID Position

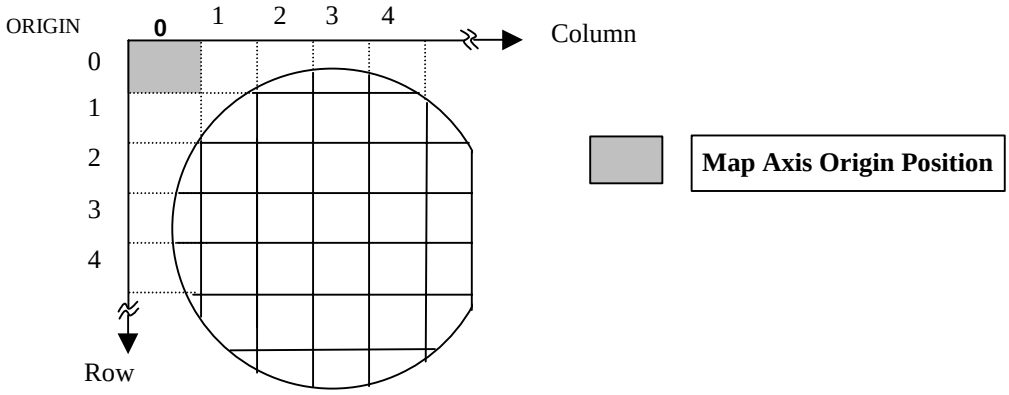


Figure A1-6
(Ex.) Map Coordinates System (OriginLocation = Top Left Top Side)

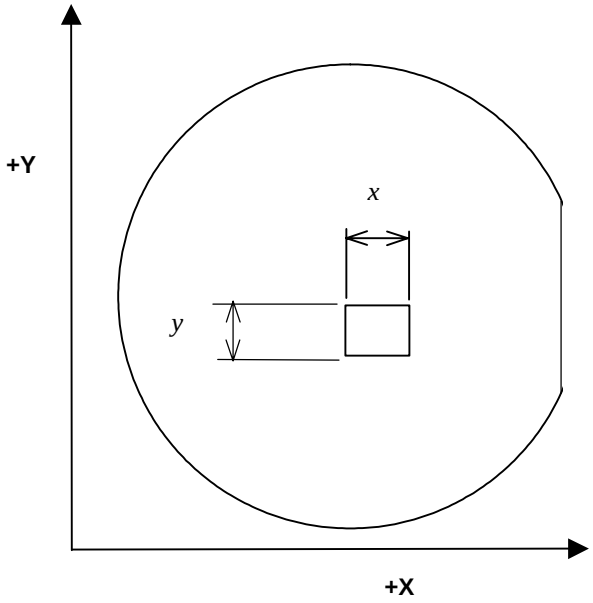
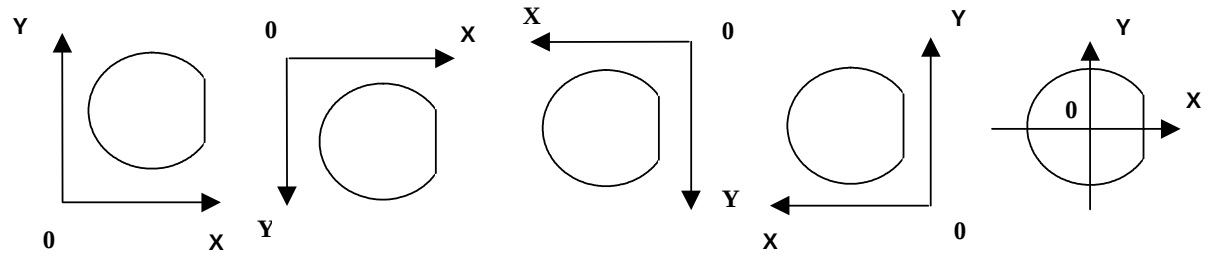


Figure A1-7
Chip Size Coordinates



Type: 'BottomLeft' **Type: 'TopLeft'** **Type: 'TopRight'** **Type: 'BottomRight'** **Type: 'Center'**

Figure A1-8
Wafer Coordinate to Address Devices (OriginLocation)

APPENDIX 2
STRIP MAP

NOTICE: The material in this appendix is an official part of SEMI G81 and was approved by full letter ballot procedures on August 27, 2001.

A2-1 This appendix shows how the map data items may be applied to strips as well as some additional information specific to this substrate type.

A2-2 The StripID shall follow the SEMI T9 specification, when applicable, or may be user definable by the factory.

A2-3 For any given process there must be a way to ensure correct orientation of the strip. The end user is responsible for providing a master manufacturing drawing showing the top side of the strip. This drawing must show any special markings or patterns that are needed to reliably flip and rotate a physical strip until it is oriented the same as the drawing. Figure A2-1 defines what is meant by top side and hence bottom side. It also defines what is meant by upper, lower and left and right.

A2-4 Each strip type will have a factory defined value for OriginLocation. This is the origin reference for the row 1, column 1 location on the strip. The factory origin, OriginLocation is selected as one of four corners by the factory host system. The row and column index will be referenced from the selected reference. This information will be provided to the equipment by the host in each strip map download scenario.

1 = Upper right (UR) top side

2 = Upper left (UL) top side

3 = Lower left (LL) top side

4 = Lower right (LR) top side

6 = Upper right (UR) bottom side

7 = Upper left (UL) bottom side

8 = Lower left (LL) bottom side

9 = Lower right (LR) bottom side

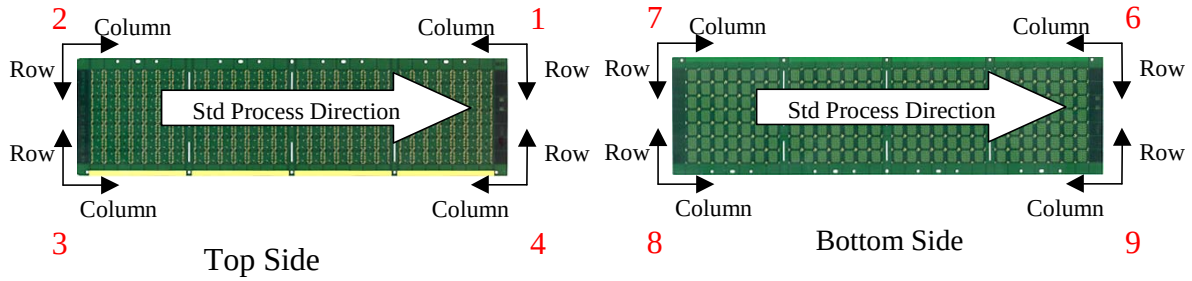


Figure A2-1
Factory Origin Settings

APPENDIX 3
TRAY MAP ORIENTATION

NOTICE: The material in this appendix is an official part of SEMI G81 and was approved by full letter ballot procedures on August 27, 2001.

A3-1 This appendix shows how the map data items may be applied to JEDEC trays as well as some additional information specific to this substrate type.

A3-2 The X-axis (Column) is assigned to the long axis of the JEDEC tray; the Y-axis (Row) is assigned to the short axis of the tray. This corresponds to Cartesian coordinate "1" (in this way all coordinate positions can be expressed in positive integer values). For the origin of the tray, the pocket nearest the bevel (at the bottom left corner of the tray in Figure A3-1 below) is defined as coordinate location 0,0. (Row/Column).

A3-3 The following values for OriginLocation apply to the JEDEC tray:

1 = Upper right (UR) top side

2 = Upper left (UL) top side

3 = Lower left (LL) top side

4 = Lower right (LR) top side

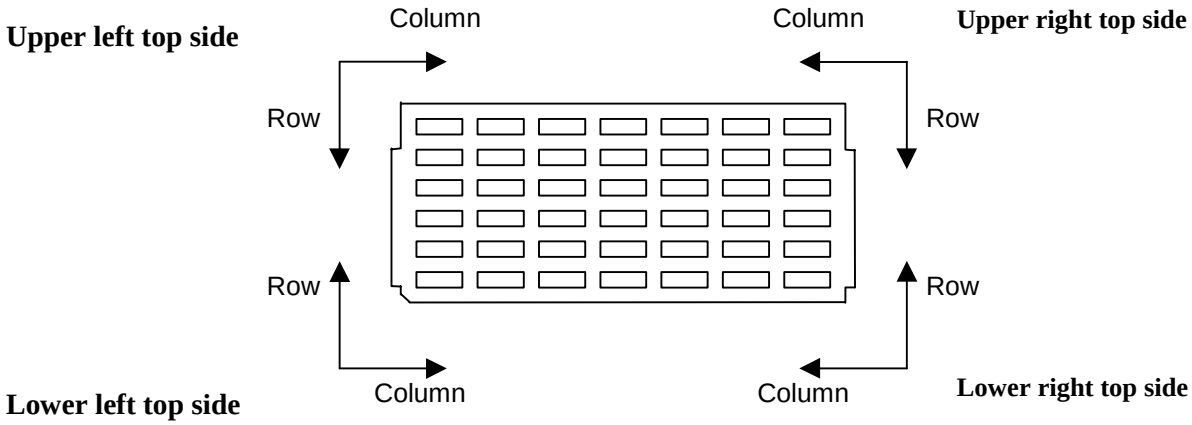


Figure A3-1
OriginLocation

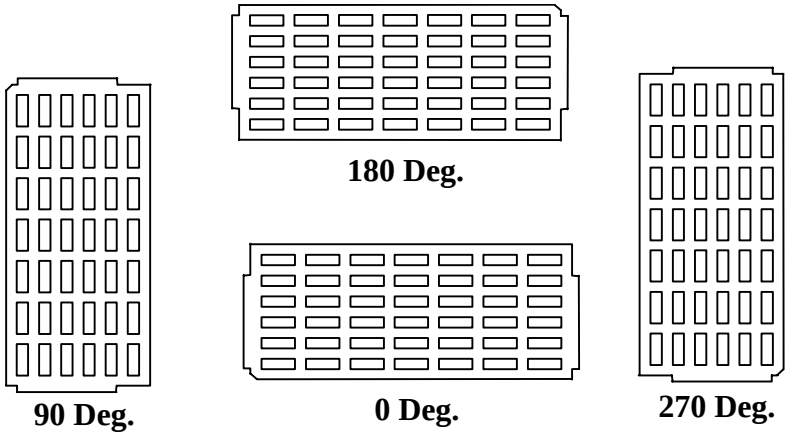


Figure A3-2
Tray Orientation

NOTICE: SEMI makes no warranties or representations as to the suitability of the standard set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copyrighted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI G82-0301[E]
PROVISIONAL SPECIFICATION FOR 300 mm LOAD PORT FOR FRAME CASSETTES IN BACKEND PROCESS

This specification was technically approved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on December 1, 2000. Initially available at www.semi.org December 2001, to be published March 2002.

[E] This document was editorially modified in November 2001 to correct a cosmetic error. Changes were made to Figure 2.

1 Purpose

1.1 This specification defines dimensional requirements for the load port of frame cassette for 300 mm wafer in backend process equipment. It is intended to promote a uniform physical interface between equipment and the factory, to facilitate the use of automated frame cassette transport systems, and/or to meet ergonomic requirements for manually loaded equipment.

2 Scope

2.1 This is a provisional standard covering equipment for 300 mm frame cassette only. The provisional status is dictated by the immaturity of designs for 300 mm equipment and additional specifications which are not defined yet.

2.2 These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Limitations

3.1 This standard is not intended for use in backend except frame cassette for 300 mm wafers. This standard does not address direct loading/unloading of vacuum load locks. Requirements of such interfaces may differ from those in this document.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E15 — Specification for Tool Load Port

SEMI E15.1 — Specification for 300 mm Load Port

SEMI E57 — Mechanical Specification for kinematic Couplings Used to Align and Support 300 mm Wafer Carriers

SEMI E64 — Specification for 300 mm Cart to SEMI E15.1 Docking Interface Port

SEMI G77 — Specification for Frame Cassette for 300 mm Wafers

5 Terminology

5.1 Please see SEMI G77 for definitions of the following terms used in this specification:

5.1.1 *bilateral datum plane*

5.1.2 *conveyor rails*

5.1.3 *facial datum plane*

5.1.4 *frame cassette*

5.1.5 *horizontal datum plane*

5.1.6 *tape frame*

5.2 Please see SEMI E15 for definitions of the following terms used in this specification:

5.2.1 *load depth*

5.2.2 *load face plane*

5.2.3 *load height*

5.2.4 *load port*

5.2.5 *spacing*

5.2.6 *tool*

5.3 *frame cassette centroid* — a datum representing the theoretical location of the center of a stack of tape frames in the frame cassette.

6 Ordering Information

6.1 The following items require communication between the tool supplier and user and shall be included in any request for quotation or purchase order:

6.1.1 If the tool has multiple load ports, provide the spacing, S, between frame cassette centroids (see SEMI E15).

6.1.2 Specify what frame cassette (e.g. optional composition, see SEMI G77) is to be accommodated by the load port (see SEMI E15).

7 Requirements

7.1 The dimensional requirements for the load port are given in Table 1 with reference to the figures of this document. Although the frame cassette transport systems shown in these figures appear similar to overhead monorails, they are intended to represent any type of transport system (AGV, PGV, conveyor, overhead track, etc.).

7.2 The dimensional requirements for the placement of the frame cassette on the load port are given in Table 1 with reference to the figures of this document.

7.3 The tape frames are to be oriented horizontally at the time they are placed on the load port.

7.3.1 The frame cassette shall be loaded and unloaded with its front parallel to and away from the load face plane (see Figure 1).

7.4 Dimension H is nominally 900 mm, fully adjustable at installation over the range of 890 to 910 mm. The precision with which the load port height must be maintained is dictated by the needs of the frame cassette delivery system.

7.5 The load port must nominally be at 900 mm, and it must be open from above to facilitate automatic frame cassette delivery from an overhead transport system. The open volume required for vertical delivery is defined by a projection of the load port area, including the area required for C1 and C2 clearances, projected upward to the top of the tool. Note that this condition need only be met when the tool is being loaded. For example, the load port may be formed by a surface that extends outward during loading to provide overhead access.

7.6 As shown in Figure 2, the maximum allowable height of an obstruction on the load port over which the frame cassette must be lifted (before being set down on the kinematic couplings) is H1. Examples of such obstructions include alignment devices and identification tag readers as well as the kinematic couplings themselves. Below H1 above the horizontal datum plane, clearances C1 and C2 no longer apply.

7.6.1 Two exclusion volumes on the left and right side of the load port must also be kept clear so that fork lifts or conveyors may be used. Each exclusion volume extends from the load face plane to D0 beyond the facial datum plane and extends H0 below the horizontal datum plane between W1 and W2 from the bilateral datum plane.

7.6.2 The load port that advances the frame cassette from the undocked position (where the frame cassette is initially delivered to the load port) to the docked position (where the frame cassette is ready for frame extraction or insertion) must reserve an exclusion volume that is intended for (but not limited to) containing automated units that read or write to an ID tag on the rear of the frame cassette in the undocked position (where the frame cassette is initially delivered to the load port). If no reader/writer unit is installed, the exclusion volume may be covered by a panel.

NOTE 1: This section is incomplete and requirements will be added to the standard once the requirements and dimensions have been fully defined.

7.7 Clearances C1 and C2 are defined with respect to the maximum dimensions of the frame cassette (see SEMI G77). To prevent interference with overhead transport systems on the same or adjacent load port, it is recommended that floor-based transport vehicles do not exceed clearances C1 and C2 when picking up or placing the frame cassette on the load port.

7.8 Dimension S specifies the recommended minimum spacing between frame cassette centroids. In any case, if S violates C1, then C1 takes precedence.

7.9 To add clearance for overhead frame cassette transport, no part of the tool in front of the plane defined by C2 may be higher than H2 from the floor. The volume below H2 may contain the frame cassette stored in an internal buffer by the tool.

7.10 The load port must provide the option to use the conveyor rails for frame cassette loading. At the time of frame cassette transfer, the conveyor rails must be positioned at HC3 as shown in Figure 2. When not in use, the conveyor rails must be lowered below the fork lift exclusion zone.

8 Related Documents

SEMI E1.9 — Provisional Mechanical Specification for Cassettes Used to Transport and Store 300 mm Wafers

SEMI E47.1 — Provisional Mechanical Specification for Boxes and Pods Used to Transport and Store 300 mm Wafers

SEMI E72 — Specification and Guide for 300 mm Equipment Footprint, Height, and Weight

SEMI G74 — Specification for Tape Frame for 300 mm Wafers

Table 1 Dimensional Requirements for 300 mm Load Port

Dimension	*Application*	*Value, mm (in.)*	*Notes*
C1	minimum	75 (3.0)	
C2	minimum	30 (1.2)	
D	range	$250\ ^{+0}_{-10}$ ($9.8\ ^{+0}_{-0.4}$)	
D0	minimum	110 (4.33)	
H	nominal	900 (35.4)	1
H0	minimum	15 (0.59)	
H1	maximum	25 (1.0)	
H2	maximum	2600 (102.4)	
HC3	range	$32\ ^{+2.0}_{-0}$ ($1.26\ ^{+0.1}_{-0}$)	2
S	minimum	482 (19.0)	3
		555 (21.9)	4
W1	maximum	130 (5.12)	
W2	minimum	205 (8.07)	

NOTE 1: This value is ergonomically compatible with the proposed 13 frame cassette and may not be ergonomically compatible with the proposed 25 frame cassette. The proposed 25 frame cassette may require assisted loading. H to be fully adjustable at installation over the range of 890 to 910 mm (35 to 35.8 inches).

NOTE 2: To avoid confusion, HC3 is used instead of H3 because H3 stands for another dimension in SEMI E15.1.

NOTE 3: Frame cassette (see SEMI G77) without manual side handles

NOTE 4: Frame cassette (see SEMI G77) with manual side handles

9 Table 1 Dimensions Definition

9.1 See SEMI E15 for definitions of the following terms used in this specification:

9.1.1 C1

9.1.2 C2

9.1.3 H

9.1.4 H1

9.1.5 S

9.2 *D* — allowable load depth to frame cassette centroid.

9.3 *D0* — minimum rear clearance of equipment boundary below H1 from facial datum plane.

9.4 *H0* — minimum height from the bottom of equipment boundary below H1 to horizontal datum plane.

9.5 *H2* — maximum overhead track clearance from the floor.

9.6 *HC3* — allowable height of conveyor rail from horizontal datum plane.

9.7 *W1* — maximum side clearance of equipment boundary below H1 from bilateral datum plane.

9.8 *W2* — minimum side clearance of equipment boundary below H1 from bilateral datum plane.

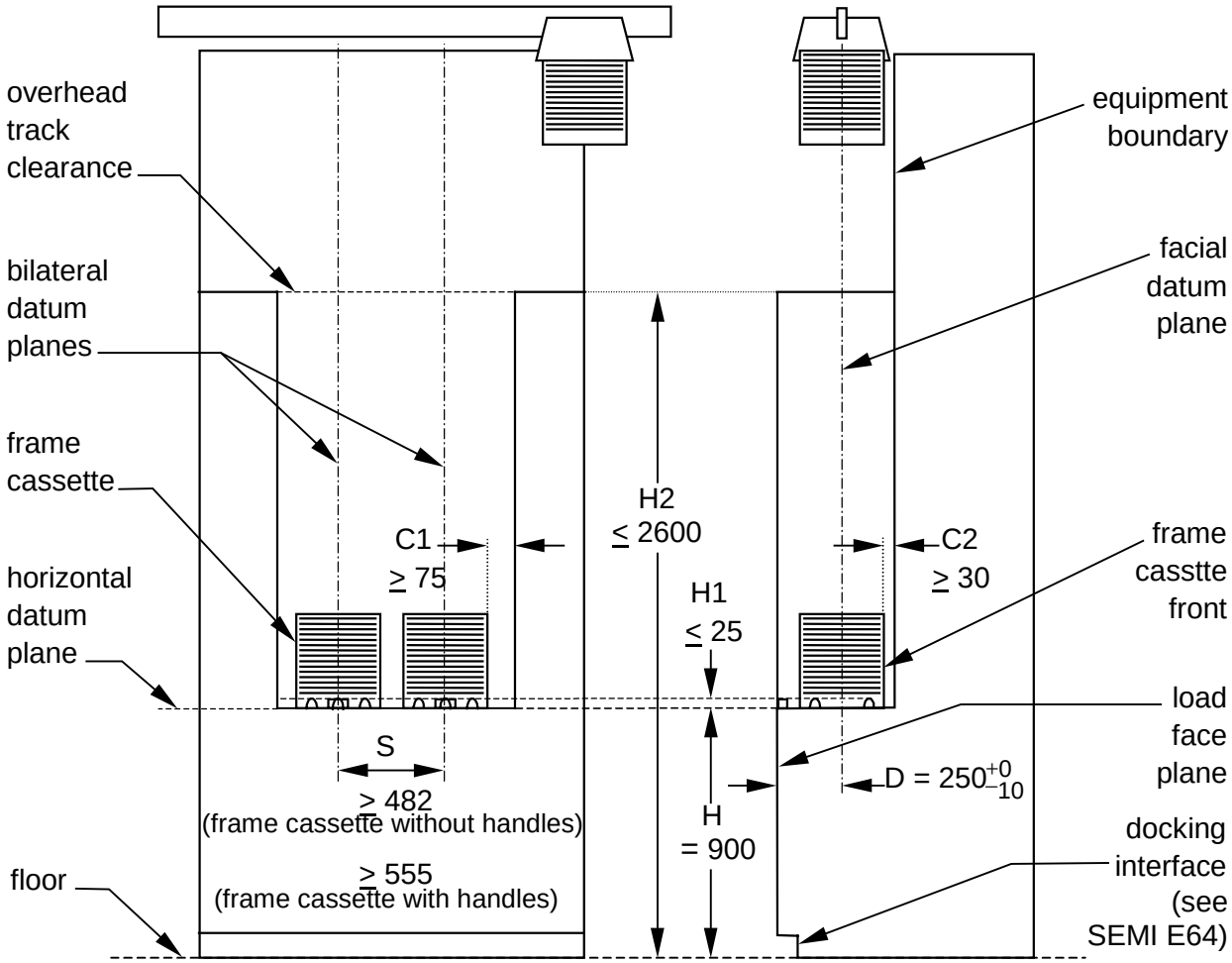


Figure 1
Load Port Requirements

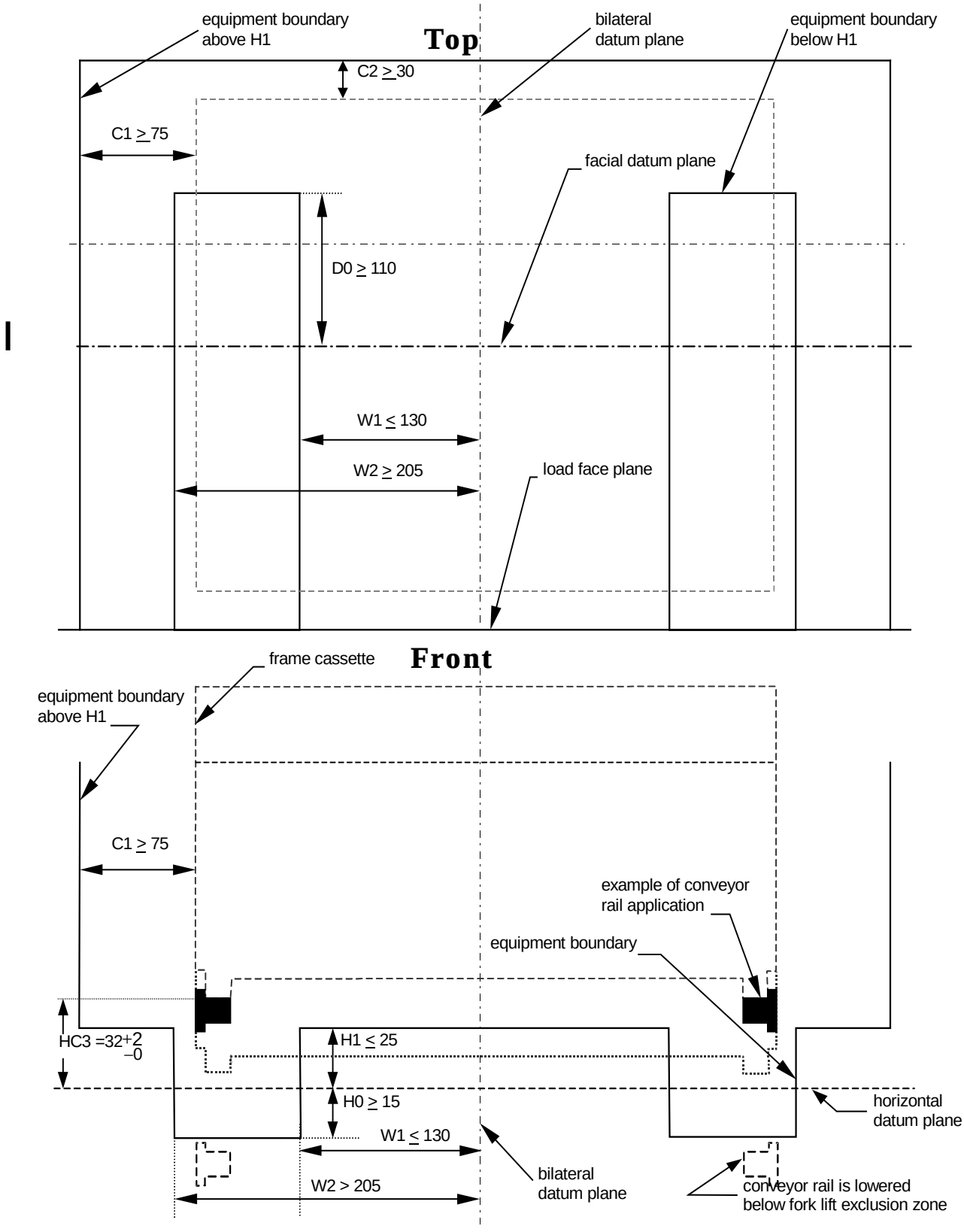


Figure 2
Trenches and Conveyor Rails

NOTICE: SEMI makes no warranties or representations as to the suitability of the standard set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials or equipment mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copy-righted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI G83-0301
SPECIFICATION FOR BAR CODE MARKING OF PRODUCT PACKAGES

This specification was technically approved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on December 1, 2000. Initially available at www.semi.org January 2001; to be published March 2001.

1 Purpose

1.1 This specification describes the area needed for adding bar codes, the bar code specifications, and the code notation format for direct and indirect material product packages (unit packs) for semiconductor packaging.

1.2 The following are the goals of this specification:

- Quality control using computers
- Prevention of mistakes created by human error
- Material control at the manufacturing site

1.3 The following is not a goal of this specification:

- Purchasing control

2 Scope

2.1 This specification is to be used for direct and indirect materials relating to packaging materials.

2.2 This specification is to be used for product packages only.

2.3 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate and safety health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI G71 — Specification for Barcode Marking of Intermediate Containers for Packaging Materials

3.2 *AIM Specifications*[1]

USS-39 — Universal Symbol Specification code 39

USS-128 — Universal Symbol Specification code 128

3.3 *ANSI Specifications*[2]

ANSI X3.182 — Bar code Print Quality - Guideline

NOTE 1: As listed or revised, all documents cited shall be the latest publications of adopted standards.

4 Terminology

4.1 Many of the items relating to bar code technology are defined in the AIM Glossary of Terms, ANSI X3.182 (Bar code Print Quality Guidelines).

4.1.1 *data field* — field (area) for adding a bar code to a product package.

4.1.2 *direct material* — components and parts that make up a semiconductor package. Examples include lead frames, molding compounds, bonding wires, die bonding materials, etc.

4.1.3 *HRI (Human Readable Identification)* — characters that can be read by a human.

4.1.4 *indirect material* — supplementary materials and parts used during processing but that do not make up a semiconductor package. Examples include bonding capillaries, dicing blades, etc.

4.1.5 *intermediate container* — container that holds one or more product packages for product/order separation in a shipping container or final container.

4.1.6 *product package* — the smallest package format, made by a single material. Also called a unit pack.

4.1.7 *shipping pack* — package or shipping container/final container (see Figure 1) that is strong enough for industrial use for product packaging, storage, and shipping.

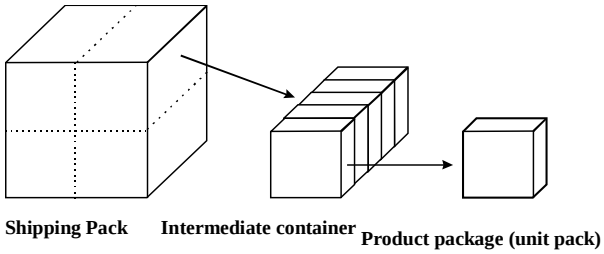


Figure 1
Package Form Regulations

1 AIM International Inc., 11860 Sunrise Valley Drive, Suite 100, Reston, VA 20191, tel 703.391.7621, fax 703.391.7624

2 American National Standards Institute, 11 West 42nd Street, New York, NY 10036, tel 212.642.4900, fax 212.398.0023

5 Requirements

5.1 *Data Field*

5.1.1 Length is 42 mm or greater, height is 15 mm or greater (see Figure 2 and Table 2).

5.1.2 The noted content bar code is HRI.

5.2 *Bar Code*

5.2.1 *Bar code character* — Bar code characters specified by AIM USS-39 or AIM USS-128 shall be used.

5.2.2 *Printing quality* — according to ANSI X3.182 Bar code Print Quality Guidelines.

5.2.3 *Code dimensions* — the bar code dimensions will be as listed in Table 1.

5.2.4 *Restrictions on use of Code 128* — use only code set B. Also, do not use shift characters within data.

5.2.5 The data digit count will be from 15 to 26 (excluding start/stop characters and check characters).

5.2.6 Use check character.

5.3 *HRI (Human Readable Identification)*

5.3.1 Just below the bar code located in the data field, a field for HRI characters is noted.

5.3.2 The HRI height will be 3.0 mm or greater.

5.3.3 The space between the HRI and bar code shall be 1.0 mm or greater (see Figure 2 and Table 2).

5.4 *Data Contents*

5.4.1 Includes items listed in Table 3.

5.4.2 The sequence, from left to right is as follows: the product recognition number, manufacturing date, sub-lot number, and lot number.

5.4.3 Product recognition number and lot number shall be included.

5.4.4 Manufacture date and sub-lot number shall be written in fixed digits. Remaining unused digits shall be filled by minus codes "-".

Figure 2
Data Field Dimensions and Placement

Table 1 Code Dimensions

Code 39, Code 128	Dimensions
Minimum element width	0.15 mm or greater.
Code 39 wide bar width	Greater than 2 times, but less than 3 times the minimum element width.
Gap between characters	Minimum element width or greater.
Character height	8.0 mm or greater.
Quiet zone	10 times or greater than the minimum element size (before and after the bar code).

Table 2 Data Field Dimensions

Item	*Dimensions*
Data field length	A ≥ 42 mm
Data field height	B ≥ 15 mm
Bar code height	C ≥ 8 mm
HRI character height	D ≥ 3 mm
Space between bar code and HRI	E ≥ 1 mm

Table 3 Data Contents (see Appendix 1)

Field Name	*Product Recognition No.*	*Manufacturing Date*	*Sub-Lot No.*	*Lot No.*
Meaning	Code used by user mainly to characterize products.	Date the material was manufactured	Code for characterizing the product package	Code used by supplier mainly to characterize products
Number of digits	5 to 12	3	2	5 to 9
Note	No regulations.	1st digit: Last digit of Gregorian calendar year. 2nd digit: Month indication, note that A = October, B = November, C = December. 3rd digit: Day indication, note that A = the tenth, B = the eleventh, C = the twelfth, ... U = the thirtieth, V = the thirty-first.	No regulations.	No regulations.

APPENDIX 1

NOTE: The material in this appendix is an official part of SEMI G83 and was approved by full letter ballot procedures on December 1, 2000 by the Japanese Regional Standards Committee.

This information explains AIM Specifications listed in Section 3.1 and examples of Data Contents specified in Table 3.

A1-1 AIM USS-39

A1-1.1 Figure A1-1 shows the AIM USS-39 characters and bar patterns.

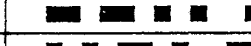
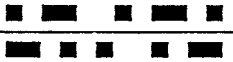
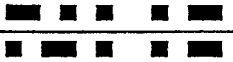
Character	Bar Pattern	Character	Bar Pattern	Character	Bar Pattern
0		F		T	
1		G		U	
2		H		V	
3		I		W	
4		J		X	
5		K		Y	
6		L		Z	
7		M		-	
8		N		.	
9		O		SPACE	
A		P		$	
B		Q		/	
C		R		+	
D		S		%	
E				*	

Figure A1-1
AIM USS-39

A1-2 AIM USS-128

A1-2.1 The AIM USS-128 characters and bar patterns are shown in Figure A1-2. Areas enclosed by bold lines indicate the code used with this specification.

Numerical value	CODE A	CODE B	CODE C	Bar pattern
0	SP	SP	00	
1	!	!	01	
2	"	"	02	
3	#	#	03	
4	$	$	04	
5	%	%	05	
6	&	&	06	
7	'	'	07	
8	(	(	08	
9	)	)	09	
10	*	*	10	
11	+	+	11	
12	,	,	12	
13	-	-	13	
14	.	.	14	
15	/	/	15	
16	0	0	16	
17	1	1	17	
18	2	2	18	
19	3	3	19	
20	4	4	20	
21	5	5	21	
22	6	6	22	
23	7	7	23	
24	8	8	24	
25	9	9	25	
26	:	:	26	
27	;	;	27	
28	<	<	28	
29	=	=	29	
30	>	>	30	
31	?	?	31	
32	@	@	32	
33	A	A	33	
34	B	B	34	
35	C	C	35	
36	D	D	36	
37	E	E	37	
38	F	F	38	
39	G	G	39	
40	H	H	40	
41	I	I	41	
42	J	J	42	
43	K	K	43	
44	L	L	44	
45	M	M	45	
46	N	N	46	
47	O	O	47	
48	P	P	48	
49	Q	Q	49	
50	R	R	50	
51	S	S	51	
52	T	T	52	
53	U	U	53	

Numerical value	CODE A	CODE B	CODE C	Bar pattern
54	V	V	54	
55	W	W	55	
56	X	X	56	
57	Y	Y	57	
58	Z	Z	58	
59	[	[	59	
60	\	\	60	
61	]	]	61	
62	^	^	62	
63	_	_	63	
64	NUL	`	64	
65	SOH	a	65	
66	STX	b	66	
67	ETX	c	67	
68	EOT	d	68	
69	ENQ	e	69	
70	ACK	f	70	
71	BEL	g	71	
72	BS	h	72	
73	HT	i	73	
74	LF	j	74	
75	VT	k	75	
76	FF	l	76	
77	CR	m	77	
78	SO	n	78	
79	SI	o	79	
80	DLE	p	80	
81	DC1	q	81	
82	DC2	r	82	
83	DC3	s	83	
84	DC4	t	84	
85	NAK	u	85	
86	SYN	v	86	
87	ETB	w	87	
88	CAN	x	88	
89	EM	y	89	
90	SUB	z	90	
91	ESC	{	91	
92	FS	|	92	
93	GS	}	93	
94	RS	~	94	
95	US	DEL	95	
96	FNC 3	FNC 3	96	
97	FNC 2	FNC 2	97	
98	SHIFT	SHIFT	98	
99	CODE C	CODE C	99	
100	CODE B	FNC 4	CODE B	
101	FNC 4	CODE A	CODE A	
102	FNC 1	FNC 1	FNC 1	
103	START(CODE A)			
104	START(CODE B)			
105	START(CODE C)			
	STOP			

Figure A1-2
AIM USS-128

A1-3 Example of Data Contents

A1-3.1 The items shown in Figures A1-3 and A1-4 are data contents of bar code that comply with this specification.

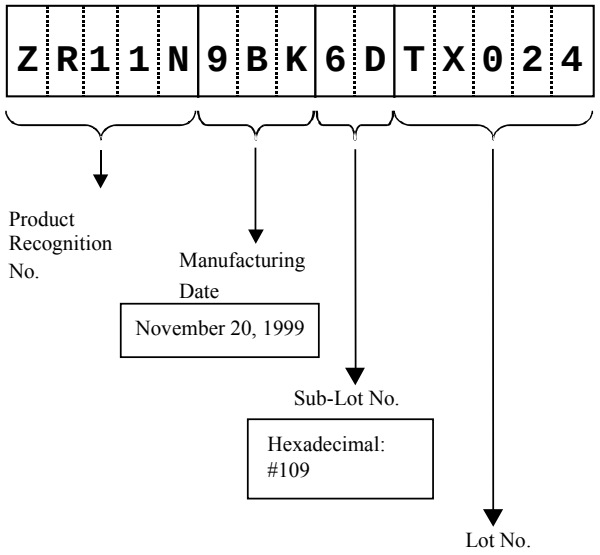


Figure A1-3
Example of Data Contents

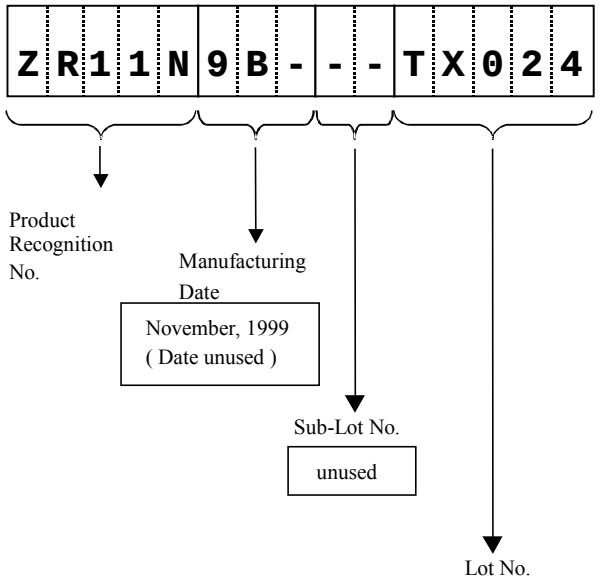


Figure A1-4
Example of Data Contents