3. Concentration dependent: to be agreed upon between user and producer
4. ≥ 3500 cm^2/V-s
5. Unspecified

B. 1. ≥ 4000 cm^2/V-s
2. ≥ 2500 cm^2/V-s
3. ≥ 1500 cm^2/V-s
4. ≥ 1000 cm^2/V-s
5. ≥ 400 cm^2/V-s
6. to be determined between user and producer

C. To be agreed upon between user and producer

NOTICE: These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copyrighted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI M20-1104
PRACTICE FOR ESTABLISHING A WAFER COORDINATE SYSTEM

This practice was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on August 16, 2004. Initially available at www.semi.org September 2004; to be published November 2004. Originally published in 1991; previously published in 2004.

1 Purpose

1.1 Processing systems now employed in advanced device manufacturing use aligning mechanisms to position the wafer rotationally and in *x*-*y* prior to processing. Many of these scan the wafer periphery and determine the geometric center of the wafer surface. This is most often seen on stepping aligners, to minimize the effects of wafer-to-wafer diameter variation in mixed aligner type fabs. Similar center-referencing subsystems are found on many characterization systems. The wafer coordinate system provides a method for referencing any other coordinate system, such as a site, pattern, or mapping array, to the physical geometry of the wafer surface.

1.2 If the points of the array lie on the front surface of the wafer, only the *x* and *y* (or *r* and θ) coordinates are relevant. It has become increasingly important in semiconductor material and device manufacturing to describe, in unambiguous terms, the position of a point on a wafer that automatic processing, test, or characterization equipment can recognize and locate. For example, characterization equipment needs to report the precise locations of defects and anomalies discovered in wafers before or after processing in order to relate the presence or absence of such defects and anomalies to device yield variations. The wafer coordinate system can be used to establish the coordinates of each point of interest, and, through transformation to the yield analysis coordinate system, relate them to the die yield map.

1.3 In response to these needs, this practice defines a wafer coordinate system to facilitate the precise locating and reporting of points on the wafer surface. If the point or points lie above or below the surface, the *z*-coordinate must also be used. Because the zero point on the *z*-axis is application specific, this practice treats the *x*-*y*-*z* (or *r*-θ-*z*) system separately from the surface coordinate system.

2 Scope

2.1 This practice covers procedures for defining a wafer coordinate system for locating uniquely any point on a wafer surface using the wafer center as the origin and either Cartesian (*x*-*y*) or polar (*r*-θ) coordinates.

2.2 For unpatterned wafers, this wafer coordinate system can be used directly or in conjunction with a rectangular or polar overlay array.

2.3 This wafer coordinate system can also be used to locate the origins or other reference points of other coordinate systems used to define or report position data of site, die, or map arrays on the front or back surface of a patterned or unpatterned wafer. In this way, the array coordinate system may be referenced to the physical geometry of the wafer. Selected modes of application of the wafer coordinate system are given for information only in Related Information 1.

2.4 This practice also covers procedures for defining a three-dimensional *x*-*y*-*z* (or *r*-θ-*z*) coordinate system for the wafer.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 Mask alignment conventions are not necessarily consistent with the wafer coordinate system.

3.2 In SEMI M1, the position of the secondary flat on silicon wafers is defined by the clockwise rotation from the primary flat. This is opposite to the convention used for the polar angle in the wafer coordinate system.

3.3 Also in SEMI M1, the coordinate system for the edge profile template is, unlike the wafer coordinate system, edge referenced. In addition, the edge profile template uses the *x* coordinate for the radial direction (positive from the wafer edge inward) and the *y* coordinate for the vertical direction (positive from the wafer surface toward the median plane of the wafer).

3.4 In SEMI E5, the “normal” position of the wafer is defined similarly to that in the wafer coordinate system; that is, the primary fiducial is downward and its bisector is the negative *y*-axis. However, the rotational position of the wafer is defined by its clockwise rotation from the “normal” position, again opposite to the convention used for the polar angle in the wafer

coordinate system. Further, in SEMI E5, the coordinate system axes do not rotate; the wafer rotates with respect to these axes. In the wafer coordinate system, the coordinate axes are referenced to the wafer itself, independent of the physical position of the wafer in space.

3.5 SEMI M12 and SEMI M13 specify the mark field location for 100 mm, 125 mm, or 150 mm diameter flatted wafers relative to the flat rather than the wafer center. Thus, the mark field location may vary with respect to the wafer center and the coordinates of the corners of the mark field location (in the wafer coordinate system) may vary from wafer to wafer. However, the mark field location for notched wafers 150, 200, and 300 mm in diameter is referenced to the wafer center.

3.6 There are some circumstances in which the front surface of an unpatterned wafer is not readily distinguished from the back surface.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E5 — SEMI Equipment Communications Standard 2 Message Content (SECS-II)

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M12 — Specifications for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M17 — Guide for a Universal Wafer Grid

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 None.

6 Summary of Practice

6.1 *Front Surface Coordinate System*

6.1.1 The wafer is positioned with its front surface up.

6.1.2 The wafer center is located.

6.1.3 A right-handed Cartesian coordinate system is erected.

6.1.4 The primary fiducial is located to be in the negative *y*-direction.

6.1.5 Cartesian or polar coordinates (referenced to the positive *x*-axis) are chosen according to the intended application.

6.2 *Back Surface Applications*

6.2.1 The wafer is rotated about the bisector of the primary fiducial (*y*-axis) until the back surface is up.

6.2.2 This reverses the direction of the *x*-axis, but otherwise the back surface coordinate system is the same as the front surface coordinate system.

6.3 *Three-dimensional Coordinate System*

6.3.1 Because the zero point on the *z*-axis is application specific, only the direction of the *z*-axis is defined and the various possibilities for locating the zero point are considered.

7 Procedure for Establishing Wafer Coordinate Systems

7.1 *Front Surface Coordinate System*

7.1.1 Position the wafer front surface up.

7.1.2 Find the center of the wafer surface.

7.1.2.1 For purposes of this document, the periphery of a wafer is assumed to be the smallest circle enclosing the wafer, disregarding fiducials and all other edge anomalies. Use the center of this circle as the center of the wafer surface.

7.1.3 Erect a right-handed Cartesian coordinate system with:

7.1.3.1 its origin at the center of the wafer surface,

7.1.3.2 the *y*-axis on the diameter in the plane of the front surface which bisects the primary fiducial (flat or notch), and

7.1.3.3 the *x*-axis on the diameter in the plane of the front surface which is perpendicular to the bisector of the primary fiducial (*y*-axis).

7.1.4 Orient the wafer so the primary fiducial is in the negative *y*-direction (see Figure 1).

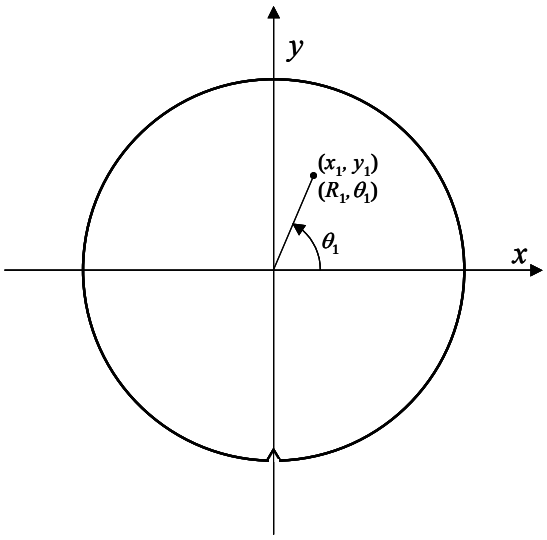
7.1.5 Take as the usual convention that the negative *y*-direction is pointing downward (on a page) or toward the operator (on a table or chuck or in a wafer carrier), and that the positive *x*-axis points toward the right.

7.1.6 Reference the polar coordinates, r and θ to the positive *x*-axis where $r = \sqrt{x^2 + y^2}$ (see Figure 1).

7.1.7 Choose Cartesian or polar coordinates according to the application.

7.2 *Back Surface Coordinates*

7.2.1 Rotate the wafer around the bisector of the primary fiducial (*y*-axis) until the back surface is up.



NOTE: The primary fiducial may be a flat or a notch.

Figure 1
Front Surface Coordinate System

7.2.2 With the primary fiducial in the negative *y* direction (downward or toward the operator), the positive *x*-axis points toward the left. In this way the *x*-*y*-coordinates of a point on the back surface are the same as the *x*-*y* coordinates of the point directly through the wafer on the front surface.

7.3 *Three-dimensional Coordinates*

7.3.1 Place the wafer with the front surface up.

7.3.2 Erect the *z*-axis through the center of the wafer surface and perpendicular to the plane of the surface with the positive direction above the front surface (see Figure 2).

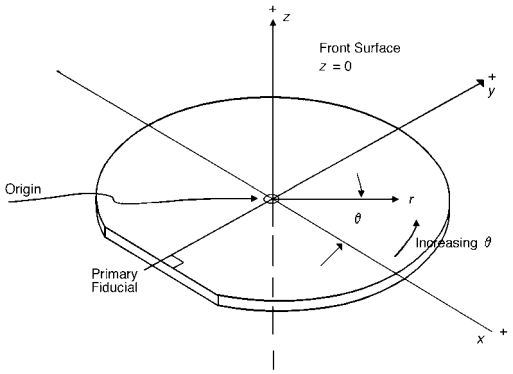
7.3.3 Assign the zero point of the *z*-axis in accordance with the application.

7.3.3.1 For example, for geometric measurements, such as warp, the center of the *z*-axis may be at the geometrical center of the wafer in three dimensions.

7.3.3.2 For front surface flatness measurements, the zero point of the *z*-axis is usually taken at the reference plane, which is chosen in accordance with the particular flatness parameter being determined.

7.3.3.3 Other applications may require locating the center of the *z*-axis at a different position.

7.3.3.4 For thickness or thickness variation measurements, the zero point of the *z*-axis may be taken at the center of the back surface of the wafer.



NOTE: The primary fiducial may be a flat or a notch.

Figure 2
Wafer Coordinate System with *z*-axis Direction Indicated

RELATED INFORMATION 1
APPLICATIONS OF THE WAFER COORDINATE SYSTEM

NOTICE: This related information is not an official part of SEMI M20. It was developed during the original development of the document. This related information was approved for publication by full letter ballot procedures.

R1-1 *SEMI E5, in Stream 12* — Wafer Mapping, delineates how a coordinate system for reporting position data may be communicated. The origin of this coordinate system, which is specified by the equipment when generating the wafer map, may be the site at any of the four corners of the array or at the array center. In addition, the stream provides for transmission of an arbitrary number of reference points to relate the map coordinate system to the physical wafer. The wafer coordinate system may be used to establish the locations of these reference points and of the origin of the map coordinate system.

R1-2 SEMI M17 defines a polar array of 1000 elements which can be used to identify the locations on a wafer of extended defects such as slip. This array is consistent with the wafer coordinate system.

SEMI M21-0304
GUIDE FOR ASSIGNING ADDRESSES TO RECTANGULAR ELEMENTS IN A CARTESIAN ARRAY

This guide was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on October 16, 2003. Initially available at www.semi.org February 2004; to be published March 2004. Originally published in 1992; last published September 1998.

1 Purpose

1.1 It is frequently very useful to have a standardized method for labeling elements in an array on a silicon wafer surface.

1.2 This guide defines an element addressing convention for locating and uniquely identifying rectangular elements in a Cartesian array.

1.3 Such arrays are useful in locating sites for site flatness characterization, defect mapping, determination of parametric distributions, etc. on unpatterned semiconductor wafers.

2 Scope

2.1 This guide covers procedures for assigning addresses that can be used to locate and identify rectangular elements in a Cartesian array. The array may be regular or tiled in one direction.

2.2 Relating the position of the array to the wafer surface is outside the scope of this guide, but it may be established through use of the wafer coordinate system defined in SEMI M20.

2.3 This guide covers procedures for assigning a unique identification (address) for each element in the array. An example of the results obtained by following this procedure are given in Related Information 1.

2.4 The element addressing convention in this guide provides an orderly progression along perpendicular directions with addresses of adjacent elements in any direction differing by 1. Consequently, distances may be calculated in a unified way.

2.5 For complex patterns, more than one array on a wafer may be defined and related to the same coordinate axes.

2.6 The element addressing convention in this guide is consistent with that of the polar array specified in SEMI M17. In addition, element addresses can be readily transformed to addresses in other types of addressing conventions for Cartesian arrays as described in Related Information 2.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M2 — Specification for Silicon Epitaxial Wafers

SEMI M11 — Specification for Silicon Epitaxial Wafers for Advanced Applications

SEMI M17 — Guide for a Universal Wafer Grid

SEMI M20 — Practice for Establishing a Wafer Coordinate System

SEMI MF1241 — Terminology of Silicon Technology

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Many terms used in silicon wafer technology are defined in SEMI MF1241.

4.2 Definitions of additional terms may be found in SEMI M1, SEMI M2, or SEMI M11.

5 Array Element Layout

5.1 The array is constructed from *m* vertical columns and *n* horizontal rows of identical elements of dimension *a* horizontally and *b* vertically. The number of elements in different rows and columns may vary to suit the application.

5.2 The address of an element is given by two numbers separated by a comma: (*i*,*j*). The first number, *i*, indicates the column and the second, *j*, the row.

5.3 The longest row and the longest column are used in identifying the Starting Element, which is assigned the address (0,0).

5.4 The array may have a tiled appearance, either with one or more rows offset relative to the row containing the Starting Element (row tiling) or with one or more columns offset relative to the column containing the Starting Element (column tiling).

5.4.1 For row tiling, the offset, t_r, is a fraction (p_r/q_r) of the horizontal element dimension, a, where p_r and q_r are small whole numbers.

5.4.2 For column tiling, the offset, t_c, is a fraction (p_c/q_c) of the vertical element dimension, b, where p_c and q_c are small whole numbers.

5.4.3 In either case, the offset may be constant or it may vary from row to row or column to column. When the offset is constant, the array pattern is repeated every q_r rows or q_c columns.

6 Element Addresses

6.1 Define the array center as the intersection of the vertical and horizontal array centerlines, found as follows:

6.1.1 If the array is regular (not tiled):

6.1.1.1 Count the number of elements, m, in the longest row.

6.1.1.2 If m is even, start at the leftmost element, count $m/2$ elements to the right, and construct a line along the right vertical boundary of this element. This line is the vertical array centerline (see Figure 1a).

6.1.1.3 If m is odd, start at the leftmost element, count the integer of $m/2$ elements to the right, continue to the next element to the right, and construct a line through the center of this element. This line is the vertical array centerline (see Figure 1b).

6.1.1.4 Count the number of elements, n, in the longest column.

6.1.1.5 If n is even, start at the topmost element, count down $n/2$ elements, and construct a line along the bottom horizontal boundary of this element. This line is the horizontal array centerline (see Figure 1c).

6.1.1.6 If n is odd, start at the topmost element, count down the integer of $n/2$ elements, continue down to the next element, and construct a line through the center of this element. This line is the horizontal array centerline (see Figure 1d).

6.1.2 If the columns of the array are tiled (see Figure 2a):

6.1.2.1 Count the number of columns, m, in the widest part of the array from left to right.

6.1.2.2 If m is even, start at the leftmost column, count $m/2$ columns to the right, and construct a line along the right vertical boundary of this column. This line is the vertical array centerline.

6.1.2.3 If m is odd, start at the leftmost column, count the integer of $m/2$ columns to the right, continue to the next column to the right, and construct a line through the center of this column. This line is the vertical array centerline.

6.1.2.4 Count the number of elements, n', in the column which contains or is immediately to the right of the vertical array centerline, depending on whether m is odd or even, respectively.

NOTE 1: The number, n', is usually equal to but may be less than n.

6.1.2.5 If n' is even, start at the topmost element, count down $n'/2$ elements, and construct a line along the bottom horizontal boundary of this element. This line is the horizontal array centerline.

6.1.2.6 If n' is odd, start at the topmost element, count down the integer of $n'/2$ elements, continue down to the next element, and construct a line through the center of this element. This line is the horizontal array centerline.

6.1.3 If the rows of the array are tiled (see Figure 2b):

6.1.3.1 Count the number of rows, n, in the widest part of the array from top to bottom.

6.1.3.2 If n is even, start at the topmost row, count down $n/2$ rows, and construct a line along the bottom horizontal boundary of this row. This line is the horizontal array centerline (see Figure 1c).

6.1.3.3 If n is odd, start at the topmost row, count down the integer of $n/2$ rows, continue down to the next row, and construct a line through the center of this row. This line is the horizontal array centerline (see Figure 1d).

6.1.3.4 Count the number of elements, m', in the row which contains or is immediately above the vertical array centerline, depending on whether n is odd or even, respectively.

NOTE 2: The number, m', is usually equal to but may be less than m.

6.1.3.5 If m' is even, start at the leftmost element, count $m'/2$ elements to the right, and construct a line along the right vertical boundary of this element. This line is the vertical array centerline.

6.1.3.6 If m' is odd, start at the leftmost element, count the integer of $m'/2$ elements to the right, continue to the next element to the right, and construct a line through the center of this element. This line is the vertical array centerline.

6.2 Locate the Starting Element (0,0) as follows:

6.2.1 If the array center falls within an element, designate that element as the Starting Element (see Figure 3a).

6.2.2 If the array is regular and the array center lies at an element corner, designate the element to the right and immediately above the array center as the Starting Element (see Figure 3b).

6.2.3 If the array is regular and the array center lies on a vertical element boundary, designate as the Starting Element that element which contains the horizontal array centerline and is immediately to the right of the vertical array centerline (see Figure 3c).

6.2.4 If the array is regular and the array center lies on a horizontal element boundary, designate as the Starting Element that element which contains the vertical array centerline and is immediately above the horizontal array centerline (see Figure 3d).

6.2.5 If columns of the array are tiled and the array center lies on a vertical boundary between columns, designate that element immediately to the right of the vertical centerline and containing the horizontal array centerline as the Starting Element. If the horizontal array centerline also falls on an element boundary in the column immediately to the right of the vertical array centerline, designate the element in this column and immediately above the horizontal array centerline as the Starting Element (see Figure 4a).

6.2.6 If rows of the array are tiled and the array center lies on a horizontal boundary between rows, designate that element immediately above the horizontal array centerline and containing the vertical array centerline as the Starting Element. If the vertical array centerline also falls on an element boundary in the row immediately above the horizontal array centerline, designate the element in this row and immediately to the right of the vertical array centerline as the Starting Element (see Figure 4b).

6.3 Assign addresses to the array elements as follows:

6.3.1 Elements along the horizontal array centerline:

6.3.1.1 If the horizontal array centerline passes through an element, assign that element the address (*i*,0), where *i* is the column number. The first column to the right of the vertical array centerline is numbered 1, the next column to the right is numbered 2, the next column to the right is numbered 3, etc. Similarly, the first column to the left of the vertical array centerline is numbered -1, the next column to the left is numbered -2, the next column to the left is numbered -3, etc. (see Figure 3a).

6.3.1.2 If the horizontal array centerline falls along an element boundary in any column, *i*, assign the address (*i*,0) to the element in that column which lies immediately above the horizontal array centerline (see Figure 3b).

6.3.2 Elements along the vertical array centerline:

6.3.2.1 If the vertical array centerline passes through an element, assign that element the address (0,*j*), where *j* is the row number. The first row above the horizontal array centerline is numbered 1, the next row up is numbered 2, the next row up is numbered 3, etc. Similarly the first row below the horizontal array centerline is numbered -1, the next row down is numbered -2, the next row down is numbered -3, etc. (see Figure 3a).

6.3.2.2 If the vertical array centerline falls along an element boundary in any row, *j*, assign the address (0,*j*) to the element in that row which lies immediately to the right of the vertical array centerline (see Figure 3b).

6.3.3 Remaining elements:

6.3.3.1 Assign addresses (*i*,*j*) to the remaining elements based on their position relative to the elements along the horizontal and vertical array centerlines. For example the address of the element immediately above (1,0) is (1,1) and the element immediately below (1,0) is (1,-1) (see Figure 5).

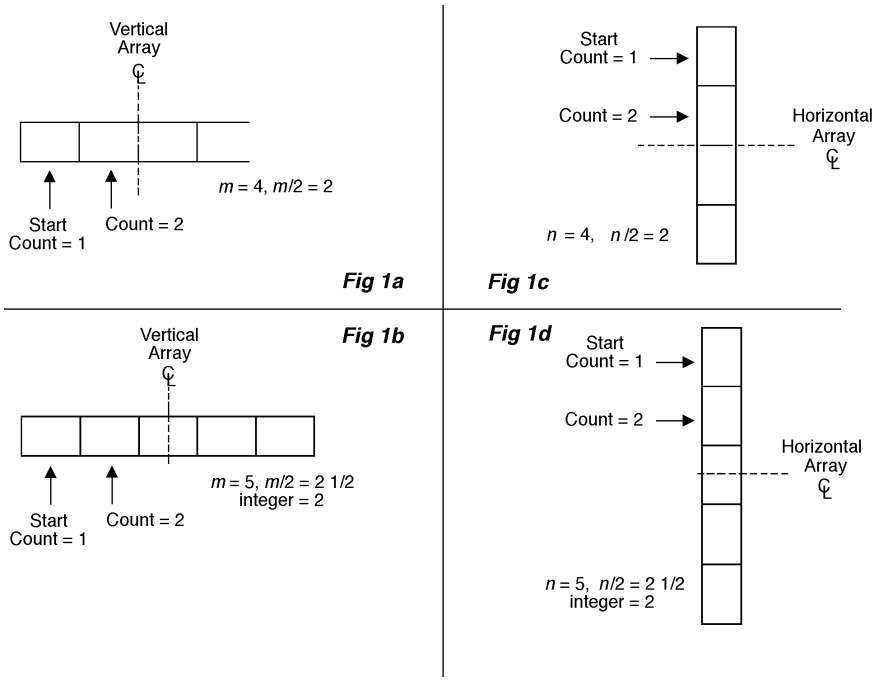


Figure 1
Array Centerlines

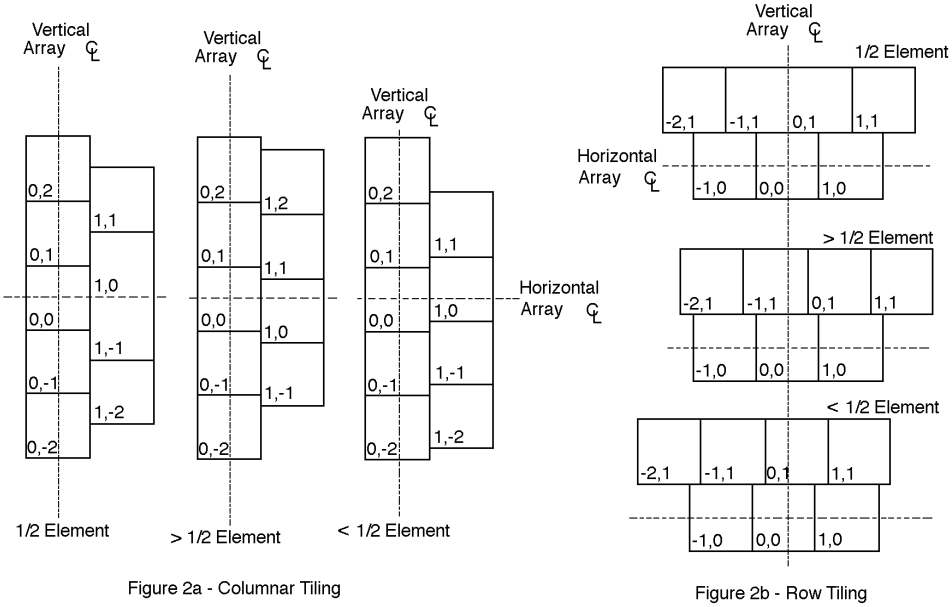


Figure 2
Tiling

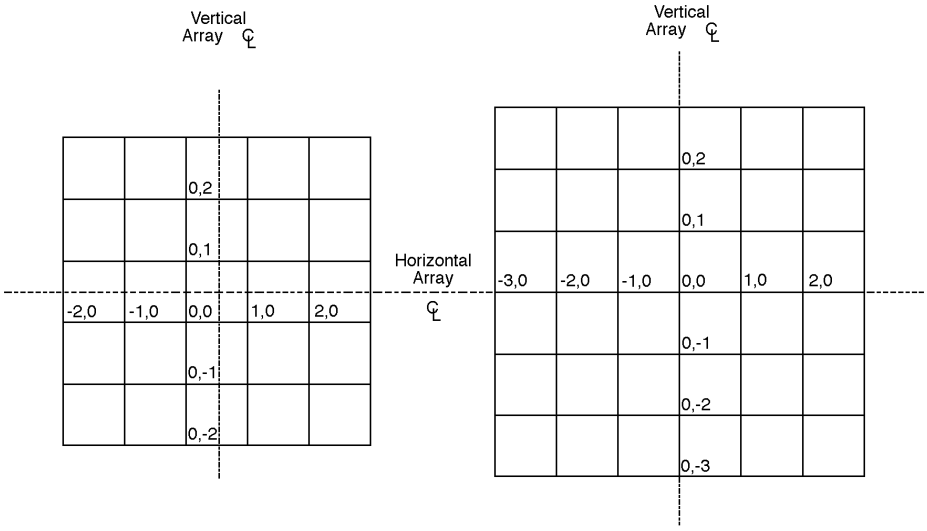


Figure 3a - Array Center within an Element

Figure 3b - Array Center on Element Corner

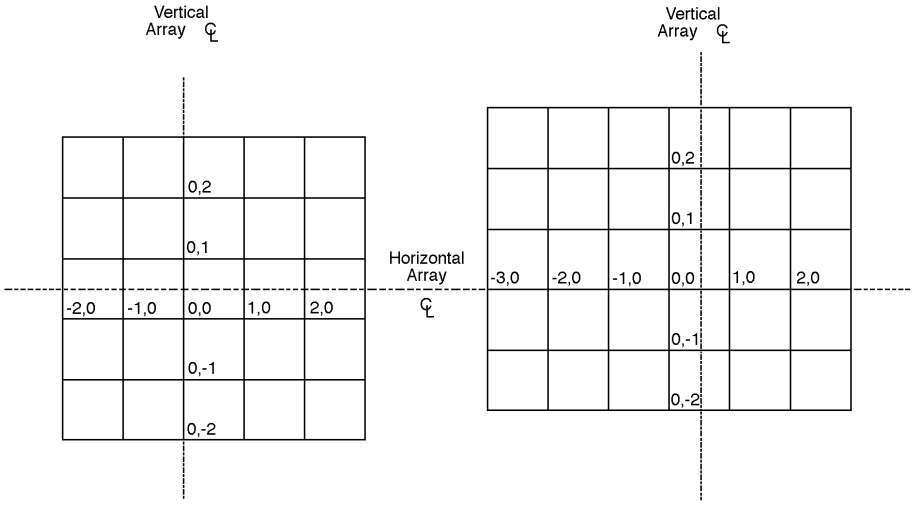


Figure 3c - Array Center along Element Vertical Edge

Figure 3d - Array Center along Element Horizontal Edge

Figure 3
On-Centerline Element Numbering

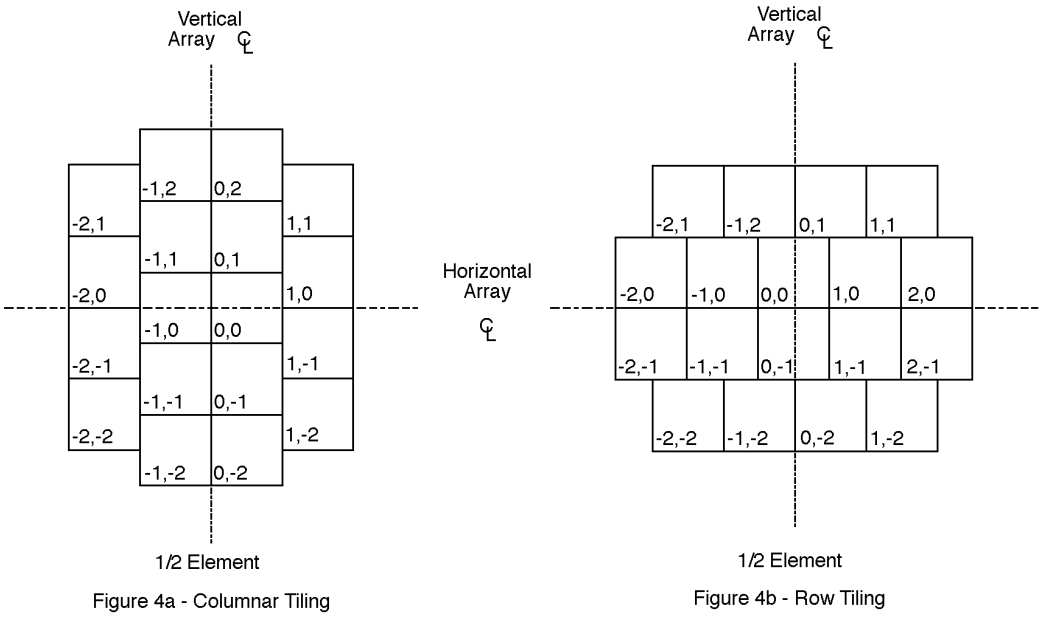


Figure 4a - Columnar Tiling

Figure 4b - Row Tiling

Figure 4
Tiled Element Numbering

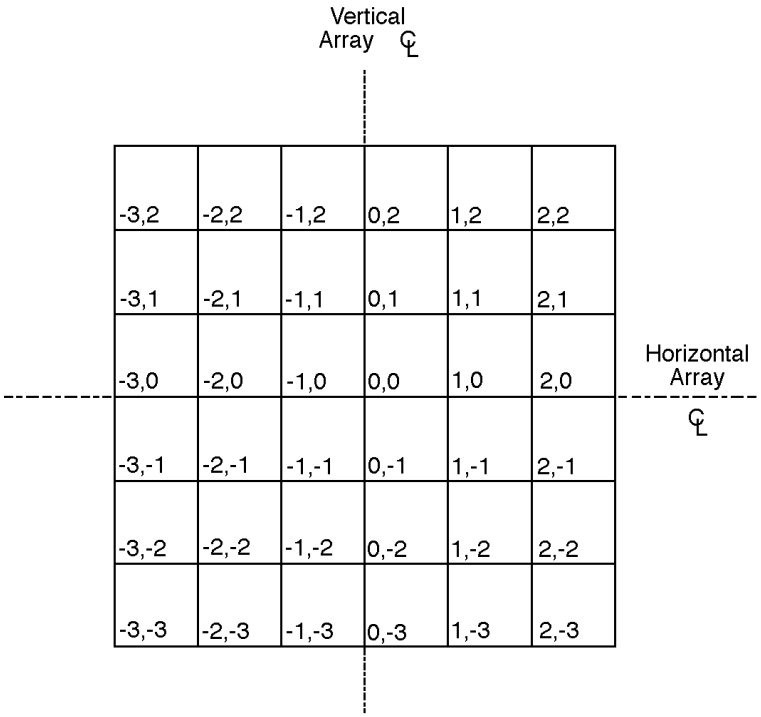


Figure 5
All Elements Numbered

RELATED INFORMATION 1
AN EXAMPLE OF ASSIGNING ADDRESSES TO AN ARRAY

NOTICE: This related information is not an official part of SEMI M21. It was developed during the original development of the document. This related information was approved for publication by full letter ballot on October 16, 2003.

R1-1 An example of a regular 29-column by 9-row array, truncated for application to a wafer, is shown in Figure R1-1. The Starting Element includes the array center because there are odd numbers of both columns and rows. In addition, Figure R1-1 shows the element addresses for elements along the right half of the horizontal array centerline, for elements along column 1, and for selected other elements in the array. Also shown are the left hand corner elements (which lie outside the truncated array).

R1-2 Figure R1-2 shows the same truncated array fitted onto a wafer. Because the truncation is not symmetrical around the vertical array centerline, the array center is located to the left of the wafer center.

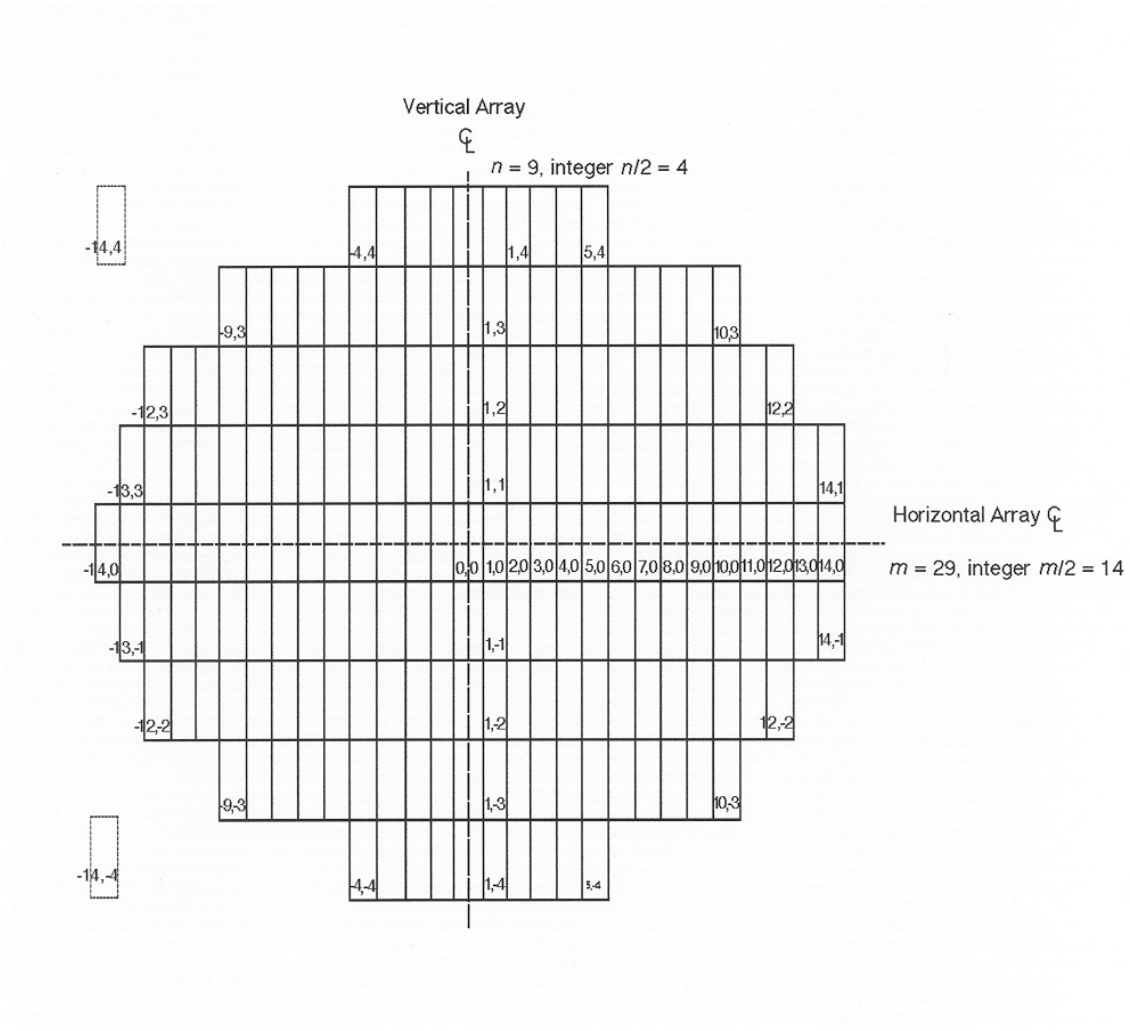


Figure R1-1
Array Truncated for Application to a Wafer

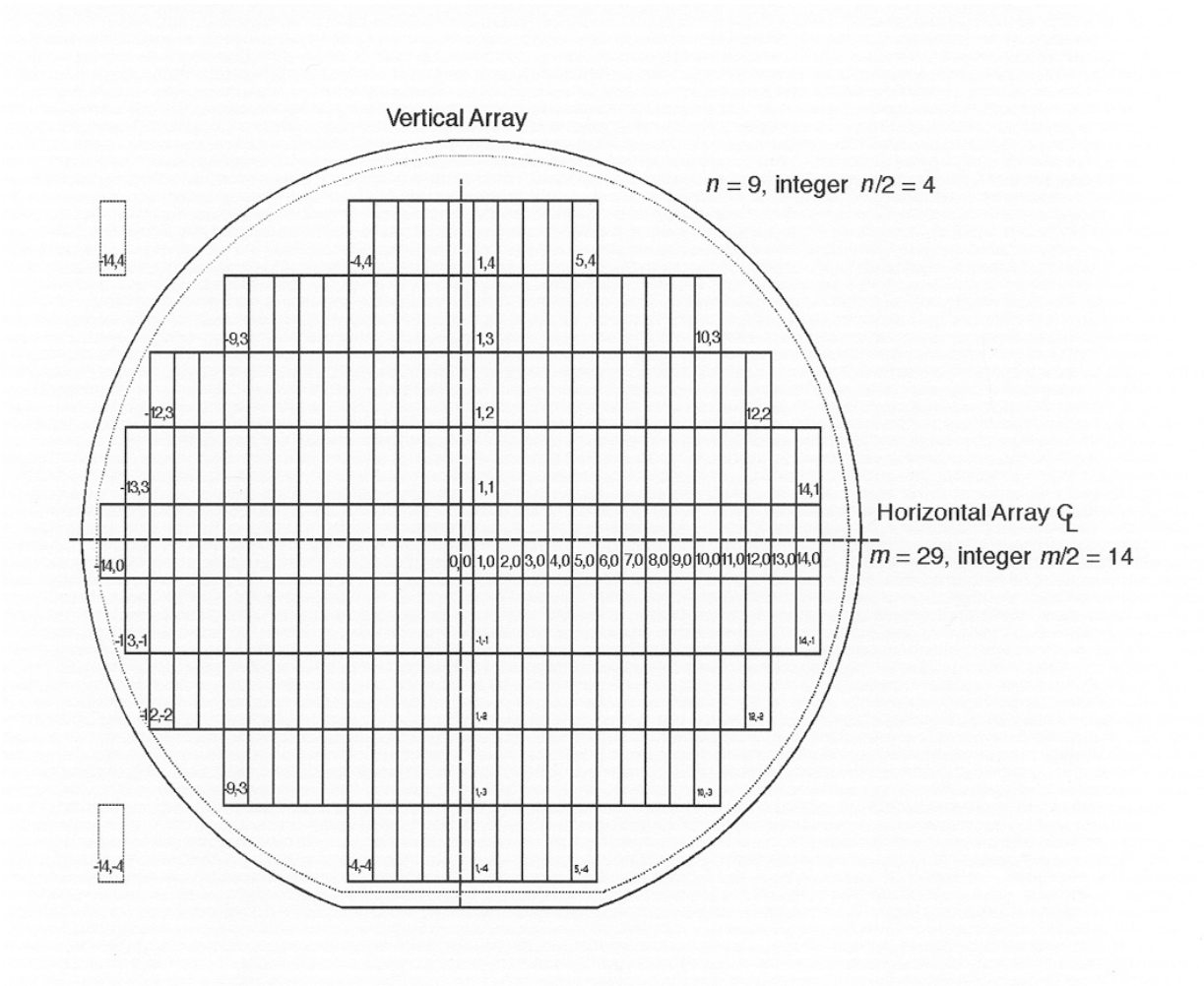


Figure R1-2
Truncated Array on the Wafer

RELATED INFORMATION 2
EXTENSIONS TO OTHER ELEMENT ADDRESSING CONVENTIONS

NOTICE: This related information is not an official part of SEMI M21. It was developed during the original development of the document. This related information was approved for publication by full letter ballot on October 16, 2003.

R2-1 Element addressing conventions other than that covered by this guide are also widely used in engineering. Two of these are illustrated in Figure R2-1 with the use of the same truncated array discussed in Related Information 1.

R2-2 *First-Quadrant Convention*

R2-2.1 Addresses in this convention start at the lower left corner of the array and increase to the right and upward in the same way as in the convention covered by this guide. The lower left corner of the array is defined by the intersection of the bottom boundary of the lowest row and the left boundary of the leftmost column. In the case of tiling, the boundaries are those of the lowest elements and the leftmost elements in the array. The lower left corner may fall outside the useful portion of the array. The lower left element of the array is the element immediately to the right and above the lower left corner of the array.

R2-2.2 The First-Quadrant Convention uses a column, row address but does not have a zero row or a zero column.

R2-2.3 The addresses of the corners of an array with m columns and n rows in the First-Quadrant Convention are as follows:

- lower left (Starting Element): (1,1)
- lower right: (m,1)
- upper left: (1,n)
- upper right: (m,n)

R2-2.4 The general formulas for obtaining the addresses of any element (i_f,j_f) in the First-Quadrant Convention from the addresses (i,j) in the convention covered by this guide are as follows:

$$i_f = i + \text{integer}(m/2) + 1$$
$$j_f = j + \text{integer}(n/2) + 1$$

R2-2.5 These equations also apply to arrays with column or row tiling if $n' = n$ or $m' = m$, respectively. If this condition is not met, the displacement of the row or column which defines the array centerline with respect to the boundary of the array must be known to transform the addresses.

R2-3 *Row, Column (Matrix) Convention*

R2-3.1 Addresses in this convention start at the upper left corner of the array and increase to the right and downward. The upper left corner of the array is defined by the intersection of the top boundary of the highest row and the left boundary of the leftmost column. In the case of tiling, the boundaries are those of the highest elements and the leftmost elements in the array. The upper left corner may fall outside the useful portion of the array. The upper left element of the array is the element immediately to the right and below the upper left corner of the array.

R2-3.2 The Row, Column (Matrix) Convention uses a row, column address and, like the First-Quadrant Convention, does not have a zero row or a zero column.

R2-3.3 The addresses of the corners of an array with m columns and n rows in the Row, Column (Matrix) Convention are as follows:

- upper left (Starting Element): (1,1)
- upper right: (1,m)
- lower left: (n,1)
- lower right: (n,m)

R2-3.4 The general formulas for obtaining the addresses of any element (i_m,j_m) in the Row, Column (Matrix) Convention from the addresses (i,j) in the convention covered by this guide are as follows:

$$i_m = \text{integer}(n/2) + 1 + j$$
$$j_m = \text{integer}(m/2) + 1 + i$$

R2-3.5 These equations also apply to arrays with column or row tiling if $n' = n$ or $m' = m$, respectively. If this condition is not met, the displacement of the row or column which defines the array centerline with respect to the boundary of the array must be known to transform the addresses.

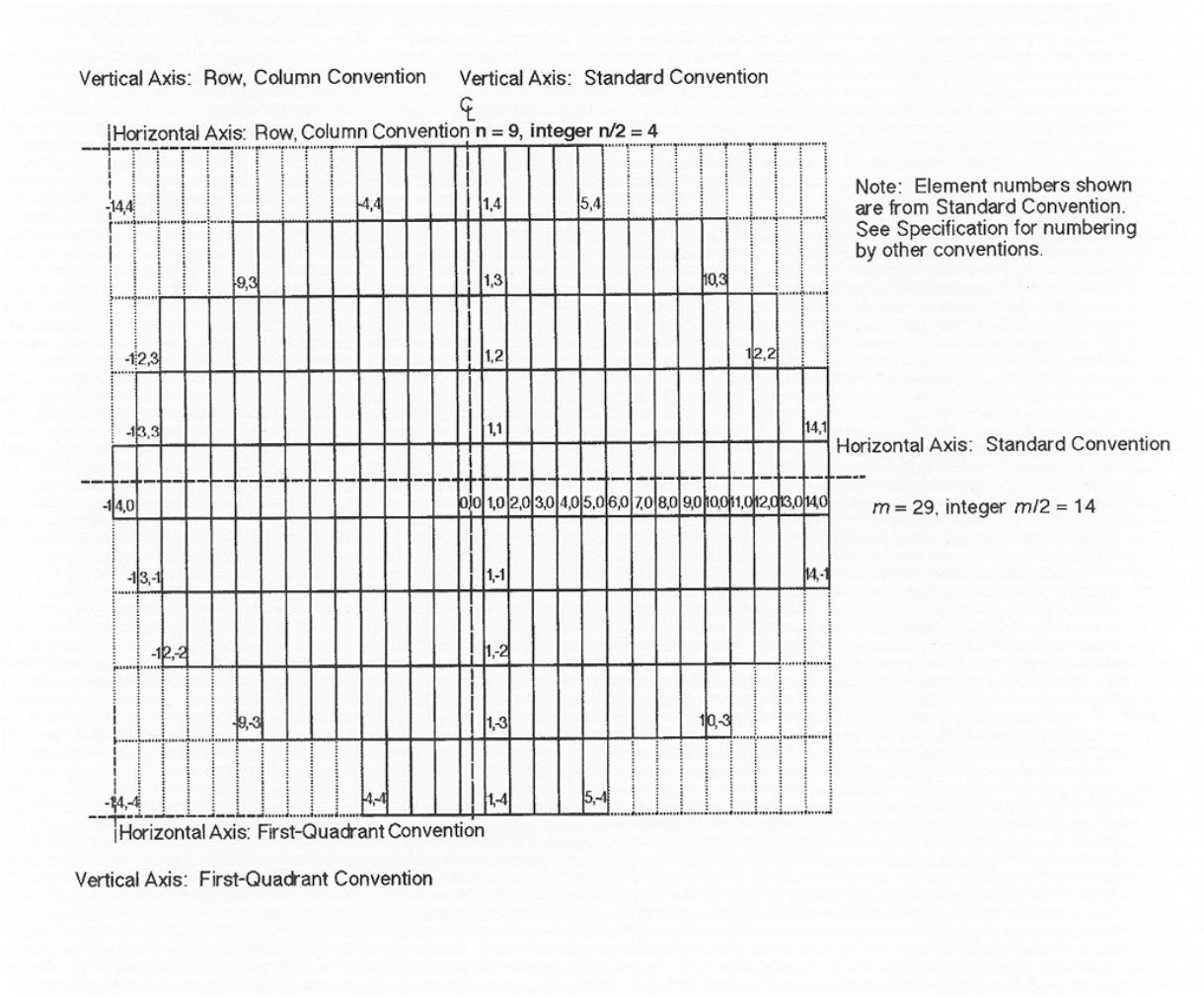


Figure R2-1
Comparison of Array Addressing Conventions

NOTICE: SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copyrighted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI M22-0303
SPECIFICATION FOR DIELECTRICALLY ISOLATED (DI) WAFERS

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on October 25, 2002. Initially available at www.semi.org December 2002; to be published March 2003. Originally published in 1992; previously published in December 1996.

1 Purpose

1.1 Dielectrically isolated (DI) wafers are used for fabricating specialized semiconductor devices, including radiation tolerant devices. This specification is intended to aid the definition and procurement of such wafers.

2 Scope

2.1 This specification defines requirements for DI wafers used for semiconductor device manufacture. By defining inspection procedures and acceptance criteria, both suppliers and consumers may uniformly define product characteristics and quality requirements.

NOTE 1: This document currently applies only to DI wafers with nominal diameter of 100 mm.

2.2 The primary standardized properties set forth in this specification relate to physical, electrical, and surface defect parameters of DI wafers.

2.3 A complete purchase specification requires that additional physical properties be specified along with suitable test methods for their measurements.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standard*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

3.2 *ASTM Standard*[1]

F 523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

3.3 *Other Standard*[2]

ANSI/ASQC Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Definitions*

4.1.1 *concentricity* — The distance between the centerpoint of the DI wafer and the centerpoint of the photolithographic pattern.

4.1.2 *connected tubs* — Adjacent tubs which are not completely surrounded by an oxide but are connected by silicon (see Figure 1).

4.1.3 *DI wafer* — A wafer consisting of polysilicon, oxide, and single crystal silicon regions. A typical cross-section is shown in Figure 2.

4.1.4 *edge indent* — An edge defect on a DI wafer that extends from the front surface to the back surface.

4.1.5 *electrical die* — An identifiable repetitive monolithic combination of tubs and polysilicon areas in a DI wafer surrounded by a grid border which as packaged becomes a component.

4.1.6 *layer of polycrystalline silicon* — The thick matrix material of a DI wafer in which the silicon tubs reside.

4.1.7 *pattern deformation* — A microscopic defect associated with missing or indented tub features of 4 microns or more (see Figure 3).

4.1.8 *rotation* — The angle of deviation between the primary flat of the DI wafer and the x-axis of the photolithography pattern.

4.1.9 *tub* — A single crystal silicon region in a DI wafer which is surrounded by an oxide layer on the sides and bottom.

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

2 American National Standards Institute, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023 Website: www.ansi.org

4.1.10 *tub depth* — The thickness of the tub as measured from the wafer surface to the buried oxide layer parallel to the wafer surface (see Figure 2).

4.1.11 *void in the polycrystalline silicon* — A microscopic depression on the surface of polysilicon areas in DI wafers (see Figure 4).

5 Ordering Information

5.1 Purchase orders for dielectrically isolated wafers shall include the following items:

5.1.1 Tub Characteristics

A. Resistivity

B. Conductivity and Dopant Type

C. Crystal Growth Method (Czochralski or Float Zone)

5.1.2 Tub Diffused Layers (if required)

A. Sheet Resistance

B. Junction Depth

C. Dopant Type

5.1.3 Polysilicon Resistivity

5.1.4 Nominal Tub Depth

5.1.5 Method of Pattern Transfer from User to Supplier

5.1.5.1 The pattern transfer of electrical die information may be accomplished through a physical exchange of photomasks or through a data exchange. Issues such as corner compensations, design rules, and alignment features shall be agreed upon between the supplier and purchaser.

5.1.6 Oxide Thickness of Isolation Layer

5.1.7 Methods of Test and Measurements (see Section 7)

5.1.8 Lot Acceptance Procedures (see Section 8)

5.1.9 Certification (if required) (see Section 9)

5.1.10 Packing and Marking (see Section 10)

6 Requirements

6.1 The complete specification for the starting substrates to produce DI wafers includes all general requirements of SEMI M1.

6.2 The Dimension and Tolerance Requirements for 100 mm DI wafers are listed in Table 1.

6.3 Visual defects on a wafer shall not exceed the limits established in Table 2.

6.4 Microscopic defects on a die and defective die on a wafer shall not exceed the limits as established in Table 3. To meet these specifications, at least 75% of the die on a wafer must be defect free.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units (see Note 1)*
Diameter	100	± 0.50	mm
Thickness, Center Point	508	± 25	mm
Surface Orientation, referenced to tub crystal axes	{100}	± 1	deg
Primary Flat Orientation, referenced to tub crystal axes	{110}	± 1	deg
Primary Flat Length	32.5	± 2.5	mm
Secondary Flat Location, optional			
Secondary Flat Length	18.0	± 2.0	mm
Bow, Max.	+ 380		µm
Total Thickness Variation, Max.	25		µm
Concentricity, Max.	3		mm
Rotation, Max.	2		deg
Edge Profile Coordinate, C_y *(see Note 2)*	170		µm

Note 1: For referee purposes the metric (SI) units apply.
Note 2: See SEMI M1, Figure 4.

Table 2 DI Wafer Defect Limits — Visual

Item	*Characteristics*	*Defect Limit*	*Illumination See Note #3*	*Notes*
1	Edge Chips Maximum Number Maximum Size	3 6.35 mm^2	Diffused	
2	Contamination, Area Minimum % of clean surface area	95%	High Intensity	1, 2
3	Cracks	None	Diffused	
4	Fractures	None	Diffused	
5	Holes	None	High Intensity	
6	Scratches Total Cumulative Length Not to Exceed	1/2 Diameter	High Intensity	1, 2
7	Pits Maximum Number Maximum Size	5 0.1 mm^2	High Intensity	1, 2

Note 1: The outer 5 mm annulus is excluded from these criteria.
Note 2: These criteria are concerned only with polished front surfaces of DI wafers.
Note 3: See ASTM Practice F 523 for definition of Illumination Conditions.

Table 3 DI Wafer Defect Limits — Microscopic

Item	*Characteristics*	*Defect Limit (per die)*	*Defect Limit (per wafer)*	*Notes*
8	Connected Tubs	None	"	
9	Pattern Deformation	None	"	
10	Polysilicon Voids	None	"	
11	Tub Depth (> + 5% or < − 5% from nominal value)	None	"	
12	Defective Die		25%	1

Note 1: The number of defects per die is not cumulative; an electrical die with one or more defects is counted as a single defective die.

7 Test Methods and Measurements

7.1 The supplier and purchaser shall agree in advance on the means for making all measurements (see Section 9).

7.2 *DI Wafer Characteristics*

7.2.1 *Tub Characteristics* — The resistivity, conductivity, dopant type, and crystal growth method are difficult to ascertain in the finished DI wafers. Verification test procedures or certification of these characteristics shall be agreed upon between the supplier and the purchaser (see Section 9).

7.2.2 *Tub Diffused Layers* — The test procedures to measure the sheet resistance, junction depth, and dopant type shall be agreed upon between supplier and purchaser (see Section 9).

7.2.3 *Visual Surface Defects and Contamination* — Determine in accordance with ASTM Practice F 523.

7.2.4 *Microscopically Observed Die Defects* — Examine a representative sampling of die (see Section 8.2) with an optical microscope with magnification such that one complete electrical die fills the field of view. If necessary for verification of defects, move to higher magnifications as required. Due to the extensive microscopic inspections required, verification test procedures or certification of these characteristics shall be agreed upon between the supplier and the purchaser (see Section 9).

8 Sampling

8.1 Unless otherwise specified, appropriate sample sizes shall be selected from each lot according to ANSI/ASQC Z1.4-1993. Each quality characteristic shall be an assigned an acceptable quality level (AQL) in accordance with ANSI/ASQC Z1.4-1993. Inspection levels shall be agreed upon between supplier and purchaser.

8.2 The sampling plan for microscopic inspection of die on the wafer, including number and location of inspected die, shall be agreed upon between supplier and purchaser.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of test results, shall be furnished at the time of shipment.

9.2 The supplier and purchaser may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 7; however, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Packing and Marking

10.1 Special packing requirements shall be subject to agreement between the supplier and purchaser. Otherwise all wafers shall be handled, inspected, and

packed in such a manner to avoid chipping, scratches, and contamination, and in accordance with the best industry practices to provide protection against damage during shipment.

10.2 The wafers supplied under this specification shall be identified by appropriately labeling the outside of each box or container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include supplier's name and reference no., date, quantity, DI wafer diameter, DI wafer thickness, and customer code no. The reference number assigned by the supplier shall provide ready access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one year after the particular lot has been shipped.

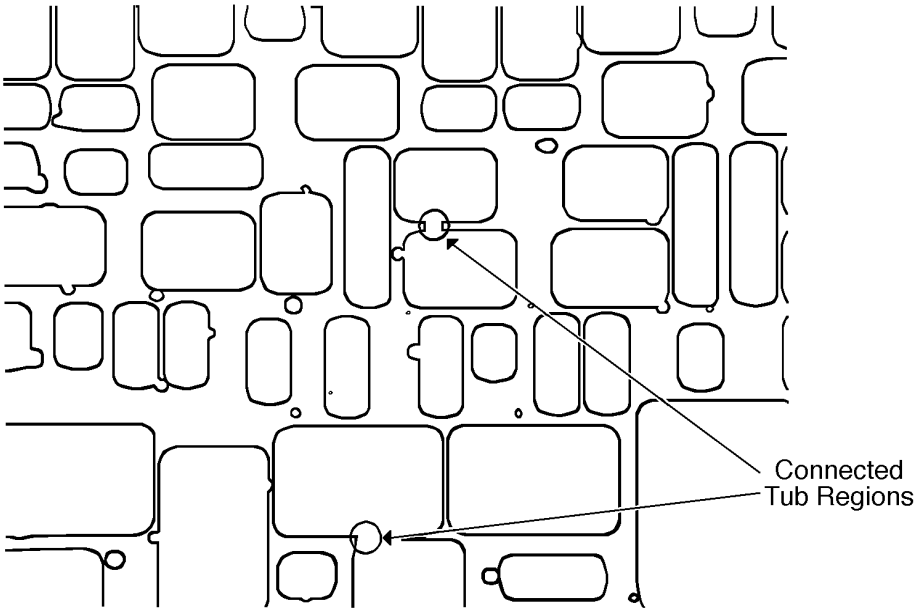


Figure 1
Connected Tubs

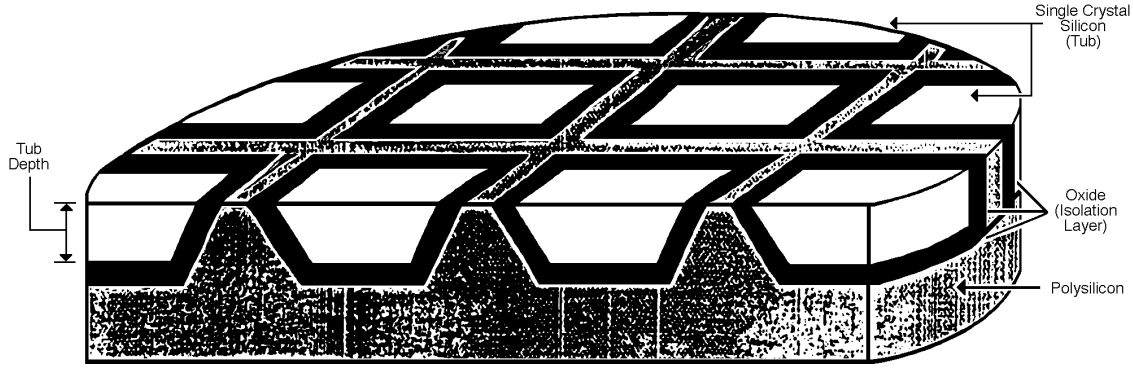


Figure 2
Cross-Section of DI Wafer

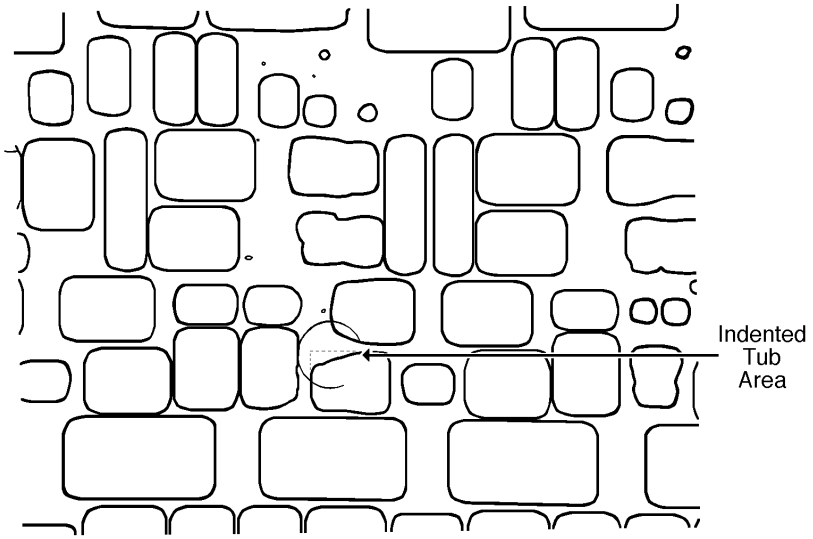


Figure 3
Pattern Deformation

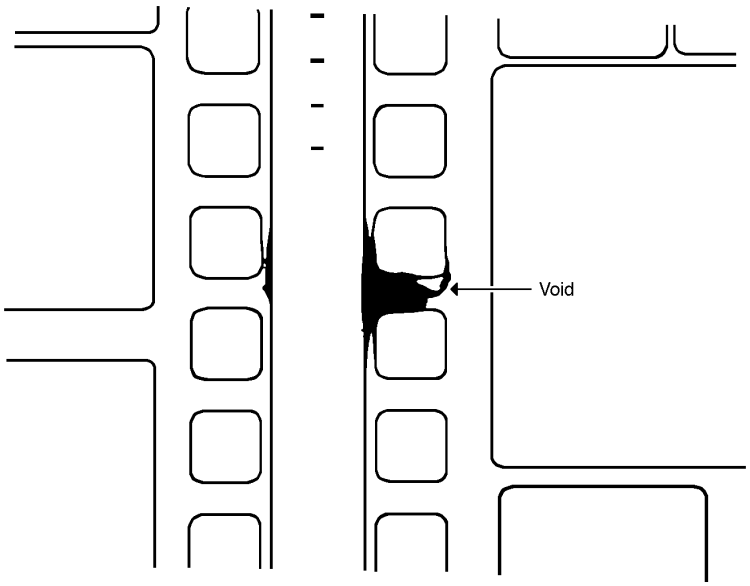


Figure 4
Void in the Polycrystalline Silicon

NOTICE: SEMI makes no warranties or representations as to the suitability of the standard set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials or equipment mentioned herein. These standards are subject to change without notice.

By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI M23-0703
SPECIFICATION FOR POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the North American Compound Semiconductor Committee. Current edition approved by the North American Regional Standards Committee on November 27, 2001. Initially available at www.semi.org December 2001; to be published March 2002. Originally published in 1993; previously published October 2000.

NOTICE: The designation of SEMI M23 was updated during the 0703 publishing cycle to reflect the addition of SEMI M23.6.

1 Purpose

1.1 These specifications cover the substrate requirements for monocrystalline high-purity indium phosphide wafers used in semiconductor and electronic device manufacturing. Dimensional and crystallographic orientation characteristics are the only standardized properties set forth below.

1.2 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed together with test methods suitable for determining their magnitude where such procedures are documented.

2 Scope

2.1 These specifications are directed specifically to indium phosphide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.2 The material is Single Crystal Indium Phosphide (InP) having a cubic zinc blende structure and the following properties:

Density	4.787 g/cm^3
Melting Point	1062°C
Dielectric Constant	12.4
Lattice Parameter	5.869 A at 27° C
Energy Gap	1.351 eV at 27° C

2.3 For reference purposes SI (System International, commonly called metric) units shall be used.

2.4 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M39 — Test Method for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility on Semi-Insulating GaAs Single Crystals

3.2 *ASTM Standards*[1]

ASTM E122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

ASTM F26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

ASTM F42 — Test Method for Conductivity Type of Extrinsic Semiconducting Materials

ASTM F76 — Test Methods for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Single Crystal Semiconductors

ASTM F84 — Test Methods for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

ASTM F154 — Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

ASTM F523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

ASTM F533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

ASTM F534 — Test Method for Bow of Silicon Wafers

ASTM F613 — Test Method for Measuring Diameter of Semiconductor Wafers

ASTM F657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Non-Contact Scanning

ASTM F671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959 (All cited standards except for E122 may be found in Volume 10.05 of the Annual Book of ASTM Standards; E122 may be found in Volume 14.02.)

ASTM F673 — Test Method for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

ASTM F928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

ASTM F1241 — Terminology of Silicon Technology

ASTM F1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements with a Mercury Probe

ASTM F1393 — Test Method for Determining Net Carrier Density in Silicon Wafers by Miller Feedback Profiler Measurements with a Mercury Probe

3.3 *Other Standards*

ANSI/ASQC[2] Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

DIN[3] Standard Test Method 50454-2 — Determination of the Dislocation Etch Pit Density in Monocrystals of III-V Compound Semiconductors - Part 2: Indium Phosphide.

DIN Test Method 50448 — Testing of Materials for Semiconductor Technology – Contactless Determination of the Electrical Resistivity of Semi-Insulation Semiconductor Slices using a Capacitive Probe

4 Terminology

4.1 *Definitions*

NOTE 1: The selected terminology defined here has been adopted from ASTM Standard F1241. Updates to this section are dependent on information exchange between ASTM and SEMI. Definitions are included for the benefit of the user, however, for a complete list, please refer to ASTM Standard F1241.

4.1.1 *bow (of a semiconductor wafer)* — the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer. Contrast flatness. Also see warp.

4.1.2 *dopant* — a chemical element, usually from the second, fourth, or sixth column of the periodic table for the case of III-V compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.3 *edge profile* — on wafers whose edges have been rounded by mechanical and/or chemical means, a description of the contour of the boundary of the wafer that joins the front and back surfaces.

4.1.4 *lot* — for the purpose of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.5 *orthogonal misorientation* — in { 100} wafers cut intentionally "off-orientation," the angle between the projection of the vector normal to the wafer surface onto the { 100} plane and the projection on that plane of the nearest direction (see Figure 5).

4.1.6 *TIR* — on a wafer surface, the smallest perpendicular distance between two planes, both parallel with the reference plane, which enclose all points on the front surface of a wafer within the flatness quality area or the site, depending on which is specified.

4.1.7 *TTV, total thickness variation* — of a semiconductor wafer, the difference between the maximum and minimum values of the thickness of the wafer.

4.1.8 *warp* — of a semiconductor wafer, the difference between the maximum and minimum distances of the median surface of a free, unclamped wafer from a reference plane, encountered during a scan pattern.

5 Ordering Information

5.1 Purchase orders for indium phosphide wafers furnished to this specification shall include the following items:

5.1.1 Nominal diameter (see applicable SEMI Standard for Polished InP wafers),

5.1.2 Thickness (see applicable SEMI Standard for polished InP Wafers),

5.1.3 Total Thickness Variation, TIR, warp and bow (determined by agreement between supplier and purchaser as to limits),

5.1.4 Surface orientation (see applicable SEMI Standard for polished InP wafers). There is only one option of flat location for 2" diameter polished monocrystalline InP wafers. The Dove-Tail option as illustrated in Figures 1 and 3 is used for 2" diameter InP. There is a choice of dovetail or V-Groove options for 3" and 100mm diameter wafers. These designations

2 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

3 Deutsches Institut fur Normung e.v., available from Beuth Verlag, Burggrafenstrasse 6, D-10787 Berlin, Germany

describe the shape of groove that can be etched perpendicular to the primary flat. The following are the options of wafer surface orientation:

A. (100) ± 0.5° as shown in Figures 1 and 2

B. (100) off 2° toward any of the nearest (110) planes. Examples shown in Figures 3 and 4.

Direction of off-orientation can be designated by α angle. (See Figure 5)

Figure 5 illustrates orthogonal misorientation.

5.1.5 Lot acceptance procedures (see Section 8),

5.1.6 Certification (see Section 11),

5.1.7 Packing and Marking (see Section 12).

5.2 *Optional Criteria* — The following items may be specified optionally in addition to those listed above:

5.2.1 Crystal growth method,

5.2.2 Etch Pit Density (EPD) of Crystal,

5.2.3 Crystal Growth Perfection,

5.2.4 Impurity Type,

5.2.5 Surface Condition of Wafer,

5.2.6 Edge Profile (see Figures 6 and 7),

5.2.7 Mobility,

5.2.8 Resistivity, and

5.2.9 Carrier Concentration.

6 Materials and Manufacture

6.1 The material shall consist of wafers from ingots grown to the material defined in the purchase order or contract.

7 Physical and Electrical Requirements

7.1 The material shall conform to the crystallographic orientation details as specified in the applicable polished indium phosphide wafer standard.

7.2 The material shall conform to the details specified in the purchase order or contract as follows:

7.2.1 Conduction Type,

7.2.2 Dopant,

7.2.3 Carrier Concentration,

7.2.4 Resistivity,

7.2.5 Etch Pit Density,

7.2.6 Mobility,

7.2.7 Surface Characteristics, and

7.2.8 Growth Methods.

8 Sampling

8.1 Unless otherwise specified, ASTM Practice E122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4-1993. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4-1993 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

9 Test Methods[4]

9.1 *Diameter* — Determined by ASTM Test Method F613.

9.2 *Thickness, Center Point* — Determined by ASTM Test Method F533.

9.3 *Flat Length* — Determined by ASTM Test Method F671.

9.4 *Flat Orientation*[5] — Determined by etching method identified in the appropriate InP wafer standard.

9.5 *Total Thickness Variation* — Determined by ASTM Test Method F533 or F657.

9.6 *Surface Orientation* — Determined by ASTM Test Method F26.

9.7 *Orthogonal Misorientation* — Determined by a method agreed upon between the supplier and purchaser.

9.8 *Surface Defects and Contamination* — Determined by ASTM Test Methods F154, F523 or a method agreed upon between the supplier and purchaser.

9.9 *Mobility* — Determined by ASTM Test Methods F76 or SEMI M39.

4 InP wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as a micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must, therefore, be used in the selection and execution of measurement methods.

5 Relating to the etchant used for identifying V-groove and/or dovetail direction, see reference: “HBr-K2 Cr2O7 – H2O etching system for indium phosphide” J.L. Weyher, et al. Materials Science and Engineering B28 (1994) 488-492.

9.10 *Resistivity of Semi-insulating Wafers* — Determined by ASTM Test Method F76 or SEMI M39 or DIN 50448.

9.11 *Conductivity or Resistivity of Doped Wafers* — Determined by ASTM Test Method F76 or F84 or F673.

9.12 *Carrier concentration* — Determined by ASTM Test Method F76 or F1392 or F1393 or Electrochemical CV[6].

9.13 *Conductivity Type* — Determined by ASTM Test Method F42 or F76.

9.14 *Crystal Perfection* — Determined by a method agreed upon between the supplier and purchaser.

9.15 *Edge Contouring* — Determined by ASTM Test Method F928.

9.16 *Bow* — Determined by ASTM Test Method F534 or a method agreed upon between the supplier and purchaser.

9.17 *Etch Pit Density* (*EPD*) — Determined by DIN Standard Test Method 50454-2

10 Standard Defect Limits

10.1 Limits are determined by an agreement between supplier and purchaser.

11 Certification

11.1 A manufacturer' s or supplier' s certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results. A certification shall be furnished at the time of shipment, upon the request of the purchaser in the contract or order.

12 Packing and Marking

12.1 Special packing and marking requirements shall be subject to agreement between the supplier and the purchaser. Otherwise, all wafers shall be handled, inspected, and packed with the best industry practices to provide ample protection against damage during shipment.

12.2 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision that the wafers will be stored prior to further processing. Identification shall include lot number and wafer number. Per the agreement between the supplier and purchaser, the following must be accessible from the lot and wafer numbers: nominal diameter, conductive dopant, orientation, resistivity, and EPD. Such information shall be retained on file at the manufacturer' s facility for at least one month or as negotiated between vendor and user after that particular lot has been accepted by the purchaser.

13 Related Documents

"HBr-$K_2Cr_2O_7$ – H_2O etching system for indium phosphide" J.L. Weyher, et al. Materials Science and Engineering B28 (1994) 488-492.

6 NOTE: Electrochemical CV test method has not been completed but is in the process of being developed by the industry.

Table 1 Equivalent Orientations — Dove-Tail Option

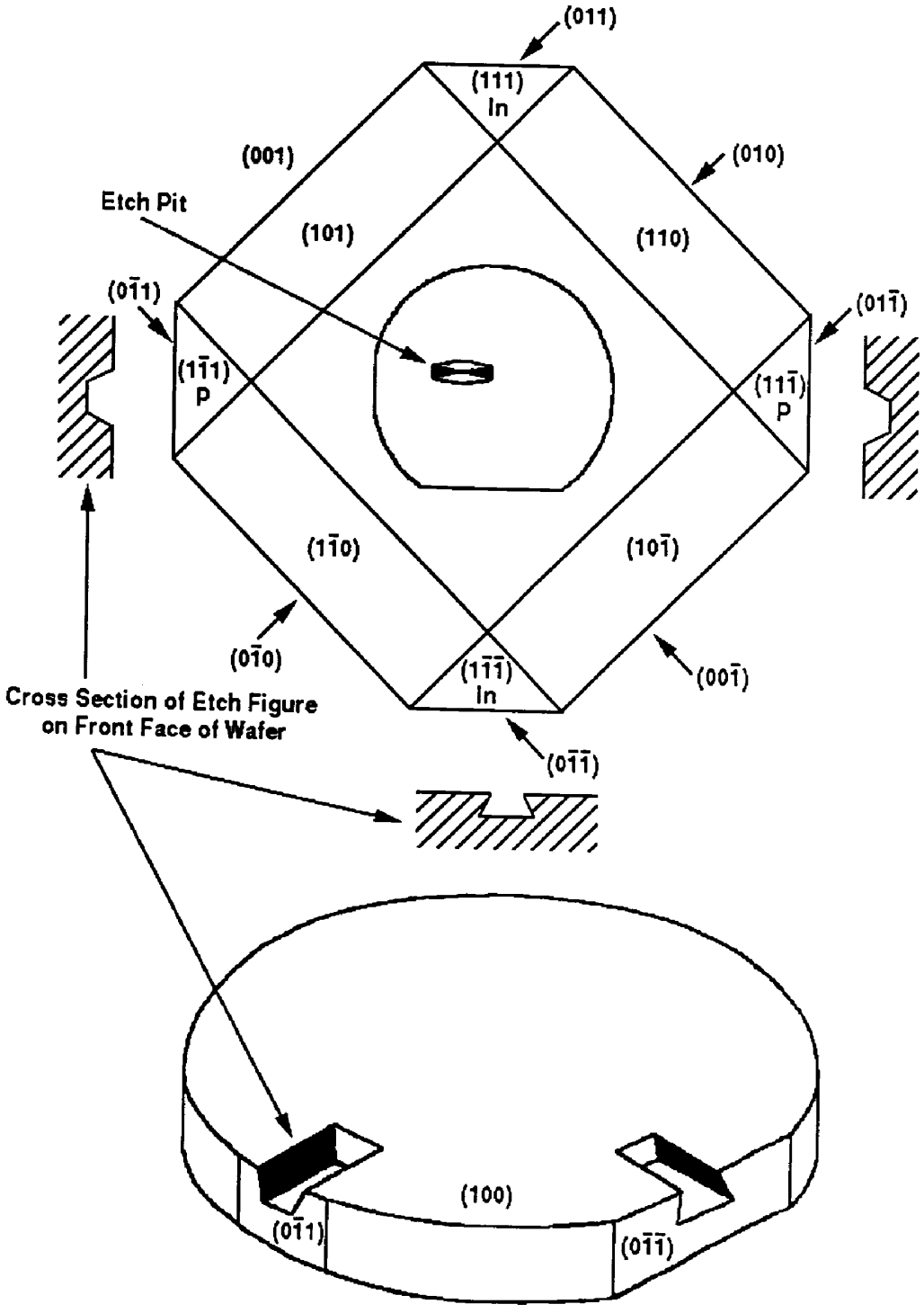
Surface orientation:	(100)	(100)	$(\bar{1}00)$	$(\bar{1}00)$
Primary flat location:	$(0\bar{1}1)$	(011)	$(0\bar{1}1)$	$(0\bar{1}1)$
Secondary flat location:	$(0\bar{1}1)$	$(0\bar{1}1)$	(011)	$(0\bar{1}1)$
For Surface orientation B, the off-orientation tilt direction is toward: (See NOTE 1)	$(\bar{1}10)$	(110)	$(\bar{1}10)$	$(\bar{1}10)$

Table 2 Equivalent Orientation — V-Groove Option

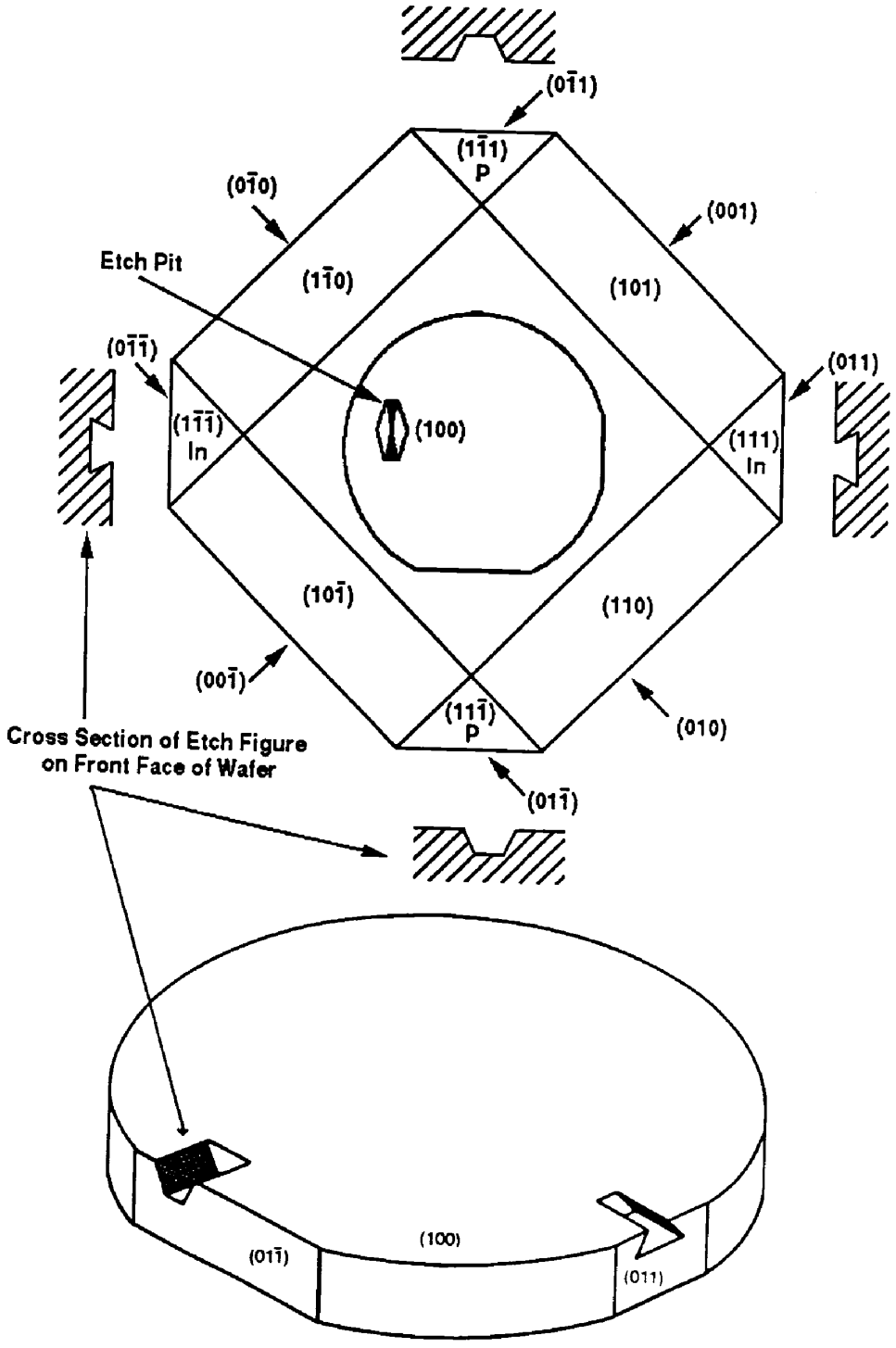
Surface orientation:	(100)	(100)	$(\bar{1}00)$	$(\bar{1}00)$
Primary flat location:	$(0\bar{1}1)$	$(0\bar{1}1)$	$(0\bar{1}1)$	(011)
Secondary flat location:	(011)	$(0\bar{1}1)$	$(0\bar{1}1)$	$(0\bar{1}1)$
For Surface orientation B, the off-orientation tilt direction is toward:	(110)	$(\bar{1}10)$	$(\bar{1}10)$	$(\bar{1}10)$

The Symmetry of InP crystal structure allows other Miller indices to be used for identifying surface and flat orientations. This table lists various possibilities that meet requirements for the above specific option.

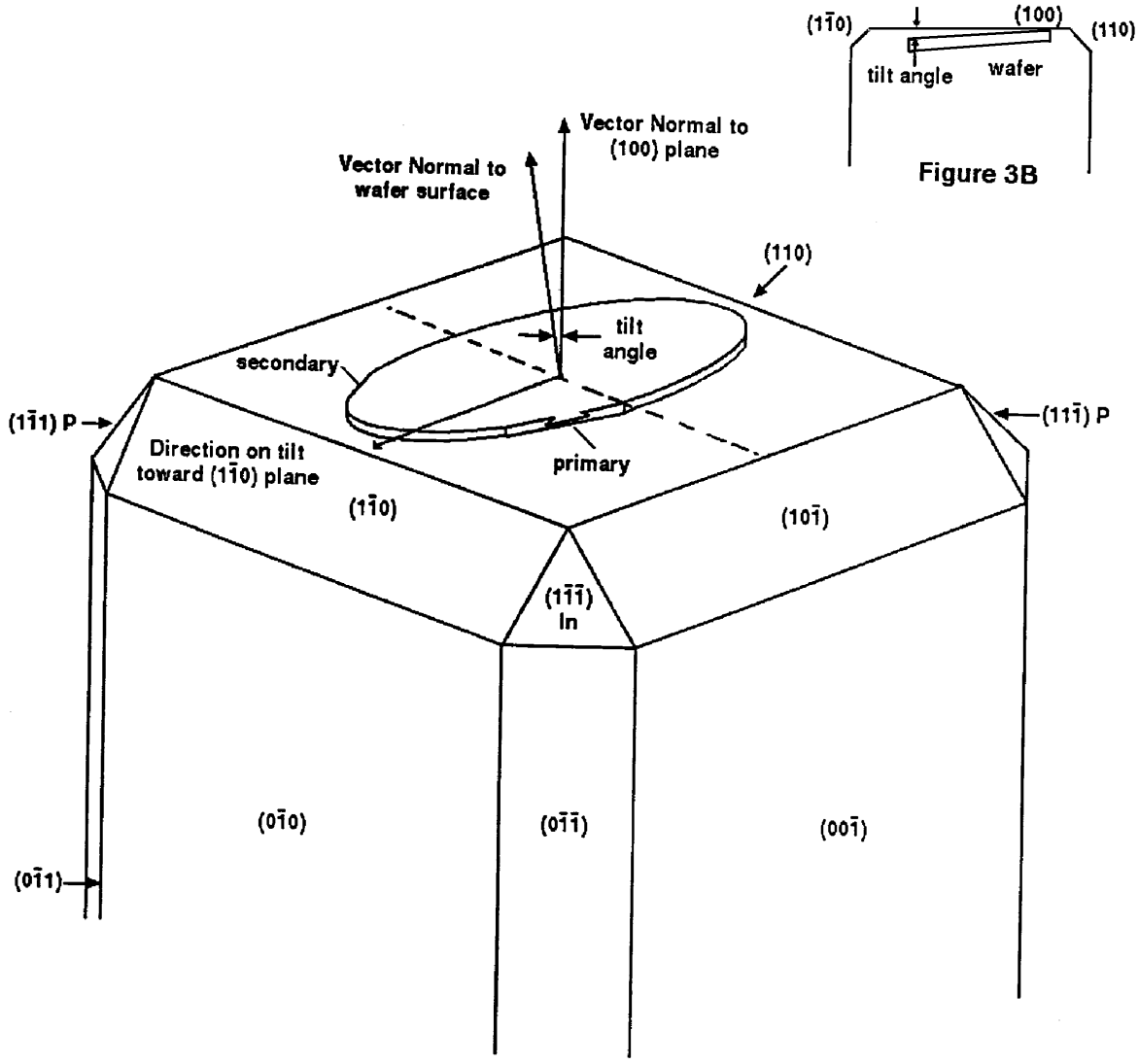
NOTE 1: For Dove-Tail Option, any of the 110 tilt directions are considered equivalent.



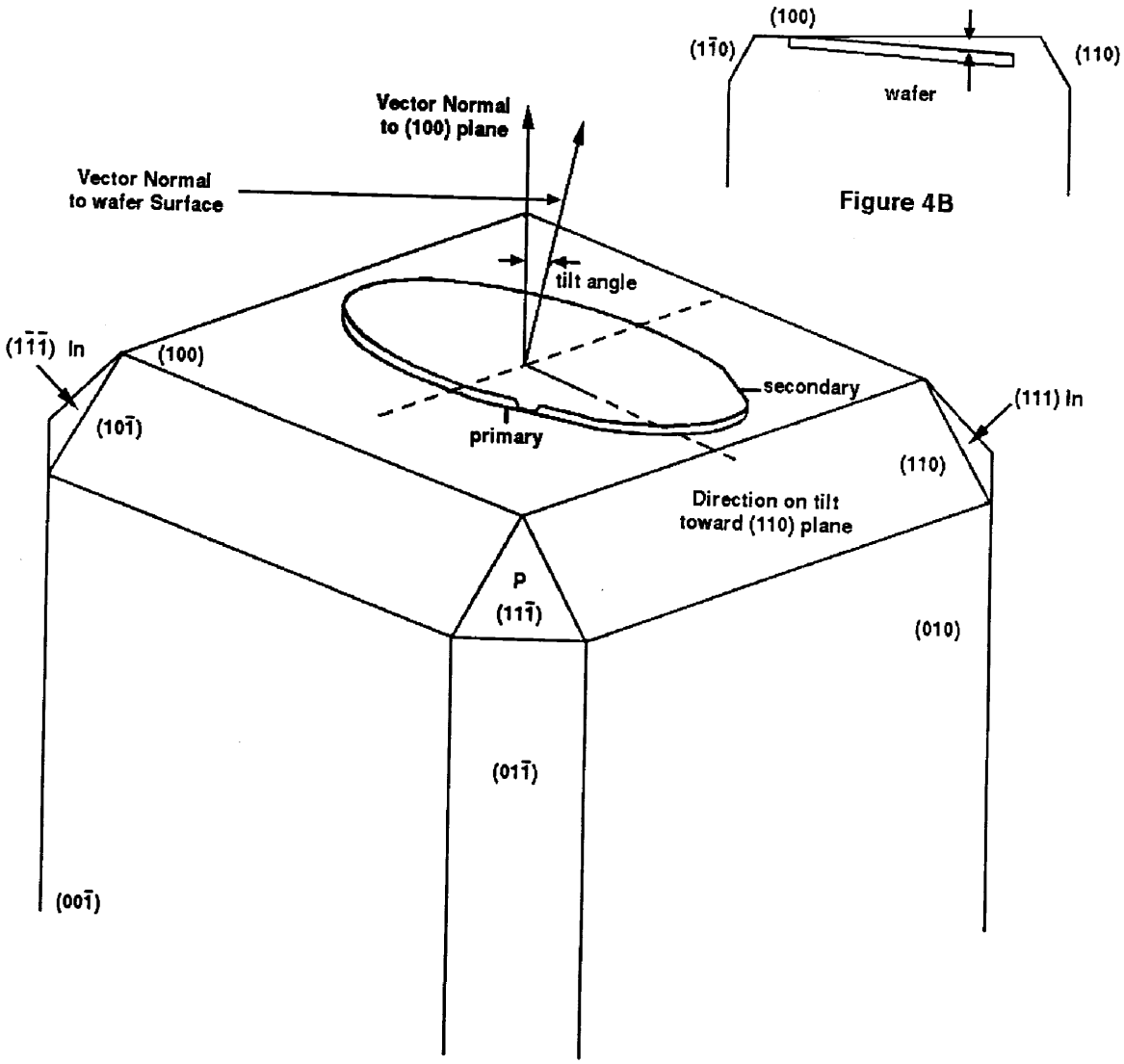
Figures 1A and 1B
Both Diagrams show an InP Wafer with Surface Orientation A and Flat Option Dove-Tail



Figures 2A and 2B
Both Diagrams show an InP Wafer with Surface Orientation A and Flat Option V-Groove



Figures 3A and 3B
Both Diagrams Show an InP Wafer with Surface Orientation B and Flat Option Dove-Tail



Figures 4A and 4B
Both Diagrams Show an InP Wafer with Surface Orientation B and Flat Option V-Groove

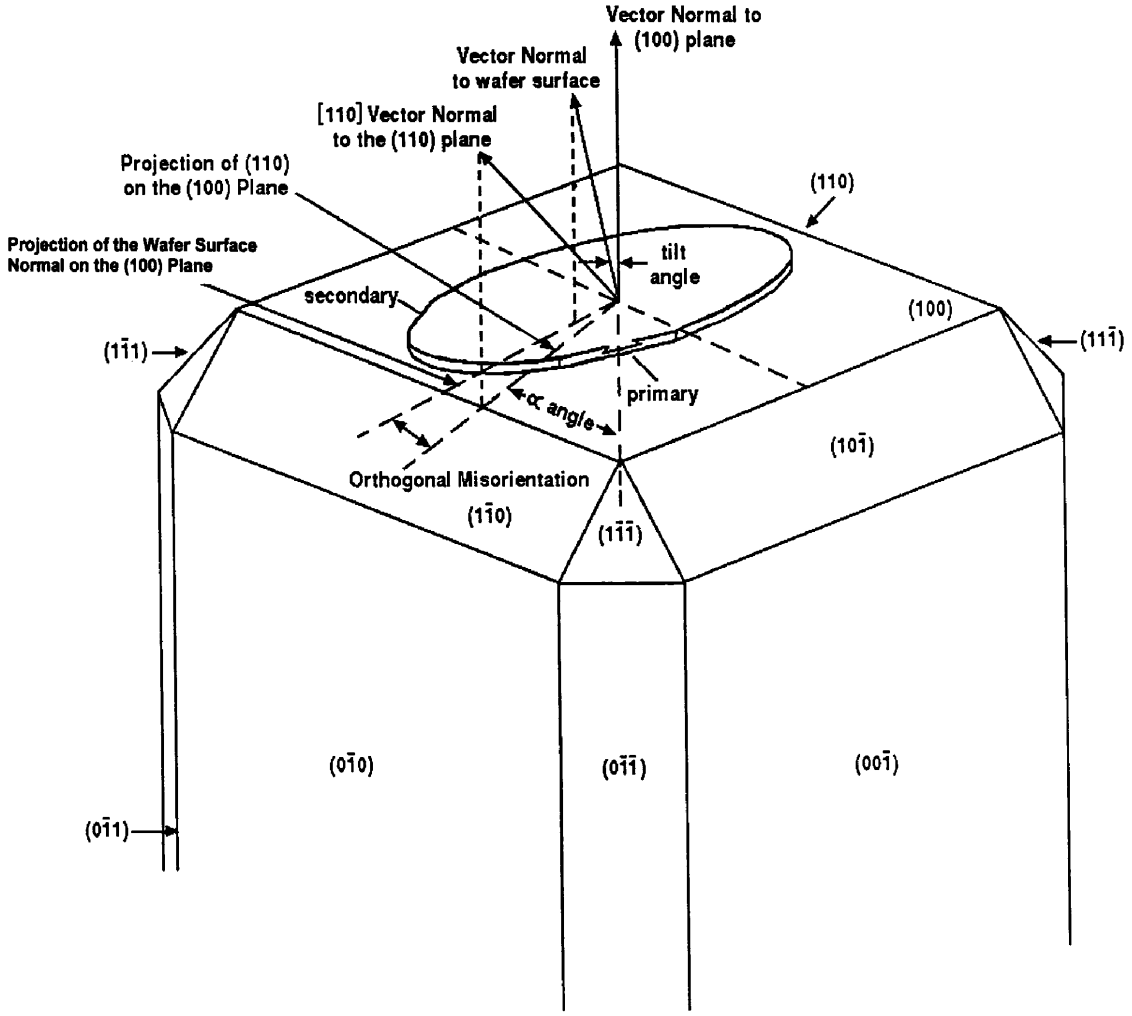


Figure 5
Diagram Shows an InP Wafer with the Same Orientation as Figure 3, but with a Few Degrees of Orthogonal Misorientation from the Intended Off-Orientation. The α angle is also shown.

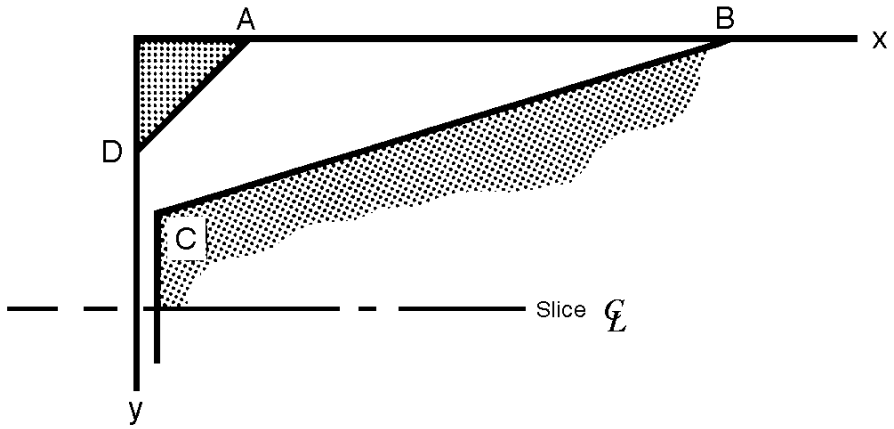


Figure 6
SEMI Wafer Edge Profile Template

Table 3 Edge Profile — Dimension and Tolerance Requirements

Property	*Dimensions*		*Units*
Edge Profile Coordinate:	x-coordinate	y-coordinate	
Point A	75	0	μm
Point B	510	0	μm
Point C	50	(See NOTE 1.)	μm
Point D	0	75	μm

NOTE 1: The y-coordinate of point C is 1/3 the nominal wafer thickness.

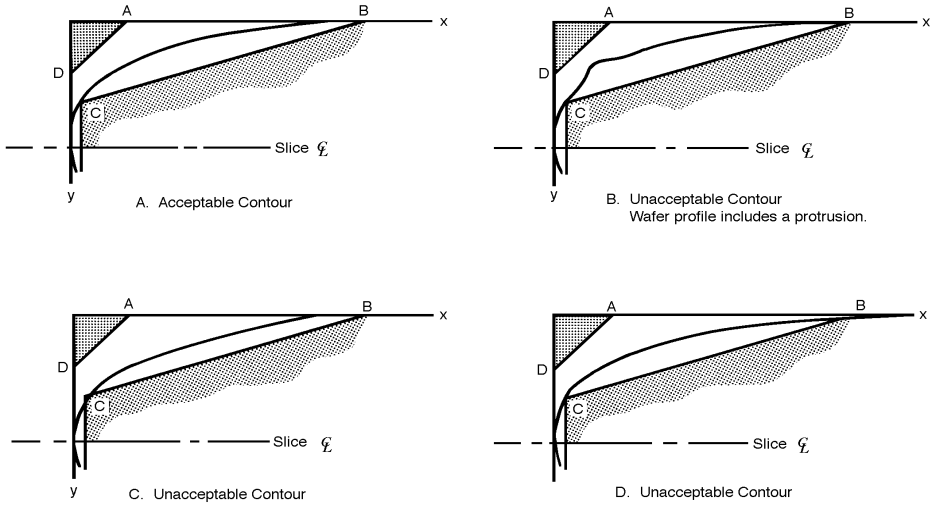


Figure 7
Example of Acceptable and Unacceptable Wafer Edge Profiles

NOTICE: SEMI makes no warranties or representations as to the suitability of the standard set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI M23.1-0600
STANDARD FOR ROUND 50 mm DIAMETER POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS

This standard was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the Japanese Compound Semiconductor Committee. Current edition approved by the Japanese Regional Standards Committee on April 28, 2000. Initially available at www.semi.org May 2000; to be published June 2000. Originally published in 1993; previously published in 1996.

The complete specification for this product includes all general requirements of SEMI M23.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*[A]
DIAMETER	50.0	± 0.5	mm
THICKNESS, CENTER POINT			
A	350	± 25	µm
B	450	± 25	µm
PRIMARY FLAT LENGTH	16	± 2	mm
SECONDARY FLAT LENGTH	8	± 2	mm
BOW	to be specified		
TOTAL THICKNESS VARIATION	to be specified		

[A]: For reference purposes, the metric (SI) units apply.

Table 2 Orientation and Flat Location Requirements

Property	*Requirement*
OPTION	Dove-Tail
PRIMARY FLAT ORIENTATION	$(0\bar{1}1)$ ± 0.5°, under an indium facet. The primary flat shall be perpendicular to the “Dove-tail” etch figure.
SECONDARY FLAT ORIENTATION	90 ± 5° clockwise from the primary flat.
SURFACE ORIENTATION	
A	{100} ± 0.5°
B	{100} off 2° ± 0.5° toward any {110} plane
ORTHOGONAL MISORIENTATION	± 5°

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SEMI M23.2-1000
STANDARD FOR ROUND 3 inch (76.2 mm) DIAMETER POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the North American Compound Semiconductor Committee. Current edition approved by the North American Regional Standards Committee on August 28, 2000. Initially available on SEMI OnLine September 2000; to be published October 2000.

NOTE: The complete specification for this product includes all requirements of SEMI M23.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units (See NOTE 1.)*
DIAMETER	76.2	± 0.5	mm
THICKNESS, CENTER POINT	600	± 25	µm
PRIMARY FLAT LENGTH	22	± 2	mm
SECONDARY FLAT LENGTH	11	± 2	mm
BOW	to be specified		
TOTAL THICKNESS VARIATION	to be specified		

NOTE 1: For reference purposes, the metric (SI) units apply.

Table 2 Orientation and Flat Location Requirements

Property	*Requirement*	
Option	*Dove-Tail*	*V-Groove*
PRIMARY FLAT ORIENTATION	$(0\bar{1}1)$ ± 0.5°, (see NOTE 1) under an indium facet. The primary flat shall be perpendicular to the "Dove-tail" etch figure. (See NOTE 2.)	$(01\bar{1})$ ± 0.5°, (see NOTE 1) under a phosphorus facet. The primary flat shall be perpendicular to the "V-Groove" etch figure. (See NOTE 2.)
SECONDARY FLAT ORIENTATION	90 ± 5° clockwise from the primary flat.	90 ± 5° counterclockwise from the primary flat.
SURFACE ORIENTATION (See NOTE 3.)		
A	{ 100} ± 0.5° (see Figure 1, SEMI M23)	{ 100} ± 0.5° (see Figure 2, SEMI M23)
B	{ 100} off 2° ± 0.5° toward any { 110} plane (see Figure 3)	{ 100} off 2° ± 0.5° toward the { 110} plane which is between the primary and secondary flats (see Figure 4)
ORTHOGONAL MISORIENTATION	± 5° (see Figure 5)	± 5° (see Figure 5)

NOTE 1: See Table 1 in SEMI M23.

NOTE 2: See Figures 1 and 2 in SEMI M23, which show the orientation of the Dovetail and V-groove figures relative to crystallographically anisotropic pits (see NOTE 4).

NOTE 3: The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted towards the (110) plane of the crystal.

NOTE 4: Relating to the etchant used for identifying V-groove and/or dovetail direction, see reference: "HBr-$K_2Cr_2O_7$ - H_2O etching system for indium phosphide" J.L.Weyher, et al. Materials Science and Engineering B28 (1994) 488-492.

NOTICE: These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI M23.3-0600
STANDARD FOR RECTANGULAR POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS

This standard was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the Japanese Compound Semiconductor Committee. Current edition approved by the Japanese Regional Standards Committee on April 28, 2000. Initially available at www.semi.org May 2000; to be published June 2000. Originally published in 1994; previously published in 1996.

The complete specification for this product includes all general requirements of SEMI M23.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*[A]
IA-1			
LONGITUDINAL SIDE LENGTH	32.6	± 0.3	mm
LATERAL SIDE LENGTH	23.1	± 0.3	mm
THICKNESS, CENTER POINT	350	± 25	µm
IA-2			
LONGITUDINAL SIDE LENGTH	23.1	± 0.3	mm
LATERAL SIDE LENGTH	16.3	± 0.3	mm
THICKNESS, CENTER POINT	350	± 25	µm
IB-1			
LONGITUDINAL SIDE LENGTH	53.0	± 0.3	mm
LATERAL SIDE LENGTH	37.5	± 0.3	mm
THICKNESS, CENTER POINT	600	± 25	µm
IB-2			
LONGITUDINAL SIDE LENGTH	37.5	± 0.3	mm
LATERAL SIDE LENGTH	26.5	± 0.3	mm
THICKNESS, CENTER POINT	600	± 25	µm

[A] For reference purposes, the metric (SI) units apply.

Table 2 Orientation and Flat Location Requirements

Property	*Requirement*
LONGITUDINAL SIDE ORIENTATION	$(0\bar{1}1)$ ± 0.5°, under a phosphorus facet.
LATERAL SIDE ORIENTATION	$(0\bar{1}\bar{1})$ ± 0.5°, under an indium facet.
SURFACE ORIENTATION	{ 100} ± 0.5°
FRONT SURFACE FINISH	Polished
BACK SURFACE FINISH	Lapped and etched
WAFER EDGE PROFILE	Cleaved face

APPENDIX 1

NOTE: The material in this appendix is an official part of SEMI M23.3 and was approved by full letter ballot procedures on April 21, 2000 by the Japanese Regional Standards Committee.

A1-1 InP is a promising material for photonic devices such as LDs, LEDs, and photodetectors for fiber communications. The consumption of InP wafers is increasing year by year due to the fiber communication systems such as LAN, ISDN, and others.

A1-2 In order to fabricate these devices, many rectangular wafers with more than 30 different sizes are industrially used but most of the sizes are not reasonably determined. From the viewpoint of material yield as explained below, the standardization of rectangular InP wafers is useful not only for InP wafer manufacturers, but also for device manufacturers.

A1-3 Figure A1-1 shows the effective area (A) as a function of ratio of longitudinal length (a) and of lateral length (b). It is a fact that the largest area can be obtained when the shape is square. However, it is difficult to distinguish V-Groove and Dove-Tail Groove orientations when the shape is square. It is, therefore, necessary to make the shape rectangular in a way that one can distinguish the orientations. It is however, noted that if the length ratio becomes too large, the effective area is dramatically decreased as seen in Figure A1-1. For instance, rectangular wafers at the point P have very little area, and most of wafer is cut off in vain. It is, therefore, very reasonable to select the length ratio at which the effective area is not largely decreased. When the length ratio (a/b ratio) is $\sqrt{2}$, the area decrease is only 5.7% as seen in Table A1-1 and Figure A1-1. It is also interesting to note that if the length ratio is determined as $\sqrt{2}$, each half of the rectangular wafer again gives a similar shape with the same ratio. In fact, this length ratio is used for paper standardization as A3/A4 or B3/B4. Rectangular wafers are therefore determined SEMI M23.3.

A1-4 Since there are already standardized 50 mm and 75 mm round wafers, the standardization is made in a way that large rectangular wafers can be obtained from these standardized wafers by removing 5 mm from the periphery as seen in Figure A1-2. Removing of 5 mm is due to EPD measurement specifications in which 5 mm periphery is excluded from the measurement.

A1-5 As explained above, it is highly recommended to use the standardized rectangular wafers because this standardization is very important in preventing proliferation of various sizes of rectangular wafers in the future.

Table A1-1

a/b Ratio	*A (mm^2)*	*A/square*
1.000	800.0	100%
1.414	754.2	94.3%
2.000	640.0	80.0%

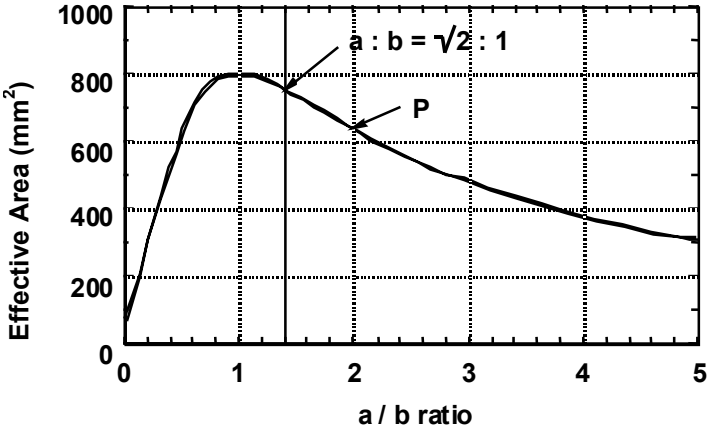

Figure A1-1
Effective Area as a Function of a/b Ratio

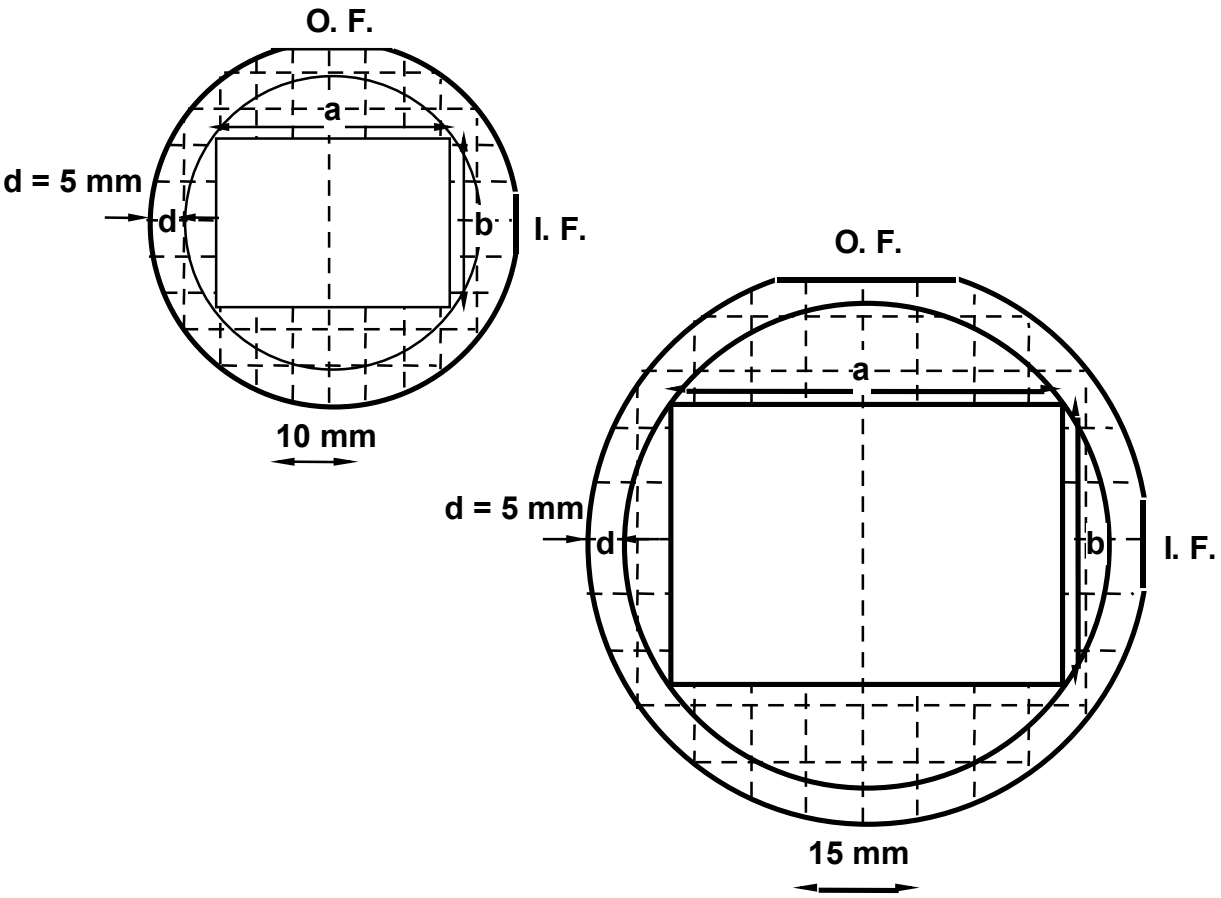

Figure A1-2
Rectangular Wafers Which can be Obtained from 50 and 75 mm Round Wafers

SEMI M23.4-0999
SPECIFICATION FOR ROUND 100 mm POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS FOR ELECTRONIC AND OPTOELECTRONIC DEVICE APPLICATIONS (DOVE-TAIL TYPE)

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the Japanese Compound Semiconductor Committee. Current edition approved by the Japanese Regional Standards Committee on June 1, 1999. Initially available at www.semi.org August 1999; to be published September 1999.

NOTE: The complete specification for this product includes all general requirements of SEMI M23.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*
DIAMETER (See NOTE 1.)	100.0	± 0.5	mm
THICKNESS, CENTER POINT	625.0	± 25	µm
PRIMARY FLAT LENGTH	32.5	± 2	mm
SECONDARY FLAT LENGTH	18.0	± 2	mm

NOTE 1: The diameter standard means that the dimension is centered to this value.

Table 2 Orientation and Flat Location Requirements

Property	*Requirement*
OPTION	Dove-Tail
PRIMARY FLAT ORIENTATION	$(0\bar{1}\bar{1})$ ± 0.5 (see Figure 1 in SEMI M23) under an indium facet. The primary flat shall be perpendicular to the "Dove-Tail" etch figure (see NOTE 1).
SECONDARY FLAT ORIENTATION	$(0\bar{1}1)$ 90° ± 5° clockwise from the primary flat.
SURFACE ORIENTATION	
A.	(100) ± 0.5° (See Figure 1 in SEMI M23.)
B.	(100) off 2° ± 0.5° toward the $(1\bar{1}0)$ plane (see NOTE 2). (See Figure 2 in SEMI M23.)
ORTHOGONAL MISORIENTATION	± 5° (See Figure 3 in SEMI M23.)

NOTE 1: Since there are various etchants, the appropriate etching method for revealing etch pits can be determined by each manufacturer. For example, see reference "HBr-$K_2Cr_2O_7$-H_2O etching system for indium phosphide" J.L. Weyher *et al.*, *Materials Science and Engineering*, B28 (1994) 488-492.

NOTE 2: The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted toward the $(1\bar{1}0)$ plane of the crystal.

SEMI M23.5-1000
SPECIFICATION FOR ROUND 100 mm POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS FOR ELECTRONIC AND OPTOELECTRONIC DEVICE APPLICATIONS (V-GROOVE OPTION)

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the North American Compound Semiconductor Committee. Current edition approved by the North American Regional Standards Committee on August 28, 2000. Initially available at www.semi.org September 2000; to be published October 2000.

NOTE: The complete specification for this product includes all requirements of SEMI M23.

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*
DIAMETER (See NOTE 1.)	100.0	± 0.5	mm
THICKNESS, CENTER POINT	625	± 25	µm
PRIMARY FLAT LENGTH	32.5	± 2	mm
SECONDARY FLAT LENGTH	18	± 2	mm

NOTE 1: The diameter standard means that the dimension is centered to this value.

Table 2 Orientation and Flat Location Requirements

Property	*Requirement*
PRIMARY FLAT ORIENTATION	$(0\bar{1}1)$ ± 0.5° (see NOTE 1) under a Phosphorus facet. The primary flat shall be perpendicular to the "V" etch figure. (See NOTE 2.)
SECONDARY FLAT ORIENTATION	(011), 90°± 5° counterclockwise from the primary flat.
SURFACE ORIENTATION (See NOTE 3.)	
A.	{ 100} (see NOTE 1) ± 0.5° (See Figure 2 in SEMI M23.)
B.	{ 100} (see NOTE 1) off 2° ± 0.5° toward the (110) plane which is between the primary and secondary flats (See Figure 4 in SEMI M23.)
ORTHOGONAL MISORIENTATION	± 5° (See Figure 5 in SEMI M23.)

NOTE 1: See Table 1 in SEMI M23.

NOTE 2: See Figure 2 in SEMI M23, which shows the orientation of the V-groove figure relative to crystallographically anisotropic pits (see NOTE 4).

NOTE 3: The frame of reference is the (100) plane of the crystal. It is the wafer normal that is tilted toward the (110) plane of the crystal.

NOTE 4: Relating to the etchant used for identifying V-groove and/or dovetail direction, see reference: "HBr-$K_2Cr_2O_7$ - H_2O etching system for indium phosphide" J.L.Weyher, et al. Materials Science and Engineering B28 (1994) 488–492.

SEMI M23.6-0703
SPECIFICATION FOR ROUND 150 mm POLISHED MONOCRYSTALLINE INDIUM PHOSPHIDE WAFERS (NOTCHED)

This specification was technically approved by the Global Compound Semiconductor Materials Committee and is the direct responsibility of the Japanese Compound Semiconductor Materials Committee. Current edition approved by the Japanese Regional Standards Committee on April 28, 2003. Initially available at www.semi.org June 2003; to be published July 2003.

1 Purpose

1.1 This specification defines properties of 150 mm monocrystalline InP substrates, in agreement with presently established industry practice. It uniquely defines those mechanical parameters that do not need, for technical reasons, a choice of different values.

2 Scope

2.1 The parameters defined include the values and tolerances of wafer diameter, thickness and surface orientation. The position and depth of the notch and laser marking are also specified.

2.2 The complete specification of this product includes the requirements of SEMI M23, excluding those that are not relevant to this specification (e.g., flat positions).

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

None.

5 Physical Requirements

Table 1 Physical Requirements

Property	*Specification*	*Tolerance*	*Unit*	*Reference*
WAFER				
Diameter	150.0	± 0.5	mm	
Thickness, center point	675	± 25	µ m	
Surface orientation A	(100)	0.5 max.	degrees	Figure 2
Surface orientation B				
Tilt	2 off (100) towards (110)	± 0.5	degrees	Figure 3
Orthogonal misorientation	0	± 5 max.	degrees	Figure 4
NOTCH				
Orientation	[010]	± 2	degrees	Figure 1
Depth	1.00	+ 0.25, -0.00	mm	Figure 5
Opening angle	90	+ 5, -1	degrees	Figure 5
LASER MARKING				
Surface	front side			
Position	adjacent to notch			Figure 6
Mandatory content	check characters			SEMI M12

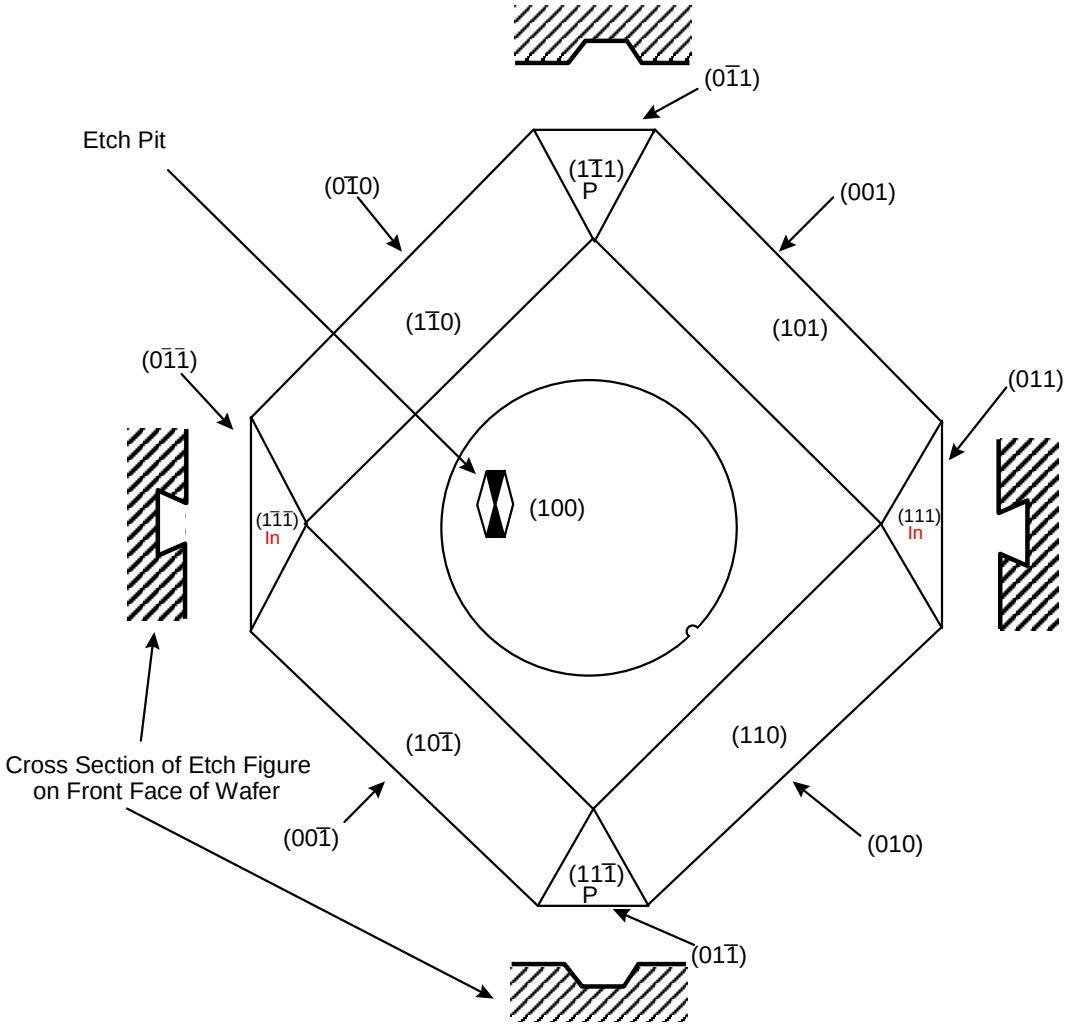

Figure 1
Diagram Shows a InP Wafer with Notch

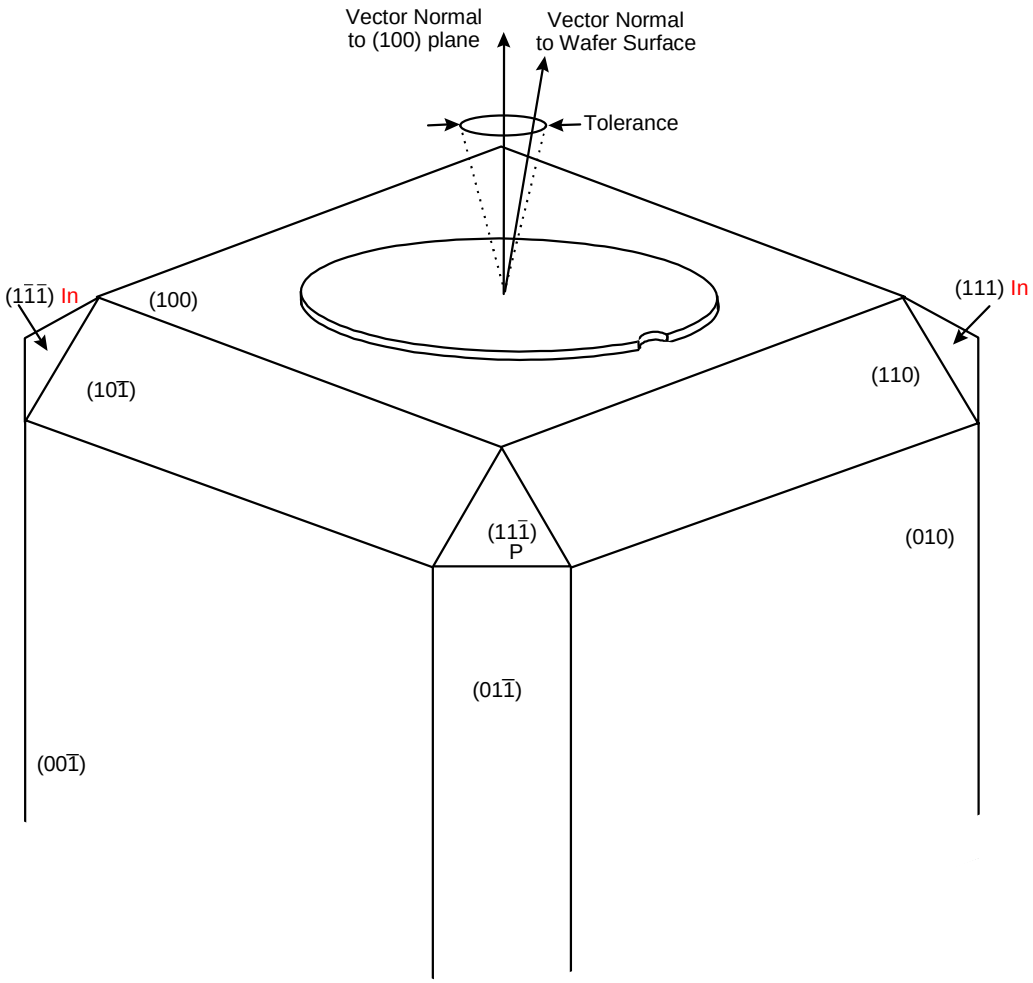

Figure 2
Notched InP Wafer Illustrating Surface Orientation A

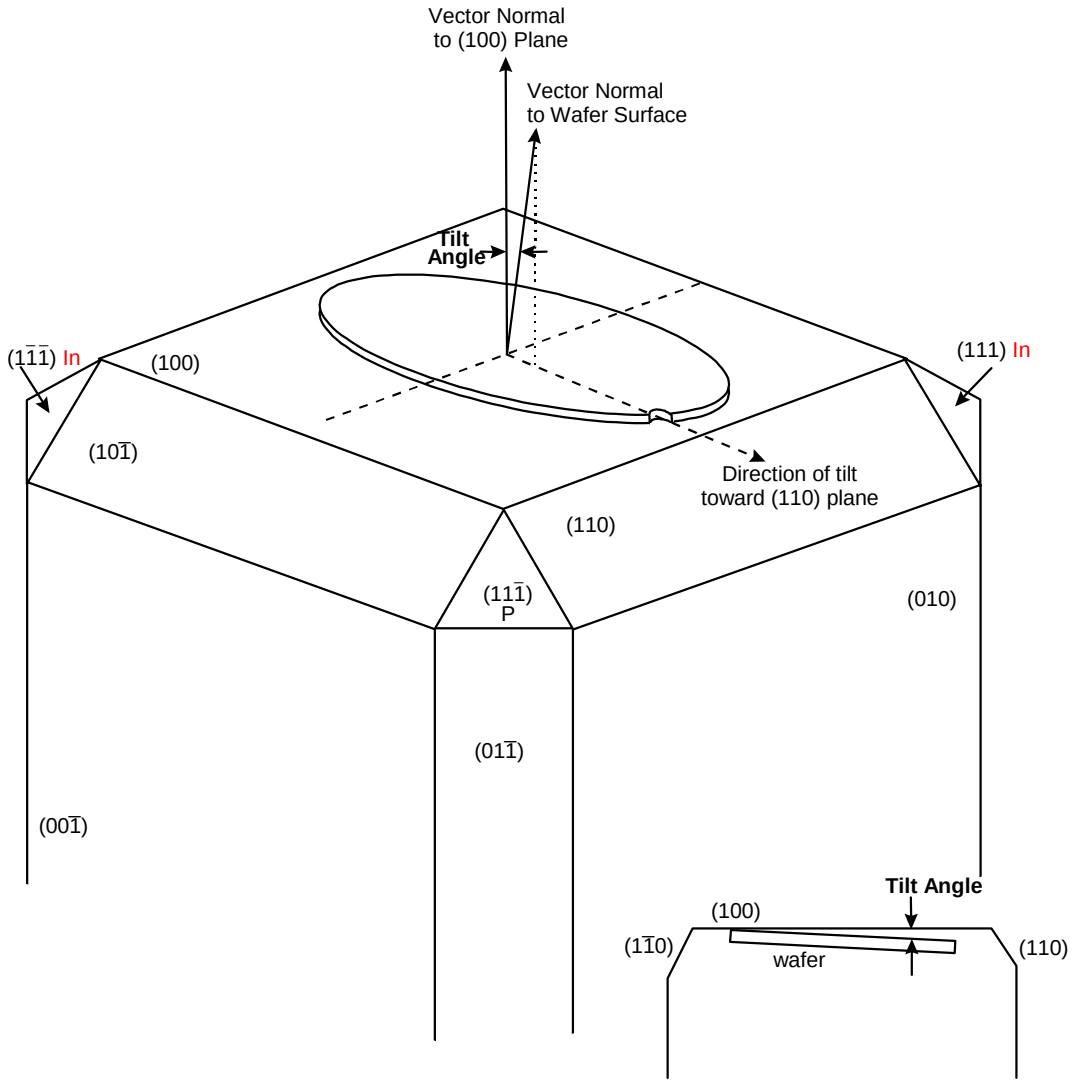

Figure 3
Notched InP Wafer Illustrating Surface Orientation B, with Tilt

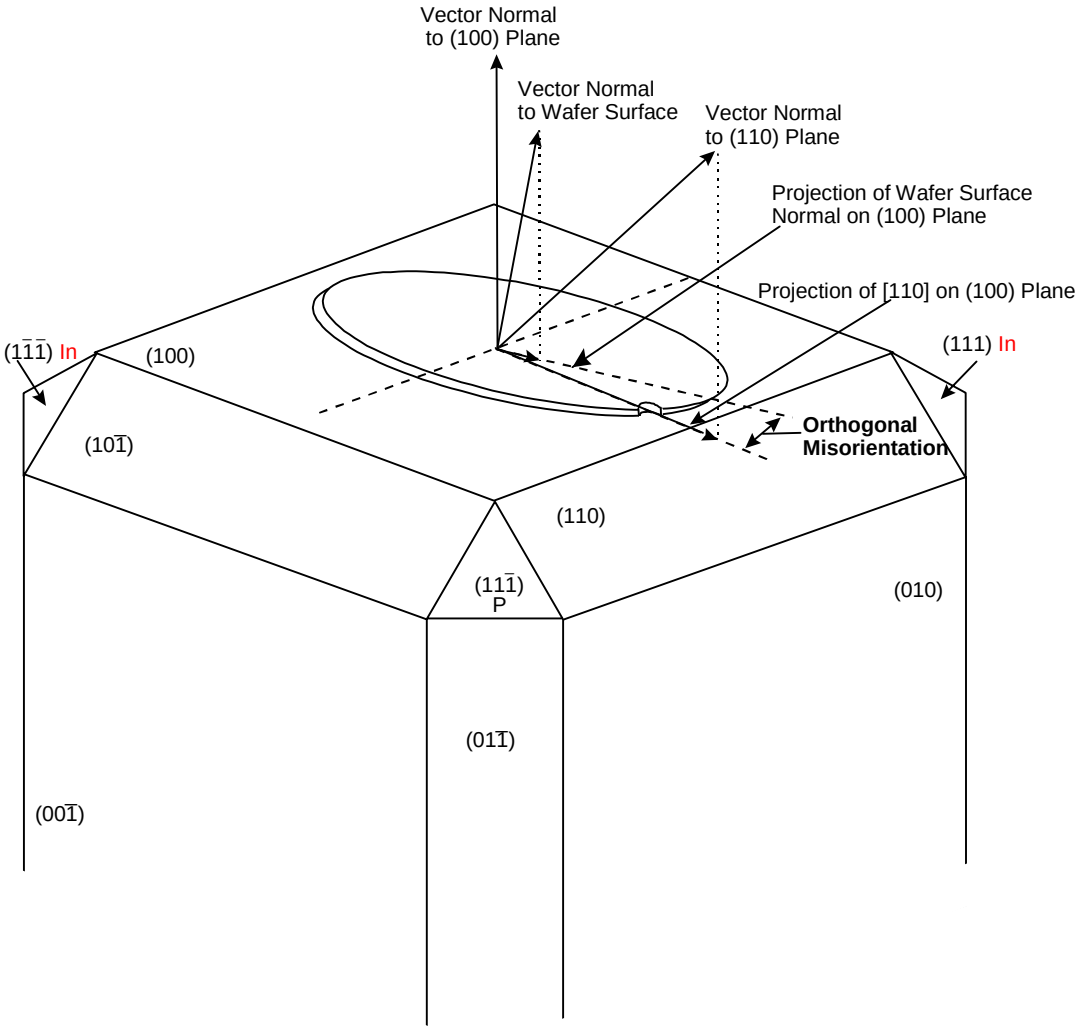

Figure 4
Notched InP Wafer Illustrating Surface Orientation B, with Tilt and Orthogonal Misorientation

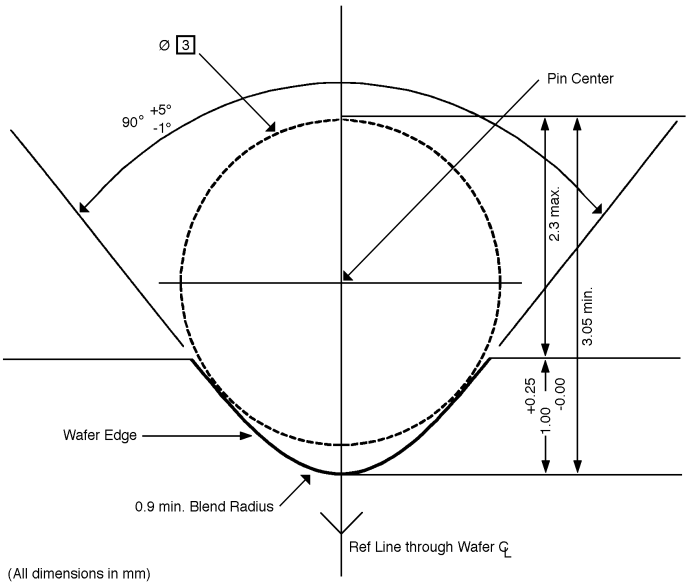

Figure 5
Notch Dimensions

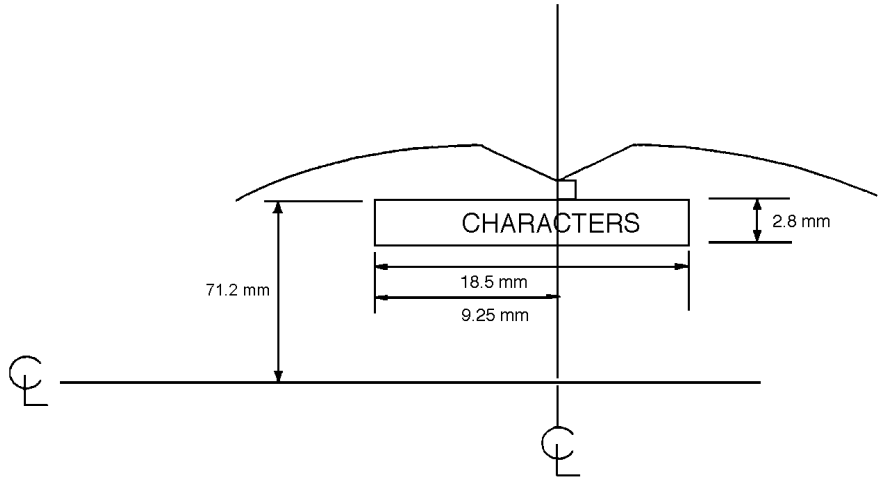

Figure 6
Character Window Location

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SEMI M24-1103
SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON PREMIUM WAFERS

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved by the Japanese Regional Standards Committee on August 8, 2003. Initially available at www.semi.org October 2003; published November 2003. Originally published in 1994; previously published November 2001.

1 Purpose

1.1 This document specifies requirements for virgin silicon premium wafers with nominal diameter from 150 mm to 300 mm used for particle counting, metal contamination monitoring, and measuring pattern resolution in the photolithography process in semiconductor manufacturing. The premium wafer has tighter specification values in some specific items for the specific usage, and looser or equal specification values in other items than a prime wafer has.

2 Scope

2.1 This specification classifies premium wafers according to surface condition and dimensional tolerances. Premium wafer classifications are summarized in Table 1.

2.2 Specification values are determined by the use for which the wafers are intended.

2.3 This specification provides premium wafers that can be used to test and evaluate leading edge device process.

2.4 For referee purposes, SI (System International) units shall be used.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M20 — Specification for Establishing a Wafer Coordinate System

SEMI M25 — Specification for Silicon Wafers for Calibration of Light Point Defect Wafer Inspection Systems with Respect to the Diameter of Polystyrene Latex Spheres

3.2 *ANSI Standard*[1]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.3 *ASTM Standards*[2]

D 523 — Standard Test Method for Specular Gloss

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

F 26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

F 42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

F 84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Probe Array

F 154 — Standard Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

F 391 — Standard Test Methods for Minority-Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

F 523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surface

F 533 — Standard Test Method for Thickness and Thickness of Variation of Silicon Wafers

F 534 — Standard Test Method for Bow of Silicon Wafers

F 613 — Standard Test Method for Measuring Diameter of Semiconductor Wafers

1 American National Standards Institute, Headquarters: 1819 L Street, NW, Washington, DC 20036, USA. Telephone: 202.293.8020; Fax: 202.293.9287, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023, Website: www.ansi.org

2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555, Website: www.astm.org

F 657 — Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

F 671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Material

F 673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

F 847 — Standard Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

F 928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

F 978 — Standard Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques

F 1049 — Standard Practice for Shallow Pit Detection on Silicon Wafers

F 1152 — Standard Test Method for Dimensions of Notches on Silicon Wafers

F 1188 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

F 1239 — Standard Test Methods for Oxygen Precipitation Characterization of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

F 1241 — Standard Terminology of Silicon Technology

F 1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

F 1391 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

F 1451 — Standard Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning

F 1526 — Standard Test Method for Measuring Surface Metal Contamination on Silicon Wafers by Total Reflection X-ray Fluorescence Spectroscopy

F 1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

F 1535 — Standard Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

F 1617 — Standard Test Method for Measuring Surface Sodium, Aluminum, and Potassium on Silicon and EPI Substrates by Secondary Ion Mass Spectroscopy

F 1619 — Standard Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle

F 1620 — Standard Practice for Calibrating a Scanning Surface Inspection System Using Monodisperse Polystyrene Latex Spheres Deposited on Polished or Epitaxial Surfaces

F 1621 — Standard Practice for Determining Positional Accuracy Capabilities of a Scanning Surface Inspection System

F 1725 — Guide for Analysis of Crystallographic Perfection of Silicon Ingots

F 1726 — Guide for Analysis of Crystallographic Perfection of Silicon Wafers

3.4 *DIN Standards*[3]

50431 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current Method with Colinear Four-Probe Array

50432 — Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot-Probe

50433/1 — Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction

50433/2 — Determination of the Orientation of Single Crystals by Means of Optical Reflection Figure

50433/3 — Determination of the Orientation of Single Crystals by Means of Laue Back Scattering

50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

50435 — Determination of the Radial Resistivity Variation of Silicon or Germanium Slices by Means of a Four-Point-DC-Probe

50438/1 — Determination of Impurity Content in Silicon by Infrared Absorption: Oxygen

50438/2 — Determination of Impurity Content in Silicon by Infrared Absorption: Carbon

50438/3 — Determination of Impurity Content in Silicon by Infrared Absorption: Boron and Phosphorus

3 Deutsches Institut für Normung e.V., Available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, Website: www.din.de

50441/1 — Determination of the Geometric Dimensions of Semiconductor Slices: Measurement of Thickness

50441/2 — Determination of the Geometric Dimensions of Semiconductor Slices: Testing of Edge Rounding

50441/4 — Determination of the Geometrical Dimensions of Semiconductor Slices: Diameter and Flat Depth of Slices

50443/1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-Ray Topography: Silicon

50445 — Contactless Determination of the Electrical Resistivity of Semiconductor Wafers with the Eddy Current Method

3.5 *JEITA Standards*[4]

JEIDA 18 — Determining the Orientation of a Semiconductor Silicon Single Crystal

JEIDA 27 — Standard Specification for Dimensional Properties of Silicon Wafers with Specular Surface

JEIDA 43 — Terminology of Silicon Wafer Flatness

JEIDA 53 — Test Method for Recombination Lifetime in Silicon Wafers by Measurement of Photoconductivity Decay by Microwave Reflectance

JEIDA 56 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

JEIDA 61 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

3.6 *JIS Standards*[5]

H 0602 — Testing Method of Resistivity for Silicon Crystals and Silicon Wafers with Four-Point Probe

H 0607 — Testing Methods for Conductivity Type of Semiconductor Materials

H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

H 0611 — Methods of Measurement of Thickness, Taper, and Bow of Silicon Wafers

H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

Z8741 — Method of Measurement for Specular Glossiness

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Definitions of terms related to silicon wafer technology are given in ASTM Terminology F 1241.

4.2 Definitions for some additional terms are given in SEMI M1.

4.3 The following definitions apply in the context of this specification:

4.4 *Definitions*

4.4.1 *furnace and thermal processes* — wafers intended for use in evaluating metal contamination in thermal process.

4.4.2 *hand scribe mark* — any marking, usually on the back surface of a wafer, scratched manually into the silicon surface, as with a diamond-tipped scribe, for purposes of wafer identification.

4.4.3 *lithography and patterning* — wafers intended for use in evaluating pattern resolution.

4.4.4 *particle counting* — wafers intended for use in evaluating the particulate contamination added by a process tool. LLSs (Localized Light Scatterers) include particles and COP (Crystal Originated Pits).

4.4.5 *premium wafer* — a silicon wafer suitable for particle counting, metal contamination monitoring, and measuring pattern resolution in the photolithography process. The premium wafer has tighter specification values in some specific items for the specific usage, and looser or equal specification values for other items than a prime wafer has.

5 Ordering Information

5.1 Purchase orders for silicon premium wafers furnished to this specification shall include the items from the appropriate specification groups listed in Table 1.

Table 1 Wafer Classifications

Classification	*Application*
Particle Counting	Particle counting
Furnace and Thermal Process	Metal contamination monitoring
Lithography and Patterning	Measurement of pattern resolution in photolithography

4 Japanese Electronic and Information Technology Industries Association, Tokyo Chamber of Commerce and Industry Bldg. 2-2, Marunouchi 3-chome, Chiyoda-ku, Tokyo 100-0005, Japan., Website: www.jeita.or.jp

5 Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014, Website: www.jsa.or.jp