Table 4 Silicon-on-Insulator (SOI) Specifications for Medium Voltage (150–250V) Power Device

Parameters (Units)	*Value*	*ASTM Test Method or Measurement Procedure*	*Acceptance*
Wafer(Overall)			
Diameter (mm)	125, 150, 200	F613-93	Note A
Thickness (μm)	(Value of regular silicon wafer) + (SOI thickness) + (Box thickness)	F533-96, F1530-94	Note A
Total Thickness Variation (μm)	Note C	F1530-94	Note C
LTV (μm)	Note C	F1530-94	Note C
Warp (μm)	≤ 100 (Note B, C, G)	F1390-92	Note C, or Certified by Wafer Manufactures
Non-SOI Edge Area (mm)	≤ 3 (Note C)	Optical Metrology	Note C, or Certified by Wafer Manufactures
Edge Profile/Edge Profile Surface Finish	Note C	F928-93	Note C, or Certified by Wafer Manufactures
Top Silicon Film			
Thickness (μm)	2–10	Note D (F399-88)	Note C, E, Must be measured on each wafer
Surface Orientation	Note C	X-ray Diffraction (F26-87a)	Note C, or Certified by Wafer Manufactures
Resistivity (ohm-cm)	Note C	F43-93, F84-93, F1527-94	Note C, or Certified by Wafer Manufactures
Conductivity Type	Note C	F42-93	Note C, or Certified by Wafer Manufactures
Oxygen Concentration (/cm^3)	Note C	F1188-93a, F1619-95	Note C, or Certified by Wafer Manufactures
Carbon Concentration (/cm^3)	Note C	F1391-93	Note C, or Certified by Wafer Manufactures
Surface Cleanliness: Metal Contamination (/cm^2)	Note A, C	AAS, ICP-MS, TXRF (F1526-95), SIMS (F1617-98)	Note A, C
Surface Cleanliness: Particle Density (/wafer)	Note A, C	Light Scattering Tomography (F1620-96) (SEMI M34)	Note A, C
Surface Roughness (nm)	Note A, C	AFM (SEMI M34)	Note A, C
Carrier Lifetime (μsec)	Note C	μ-PCD Method (F1535-94)	Note C
Crystalline Alignment of Top Silicon Film to Base Wafer(°)	Note C	X-ray Diffraction (F847-94)	Note C
Surface Feature (Haze, Scratch, etc)	None	F154-94, F523-93, F1726-97	Must be measured on each wafer
OSF Density (/cm^2)	Note C	Optical Metrology (F1727-97)	Note C, or Certified by Wafer Manufactures
Buried Oxide (BOX)			
Thickness (μm)	0.5–3	Ellipsometry (F576-95) or Reflective Spectroscopy (SEMI M34)	Tolerance is ± 5%; Note C, or Certified by Wafer Manufactures

Parameters (Units)	*Value*	*ASTM Test Method or Measurement Procedure*	*Acceptance*
Location of Bonded Interface	Lower Surface, or Inside Oxide	TEM	Certified by Wafer Manufactures
Void Density (/cm^2)	None	Scanning Acoustic Tomography, Optical Defect Inspection	Note C
Oxide Defect Density (/cm^2)	Note C	I-V on Capacitor, Cu Decoration (SEMI M34)	Note C
Dielectric Breakdown Voltage (V)	Note C	I-V on Capacitor	Note C
Interface States (/cm^2)	Note C, H	C-V Technique	Note C
Fixed Charge Density (/cm^2)	Note C, H	C-V Technique (F1153-92)	Note C
Bonding Strength (kg/cm^2)	Note C	Tensile Strength	Note C, or Certified by Wafer Manufactures
Base Silicon Wafer			
Surface Orientation	Note C	F26-87a	Note C
Resistivity (ohm-cm)	Note C	F43-93, F84-93, F1527-94	Note C
Conductivity Type	Note C	F42-93	Note C
Fiducial Axis Orientation (Flat/Notch)	Note C	F671-90, F1152-93	Note C
To-be-bonded Surface Cleanliness: Metals (/cm^2)	Note C	AAS, ICP-MS, TXRF (F1526-95), SIMS (F1617-98)	Note C
Back Surface Finish	Note C	Optical Metrology	Note C

Table 5 Silicon-on-Insulator (SOI) Specifications for High Voltage (500–600V) Power Device

Parameters (Units)	*Value*	*ASTM Test Method or Measurement Procedure*	*Acceptance*
Wafer(Overall)			
Diameter (mm)	125, 150, 200	F613-93	Note A
Thickness (μm)	(Value of regular silicon wafer) + (SOI thickness) + (Box thickness)	F533-96, F1530-94	Note A
Total Thickness Variation (μm)	Note C	F1530-94	Note C
LTV (μm)	Note C	F1530-94	Note C
Warp (μm)	≤ 100 (Note B,C,G)	F1390-92	Note C, or Certified by Wafer Manufactures
Non-SOI Edge Area (mm)	≤ 3 (Note C)	Optical Metrology	Note C, or Certified by Wafer Manufactures
Edge Profile / Edge Profile Surface Finish	Note C	F928-93	Note C, or Certified by Wafer Manufactures
Top Silicon Film			
Thickness (μm)	3–17	Note D (F399-88)	Note C, E, Must be measured on each wafer
Surface Orientation	Note C	X-ray Diffraction (F26-87a)	Note C, or Certified by Wafer Manufactures

Parameters (Units)	*Value*	*ASTM Test Method or Measurement Procedure*	*Acceptance*
Resistivity (ohm-cm)	Note C	F43-93, F84-93, F1527-94	Note C, or Certified by Wafer Manufactures
Conductivity Type	Note C	F42-93	Note C, or Certified by Wafer Manufactures
Oxygen Concentration (/cm^3)	Note C	F1188-93a, F1619-95	Note C, or Certified by Wafer Manufactures
Carbon Concentration (/cm^3)	Note C	F1391-93	Note C, or Certified by Wafer Manufactures
Surface Cleanliness: Metal Contamination (/cm^2)	Note A, C	AAS, ICP-MS, TXRF (F1526-95), SIMS (F1617-98)	Note A, C
Surface Cleanliness: Particle Density (/wafer)	Note A, C	Light Scattering Tomography (F1620-96) (SEMI M34)	Note A, C
Surface Roughness (nm)	Note A, C	AFM (SEMI M34)	Note A, C
Carrier Lifetime (μsec)	Note C	μ-PCD Method (F1535-94)	Note C
Crystalline Alignment of Top Silicon Film to Base Wafer (^{o})	Note C	X-ray Diffraction (F847-94)	Note C
Surface Feature (Haze, Scratch, etc)	None	F154-94, F523-93, F1726-97	Must be measured on each wafer
OSF Density (/cm^2)	Note C	Optical Metrology (F1727-97)	Note C, or Certified by Wafer Manufactures
Buried Oxide (BOX)			
Thickness (μm)	3–5	Ellipsometry (F576-95) or Reflective Spectroscopy (SEMI M34)	Tolerance is ± 5%; Note C, or Certified by Wafer Manufactures
Location of Bonded Interface	Inside Oxide (Lower Surface)	TEM	Certified by Wafer Manufactures
Void Density (/cm^2)	None	Scanning Acoustic Tomography, Optical Defect Inspection	Note C
Oxide Defect Density (/cm^2)	Note C	I-V on Capacitor, Cu Decoration (SEMI M34)	Note C
Dielectric Breakdown Voltage (V)	Note C	I-V on Capacitor	Note C
Interface States (/cm^2)	Note C, H	C–V Technique	Note C
Fixed Charge Density (/cm^2)	Note C, H	C–V Technique (F1153-92)	Note C
Bonding Strength (kg/cm^2)	Note C	Tensile Strength	Note C, or Certified by Wafer Manufactures
Base Silicon Wafer			
Surface Orientation	Note C	F26-87a	Note C
Resistivity (ohm-cm)	Note C	F43-93, F84-93, F1527-94	Note C
Conductivity Type	Note C	F42-93	Note C
Fiducial Axis Orientation (Flat/Notch)	Note C	F671-90, F1152-93	Note C

Parameters (Units)	*Value*	*ASTM Test Method or Measurement Procedure*	*Acceptance*
To-be-bonded Surface Cleanliness: Metals (/cm^2)	Note C	AAS, ICP-MS, TXRF (F1526-95), SIMS (F1617-98)	Note C
Back Surface Finish	Note C	Optical Metrology	Note C

Note A: Same as the standard of regular silicon wafer
Note B: The value is of 150 mm wafers, and is determined according to wafer diameter.
Note C: To be determined by negotiation between wafer users and suppliers
Note D: Reflective spectroscopy or FT-IR is recommended for top silicon film of less than several μm (about 7 μm), and FT-IR for top silicon film of more than several μm (about 7 μm).
Note E: Tolerance of ± 0.5 μm is recommended for top silicon film of less than several μm (about 7 μm), and ± 1.0 μm for top silicon film of more than several μm (about 7 μm).
Note F: The value is without the compensation method by backside oxide.
Note G: The value is with the compensation method by backside oxide.
Note H: This item can be neglected if the bonding interface is between BOX and base wafer.

7 Sampling Plan

7.1 Unless otherwise specified, ASTM Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) of lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contact or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the users and the suppliers.

8 Test Methods - Dimensions

NOTE 3: Detailed test procedures of each item should be determined between the users and the suppliers.

8.1 *Thickness of Top Silicon Film* — The following two methods are available for thickness measurement.

8.1.1 *Reflective Spectroscopy* — The light of visual wavelength (400–800 nm) is introduced into top silicon film by varying its wavelength continuously, and then the reflective spectra is measured. When the light is introduced into multi-layers of SOI wafers, reflection occurs on the surface of top silicon film and the front and backside of BOX. In such a case, the phase varies. The final intensities of the light that reflects from top silicon film surface are the sum of the intensity of light that reflects from each layer. The thickness of top silicon film and BOX makes optical path difference and then results in phase difference that is dependent on its wave length. The reflective light intensities, depending on its wavelength, are measured. The reflective spectra are defined as the ratio of reflective light intensity to incident intensity. This spectra curve varies by the thickness of top silicon film and BOX. The top silicon film thickness is derived from the obtained spectra curve by approximate calculation based on simulation or by comparing with the database.

8.1.1.1 Reference: J.-P. Colinge, "Silicon-On-Insulator Technology", Kluwer Academic Publisher, 1991.

NOTE 4: Thickness of top silicon film and BOX layer are limited to measure because of using visual light.

Example: Nanospec/AFT model : 210LCW, SP-FSC15

Top silicon film thickness: 0.01–15 μm

BOX thickness: 0.004–3 μm

NOTE 5: Optical constant is already known in each of multilayers, and it should be constant in the whole layer.

8.1.2 *FT-IR (Fourier Transform Infra-Red Spectrometry)* — The reflectance spectrum of the specimen, which exhibits successive maxima and minima characteristics of optical interference phenomena, is measured as a function of wavelength using an infrared spectrophotometer. These maxima and minima are observed when the optical path lengths of the infrared beam, reflected from both the top silicon film surface and the top silicon film–buried oxide interface, differ by an integral number of half wavelengths. Consequently, the thickness of top silicon film is calculated using the wavelength of the extreme maximum and minimum in reflectance spectrum, the refractive index of Silicon and Silicon dioxide, and the angle of incidence of the infrared beam upon the SOI wafer.

Reference: F95 – Standard Test Method for Thickness of Lightly Doped Silicon Epitaxial Layers on Heavily Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer

8.1.3 *Definition of top silicon film thickness tolerance* — Thickness tolerance is defined below.

8.1.3.1 After top silicon film thickness is measured at predetermined number of points within an SOI wafer, the maximum and the minimum values are chosen, and then the tolerance is defined as;

Tolerance = Maximum value – Minimum value

NOTE 6: The location and numbers of measuring points should be determined between users and suppliers.

8.1.3.2 In case of multi-points measurements (ex. a few hundreds) within an SOI wafer, the tolerance is defined as;

Tolerance = 3σ (3 times of the standard deviation)

8.1.3.3 Measurement exclusion area such as wafer edge should be determined between users and suppliers.

NOTE 7: Recommendable metrology

a) Reflective spectroscopy or FT-IR is recommended

- for top silicon film of less than several μm (about 7 μm),
- and FT-IR for top silicon film of more than several μm (about 7 μm)

b) Tolerance is defined as the difference between the maximum and the minimum value after measuring several (ex. 9) points.

c) It is not necessary to measure the BOX thickness of SOI wafer after bonding. It is OK to measure it before wafer bonding.

d) In case of the above 1) ~ 3), the number of measurement points and their location should be specified in case of several points measuring, and the measurement exclusion area should be specified in case of multi-points measuring.

8.2 *Crystal Defect of Top Silicon Film*

8.2.1 *OSF (Oxidation induced Stacking Fault)* — This technique is applicable to the top silicon film of thicker than 1.5 μm. OSF density is measured by preferential chemical etching and microscopic observation. Preparation of samples and measurement of OSF density are as follows:

8.2.1.1 *Sample Preparation* — SOI wafers are oxidized at 1,100°C, 1 h, in H_2 / O ambient after the SC-1 and SC-2 cleaning. Oxide is removed by ca. 25 % HF and then the SOI wafers are preferentially etched by 1 μm, applying JIS H 0609:1994(B), and then rinsed thoroughly in distilled water and blown dry. JIS H 0609 defines the chromium-free preferential solution, which is composed of HF, HNO_3, CH_3COOH and H_2O.

8.2.1.2 *Measurement of OSF Density* — Samples are examined by an optical microscope. The sample surface is observed by magnification of 200 X, and OSF is counted on SOI wafer within the scope along the two lines, which are parallel and perpendicular to the orientation flat (so called cross scanning). OSF density is calculated from the count number and scanning area.

8.3 *Buried Oxide Defect*

8.3.1 *Cu Decoration Method* — In case of Bonded SOI, the buried oxide is usually formed by thermal oxidation. Therefore, the defect of buried oxide is taken into consideration only for the thin oxide cases. Buried oxide defect such as pinholes can be evaluated by Cu decoration method. This method has been applied to the buried oxide film of less than 400 nm thickness. Sample preparation and Cu decoration are conducted by the following procedure. The top silicon film on the buried oxide is removed by KOH solution, and then cleaned and rinsed. The sample is set on a gold-plated brass (Cathode) in the methanol solution. On the other side, a copper plate (Anode) is placed 5 mm above the sample surface. Positive constant bias of 1–3 MV/cm (ex. 40–120 V for 400 nm oxide) is applied to the copper plate for 5 minutes. Small leakage current passes through the buried oxide defect, and consequently copper precipitates on the defects. Typical allowable defect density is $< 0.1/cm^2$.

8.4 *Metal Contamination*

8.4.1 The surface metal contamination can be measured by TXRF, AAS and ICP-MS methods.

8.4.2 *TXRF (Total X-Ray Fluorescence)* — Total X-ray Fluorescence uses a low angle incident, and a tightly collimated X-ray beam excites the characteristic X-rays from impurity atoms near the sample surface. Usually, the angle of X-ray incident is less than 0.1 degree. The element identification and the amount of the element can be obtained by measuring energy and intensities of fluorescence X-ray. The instrument provides a map of impurity element distribution. The surface metal contamination (typically from Na to Zn) shall be less than 10^{11} cm^{-2} in total.

NOTE 8: This TXRF method is conveniently used to detect the metals on the SOI wafer surface.

8.4.3 *AAS (Atomic Absorption Spectrophotometry)* — The elemental characteristic absorption of the atom is measured by introducing sample solution as aerosol into the flame and then spectral absorption through the flame from the light source is detected by the spectroscope. The flameless method, superior to the flame method in the sensitivity, is now broadly used.

8.4.3.1 *Sample Preparation* — Careful sample preparation is necessary for the precise measurement. SOI wafer surface is exposed to HF vapor, and the metals on the surface are collected as droplet. To improve the sensitivity, the volume of collective solution should be as tiny as possible and the HF drops are rolled all over the surface in collective operation. In case of precious metals, it is better to use other kinds of collective solutions instead, since they are not dissolved or collected by HF solution itself.

Examples:

For Cu; HF-H_2O_2 (HF : H_2O_2: H_2O = 1 : 17 : 82)

For Au and Pt; aqua regia (HNO_3 : HCl = 1 : 3)

8.4.4 *ICP-MS (Inductively Coupled Plasma Mass Spectrometry)* — ICP-MS is composed of ICP (Inductively Coupled Plasma) part as an ion source and MS (Mass Spectrometer) part, which measures the ions generated at ICP part. Usually, sample solution is vaporized in the nebulizer and then finally introduced into Argon plasma in the silica tube called torch through the spray chamber. The sample is decomposed, evaporated, atomized and then ionized in the Argon plasma. Except for few atoms that have relatively high ionization potential, most of the elements (> 90%) can be ionized. Ions are identified and measured in amount by the mass spectrometer.

8.4.4.1 *Sample Preparation* — The same method as AAS method is applicable. In case of quantitative measurement of Fe, since its mass weight is close to that of ArO^+, it is necessary to pay attention to the degradation of detection sensitivity.

8.5 *Particle Density (LPD : Light Point Defect)*

8.5.1 *Light Scattering Tomography* — The particle larger than 0.2 μm on the thick SOI wafers is counted by Automated particle counter. The particles in the order of 0.1 μm can be detected if top silicon film is sufficiently thick.

8.5.2 *Principle of measurement* — By scanning the laser beam on the wafer surface, the light scattered by the particles on the wafer is detected. The scattered light and the noise from the wafer surface is detected as a direct current, on the other hand, the scattered light by the particles can be detected as pulse components. The particle size can be calibrated with standard polystyrene latex spheres. Multi-layers of SOI wafers usually have scattering noise from the layer interface. In case of less than 1 μm of the top silicon film thickness, it is necessary to reduce incident angle of the laser beam to increase the reflective component from the surface. For example, S/N ratio is improved when using S-polarized light of 10 degree incident, 85% of its component is reflected from silicon surface.

NOTE 9: In case of SOI wafer (Thickness > 1 μm)

Particle counter with a vertical incident laser, which is the same one used for the bulk wafer, is applied. It should be noted that bypass filter to erase the interference signals due to thickness dispersion, and adjustment of photo-multiplier sensitivity are necessary. By this technique, it is capable of detecting particles (> 0.1μm) as much as on the bulk wafer.

NOTE 10: In case of SOI wafer (Thickness < 0.5 μm)

It is recommended to use S - polarized light or normal light with low incident angle because of high scattering noise. However, the adjustment of photo-multiplier sensitivity is necessary to reduce the noise component. The sensitivity depends on the magnitude of the noise and it is usually possible to detect particles of around more than 0.5μm (in bulk wafer, > 0.2 μm).

8.5.3 *Visual Inspection* — SOI wafer can be visually inspected in accordance with ASTM F523. The automatic inspection equipment is also used when available. For visual inspection, the collimated high intensity bright light (ex. 500,000 lux) is used. Under using this light, SOI wafer is inspected for haze, slip, scratches, chips, cracks, pits, dimples, mound, orange peel, LPD and contamination.

8.6 *Surface Roughness*

8.6.1 *AFM (Atomic Force Microscope)* — By contacting the probe equipped with the cantilever onto the wafer surface of the sample, and by scanning the cantilever and detecting the variation by i.e., optical method, the roughness information is obtained.

NOTE 11: It is expected to set the observation area as > 20 μm × 20 μm to increase reliability of the data.

NOTE 12: Height calibration of concave and convex: Refer to UC standard ("Calibration method of 1 μm order height in AFM", [Ultra Clean Technology, Vol. 7, No. 2, pp. 43, 1995]).

8.7 *Inclusions*

8.7.1 In bonded SOI wafer, there exists the contaminants at the bonding Si/SiO_2 or SiO_2/SiO_2 interface such as particles, metals, boron, and hydrocarbon. Here, inclusions means the contaminants. Although there has been no report on the influence of contaminants to the device characteristics, the improvement of the contamination level is required.

8.8 *Void*

8.8.1 *Scanning Acoustic Topography* — The void can be detected by means of the traveling time difference of the acoustic waves. The void mapping can be made by scanning an ultrasonic wave and detecting the reflecting wave from the both surfaces of the void. Measuring in water improves the resolving power of location since the ultrasonic wave can be tightened by acoustic lenses.

NOTE 13: It is not suitable to measure SOI wafer that is not bonded firmly because measurement is conducted in water.

NOTE 14: It is not suitable to measure top silicon film (< 7 μm) because it is impossible to separate reflective waves both from top silicon film surface and the bonding interface.

NOTE 15: Detectable void gap depends on acoustic wave frequency. Detectable void diameter depends on the size of the acoustic source and the receiver. For example, if using 75

MHz frequency, 5 nm void gap and 50 μm void diameter can be detected.

NOTE 16: Void is defined as "empty space" that is due to the imperfect bonding at Si/SiO_2 and SiO_2/SiO_2 interface. This void should be discriminated from the splitting at bonding strength test.

NOTE 17: Void can be only evaluated during SOI wafer processing, not at the shipping.

8.9 *Bonding Strength*

8.9.1 *Tensile Testing Method* — Bonding strength is defined and evaluated by tensile strength (kgf/cm^2) which is needed to split the bonding interface vertically. Details of the test structure and the test method should be determined by negotiation between wafer users and wafer suppliers.

Table 6 Test Summary Table

Parameter	*Reference*	*Method*
Wafer Diameter	F613-93	Optical Comparator
Wafer Thickness	F533-96, F1530-94	Thick. Gage, Auto. Noncontact Scan.
Total Thickness Variation LTV	F1530-94	Automated Noncontact Scanning
Warp	F1390-92	Automated Noncontact Scanning
Crystal Orientation Top Silicon Film (SOI) Base Wafer	F26-87a (1993)	X-ray Diffraction
Substrate Type / Dopant	F42-93	Hot-Probe (Test Method A)
Substrate Resistivity	F43-93, F84-93, F1527-94	4 Point Probe
Substrate RRG	F81-95	4 Point Probe
Top Si Film Thickness	Section 8.1	Reflective Spectroscopy or FTIR
Crystal Defect (OSF)	Section 8.2, (JIS H 0609 :1994 B)	Cr-free Etch / Optical Microscopy
Buried Ox defects	Section 8.3, (SEMI M34)	(a) Cu Decoration, (b) BOX Capacitor
Metal Contamination (per unit area)	Section 8.4, (F1526-95)	TXRF, AAS/ICP-MS
Particle Density (LPD)	Section 8.5 (F1620-96)	Light Scattering Tomography (Automated Particle Counter)
Haze	F523-93 (see NOTE 1), F154-94	Visual Inspection
Slip	F523-93 (see NOTE 1), F154-94	Visual Inspection
Scratches	F523-93 (see NOTE 1), F154-94	Visual Inspection
Chips / Cracks	F523-93 (see NOTE 1), F154-94	Visual Inspection
Pits and Dimples	F523-93 (see NOTE 1), F154-94	Visual Inspection
Mounds	F523-93 (see NOTE 1), F154-94	Visual Inspection
Orange peel	F523-93 (see NOTE 1), F154-94	Visual Inspection
Particle Density (LPD)	F523-93 (see NOTE 1), F154-94	Visual Inspection
Contamination (Both Side)	F523-93 (see NOTE 1), F154-94	Visual Inspection
Surface Roughness	Section 8.6	AFM
Inclusions	Section 8.7	SIMS
Voids	Section 8.8	Scanning Acoustic Tomography
Bonding Strength	Section 8.9	Tensile Strength

NOTE 1: Users and suppliers may agree on the non-SOI edge area for these specifications. For example the area within 6 mm proximity of the wafer edge may be excluded.

Table 7 Example: Soi Wafer Surface Visual Inspection Criteria

Criterion Items	*Allowed Quantity (Per 150 mm Wafer)*	*Description*
Haze	NONE	
Slip	< 4 2 mm width and < 15 mm length	
Scratches	NONE	
Chips / Cracks	< 3 for @ 0.5 mm circumferential x 0.3 mm length	Edge : Base Wafer
Pits and Dimples	NONE	
Particle Density (LPD)	< 30 for @ > 0.2 μm	<0.17 / cm^2 for 150 mm Wafer
Contamination	NONE	Both Surface and Backside

NOTE 1: The surface visual inspection is conducted under the collimated bright light.
NOTE 2: Non-SOI edge area (E.E.) of 6 mm is applied to the criterion items except for edge chips/cracks.
NOTE 3: The whole wafer (Top silicon film and Base wafer) is inspected except for edge chips/cracks.

Table 8 Soi Electrical Parameters

Parameters	*Reference*	*Value*	*Method*
Photo-conductivity Lifetime	Section 9.1	To be determined	μ-PCD
BOX Breakdown	Section 9.2	To be determined	I-V
BOX Charge	Section 9.3	To be determined	C-V
BOX Surface States	Section 9.4	To be determined	C-V
Doping Density Top silicon film, Base wafer	Section 9.5	To be determined	SIMS or 4 pt. probe

9 Electrical Parameters

9.1 *Photo-conductivity Lifetime*

9.1.1 *Test Method: μ-PCD method*

9.1.1.1 Excess carriers that are created in the wafer by a light pulse increases the conductivity of the sample. When the light is turned off, the conductivity is decreased by the carrier recombination. This phenom-enon is monitored by means of microwave reflectance. The microwave detects an exponential decay in conduc-tivity, from which a decay constant is determined.

9.1.2 The effective recombination lifetime τ_{eff} is given by the following expression:

$$1/\tau_{eff} = 1/\tau_B + 1/(\tau_S + \tau_D)$$

$$\tau_S = d/(S_{Si/Box} + S_{Si}),\ \tau_D = d/\pi^2 D$$

Where τ_B is bulk recombination lifetime, τ_S is surface recombination lifetime, τ_D is diffusion lifetime, $S_{Si/Box}$ is recombination velocity at the Box interface, S_{Si} is recombination velocity at the silicon surface, D is diffusion coefficient and d is top silicon film thickness.

9.1.3 The wavelength of the light has to be selected, depending on the top silicon film thickness (see Table 9).

9.2 *Box Breakdown Voltage*

9.2.1 *Test Structure* — Box capacitor having an area (Ex. 1 cm^2).

9.2.2 *Test Method: Staircase I-V Measurement* — Voltage is stepwise increased in one-volt increments from zero to the (+/-) specified voltage. Details of the test structure and the test method are determined by negotiation between wafer users and wafer suppliers.

9.3 *Box Charge*

9.3.1 *Test Structure* — Box capacitor having an area (Ex. 1 cm^2).

9.3.2 *Test method* — MOS high-frequency C-V measurement of a Box capacitor normally yields a flat band voltage. Details of the test structure and the test method are determined by negotiation between wafer users and wafer suppliers.

9.4 *Buried Oxide Fast Interfaces State Density*

9.4.1 *Test Structure* — Box capacitor having an area. (Ex. 1 cm^2)

9.4.2 *Test Method* — High-Low Frequency MOS C-V.

9.4.3 If care is taken in their fabrication to minimize oxide surface damage and contamination during silicon etching, good quality quasi-static MOS C-V curves can be measured. From comparison of high and low frequency C-V curves, midgap interface state density can be determined. Details of the test structure and the test method are determined by negotiation between wafer users and wafer suppliers.

9.5 *Doping Density*

9.5.1 *Test Method* — SIMS

9.5.1.1 Be careful of electrical charging up of test pieces due to the existence of BOX, the difference of detecting sensitivity between silicon and silicon dioxide, and the existence of disturbance ions such as $Si^{30}H^1$ in case of P^{31} measurement.

Table 9 Relationship Between Wavelength of the Light and Penetration Depth

Wavelength [nm]	450	532	635	670	780	820	850
Depth [μm]	~ 0.8	~ 1.4	~ 3.0	~ 4.0	~ 10.0	~ 14.0	~ 18.0

9.5.2 *Test Method* — Four point probe

9.5.2.1 By contacting the equally spaced four point probes with a wafer and by supplying current between the outer two probes, the voltage difference between the inner two probes is measured. The silicon resistivity ρ is determined by the following equation (JIS H0602):

$$\rho = \pi V / \ln 2 \bullet I \bullet d [\Omega cm] \quad \text{if probe interval} >> \text{top silicon film thickness: d}$$

9.5.3 The specific test method should be determined between wafer users and wafer suppliers.

10 Packing and Marking

10.1 Special packing requirements shall be subject to agreement between the users and the suppliers. Otherwise all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches and contamination, and in accordance with the best industry practices to provide sample protection against damage during shipment.

10.2 The wafer supplied under these specifications shall be identified by appropriately labeling on the outside of each box or other container and each subdivision thereof in which it may be reasonably expected that the wafers will be stored prior to further processing. Identification marks, codes, symbols and content shall be agreed upon between users and suppliers.

SEMI M42-1000
SPECIFICATION FOR COMPOUND SEMICONDUCTOR EPITAXIAL WAFERS

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the North American Compound Semiconductor Committee. Current edition approved by the North American Regional Standards Committee on August 28, 2000. Initially available at www.semi.org September 2000; to be published October 2000.

1 Purpose

1.1 Compound semiconductor epitaxial layers have been extensively used for many years as the basis of high speed electronics and optoelectronic devices. There are suppliers of epitaxial layers who will grow material to the customer's specification. There is a need to define standardized descriptive terms, tolerance schedules and recommended test methods to reduce ambiguity in the interpretation of specifications for such wafers. Special emphasis is placed on the definitions pertaining to uniformity. This proposed document addresses only the basic requirements. Further clarification may be required between supplier and purchaser for the particular layers required.

2 Scope

2.1 These specifications cover the requirements for epitaxial layers of the generic composition $A_aB_bC_c...N_n$ grown on monocrystalline wafers of GaAs or InP (other substrates may be considered where appropriate documents exist to describe the specification of the substrate). This document may only cover a portion of the properties considered to be part of the purchase specification.

2.2 This specification does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this specification to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standard*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

3.2 *ASTM Test Methods*[1]

ASTM F76 — Standard Test Methods for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Single-Crystal Semiconductors.

ASTM F673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy Current Gage.

3.3 *DIN Standard*[2]

DIN 50447 — Contactless Determination of the Electrical Sheet Resistance of Semiconductor Layers with the Eddy Current Method

4 Terminology

4.1 *epitaxy* — the growth of a single crystal layer on a substrate of the same material, homoepitaxy; or on a substrate of different material with compatible crystal structure, heteroepitaxy

4.2 *fixed quality area (FQA)* — (refer to Figure 1 of SEMI M1) the central area of the wafer surface, defined by a nominal edge exclusion, X, over which the specified values of a parameter apply.

4.3 *mismatch* — the ratio, m_c, defined by the lattice constant of the epitaxial layer perpendicular to the surface, c, minus that of the substrate, a_o divided by the substrate lattice constant.

$$m_c = (c - a_o)/a_o$$

4.4 *mole fraction* — the normalized fraction of a particular element occupying the same lattice site in a compound. E.g. in the compound $A_aB_bC_cD_d$, a, b, c and d are the mole fractions of the elements A, B, C and D respectively. If, in this example, A and B share the same lattice site, and C and D share the other lattice site, then by definition the sum of a and b, and the sum of c and d each must be 1.

4.5 *graded layer* — a layer whose properties vary smoothly in the direction perpendicular to the surface. The properties of a graded layer are specified in terms of the parameters at the top (last to grow surface) and bottom (first to grow surface) of the layer and unless otherwise specified, are expected to vary linearly between these two end values.

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959

2 Deutsches Institut für Normung e.V., available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany

5 Wafer Ordering Information

5.1 Purchase orders for epitaxial layers must include the following items:

5.1.1 The substrate (as described by the relevant SEMI Standard).

5.1.2 The epitaxy growth method.

5.1.3 The nominal edge exclusion used to define the FQA.

5.1.4 The composition of each layer in terms of mole fraction(s) and a description of the test method used to measure it and/or calibrate the growth conditions of that layer. Note that in the case of a ternary compound, the purchaser may require that the specification for mismatch or bandgap energy take precedence over that for nominal composition. Similarly in the case of a quaternary compound, a specification of mismatch and bandgap energy may be preferred. This is because the mismatch and bandgap energy, which depend on the composition, are often easier to measure than the composition directly.

5.1.5 The thickness of each layer and a description of the test method used to measure it and/or calibrate the growth conditions of that layer.

5.1.6 The dopant used for each layer.

5.1.7 The carrier concentration of each layer and a description of the test method used to measure it and/or calibrate the growth conditions of that layer. In the case of layers with significant interface or surface depletion, the carrier concentration refers to the value that would be observed in thicker layers, once the appropriate correction is applied for interface and surface depletion effects.

5.1.8 *Optional Criteria* — The following items may also be specified in addition to those listed above.

5.1.8.1 The mobility of each layer.

5.1.8.2 The sheet resistance of the epitaxial layers.

5.1.8.3 The mismatch for each layer. The test method must be described.

5.1.8.4 The bandgap energy for each layer. The test method must be described.

5.1.8.5 The sheet carrier concentration and mobility of the whole structure. This is relevant to those structures where the carriers are expected to redistribute to an adjacent material or interface.

5.1.8.6 The surface defect density.

5.1.8.7 The end values and thickness of each graded layer.

5.1.8.8 The surface roughness. The test method must be described.

5.1.8.9 The growth and test methods of a calibration structure along with a schedule for the growth of such a structure.

6 Tolerance Requirements

6.1 The tolerance requirements for the specified parameter, unless otherwise agreed to between the supplier and purchaser, are as in Table 1. Tolerance is defined as the allowed range of values permissible within the FQA and includes variations due to non-uniformity and deviation from the customer's target value. The measurement point schedule (map of measurement points) should be agreed upon between the supplier and purchaser. Three classifications are given for products of varying control needs.

Table 1 Parameter and Tolerance Requirements

Parameter	*Tolerance A*	*Tolerance B*	*Tolerance C*
composition [mole fraction (s)]	± 0.05	± 0.01	± 0.005
thickness [percent of nominal]	± 20%	± 10%	± 5%
carrier concentration [percent of nominal]	± 20%	± 10%	± 5%
sheet resistance [percent of nominal]	± 20%	± 10%	± 5%

Table 2 Parameter and Recommended Measurement Technique

Parameter	*Technique*	*Test Method*
composition	infer from bandgap energy measured by photoluminescence, or photo reflectance	under development
	and/or from mismatch measured by high resolution X-ray diffractometry	none as yet
thickness	cleaved cross sections measured by optical or scanning electron microscopy	needs revision
	and/or profilometry of selectively etched layers	none as yet
carrier concentration	Hall effect	ASTM F 76- needs revision
	or C-V profiling (electrochemical or mercury probe)	none as yet
sheet resistance	Van der Pauw technique	ASTM F 76
	and/or eddy current	ASTM F 673 or DIN 50447
mobility	Hall effect	ASTM F 76

7 Test Methods

7.1 Measurements shall be carried out according to the methods outlined in Table 2. Where no methods are specified, or where choices are given, the supplier and purchaser shall agree in advance on the means for making the measurement.

7.2 Given the state of development for the recommended test methods and the lack of standard reference materials, it is advisable that the vendor and purchaser exchange samples to cross calibrate their measurement instruments and procedures.

8 Marking

8.1 In addition to the requirements set out in the specification for the substrates, a unique number traceable to the growth run shall be identified on the supplier's certificate.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 The user and supplier may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 7; however, if the user performs the test and the material fails to meet the requirement, the material may be subject to rejection.

SEMI M43-0301
GUIDE FOR REPORTING WAFER NANOTOPOGRAPHY

This guide was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on November 22, 2000. Initially available at www.semi.org December 2000; to be published March 2001.

1 Purpose

1.1 This guide provides a framework for reporting of nanotopography surface features on silicon wafers.

2 Scope

2.1 This guide addresses reporting the characterization of nanotopography surface features found on wafer surfaces. Nanotopography is the non-planar deviation of the whole front wafer surface within a spatial wavelength range of approximately 0.2 to 20 mm and within the fixed quality area (FQA). Typical examples include dips, bumps or waves on the wafer surface that vary in peak to valley height from a few nanometers to a several hundred nanometers.

2.2 This guide provides a framework for communicating specific values limiting feature levels and/or densities as agreed upon between suppliers and users.

2.2.1 *Discussion* — Nanotopography measurements have not been needed for 0.25 µm generation devices, but are expected to be required for smaller feature sizes to meet CMP requirements. Nanotopography on a wafer surface prior to CMP processes can result in variations in post-CMP dielectric thickness with potential negative consequences for circuit performance and yield; features as small as 20 nm (peak to valley) can result in post CMP discoloration of dielectrics as a result of local thickness variation of the remaining dielectric[1]. Height variations over specified distances (determined by CMP issues and/or lithography systems) need to be properly controlled to assure that wafers are acceptable for selected process steps. In the case of CMP, the issue is control of film thickness variation introduced by nanotopography. The metrology industry is building tools that will measure and map surface features at nanotopography amplitudes and spatial wavelengths. Nanotopography features are characterized by their height variation within an area, and are discriminated from other features of similar height by their spatial wavelength range.

2.3 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability or regulatory limitations prior to use.

3 Limitations

3.1 The reported surface features will be influenced by limitations and parameters of the measurement tool. These include:

3.1.1 The finite surface spatial bandwidth of the tool and the applied filtering will prevent surface variations outside the bandwidth of operation from being measured. Also, the finite bandwidth of filtering produces non-physical artifacts that may be apparent in regions where the power in the rejected bands is high.

3.1.2 Bandwidth edges are not always well defined. Measurement results do not always agree well between systems, because different tool designs employ different geometries and operate them over different spatial bandwidths.

3.1.3 All surface profiling measurement systems have a minimum height variation sensitivity that will distort signals near the noise floor.

3.1.4 The reported shape of some features may also depend on the pixel grid orientation employed by the instrument.

3.1.5 The pixel size and sampled area will affect the bandwidth limits.

3.2 Reported profiles also vary with interactions between wafer and tool. These limitations include:

3.2.1 Measurements made near the wafer edge may result in false readings. Under certain conditions, this may cause incorrect height measurement within the FQA.

3.2.2 Closely spaced features may be counted as a single feature, or as no feature, if the pixel size is larger than the feature, or is larger than the spacing between features. Reported features may result from the combination of the actual surface features, the manner in which the wafer is chucked, or be caused by particles trapped between the wafer back surface and the chuck.

3.2.3 High-pass (spatial frequency) filtering is typically used with these measurements to remove the (long-spatial wavelength) effects of wafer shape (such

1 K. V. Ravi, "Wafer Flatness Requirements for Future Technologies," Future Fab International, July 1999.

as bow, warp and sori). This filtering may affect the reported results.

3.3 Nanotopography characterization does not include microroughness, which applies to a shorter spatial wavelength range.

3.4 The location of defective areas as calculated in section 6 may not coincide with the location of the surface features that lead to those values. This may cause lack of spatial correlation between reported defective areas and device process defect areas.

3.5 The height map used to create nanotopography reports may be affected by wafer shape and measurement chuck effects.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI M1 — Specification for Monocrystalline Polished Silicon Wafers

NOTE 1: As listed or revised, all documents cited shall be the latest publications of adopted standards.

5 Terminology

5.1 *fixed quality area (FQA)* [SEMI M1] — the central area of a wafer surface, defined by a nominal edge exclusion, X over which the specified values of a parameter apply.

Discussion: The boundary of the FQA is at all points the distance X away from the periphery of a wafer of nominal dimensions. (See Figure 1). The size of the FQA is independent of the wafer diameter and flat length tolerances. For the purpose of defining the FQA, the wafer periphery at locations with notch fiducials is assumed to follow the circumference of a circle with diameter equal to the nominal wafer diameter.

5.2 *nanotopography, of a wafer surface* — the non-planar deviation of a surface within a spatial wavelength range of approximately 0.2 to 20 mm.

5.3 *nanotopology, of a wafer surface* — see *nanotopography*.

5.4 *roughness* [SEMI M1] — the more narrowly spaced components of surface texture.

Discussion: These components are considered within defined limits of spatial wavelength (or frequency).

5.5 *spatial wavelength* — the spacing between adjacent peaks of a purely sinusoidal profile.

6 Measurements

6.1 The height map is obtained from a front-surface measurement. An explicit reference plane is not used for calculating and assigning values.

NOTE 2: Other methods of analyzing nanotopography may require the use of an explicit reference plane.

6.2 The high-pass filter removes long spatial wavelength wafer tilt and topography effects, effectively creating a global reference surface.

6.3 *Calculation* — The calculation determines the peak to valley height (P-V) variation among the pixels included in the analysis area, and assigns that variation in nanometers to the center of the analysis area. The calculation is performed for every analysis area within the FQA of the wafer. These calculations may be repeated for analysis areas of different dimension D.

NOTE 3: This calculation describes the "full-analysis area" method. There is another calculation, the "partial analysis area" method, where the calculation is performed for every analysis area whose center pixel is within the FQA of the wafer. The partial analysis area method, not defined in this document, is being addressed by SEMI for inclusion in a standard.

6.4 The following measurement elements should be reported:

6.4.1 *Filtering*

a) Spatial cutoff of high pass filter

b) Type of Filter

c) Pixel spacing

Filtering is used to remove long wavelength shape components from the raw height data.

6.4.2 *Analysis Area* — Specify this analysis area's:

a) Shape, e.g., square, circle, and

b) Dimension *D* of the analysis area

An analysis area contains a pixel at its center (Figure 1). The pixels within the surrounding analysis area of dimension *D*, and within the FQA, are used to determine the value assigned to the center pixel location.

6.4.3 *Data Report* — Report one or more of the following:

6.4.3.1 *Statistical Representation by Threshold Curve* — Plot, for each D, % area vs. threshold T, in nanometers, where % area is the ratio of

a) the number of analysis areas whose assigned value (calculated per Section 6.3) exceeds the threshold T, to

b) the number of pixels within the FQA.

The ratio is expressed as a percentage.

6.4.3.2 *Tabular Representation by % Area Sorted* — Specify a threshold T for each D and report the % area.

6.4.3.3 *Tabular Representation by Threshold* — Specify a % area for each D and report the Threshold, T.

6.4.3.4 *Spatial Representation by Height Map* — Generate a whole wafer height map of the surface.

6.4.3.5 *Spatial Representation by Defect Map* — Generate a whole wafer height map of the surface. Analysis areas whose assigned values (calculated per Section 6.3) exceed the threshold in Section 6.4.3.2 are flagged for each D.

6.4.3.6 *Spatial Representation by PV Analysis Map* — Generate a whole wafer map of the values assigned in Section 6.3.

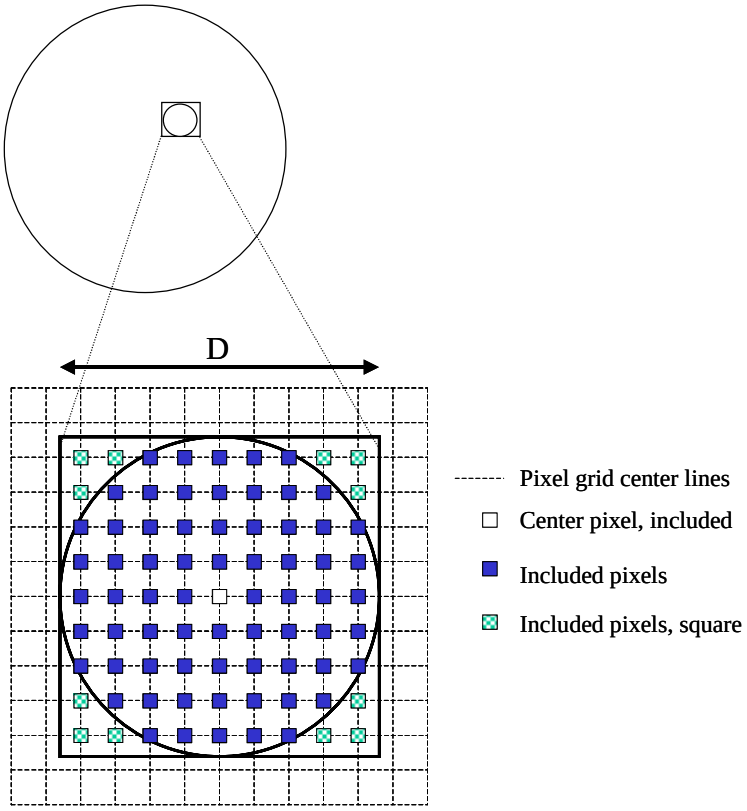

Figure 1
The Analysis Area Of Dimension D, Center And Included Pixels Are Indicated

RELATED INFORMATION 1

NOTE: This related information is not an official part of SEMI M43 and is not intended to modify or supercede the proposed standard. It is provided for information purposes. The proposed standard should be referred to in all cases.

R1-1 SEMI M43 describes reporting wafer nanotopography. The figure below illustrates the flow of data from measurement through reporting referenced to the document sections.

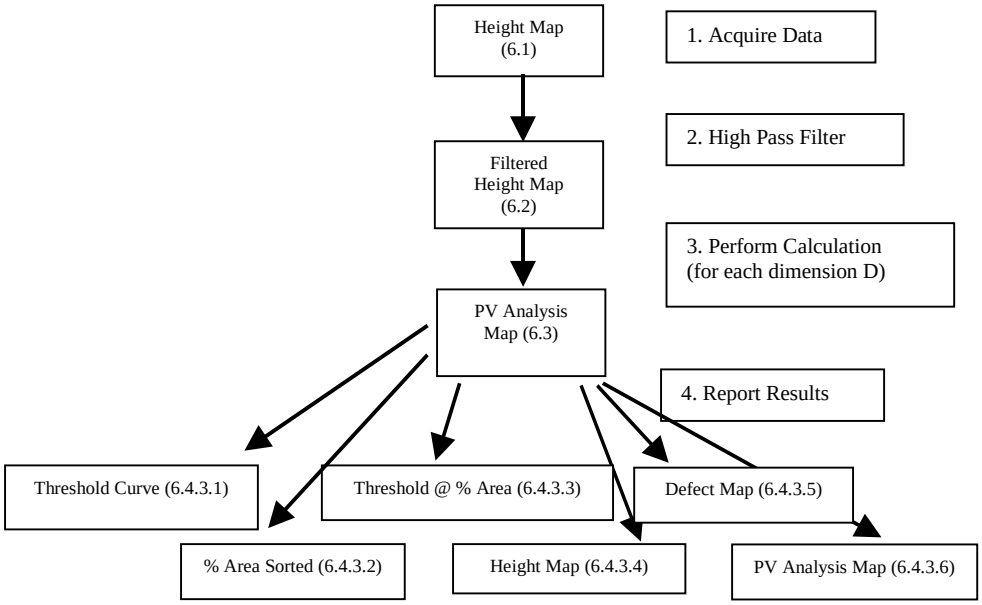

Figure R1-1
Nanotopography Reporting Flow

SEMI M44-0305
GUIDE TO CONVERSION FACTORS FOR INTERSTITIAL OXYGEN IN SILICON

This guide was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved for publication by the Japan Regional Standards Committee on January 11, 2005. Initially available at www.semi.org January 2005; to be published March 2005. Originally published March 2001; previously published July 2002.

1 Purpose

1.1 Over the years numerous calibration factors used to calculate the interstitial oxygen content of silicon from the peak room-temperature infrared absorption at 1107 cm^{-1} have been standardized by several standards development organizations in various parts of the world. All such standards have since been revised to use the IOC-88 calibration factor[1,2] that more correctly relates the true oxygen content of silicon to the absorption peak. Nevertheless, many of the old calibration factors remain in common use throughout the industry.

1.2 This guide is a compilation of the conversion and calibration factors used in standards established by various organizations since 1970 for the measurement of interstitial oxygen in silicon.

2 Scope

2.1 This guide allows the user of the guide to convert quantitative values obtained from one standard to another.

2.2 Two tables are included in the guide.

2.2.1 Table 1 gives the calibration factors to relate peak absorption coefficient (cm^{-1}) to interstitial oxygen content in both parts per million atomic (ppma) and atoms/cm^3 for various standards, all of which have been replaced by newer revisions.

2.2.1.1 These calibration factors are at times referred to by common names as indicated in column 1 of the tables and at other times by the designation of the (obsolete) standard in which they were standardized (as indicated in the footnotes to Table 1). Despite the fact that there is a test method associated with each calibration factor, the detailed procedures in these test methods are usually ignored in common practice and measurements are most frequently made with automated (black-box) instruments that have internal algorithms. Thus, reference to a particular standard most often indicates only the value of the calibration factor to be used.

2.2.2 Table 2 gives the conversion factors to convert oxygen concentration of one standard to oxygen concentration of another standard.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health guides and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M59 — Terminology for Silicon Technology

SEMI MF1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption with Short Baseline

1 Baghdadi, A., Bullis, W. M., Croarkin, M. C., Li Yue-zhen, Scace, R. I., Series, R. W., Stallhofer, P., and Watanabe, M., "Interlaboratory Determination of the Calibration Factor for the Measurement of the Interstitial Oxygen Content of Silicon by Infrared Absorption," *J. Electrochem. Soc.* **136**, 2015–2034 (1989).

2 Baghdadi, A., Scace, R. I., and Walters, E. J., "*Semiconductor Measurement Technology:* Database for and Statistical Analysis of the Interlaboratory Determination of the Calibration Factor for the Measurement of the Interstitial Oxygen Content of Silicon by Infrared Absorption," NIST Special Publication 400-82, July 1989.

3.2 *ASTM Standards*

F 121-70 through F 121-79 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption[3]

F 121-80 through F 121-83 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption[4]

3.3 *JEITA* (*formerly JEIDA*) *Standard*

EM-3504 (61) — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption[5,6]

3.4 *DIN Standards*

DIN 50438 Part 1 [1978] — Determination of Impurity Content in Silicon by Infrared Absorption: Oxygen[7]

DIN 50438 Part 1 [1994, 1995] — Determination of Impurity Content in Silicon by Infrared Absorption; Part 1 Oxygen[8]

3.5 *Guo Biao Standard*

GB/T 1557-1989 — Test Method for Interstitial Oxygen Content in Silicon Crystals by Infrared Absorption Spectroscopy (in Chinese)[9]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Many terms relating to silicon technology are defined in SEMI M59.

5 Other Techniques

5.1 Other measurement techniques for measuring oxygen in silicon (e.g., SIMS or gas fusion analysis, GFA) measure total oxygen whereas the infrared absorption methods, to which this guide applies, measure interstitial oxygen only.

6 Conversion Factors Among International Standards

6.1 Table 1 gives the calibration factors published in various standard test methods for determination of interstitial oxygen content in silicon by infrared absorption. The factor to obtain the oxygen concentration in parts per million atomic is given in column 2 while the factor to obtain the oxygen density in atoms/cm^3 is given in column 3. The calibration factors are listed in order from the smallest value to the largest value irrespective of the time frame over which they were adopted.

6.2 Table 2 gives the factors to convert oxygen concentration of one standard to oxygen concentration of another standard. The interstitial oxygen content found by any procedure may be reported in any other standardized scale by multiplying the value by the appropriate conversion factor in Table 2. The factors are listed in the same order as in Table 1.

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3 Revised to change the calibration factor in 1980; last available edition in the 1980 edition of *Annual Book of ASTM Standards*, Part 43. ASTM International, 100 Barr Harbor Drive, West Conshohocken, PA 19428. Telephone: 610-832-9500, Fax: 610-832-9555, Website: www.astm.org

4 Withdrawn in 1988; last available edition in the 1987 edition of *Annual Book of ASTM Standards*, Vol 10.05. Replaced by ASTM F 1188 (now SEMI MF1188) that refers to IOC-88.

5 Japan Electronics and Information Technology Industries Association, 3rd floor, Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan, Telephone: 81.3.3518.6434, Fax: 81.3.3295.8726, Website: www.jeita.or.jp.

6 This standard replaces the calibration factor reported in T. Iizuka, S. Takasu, M. Tajima, T. Arai, T. Nozaki, N. Inoue, and M. Watanabe, "Determination of Conversion Factor for Infrared Measurement of Oxygen in Silicon," *J. Electrochem. Soc.* **132**, 1707-1713 (1985), which was previously widely used in Japan.

7 Deutches Institut für Normung e.V., Burggrafenstrasse 6, 10787 Berlin, Germany, Telephone: 49.30.2601-0, Fax: 49.30.2601.1263, Website: www.din.de. Replaced in 1994 by revised edition that refers to IOC-88.

8 Deutches Institut für Normung e.V standards are available in both English and German editions from Beuth Verlag GmbH, Burggrafenstrasse 6, 10787 Berlin, Germany, Telephone: 49.30.2601.0, Fax: 49.30.2601.1263, Website: www.beuth.de.

9 China Electronic Standardization Institute, Beijing, China

6.3 Irrespective of the calibration factor, to convert oxygen density (atoms/cm^3) to oxygen concentration (ppma), within the same calibration factor, divide the oxygen density value by the factor 5×10^{16} (atoms·cm^{-3}·$ppma^{-1}$), and to convert oxygen concentration (ppma) to oxygen density (atoms/cm^3), within the same calibration factor, multiply the concentration value by the same factor.

Table 1 Calibration Factors

Calibration Factor	*Cited in Standard(s) or Publication*	*Value to Obtain Oxygen Content in ppma*	*Value to Obtain Oxygen Content in atoms/cm^3*
New ASTM	ASTM F 121, 1980-1983; DIN 50438/1, 1978	4.90	2.45×10^{17}
"JEIDA Coefficient (Original)"	Cited in Iizuka *et al*., see Footnote 6	6.06	3.03×10^{17}
Guo Biao (Old Edition)	Cited in Baghdadi *et al*., see Footnotes 1 and 2.	6.20	3.10×10^{17}
IOC-88	SEMI MF1188; DIN 50438, 1994 and 1995; JEITA EM3504; Guo Biao GB/T 1557-1989	6.28	3.14×10^{17}
Old ASTM	ASTM F 121, 1970-1979	9.63	4.815×10^{17}

Table 2 Conversion Factors

To: → / *Convert From: ↓*	*New ASTM*[#1]	*"JEIDA Coefficient (Original)"*[#2]	*Guo Biao (Original)*[#3]	*IOC-88*[#4]	*Old ASTM*[#5]
New ASTM[#1]	1	1.237	1.265	1.282	1.965
"JEIDA Coefficient (Original)"[#2]	0.809	1	1.023	1.036	1.589
Guo Biao (Old Edition)[#3]	0.790	0.977	1	1.013	1.553
IOC-88[#4]	0.780	0.965	0.987	1	1.533
Old ASTM[#5]	0.509	0.629	0.644	0.652	1

[#1] Cited in all editions of ASTM F 121 from 1980 through 1983 (replaced by ASTM F 1188, now SEMI MF1188, in 1988) and in the 1978 edition of DIN 50438, Part 1.

[#2] Reported in T. Iizuka *et al.,* Reference 6.

[#3] Old edition; cited in Baghdadi *et al*., see footnotes 1 and 2. Since revised to cite IOC-88.

[#4] See footnotes 1 and 2. Cited in all editions of SEMI MF1188, the 1994 and 1995 editions of DIN 50438, Part 1, all editions of JEITA EM-3504 (and its predecessor JEIDA 16), and the 1989 edition of GB/T 1557.

[#5] Cited in all editions of ASTM F 121 from 1970 to 1979.

SEMI M45-0703
PROVISIONAL SPECIFICATION FOR 300 mm WAFER SHIPPING SYSTEM

This provisional specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the European Silicon Wafer Committee. Current edition approved by the European Regional Standards Committee on April 3, 2003. Initially available at www.semi.org June 2003; to be published July 2003. Originally published March 2001.

1 Purpose

1.1 This standard stipulates transport related materials and systems to minimize the total cost relating to transport of 300 mm wafers from the wafer supplier to the customer.

2 Scope

2.1 This standard stipulates materials relating to transport of 300 mm wafers using Shipping Boxes (FOSB) regulated by SEMI M31, and includes wafer shipping boxes, bags, labels, cushions, secondary containers, pallets, and shipping documentation.

NOTE 1: This standard is provisional because some technical issues are not implemented. Once these issues are addressed, this standard should be modified and upgraded from provisional status.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M31 — Provisional Mechanical Specifications for Front-Opening Shipping Box Used to Transport and Ship 300 mm Wafers

SEMI T3 — Specification for Wafer Box Labels

3.2 *ANSI Standards*

ASNI/EAI-556-B — Outer Shipping Container Label Standard[1]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

1 American National Standards Institute, Headquarters: 1819 L Street, NW, Washington, DC 20036, USA. Telephone: 202.293.8020; Fax: 202.293.9287, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023, Website: www.ansi.org

4 Terminology

4.1 *Definitions*

4.1.1 *bag* — a package used for sealing the outside of the wafer shipping box. Typically two or three types of different plastic film and aluminum film are laminated, and these are usually heat-sealed.

4.1.2 *cushions* — materials placed between the wafer shipping box and secondary container in order to absorb shock during shipping and to stabilize the wafer shipping box within the secondary container.

4.1.3 *label* — the label on the wafer shipping box or items such as bags identifying the product and its manufacturer.

4.1.4 *pallet* — a flat container used for collecting and holding a suitable amount of secondary containers that hold wafers, to make handling with forklifts easier.

4.1.5 *recycle* — to use an already used item for some other useful purpose.

4.1.6 *reuse* — to repeat use of an item in its original shape for the same purpose as initially intended.

4.1.7 *secondary container* — the outermost box of the smallest transport unit. Typically cardboard boxes or similar boxes are used.

4.1.8 *shipping document* — documents required when shipping.

4.1.9 *wafer shipping box* — a box that directly holds the wafers. In this standard, this box is specified by SEMI M31.

5 Requirements

5.1 *Wafer Shipping Box*

5.1.1 Wafer shipping boxes that comply with SEMI M31 must be used.

5.1.2 There are no grounding or ESD requirements for wafer shipping box.

5.1.3 To make sure raw materials are traceable, the product number, revision number, and manufacturing period (year, week) must be displayed on the wafer

shipping box main device and door by molding or by a method that cannot be easily erased.

5.1.4 The wafer shipping box door must be designed so that it can be automatically as well as manually opened and closed.

5.1.5 Optional top robotic handling flange or side mounted human handles will not be attached during transport of the wafer shipping box. If required, these items will be applied at the receiving site. The design of these features will allow for quick, lockable attachment to the wafer shipping box.

5.1.6 Wafers must be visible inside when the wafer shipping box is closed.

5.1.7 No tape may be used to seal the wafer shipping box.

5.1.8 The only environment in which wafers can be placed into or taken out of a wafer shipping box bag, as well as the surrounding environment thereafter, is clean room air.

5.1.9 The body and door of the wafer shipping box must be designed to allow for multiple reuse cycles without compromising wafer quality.

5.1.10 After a customer has transferred an accepted wafer to a fab carrier, the wafer shipping box must be returned to the supplier without having used it for any other purpose. The wafer shipping box will be inserted into a bag sealed prior to return to the wafer supplier using the same type bag (agreed upon by supplier and customer).

5.1.11 Each wafer shipping box must be returned only to the supplier that delivered the wafers for which the wafer shipping box was used. A display for the supplier showing the number of times a wafer shipping box was used is optional.

5.1.12 The property rights of wafer shipping box used to deliver wafers and to be returned after unloading belong to the wafer manufacturers.

5.1.13 The wafer shipping box will maintain its dimensional stability throughout its lifetime.

5.1.14 Wafer shipping box materials must be recyclable after useful life.

5.2 *Wafer Shipping Box Bagging System*

5.2.1 It is preferable that the bag material is recyclable, but until a technical solution is found, bags should be easily disposable.

5.2.2 The bagging system must consist of two or more layers of bags. At least one layer must be a moisture barrier.

5.2.3 The use of desiccant between the bag layers is currently optional. Its use must not negatively impact the cleanliness of the bagging system.

5.2.4 Bags may be evacuated optionally. The initial bag ambient, prior to evacuation and sealing, may be temperature/humidity controlled clean room air, clean dry air (CDA), or nitrogen (N2).

5.3 *Wafer Shipping Box and Bag Labeling*

5.3.1 Prepare and apply two identical labels that are in accordance with SEMI T3, with additional requirements as noted below.

5.3.1.1 Label size may be as large as 120 mm x 120 mm.

5.3.1.2 Label data content shall include all the data specified in SEMI T3, including wafer ID and FOSB slot #. Additional data may be added optionally, as agreed to between supplier and user.

5.3.1.3 Apply one label to the center of the rear surface of the FOSB. The long axis of the label shall be parallel to the FOSB base.

5.3.1.4 Apply the other label to the shipping bag, on the door side of the FOSB.

5.3.2 The wafer shipping box and outer bag labels should use the same peelable, cleanroom compatible label stock. The labels must not leave residual adhesive or backing material on the wafer shipping box when removed.

5.4 *Secondary Container Labeling*

5.4.1 Labels shall be placed in accordance with EIA-556-B.

5.4.2 Prepare labels in accordance with EIA-556-B. Information shall include at least the following [Items below marked by an asterisk (*) are mandatory EIA-556-B data fields]:

5.4.2.1 *Bar Code Data Fields*

- Transport unit License Plate number*
- Transaction identification (Purchase Order number)*
- Total Quantity of Wafers*
- Total Quantity of Cartons
- Customer Part number*

5.4.2.2 *Non-Bar Code Data Fields*

- Ship-to address (including Customer name)*
- Ship-from address (including Supplier name)*

5.4.2.3 Optional information, as agreed to between supplier and user, may be included.

5.5 *Secondary Container*

5.5.1 Whether the secondary container material is a single use material or a material that can be reused multiple times should be decided by considering the transport environment to minimize the packaging cost. The same is true for the secondary container sealing system.

5.5.2 The secondary container should be collapsible for efficient storage and empty transport.

5.5.3 The materials for the secondary container should be recyclable after the designated number of uses is completed.

5.5.4 The design and size of the secondary container should have an optimal fit with the standard pallet noted in Section 5.7.2, and should have the strength to be stacked in four layers.

5.5.4.1 *Secondary Container Dimensions* —The outer size of the secondary container shall be 580 mm wide by 500 mm deep by 460 mm high.

NOTE 2: The specification does not specify tolerances on the dimensions, but the specified dimensions should be adhered to as closely as possible to enhance container stackability.

NOTE 3: These values of width (W) and depth (D) are selected to allow four containers to be placed on the world wide standard pallet (1200 mm by 1000 mm).

NOTE 4: The value of height (H) is selected to allow three layers to be stacked in a standard airfreight container.

NOTE 5: The outer dimensions of the secondary container should be determined considering the requirements of Sections 5.1 (wafer shipping box) and 5.2 (bagging system) and allowance for cushioning thickness sufficient to prevent wafer breakage by accidental drop from a height of 800 mm.

NOTE 6: Height (H) can be negotiated between wafer supplier and user, if the proposed specification is not satisfied for either the supplier or the user.

5.5.5 The number of wafer shipping boxes per secondary container must allow for optimal transportation costs.

5.5.6 Ergonomic considerations should be made for the secondary container, and should be compatible with manual handling. When handling very large quantities, a supplemental handling system is necessary.

5.5.7 The secondary container design is not required to provide specific weather protection. The storage environment should not be affected by the weather.

5.6 *Cushions*

5.6.1 Whether the cushion material is a single use material or a material that can be reused multiple times should be decided by considering the transport environment to minimize the packaging cost.

5.6.2 For the sake of efficiency during holding and transport, it is preferable to have only one or two cushions per secondary container.

5.6.3 The materials for the cushions should be recyclable after the designated number of uses is completed.

5.7 *Pallet*

5.7.1 Pallets must be stand-alone components and are not integrated with secondary containers.

5.7.2 Considering space efficiency of ocean freight containers, it is preferable that the pallet size be 1130 mm max on at least one side.

5.7.3 Palletized containers must be banded and film-wrapped.

5.7.4 Pallet material must meet transportation industry requirements and allow for reuse and recycle after end of useful life.

5.7.5 Pallets must be able to be accessed by a forklift from at least two directions.

5.8 *Shipment Documentation*

5.8.1 English should be used for all international shipment documentation. The local language may be used only for domestic shipments only.

5.8.2 Packing list and customs invoice (if required) should be located on the outside of container number 1 with a sufficient number of copies to ensure the customer receives one copy.

5.8.3 Customs invoices must meet appropriate government regulations. Key content items are: PO number, product description, price, shipping address, and cross-reference to packing list.

5.8.4 The packing list must contain: date, customer shipping address, supplier name, country of origin, PO number, customer part number, shipment quantity, total number of cartons, carton identifiers.

5.8.5 The certificate of analysis or conformance should be electronically transmitted from wafer supplier to customer. Electronic transmission format must be flexible to allow for future content changes.

5.9 *Transportation Logistics*

5.9.1 Small quantity shipments or expedited shipments may require a special secondary container size.

5.9.2 The 300 mm wafer shipping system design must comprehend both surface and air transportation.

APPENDIX 1

NOTICE: This appendix was approved as an official part of SEMI M45 by full letter ballot procedure, but the recommendations in this appendix are optional and are not required to conform to this standard.

A1-1.1 The 300 mm Wafer shipping box must be re-usable in view of the wafer manufacturing cost and environmental concerns.

A1-1.2 When the shipping box is re-used, the customer who received wafers must keep the shipping box in good condition after opening the package and return to the wafer supplier.

A1-1.3 The box cleaning process of the supplier can not remove ink, adhesive, and excessive metal contamination of the returned shipping box.

A1-1.4 The customers must avoid contaminating the shipping boxes in this way. The customers must keep the shipping box separate from those contaminated conditions. Contaminated shipping boxes must not be returned to the supplier.

SEMI M46-1101[E]
TEST METHOD FOR MEASURING CARRIER CONCENTRATIONS IN EPITAXIAL LAYER STRUCTURES BY ECV PROFILING

This test method was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the European Compound Semiconductor Materials Committee. Current edition approved by the European Regional Standards Committee on June 29, 2001. Initially available at www.semi.org December 2001; to be published March 2002.

[E] This document was editorially modified in November 2001 to correct a typographical error. A change was made to Section 7.3.3.

1 Purpose

1.1 The purpose of this document is to specify a method to measure the carrier concentration and carrier concentration vs. depth profile of epitaxial layers by Electrochemical Capacitance Voltage ECV profiling.

2 Scope

2.1 This test method covers a procedure for measuring the carrier concentration of epitaxial layers by ECV profiling. This method focuses on improving the accuracy and repeatability of the measurement by standardizing the test conditions and reporting and by routine calibration of the measurement.

2.2 This test method is intended to cover the majority of routine samples measured. However, because of the number of different materials encountered it cannot cover every contingency.

2.3 This standard may involve hazardous materials. This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI C1 — Specifications for Reagents

3.2 *ASTM Standards*

D1125-95 (1999) — Standard Test Methods for Electrical Conductivity and Resistivity of Water

4 Terminology

4.1 *bias* — the potential applied to the sample with respect to a reference electrode.

4.2 *capacitance voltage CV measurements* — electrical measurements where the capacitance of a rectifying barrier is measured as a function of applied bias and is a measure of the net fixed ionized charge per unit volume.

4.3 *carrier concentration* — the net fixed ionized charge per unit volume. Equal to the free carrier concentration if the dopant is fully ionized and the material is free of traps.

4.4 *current voltage IV measurements* — electrical measurements where the current through the rectifying barrier is measured as a function of applied bias.

4.5 *dissipation factor* — the ratio of the real part to the imaginary part of the complex admittance. It is a measure of the non-ideality of the barrier.

4.6 *electrochemical* — chemical reaction in which charge transfer takes place via an external circuit.

4.7 *epitaxial layer* — a layer of single crystal semiconductor material grown on a host substrate which determines its orientation.

4.8 *excess area* — the difference between the wetted and illuminated areas.

4.9 *flatband potential* — the intercept on the voltage axis of the $1/C^2$ vs V plot. A measure of the built in field or barrier height.

4.10 *illuminated area* — the area of the sample which can be illuminated during electrochemical etching.

4.11 *rectifying barrier* — a potential gradient formed at the junction between two materials which permits the flow of charge in one direction only.

4.12 *reference electrode* — half cell which has a constant electrode potential, such as a saturated calomel electrode, SCE.

4.13 *rest potential* — the open circuit potential of the sample with respect to the reference electrode.

4.14 *wetted area* — the area of contact between the electrolyte and the sample.

5 Summary of Method

5.1 In this method, the carrier concentration of the epitaxial layer is measured by the CV method.

5.1.1 Ohmic contacts are formed on the sample.

5.1.2 A rectifying barrier, of known contact area, is formed by placing the sample in contact with an electrolyte.

5.1.3 The quality of the barrier is assessed using I-V and C-V measurements.

5.1.4 From the measured C-V data the carrier concentration of the layer is determined.

5.1.5 The sample is anodically etched to produce a new barrier deeper in the material. The etch depth is determined using Faraday's law of electrolysis.

5.1.6 Sections 5.1.4 and 5.1.5 are repeated to generate a carrier concentration vs. depth profile.

6 Interferences

6.1 *Thin Layers* — Diffusion of carriers into adjacent regions set a fundamental resolution limit to the measurement. In addition if the layer has a high sheet resistivity this can also affect the value obtained.

6.2 Double Layer Capacitance — A limitation imposed by the physical nature of the electrolyte/semiconductor barrier which sets an upper limit to the measured carrier concentration, for accurate measurements, of 1×10^{19} cm^{-3}. The technique can be used beyond this value, but with progressive degradation.

6.3 *Etch Well Uniformity*

6.3.1 *Etch Well Flatness* — Non-uniformity increases the effective area and may result in the measurement not being wholly made in the layer of interest. The main causes of non-uniformity are gas bubbles, inadequate electrolyte circulation and uneven illumination.

6.3.2 *Etch Well Roughness* — indicates poor etching and has a deleterious effect on the measurements. Generally overcome by selecting a more appropriate electrolyte and/or etching conditions.

6.4 *Non-Ideal Electrical Characteristics*

6.4.1 *Series Resistance* — From the contacts, sample and electrolyte affect the accuracy of the measurements. This effect is minimized by using a highly conductive electrolyte, making large area ohmic contacts and by employing a low measurement frequency.

6.4.2 *Leakage Currents* — Parallel conduction can affect the accuracy of the measurement. Its influence is reduced by employing a high measurement frequency.

6.4.3 *Large Excess Area* — Can give rise to errors on n-type material particularly when profiling Hi-Lo structures. The excess area is electrolyte dependent but is mainly affected by the quality of the seal used to define the area. Large excess areas indicate a poor seal and are corrected by replacing the seal.

6.5 *Hi-Lo Structures* — Measurement is subject to inaccuracy due to carrier diffusion and excess area errors. For accurate measurements, chemically etch to the layer of interest before measurement.

6.6 *Contact Quality* — Non-Ohmic or high resistance contacts have a deleterious effect on the measurement. Contacts should be checked by measuring the resistance between two similar contacts and then reversing the current direction and repeating the measurement.

6.7 *Surface and Deep States* — Cause the measured capacitance to be frequency dependent and/or dependent on the rate at which the bias is changed. Usually resolved by using a high measurement frequency. This should not be confused with the frequency dependence which is more usually attributed to high series resistance.

6.8 *Surface Films* — Have a deleterious effect on the capacitance measurement. Film formation should be avoided by using an appropriate electrolyte, control of the etching bias and time and by electrolyte circulation.

6.9 Surface Roughness — The surface of the sample should be smooth and free of features that would affect the action of the seal.

6.10 *Light* — Light can affect the capacitance measurement, so the sample must be placed in a dark environment during the measurement.

6.11 *Sample Loading* — The accuracy of the measurement depends on the repeatability of the area. If a compliant seal is involved, such as a plastic ring, the sample should be held in contact with the seal by applying a controlled and constant force. No relative lateral movement should take place during the loading process.

6.12 *Ring Variability* — The condition of the ring has a large effect on the measurement. Good seals will have a small to zero excess area and exhibit a well defined and reproducible contact area.

7 Apparatus

7.1 *Measurement of Etch Well and Ring Areas* — Measuring microscope with either an XY stage, with a linear resolution of 0.01 mm or better, or a camera and image processing system capable of measuring an area of 0.1 cm^2 to better than 0.5%.

7.2 *Measurement of Etch Well Flatness* — (Optional) A means such as a stylus profiler for checking the flatness and roughness of the etch well. In most cases visual inspection of the etch well, for a mirror like appearance, is sufficient indication of low roughness.

7.3 *Instrumentation*

7.3.1 *Capacitance Meter* — Capable of measuring values up to 300 nF, employing a test signal of amplitude less than 100 mV RMS. The measurement frequency should be typically between 1 and 100 kHz.

7.3.2 *Equivalent Circuit Model* — The meter should assume a parallel circuit model for the electrolyte/semiconductor interface and provision should be made to compensate for the large series resistance of the electrolyte and contacts.

7.3.3 *Potentiostat* — Capable of maintaining the potential of the sample with respect to a reference electrode constant to ±5mV during the measurement and with a reference input impedance of > 10^{13} Ohms.

7.3.4 *Light Source* — A source of uniform illumination of above band gap energy for etching n-type materials.

7.4 *Sample Holder*

7.4.1 *Electrochemical Cell* — Used to hold the sample, contain the electrolyte and support the sealing ring and other electrodes, see Figure 1.

7.4.1.1 *Sealing Ring* — A corrosion resistant ring which forms a seal between the electrolyte and the sample. This ring defines the measurement area which should be reproducible and well defined. The ring area should not be less than 0.008 cm^2 and the reproducibility between runs should be better than ± 3%. Large ring areas (typically ≥ 0.1 cm^2) are preferred for more accurate measurements.

7.4.1.2 *Reference Electrode* — Used to control the sample bias via a potentiostat.

7.4.1.3 *Counter Electrode* — The bias and test signals are applied between this electrode and the sample.

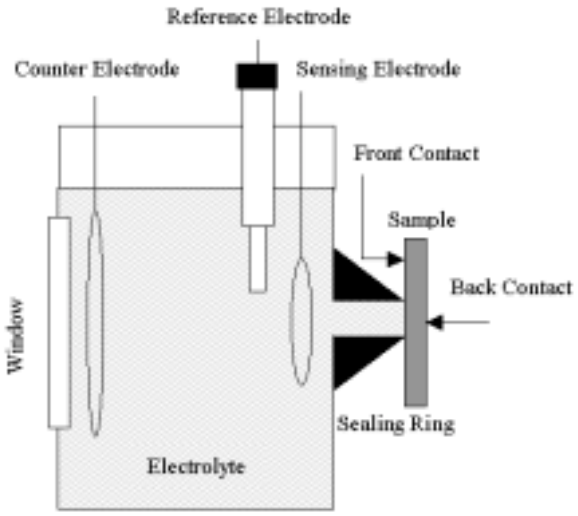

Figure 1
Electrochemical Cell

7.4.1.4 *Sensing Electrode* — Placed close to the sample-electrolyte interface and used to measure the admittance of the sample.

7.4.1.5 *Sample Contacts* — Ohmic contacts to the front and/or back surface of the sample for the purpose of applying bias.

8 Reagents and Materials

8.1 *Purity of Reagents* — All chemicals for which such specifications exist shall conform to SEMI C1.

8.2 *Purity of Water* — Use either distilled or de-ionized water having a resistivity greater than 2 MOhm•cm at 25°C as determined by the Non-Referee Test of Test Methods D 1125.

8.3 *Selection of Electrolyte* — The choice of electrolyte is not defined by this standard and is up to the discretion of the user or by agreement between the customer and the supplier.

8.3.1 *InP, GaAs and Related Compounds* — Preferred electrolyte, Na_2.EDTA (0.1 M) basified with ethylenediamine to a pH of 10, although other electrolytes can be satisfactorily used.

NOTE 1: Preferred electrolyte, see reference "Electrochemical C-V Profiling of Heterojunction Device Structures" A.C.Seabaugh et al. IEEE Trans on Electron Dev 36 No 2 (1989) 309-313.

9 Safety Precautions

9.1 The electrolytes used are potentially hazardous. Read the Materials Safety Data Sheets before attempting to prepare the electrolytes. Use safety

eyewear, rubber gloves and protective clothing. Prepare all electrolytes in a fume hood.

9.2 Ensure that all electrolytes are correctly labeled.

10 Specimen Preparation

10.1 The sample should be free from surface debris and scratches. The sample should be cleaned with deionized (DI) water and dried.

10.2 To measure a single layer or upper layer of a multilayered structure, no additional sample preparation is required.

10.3 For a buried layer in a multilayered structure, measurement accuracy is improved by removing the overlaying layers by either the use of selective or controlled chemical etches.

10.4 If the upper layers cannot be removed by chemical etching then the sample can be profiled electrochemically but in some cases this may reduce the accuracy of the method.

10.5 For conducting substrates Ohmic contacts should be made to either the front or back of the wafer. For insulating substrates an Ohmic contact should be made to the front of the epilayer. Contacts are formed electrically, by alloying or by any other suitable method. The quality of the contact should be verified electrically.

11 Calibration and Standardization

11.1 *Sealing Ring* — Calibration of the sealing ring areas is performed using a "blue slice", made by growing an anodic oxide film on a polished n-type substrate.

11.1.1 The "blue slice" is profiled according to this test method. Etch only the minimum amount necessary to see the illuminated area (typically 0.5 μm). Flush the cell several times with DI water before removing the sample. Wash and measure the sample as soon as possible.

11.1.2 *Wetted Area* — The wetted area is observed due to chemical attack of the oxide film and is measured using a measuring microscope with cross hair eye-pieces and micrometer XY stage or by using a zoom camera and image processing system.

11.1.3 *Illuminated Area* — Etches in the light and forms a well defined etch well, which is measured as per the wetted area.

11.1.4 *Calibration Interval* — Regularly check the area and condition of the sealing ring. For daily use, the ring areas should be calibrated at least three times a week.

11.1.5 *Replacement* — Rings should be replaced if the excess area exceeds 10% for rings of area ≤ 0.05 cm^2 or 5% for rings of area > 0.05 cm^2 or if the perimeter is not uniform.

11.1.6 *Alternative Calibration Method* — The areas can be measured using known n and p-type test samples. This method is best suited for continual monitoring of the ring area between "blue slice" calibrations.

11.2 *Instrumentation* — The bias voltage, measurement frequency and capacitance measurement should be checked annually.

11.2.1 *Bias* — The bias voltage should be checked with a DVM with an input impedance > 1 MOhm.

11.2.2 *Capacitance* — The capacitance measurement should be checked using calibrated fixed value capacitors covering the expected sample capacitance range or from 1–100 nF.

11.2.3 *Frequency* — The measurement frequency should be checked with a frequency counter.

12 Measurement Procedure

12.1 *Choice of Electrolyte* — An electrolyte should be selected that forms a rectifying barrier with the sample, gives a flat, mirror finish etch well and generates only a small excess area.

12.2 *Sample Mounting* — A region of the sample should be defined which will form the rectifying contact with the electrolyte. This area can be defined by some form of sealing ring or mask, but it is important that the area of contact between the electrolyte and the sample be precisely known and remain constant during the measurement.

12.2.1 *Sealing Ring* — If the sample is pressed against a sealing ring, the seal must be cleaned with DI water and dried before positioning the sample. If the sample needs repositioning, the sample and sealing ring should be recleaned and dried.

12.2.2 *Ring Loading* — As the mounting pressure may effect the reproducibility of the measurement and the lifetime of the sealing ring, it must be controlled (e.g. by the reproducible use of a suitable compression spring).

12.3 *Cell Filling and Debubbling* — Fill the cell, which holds the sealing ring and other measurement electrodes, with the electrolyte. The process of filling the cell frequently traps bubbles of air on the surface of the sample. These bubbles must be removed before a measurement can be made.

12.4 *Contact Evaluation* — Verify that the contacts, for both directions of current flow have low and approximately equal resistance.

12.5 *Rest Potential* — Measure the sample's rest potential to verify that the reference electrode and sample are electrochemically stable. Its value usually lies between 0 and −1 V (respective to a SCE reference electrode). Values outside this range can indicate a problem with the sample or reference electrode.

12.6 *Cable Compensation* — Determine any stray capacitance or additional resistance associated with the cell and test leads that would impact the measurement.

12.7 *Current vs. Voltage (I-V)* — Used to select the bias for measurement and etching and as a general test of material quality.

12.7.1 *Measurement Bias* — is set in the reverse bias, low dark current region.

12.7.2 *Etching Bias (p-type material)* — is set in the forward bias region. The abruptness of the forward bias breakdown is indicative of the ohmic nature of the contacts. No or shallow forward breakdown often indicates unsuitable ohmic contacts.

12.7.3 *Etching Bias (n-type material)* — is set in the reverse bias, low dark current region. Illumination should result in a significant increase in current (photo-current).

12.8 *Capacitance vs. Voltage (C-V)* — Used to evaluate the quality of the electrochemical diode and to select a range of possible measurement voltages. The measured flatband potential (respective to a SCE reference electrode) should lie between −0.5 and −2.5 V for n-type semiconductors and between –1 and +1 V for p-type semiconductors.

12.8.1 *Measurement Bias* — is set in a region of low dissipation, where the $1/C^2$ vs V plot is linear. For layers grown with concentration gradients, the latter condition cannot be strictly adhered to and in such cases the amplitude of the test signal, used for capacitance measurement, should be kept as small as possible.

12.8.2 *Dissipation* — The normally accepted safe level is < 0.4.

12.8.3 *Excess Area Capacitance* — For n-type surface layers the capacitance of the electrolyte/semiconductor interface is measured prior to etching and the capacitance associated with the excess area is computed by multiplying the measured capacitance by the ratio of the excess area to the wetted area.

12.9 *Carrier Concentration Profiling* — Profile the sample using the etching and measurement conditions determined from the I-V and C-V data.

12.9.1 *Carrier Concentration* — The carrier concentration is determined from the C-V data.

12.9.2 *Excess Area Correction* — For n-type material the capacitance associated with material in the excess area should be subtracted from the measured capacitance.

12.9.3 *Etching* — The sample is anodically etched at the etching bias. The depth of the etch well is determined from the time integral of the current using Faraday's law of electrolysis.

12.9.4 *Profiled Depth* — The profile assumes that the measured carrier concentration lies at a depth equal to the sum of the etch and the depletion depths.

12.10 *Ring Area* — It is advised to measure the etch well area after profiling and to use this value to recalculate the carrier concentration vs. depth profile.

13 Calculations and Interpretation of Results

13.1 *Carrier Concentration,* N

The principle of this method is based on measuring the slope of $1/C^2$ vs V.

$$N = \frac{-2}{q\varepsilon_0\varepsilon_r A^2}\cdot\left[\frac{d\left(1/C^2\right)}{dV}\right]^{-1} \qquad [\text{cm}^{-3}]$$

where

C is the measured capacitance (for n-type material the capacitance associated with the excess area should be subtracted from the measured capacitance),
V is the applied bias,
q is the electronic charge,
ε_r is the relative permittivity of the sample,
ε_o is the permittivity of free space
(= 8.854×10^{-12} Fm^{-1})
A is the area of the etch well

It is also possible to measure dC/dV by modulating the bias with a low frequency (secondary signal). The $d(1/C^2)/dV$ of the upper equation may be evaluated to result in the following formula.

$$N = \frac{1}{q\varepsilon_0\varepsilon_r A^2}\cdot\frac{C^3}{dC/dV} \qquad [\text{cm}^{-3}]$$

13.1.1 *Excess Area Capacitance,* C_{excess}

$$C_{excess} = C.\frac{A_w - A_i}{A_w} \qquad [\text{F}]$$

Where

C_{excess} is the capacitance of material in the excess area,

A_w is the wetted area,

A_i is the illuminated area

13.2 *Depletion Depth*, W_d, — calculated from the parallel plate capacitor equation.

$$W_d = \frac{\varepsilon_0 \varepsilon_r A}{C} \qquad [\mu m]$$

13.3 *Etched depth*, W_e, — calculated from the charged passed through the cell using Faraday's law for electrolysis.

$$W_e = \frac{M}{zFDA} \int Idt \qquad [\mu m]$$

Where

z is the effective dissolution valency,
F is the Faraday constant,
($= 9.65 \times 10^4$ Cmol^{-1})
D is the density of the semiconductor,
M is the molecular weight of the semiconductor
I is the etch current

13.4 *Total depth*, W, — the sum of the depletion and etch depths and is the depth at which the measurement is made.

$$W = W_d + W_e \qquad [\mu m]$$

14 Reporting Results

14.1 The following information shall be included in the report:

14.1.1 *Identification of Specimen* — including details of any pretreatment such as the use of a selective etch to chemically etch the sample to the layer of interest.

14.1.2 *Sealing Ring Area* — both the wetted and illuminated areas should be reported.

14.1.3 *Electrolyte* — the composition of the electrolyte should specify the molecular concentration.

14.1.4 *Material Constants* — The relative permittivity of the sample, ε_r and the effective dissolution valency, z.

14.1.5 *Primary Measurement Signal* — the frequency and amplitude of the signal used for the capacitance measurement.

14.1.6 *Secondary (bias) Signal* — If the measurement is made using a secondary modulation component its frequency and amplitude should be reported. If the measurement is made by changing the bias, its minimum and maximum value should be specified.

14.1.7 *Measurement Bias* — The average value (DC component) of the bias used during the capacitance measurement.

14.1.8 *Electrochemical Etching Bias* — The bias used to etch the sample including whether or not the sample was illuminated. If etched at a constant current this should be stated. Then it is not necessary to report the bias.

14.1.9 *Electrochemical Etching Current* — If etched at constant bias the average value of current measured during electrochemical etching. If etched at a constant current the value used.

SEMI M47-0704
SPECIFICATION FOR SILICON-ON-INSULATOR (SOI) WAFERS FOR CMOS LSI APPLICATIONS

This specification technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved by the Japanese Regional Standards Committee on April 30, 2004. Initially available at www.semi.org June 2004; to be published July 2004. Originally published November 2001; previously published March 2002.

1 Purpose

1.1 This specification defines thin-layer silicon-on-insulator (SOI) wafer requirements for CMOS large scale integrated circuit (LSI) devices. In another aspect, this specification defines the generic characteristics of SIMOX and bonded silicon-on-insulator wafers having typically no more than 0.2 μm SOI layer thickness. By defining parameters, inspection procedures and acceptance criteria, both users and suppliers may uniformly define product characteristics and quality requirements.

2 Scope

2.1 This specification is specifically directed to SIMOX and bonded silicon-on-insulator wafers, which are exclusively used for LSI applications made up of CMOS devices.

2.2 A complete purchase specification requires the base silicon wafer, SOI surface and layer, and buried oxide layer properties detailed in this standard, suitable test methods for their characterization. SEMI M18 may be for purchase specification purpose.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Integrated Circuit (IC) Applications

SEMI M18 — Format for Silicon Wafer Specification From for Order Entry

SEMI M22 — Specifications for Dielectrically Isolated (DI) Wafers

SEMI M34 — Guide for Specifying SIMOX Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M41 — Specification of Silicon-on Insulator (SOI) for Power Device/ICs

SEMI MF26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconductor Materials

SEMI MF84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Standard Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Standard Test Methods for Dimensions of Notches on Silicon Wafers

SEMI MF1188 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

SEMI MF1241 — Standard Test Methods for Terminology of Silicon Technology

SEMI MF1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1526 — Standard Test Method for Measuring Surface Metal Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence Spectroscopy

SEMI MF1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1619 — Standard Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at Brewster Angle

SEMI MF2074 — Standards Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.2 *ASTM Standards*[1]

E122 — Practice for Choice of Sample Size to Estimate Average Quality of a Lot or Process

F1620 — Standard Practice for Calibrating a Scanning Surface Inspection System Using Monodisperse Polystyrene Latex Spheres Deposited on Polished or Epitaxial Wafer Surfaces

3.3 *JEITA Standards* [2]

JEITA EM-3602 — Standard Specification for Dimensional Properties of Silicon Wafers with Specular Surface

JEITA EM-3504[3] (JEIDA 61 in old version) — Standard Test Method for Interstitial Atomic Oxygen of Silicon by Infrared Absorption

JEITA EM-3505 — Height calibration in 1 nm order for AFM

3.4 *ANSI Standard* [4]

ANSI/ASQCZ1.4 — Sampling Procedure and Tables for Inspection

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Many terms relating to silicon technology are defined in ASTM Terminology F 1241. Other terms are defined as below.

4.2 *Abbreviations and Acronyms*

4.2.1 *BOX* — buried oxide layer

4.2.2 *SIMOX* — separation by implanted oxygen

4.3 *Definitions*

4.3.1 *bonded interface* — the plane where the bonding between handle and device wafers takes place.

4.3.2 *bonded wafer* — an SOI wafer made by bonding two silicon wafers with an insulating layer between them. The insulating layer is typically thermally grown oxide.

4.3.3 *BOX pin-hole* — electrically conductive path through the BOX.

4.3.4 *buried oxide layer* — the silicon dioxide layer between SOI layer and base silicon substrate.

4.3.5 *handle wafer or base silicon wafer or base silicon substrate* — the substrate which structurally supports the BOX and the SOI layer.

4.3.6 *HF defect* — defect in the SOI layer decorated by immersing the wafer in HF for a certain time.

4.3.7 *non-SOI edge area* — an annulus between the nominal radius of the surface silicon layer and the nominal radius of the base silicon wafer (for bonded SOI wafers). The annulus which implies an area is determined by its width as one dimension. It is the difference in the nominal radius of the surface silicon layer and the base silicon wafer.

4.3.8 *SIMOX wafer* — SOI wafer made by oxygen implantation technology

4.3.9 *SOI etch pit* — defect in an SOI layer decorated by immersing the wafer in Secco etch solution.

4.3.10 *SOI layer or surface silicon layer* — the silicon layer on the BOX of the SOI wafer.

4.3.11 *void* — local absence of SOI layer and/or BOX in bonded wafer.

5 Ordering Information

5.1 Purchase orders for SIMOX or bonded silicon-on-insulator wafers furnished to this specification shall include the following items:

- Characteristics for the SOI layer (thickness, crystal orientation, dopant, etc.)
- Characteristics for the base silicon substrate (thickness, crystal orientation, dopant, etc.)
- Characteristics of the buried oxide (thickness, dielectric breakdown voltage, etc.)
- Misalignment of wafer orientation between the SOI layer and the handle wafer

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

2 Japanese Electronic and Information Technology Industries Association, Tokyo Chamber of Commerce and Industry Bldg. 2-2, Marunouchi 3-chome, Chiyoda-ku, Tokyo 100-0005, Japan. Website: www.jeita.or.jp

3 Since a new number is assigned, it will be published soon. Until then, an old version spec number is to be referred.

4 American National Standards Institute, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023 Website: www.ansi.org

- Sampling plan and lot acceptance procedures (see Section 7)
- Methods of test and measurements (see Section 8)

6 Requirement

6.1 Requirements of SOI wafers consists of a base silicon wafer specification part and an SOI wafer specification part. A base silicon wafer is specified based on a SEMI M18 format. A similar format is applied for the specification of an SOI wafer.

6.2 As a minimum, the base silicon wafer shall conform to SEMI M1 and the appropriate individual polished monocrystalline silicon wafer standard; i.e. JEITA EM-3602.

6.3 SOI wafer specified items and test methods are listed in Table 1 and shall not exceed the limits as given in Table 1.

Table 1 Specification of SOI Wafers for CMOS LSI Applications

	Item	*Specification Units*		*Standard reference*	*Test method*
		SIMOX	*Bonded*		
Base Silicon Wafer					
1. GENERAL CHARACTERISTICS					
1.1	Growth Method	CZ	CZ		
1.2	Crystal Orientation	(100) ± 1°	(100) ± 1°	SEMI MF26	X-ray diffraction
1.3	Conductivity Type	P-type	P-type	SEMI MF42	Hot point probe
1.4	Dopant	Boron	Boron		
1.5	Edge Exclusion, Nominal	3 (mm)	3 (mm)		
2. ELECTRICAL CHARACTERISTICS					
2.1	Resistivity (Center Point)	See NOTE 1.	See NOTE 1.	SEMI MF84	4-point probe
3. CHEMICAL CHARACTERISTICS					
3.1	Oxygen Concentration	See NOTE 1.	See NOTE 1.	SEMI MF1188, SEMI MF1619, JEITA EM-3504	IR absorption
4. STRUCTURAL CHARACTERISTICS					
4.2	Slip	None	None	SEMI MF523	Visual inspection
4.3	Lineage	None	None	SEMI MF523	Visual inspection
4.4	Twin	None	None	SEMI MF523	Visual inspection
4.5	Swirl	None	None	SEMI MF523	Visual inspection
4.6	Shallow Pits	None	None	SEMI MF523	Visual inspection
5. WAFER PREPARATION CHARACTERISITICS					
5.1	Wafer ID	See NOTE 1.	See NOTE 1.		
5.4	Extrinsic Gettering Treatment	See NOTE 1.	See NOTE 1.		
6. MECHANICAL CHARACTERISTICS					
6.1	Nominal Diameter	150 / 200 (mm)	150 / 200 (mm)	SEMI MF2074	
	Diameter Tolerance	≤ ± 0.2 (mm)	≤ ± 0.2 (mm)	SEMI MF2074	
6.2	Primary Flat Length/Notch Dimension	SEMI M1 or JEITA EM-3602	SEMI M1 or JEITA EM-3602		
6.3	Primary Flat/Notch Orientation	[011] ± 1°	[011] ± 1°	SEMI MF671, SEMI MF1152	
6.6	Edge Profile	SEMI M1	SEMI M1	SEMI MF928	
6.6.1	Edge Surface Finish	See NOTE 1.	See NOTE 1.	SEMI MF928	
6.7	Thickness	SEMI M1 or JEITA EM-3602	SEMI M1 or JEITA EM-3602	SEMI MF533	Thickness gauge
6.8	Thickness Variation (TTV)	SEMI M1	SEMI M1	SEMI MF533	Thickness gauge
6.14	Flatness Site	See NOTE 1.	See NOTE 1.		

	Item	*Specification Units*		*Standard reference*	*Test method*
		SIMOX	*Bonded*		
		(Refer to SEMI M18.)	(Refer to SEMI M18.)		
8. FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS					
8.01	Specified according to SEMI M1 Table 1			SEMI MF523	Visual inspection
9. BACK SURFACE VISUAL INSPECTION CHARACTERISTICS					
9.01	Specified according to SEMI M1 Table 1			SEMI MF523	Visual inspection
SOI Wafer					
25. SOI LAYER CHARACTERISTICS					
25.0	Type of SOI	SIMOX	Bonded		
25.1	Growth Method	CZ	See NOTE 1.		
25.2	Surface Silicon Thickness	≤ 0.2 (μm) See NOTE 1.	≤ 0.2 (μm) See NOTE 1.		Spectroscopic ellipsometry, Spectroscopic reflectometry
25.3	Surface Silicon Thickness Mean Value Variation	≤ ± 5 (nm)	≤ ± 5 (nm) See NOTE 2.		Spectroscopic ellipsometry, Spectroscopic reflectometry
25.4	Surface Silicon Thickness Variation in Wafer	≤ ± 3 (nm)	≤ ± 7.5 (nm) See NOTE 2.		
25.5	Crystal Orientation	(100) ± 1°	(100) ± 1°	SEMI MF26	X-ray diffraction
25.6	Rotation Misalignment	NA	≤ ± 1°		Visual
25.7	Edge Exclusion, Nominal	5 (mm) See NOTE 3.	5 (mm) See NOTE 3.		
25.8	Non-SOI Edge Area	NA	≤ 3 (mm)		Visual
25.9	Conductivity Type	P-type	P-type	SEMI MF42	
25.10	Dopant	Boron	Boron		Secondary ion mass spectroscopy
25.11	Dopant Concentration	See NOTE 1.	See NOTE 1.		Secondary ion mass spectroscopy
25.12	SOI Etch Pit	$< 1 \times 10^6$ (/cm^2)	$< 1 \times 10^4$ (/cm^2)		Secco's etching
25.13	Threading Dislocation	$< 5 \times 10^4$ (/cm^2) (LD) $< 5 \times 10^5$ (/cm^2) (HD)	NA		Secco's etching
25.14	HF Defect	< 0.5 (/cm^2)	< 0.5 (/cm^2) (150 mmϕ) < 0.3 (/cm^2) (200 mmϕ)		HF etching
25.15	Void	NA	See NOTE 1.		Visual, Automated particle counter
25.16	Roughness (Si surface) rms @ 2 × 2μm	< 0.4 (nm)	< 0.2 (nm)	JEITA EM-3505	Atomic force microscope
25.17	Surface Metal Contamination (Fe, Cr, Ni, Cu)	$< 5 \times 10^{10}$ (/cm^2) for each atom	$< 5 \times 10^{10}$ (/cm^2) for each atom	SEMI MF1526	TXRF AAS, ICP-MS

	Item	Specification Units		Standard reference	Test method
		SIMOX	Bonded		
26. BOX CHARACTERISTICS					
26.1	BOX Thickness	≤ 0.4 (μm) See NOTE 1.	≤ 0.4 (μm) See NOTE 1.		Spectroscopic ellipsometry, Spectroscopic reflectometry
26.2	BOX Thickness Variation	≤ ± 5 (%)	≤ ± 5 (%)		Spectroscopic ellipsometry, Spectroscopic reflectometry
26.3	Bonded Interface Location	NA	See NOTE 1.		
26.4	BOX Pinholes	< 0.5 (/cm^2) (LD) < 0.1 (/cm^2) (HD)	< 0.1 (/cm^2)		Cu plating, BOX capacitor
26.5	Dielectric Breakdown	> 5 (MV/cm)	> 6 (MV/cm)		BOX capacitor
27. MECHANICAL CHARACTERISTICS					
27.1	Warp	< 40 (μm) (LD) < 50 (μm) (HD)	< 40 (μm)	SEMI MF1390	Automated noncontact scanning
27.2	Flatness-site	See NOTE 1. (Refer to SEMI M18.)	See NOTE 1. (Refer to SEMI M18.)		
28. FRONT SURFACE VISUAL INSPECTION CHARACTERISTICS					
28.1	Scratch	None	None	SEMI MF523	Visual inspection
28.2	Haze	None	None	SEMI MF523	Visual inspection
28.3	LLS @particle size	≤ 0.3 (/cm^2) @ > 0.25 μm	≤ 0.3 (/cm^2) @ > 0.2 μm	SEMI MF523	Automated particle counter
28.4	Slip	See NOTE 1.	See NOTE 1.	SEMI MF523	Visual inspection
28.5	Edge Chip	SEMI M1	SEMI M1	SEMI MF523	Visual inspection
28.6	Edge Crack	SEMI M1	SEMI M1	SEMI MF523	Visual inspection
28.7	Foreign Matter	See NOTE 1.	See NOTE 1.	SEMI MF523	Visual inspection
29. BACK SURFACE CHARACTERISTICS					
29.1	Backside Metal Contamination (Fe, Cr, Ni, Cu)	< 1 × 10^{11} (/cm^2) for each atom	< 1 × 10^{11} (/cm^2) for each atom		AAS, ICP-MS

NOTE 1: to be specified or discussed between users and suppliers

NOTE 2: typically 0.1 μm and thicker SOI are specified. Thinner SOI is to be discussed between users and suppliers.

NOTE 3: It is specified by a distance from the FQA boundary to the periphery of a base wafer of nominal dimensions. It is not a distance from an edge of an SOI layer.

NA: not applicable

LD: Low dose SIMOX with BOX thickness ≤ 200 nm

HD: High dose SIMOX with BOX thickness > 200 nm

7 Sampling Plan

7.1 Unless otherwise specified, ASTM Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned with an acceptable quality level (AQL) of lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between users and suppliers.

8 Test Methods

8.1 *Thickness of Surface Silicon Layer and Buried Oxide Layer*

8.1.1 *Measurement Methods* — Two non-contact, non-destructive optical characterization techniques, spectroscopic ellipsometry (SE) and spectroscopic

reflectometry, have proven useful both for surface silicon layer and buried oxide (BOX) layer thickness measurements. Both techniques use reflected light to allow deduction of the thickness and refractive index of thin layers. In both cases, layer thickness and index of refraction data must be "backed out" of the measured optical data by a process of successive approximation. Silicon islands in the BOX layer of SIMOX and interface non-uniformity make these techniques less reliable.

8.1.1.1 *Spectroscopic Ellipsometry (SE) Measurement* — In this measurement, white light from a xenon arc lamp passes through a polarizing rotating filter and illuminates the sample site under study; reflected light passes through an analyzer to a monochrometer and photomultiplier detector. For each wavelength, reflectivity oscillates with polarizer rotation; the magnitude and phase of reflectivity changes are measured to determine ellipsometric angles, δ and Ψ. The two measured spectra are fit by successive approximation to allow determination of the surface silicon layer and BOX layer thickness and oxide composition. For SE, the choice of instrument and associated model and fitting parameters affect the confidence-of-fit, so they should be taken into account in the user-supplier agreement.

8.1.1.2 *Spectroscopic Reflectometry Measurement* — In this measurement, light from a xenon arc lamp passes through a grating monochrometer or optical band-pass filters and illuminates the sample site under study; reflected light is gathered by a detector. Specular reflectivity is plotted as a function of wavelength from 0.4 μm to 1.1 μm. The analysis proceeds by making successively better approximations to index of refraction and absorption of each layer until an acceptable fit is achieved. Measurements are made with a reflectance mode optical interferometer.

8.1.1.3 *Optical Model Fitting and Correlation* — There are slight, systematic differences between layer thickness measured by SE and spectroscopic reflectometry. Because of this, users and suppliers should specify the actual measurement method to be used. The two methods offer results which are reproducible and well-correlated with each other over a wide range of conditions. If both measurement techniques are used, it is recommended that the reflectance system measurements should be calibrated to fit the results of the SE.

8.1.2 *Measurement Positions* — The measurement strategy is to make a detailed measurement with an accurate fit on at least nine wafer sites, for example, the wafer center, four points at half of the wafer radius and four points at 10 mm from the wafer edge. The number and position of wafer sites to be monitored should be agreed on between users and suppliers. Generally, the greater the variability relative to the mean, the larger the number of sites that should be monitored. In each case, the measurement system supplies a "goodness-of-fit" parameter that indicates a level of confidence in the fit to the measured data.

8.1.3 *Surface Silicon Layer and Buried Oxide (BOX) Layer Thickness* — Spectra for each site are fit independently with both the surface silicon and BOX layer thickness as adjustable parameters. Both the mean thickness and the uniformity should be specified.

8.1.4 *Surface Silicon Thickness Mean Value Variation*

8.1.4.1 After surface silicon layer thickness is measured for predetermined number of wafers and mean value of surface silicon thickness is derived for each wafer, the maximum and the minimum values are chosen, and then the variation (nm) is calculated as;

± (Maximum mean value – Minimum mean value) / 2

8.1.4.2 In case of quite large number of wafers (ex. a few hundreds), the variation (mm) can be calculated as;

$\pm 3\sigma$ (3 times of the standard deviation)

under agreement between users and suppliers.

8.1.5 *Surface Silicon Thickness Variation in Wafer*

8.1.5.1 After surface silicon layer thickness is measured at predetermined number of points within an SOI wafer, the maximum and the minimum values are chosen, and then the variation (nm) is calculated as ;

± (Maximum value – Minimum value) / 2

8.1.5.2 In case of multi-points measurements (ex. a few hundreds) within an SOI wafer, the variation (nm) can be calculated as;

$\pm 3\sigma$ (3 times of the standard deviation)

under agreement between users and suppliers.

8.1.6 *Buried Oxide (BOX) Thickness Variation*

8.1.6.1 After BOX thickness is measured for predetermined number of points on predetermined number of wafers, the maximum and the minimum values are chosen, and then the variation (%) is calculated as;

± (Maximum value – Minimum value) × 100 / (2 × mean value)

8.1.6.2 In case of multi-points measurements (ex. a few hundreds) within an SOI wafer or quite large number of wafers (ex. a few hundreds), the variation (%) can be calculated as;

$\pm 3\sigma$ (3 times of the standard deviation) × 100 / (mean value)

under agreement between users and suppliers.

8.2 *Dopant Concentration*

8.2.1 Secondary Ion Mass Spectroscopy (SIMS) is utilized to determine dopant concentration in surface silicon layer.

8.2.2 The acceptable dopant concentrations are to be determined by agreement between users and suppliers.

8.3 *Defects in Surface Silicon Layer*

8.3.1 *SOI Etch Pit*

8.3.1.1 Defects in surface silicon layer including stacking faults, threading dislocations and other crystal defects are evaluated by destructive chemical etching and microscopic etch pit density measurements. The appropriate evaluation procedure for SOI wafers, which depends on type of defects targeted and thickness of surface silicon layers, is determined by agreement between users and suppliers.

8.3.1.2 Following are examples of the evaluation on SIMOX wafers and bonded wafers.

8.3.1.3 *Example 1* — SOI etch pit evaluation in SIMOX wafers: Samples are first immersed in HF to remove oxide from the surface. Then the samples are etched by Secco etch. In the case of a relatively thick SOI layer such as 170–200 nm, freshly prepared standard Secco Etch can be used: one part (by volume) of a 0.15 molar solution of $K_2Cr_3O_7$ in distilled water and two parts HF (49%). In the case of a thin SOI layer below 100 nm, the samples are etched for 30 seconds in the solution[5]: 50 ml of HF (49%) plus 80 ml of HNO_3 (61%) plus 160 ml of H_2O [$K_2Cr_2O_7$ 1g + $Cu(NO_3)_2{\cdot}3H_2O$ 4g] (a sort of diluted Secco etch). For both cases, the etching should continue until 50 nm of the surface Si remains. After the etching and rinsing in water, samples are dipped in HF (49%) for 5 minutes. The HF etches the buried oxide and creates cavities under the etch pits. The number of etch pits is counted through optical microscope. The etch pits include various defects such as threading dislocations and stacking fault pyramid.

8.3.1.4 *Example 2* — SOI etch pit evaluation in bonded SOI wafers fabricated by delamination followed by CMP: SOI etch pit density increases when remaining SOI thickness after Secco etching is thinner and thinner. SOI layers thicker than 150 nm are usually etched down to 50 nm by Secco etching before SOI etch pits are counted. These pits are detected when selectively etched depth or the size of defects is larger than SOI layer thickness remaining after Secco etching. Thus, damages deeper than 50 nm or defects larger than 50 nm can be detected. These pits come from defects contained in original silicon material and/or damages or defects induced in SOI fabrication process. The former includes COP, bulk micro defects, oxygen precipitates, and so on. The latter includes CMP damages, defects induced by heat cycles and so on, as possibility. To define origins of SOI etch pits, their distribution in depth of SOI layers and/or that on a wafer should be evaluated. For example, CMP damages may be localized on surface of SOI layers. By etching SOI surfaces up to desired depth with using non-selective etching such as KOH followed by Secco etching, etch pits due to CMP damages disappear. The depth distribution of defects or damages can be evaluated in this manner.[6]

8.3.1.5 *Example 3* — SOI etch pit evaluation in bonded SOI wafers formed by epitaxial layer transfer technology: In this case, there is no COP, bulk micro defects, and oxygen precipitates in the SOI layer because it is made of epitaxially grown Si on porous Si. In addition, mechanical damage related defect is not introduced, since the SOI surface is smoothed out by hydrogen annealing instead of polishing. The major defect in this type of SOI wafers is same sided pyramidal stacking fault, that is induced at the initial stage of the epitaxy, and is grown through the epitaxy with upside-down pyramidal shape[7], and then is turned upside-down again by bonding. This defect is decorated as the etch pit by standard or diluted Secco's etching as described in Example 1 in conjunction with HF dipping. It is enough to etch until 50 nm of the SOI layer remaining to etch the defect portion through the SOI layer selectively by the defect etching such as Secco etching because the stacking fault penetrates through the SOI layer. The following HF dipping etches the BOX through the etch pit to form large cavity. It helps to count low density of defects in a wide observation area with low magnification microscope.

8.3.2 *Threading Dislocation*

8.3.2.1 The etching of the SIMOX sample shown above in Section 8.3.1.3 (Example 1) is terminated when the remaining surface silicon layer thickness is 1/3–1/2 of the initial thickness and then dipped in HF as the same manner as Example 1. In this case the etch pits include mainly threading dislocations only which can be counted through optical microscope.

8.3.3 *HF Defect*

8.3.3.1 Measurement of the microscopic etch pit density following an HF etch is commonly used to disclose defects in SOI material. Pitting of surface

5 L. F. Giles, A. Nejim, and P. L. F. Hemment, *Materials Chemistry and Physics*, vol.35, p. 129, 1993.

5 K. Mitani, H. Aga, and M. Nakano, *Jpn. J. Appl. Phys.* vol.36, p. 1646 1997.

7 N. Sato, K. Sakaguchi, K. Yamagata, Y. Fujiyama, J. Nakayama, and T. Yonehara, *Jpn. J. Appl. Phys.* vol.35, p. 973 (1996).

silicon may be present before the HF etch or be caused by HF etching. For this destructive measurement, a whole wafer or at least one quarter of a wafer should be used. The sample is placed in concentrated (49%) HF for 10 to 15 minutes or diluted (e.g. 25%) HF for longer time (e.g. 3 to 4 hours), then removed, rinsed and dried. If there are pits or voids and/or metal particles or silicides formed in the surface silicon layer, the HF etches the metals/silicides and then etch the buried oxide. This results in local etching of BOX with 25−50 μm diameter (depending on the HF concentration and the etch time) centered on the original defects. The defect density is then measured in an optical microscope using a 5× objective and 10× eyepiece or comparable setup. The samples should be scanned for whole surface within edge exclusion boundary.

8.3.4 *Void*

8.3.4.1 Voids are determined as an unbonded area on bonded SOI wafers. See SEMI M41. Because SOI layer in thin bonded SOI wafers are typically 0.2 μm thick or thinner, void areas are broken and SOI layers as well as BOX are usually absent. By this reason, voids are specified as local absence of SOI layers and/or BOX in bonded wafers in this specification.

8.3.4.2 *Visual inspection* — Under visible light, the edge of voids is detected because the edge area is step-shaped due to absence of SOI layers and/or BOX layers. See Section 8.8 for inspection conditions.

8.3.4.3 *Detection as large LLS* — The edge of local absence of SOI layer and/or BOX scatters light. Therefore, voids are detected as large LLS. See Section 8.7.2 for the principle. A size of LLS corresponding to various sizes of voids should be calibrated or correlated by comparison of defects one by one using a microscope.

8.4 *Surface Roughness*

8.4.1 *AFM (Atomic Force Microscope)* — By contacting the probe equipped with the cantilever onto the wafer surface of the sample, and by scanning the cantilever and detecting the variation by optical method, the roughness information is obtained. A tapping mode is commonly used.

8.5 *Metal Contamination*

8.5.1 The surface metal contamination can be measured by TXRF, AAS and ICP-MS methods.

8.5.2 *TXRF (Total X-Ray Fluorescence)* — Total X-ray Fluorescence uses a low angle incident, and a tightly collimated X-ray beam excites the characteristic X-rays from impurity atoms near the sample surface. Usually, the angle of X-ray incidence is less than 0.1 degree. The element identification and the amount of the element can be obtained by measuring energy and intensities of fluorescence X-ray. The instrument provides a map of impurity element distribution. Surface roughness may change metal detection sensitivity. Thus, calibration is suggested before samples with deferent level of roughness, e.g. back surface, are measured. A reference for details is SEMI MF1526.

8.5.3 *AAS (Atomic Absorption Spectroscopy)*

8.5.3.1 The elemental characteristic absorption of the atom is measured by introducing sample solution as aerosol into the flame and then spectral absorption through the flame from the light source is detected by the spectrometer. The flameless method, superior to the flame method in the sensitivity, is now broadly used.

8.5.3.2 *Sample Preparation* — Careful sample preparation is necessary for the precise measurement. SOI wafer surface is exposed to HF vapor, and metals on the surface are collected as droplet. To improve sensitivity, the volume of collective solution should be as small as possible and HF drops are rolled all over the surface in collective operation. In case of precious metals, it is better to use other kinds of collective solutions instead, since they are not dissolved or collected by HF solution itself.

Examples:

1. For Cu ; HF-H_2O_2 (HF (50 wt.%) : H_2O_2 (31 wt.%): H_2O = 1 : 17 : 82 volume ratio)
2. For Au and Pt ; aqua regia (HNO_3 (68 wt.%) : HCl (36 wt.%) = 1 : 3 volume ratio)

8.5.4 *ICP-MS (Inductively Coupled Plasma Mass Spectroscopy)*

8.5.4.1 ICP-MS is composed of ICP (Inductively Coupled Plasma) part as an ion source and MS (Mass Spectrometer) part, which measures the ions generated at ICP part. Usually, sample solution is vaporized in the nebulizer and then finally introduced into Argon plasma in the silica tube called torch through the spray chamber. The sample is decomposed, evaporated, atomized and then ionized in the Argon plasma. Except for few atoms that have relatively high ionization potential, most of the elements (> 90%) can be ionized. Ions are identified and measured in amount by the mass spectrometer.

8.5.4.2 *Sample Preparation* — The same method as AAS method is applicable. In case of quantitative measurement of Fe, since its mass weight is close to that of ArO^+, it is necessary to pay attention to degradation of detection sensitivity.

8.6 *BOX Defect*

8.6.1 *BOX Pinhole Measurement-1 (by $CuSO_4$ plating or copper decoration)*

8.6.1.1 BOX pinhole evaluations shall be made by $CuSO_4$ plating or copper decoration methods. They can be also evaluated by BOX capacitor dielectric breakdown, the details of which are explained later in *BOX Pinhole Measurement-2*.

8.6.1.2 In evaluation by $CuSO_4$ plating method, the sample wafer is placed (front face down) on a paper towel soaked in 20% $CuSO_4$ solution on top of a copper plate. An aluminum plate is placed on the back of the wafer. The copper plate is grounded, and −25 V_{DC} is applied to the aluminum plate. Small leakage currents (sub-μA) through pinholes in the BOX cause copper to plate out onto the towel with the density same as BOX pinhole density.

8.6.1.3 In evaluation by copper decoration method, an SOI layer is first etched off by KOH solution to expose a BOX layer. Then the wafer is immersed in methanol and brought downward into direct contact with the gold-coated cathode. A copper mesh as an anode is immersed in the liquid 5 mm above the wafer. Required voltage is applied, such as the electric field in the buried oxide layer is 1 MV/cm. The voltage is measured at the oxide surface with a surface voltage probe. Localized copper decorations at pinhole sites in the oxide are observed with a low power optical microscope.

8.6.2 *BOX Capacitor Dielectric Breakdown* — This parameter can be measured with BOX capacitor. The BOX thickness affects both the test procedure (such as capacitor area and voltage criterion) and the allowable values of measured parameters. These should be determined by agreement between users and suppliers.

8.6.2.1 *Test Structure* — BOX capacitor utilizing mesa-etched SOI layers and Si substrates for both electrodes to apply electric field to the embedded buried oxide is used. The area of capacitor, which affects the breakdown voltage, should be determined by agreement between users and suppliers. Typical capacitor area is 0.01–0.1 cm^2. The electrode material and thickness affect the breakdown phenomena due to thermal effects, and so should be included in the agreement.

8.6.2.2 *Test Method: Staircase I-V Measurement* — Voltage is stepped in one-volt increments from zero to until destructive breakdown is sensed. The test detects the onset of high field conduction, as well as the point of destructive or massive charge injection and trapping.

8.6.3 *BOX Pinhole Measurement-2 (by Dielectric Breakdown)*

8.6.3.1 Buried oxide pinhole can be detected also by BOX capacitor.

8.6.3.2 *Test Structure* — BOX capacitor having an area equal to or greater than 0.05 cm^2.

8.6.3.3 *Test Method: Staircase I-V* — Measurement testing can be done for both Type I and Type II defects where Type I defects are silicon pipes traversing the buried oxide, and Type II defects are local regions of thin buried oxide. If Type II defect density is sought, capacitors are subjected to a series of 30 voltage steps of 3.3 volts, with current monitored after each step, using a failure criterion of 1 nA.

8.6.3.4 Any capacitor displaying the failure current or more for applied field less than 2 MV/cm is considered defective. Defect density of either type is calculated from the yield of good capacitors, (Y = 1 – # failed/# tested), using Poisson statistics;

$$D = -1n\,(Y)/A,$$

where A is the total area of the capacitors tested.

8.7 *Particle (LLS : Localized Light Scatterer)*

8.7.1 *Light Scattering Tomography* — The particle larger than predetermined threshold size is counted by an automated particle counter.

8.7.2 *Principle of Measurement* — By scanning the laser beam on the wafer surface, the light scattered by particles on a wafer is detected. The scattered light and the noise from the wafer surface is detected as a direct current, on the other hand, the scattered light by the particles can be detected as pulse components. The particle size can be calibrated with standard polystyrene latex spheres. SOI wafers usually have scattering noise from the layer interface. It is necessary to reduce incident angle of the laser beam to increase the reflective component from the surface. For example, S/N ratio is improved when using S-polarized light of 10 degree incident, 85% of its component is reflected from silicon surface.

NOTE 2: Detailed procedure of size calibration with standard polystyrene latex spheres: Refer to ASTM F1620.

NOTE 3: Measurement procedure should be determined by agreement between users and suppliers.

8.8 *Visual Inspection* — SOI wafer can be visually inspected in accordance with SEMI MF523. The automatic inspection equipment is also used when available. For visual inspection, the collimated high intensity bright light (e.g. 500,000 lux) is used. Under using this light, SOI wafer is inspected for haze, slip,

scratches, chips, cracks, pits, dimples, mound, orange peel, voids, LLS and contamination.

NOTICE: SEMI makes no warranties or representations as to the suitability of the standard set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI M48-1101
GUIDE FOR EVALUATING CHEMICAL-MECHANICAL POLISHING PROCESSES OF FILMS ON UNPATTERNED SILICON SUBSTRATES

This guide was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on August 27, 2001. Initially available at www.semi.org September 2001; to be published November 2001.

1 Purpose

1.1 The purpose of this document is to provide a guide for evaluation of chemical-mechanical polishing (CMP) processes of thin films on unpatterned silicon substrates. This includes recommended procedures for process testing and reporting formats.

1.2 This guide is intended for use by both suppliers and end users.

2 Scope

2.1 This document provides a guide for evaluating a CMP process for films deposited or grown on an unpatterned silicon substrate. These evaluations could include tests with fixed polishing time, fixed removal rate, fixed ending thickness, time-dependent material removal, and others.

2.2 Recommended procedures for characterizing a CMP process are discussed in this guide.

2.3 This guide suggests selected parameters and values of the properties of the starting monitor wafer.

2.4 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability or regulatory limitations prior to use.

3 Limitations

3.1 The guide does not address evaluation of CMP processes for films on patterned substrates.

3.2 Evaluation of surface quality or surface contamination is not addressed in this document. Surface quality and surface contamination are important aspects of the CMP process evaluation but they are beyond the scope of this guide.

3.3 This guide employs sample standard deviation to estimate variation.

3.4 Wafer positioning precision on a metrology tool can affect the precision of the polishing evaluation. This issue is not addressed in this standard.

3.5 The values derived from the calculations in this guide are sample-dependent. They are affected by measurement location and number of observations.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E89 — Guide for Measurement System Capability Analysis

SEMI M1 — Specifications For Polished Monocrystalline Silicon Wafers

SEMI M11 — Specifications For Silicon Epitaxial Wafers For Integrated Circuit (IC) Applications

SEMI M20 — Specification for Establishing a Wafer Coordinate System.

4.2 *ASTM Standards*[1]

F 534 — Test Method for Bow of Silicon Slices

F 1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

F 1530 — Test Method for Measuring Flatness, Thickness and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

F 1618 — Standard Practice for Determination of Uniformity of Thin Films on Silicon Wafers.

4.3 *DIN Standards*[2]

DIN 50441/4 — Prüfung von Materialen für die Halbleitertechnologie; Messung der geometrischen Dimensionen von Halbleiterscheiben; Scheibendurchmesser und Flattiefe. (Measurement Determination of the Geometric Dimensions of Semiconductors Slices [including] Diameter and Flat Depth)

NOTE 1: Unless otherwise indicated, all documents cited shall be the latest published versions.

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

2 DIN Standards, Deutsches Institut fur Normung e.v., available from Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-1000 Berlin 30, Germany

5 Terminology

5.1 *blanket polish* — polishing of material deposited on an unpatterned silicon substrate.

5.2 *diameter scan* — measurements of material on a wafer taken along a specified diameter. The diameter scan is useful in determining the thickness profile of the material on the wafer surface.

5.3 *edge scan* — measurements of material taken along a specified radial segment in the edge region of the wafer. A series of edge scans can be employed to determine circumferential thickness profile.

5.3.1 *Discussion* — the data density for edge scan measurements is generally higher than for other measurements. Combining a low-density diameter scan in the central region of the wafer with a higher-density edge scan, taken along the same scan line, can improve throughput with appropriate local measurement data density.

5.4 *film total thickness variation (film TTV)* — the total thickness variation ($Thk_{max} - Thk_{min}$) of film material among a set of measurement points.

5.4.1 *Discussion* — The variation may pertain to a region within a wafer, a complete wafer or multiple wafers with a single polish head, or multiple wafers with multiple polish heads. These wafer and head combinations must be considered in planning and comparing measurements. If one assumes that a given wafer is polished by a subset of the tool heads (typically one), a hierarchical relationship exists such that wafers must be associated with the (tool head) subsets used to polish them. Another way to look at this is, if *head* is considered an experimental treatment, then a wafer polished by one head will be assumed to be treated differently than a wafer polished by a different head. This relationship leads to what is known as a hierarchic or nested model. (In this case, one says that wafer is nested within *head*). A more complete model would also treat *head* as a fixed effect, *wafer* random and nested within *head*, and error as nested with *head* and *wafer*. A random effect indicates that the observation comes from a random sample of a larger population. *Head* is a fixed effect because the entire population of heads (i.e., all the heads on the tools) constitutes the entire population of interest. Given this model, variance components would be used to estimate the different sources of variation. In this case, the sample standard deviation underestimates the population standard deviation. Historically, the expected value of the variance components is equal to the population standard deviation. This is not the case for the sample standard deviation.

5.5 *head to head removal rate non-uniformity (HTHNU)* — this metric is useful when evaluating polishing processes on a multi-head tool configuration. It is the standard deviation (1σ) of the removal rate variation from polish head (HTH) to polish head for a fixed number of wafers where the number of wafers run for each head must be equal. It is expressed as follows:

$$HTHNU = \sqrt{\frac{\sum_{k=1}^{p} (\overline{RR_k} - \overline{\overline{RR_{HTH}}})^2}{p-1}} \quad 1)$$

Where k is the head indexer and p is the total number of heads. $\overline{RR_k}$ is the average within wafer removal rate of head k. $\overline{\overline{RR_{HTH}}}$ is the head to head wafer removal rate averaged across all wafers and all heads. The measurement site locations on each wafer must be identical for all wafers sampled.

It may also be expressed as a percentage of the average head to head removal rate:

$$\%\ HTHNU = \frac{\sqrt{\frac{\sum_{k=1}^{p} (\overline{RR_k} - \overline{\overline{RR_{HTH}}})^2}{p-1}}}{\overline{\overline{RR_{HTH}}}} \times 100 \quad 2)$$

5.6 *removal rate (RR)* — the amount of material removed per unit time during the polish process. At any given point i on the wafer, the removal rate is expressed by

$$RR_i = \frac{Thk_{pre_i} - Thk_{post_i}}{Polish\ \ time} \quad 3)$$

5.7 *thickness, prepolish (Thk_{pre})* — the thickness of material on an incoming blanket film wafer prior to polish.

5.8 *thickness, post-polish (Thk_{post})* — the thickness of material remaining at a measurement site on a silicon substrate after completion of the polish process.

5.9 *wafer to wafer (WTW) variation* — the variation across multiple wafers at site locations where the locations on each wafer are identical for all wafers sampled.

5.10 *wafer to wafer removal rate nonuniformity (WTWNU)* — a measure of the wafer to wafer removal rate variation. It is the standard deviation (1σ) of the removal rate variation wafer to wafer over a polish run

that employs a single polishing head. The average removal rate for such a group of wafers is expressed as:

$$\text{Average WTW RR} \Rightarrow \overline{\overline{RR}_{WTW}} = \sum_{j=1}^{m} \frac{\overline{RR_j}}{m} \quad 4)$$

where *j* is the wafer indexer and *m* is the total number of wafers within the group. A typical number for m is ≥ 25.

The measurement site locations on each wafer must be identical for all wafers sampled. The wafer-to-wafer removal non-uniformity is expressed as follows:

$$WTWNU = \sqrt{\frac{\sum_{j=1}^{m} \left(\overline{RR}_{WIW} - \overline{\overline{RR}}_{WTW}\right)^2}{m-1}} \quad 5)$$

It may also be expressed as a percentage of the average wafer to wafer removal rate:

$$\%\ WTWNU = \frac{\sqrt{\frac{\sum_{j=1}^{m} \left(\overline{RR}_{j_{WIW}} - \overline{\overline{RR}}_{WTW}\right)^2}{m-1}}}{\overline{\overline{RR}}_{WTW}} \times 100 \quad 6)$$

5.11 *within wafer average removal rate* — the average removal rate within a wafer. It is given as

$$\text{Average WIW RR} \Rightarrow \overline{RR}_{WIW} = \sum_{i=1}^{n} \frac{RR_i}{n} \quad 7)$$

where *i* is the site indexer and *n* is the total number of measurement sites within the wafer, and RR_i is within wafer removal rate.

5.12 *within wafer removal rate nonuniformity (WIWNU)* — a measure of removal rate variation. It is the standard deviation (1σ) of the removal rate within the wafer and is expressed as follows:

$$WIWNU = \sqrt{\frac{\sum_{i=1}^{n} \left(RR_i - \overline{RR}_{WIW}\right)^2}{n-1}} \quad 8)$$

where *i* is the site indexer, *n* is the total number of measurement sites on the wafer and $\overline{RR_{WIW}}$ is the average within wafer removal rate. It may also be expressed as a percentage of the average removal rate:

$$\%\ WIWNU = \frac{\sqrt{\frac{\sum_{i=1}^{n} \left(RR_i - \overline{RR}_{WIW}\right)^2}{n-1}}}{\overline{RR}_{WIW}} \times 100 \quad 9)$$

5.13 *within wafer (WIW) variation* — the variation in measurement values obtained at defined locations within a single wafer.

6 CMP Process Test

6.1 *Introduction*

6.1.1 The CMP process test should be performed with attention to the quality of both the substrate and the incoming film material, and the relative condition of the consumables and polishing system being utilized.

6.1.2 The number of wafers within the group should be specified.

6.2 *Monitor Wafer*

6.2.1 Monitor wafer specifications should be per SEMI M1 for incoming bow, warp, total thickness variation (TTV), and edge profile.

6.2.2 The geometry of the wafer may influence the CMP process results. Tables R-1 and R-2 in Related Information 1 recommend specifications for wafer geometry that can minimize the effects of such geometry on the CMP process test.

6.2.3 Record bow, warp and other wafer geometry characteristics.

6.2.4 Wafers can be laser-marked for ease of tracking. Data taken in this mark area should be excluded from the process analysis. It is desirable that all wafers in an evaluation lot contain marks at the same nominal locations.

6.3 *Incoming Film Properties*

6.3.1 Record the incoming film type and deposition tool and, where applicable, the deposition process conditions.

6.3.2 Ascertain that the incoming film thickness is sufficient to prevent polishing through to the substrate. See Tables R-1 and R-2 in Related Information 1 for recommended values for incoming film thickness.

6.4 *Post-process Measurements*

6.4.1 Record bow, warp and the same other wafer geometry characteristics determined in Section 6.2.3.

NOTE 2: These post-process measurement values may vary arbitrarily relative to the pre-process values.

6.4.2 Record final film thickness in the same locations employed for the starting film.

6.4.3 Calculate global and local film thickness changes appropriate for the application of interest.

6.5 *Metrology tools*

6.5.1 Select a film thickness measurement system suitable for the film and sampling pattern to be characterized.

6.5.1.1 Perform a gauge study on each metrology tool accordance with SEMI E89 to determine its effectiveness for the films to be measured.

6.5.2 Ascertain that the metrology tool is operating properly under Statistical Process Control prior to use in the CMP process test.

6.5.3 Perform tool calibration in accordance with the tool supplier's instructions.

6.6 *CMP Consumables*

6.6.1 Identify all consumables including pad, insert film, slurry type, and conditioning end effector.

6.6.2 Record the manufacturer's part number and lot number (if available) of each consumable item.

6.6.3 Record the status and history of each consumable prior to starting the process test.

NOTE 3: The history of consumables can affect the CMP process test.

6.6.4 Perform break-in procedures for pad and carrier film as required to ensure stable operation. Base these break-in procedures on recommendations from the consumable supplier.

6.7 *Polishing Tool*

6.7.1 Calibrate and record polish downforce, alignment tolerances, velocity, fluid dispense rates and other operational parameters based on recommended procedures from the equipment manufacturer.

6.7.2 Polish the samples.

7 Measurement Locations on the Wafer

7.1 The number and location of measurement sites are specific to the process test. In general, locations should be evenly spaced. Data extrapolation beyond the boundary of the measurement site population should not be performed.

7.2 ASTM F 1618 covers a set of site distribution patterns for measuring the uniformity of a thin film on a silicon wafer, similar to Figures 2 – 5, as well as simple procedures for analyzing and reporting the results of those measurements. For edge-scan measurements, see Section 7.3.6 below. For spiral-scan measurements, see Section 7.3.7 below. For full-wafer, high-density measurements, see Section 7.3.10 below.

7.3 Select one of these patterns for CMP process analysis on unpatterned wafers, unless otherwise agreed to.

7.3.1 Sampling plans are based on concentric circles, spirals, Cartesian sites, partial-radius, and partial and single-diameter sites.

7.3.2 Measurements are made at the sites specified in the chosen sampling plan, using the appropriate instrumentation and measurement procedure for the film parameter of interest.

7.3.3 Measures of the dispersion of the values are obtained by simple statistics specified for the sampling plans.

7.3.4 For diagonal scan measurements, refer to Figure 1. Select values for each of the following scan parameters:

- Scan Angle, θ
- Scan Radius Start/Stop, r_1 / r_2
- Number of Measurement Points, n, across the diameter.

7.3.5 For edge scan measurements, refer to Figure 6. Select values for each of the following scan parameters:

- Scan Angle, θ
- Inner Scan Radius, r_1
- Outer Scan Radius, r_2
- Number of Measurement Points, n, between r_1 and r_2.

NOTE 4: These n measurement sites are uniformly distributed.

7.3.5.1 *Discussion* — the data density for edge scan measurements is generally higher than for other measurements. Combining a low-density diameter scan in the central region of the wafer with a higher-density edge scan, taken along the same scan line, can improve throughput with appropriate local measurement data density.

7.3.6 For spiral scan measurements, refer to Figure 7. In such scans, the measurements are evenly distributed from near the center ($r = 0$) to near the edge exclusion boundary ($r = 1 – EE$). For each successive point, both the radius and the angle θ are systematically changed. For the 200 mm example with 3 mm edge exclusion shown in Figure 7, the 81 measurement points start at

R_1 = 0.10 mm and θ_1 = 0.52°. Successive points are incremented with ΔR = 1.21 mm and $\Delta\theta$ = 1.16°.

NOTE 5: Spiral scans uniformly sample properties that are radially symmetrical. These scans apply equal weight to all measurement sites. They also provide radial information, similar to diameter scans, as well as additional theta-related information that may not be provided by diameter scans.

7.3.7 For concentric circle scans, refer to Figures 2 and 3. In these scans, the inner circles lie on a fraction of the nominal radius. For notched wafers, the outer circle lies on a radius equal to the nominal radius less the edge exclusion, which is conformal with the notch on notched wafers. For flatted wafers the outer circle lies on a radius equal to the nominal radius less the sum of the flat depth plus the edge exclusion.

7.3.8 For Cartesian measurement scans, refer to Figure 4.

7.3.9 For full-wafer measurements, the measurements sites are evenly spaced over the entire area being examined. Typically, the first point is the wafer center, and the remaining measurement sites are equally spaced about the wafer center in X and Y. This X-Y grid is similar to Figure 4, but with significantly higher spatial density.

7.4 Record and identify the measurement site locations in accordance with SEMI M20.

7.4.1 Include an illustration of these locations with the test setup and with the recorded data set.

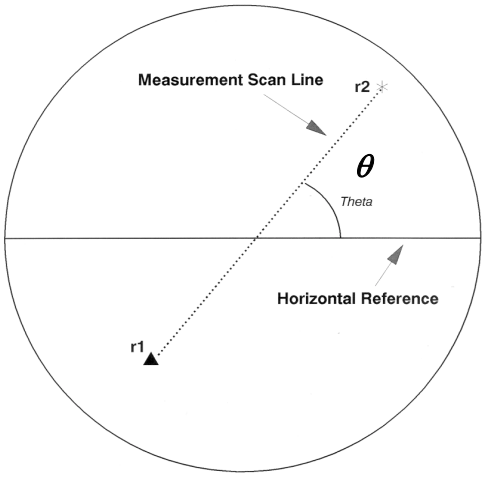

Figure 1
Diameter Scan
θ = scan orientation; r_1, r_2 = scan start/stop

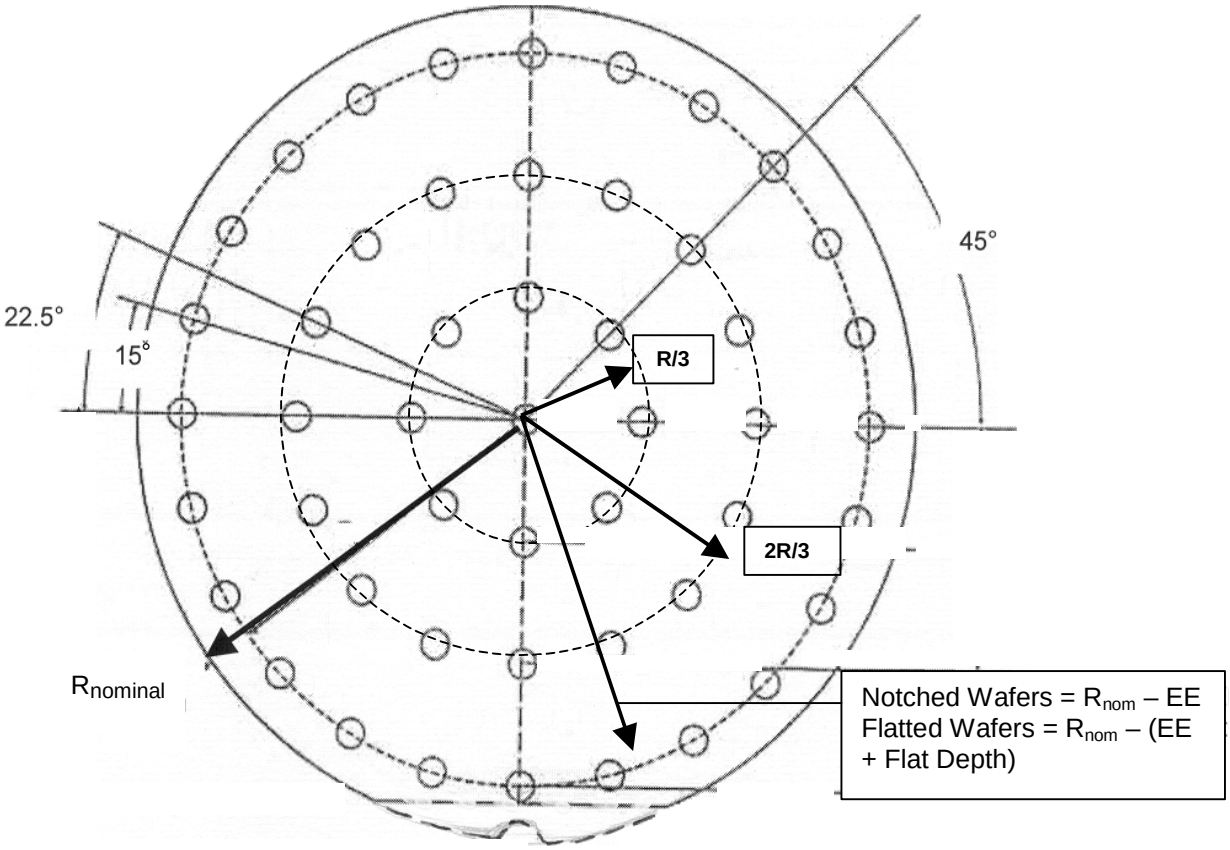

Figure 2
Three Concentric Circles

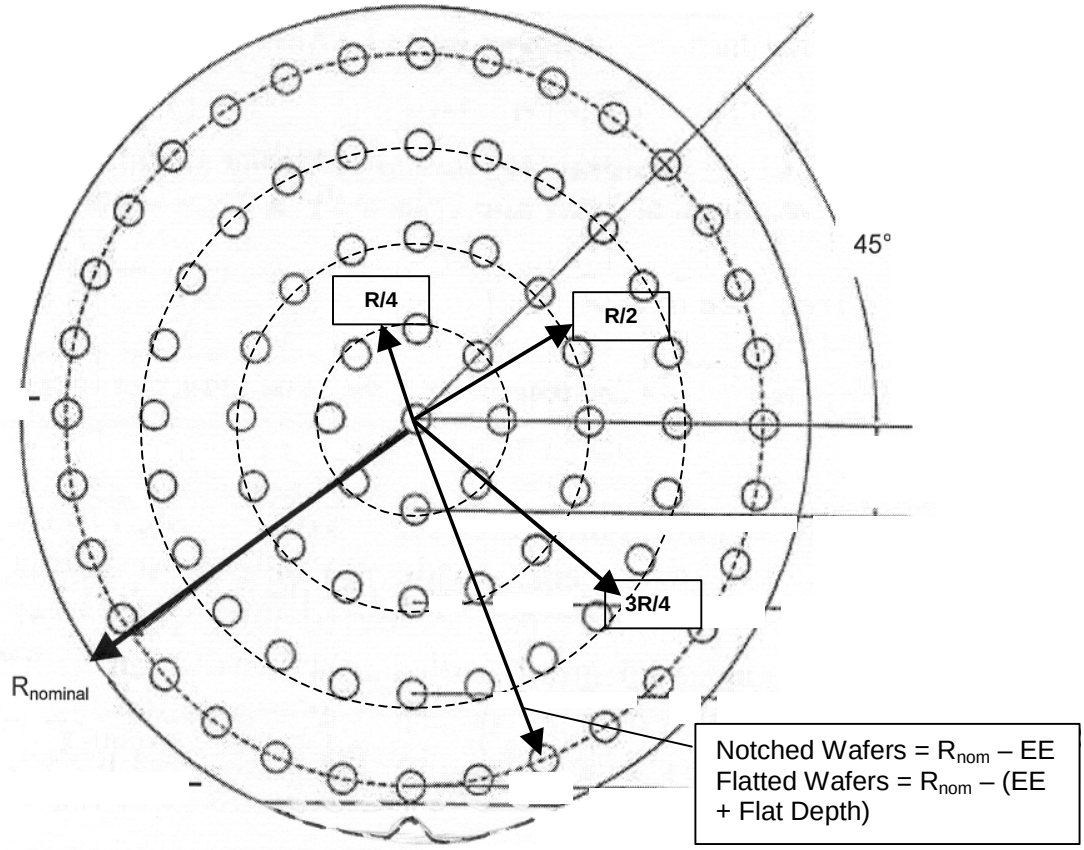

Figure 3
Four Concentric Circles

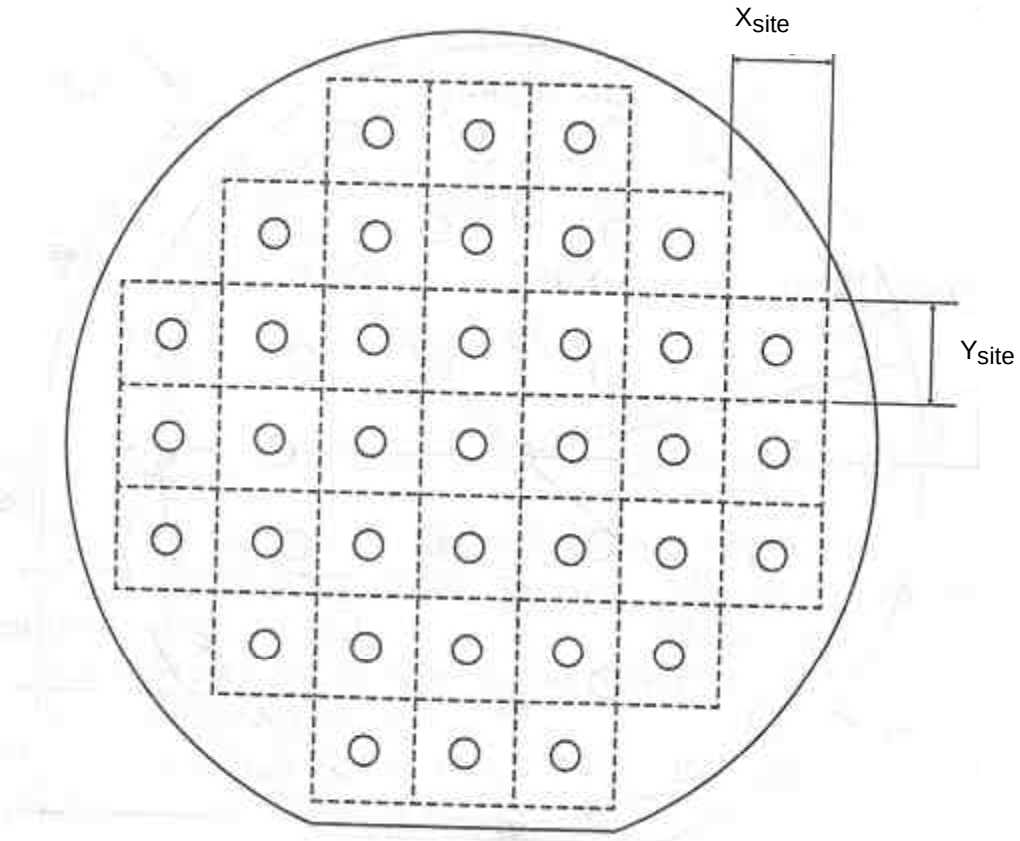

Figure 4
Cartesian Measurement Site Patterns

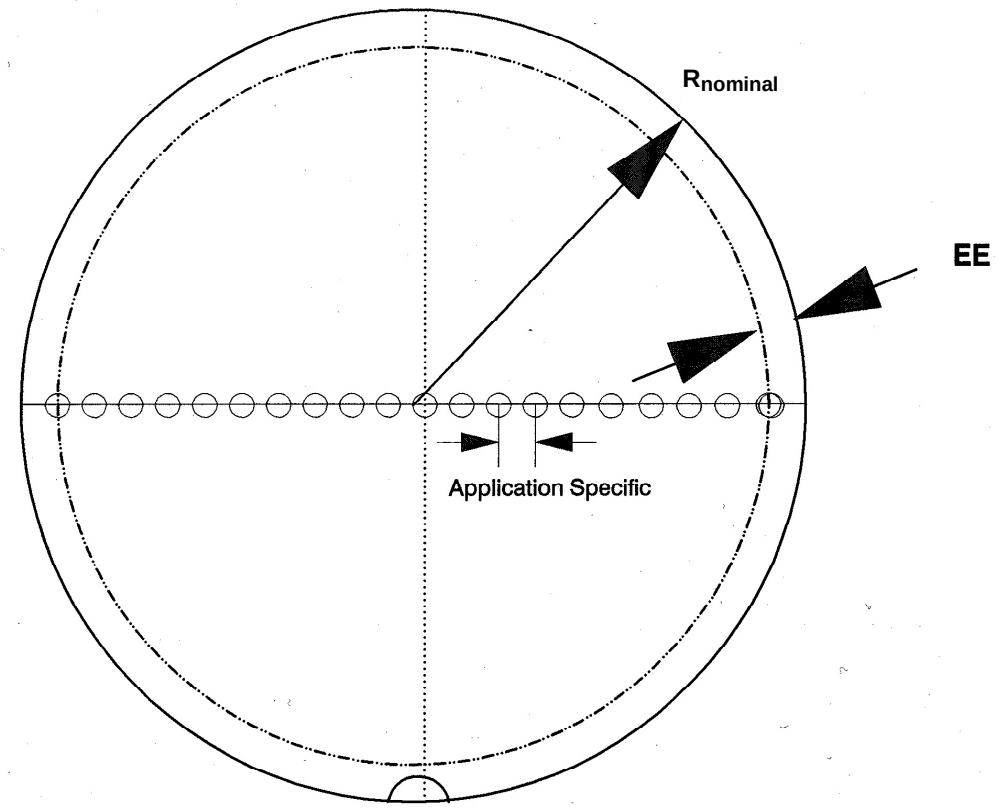

Figure 5
Single-Diameter High-Density Measurement Sites

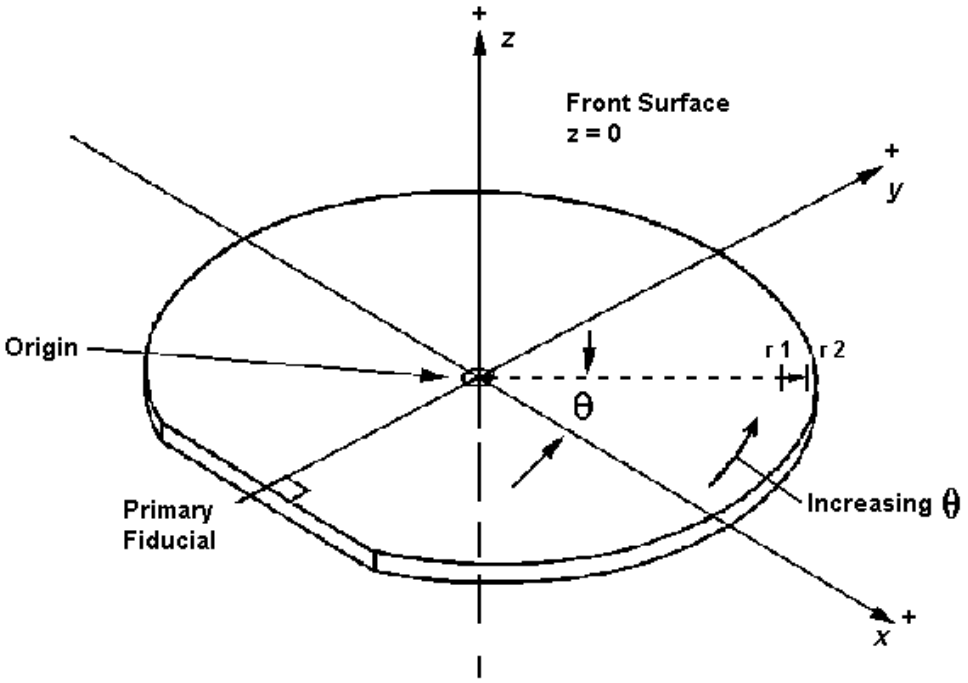

Figure 6
Edge Scan Location

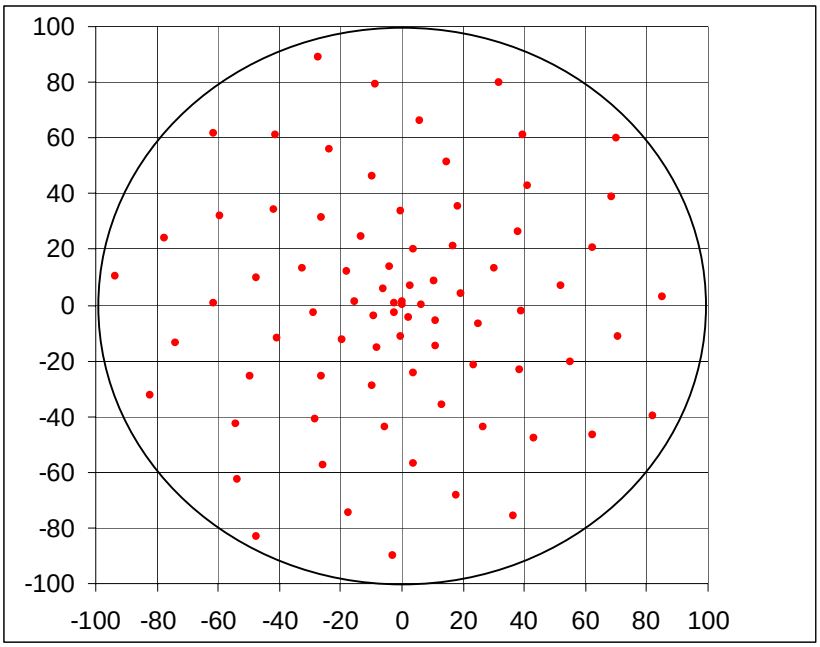

Figure 7
Spiral Scan Example - 200 mm Diameter Wafer, 81 Points