6.2 Unlike OEE, OFE and its factors are not dimensioned in time divided by time, because not all equipment in the factories is present or operating for the same amount of time. Similar to OEE, this metric:

- is dependent on product mix, process flow, operations, and time period, so be aware of this when comparing different factories or even comparing different time periods in the same factory when the product mix or process has changed (although such comparisons are still valid) especially when the factory variability is due to external factors (such as demand or excess capacity in non-bottleneck equipment).
- does not comprehend down-stream demand or the varying importance of different products (which might be addressed by a separate metric).
- varies between zero (total chaos or gridlock) and one (unobtainable perfection).
- is a product of dimensionless efficiencies.

$$\left(\begin{matrix}\textit{overall factory}\\ \textit{efficiency}\end{matrix}\right) = \left(\begin{matrix}\textit{volume}\\ \textit{efficiency}\end{matrix}\right) \times \left(\begin{matrix}\textit{yield}\\ \textit{efficiency}\end{matrix}\right) \quad (1)$$

$$\left(\begin{matrix}\textit{volume}\\ \textit{efficiency}\end{matrix}\right) = \left(\begin{matrix}\textit{normalized}\\ \textit{production}\\ \textit{efficiency}\end{matrix}\right) \times \left(\begin{matrix}\textit{balance}\\ \textit{efficiency}\end{matrix}\right) \quad (2)$$

$$\left(\begin{matrix}\textit{yield}\\ \textit{efficiency}\end{matrix}\right) = \left(\begin{matrix}\textit{line}\\ \textit{yield}\end{matrix}\right) \times \left(\begin{matrix}\textit{test}\\ \textit{yield}\end{matrix}\right) = \frac{\textit{equivalent good units out}}{\left(\begin{matrix}\textit{finished}\\ \textit{units out}\end{matrix}\right) + \left(\begin{matrix}\textit{scrapped}\\ \textit{units out}\end{matrix}\right)} \quad (3)$$

$$\left(\begin{matrix}\textit{normalized}\\ \textit{production efficiency}\end{matrix}\right) = \left(\begin{matrix}\textit{production}\\ \textit{efficiency}\end{matrix}\right)^{\left(\begin{matrix}\textit{normalizing}\\ \textit{exponent}\end{matrix}\right)} \quad (4)$$

$$\left(\begin{matrix}\textit{balance}\\ \textit{efficiency}\end{matrix}\right) = \frac{\textit{critical WIP}}{\textit{process capacity}} \quad (5)$$

$$\left(\begin{matrix}\textit{line}\\ \textit{yield}\end{matrix}\right) = \frac{\textit{finished units out}}{\left(\begin{matrix}\textit{finished}\\ \textit{units out}\end{matrix}\right) + \left(\begin{matrix}\textit{scrapped}\\ \textit{units out}\end{matrix}\right)} \quad (6)$$

$$\left(\begin{matrix}\textit{test}\\ \textit{yield}\end{matrix}\right) = \frac{\textit{good unit equivalents out}}{\textit{finished units out}} \quad (7)$$

$$\left(\begin{matrix}\textit{production}\\ \textit{efficiency}\end{matrix}\right) = \left(\begin{matrix}\textit{throughput-rate}\\ \textit{and cycle-time}\\ \textit{efficiency}\end{matrix}\right) \times \left(\begin{matrix}\textit{WIP}\\ \textit{efficiency}\end{matrix}\right) \quad (8)$$

$$\left(\begin{matrix}\textit{normalizing}\\ \textit{exponent}\end{matrix}\right) = \frac{1}{\log_2\left[\dfrac{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right) + \left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right) - 1}{\min\left\{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right)\right\}}\right]} \quad (9)$$

NOTE 13: For $x>0$, $\log_2(x) = \log_{10}(x)/\log_{10}(2) = \ln(x)/\ln(2)$.

$$\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right) = \left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right) \times \left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput rate}\end{matrix}\right) \quad (10)$$

$$\left(\begin{matrix}\textit{process}\\ \textit{capacity}\end{matrix}\right) = \sum_{e \in E}\left[\left(\begin{matrix}\text{average}\\ \text{number}\\ \text{of tools}\\ \text{in}\\ \text{equipment}\\ \text{type } e\end{matrix}\right) \times \left(\begin{matrix}\text{maximum}\\ \text{number of}\\ \text{units processed}\\ \text{simultaneously}\\ \text{on a tool of}\\ \text{equipment}\\ \text{type } e\end{matrix}\right)\right] \quad (11)$$

NOTE 14: The symbol *e*, *e**, *E*, *f*, *F*, *p*, *P*, *s*, and *S* are defined in Sections 5.1.23 through 5.1.27.

$$\left(\begin{matrix}\textit{good unit}\\ \textit{equivalents}\\ \textit{out}\end{matrix}\right) = \sum_{p \in P}\frac{\left(\begin{matrix}\text{total number}\\ \text{of good}\\ \text{product devices}\\ \text{of type } p \text{ in}\\ \textit{finished units out}\end{matrix}\right)}{\left(\begin{matrix}\text{number of product}\\ \text{devices on each}\\ \text{unit of type } p\end{matrix}\right)} \quad (12)$$

$$\left(\begin{matrix}\textit{throughput-rate and}\\ \textit{cycle-time efficiency}\end{matrix}\right) = \frac{\textit{best-case cycle time}}{\textit{average cycle time}} \quad (13)$$

$$\left(\begin{matrix}\textit{WIP}\\ \textit{efficiency}\end{matrix}\right) = \frac{\min\left\{\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}}{\max\left\{\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}} \quad (14)$$

$$\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right) = \left(\begin{matrix}\textit{average}\\ \textit{cycle time}\end{matrix}\right) \times \left(\begin{matrix}\textit{actual}\\ \textit{throughput rate}\end{matrix}\right) \quad (15)$$

$$\left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right) = \frac{\displaystyle\sum_{p \in P}\left\{\left(\begin{matrix}\text{number}\\ \text{of units}\\ \text{of}\\ \text{product}\\ \text{type } p\\ \text{in}\\ \textit{finished}\\ \textit{units}\\ \textit{out}\end{matrix}\right) \times \sum_{e \in E}\left[\sum_{s \in S_{pe}}\left(\begin{matrix}\text{minimum}\\ \text{cycle}\\ \text{time of}\\ \text{a single}\\ \text{unit of}\\ \text{product}\\ \text{type } p \text{ in}\\ \text{step } s \text{ on}\\ \text{equipment}\\ \text{type } e\end{matrix}\right)\right]\right\}}{\textit{finished units out}} \quad (16)$$

$$\left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right) = \frac{\left(\begin{matrix}\textit{finished}\\ \textit{units}\\ \textit{out}\end{matrix}\right) \times \left(\begin{matrix}\text{average}\\ \text{number of}\\ \text{tools in}\\ \text{bottleneck}\\ \text{equipment}\\ \text{type } e^*\end{matrix}\right) \times \left(\begin{matrix}\text{average}\\ \textit{availability}\\ \textit{efficiency}\\ \text{of bottleneck}\\ \text{equipment}\\ \text{type } e^*\end{matrix}\right)}{\sum_{p \in P}\left[\left(\begin{matrix}\text{number of}\\ \text{units of}\\ \text{product}\\ \text{type } p \text{ in}\\ \textit{finished}\\ \textit{units out}\end{matrix}\right) \times \sum_{s \in S_{pe^*}}\left(\begin{matrix}\textit{theoretical}\\ \textit{production}\\ \textit{time per unit}\\ \text{for product type}\\ p \text{ in step } s \text{ on}\\ \text{bottleneck}\\ \text{equipment}\\ \text{type } e^*\end{matrix}\right)\right]} \quad (17)$$

NOTE 15: One of the factors in this metric is the average number of available tools in the current bottleneck equipment set, not the total number of tools nominally in the set.

$$\left(\begin{matrix}\textit{best-}\\ \textit{case}\\ \textit{cycle}\\ \textit{time}\end{matrix}\right) = \max\left\{\left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right), \frac{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)}{\left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right)}\right\} \quad (18)$$

NOTE 16: See Related Information 1 for why Equations (18) and (20) theoretically represent the best possible cases.

$$\left(\begin{matrix}\textit{actual}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right) = \frac{\textit{finished units out}}{\textit{total time}} \quad (19)$$

$$\left(\begin{matrix}\textit{best-case}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right) = \min\left\{\frac{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)}{\left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right)}, \left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right)\right\} \quad (20)$$

$$\left(\begin{matrix}\textit{theoretical}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right) = \min\left\{\frac{\left(\begin{matrix}\textit{WIP}\\ \textit{capacity}\end{matrix}\right)}{\left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right)}, \left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right)\right\} \quad (21)$$

$$\left(\begin{matrix}\textit{WIP}\\ \textit{turnover}\end{matrix}\right) = \frac{\textit{finished units out}}{\textit{average WIP}} \quad (22)$$

7 Related Documents

7.1 *SEMI Standards*

SEMI E35 — Cost of Ownership for Semiconductor Manufacturing Equipment Metrics

SEMI E58 — Automated Reliability, Availability, and Maintainability Standard (ARAMS): Concepts, Behavior, and Services

SEMI E116 — Provisional Specification for Equipment Performance Tracking

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

RELATED INFORMATION 1
MANUFACTURING SCIENCE BACKGROUND

NOTICE: This related information is not an official part of SEMI E124 and was derived from work by the task force. This related information was approved by full letter ballot procedures on July 27, 2003.

R1-1

R1-1.1 To understand the production metrics given in Section 6, we need to understand the underlying science behind factory dynamics. The most important concept is Little's law given in the following equation, which is the same as Equation 15 in Section 6:

$$\begin{pmatrix} average \\ WIP \end{pmatrix} = \begin{pmatrix} average \\ cycle\ time \end{pmatrix} \times \begin{pmatrix} actual \\ throughput\ rate \end{pmatrix} \qquad (1)$$

R1-1.2 In *Factory Physics*[1], this identity is called the "$F = ma$" of manufacturing science. Little's law relates the three most significant fundamental quantities of production systems. Unfortunately, it says that all three metrics cannot be optimized simultaneously. Little's law is shown graphically in Figure R1-1. In all of the figures in this Related Information, the colors denote different values of the *normalized production efficiency* metric with green representing values close to one (at the *bottleneck throughput rate* and *theoretical cycle time*), yellow representing values close to ½ (the threshold case as discussed in Section R1-1.7), and red representing values close to zero (when the *throughput rate* goes to zero or the *cycle time* gets large). On the floor of Figure R1-1 are the linear contours of the *cycle time* level sets. Note that the boundaries of the operating region are determined by the *theoretical cycle time* (T_{min}), the *bottleneck throughput rate* (R_{max}), and the *WIP capacity* (W_{max}).

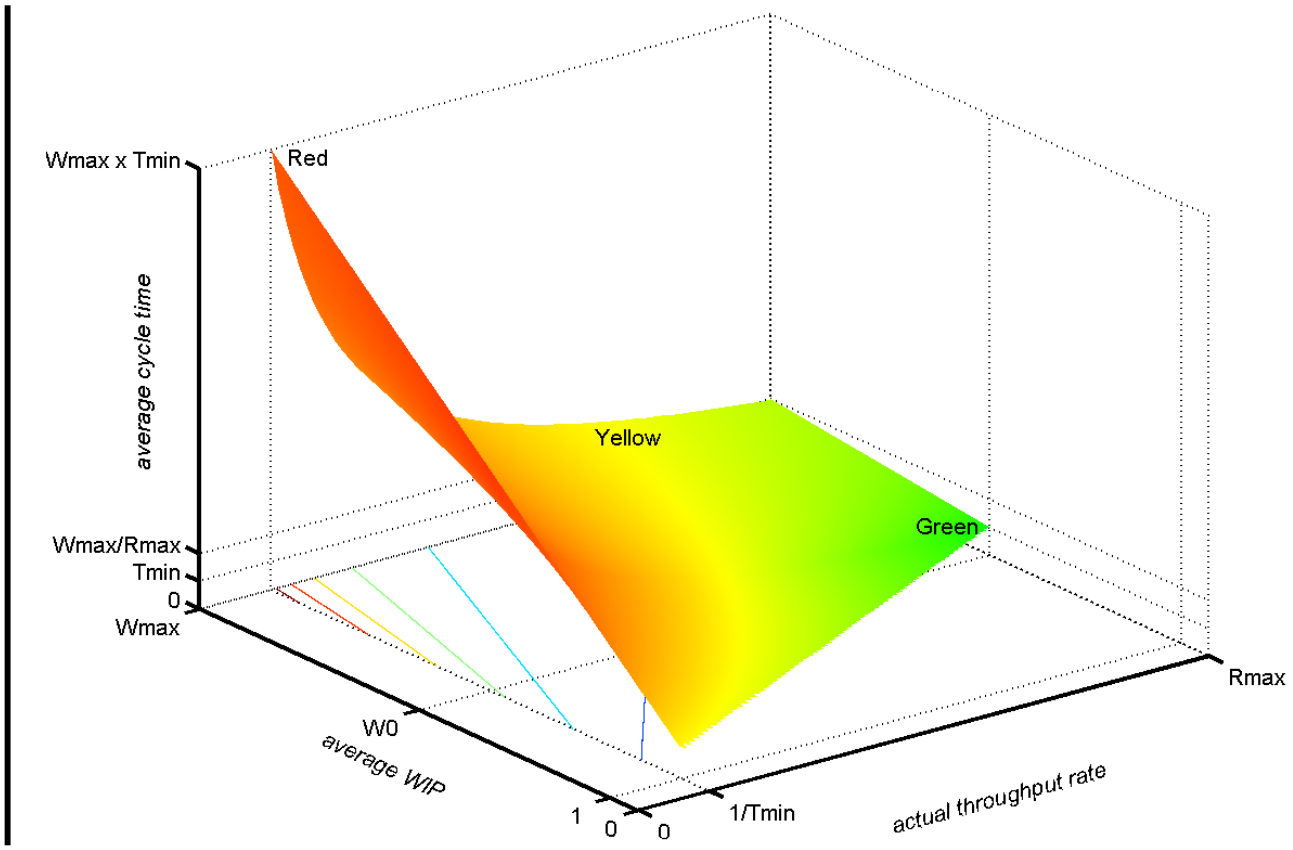

Figure R1-1
Surface Plot of Little's Law

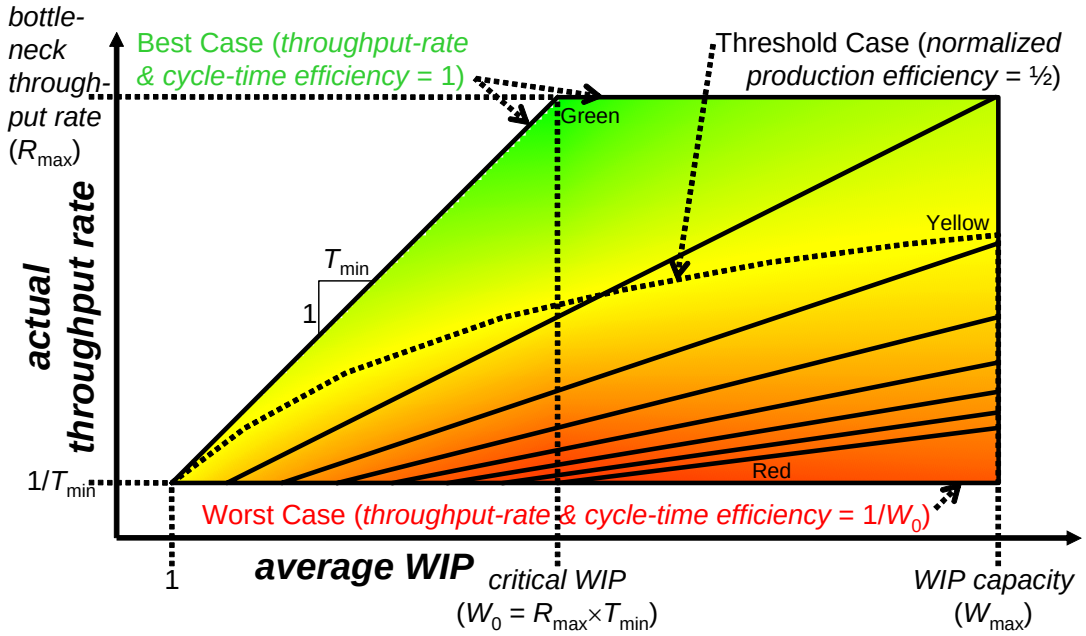

Figure R1-2
Plot of Actual Throughput Rate vs. Average WIP

R1-1.3 If we look at two of these fundamental quantities at a time, the factory dynamics become more clear. For example, Figure R1-2 above shows *actual throughput rate* as a function of *average WIP* levels. Here the diagonal solid black lines represent different constant cycle times, but no known strategy will keep the factory operating exactly on one of these lines.

R1-1.4 Now suppose the factory is managed with a push strategy where a constant throughput rate is enforced so that WIP levels are allowed to reach their equilibrium state. As shown below in Figure R1-3, this amounts to choosing to operate the factory on one of the diagonal solid black lines (each of which represent different constant throughput rates). We try to drive the factory along that line toward the bottom left (for lower *average cycle time* and *average WIP* levels) by using better operating principles, but we are resisted by the inherent variability of the factory.

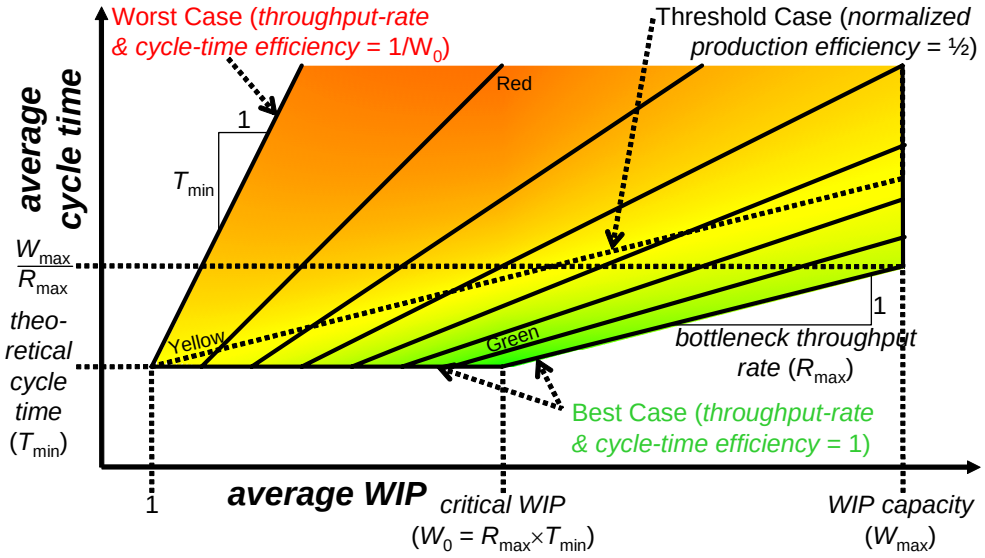

Figure R1-3
Plot of Average Cycle Time vs. Average WIP

R1-1.5 Now suppose the factory is managed with a pull strategy where a constant WIP level is enforced so that throughput rates are allowed to reach their equilibrium state. In general, this is a better strategy, because studies have shown that a constant WIP level will result in a higher average throughput rate than the constant throughput rate that results in the same average WIP level. As shown below in Figure R1-4, this constant WIP strategy (known as CONWIP) amounts to choosing to operate the factory on one of the solid black curves (each of which represents a different constant WIP level). We try to drive the factory along that curve toward the bottom right (for lower *average cycle time* and a higher *actual throughput rate*) by using better operating principles, but we are resisted by the inherent variability of the factory.

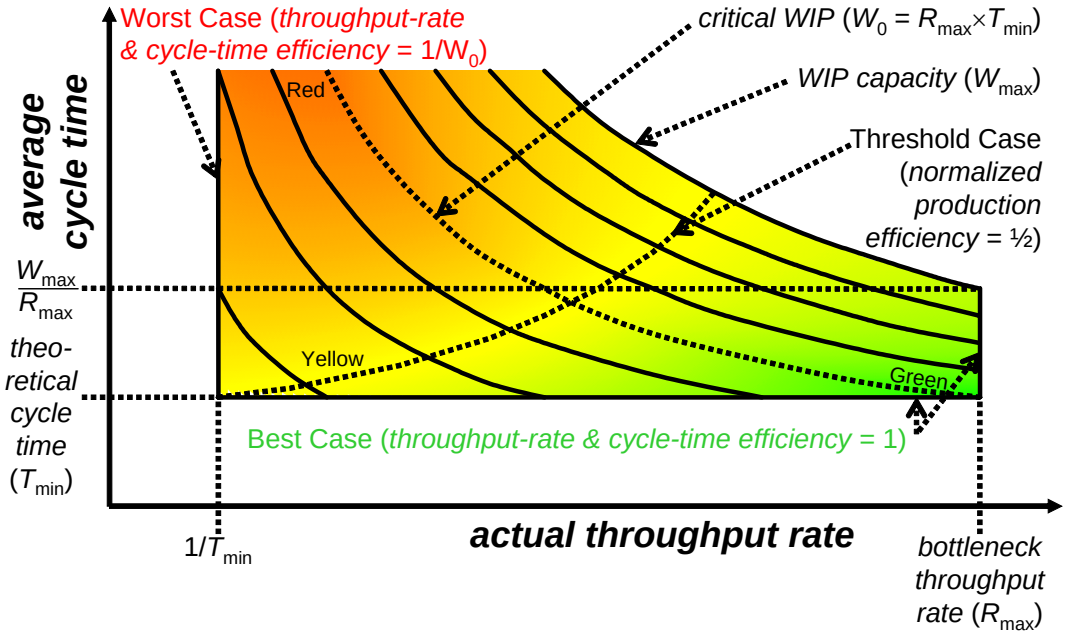

Figure R1-4
Plot of Average Cycle Time vs. Actual Throughput Rate

R1-1.6 We can now see why the efficiency of throughput rate and cycle time can both be measured by the same metric (*throughput-rate and cycle-time efficiency*). The following derivation also gives alternative definitions for *throughput-rate and cycle-time efficiency* for use when cycle time information is not available (such as in resource-based simulations).

$$\begin{aligned}
&\left(\begin{matrix}\textit{throughput-rate and}\\ \textit{cycle-time efficiency}\end{matrix}\right)\\
&= \frac{\textit{best-case cycle time}}{\textit{average cycle time}}\\
&= \frac{\max\left\{\left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right), \dfrac{\textit{average WIP}}{\textit{bottleneck throughput rate}}\right\}}{\textit{average cycle time}}\\
&= \frac{\max\left\{\left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right), \dfrac{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)}{\left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right)}\right\}}{\left(\begin{matrix}\textit{average}\\ \textit{cycle time}\end{matrix}\right)} \Big/ \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\\
&= \frac{\max\left\{\dfrac{\textit{theoretical cycle time}}{\textit{average WIP}}, \dfrac{1}{\left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput rate}\end{matrix}\right)}\right\}}{1/\left(\textit{actual throughput rate}\right)}\\
&= \frac{\textit{actual throughput rate}}{\min\left\{\dfrac{\textit{average WIP}}{\textit{theoretical cycle time}}, \left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput rate}\end{matrix}\right)\right\}}\\
&= \frac{\textit{actual throughput rate}}{\textit{best-case throughput rate}}\\
&= \frac{\left(\textit{finished units out}\right)/\left(\textit{total time}\right)}{\left(\textit{average WIP}\right)/\left(\textit{theoretical cycle time}\right)}\\
&= \frac{\textit{theoretical cycle time}}{\textit{total time}} \times \frac{\textit{finished units out}}{\textit{average WIP}}\\
&= \left(\begin{matrix}\textit{theoretical cycle time}\\ \text{as a fraction of } \textit{total time}\end{matrix}\right) \times \left(\begin{matrix}\textit{WIP}\\ \textit{turnover}\end{matrix}\right)
\end{aligned} \tag{2}$$

R1-1.7 The *production efficiency* is normalized by the power of the *normalizing exponent* so that a value of ½ for the *normalized production efficiency* indicates that the factory is performing at the level of the threshold case (which divides a well run factory from one badly operated). This threshold case is also known as the practical worst case, because it represents what the best operating procedures can do in a maximally random factory (see the *Factory Physics* book for more on this case). In the threshold case,

$$\left(\begin{matrix}\textit{average}\\ \textit{cycle time}\end{matrix}\right) = \frac{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right) + \left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right) - 1}{\textit{bottleneck throughput rate}} \tag{3}$$

which results in the following *production efficiency*.

$$\begin{aligned}
&\left(\begin{matrix}\textit{production}\\ \textit{efficiency}\end{matrix}\right)\\
&= \left(\begin{matrix}\textit{throughput-rate and}\\ \textit{cycle-time efficiency}\end{matrix}\right) \times \left(\begin{matrix}\textit{WIP}\\ \textit{efficiency}\end{matrix}\right)\\
&= \frac{\max\left\{\left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right), \dfrac{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)}{\left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right)}\right\}}{\textit{average cycle time}} \times \left(\begin{matrix}\textit{WIP}\\ \textit{efficiency}\end{matrix}\right)\\
&= \frac{\max\left\{\left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right) \times \left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}}{\left(\begin{matrix}\textit{average}\\ \textit{cycle time}\end{matrix}\right) \times \left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput rate}\end{matrix}\right)}\\
&\quad \times \left(\textit{WIP efficiency}\right)\\
&= \frac{\cancel{\max\left\{\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}}}{\left(\begin{matrix}\textit{average}\\ \textit{cycle}\\ \textit{time}\end{matrix}\right) \times \left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right)}\\
&\quad \times \frac{\min\left\{\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}}{\cancel{\max\left\{\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}}}\\
&= \frac{\min\left\{\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}}{\dfrac{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right) + \left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right) - 1}{\cancel{\left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput rate}\end{matrix}\right)}} \times \cancel{\left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput}\\ \textit{rate}\end{matrix}\right)}}\\
&= \frac{\min\left\{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right)\right\}}{\left(\textit{average WIP}\right) + \left(\textit{critical WIP}\right) - 1}
\end{aligned} \tag{4}$$

R1-1.8 Thus, if we set *normalized production efficiency* to have a value of ½ at this *average cycle time*, we get

$$\begin{aligned}\frac{1}{2} &= \begin{pmatrix} normalized \\ production \\ efficiency \end{pmatrix} \\ &= \begin{pmatrix} production \\ efficiency \end{pmatrix}^{\left(\begin{smallmatrix} normalizing \\ exponent \end{smallmatrix}\right)} \\ &= \left[\frac{\min\left\{ \left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right), \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) \right\}}{\left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right) + \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) - 1} \right]^{\left(\begin{smallmatrix} normalizing \\ exponent \end{smallmatrix}\right)}\end{aligned} \tag{5}$$

and, taking logarithms of both sides,

$$\begin{aligned}&\log_2\left(\frac{1}{2}\right) \\ &= \log_2 \left\{ \left[\frac{\min\left\{ \left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right), \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) \right\}}{\left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right) + \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) - 1} \right]^{\left(\begin{smallmatrix} normalizing \\ exponent \end{smallmatrix}\right)} \right\} \\ &= \left(\begin{smallmatrix} normalizing \\ exponent \end{smallmatrix}\right) \times \log_2 \left[\frac{\min\left\{ \left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right), \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) \right\}}{\left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right) + \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) - 1} \right]\end{aligned} \tag{6}$$

so

$$\begin{aligned}\left(\begin{smallmatrix} normalizing \\ exponent \end{smallmatrix}\right) &= \frac{\log_2\left(\frac{1}{2}\right)}{\log_2 \left[\frac{\min\left\{ \left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right), \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) \right\}}{\left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right) + \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) - 1} \right]} \\ &= \frac{-1}{-\log_2 \left[\frac{\left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right) + \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) - 1}{\min\left\{ \left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right), \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) \right\}} \right]} \\ &= \frac{1}{\log_2 \left[\frac{\left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right) + \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) - 1}{\min\left\{ \left(\begin{smallmatrix} average \\ WIP \end{smallmatrix}\right), \left(\begin{smallmatrix} critical \\ WIP \end{smallmatrix}\right) \right\}} \right]}\end{aligned} \tag{1}$$

which is the same as Equation (9) that was given in Section 6 of the main body of this guide.

RELATED INFORMATION 2
EXAMPLE APPLICATION

NOTICE: This related information is not an official part of SEMI E124 and was derived from an example developed by the task force using this guide. This related information was approved for publication by full letter ballot on April 11, 2003.

R2-1

R2-1.1 As an example to show how the metrics in this guide are applied, the diagram in Figure R2-1 shows the process flow for a grossly simplified model of a wafer fab (developed by Karl Kempf at Intel) that has only five machines in three tool sets, one process flow with six steps, and a single material handling vehicle (that transports 25 wafers at a time).

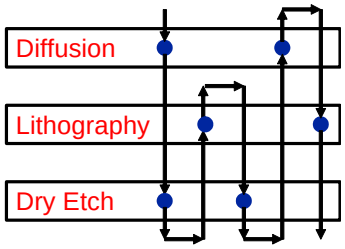

Figure R2-1
MiniFab Process Flow

R2-1.2 The data for this model are shown in the first few columns of Table R2-1 and Table R2-2. A simulation gave the following additional run data:

total time	= 9 years	= 4,733,640 minutes
average cycle time	= 1.8 days	= 2,592 minutes
total units out	= 39,420 lots	= 985,500 wafers
finished units out		= 938,571 wafers
scrapped units out		= 46,929 wafers
good unit equivalents out		= 891,642.1 wafers

R2-1.3 In the next-to-last column of Table R2-1, we added together (for each step) all of the times (to load, process batch, unload, and travel to next step) and summed the results to get a *theoretical cycle time* of 812.4 minutes. In the last column of Table R2-1, we computed the *theoretical production time per unit* for each step. These values were then used in the last column of Table R2-2 to compute the *throughput rate* for each equipment set. The *throughput rate* for the lithography equipment set (0.2182 wafers/minute) is the *bottleneck throughput rate*, not because it is the smallest *throughput rate* (it is), but because the lithography equipment set has the highest average *operational efficiency*. The remaining terms are derived on the following pages.

Table R2-1 Process Data

Process Step Number	*Equipment Set Name*	*Time to Load Batch, minutes*	*Time to Process Batch, minutes*	*Time to Unload Batch, minutes*	*Time to Travel to Next Step, minutes*	*theoretical cycle time* (See Note 1), *minutes*	*theoretical production time per unit* (See Note 2), *minutes/wafer*
1	Diffusion	20	225	40	8	293	3.0
2	Dry Etch	15	30	15	4	64	1.2
3	Lithography	10	2.2	10	4	26.2	2.2
4	Dry Etch	15	50	15	8	88	2.0
5	Diffusion	20	255	40	4	319	3.4
6	Lithography	10	2.2	10	-	22.2	2.2
Sum	-	90	564.4	130	28	812.4	-

NOTE 1: (*theoretical cycle time*) = (*Time to Load Batch*) + (*Time to Process Batch*) + (*Time to Unload Batch*) + (*Time to Travel to Next Step*)
NOTE 2: (*theoretical production time per unit*) = (*Time to Process Batch*)/(*Process Batch Size*)

Table R2-2 Equipment Data

Equipment Set Name	*Number in Set*	*Process Batch Size, wafers*	*Buffer Size, wafers*	*Average operational efficiency*	*availability efficiency (each tool)*	*Average availability efficiency*	*bottleneck throughput rate* (See Note 1), *wafers/minute*
Diffusion	2	75	450	88%	93% & 97%	95%	0.2969
Dry Etch	2	25	300	78%	81% & 85%	83%	0.5188
Lithography	1	1	300	91%	96%	96% (max!)	0.2182
Transport	1	25	0	69%	62%	62%	0.5536

NOTE 1: (*bottleneck throughput rate*) = (*Number in Set*) × (*Average availability efficiency*)/Σ(*theoretical production time per unit*)

$$\begin{aligned}\left(\begin{matrix}WIP\\capacity\end{matrix}\right) &= \sum_{e\in E}\left[\left(\begin{matrix}Buffer\\Size\end{matrix}\right)+\left(\begin{matrix}Process\\Batch\\Size\end{matrix}\right)\times\left(\begin{matrix}Size\\of\\Set\end{matrix}\right)\right]\\ &= [450+75\times 2]+[300+25\times 2]\\ &\quad +[300+1\times 1]+[0+25\times 1]\\ &= [450+150]+[300+50]\\ &\quad +[300+1]+[0+25]\\ &= 600+350+301+25\\ &= 1276 \text{ wafers}\end{aligned} \tag{1}$$

$$\begin{aligned}\left(\begin{matrix}actual\\throughput\ rate\end{matrix}\right) &= \frac{finished\ units\ out}{total\ time}\\ &= \frac{938{,}571 \text{ wafers}}{4{,}733{,}640 \text{ minutes}}\\ &\approx 0.1983\frac{\text{wafers}}{\text{minute}}\end{aligned} \tag{2}$$

$$\begin{aligned}\left(\begin{matrix}average\\WIP\end{matrix}\right) &= \left(\begin{matrix}average\\cycle\ time\end{matrix}\right)\times\left(\begin{matrix}actual\\throughput\ rate\end{matrix}\right)\\ &\approx (2592 \text{ minutes})\times\left(0.19827\frac{\text{wafers}}{\text{minute}}\right)\\ &\approx 513.9 \text{ wafers}\end{aligned} \tag{3}$$

$$\begin{aligned}\left(\begin{matrix}WIP\\turnover\end{matrix}\right) &= \frac{finished\ units\ out}{average\ WIP}\\ &\approx \frac{938{,}571 \text{ wafers}}{513.9 \text{ wafers}}\\ &\approx 1826.3 \text{ turns}\end{aligned} \tag{4}$$

$$\begin{aligned}\left(\begin{matrix}theoretical\\throughput\\rate\end{matrix}\right) &= \min\left\{\frac{\left(\begin{matrix}WIP\\capacity\end{matrix}\right)}{\left(\begin{matrix}theoretical\\cycle\ time\end{matrix}\right)}, \left(\begin{matrix}bottleneck\\throughput\\rate\end{matrix}\right)\right\}\\ &\approx \min\left\{\frac{1276 \text{ wafers}}{812.4 \text{ minutes}}, 0.2182\frac{\text{wafers}}{\text{minute}}\right\}\\ &\approx \min\{1.5707, 0.2182\}\frac{\text{wafers}}{\text{minute}}\\ &\approx 0.2182\frac{\text{wafers}}{\text{minute}}\end{aligned} \tag{5}$$

$$\begin{aligned}\left(\begin{matrix}best\text{-}case\\throughput\\rate\end{matrix}\right) &= \min\left\{\frac{\left(\begin{matrix}average\\WIP\end{matrix}\right)}{\left(\begin{matrix}theoretical\\cycle\ time\end{matrix}\right)}, \left(\begin{matrix}bottleneck\\throughput\\rate\end{matrix}\right)\right\}\\ &\approx \min\left\{\frac{513.9 \text{ wafers}}{812.4 \text{ minutes}}, 0.2182\frac{\text{wafers}}{\text{minute}}\right\}\\ &\approx \min\{0.6326, 0.2182\}\frac{\text{wafers}}{\text{minute}}\\ &\approx 0.2182\frac{\text{wafers}}{\text{minute}}\end{aligned} \tag{6}$$

$$\begin{aligned}\left(\begin{matrix}best\text{-}\\case\\cycle\\time\end{matrix}\right) &= \max\left\{\left(\begin{matrix}theoretical\\cycle\ time\end{matrix}\right), \frac{\left(\begin{matrix}average\\WIP\end{matrix}\right)}{\left(\begin{matrix}bottleneck\\throughput\\rate\end{matrix}\right)}\right\}\\ &\approx \max\left\{812.4 \text{ minutes}, \frac{513.9 \text{ wafers}}{0.2182\frac{\text{wafers}}{\text{minute}}}\right\}\\ &\approx \max\{812.4 \text{ minutes},\ 2355.5 \text{ minutes}\}\\ &\approx 2355.5 \text{ minutes}\end{aligned} \tag{7}$$

NOTE 1: For this *average WIP* level, the *best-case cycle time* was not determined by the *theoretical cycle time*, but by the *bottleneck throughput rate*. Thus, a simple metric like (*average cycle time*)/(*theoretical cycle time*) underestimates how well the factory is doing.

$$\left(\begin{matrix}\textit{throughput-rate and}\\ \textit{cycle-time efficiency}\end{matrix}\right) = \frac{\textit{best-case cycle time}}{\textit{average cycle time}} \approx \frac{2355.5 \text{ minutes}}{2592.0 \text{ minutes}} \approx 90.88\% \quad (8)$$

$$\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right) = \left(\begin{matrix}\textit{theoretical}\\ \textit{cycle time}\end{matrix}\right) \times \left(\begin{matrix}\textit{bottleneck}\\ \textit{throughput rate}\end{matrix}\right) \approx (812.4 \text{ minutes}) \times \left(0.2182 \ \frac{\text{wafers}}{\text{minute}}\right) \approx 177.3 \text{ wafers} \quad (9)$$

$$\left(\begin{matrix}\textit{process}\\ \textit{capacity}\end{matrix}\right) = \sum_{e \in E} \left[\left(\begin{matrix}\text{average}\\ \text{number}\\ \text{of tools}\\ \text{in}\\ \text{equipment}\\ \text{type } e\end{matrix} \right) \times \left(\begin{matrix}\text{maximum}\\ \text{number of}\\ \text{units processed}\\ \text{simultaneously}\\ \text{on a tool of}\\ \text{equipment}\\ \text{type } e\end{matrix} \right) \right] = [2 \times 75] + [2 \times 25] + [1 \times 1] + [1 \times 25] \text{ wafers} = 150 + 50 + 1 + 25 \text{ wafers} = 226 \text{ wafers} \quad (10)$$

$$\left(\begin{matrix}\textit{WIP}\\ \textit{efficiency}\end{matrix}\right) = \frac{\min\left\{\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}}{\max\left\{\left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right)\right\}} \approx \frac{\min\{513.9,\ 177.3\} \text{ wafers}}{\max\{513.9,\ 177.3\} \text{ wafers}} \approx \frac{177.3 \text{ wafers}}{513.9 \text{ wafers}} \approx 34.49\% \quad (11)$$

$$\left(\begin{matrix}\textit{production}\\ \textit{efficiency}\end{matrix}\right) = \left(\begin{matrix}\textit{throughput-rate}\\ \textit{and cycle-time}\\ \textit{efficiency}\end{matrix}\right) \times \left(\begin{matrix}\textit{WIP}\\ \textit{efficiency}\end{matrix}\right) \approx (0.9087) \times (0.3449) \approx 31.34\% \quad (12)$$

$$\left(\begin{matrix}\textit{normalizing}\\ \textit{exponent}\end{matrix}\right) = \frac{1}{\log_2\left[\frac{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right) + \left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right) - 1}{\min\left\{\left(\begin{matrix}\textit{average}\\ \textit{WIP}\end{matrix}\right), \left(\begin{matrix}\textit{critical}\\ \textit{WIP}\end{matrix}\right)\right\}}\right]} \approx \frac{1}{\log_2\left[\frac{513.9 + 177.3 - 1 \text{ wafers}}{\min\{513.9,\ 177.3\} \text{ wafers}}\right]} \approx \frac{1}{\log_2\left[\frac{690.2 \text{ wafers}}{177.3 \text{ wafers}}\right]} \approx \frac{1}{\log_2[3.894]} \approx \frac{1}{1.961} \approx 0.5099 \quad (13)$$

$$\left(\begin{matrix}\textit{normalized}\\ \textit{production}\\ \textit{efficiency}\end{matrix}\right) = \left(\begin{matrix}\textit{production}\\ \textit{efficiency}\end{matrix}\right)^{\left(\begin{matrix}\textit{normalizing}\\ \textit{exponent}\end{matrix}\right)} \approx (0.3134)^{0.5099} \approx 55.35\% \quad (14)$$

$$\left(\begin{matrix}\textit{balance}\\ \textit{efficiency}\end{matrix}\right) = \frac{\textit{critical WIP}}{\textit{process capacity}} \approx \frac{177.3 \text{ wafers}}{226 \text{ wafers}} \approx 78.43\% \quad (15)$$

$$\left(\begin{matrix}\textit{volume}\\ \textit{efficiency}\end{matrix}\right) = \left(\begin{matrix}\textit{normalized}\\ \textit{production}\\ \textit{efficiency}\end{matrix}\right) \times \left(\begin{matrix}\textit{balance}\\ \textit{efficiency}\end{matrix}\right) \approx (0.5535) \times (0.7843) \approx 43.41\% \quad (16)$$

$$\left(\begin{matrix}\textit{test}\\ \textit{yield}\end{matrix}\right) = \frac{\textit{good unit equivalents out}}{\textit{finished units out}} \approx \frac{891{,}642.1 \text{ wafers}}{938{,}571.0 \text{ wafers}} \approx 95.00\% \quad (17)$$

$$\left(\begin{matrix}\textit{line}\\ \textit{yield}\end{matrix}\right) = \frac{\textit{finished units out}}{(\textit{finished units out}) + (\textit{scrapped units out})} = \frac{938{,}571 \text{ wafers}}{(938{,}571 \text{ wafers}) + (46{,}929 \text{ wafers})} = \frac{938{,}571 \text{ wafers}}{985{,}500 \text{ wafers}} \approx 95.24\% \quad (18)$$

$$\begin{pmatrix} yield \\ efficiency \end{pmatrix} = \begin{pmatrix} line \\ yield \end{pmatrix} \times \begin{pmatrix} test \\ yield \end{pmatrix}$$
$$\approx (0.9524) \times (0.9400) \quad (19)$$
$$\approx 90.48\%$$

$$\begin{pmatrix} overall\ factory \\ efficiency \end{pmatrix} = \begin{pmatrix} volume \\ efficiency \end{pmatrix} \times \begin{pmatrix} yield \\ efficiency \end{pmatrix}$$
$$\approx (0.4341) \times (0.9048) \quad (20)$$
$$\approx 39.27\%$$

RELATED INFORMATION 3
SUPPLEMENTARY INFORMATION

NOTICE: This related information is not an official part of SEMI E124 and was derived from work by the task force. This related information was approved by full letter ballot procedures on April 11, 2003.

R3-1

R3-1.1 As was mentioned in Section 2.1, there are at least three things in need of measurement in a factory: production, utilization of assets, and costs. This guide focuses on evaluating production; utilization of assets and costs (as well as other economic factors) are outside its scope. For measuring effectiveness of asset use, an average (over all of the equipment in the factory) of overall equipment efficiency (OEE) weighted by cost of ownership (COO) can be defined in one of those documents. However, the use of consumables, utilities, and human resources would still need to be comprehended. For measuring costs, some other new standard might define a new metric (like COO) for the cost of factory ownership in such terms as $/(good wafers), $/(good chips), $/(metal levels), $/(good transistors), $/circuit, or $/bit.

R3-1.2 As was mentioned in Section 3.2, the metrics in this guide are intended for evaluating the overall health of the factory production, not for diagnosing problems (or opportunities for improvement) in the factory, although some component metrics can be used that way. These metrics should indicate whether the factory is running poorly (like taking a person's temperature tells whether they are sick) while some of its components and other diagnostic metrics might indicate what the cause of the problem is (like doing a blood analysis in the lab identifies the disease). The following are examples of metrics not in this guide that can be used for diagnosis:

- ratio of turns to work in process (WIP) at key operations or for blocks of operations.
- overall WIP distribution.
- daily starts and output.
- defect density.
- throughput, utilization, and available up-time of bottleneck equipment.

SEMI E129-1103
GUIDE TO ASSESS AND CONTROL ELECTROSTATIC CHARGE IN A SEMICONDUCTOR MANUFACTURING FACILITY

This guide was technically approved by the Global Metrics Committee and is the direct responsibility of the North American Metrics Committee. Current edition approved by the North American Regional Standards Committee on September 3, 2003. Initially available at www.semi.org October 2003; to be published November 2003.

1 Purpose

1.1 The purpose of this document is to minimize the negative impact on productivity caused by static charge in semiconductor manufacturing environments. It is a guide for establishing electrostatic compatibility in facilities used for semiconductor manufacturing.

1.2 Electrostatic surface charge causes a number of undesirable effects in semiconductor manufacturing environments. Electrostatic discharge (ESD) damages both products and reticles. ESD events also cause electromagnetic interference (EMI), resulting in equipment malfunctions. Charged wafer and reticle surfaces attract particles (electrostatic attraction or ESA) and increase the defect rate. Charge on products can also result in equipment malfunction or product breakage. Operating problems and additional product defects due to static charge can have a negative impact on the cost of ownership of semiconductor manufacturing equipment (refer to SEMI E35).

1.3 For product and reticle protection or EMI control, the measurement of the ESD risk of an area is defined by the presence and nature of the ESD events that occur. For contamination control by reducing particle attraction, the static risk of an area is defined by the presence and level of static charges.

1.4 While an increasing amount of semiconductor production is done in minienvironments or within the production equipment, product and reticles must still be transported throughout the manufacturing facility. They are both affected by, and the cause of static problems during transport. Moving personnel in the manufacturing facility are also sources of static charge problems. This document addresses the presence of static charge in the entire facility, including the production equipment and minienvironments.

1.5 Static control methods can be incorporated in the factory design to reduce static charge to acceptable levels. This guide is intended for use primarily by semiconductor manufacturers and cleanroom facilities designers during the design of their facilities. Producers of the silicon wafers and photomasks used in semiconductor manufacturing will also find it useful. There are test methods available (see Section 7 and Related Information 2 of this guide) to demonstrate the effectiveness of the static control methods. The end user will be able to use the same test methods to verify compliance with a facility design specification after the facility is built or after design changes have been made, and to verify ongoing compliance as a part of factory maintenance procedures.

1.6 Semiconductor process technology will continue to move toward smaller product geometries. Acceptable static charge levels will decrease with product feature size. This document will help to assure that facility static charge limits are appropriate for the product being manufactured.

2 Scope

2.1 The scope of this document is limited to methods of measurement and a guide for the maximum recommended level of static charge on all facility surfaces including:

- Product, photomasks or their carriers,
- Facility construction materials and furniture,
- Personnel,
- Packaging and transport materials, and
- Equipment (through reference to SEMI E78)

2.2 This document references SEMI E78, SEMI E43 and other methods of measuring static charge as well as the performance parameters of static control methods.

2.3 Appendix 1 describes the methodology for determining the maximum recommended static charge levels that are shown in Section 12.5 Table 1.

NOTE 1: Related Information 1 discusses device sensitivity measurements, which are the first step in setting recommended static levels in a facility. Related Information 2 describes static control methods commonly used in semiconductor manufacturing. Related Information 3 discusses the relationship between ESD and EMI.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Limitations

3.1 *Static Measurements* — Measurements of electrostatic quantities such as charge, electric field, voltage, and resistance to ground are difficult to make. The nature of the object (insulator or conductor), its geometry, its surroundings, and the measuring equipment itself, are only a few of the factors affecting the accuracy of an electrostatic measurement. In general, direct measurement of static charge is possible with small, moveable objects. Larger objects, and those fixed in position, will need to be characterized by the electric field that results from the static charge.

3.2 *Location* — The test methods for static charge and maximum recommended levels of static charge on facility surfaces are meant to be applied after the facility has been built. Testing the performance of static control methods may be done before or after construction. It may be difficult to directly relate the performance of the static control method to the static charge level that results in the completed facility. Prior experience of the static control supplier will be a source of this information.

3.3 *Test Methods* — The test methods referenced in this document do not guarantee precise measurements of static charge levels. The maximum static charge levels recommended in this document have large tolerances. See Section 15.1.

3.4 *Static Charge Control* — There are a variety of static related issues in a semiconductor-manufacturing environment. The issues are complex due to the wide range of electrostatic problems, and device or equipment sensitivities to these problems. This guide contains general recommendations. Users of this document are cautioned that specific static related problems may require or allow different levels of static charge than are recommended in this document.

3.5 *Measurements*

3.5.1 *Measurements of Very High Static Potentials (> 30,000 V)* — Measurements of very high static potentials (> 30,000 V) may need to be done at larger distances to avoid exceeding the measurement range of the meter and/or an ESD event to the meter.

3.5.2 *Measurements on Moving Objects or Surfaces* — Care should be taken, when attempting to read electrostatic charges on moving objects or surfaces, to maintain correct distance and avoid any contact; this is to ensure "good" readings with no mechanical damage or personal injury.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E10 — Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM)

SEMI E33 — Specification for Semiconductor Manufacturing Facility Electromagnetic Compatibility

SEMI E35 — Cost of Ownership for Semiconductor Manufacturing Equipment Metrics

SEMI E43 — Guide for Measuring Static Charge on Objects and Surfaces

SEMI E78 — Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment

4.2 *ESD Association Standards and Advisories*[1]

ANSI EOS/ESD S8.1 — ESD Awareness Symbols

ANSI ESD S1.1 — Evaluation, Acceptance, and Functional Testing of Wrist Straps

ANSI ESD S11.31 — Evaluating the Performance of Electrostatic Discharge Shielding: Bags

ANSI ESD S20.20 — Standard for the Development of an ESD Control Program

ANSI ESD S4.1 — Worksurfaces – Resistance Measurements

ANSI ESD STM11.12 — Volume Resistance Measurement of Static Dissipative Planar Materials

ANSI ESD STM12.1 — Seating – Resistive Characterization

ANSI ESD STM2.1 — Resistance Test Method for Electrostatic Discharge Protective Garments

ANSI ESD STM3.1 — Ionization

ANSI ESD STM4.2 — Worksurfaces – Charge Dissipation Characteristics

ANSI ESD STM5.2 — Electrostatic Discharge Sensitivity Testing – Machine Model

ANSI ESD STM5.3.1 — Charged Device Model (CDM) – Component Level

ANSI ESD STM9.1 — Resistive Characterization of Footwear

ANSI ESD STM97.1 — Floor Materials and Footwear – Resistance Measurement in Combination with a Person

1 ESD Association, 7900 Turin Road, Rome, NY 13440, USA (www.esda.org)

ESD ADV1.0 — Glossary of Terms

ESD ADV53.1 — ESD Protective Workstations

ESD S6.1 — Grounding – Recommended Practice

ESD SP10.1 — Automated Handling Equipment

ESD STM11.11 — Surface Resistance Measurement of Static Dissipative Planar Materials

ESD STM5.1 — Electrostatic Discharge Sensitivity Testing – Human Body Model

ESD STM7.1 — Floor Materials – Resistive Characterization of Materials

ESD STM97.2 — Floor Materials and Footwear Voltage Measurement in Combination with a Person

ESD TR11-01 — Electrostatic Guidelines and Considerations for Cleanrooms and Clean Manufacturing

ESD TR20.20 — ESD Handbook

4.3 *IEC Documents*[2]

IEC 61000-4-2 — Electromagnetic compatibility (EMC) Part 4.2: Testing and measurement techniques – Electrostatic discharge immunity test, Transient Immunity Standard, International Electrotechnical Commission (IEC).

IEC EN 61340-5-1 — Electrostatics – Part 5.1: Protection of electronic devices from electrostatic phenomena — General Requirements.

NOTE 2: This replaces CENNELEC 100015-1 — Elements of a Static Control Program

IEC EN 61340-5-2 — Electrostatics – Part 5.2: Protection of electronic devices from electrostatic phenomena – Users' Guide – Elements of a Static Control Program

4.4 *JEDEC Documents*[3]

JESD22-A114 — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

JESD22-C101 — Field-Induced Charged-Device Model Test Methods for Electrostatic Discharge Withstand Thresholds of Microelectronic Components

JESD625 — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

4.5 *Other Documents*

89/336/EEC — Directive on Electromagnetic Compatibility – European Commission[4]

BS EN 50082-2 — Electromagnetic Compatibility (EMC). Generic Immunity Standards. Immunity for Industrial Environments, British Standards Institution (BSI)[5]

ITRS 2003 — International Technology Roadmap for Semiconductors – International SEMATECH[6]

MIL-STD 883 — Test Method Standard – Microcircuits (Method 3015.7 – Electrostatic Discharge Sensitivity Classification), Defense Supply Center Columbus[7]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Definitions*

5.1.1 *carrier* — a device for holding wafers, dies, packaged integrated circuits, or reticles for various processing steps in semiconductor manufacturing (from SEMI E78).

5.1.2 *electromagnetic interference (EMI)* — any electrical signal in the non-ionizing (sub-optical) portion of the electromagnetic spectrum with the potential to cause an undesired response in electronic equipment.

5.1.3 *electrostatic attraction (ESA)* — the force between two or more oppositely charged objects.

NOTE 3: The result is increased deposition rate of particles onto charged surfaces, or movement of charged materials.

5.1.4 *electrostatic compatibility* — charge control adequate to allow the manufacturing of products and the inter-equipment transfer of products, reticles, and carriers without electrostatic problems.

5.1.5 *electrostatic discharge (ESD)* — the rapid spontaneous transfer of electrostatic charge induced by a high electrostatic field.

NOTE 4: Usually the charge flows in a spark between two objects at different electrostatic potentials.

2 IEC, 3, Rue de Varembe, CH - 1211 Geneva 20 Switzerland (www.IEC.org.ch)

3 JEDEC, 2500 Wilson Blvd., Arlington, VA 22201-3834, USA (www.jedec.org)

4 European Commission, Rue de la Loi, Wetstraat 200, B-1049 Brussels, Belgium (www.europa.eu.int)

5 BSI, 389 Chiswick High Road, GB - LONDON W4 4AL (www.BSI-global.com)

6 International SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, USA (www.sematech.org)

7 Defense Supply Center Columbus, P.O. Box 3990, Columbus, OH 43216-5000, USA (www.dscc.dla.mil)

5.1.6 *ESD simulator* — an instrument providing a specified electrostatic discharge current waveform when discharged directly to a product or equipment part.

5.1.7 *facility electrostatic levels* — acceptable static charge levels related to the major technology nodes of product and reticle feature sizes.

5.1.8 *minienvironment* — a localized environment created by an enclosure to isolate the product from contamination and people.

5.1.9 *product* — any unit intended to become a functional semiconductor device.

6 Requirements

6.1 *Measurement Methods and Instrumentation* — No single method of testing for static charge can determine a "safe" level. The amount of static charge, the distribution of static charge on an object, and the nature of the static discharge will all interact to determine if the charge level is safe. It will be difficult to determine levels that *guarantee* static related problems are totally eliminated. The goals of this guide are to assist the user in identifying static charge levels likely to cause problems in the semiconductor manufacturing facility, and to direct the user to static control methods appropriate to mitigate these problems. This guide is intended to provide the user with enough insight to define test methodologies for measuring static charge and for evaluating the methods to control it.

6.2 *ESD Damage — Direct Discharge*

6.2.1 When considering direct ESD damage to an object (e.g., product, reticle, or equipment), the important parameter is the current accompanying the charge transfer to or from the object. The charge may be transferred from facility and furniture surfaces, personnel, equipment parts, carriers, packaging materials, or anything else that contacts the object.

6.2.2 Established test methods exist for determining the threshold of damage to a particular object. When testing packaged devices, ESD simulators of various types are used. Refer to ESD Association standards ESD STM5.1, ANSI ESD STM5.2, and ANSI ESD STM5.3.1, JEDEC JESD22-A114 and JESD22-C101, or MIL-STD 883 for further information concerning device testing. There are no established standards for ESD simulator testing of wafers, reticles, or unpackaged semiconductor devices. ESD damage thresholds for these items may be significantly different than for packaged devices.

6.2.3 Once the damaging current level for a product is determined using an appropriate ESD simulator, the corresponding amount of charge is known from the ESD simulator operating parameters.

6.2.4 In the manufacturing facility, it is important to know the charge on any objects that might directly contact the product. Charge measurement methods using a coulombmeter and Faraday Cup are described in SEMI E78 and SEMI E43 for isolated conductors (including personnel), or small and moveable objects. The measurement methods of SEMI E43 can be used to establish that the charge levels on these objects will pose a hazard to products or reticles from a direct ESD event.

6.2.5 Electric field measurements on large and fixed objects, or insulators are less useful in estimating whether or not a damaging direct ESD event will occur. On objects that cannot be conveniently measured with a coulombmeter, Electrostatic Fieldmeter measurements can be useful in estimating the ESD threat, even though the measurement may be less quantitative than the coulombmeter measurement.

6.3 *ESD Damage — Induced Charge*

6.3.1 Charge may be induced on an object that results in ESD damage. Part of a product (e.g., epoxy package) or reticle (e.g., quartz substrate) may become charged and *induce* charge separation to occur on another part of the product (e.g., lead pins) or reticle (e.g., chrome traces). ESD will occur if the lead pins or chrome traces contact ground. Using a coulombmeter or Faraday Cup and the methods of SEMI E43, the end user should test product or reticles to determine the level of static charge at which ESD damage occurs.

6.3.2 Alternatively, either the product or reticles may be handled in proximity to another charged object. The field from this charged object induces charge on product or reticles, and ESD can result if the product or reticle contacts ground while in the presence of the field. Using an electrostatic fieldmeter and the methods of SEMI E43, the end user should test products and reticles to determine the acceptable levels of electric field from static charge.

6.3.3 It has been shown that a changing electric field causes ESD damage to reticles without ground contact occurring. A changing electric field can result at the reticle when an object in proximity to the reticle acquires a charge, the reticle or a charged object are in motion with respect to each other, or grounding conditions change the field between a charged object and the reticle (for example, due to robot handling). See references in Related Information 2. In areas of the manufacturing facility that produce or handle reticles, electric field from any charged object will need to be limited to levels that do not cause reticle ESD damage. Test methods for electric field are contained in SEMI

E43. There are currently no industry standards for determining the electric field sensitivity of reticles, but test methods do exist.

6.3.4 Finally, there is increasing anecdotal evidence that the *presence* of static charge on wafer surfaces is becoming an ESD hazard as gate oxide thicknesses become thinner. In the future, there may need to be further limits on allowable static charge on wafer surfaces to prevent ESD-related gate oxide damage during front-end semiconductor manufacturing. Further research is needed in this area.

6.4 *Particle Attraction*

6.4.1 Electrostatic attraction (ESA) of particles can occur due to the electrostatic field created by the charge on the surface of an object. Refer to SEMI E78 and SEMI E43 for an analysis of this effect and its measurement methods.

6.4.2 Particles may be attracted to charged facility surfaces, or directly to charged products or reticles. Subsequently, they may be dislodged from facility surfaces and transfer to products or reticles. Once on products or reticle surfaces they may cause either random or repeating defects.

6.4.3 Electrostatic particle deposition velocity depends only on electric field, particle size and particle charge. However, the number of particles deposited on a surface also depends on the particle concentration in the area and the length of the exposure time during which particle deposition occurs. SEMI E78 contains information to relate allowable electric field to ambient particle concentration and exposure time.

6.4.4 The measurement methods of SEMI E43 can be used to establish that the electric field from any facility surface meets the requirements of this document.

6.4.5 Charge is difficult to evaluate on large objects, especially insulators. Electric field measurements on these objects may be useful in estimating the risk that a damaging direct ESD event might occur. However, electric field measurements on insulators are highly qualitative and only provide a figure of merit as to the threat that these charges may represent to the ESD-sensitive device.

6.5 *Equipment ESD*

6.5.1 Equipment ESD immunity has been established at levels considerably higher than those that result in damage to product and reticles. If facility static charge limits shown in Table 1, of Section 12.5 are used to protect product and reticles, they will provide sufficient protection for the equipment.

6.5.2 Equipment ESD immunity is addressed, in general, through a number of international standards including SEMI E78, IEC 61000-4-2, and BS EN50082-2 for European CE compliance. Measurements are made using an ESD simulator, which is described in these standards.

7 Apparatus

7.1 *ESD Damage* — For measuring the charge generated on product, reticles, or carriers, the Faraday Cup test method is shown in Figure 1. Additional information on this test method is contained in SEMI E43.

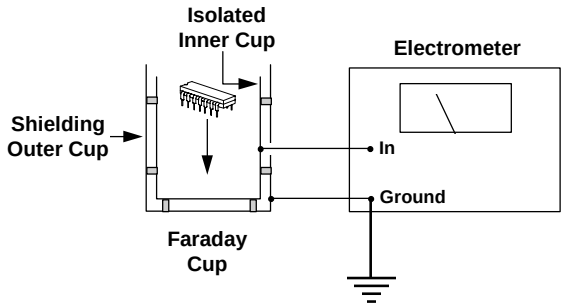

Figure 1
Faraday Cup Charge Measurement

7.2 When the object whose charge is to be measured is conductive, a nanocoulombmeter may be used. Additional information on this test method is contained in SEMI E43.

7.3 The instrument used for making electrostatic field measurements on large objects or surfaces is known as an electrostatic fieldmeter. Instructions concerning its use should be obtained from the instrument manufacturer and SEMI E43. The measurement configuration is shown in Figure 2.

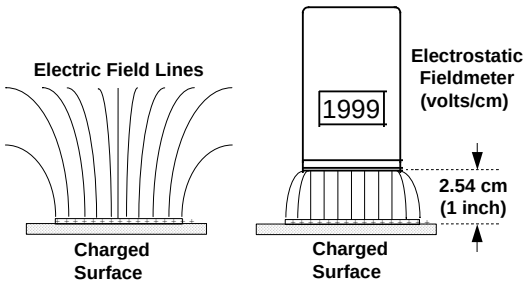

Figure 2
Electrostatic Field Measurement

7.4 For small objects or surface areas, an electrostatic voltmeter is appropriate.

8 Safety Precautions

8.1 *Personnel* — Static charges can create safety hazards during some semiconductor production processes.

8.1.1 ESA, ESD, and EMI events that result in the jamming or breakage of product in high-speed equipment may create a personnel hazard.

8.1.2 ESD events that produce sparks must be prevented in areas that use flammable or explosive chemicals or gases.

8.1.3 ESD events to personnel are usually not harmful, but they may result in an unwanted reflex, or "startle" reaction. This reflex may create a personnel hazard, particularly in the vicinity of moving equipment or where caustic chemicals are in use.

8.1.4 EMI resulting from ESD events may cause unpredictable behavior of robotics or other moving equipment that put personnel at risk.

8.1.5 It may be necessary to use additional static charge control methods, beyond those used inside the equipment, to minimize these personnel hazards.

8.2 *Measurement Safety* — Users should exercise caution while making static charge measurements in the vicinity of moving parts of production equipment, or in areas where static potentials on ungrounded conductors may exceed 30,000 V. Refer to SEMI E43 for additional measurement safety considerations.

9 Test Specimen

9.1 The user, material supplier, facility designer/builder, and equipment manufacturer should agree upon and document:

- Type(s) of testing to be performed
- Location of the testing (e.g., in a test chamber or in the actual use location)
- Who will do the testing
- Number and type of test samples
- Number of measurements
- Acceptable test results

9.2 The user, material supplier, facility designer/builder, and equipment manufacturer should agree upon and document all appropriate environmental conditions (e.g., temperature, humidity, dew point, airflow).

9.3 The user, material supplier, facility designer/builder, and equipment manufacturer should agree upon and document the operating history of equipment prior to, or during testing (e.g., warm-up time, type of carrier, number of products processed, operating speed).

10 Preparation of Apparatus and Sample

10.1 Depending on the type of testing to be done, consult the appropriate testing document for apparatus and sample preparation. See Section 4.

11 Calibration and Standardization

11.1 Depending on the type of testing to be done, consult the appropriate testing document for apparatus calibration and verification. See Section 4.

12 Procedures

12.1 See Sections 6 and 7 and the appropriate test methods of Section 4.

12.2 *ESD Damage*

12.2.1 Users should establish product damage thresholds for their products. Measurement methods for integrated circuits are described in SEMI E78 Related Information 1 and the documents contained in Section 4. Appropriate measurement methods for ESD damage to wafers, reticles, and other items may be adapted from the instrumentation used in these test methods.

12.2.2 In place of using the test methods referenced in Section 12.2.1, users may decide to follow the recommendations for acceptable electrostatic levels contained in Section 12.5 Table 1, which are based on product and reticle geometry. See Appendix 1 for more information.

12.2.3 Measurements of ESD damage levels are made in units of coulombs, or more conveniently in nanocoulombs (nC = 10^{-9} coulombs).

12.2.4 The Faraday Cup method is used to determine the static charge levels on products, carriers and equipment parts. See Section 7.1. Each item should be transported to the Faraday Cup in a way that does not alter its charge level. Consult the measurement equipment manufacturer's instructions for recommendations on how to achieve this.

12.3 *Electrostatic Field*

12.3.1 Users should work with cleanroom designers, material suppliers, equipment manufacturers and reticle suppliers to determine ambient particle levels, product exposure times during processing, and reticle damage levels due to electric field.

12.3.2 Electrostatic field measurements should be made at a minimum on all surfaces within the facility

that will come within 30.5 cm (12 inches) of ESD-sensitive items. Typical surfaces to measure would include construction materials, furniture, personnel, products, carriers, and equipment surfaces.

12.3.3 Measurements should be made in at least three different locations on any item. Locations should be separated by approximately three times the distance between the measuring instrument and the measurement location. For most electrostatic fieldmeters measuring at 25.4 mm (1 inch), the measurement locations will be 76.2 mm (3 inches) apart. Refer to SEMI E43 for additional measurement considerations.

12.3.4 Measurements of electrostatic field are expressed in V/cm or V/inch. Typically, five measurements should be sufficient to demonstrate compliance with the selected electrostatic level.

12.4 All elements of the semiconductor factory, including but not limited to construction materials, furniture, equipment, personnel, product, reticles, carriers, and transport and packaging materials, should meet the following electrostatic levels shown in Section 12.5 Table 1 for protection from problems caused by static charge.

12.5 It is desirable in this document to avoid confusion with SEMI E78 sensitivity levels, as well as to synchronize with the major changes in technology mapped in the International Technology Roadmap for Semiconductors (ITRS). Recommendations for acceptable static charge levels are listed in Table 1 and given for the major technology nodes of the 2003 ITRS that relate to the size of the features on the wafer.

Table 1 Recommended Facility Electrostatic Levels

Year Node	*Electrostatic Discharge, nC*	*Electrostatic Field, V/cm*	*V/inch*
2000 180 nm	2.5–10	200	500
2002 130 nm	2.0	150	375
2003 100 nm	1.5	125	300
2004 90 nm	1.0	100	250
2007 65 nm	0.5	70	175
2009 50 nm	0.25	50	125
2012 32 nm	0.125	35	88
2015 25 nm	0.1	25	63

12.5.1 Since many decisions to use static control materials will result in the permanent installation of these materials, users may want to consider the eventual use of their semiconductor facility in selecting the acceptable electrostatic level. For example, at startup the facility may be processing at 180-nm geometry, but in five years it is anticipated to be at 90 nm. The facility may need to be designed for the limits recommended for the 90-nm use.

12.5.2 The levels in Table 1 assume that the manufacturing facility is processing silicon semiconductors. Manufacturers of specialized components may need to choose lower levels. Examples are manufacturers of gallium arsenide semiconductors or magneto-resistive (MR) disk drive read heads, those experiencing significant losses due to contamination, or those using specialized equipment.

12.6 The levels listed in Table 1 have been determined as the result of an analysis of working conditions, or experiments done in operating semiconductor facilities. Justifications for these levels are found in Appendix 1. The actual levels to be used for any production area may be decided by agreement between the user and designer/builder of the facility.

12.7 Other levels may be appropriate under specific operating conditions and for specific devices.

13 Calculations

13.1 A series of five measurements should be made. The average of the five measurements should not exceed the recommended level. No measurement should exceed two times the recommended level.

14 Reporting Results

14.1 Data records should contain the following information:

- Description of the materials or equipment under test including model and serial numbers,
- Description of the factory operating conditions and environment,
- Measurement equipment and last calibration date,
- Description of objects measured and measurement locations,
- Humidity, temperature, and dew point at measurement location when measurements were made,
- Results of measurements,
- Personnel making the measurements, and
- Any other relevant comments.

15 Test Method Precision and Accuracy

15.1 The test methods referenced in this document do not guarantee precise measurements of static charge levels. Similarly, maximum static charge levels recommended in this document are not stated as precise requirements. Accuracy of approximately ± 20% is acceptable in all measuring instrumentation. At low static charge levels, or for more accurate measurements, alternative instrumentation and test methods may be needed.

15.2 To evaluate low levels of electric field strength or the voltage on an object, use an electrostatic fieldmeter or electrostatic voltmeter with the resolution and accuracy required. Under appropriate conditions, electrostatic voltmeters exhibit a high degree of accuracy and stability that is independent of the distance from the charged object. The electrostatic voltmeter probe can be located very close to a charged surface without arc-over, and it is able to resolve the field from a small charged object.

APPENDIX 1
DEVELOPING THE RECOMMENDATIONS FOR ELECTROSTATIC LEVELS

NOTICE: This appendix offers information related to the Electrostatic Levels contained in Section 12.5. It was approved as an official part of SEMI E129 by full letter ballot procedures on September 3, 2003.

A1-1 Recommended Levels

A1-1.1 The recommended charge and electrostatic field levels in this guide are not based on specific protection thresholds for individual devices or process tools. Rather, their aim is to classify the types of ESD events or static levels that are likely to be of concern. Facility designers and users should determine the types of events that are of most concern to their products and processes, to apply this guide to their needs. Information on specific device damage thresholds is best determined on an individual basis.

A1-2 Justification of Guide Recommendations in Section 12.5 Table 1

A1-2.1 *Recommendations for ESD Damage*

A1-2.1.1 An analysis of the recommended levels to protect semiconductor devices is found in Appendix 1 of SEMI E78. Related Information 1 of SEMI E78 discusses test methods for determining ESD damage thresholds for semiconductor devices. Devices are qualified according to the highest ESD stresses they can withstand without measurable change in their operating parameters. This section attempts to develop guide recommendations for minimizing ESD damage based on those discussions in SEMI E78.

A1-2.1.2 The information contained in SEMI E78 was developed with respect to semiconductors handled by equipment. It was current when published in 1998. Device damage thresholds continue to decrease as geometries get smaller, and although the classification systems discussed in SEMI E78 have not changed, more devices are falling into the more sensitive classifications.

A1-2.1.3 It is desirable in this document to avoid confusion with SEMI E78 sensitivity levels, as well as to synchronize with the major changes in technology mapped in the International Technology Roadmap for Semiconductors (ITRS). Recommendations for acceptable static charge levels are listed in Section 12.5 Table 1 and given for the major technology nodes of the 2003 ITRS, which relate to the size of the features on the wafer.

A1-2.2 *Charge Levels for ESD Damage*

A1-2.2.1 Related Information 1.1 discusses test methods for determining ESD damage thresholds for semiconductor devices. Devices are qualified according to the highest ESD stresses they can withstand without measurable change in their operating parameters. This section attempts to develop guide recommendations for minimizing ESD damage based on the discussion in Related Information 1.1.

A1-2.2.2 As discussed in Related Information 1.1.3, ESD Simulator testing uses different capacitances for each model. For Human Body Model (HBM) it is 100 pF, for Machine Model (MM) it is 200 pF, and for Charged Device Model (CDM) it depends on the capacitance of the actual device being tested. In any case, it is charge (charge = voltage × capacitance) that damages the device. It would seem appropriate, therefore, that the guide recommendations in Table 1 in Section 12.5 be stated in units of charge (e.g., nC).

A1-2.2.3 Based on industry testing reflected in device data sheets, there appears to be a wide range for ESD immunity in semiconductor devices, and it depends on the type of ESD simulator used. HBM-type ESD discharges are due to personnel handling and not likely to occur within equipment. Charged equipment parts contacting devices (i.e., MM) and charged devices contacting machine parts (i.e., CDM) are the most likely causes of ESD damage to devices in equipment.

A1-2.3 *Industry Device Damage Levels*

A1-2.3.1 The recommended electrostatic levels are based on the following industry classifications. Each of the test methods, (i.e., HBM, MM, and CDM) have a set of qualification levels defined. These are contained in Tables A1-1, A1-2, and A1-3 below.

Table A1-1 HBM Classification Levels

Class	*Voltage, V*
0	< 250
1A	250–499
1B	500–999
1C	1000–1999
2	2000–3999
3A	4000–7999
3B	≥ 8000

Table A1-2 MM Classification Levels

Class	*Voltage, V*
M1	< 100
M2	100–199
M3	200–399
M4	≥ 400

Table A1-3 CDM Classification Levels

Class	*Voltage, V*
C1	< 125
C2	125–249
C3	250–499
C4	500–999
C5	1000–1499
C6	1500–1999
C7	≥ 2000

A1-2.4 *Guide Recommendations*

A1-2.4.1 At the 180-nm technology node for the year 2000, it is assumed that devices (although some may withstand higher levels of ESD) pass testing at HBM Class 0 (250 V × 100 pF = 25 nC), MM Class M1 (100 V × 200 pF = 20 nC), and CDM Class C3 (500 V × 10 pF device capacitance = 5.0 nC).

A1-2.4.2 This guide recommends (Table 1 in Section 12.5) 2.5–10 nC at the 180-nm node in the year 2000. It is assumed, for this and all further recommendations, that the device capacitance is 10 pF.

A1-2.4.3 For major technology nodes, the allowable ESD levels have decreased approximately with the square of the ratio of the critical dimension. The assumption is that energy dissipation capability is proportional to the area of the feature.

A1-2.4.4 For example, in Table A1-4 at the 90-nm node this guide recommends approximately 25% of the 180-nm node or 1 nC, at the 50-nm node the value has changed to 0.25 nC, and at the 25-nm node the value is 0.1 nC. Intermediate technology years have been changed accordingly.

A1-2.5 *Recommendations for Particle Deposition*

A1-2.5.1 SEMI E78 Related Information 1.2.2 discusses the enhancement of particle deposition due to electrostatic fields from charges on the wafer surface. This section attempts to develop the guide recommendations for minimizing particle deposition based on that discussion.

$$N/A = cv_{elect}t \qquad (1)$$

where *N/A* equals the particle burden added to a wafer during exposure time *t*, to a particle concentration *c*, in an environment characterized by an electrostatic particle deposition velocity, v_{elect} .

Table A1-4 Guide Recommendations to Prevent ESD Damage

Year *Node*	*Electrostatic Discharge, nC*
2000 180 nm	2.5–10
2002 130 nm	2.0
2003 100 nm	1.5
2004 90 nm	1.0
2007 65 nm	0.5
2009 50 nm	0.25
2012 32 nm	0.125
2015 25 nm	0.1

A1-2.5.2 Target values for N/A are given in the International Technology Roadmap for Semiconductors (ITRS 2002 Defect Reduction chapter). These target values vary, depending on the type of product, the critical dimensions of the technology, the type of process, etc. An average of random particles added per process step is developed, and for purposes of this discussion will represent those resulting from particle deposition. The variables *c* and *t* are process step dependent and may or may not be controllable.

A1-2.5.3 The only variable in Equation 1 that depends on electrical forces is v_{elect} Both the particle charge and the electric field in the vicinity of the wafer affect the magnitude of v_{elect} Particle charge is generally unknown unless it is deliberately controlled by a neutralizing action, and in the absence of this condition, a Fuchs-type charge distribution is a reasonable assumption for the particle charge. This assumption was used to calculate the value of E_0, the electric field at which v_{elect} is equal to the particle deposition velocity from diffusion (dominant for small particles).

A1-2.5.4 Using the process step values of *c* and *t*, and the value of v_{elect} calculated from Equation 10 in SEMI E78 Related Information 1.2.2, the value of *N/A* for any process step can be estimated. Alternatively, having target values for *N/A* and *c*, and estimating the value of v_{elect} as outlined in the previous paragraph, allows one to calculate the tolerable value of *t*:

$$t = [N/A]/cv_{elect} \quad (2)$$

Using higher values of *N/A* in Equation 2 will increase the acceptable values of *t*. Accepting higher values of *c* will reduce max *t*.

A1-2.5.5 The value of the electrostatic field is initially calculated at a distance of one wafer radius from the wafer. While electrostatic field measurements can certainly be made at this distance, they are typically made at 2.5 cm (1 inch) with common instrumentation. This is described in SEMI E43. Measurements made at this smaller distance will be proportionally higher, but under varying measurement conditions, it is difficult to determine a precise relationship between electric field and measurement distance. To provide a safety factor, assume a linear relationship, rather than one proportional to the square of the distance. For example, with a 300-mm wafer, 3000 V/cm at 2.5 cm would result in 500 V/cm at 15 cm.

A1-2.5.6 In SEMI E78, calculations were based on a defect density $N/A = 0.016$ defects/cm^2 and a deposition velocity v_{elect} of 0.0105 cm/s. An example of the resulting calculations is found in SEMI E78 Appendix 1 Table A1-2.2, a portion of which is shown in Table A1-5.

Table A1-5 SEMI E78 Guide Table A1 – 2.2

E, V/cm at 2.5 cm	*N/A, defects/ cm^2*	*v_{elect}, cm/s*	*ct, s/cm^3*	*max t in Class 1, s*
200	0.016	0.0105	1.524	1220

A1-2.5.7 Tables A1-6 and A1-7 below are derived from Table A1-5 above, which is taken from SEMI E78 Appendix A1-2.2.2. They contain the same assumptions used for the SEMI E78 table, but reflect values for defect density (*N/A*) and particle deposition velocity contained in the ITRS 2002 document for each technology node. Assumptions are:

- Calculations are made for ISO Class 3 (formerly Federal Standard 209E Class 1) where $c \leq 0.00124$ particles/cm^3.
- As contained in both the 1999 and 2002 ITRS, particle deposition velocity is assumed to be 0.01 cm/s (2002 ITRS Yield Enhancement Chapter, Notes Table 95a). Calculations are made assuming the electrostatic deposition velocity, v_{elect}, is equal to this value.
- For N/A = 0.0141 defects/cm^2 as specified in the 1999 ITRS for the 180-nm node (Defect Reduction Chapter, Table 77, assuming "Random Defects" per mask layer are all the result of particle deposition), the corresponding table becomes:

Table A1-6 Modified SEMI E78 Guide Table A1 – 2.2

E, V/cm at 2.5 cm	*N/A, defects/ cm^2*	*v_{elect}, cm/s*	*ct, s/cm^3*	*max t in Class 1, s*
190	0.0141	0.01	1.41	1140

- The values from the 2002 ITRS (Yield Enhancement Chapter, Table 91) N/A = 0.0093 defects/cm^2 as specified for the 130-nm node, 0.0089 defects/cm^2 for the 100-nm node, 0.0059 for the 65-nm node, 0.0056 for the 45-nm node, 0.0043 for the 32-nm node, and 0.0044 for the 22-nm node technology are used.
- Calculations are normalized for an exposure time of 1200 s (i.e., E values multiplied by 1140/1200).
- Relationship of electrostatic field, technology node, and constant airborne particle concentration are shown in Table A1-7.
- The years and technology nodes shown in Table A1-7 correspond to those to be used in the 2003 ITRS.

A1-2.6 *Recommendations for Induced ESD Damage*

A1-2.6.1 The presence of electrostatic fields in semiconductor manufacturing areas also creates the potential for induced ESD damage. When an isolated conductor is placed in an electric field, a charge separation occurs in the conductor. If the conductor momentarily touches ground, a flow of charge will occur to the conductor. This flow of charge is a potentially damaging ESD event. If the conductor, now possessing excess charge, is removed from the electric field, a second ESD event can occur when the conductor contacts ground again.

A1-2.6.2 The most obvious example of these phenomena occurs once the semiconductor device is packaged. The package material is epoxy, an easily charged insulator. The electric field from the charged package induces a charge on the device leads. ESD events occur when the leads contact ground during processing.

Table A1-7 Electrostatic Field Levels – Limit Particle Deposition in a Class 1 Environment

Year Node	*N/A, defects/cm²*	*Electrostatic Field, V/cm*
2000 180 nm	0.0141	180
2002 130 nm	0.0093	120
2003 100 nm (2004) (90 nm)	0.0089	114
2007 65 nm	0.0059	75
2009 50 nm (2010) (45 nm)	0.0056	71
2012 32 nm	0.0043	55
2015 25 nm (22 nm)	0.0044	56

A1-2.6.3 A second problem for semiconductor manufacturing occurs in the presence of a changing electric field. This occurs when there is movement of isolated conductors within an electric field, or the field itself changes in magnitude. The result is that the charge, and hence the voltage, induced on the individual isolated conductors will not always be the same, creating a potential difference between the conductors. Under the right circumstances, ESD events can occur between conductors at different potentials. With the electric field changing, there is also the likelihood that multiple ESD events will occur.

A1-2.6.4 This phenomenon of charge induced by changing electric fields is mostly a concern in the handling of photomasks with μm and sub-micron feature sizes. While ESD damage occurred with 5× photomasks with 3 to 5-μm features, it was infrequent. At the 180-nm technology node, even 5× masks have sub-micron features and the trend is to 4× masks, making the feature sizes even smaller.

A1-2.6.5 The problem occurs because a photomask is basically a large collection of closely spaced, isolated conductors on an insulating quartz substrate. The substrate is easily charged, creating an electric field. The field changes whenever the spacing between the photomask and ground changes (e.g., during handling by robotics). Transporting the photomask, whether in static dissipative reticle carriers or not, exposes it to changing electric fields from other charged objects (e.g., equipment panels, windows, work surfaces, and equipment parts). The result is an increasing incidence of ESD damaged photomasks as geometries shrink.

A1-2.6.6 While there have been several studies documenting the existence of the field charging problem on photomasks, there is currently a need for further research to demonstrate the level at which it occurs for production facilities. A recent study (Montoya, et al.) was able to produce the following information:

1. Testing was done on a photomask test device with 1.5-μm gaps between features. Approximately 800 V/cm (2 kV/inch) of electric field was needed to cause damage.
2. Current production 180-nm photomasks are 4× with a nominal gap width of 0.72 μm (or less depending on the technology). ESD should occur at 400 V/cm (1 kV/inch) or less.
3. To avoid ESD on 180-nm photomasks, electric fields should be kept below 50% of the damage threshold, or 200 V/cm (500 V/inch).

A1-2.6.7 Table A1-8 below is based on these measurements. It is acknowledged that discharge phenomena may change at very small conductor spacing, and that the relationship to electric field may not be a linear function of the geometry. The values in Table A1-8 may need to be changed as more information becomes available.

Table A1-8 Electrostatic Field Levels – Limit Induced ESD Damage on Photomasks

Year Node	*Electrostatic Field Limits Induced ESD Damage, V/cm*	*Electrostatic Field Limits Particle Attraction, V/cm*
2000 180 nm	200 (200)	180
2002 130 nm	144 (150)	120
2003 100 nm	111 (125)	114
2004 90 nm	100 (100)	114
2007 65 nm	72 (70)	75
2009 50 nm (45 nm)	55 (50)	71
2012 32 nm	35 (35)	55
2015 25 nm (22 nm)	27 (25)	56

A1-2.7 *Guide Recommendations*

A1-2.7.1 This document recommends the values shown in parentheses in the second column of Table A1-8 of this Appendix and includes them in Section 12.5 Table 1.

A1-2.8 *Guide Recommendations for Equipment Malfunctions*

A1-2.8.1 Most semiconductor manufacturing equipment should comply with the ESD immunity requirements of the European Economic Community (EEC). The testing mandated by the EEC uses the test methods and ESD immunity levels specified in IEC/TS 61000-4-2. To test for compliance, measurements are made with an ESD simulator described by IEC/TS 61000-4-2. Equipment is required to pass a test involving the discharge produced by a 150-pF capacitor charged to 4000 V, or 600 nC.

A1-2.8.2 Users should note that the above test discharge level and properties (i.e. discharge voltage, discharge model and pulse rise time) may not be sufficient to predict actual discharges that occur in semiconductor production environments. In addition, the ESD immunity of equipment in an isolated test environment may change when it is installed in a production environment.

A1-2.8.3 The discharge test specified in IEC/TS 61000-4-2 is done at significantly higher charge levels than are recommended for objects in the facility in Table A1-2 of this Appendix. If the recommendations of Table A1-2 are followed, static charge levels should be low enough to prevent ESD-induced equipment malfunctions.

A1-2.8.4 If the recommended electrostatic levels regarding ESD contained in Section 12.5 Table 1 are not used, those contained in SEMI E78 should be used for equipment.

A1-3 References

SEMI E78 — Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment

Montoya, J. A., Levit, L., and Englisch, A., “A Study of the Mechanisms of ESD Damage for Reticles”, Electrical Overstress/Electrostatic Discharge Symposium Proceedings, 394-405 (2000)

Cooper, D. W., Miller, R. J., Wu, J. J., and Peters, M. H., "Deposition of Submicron Aerosol Particles During Integrated Circuit Manufacturing: Theory", *Particulate Sci. Technol. 8 (3 and* 4): 209-224 (1990)

Liu, B. Y. H., and Ahn, K. H., "Particle Deposition on Semiconductor Wafers", *Aerosol Sci. Technol. 6:* 215 - 224 (1987)

International Technology Roadmap for Semiconductors (1999, 2002, 2003)[8]

ISO 14644 – Cleanrooms and Associated Controlled Environments – Part 1 – Classification of Air Cleanliness[9]

8 International SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, USA (www.sematech.org)

9 Institute of Environmental Sciences and Technology (IEST), 5005 Newport Drive, Rolling Meadows, IL, 60008-38411, USA (www.iest.org)

RELATED INFORMATION 1
DEVICE SENSITIVITY MEASUREMENTS

NOTICE: The material contained in this related information is not an official part of SEMI E129 and is not intended to modify or supersede the guide in any way. These notes are provided as a source of information to aid in the application of the guide, and are to be considered reference material. Determination of the suitability of the material is solely the responsibility of the user. This related information was approved by full letter ballot procedures on September 3, 2003.

R1-1 ESD Damage

R1-1.1 *Introduction*

R1-1.1.1 ESD damage to devices occurs when they come into contact with personnel and facility or equipment surfaces. Either may store a residual charge large enough to destroy the device if a discharge occurs. It is also possible that charge stored on insulating parts of products or reticles will induce charges on their conductive parts. Discharges may occur between conductive parts at different potentials or when the conductive parts touch ground. The same types of induced charge can be produced when products or reticles are placed in the electrostatic field produced by static charge on facility or equipment surfaces that are insulative or isolated from ground. In the semiconductor industry, it has been established that significant proportions of customer field returns are attributed to damage resulting from ESD.

R1-1.2 *Description of ESD Damage Mechanisms*

R1-1.2.1 ESD failures are the result of either a current-induced phenomenon or a charge-induced phenomenon, and the damage can either be junction, contact, dielectric or oxide related. The apparent similarity in current-induced damage resulting from ESD due to human body model (HBM) discharges or machine model (MM) discharges results from the thermal nature of both of these processes. The HBM and MM damages result when the temperature (joule heating) of the region dissipating the ESD pulse energy reaches a critical value and melting occurs.

R1-1.2.2 The charged device model (CDM) predicts charge-induced phenomena. For CDM-type discharges, oxide punch through occurs when the ESD voltage applied across the oxide creates a high enough field to break down the oxide. Excessive current flow results, causing an oxide short, but there is no heat transfer (adiabatic process). It should be noted here that the time duration for typical ESD events from charged objects and personnel ranges from 10 to 100 ns, while CDM-type events occur in less than 1 ns.

R1-1.3 *Device Testing Models*

R1-1.3.1 *Human Body Model (HBM)* — The HBM is the oldest and the most widely used of the three ESD models. The model attempts to replicate the discharge when a charged human touches a device that is at a lower potential. Human capacitance and resistance have been chosen to be 100 pF and 1500 Ω respectively. The values were chosen after measurements were made on humans in varying positions with respect to their surroundings. The resulting discharge waveform has a double exponential shape with rise time range of 2–10 ns and a decay constant (1/e position) of 150 ± 20 ns. The typical peak currents range from 0.67 A at 1000 V to 2.67 A at 4000 V.

R1-1.3.2 *Machine Model (MM)* — The MM is described by the Electronic Industries Association of Japan (EIAJ) as a worst-case HBM. The model attempts to replicate the discharge from a metallic arm of an automatic handler coming into contact with the metallic leads of a semiconductor device. A capacitance of 200 pF and ideally zero resistance produces a sinusoidal decaying waveform with an effective pulse duration of 200 ns. The typical peak currents range from 1.75 A at 100 V to 14.0 A at 800 V. Note that MM failures occur at 5–10 times lower voltage than HBM.

R1-1.3.3 *Charged Device Model (CDM)* — The CDM in its purest form is actually a field-induced model because the device is actually part of model. This model attempts to describe a device which itself becomes charged due to an external field, or due to triboelectric charging of the device surfaces. During discharge the parasitics (i.e., capacitance, inductance and impedance) in the device play a significant role in the resulting failure. The discharge pulse is a sinusoidal waveform with an extremely fast rise time of less than 500 ps. The waveform decays rapidly with a total pulse duration of less than 5 ns. The peak currents range from 2.0 A at 250 V charging voltage to 18.0 A at 2000 V charging voltage.

R1-1.3.4 *Correlation Between Models* — Whether or not a correlation exists between HBM and MM is debatable. While some companies report a correlation

of roughly 10:1 between the two models, other companies have seen anywhere from 5–20:1 differences in passing voltages between the two models. There is also no established voltage correlation between CDM damage and HBM or MM ESD events. In equipment, ESD damage events will be related to the MM or CDM types of ESD. Users will need to determine the type of ESD hazard to their devices and choose the test method accordingly.

R1-2 ESD Laboratory Simulation Testing

R1-2.1 *Description of Test Methods* — Test procedures discussed here for ESD simulation conform to those established by the ESD STM5.1, ANSI ESD STM5.2, ANSI ESD STM5.3.1 and MIL-STD 883 Method 3015.7. Details are to be found in these standards. Devices are qualified at a level corresponding to the highest ESD stress they are able to withstand.

R1-2.2 S*imulation Test Results* — In general all units must be data-logged both pre- and post-stress test. Any leakage current equal to or greater than a specific amount (company dependent—typically 10 μA or less) is "flagged" as a failure, and any current shift greater than about 200 nA is marked on the record.

R1-2.3 *HBM Stress Testing* — A resistance-capacitance (R-C) network is used to simulate the ESD event. In an HBM ESD Simulator, a high voltage is used to charge the capacitor (100 pF) which discharges through the resistor (1500 Ω) into the device under test. The present standard test method requires a minimum of 2 discharges (i.e., 1 positive and 1 negative) per voltage level.

R1-2.4 *MM Stress Testing* — An R-C network is also used in the MM ESD Simulator for ESD testing. High voltage charges the capacitor (200 pF) which discharges through the short wire (~0 Ω) into the device under test. The present standard requires a minimum of 6 discharges (i.e., 3 positive and 3 negative).

R1-2.5 *CDM Stress Testing* — The package and lead frame of the device are charged by direct charging or field induction.

R1-2.5.1 For the Direct Charging Method, direct contact is made to one of the device leads connected to the substrate or bulk material of the device. The device is then discharged via a 1-ohm resistor to ground.

R1-2.5.2 For the Field Induced Method, the device is placed on a metallic charging plate with the device packaging material touching the plate. Applying a voltage to the charging plate raises the potential of the device. The induced voltage on the device is discharged to ground through a 1-ohm resistor that contacts each device lead. The present standard requires a minimum of 6 discharges (i.e., 3 positive and 3 negative) from each device lead.

R1-3 References

R1-3.1 *ESD Association Standards and Advisories*

ANSI ESD STM5.2 — Electrostatic Discharge Sensitivity Testing – Machine Model

ANSI ESD STM5.3.1 — Charged Device Model (CDM) – Component Level

ESD ADV11.2 — Triboelectric Charge Accumulation Testing

ESD S6.1 — Grounding - Recommended Practices

ESD STM5.1 — Electrostatic Discharge Sensitivity Testing – Human Body Model

ESD TR11-01 — Electrostatic Guidelines and Considerations for Cleanrooms and Clean Manufacturing

R1-3.2 *JEDEC Documents*

JESD22-A114 — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

JESD22-C101 — Field-Induced Charged-Device Model Test Methods for Electrostatic Discharge Withstand Thresholds of Microelectronic Components

JESD625 — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

R1-3.3 *Other Documents*

ANSI IEEE STD 142 — IEEE Recommended Practice for Grounding of Industrial and Commercial Power Systems

ANSI/NFPA 70 — National Electrical Code

MIL-STD 883 — Test Method Standard Microcircuits (Method 3015.7 – Electrostatic Discharge Sensitivity Classification), Defense Supply Center Columbus, P.O. Box 3990, Columbus, OH 43216-5000, USA (www.dscc.dla.mil)

Avery, L.R., "ESD Protection Structures to Survive the Charged Device Model (CDM)", Proceedings of the EOS/ESD Symposium, Orlando, FL (1987), pp. 186-191.

Avery, L.R., "Charged Device Model Testing: Trying to Duplicate Reality", Proceedings of the EOS/ESD Symposium, Orlando, FL (1987), pp. 88-92.

Cook, C., Daniel, S., "Characterization and Failure Analysis of Advanced CMOS Sub-Micron ESD Protection Structures", Proceedings of the EOS/ESD Symposium, Dallas, TX (1992), pp. 149-157.

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Renninger, R.G., Jon, M.C., Lin, D.L., Diep, T., Welsher, T.L., " A Field-Induced Charged-Device Model Simulator", Proceedings of the EOS/ESD Symposium, New Orleans, LA (1989), pp. 59-71.

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

R1-4 Acknowledgement

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RELATED INFORMATION 2
STATIC CONTROL METHODS

NOTICE: The material contained in this related information is not an official part of SEMI E129 and is not intended to modify or supersede the guide in any way. These notes are provided as a source of information to aid in the application of the guide, and are to be considered reference material. Determination of the suitability of the material is solely the responsibility of the user. This related information was approved by full letter ballot procedures on September 3, 2003.

R2-1 Static Charge Control

R2-1.1 It is usually impossible to eliminate static electricity from work areas, but with proper use of equipment and remedial procedures, most static problems can be controlled. Many approaches to controlling static charge have been tried over the years and it is clear that there exists no single method for controlling all static charge problems. However, it has been shown that a consistently applied process for static charge control greatly reduces problems associated with static electricity.

R2-1.2 One overriding issue should not be forgotten in the choice of static control materials and procedures. This is the need for compatibility with the cleanliness requirements of the area in which they are installed. A variety of static control materials are available, but some may not be cleanroom compatible due to issues of particle shedding, outgassing, or their chemical makeup. Each manufacturing area in the semiconductor factory should contain only those static control materials that are appropriate to the cleanliness requirements of the area. Consult ESD TR11 for additional information.

R2-2 Charge Generation

R2-2.1 *Triboelectric Charging*

R2-2.1.1 A fundamental law of nature states that an electrostatic charge is generated whenever two dissimilar materials contact and then separate. The materials themselves, intimacy of contact, speed of separation and a variety of other factors determine the amount or level of electrostatic charge that is generated during any given contact and separation event. Predicting the level of charge ahead of time is nearly impossible. Due to this unpredictability, the best that can be done in a factory setting is to understand that electrostatic charge generation will always occur. However, electrostatic charge generation can be measured and charge mitigation is normally a possibility. Reducing charge generation requires modification of surfaces to increase lubricity (i.e., reduce friction), increase conductivity (i.e., allows charges to relax and flow back), and make the surfaces chemically similar. Normally, more than one of the above actions is required to provide a low charge-generating system.

R2-2.1.2 While no intrinsic test method exists for the determination of triboelectric charge-generation properties, several practical evaluation techniques that apply to many factory situations may be found in ESD ADV 11.2.

R2-2.2 *Effect of Humidity on Charge Generation*

R2-2.2.1 It is generally understood that at constant temperature and at increased relative humidity the normally observed manifestations of static charge generation, such as static cling and static shocks, are greatly reduced. This does not mean that static charge is not present in the environment. Even at 90% RH, static charge may accumulate at a sufficient level to cause problems with some processes or cause damage to sensitive parts. Most factory processes, including cleanrooms, are run at a humidity level of 30–70%. Within this range, most of the humidity-dependant low-charging materials will function within their intended specifications. At lower humidity, surfaces dry out and may become a source of charge generation.

R2-2.2.2 Specifying a humidity level for a factory is a reasonably good idea if kept realistic. However, maintaining a minimal level of humidity may be very expensive in some areas of the world during normally dry winter months. It could be more important and cost effective to choose materials that provide the required function for charge generation or dissipation at the lowest expected humidity. Many parts of the world experience humidity levels of 10% or less during the winter months when outside air is brought inside and then heated to warm interior spaces. In these locations, which include the northern tier of US states and Canada, much of northern Asia, as well as northern Europe, careful attention to material selection is of major importance to assure adequate dissipative and low charge-generation performance.

R2-3 Grounding Conductors and Static Dissipative Materials

R2-3.1 The primary method of controlling static charge is grounding. If there is a path for the charge to flow to earth ground, the static charge on facility surfaces,

furniture, equipment, materials handled by the equipment, and any ESD-protective materials can be rapidly, and harmlessly, neutralized. Providing a path to ground brings everything to the same "zero" voltage electrical potential. All conductors in the environment, including personnel, should be electrically connected and attached to a known ground. It is important to note that insulators cannot lose their electrostatic charge by attachment to ground. Other charge-mitigating techniques (discussed in later sections) are required to neutralize excessive charge (i.e., electric field reduction) on the necessary insulators used in the electrostatic protective area (EPA), if their charge is considered a risk to sensitive parts handled in that location.

R2-3.2 Grounding methods and their measurement are described in detail in ESD S6.1. Information on electrical power grounding, which is a separate issue not addressed in this document, may be found in ANSI/NFPA 70, ANSI/IEEE STD 142, or appropriate country guidelines.

R2-3.3 Grounded conductors cannot maintain a static charge for very long. This is primarily dependent on the overall electrical resistance of the system. System resistance includes the resistance of the item being grounded, the contact resistance at the interface between items and the resistance in the actual grounding path. Since resistance of the system ground path determines the rate of discharge, it determines the amount of protection provided to ESD-sensitive devices. A permanent connection to ground will certainly prevent any charge from building up on an object and its subsequent transfer to an ESD-sensitive device. However, if an ungrounded, charged object contacts a material with too low a resistance to ground, a damaging discharge may occur. Even if no direct damage occurs, the ESD event creates EMI that may affect the operation of nearby production equipment.

R2-3.4 It should be noted that attaching a large metallic object (e.g., a stainless steel work surface) to ground through a high resistance will not prevent a discharge from occurring to the large metallic object. The high capacitance of the metallic object, with respect to the ESD-sensitive device, can still result in ESD damage or EMI.

R2-3.5 To prevent these conditions from occurring, the proper resistance for the ground path should be chosen. A class of materials has been developed, called static dissipative materials, which help to control discharge rates when materials are placed in contact. Static dissipative materials are created by lowering the resistivity of insulating materials through the addition of conductive particles, carbon particles, or chemical additives. When connected to ground, these materials slow the discharge rate from nanoseconds (typical for metal-to-metal contact) to as long as hundreds of milliseconds (depending on the size of the materials involved). While a discharge occurs to allow charge equalization with ground, a rapid, spark-producing discharge may not occur.

R2-3.6 In modern production equipment, the frame and other machine elements are normally metallic and thus conductive. These machine elements are often covered with static dissipative materials. In these design situations, the conductive frame should be attached to ground without any added resistance to provide a ground plane. The dissipative surface over the conductive frame provides charge-draining characteristics suitable for reducing risk of damage from rapid discharges.

R2-3.7 Static dissipative materials will need to retain their dissipative properties over the range of temperature and humidity conditions they will encounter, and not change significantly over time. In cleanrooms they should also meet requirements for avoiding micro-particle production and outgassing.

R2-3.8 Measurements of the resistance and resistivity of static dissipative materials are used to characterize their effectiveness in a static control program. Measurements should be made of the materials themselves, as well as their performance in their installation location. There are several measurement methods available depending on the application. Acceptable resistance ranges may depend on the ESD sensitivity of the products or photomasks that are handled in the area. These will need to be determined by the end user and the material suppliers.

R2-3.9 See the following test methods for resistance measurements of various items:

- ESD STM11.11: Surface Resistance Measurement of Static Dissipative Planar Materials
- ANSI ESD STM11.12: Volume Resistance Measurement of Static Dissipative Planar Materials

Both test methods characterize the resistivity or resistance of either static dissipative or conductive materials. These test methods can be used for construction materials, work surfaces, furniture components and most planar surfaces. They may also be used for packaging and transport materials.

- ANSI ESD S4.1 can be used to measure the resistance to a groundable point of these materials once they are in place. This can be done for work surfaces, construction materials (other than flooring), and other planar surfaces on furniture or equipment.

- ESD STM7.1 can be used to measure the resistance to a groundable point and resistance point-to-point for flooring,
- ANSI ESD STM12.1 can be used to measure the resistance to a groundable point for components of chairs.
- Resistance characteristics of the wrist straps used to ground personnel are covered in ANSI ESD S1.1.
- Cleanroom garments may be tested with the methods of ANSI ESD STM2.1.

R2-4 Static Charge Decay Time

R2-4.1 In some cases, it will be important to know the actual time it takes to remove a known amount of charge from an object.

- FED-STD-101 Method 4046 is often used for homogeneous materials.
- ANSI ESD STM4.2 is used to measure decay time of worksurface materials.

R2-4.2 Please be aware that static decay time may not fully characterize an item or a material. However, the information gathered in a decay time test may provide valuable insight into the electrostatic performance of an item or material when used in conjunction with other data such as resistance or resistivity. Decay time is only useful for materials with a high resistance/resistivity. For materials with resistance less than 10^{10} Ω, decay time does not apply because the equipment used is unable to measure decay times faster than 0.01 s.

R2-5 Measuring Static Charge Levels on Personnel

R2-5.1 Since personnel are mobile electrical conductors, they pose a significant hazard in any ESD-susceptible workplace. Thus, grounding of personnel is among the most important of all static control technical requirements. All of the industry program management standards accepted around the world require grounding of personnel as a foremost requirement. The most important consideration for personnel in a properly designed electrostatic protective area (EPA) is to maintain the resistance to ground at < 35 MΩ for operations handling parts sensitive to above 100-V Human Body Model sensitivity. For areas handling parts susceptible to less than 100-V HBM, the resistance-to-ground specification should be reduced to less than 10 MΩ to ground. Testing by the ESD Association has shown that at 35 MΩ to ground, a person can generate up to 100 V by vigorous movement such as sliding feet on the floor. At 10 MΩ to ground, the maximum voltage potential drops to about 6 V, a level that is highly unlikely to contribute to damaging even the most sensitive parts (consider the resistance discussion above). Standard wrist strap test methods are described and defined in ANSI ESD S1.1.

R2-5.2 For high-risk applications, advanced testing of personnel grounding systems may be required. A modern concept for continuous verification of personnel grounding includes wrist strap constant monitor systems. Choosing an appropriate system of constant monitoring requires an understanding of the actual performance measurement. To verify personnel grounding, it is important to measure the condition of the total system including the interaction of all the contact resistances, together with wrist strap bands and skin as well as ground cord, and shoes or shoe straps with skin or stocking moisture. Make sure all measurements include all the resistive interconnections of the grounding systems. Do not do system measurements without including all the components and personnel.

R2-5.3 A common grounding appliance for personnel is a wrist strap and connecting ground cord attached to a common point grounding terminal at a workstation. Since this methodology is most suitable for seated personnel, it is a stated requirement in all of the recognized static control programs (i.e., ANSI ESD S20.20, JEDEC JESD625, IEC 61340-5-1, and EN 61340-5-1 (formerly CENNELEC 100015-1).

R2-5.4 Another common methodology for grounding mobile personnel is a static control floor with static control footwear. If this concept is used as the primary grounding system, the resistance to ground has to be the same as for a wrist strap. A useful test method for resistance to ground of personnel through a floor-footwear system is ANSI ESD STM97.1. An alternative methodology in ANSI ESD S20.20 where the resistance to ground of the floor-footwear system is above 35 MΩ is to measure the voltage of a person relative to ground using ESD STM97.2. This method measures the charge generation characteristics of a person moving about on a floor.

R2-5.5 Clothing coverings using approved static control materials are often a requirement, especially in cleanrooms. When ESD issues are involved, garments need to be tested using approved test methods. A useful method is ANSI ESD STM2.1.

R2-5.6 Additional static control information, useful where personnel are concerned, may come from ESD TR03 for gloves and finger cots, ESD TR05 for garments, and ESD TR06 for triboelectrically charged garments.

R2-6 Neutralizing Charge on Insulators

R2-6.1 Static charge on a conductive or static-dissipative object can be controlled if the object is provided with a path for the charge to flow to earth ground. Unfortunately, grounding methods do not provide complete protection from static-related problems. Even when earth grounding is an option, it is subject to human error. In applications where contamination is an issue, additives and carbon particles used in static-dissipative materials may become sources of contamination themselves.

R2-6.2 While charge is mobile in a conductor (or in a static-dissipative material), in insulators charge is not mobile, and earth grounding is not an effective means of eliminating the static charge. More often than not, the product itself uses insulating materials, making earth grounding unavailable as an option. While silicon is a semiconductor, its oxide coating transforms it into an insulator. Polytetrafluoroethylene (PTFE) is used in many chemical processes, and quartz in high-temperature processes. Epoxy and ceramic packages are used for integrated circuits. Insulators are easily charged, retain their charge for long periods of time, and are often close to the product.

R2-6.3 Dealing with static charge on insulators and isolated conductors will often require the use of some type of ionization or surface-resistance modification. Ionizers are the most effective means of dealing with static charges on insulators and isolated conductors if the surface cannot be modified by coating or treatment with some form of surface-dissipative or low-charging "antistatic" agent.

R2-7 Ionization

R2-7.1 For purposes of static charge control, ions are molecules of the gases in air (i.e., nitrogen, oxygen, water vapor, carbon dioxide) that have lost or gained an electron. Ions are present in normal outside air but are removed when air is subjected to filtration and air conditioning. Ionization systems work by increasing the conductivity of the air by supplying ionized gas molecules. Another way of looking at the application of ionization is to interpret the function as supplying opposite polarity charge from the air to surfaces charged to the opposite polarity. When ionized air comes in contact with a charged surface, the charged surface attracts ions of the opposite polarity. As a result, the static charge that has built up on products, equipment and surfaces is neutralized.

R2-7.2 The most common methods of producing air ions are radioisotopes and "corona discharge" resulting from the electric field created when high voltage is applied to a sharp point.

R2-7.3 The radioisotope most commonly used to produce ionization is polonium-210, an alpha particle emitter. The alpha particle collides with the surrounding gas molecules, dislodging electrons. Gas molecules that lose an electron become positive ions. The free electron is quickly captured by another neutral gas molecule, creating a negative air ion. Note that the process always creates pairs of positive and negative ions.

R2-7.4 The corona discharge method produces a very high electric field that interacts with the electrons in the surrounding gas. The polarity of the ions depends on the polarity of the high voltage on the emitter point. Ionizers using the corona discharge method will often include some type of monitoring and feedback circuitry to assure that equal numbers of positive and negative ions are created.

R2-7.5 Ions of opposite polarity to the charged surface are required. Either polarity of static charge may be created on facility and equipment surfaces, or on the product. Ionizers may be installed on the ceiling of the room or may be hung from the ceiling using appropriate mounting methods. Ionizers are installed in minienvironments, particularly in the product load and unload areas. Ionizers may also be installed in the interior of process equipment. No single ionizer type or installation location is sufficient to solve all the static problems in the semiconductor facility.

R2-7.6 Ionizers should deliver ionization over a wide range of humidity and temperature conditions. Back-end assembly and test areas often do not have the level of temperature and humidity control found in front-end wafer production. Ionizers installed in the cramped spaces of production equipment will be close to the product, in areas surrounded by grounded metal parts. Ionizers should isolate the emitter points from both the product and adjacent grounded surfaces. Ionizers should produce sufficient ions to discharge static on surfaces and on products moving at high speeds despite losses to ground. Most ionizers require maintenance and periodic verification of their performance. The appropriate ionizer installation will need to be engineered for each specific application.

R2-8 Packaging Materials

R2-8.1 *Types of Packaging*

R2-8.1.1 Many forms of flexible and rigid packaging are used to protect ESD-susceptible items. Bags, boxes, wraps, tape and reel, pouches, cushioning foams, totes, tubes and numerous other forms of containers are available for any imaginable application. Each of these container forms is available in an ESD-protective version. Application in cleanroom environments adds

additional requirements to the ESD-protective packaging properties. Some of these considerations may actually preclude the ability to provide ESD protection. Therefore, there may often be a tradeoff between ESD protection, cleanliness, and other required material properties.

R2-8.1.2 The dissipative property for ESD protection requires some type of chemical, metallic or elemental additive to the bulk of the material or the surface of an ESD-protective item. Adding a highly conductive layer within the structure of the material or item provides the electrostatic-shielding property. Any additive or treatment may contribute to contamination concerns for application in cleanrooms.

R2-8.1.3 Making a material low charging ("antistatic") requires modification of the surface to decrease surface resistance and reduce friction. Often, low charging materials allow a transfer of materials to contacting surfaces to make the actual surfaces similar in chemistry. Materials with chemically similar surfaces usually do not show high levels of charge generation when placed into contact and then separated from each other. A downside to this process is the potential contamination issue that may be involved if the materials are used in clean areas. Take care in selecting low-charging materials if cleanliness is a major issue. This concern includes ionic contamination, non-volatile-residue and outgassing.

R2-8.2 *Material Guidelines*

R2-8.2.1 *Physical Guidelines* — The required material physical properties depend on the application involved. The selection process for a packaging material or system should consider all of the physical attributes generally associated with protecting an item during transit or storage. The physical requirements normally evaluated for any packaging system and associated test methods are shown in Table R2-1.

Table R2-1 Packaging System Physical Properties

Physical Properties	*Test Method*
Tensile Strength	ASTM D882
Elongation	ASTM D882
Tear Strength	ASTM D1922
Puncture Resistance	FED-STD-101/2065
Seam Seal Strength (if applicable)	ASTM F88
Light Transmission	ASTM F1003
Moisture Vapor Transmission (if applicable)	ASTM F1249
Light Transmission Rate (if applicable)	ASTM D1003

R2-8.2.2 *ESD-Protective Packaging Guidelines* — The type of packaging required for ESD-susceptible items depends on where the item is going. Packaging materials used inside of an ESD-protected work area are static dissipative or low charging. When sensitive items are moved outside of the protected area, the level of protection should increase to include electrostatic discharge shielding. Some extremely sensitive items may require additional EMI or RFI protection provided by heavier layers of shielding. Materials that provide increased shielding may also provide moisture barrier protection for enclosed items. The necessary electrical properties for packaging materials that are normally evaluated are shown with their associated test methods in Table R2-2.

Table R2-2 ESD-Protective Packaging Properties

Electrical Properties	*Test Method*
Surface Resistance	ESD STM11.11
Volume Resistance	ANSI ESD STM11.12
Shielding	ANSI ESD S11.31
Static Decay	FED-STD-101/4046

R2-8.2.3 *Contamination Control Guidelines* — Contamination issues are not limited to particles. Plastic processing additives to plastic packaging and handling materials, chemical and molecular compatibility should also be of concern. Users can evaluate plastic packaging and handling materials using published standard test methods. There are multiple test methods and procedures to identify contamination properties, as shown in Table R2-3. The user is advised to select the method best suited to their products that require protection.

Table R2-3 Contamination Control Properties

Contamination Properties	*Test Method*
Particles	ISO Std 14644
	IEST-STD-CC1246D
	IDEMA M9
	ARP 598
	KSC-C-123
Non-Volatile Residue	IDEMA M7
	ASTM E1235
	ASTM F331
	IPA extraction method
Outgassing	IDEMA M11 Dynamic Headspace Analysis
	ASTM E595
Ionics	IDEMA M12
	Extractable/leachable cation levels by ion chromatography

R2-9 Problem of Controlling Static Charge in Manufacturing Equipment

R2-9.1 The interior of high-speed production equipment is a challenge to static control methods. The high cost of production space requires equipment occupying the space to be compact and operate at as high a speed as practical. Product moves through small spaces at high speed by a variety of robotic and other mechanisms. Triboelectric charging (i.e., charge generation due to friction or contact and separation of dissimilar materials) and contact with ground are almost unavoidable.

R2-9.2 Grounding of equipment parts that contact the product presents added difficulties when the equipment parts are moving at high speeds. Dissipating charge from insulating surfaces and integrated circuit (IC) packages may be difficult if the charged surfaces are not accessible. Using ionizers in these confined spaces presents challenges.

R2-9.3 Measuring the effectiveness of static control methods in equipment will take some ingenuity. Test methods are contained in SEMI E78 as well as ESD SP10.1.

R2-10 Measurement of Charge and Potential on Moving Objects

R2-10.1 The fundamental problem in measuring accumulated charge on moving items in-situ is that only the static voltage or electrostatic field can be measured and not the actual charge. Direct measurements of static charge can be made with a coulombmeter or Faraday Cup (Pail), but only on stationary objects. Therefore, any measurements or alarm limits for moving objects can be set only in terms of accumulated static voltage or electric field.

R2-10.2 Another difficulty in measuring the static voltage or electric field from accumulated charge on moving items in a manufacturing process is the response time of the instrumentation. Non-contact instruments measure the electric field emanating from the surface of a charged object and this takes a finite amount of time. While some instrument technologies are faster than others, the measurement tools selected for any application should consider the speed of the process. A similar situation occurs in selection of mitigation techniques, in particular ionizers, as speed of neutralization depends solely on the number of ions present in the immediate environment.

R2-10.3 Electrostatic charge on an object (has to be a conductor to be accurate) is related to the electrical potential between the object and ground and the capacitance of the object relative to ground and the surroundings. There is a measurable relationship between an electric field measurement and the potential of the conductive object. For insulators, electrostatic charge cannot be determined by measuring electric fields. The electric field measurement on an insulator does not directly relate to electrostatic charge so therefore it cannot be used to determine the level of electrostatic hazard directly. A charged insulator can only discharge from a very small area upon contact. The electric field from a charged insulator causes damage only when it is of sufficient strength and the ESD-susceptible item is grounded while in the presence of that electric field.

R2-10.4 ESD-instrument manufacturers are developing new instruments that have improved response time over earlier offerings. Much of this effort supports ESD SP10.1, which describes measurement of voltage and charge in Automated Handling Equipment. These instruments will enable static measurements, even in high-speed automated equipment.

R2-10.5 Non-contact voltmeters are an important instrument type for measuring the electric field from charged objects. Reducing the response time for this class of instruments has been of major importance to allow meaningful measurement in moving systems.

R2-10.6 Although the coulombmeter and Faraday Cup can only be used to measure static charge on stationary objects, they can still be useful in understanding the charge generation characteristics of parts traveling through process paths in component handling equipment. Direct charge measurements combined with estimates of electrical potential from the electric field from a charged object can be used to determine appropriate ionization levels, surface treatment needs, grounding faults and provide insight into ESD risks associated with component movement.

R2-11 Standards and Process Control

R2-11.1 Without any doubt, the most important aspect of electrostatic control today is the advance made in standardization and process control. Several industry standards that cover the development and implementation of an ESD Control Program were released in the years since 1999. The four most important standards are as follows:

- IEC 61340-5-1 — This document is a result of international cooperation at the International Electrotechnical Commission - Technical Committee TC 101 – Electrostatics. The companion User Guide IEC 61340-5-2 offers considerable guidance that may assist the new practitioner in ESD control.

- EN 61340-5-1 (formerly CENNELEC100015) — As a European Normative Standard (EN), this document has considerable influence among the European Common Market (ECM) countries and those that supply products to the ECM. The content of this document is identical to IEC 61340-5-1.
- JEDEC JESD625 — A revision of EIA 625, this document provides a great deal of information regarding ESD-program planning, implementation and auditing. The technical requirements are harmonized fairly well with the above referenced documents.
- ANSI ESD S20.20 — Technical requirements are similar to those stated in the above documents but the administrative requirements are quite different. ANSI ESD S20.20 was written to comply with ISO 9001-2000 type requirements for validation, verification and maintenance. Adopted by the US Department of Defense (DoD), National Aeronautics and Space Administration (NASA), Food and Drug Administration (FDA), and numerous corporations, ANSI ESD S20.20 is the only ESD-program standard that has an official certification program. ISO 9000 registrars have been trained and others are in training at this time to allow them to provide officially recognized audits leading to certification granted by the ISO registrar and the ESD Association.
- The ESD Association is the certifying body that recognizes trained registrar companies. At this time, four registrar companies have trained personnel on staff that can support certification audits throughout most of Asia, North America and much of Europe. Numerous other registrars are being asked by their ISO/QS clients about ANSI ESD S20.20 certification so the list of certified registrars is expected to grow over time.

R2-12 References

R2-12.1 *SEMI Standards*

SEMI E78 — Electrostatic Compatibility – Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment

R2-12.2 *ASTM Standards*

ASTM D882 — Standard Test Method for Tensile Properties of Thin Plastic Sheeting

ASTM D1003 — Standard Test Method for Haze and Luminous Transmittance of Transparent Plastics

ASTM D1922 — Standard Test Method for Propagation Tear Resistance of Plastic Film and Thin Sheeting by Pendulum Method

ASTM E595 — Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in A Vacuum Environment

ASTM E1235 — Standard Test Method for Gravimetric Determination of Nonvolatile Residue (NVR) in Environmentally Controlled Areas for Spacecraft

ASTM F88 — Standard Test Method for Seal Strength of Flexible Barrier Materials

ASTM F331 — Standard Test Method for Nonvolatile Residue of Solvent Extract from Aerospace Components (Using Flash Evaporator)

R2-12.3 *ESD Association Standards and Advisories*

ANSI ESD S1.1 — Evaluation, Acceptance, and Functional Testing of Wrist Straps

ANSI ESD S4.1 — Worksurfaces – Resistance Measurements

ANSI ESD S11.31 — Evaluating the Performance of Electrostatic Discharge Shielding Bags

ANSI ESD S20.20 — Standard for the Development of an ESD Control Program

ANSI ESD STM2.1 — Resistance Test Method for Electrostatic Discharge Protective Garments

ANSI ESD STM4.2 — Worksurfaces – Charge Dissipation Characteristics

ANSI ESD STM11.12 — Volume Resistance Measurement of Static Dissipative Planar Materials

ANSI ESD STM12.1 — Seating Resistive Characterization

ANSI ESD STM97.1 — Floor Materials and Footwear – Resistance in Combination with a Person

ESD ADV11.2 — Triboelectric Charge Accumulation Testing

ESD S6.1 — Grounding – Recommended Practice

ESD SP10.1 — Automated Handling Equipment

ESD STM7.1 — Floor Materials – Resistive Characterization of Materials

ESD STM11.11 — Surface Resistance Measurement of Static Dissipative Planar Materials

ESD STM97.2 — Floor Materials and Footwear - Voltage Measurement in Combination with a Person

ESD TR02 — High Resistance Ohmmeters – Voltage Measurements

ESD TR03 — Glove & Finger Cots

ESD TR05 — Consideration for Developing ESD Garment Specifications

ESD TR06 — Static Electricity Hazards of Triboelectrically Charged Garments

ESD TR11 — Electrostatic Guidelines and Considerations for Cleanrooms and Clean Manufacturing

R2-12.4 *Federal Standards*

FED-STD-101/4046 — Electrostatic Properties of Materials

FED-STD-101/2065 — Puncture Resistance and Elongation Test (1/8 Inch Radius Probe Method)

R2-12.5 IDEMA Documents

IDEMA M7 — Organic Contamination as Nonvolatile Residue (NVR)

IDEMA M9 — Particulate Contamination Test Methods for Hard Disk Drive Components

IDEMA M11 — General Outgas Test Procedure by Dynamic Headspace Analysis

IDEMA M12 — Measurement of Extractable /Leachable Cation Contamination Levels on Drive Components by Ion Chromatography (IC)

R2-12.6 *IEC Documents*

IEC EN 61340-5-1 — Electrostatics – Part 5.1: Protection of electronic devices from electrostatic phenomena — General Requirements.

IEC EN 61340-5-2 — Electrostatics – Part 5.2: Protection of electronic devices from electrostatic phenomena – Users' Guide – Elements of a Static Control Program

R2-12.7 *Other Documents*

ANSI IEEE STD 142 — IEEE Recommended Practice for Grounding of Industrial and Commercial Power Systems

ANSI NFPA 70 — National Electrical Code

ARP 598 — The Determination of Particulate Contamination in Liquids by the Particle Count Method

ISO 14644 — Cleanrooms and Associated Controlled Environments

NASA KSC-C-123 — Specification for Surface Cleanliness of Fluid Systems

IEST-STD-CC1246D — Product Cleanliness Levels and Contamination Control Program

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

R2-13 Acknowledgement

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RELATED INFORMATION 3
MEASURING ELECTROMAGNETIC INTERFERENCE FROM ESD

NOTICE: The material contained in this related information is not an official part of SEMI E129 and is not intended to modify or supersede the guide in any way. These notes are provided as a source of information to aid in the application of the guide, and are to be considered reference material. Determination of the suitability of the material is solely the responsibility of the user. This related information was approved by full letter ballot procedures on September 3, 2003.

R3-1 Background

R3-1.1 Electrostatic discharges (ESD events) generate strong electromagnetic fields that cause undesirable behavior of electronics equipment generally by inducing extraneous voltages and currents into its circuits. There are many other sources of electromagnetic interference (EMI) in the semiconductor-manufacturing environment that also cause similar effects. EMI is propagated via different means such as air, cables and even imperfectly installed grounding networks.

R3-1.2 There are several regional and international standards regulating EMI susceptibility and parasitic emission of electronics products. Compliance of equipment with those standards is not a guarantee of complete immunity to EMI for several reasons, among which are:

- EMI conditions in semiconductor manufacturing environments often exceed the limits set forth by those standards.
- EMI performance of equipment can be substantially affected by installation, although EMC compliance testing does not take this into account.
- Interconnection of tools in the actual production environment creates a network of tools, which has its own EMI properties that are never tested during product design and approval cycle.

There are neither guidelines nor regulations at the moment to guide EMI-conscious design of facilities or to properly maintain them in that regard. It would be beneficial to provide (at minimum) guidelines to cleanroom designers and maintenance personnel to assist them in implementing good EMI practices in their facilities.

R3-2 EMI GENERATION

R3-2.1 Controlling EMI generation is a key component in EMI management. There are several types of generators of electromagnetic emission that can eventually cause EMI.

- ESD events (discharges)
- Parasitic emission from equipment
- Intentional emission from equipment that uses electromagnetic fields as a part of the process

R3-2.2 An *ESD event* is characterized by a very rapid transfer of electric charges. As a result, a very fast transient electromagnetic field is generated. The effect on the equipment is determined not only by the voltage that was discharged by the ESD event, but also by the charge that was dissipated during the event and the properties of contact. Another important parameter in assessing EMI impact of ESD events is the propagating properties of the discharging parts. More effective antennas lead to a higher magnitude of electromagnetic field.

R3-2.3 *Parasitic emissions from equipment* are a side product of normal operation of equipment. Though FCC, CE or similar regulations tightly control parasitic emission, in actual installations these emissions are often higher than expected. This is often attributed to high tool densities, extra long cabling, partially engaged connectors, and often-open covers that are supposed to attenuate electromagnetic emission from these cables.

R3-2.4 *Intentional radiation* generated by some types of tools causes substantial EMI as a part of normal operation. Examples include CVD tools and ion implanters.

R3-2.5 *EMI Propagation*

R3-2.5.1 Controlling the propagation path is another key component in EMI management. Electromagnetic field propagation paths include:

- Radiated – via air
- Conducted – via cables and wires
- Combined – an example of such is EMI picked up from the air by a cable or a wire and carried into equipment as a conducted emission.

R3-2.5.2 Poor grounding and power distribution networks provide paths for EMI to propagate from one tool to another. It is not uncommon to witness EMI from one corner of a cleanroom to manifest itself in another, distant corner.

R3-2.6 The following categories of EMI are recommended for consideration in setting limits:

- Continuous radiated emission
- Continuous conducted emission
- Transient radiated emission
- Transient conducted emission
- EMI levels on the ground and on the power lines

It is anticipated that FCC and CE regulations would be considered as one of the factors in setting the limits, but surveys of the actual environment in the factory will also need to be considered.

R3-3 EMI Effect on Equipment

R3-3.1 There are three main ways EMI can affect equipment:

R3-3.1.1 *Destruction* — The signals created by EMI in the circuit exceed the breakdown threshold of components, which leads to their destruction. This is especially relevant to conducted EMI.

R3-3.1.2 *Malfunction* — EMI injects pseudo-legitimate signals into the circuit, which leads to that circuit's malfunction. Such malfunction may range from complete lockup to unwanted operation of the tool. This is frequently misdiagnosed as software errors. Often, this type of malfunction involves several tools connected together.

R3-3.1.3 *False Sensor Readings* — Signals induced by EMI add to the signals coming from sensors and leads equipment to misread sensor data.

R3-4 EMI Measurements

R3-4.1 Measuring EMI can be a very effective tool in ESD management in the cleanroom, as EMI is a signature that ESD events are occurring. The following are some of the parameters and test methods that are recommended to be checked during such audits.

R3-4.2 *Radiated EMI Levels Near Equipment* — Both continuous and transient (peak) should be measured and identified.

R3-4.3 *Conducted EMI on Cables* — Both continuous and transient (peak). Due to practical considerations, an acceptable method will have to be devised to measure conducted EMI on hard-to-reach cables.

R3-4.4 Electromagnetic emissions generated by ESD events have unique properties. These include:

- Very short rise time – as short as hundreds of picoseconds,
- Very short duration – from a few nanoseconds to several hundred nanoseconds,
- Very broad frequency range (up to several GHz), and
- Often high magnitude.

There are several types of equipment available to detect and measure electromagnetic fields from ESD events.

R3-4.5 *AM Radio*

R3-4.5.1 Since electromagnetic fields from ESD events are manifested as short bursts of energy, they may be detected by a conventional AM radio tuned to a frequency free of radio stations. The radio produces "clicks" when it detects ESD events. The AM radio has difficulties picking up weak and very rapid discharges, and in industrial environments it is likely to pick up noise from normal equipment operation.

R3-4.6 *EMI Locators*

R3-4.6.1 Several types of EMI Locators are available, including portable handheld types and larger instruments. The simplest type provides both a visual and audible indication of the transient EMI from an ESD event. Although it can discriminate between two sensitivity levels for EMI, it gives no information regarding the magnitude of the ESD event that produced the EMI. Their frequency response is also limited to approximately 150 MHz and they may miss the faster EMI signals.

R3-4.6.2 A second type of EMI Locator is a general-purpose electromagnetic field strength meter with a bandwidth (up to 2 GHz) to measure EMI from ESD events. It has a directional antenna to help identify sources of emission, and provides outputs for emission levels and the counting of ESD events, including time stamping. This can be very useful in correlating ESD events with equipment malfunctions. Some units will also provide discrimination of multiple ESD events and provide output signals directly to a computer or factory management system.

R3-4.7 *High-Speed Storage Oscilloscopes*

R3-4.7.1 An oscilloscope equipped with proper antennae provides the most comprehensive information about waveform and magnitude of EMI caused by ESD events. The minimum requirements for an oscilloscope used for this purpose are a 500-MHz bandwidth and a 5-gigasamples/s sampling rate. Instruments with lesser performance specifications would either miss or misinterpret EMI parameters.

R3-4.7.2 The use of a high-speed oscilloscope should be accompanied by the use of a proper antenna for receiving the electromagnetic fields. For time domain

measurements it is important to use an antenna with a flat frequency response since frequency correction that is common in the frequency domain is not possible for time domain measurements. Another important note is that a typical oscilloscope captures only one event (i.e., first or last one, depending on trigger setting), missing multiple events that are common.

R3-4.7.3 Spectrum analyzers common in EMC test and wireless communication are not practical for detecting EMI from ESD events due to their unacceptably low acquisition speed.

R3-4.8 Below is comparison Table R3-1 of EMI/ESD measurement instruments.

R3-5 EMI and Ground

R3-5.1 An essential component of EMI management is a consideration of EMI in grounding. High impedance to ground at high frequencies prevents EMI from being dissipated. Long ground wires act as receiving antennae that inject high-frequency signals into tools. A common ground for several tools, with high impedance to the rest of the grounding network, facilitates propagation of EMI from one noisy tool to another.

R3-6 Related Documents

R3-6.1 *SEMI Standards*

SEMI E33 — Specification for Semiconductor Manufacturing Facility Electromagnetic Compatibility

R3-6.2 *ANSI Documents*

ANSI C63.13 — American National Standard Guide on the Application and Evaluation of EMI Power-Line Filters for Commercial Use. (http://standards.ieee.org/reading/ieee/std_public/description/emc/C63.13-1991_desc.html)

ANSI C63.16 — American National Standard Guide for Electrostatic Discharge Test Methodologies and Criteria for Electronic Equipment. http://standards.ieee.org/reading/ieee/std_public/description/emc/C63.16-1993_desc.html

R3-6.3 *EN / IEEE Documents*

EN 61000-4-2 / IEC 61000-4-2 — Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques. Section 2: Electrostatic discharge immunity test (ESD).

EN 61000-4-3 / IEC 61000-4-3 (ENV 50140 & ENV 50204) — Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques, Section 3: Radiated, radio frequency, electromagnetic field immunity test

EN 61000-4-4 / IEC 61000-4-4 — Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques. Section 4: Electrical fast transient / burst immunity test IEC 61000-4-4-am2 to Ed. 1:2001

EN 61000-4-5 / IEC 61000-4-5 (ENV 50142) — Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques. Section 5: Surge immunity requirements

EN 61000-4-6/ IEC 61000-4-6 (ENV 50141) — Electromagnetic compatibility (EMC) – Part 4-6: Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields

EN 61000-6-2 — Electromagnetic compatibility (EMC) – Part 6-2: Generic standards—Immunity for industrial environments.

R3-6.4 *IEEE Documents*

IEEE 518 — IEEE Guide for the Installation of Electrical Equipment to Minimize Electrical Noise Inputs to Controllers from External Sources (http://standards.ieee.org/reading/ieee/std_public/description/emc/518-1982_desc.html)

Table R3-1 EMI/ESD Measuring Instruments

Instrument	*Ease-of-Use*	*Cost*	*Sensitivity*	*Multiple Discharges*	*Event Magnitude*	*Event Count*
AM Radio	Easy	$	Low	No	No	No
EMI Locators	Easy to Medium	$$-$$$$	Medium to High	Some	High/Low to Full Range	Some
High-Speed Storage Oscilloscope	Difficult	$$$$$	High	No	Full Range	Some

R3-7 ACKNOWLEDGEMENT

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SEMI E131-0304
SPECIFICATION FOR THE PHYSICAL INTERFACE OF AN INTEGRATED MEASUREMENT MODULE (IMM) INTO 300 mm TOOLS USING BOLTS-M

This specification was technically approved by the Global Physical Interfaces & Carriers Committee and is the direct responsibility of the North American Physical Interfaces & Carriers Committee. Current edition approved by the North American Regional Standards Committee on December 4, 2003. Initially available at www.semi.org February 2004; to be published March 2004.

1 Purpose

1.1 This document establishes the specification for the interface requirements between an integrated measurement module (IMM) and 300 mm tools using an interface as defined by SEMI E63 (BOLTS-M).

NOTE 1: The 1997 and 2000 SIA roadmaps call for the implementation of metrology integrated with process tools. Such technology is important as specifications tighten the cost of monitor substrates at larger size increases, and as materials and processing steps become more complex.

NOTE 2: The 300 mm equipment generation offers an opportunity for integration of measurement equipment modules in a configuration that could be standard across different tools.

1.2 The standard will permit the tool suppliers, robotics suppliers, and measurement module suppliers, to provide plug and play integrated measurement solutions on a mechanical level.

1.3 It is the purpose of this standard to facilitate process monitoring through rapid access to measurement data, to reduce material handling between process and measurement equipment, and to provide the opportunity to increase process monitoring with a minimum or no decrease in throughput.

2 Scope

2.1 This standard is intended to set an appropriate level of specification that places minimal limits on innovation while ensuring modularity and interoperability at all mechanical interfaces. It establishes the mechanical interface specifications for integration of measurement modules intended for, but not limited to, 300 mm process tools using a BOLTS-M interface, while utilizing existing SEMI Standards as much as possible.

2.2 This standard specifies that SEMI E63 is utilized for the tool side of the interface.

2.3 This standard covers the following topics:

- General physical requirements for integration of the IMM,
- Nominal wafer-seating plane within the IMM,
- Maximum outer dimensions of the IMM, in case it is located at the front of a tool.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This standard does not specify the location of the IMM relative to the tool.

3.2 This standard does not specify facility or communication interfaces.

3.3 No materials requirements or micro-contamination limits are given.

3.4 Substrate input and retrieval will be the obligation of the tool.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E1.9 — Mechanical Specification for Cassettes Used to Transport and Store 300 mm Wafers

SEMI E15 — Specification for Tool Load Port

SEMI E15.1 — Specification for 300 mm Tool Load Port

SEMI E47.1 — Provisional Mechanical Specification for Boxes and Pods Used to Transport and Store 300 mm Wafers

SEMI E57 — Mechanical Specification for Kinematic Couplings Used to Align and Support 300 mm Carriers

SEMI E63 — Mechanical Specification for 300 mm Box Opener/Loader to Tool Standard (BOLTS-M) Interface

SEMI E64 — Specification for 300 mm Cart to SEMI E15.1 Docking Interface Port

SEMI E127 — Specification for Integrated Measurement Module Communications: Concepts, Behavior, and Services (IMMC)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *IMM* — Integrated Measurement Module

5.2 *Definitions*

5.2.1 *bilateral datum plane* — a vertical plane that bisects the substrates and that is perpendicular to both the horizontal and facial datum planes. (As defined in SEMI E57.)

5.2.2 *BOLTS plane* — a plane parallel to the facial datum plane near the front of the tool where the box/opener loader is attached. (As defined in SEMI E63.)

5.2.3 *facial datum plane* — a vertical plane that bisects the wafers and that is parallel to the front side of the carrier (where wafers are removed or inserted). On tool load ports, it is also parallel to the load face plane specified in SEMI E15 on the side of the tool where the carrier is loaded and unloaded. (As defined in SEMI E57.)

5.2.4 *horizontal datum plane* — a horizontal plane from which projects the kinematic-coupling pins on which the carrier sits. On tool load ports, it is at the load height specified in SEMI E15 and might not be physically realized as a surface. (As defined in SEMI E57.)

5.2.5 *integrated measurement module (IMM)* — a measurement module intended to be integrated into manufacturing equipment, and with the capability of receiving substrates from the equipment, measuring those substrates, and returning the substrates and the measurement results to the equipment and other concerned clients. (As defined in SEMI E127.)

5.2.6 *measurement module* — an equipment module whose intended function is to measure or inspect the product and to report the results. Measurement of the product is the factory's means of gaining feedback on the manufacturing process. (As defined in SEMI E127.)

5.2.7 *nominal wafer-seating plane* — horizontal plane that bisects the wafer pick-up volume. (As defined in SEMI E1.9.)

6 Requirements

6.1 The IMM is required to mate with an interface as defined by SEMI E63. This includes meeting the requirements for the hole opening, bolt hole pattern, and other relevant requirements. Note that certain requirements in SEMI E63, such as y76 (facial datum plane when carrier is undocked), do not have relevance for the IMM but will not be in conflict.

6.2 *Use of Datum Planes* — The location in space where a substrate is delivered to an IMM is the intersection of three orthogonal datum planes defined in other standards: the facial datum plane, the nominal wafer-seating plane and the bilateral datum plane. The BOLTS plane, as in SEMI E63, is defined to be parallel to, and at a distance of y70 from the facial datum plane.

6.2.1 *Bilateral Datum Plane* — All bilateral dimensions of the interface are symmetric about the bilateral datum plane as shown in Figure 1.

6.2.2 *Facial Datum Plane* — This is the vertical plane, parallel to the BOLTS plane, which bisects the substrate at the insertion and removal position of the substrate inside of the IMM. The distance from the BOLTS plane to the facial datum plane in the IMM is determined by y70 of SEMI E63.

6.2.3 *Nominal Wafer-Seating Plane* — The nominal wafer-seating plane is the horizontal plane within the IMM where a substrate is to be loaded to or unloaded from by the tool. It can be anywhere between the given minimum and maximum values that follow. This range is not defined by a single standard, rather it results from a combination of dimensions of SEMI E1.9, SEMI E15.1 and SEMI E47.1. (See Figure 1.)

6.2.3.1 The minimum value for a nominal wafer-seating plane is the sum of (H + z44 + z8), measured from the floor.

6.2.3.2 The maximum value for a nominal wafer-seating plane is calculated by (H + z44 + z8 + (25-1) * z12), measured from the floor.

6.2.3.3 For both calculations, H is from SEMI E15.1, z44 is from SEMI E47.1, and z8 and z12 are from SEMI E1.9.

6.3 *Internal Clearances* — There are requirements relating to clearances inside the IMM. These relate to robot arm requirements for substrate handoff, and can be referenced from SEMI E1.9 and SEMI E47.1 as the same restrictions apply.

6.3.1 This includes clearance in front of the wafer set-down location of radius *r*3, and heights bounded by z11 and z10 relative to the nominal wafer-seating plane. All clearance requirements above the highest and below the lowest slot from SEMI E1.9 and SEMI E47.1 must

be followed depending on the nominal wafer-seating plane selected.

6.4 *Maximum Outer Dimensions* — If the IMM is intended to be located at the front side of a tool (where load ports are usually located), the outer dimensions of the IMM shall not exceed the volume as it would be used, when a load port is attached to a BOLTS-M interface.

6.4.1 *Depth* — The depth of the IMM located at the front of the process tool shall not exceed the maximum depth of a load port. The entire depth of the IMM shall not exceed the sum of y70 + y76 + D (from SEMI E63 and SEMI E15.1 respectively), as measured from the BOLTS plane.

6.4.1.1 The IMM shall not extend toward the tool beyond the BOLTS plane, except for possible temporary use of the reserved space defined in SEMI E63.

6.4.2 *Width* — If locating the IMM adjacent to another load port, there are width requirements defined by the carrier centroid spacing dimension S from SEMI E15.1.

6.4.2.1 If locating the IMM adjacent to an occupied load port containing a FOUP with handles, then the design of the width should not compromise the C1 clearance dimension from SEMI E15.1.

NOTE 3: Most tools today are designed with the dimension S chosen for spacing of boxes with handles. If the IMM width exceeds twice the x50 dimension for a FOUP with handles (from SEMI E47.1) then the IMM may not comply with the C1 requirement for integration with most existing tools.

6.4.3 *Height* — A height H2 (from SEMI E15.1) is the upper maximum boundary for the IMM when located at the front of the tool.

6.4.4 *Exclusion Volume* — There is an exclusion volume, defined by dimensions L_d and L_h at the bottom rear of the IMM reserved for requirements from SEMI E64. The width of this exclusion volume is the full width of the tool.

6.4.5 The front of the IMM (towards the tool) between the floor and up to the height of a load port, as given by the sum of H (SEMI E15.1) plus z79 (SEMI E63), is identical with the BOLTS plane. Above this height, the front of the IMM is limited by the equipment boundary as defined in SEMI E15.1.

NOTE 4: The BOLTS plane and the equipment boundary are defined by a different set of dimensions and thus are at different positions. The BOLTS plane is located more towards the tool.

7 Related Documents

7.1 *SEMI Standards*

SEMI E6 — Guide for Semiconductor Equipment Installation Documentation

SEMI E51 — Guide for Typical Facilities Services and Termination Matrix

SEMI E62 — Specification for 300 mm Front-Opening Interface Mechanical Standard (FIMS)

SEMI E101 — Provisional Guide for EFEM Functional Structure Model

SEMI E106 — Provisional Overview Guide to SEMI Standards for Physical Interfaces and Carriers for 300 mm Wafers

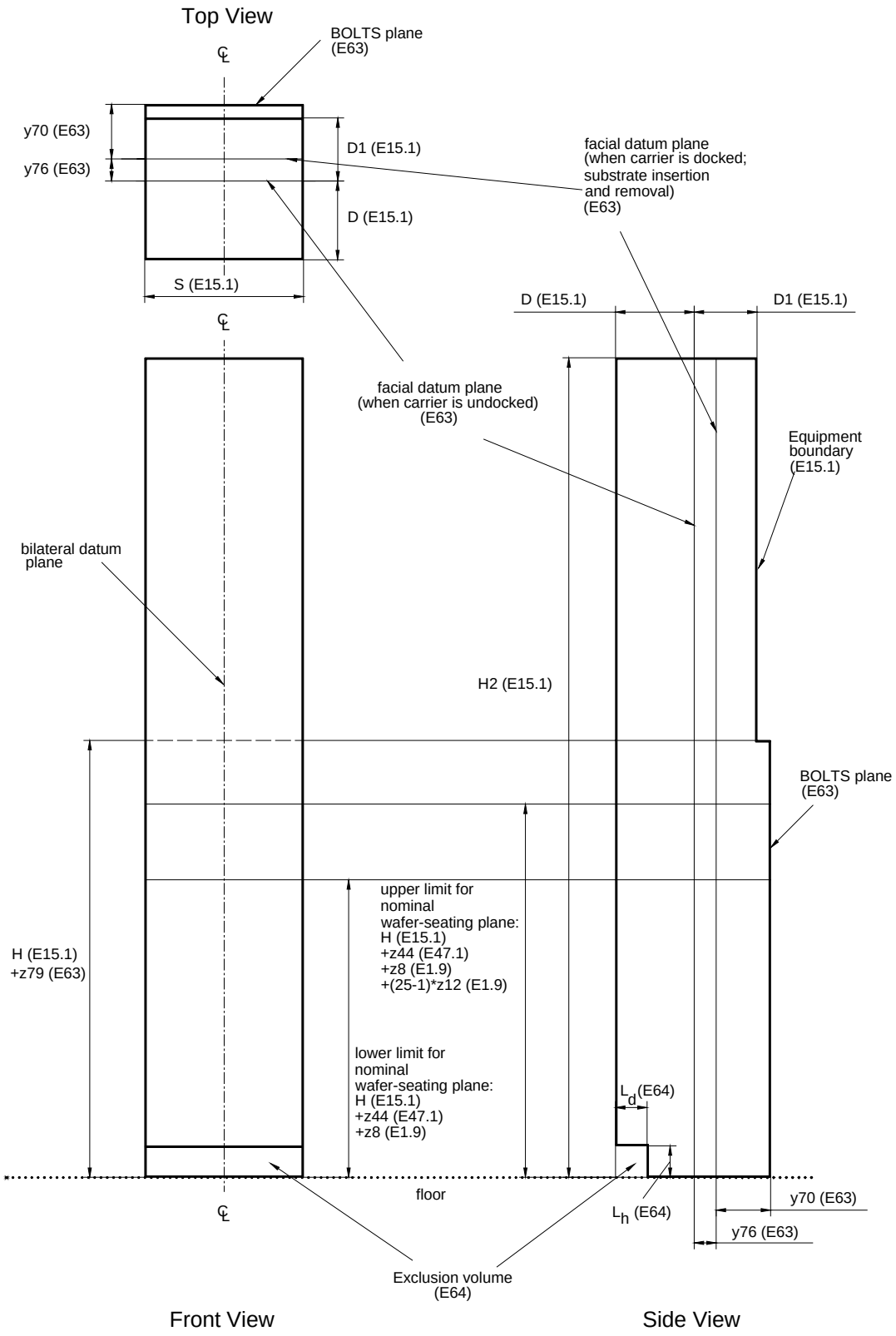


Figure 1
IMM Dimensional Requirements

RELATED INFORMATION 1
CALCULATION OF NOMINAL WAFER-SEATING PLANE

NOTICE: This related information is not an official part of SEMI E131 and was derived from work by the originating task force. This related information was approved for publication by full letter ballot procedures on December 4, 2003.

R1-1 The nominal wafer-seating plane is calculated using values found in a number of other standards, as follows.

R1-1.1 In SEMI E1.9 (the specification where this plane is defined), the nominal wafer-seating plane is referenced from the horizontal datum plane. SEMI E15.1 defines the horizontal datum plane H to identify a reference plane for positioning kinematic couplings. While there are no kinematic couplings required for the IMM, we use this same dimension as a starting point for defining the nominal wafer-seating plane for wafer insertion and removal. As in SEMI E15.1, the horizontal datum plane is given at a height H relative to the floor.

R1-1.2 Next, from SEMI E47.1 there is defined an external horizontal datum plane (equal to the horizontal datum plane from SEMI E15.1) and an internal horizontal datum plane, where the internal horizontal datum plane is located at a height of z44 above the external horizontal datum plane.

R1-1.3 Then, FOUP slot number 1 is defined at a height z8 in SEMI E1.9, but should be measured from the internal horizontal datum plane from SEMI E47.1.

R1-1.4 Finally, z12 in SEMI E1.9 is the slot-to-slot spacing within a cassette. So for a 25 substrate cassette, the distance from the FOUP slot number 1 to slot 25 is (25-1) * z12.

SEMI E135-0704
TEST METHOD FOR RF GENERATORS TO DETERMINE TRANSIENT RESPONSE FOR RF POWER DELIVERY SYSTEMS USED IN SEMICONDUCTOR PROCESSING EQUIPMENT

This test method was technically approved by the Global Metrics Committee and is the direct responsibility of the North American Metrics Committee. Current edition approved by the North American Regional Standards Committee on April 22, 2004. Initially available at www.semi.org on June 2004; to be published July 2004.

1 Purpose

1.1 The purpose of this document is to define a test method used to determine the transient response for an RF Generator used in RF power delivery systems for semiconductor processing equipment to support SEMI E113.

2 Scope

2.1 This document specifies the testing procedures and test equipment required for determining the transient response of an RF generator operating into a nominal 50-ohm load as a function of the change in set point level, including the time delay between the request for power (i.e., RF enable signal) and the start or stop of the RF output signal.

2.2 The primary focus for this document is semiconductor processing equipment including, but not limited to, the following tool types:

- Dry etch equipment,
- Film deposition equipment (CVD and PVD).

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This standard addresses RF generators used in RF systems that primarily operate in the frequency range of 0.2–100 MHz. It does not address higher frequency RF systems or microwave systems.

3.2 This standard is meant for analyzing RF generators that are designed to have a nominal characteristic impedance of 50 ohms. This standard can also be used with RF generators with a different characteristic impedance if the appropriate standard terminations are used.

3.3 International, national, and local codes, regulations and laws should be consulted to ensure that the equipment and procedures meet regulatory requirements in each location.

3.4 This standard does not address any safety or performance issues related to RF emissions or electrical codes (e.g., Underwriter's Laboratory, Inc. (UL), the National Electrical Code (NEC®), Federal Communications Commission (FCC)). It is the responsibility of the users of this standard to conform to the appropriate local codes and regulations as applied to this type of equipment, some of which are covered by referenced documents.

4 Referenced Standard

4.1 *SEMI Standard*

SEMI E113 — Specification for Semiconductor Processing Equipment RF Power Delivery Systems

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *CVD* — Chemical Vapor Deposition

5.1.2 *PVD* — Physical Vapor Deposition

5.1.3 *RF* — Radio Frequency

5.1.4 *VSWR* — Voltage Standing Wave Ratio

5.2 *Definitions of Terms*

5.2.1 *cable assembly* — the section of cable (transmission line), including the connectors, used to connect various parts of the RF power delivery system.

5.2.2 *device under test (DUT)* — the RF generator to be tested.

5.2.3 *load impedance* — the load impedance is the impedance to which a generator is attached.

5.2.4 *RF enable signal* — the signal that a generator receives to turn on the output power.

5.2.5 *RF set point signal* — the signal that a generator receives that corresponds to a desired output power.

6 Test Apparatus

6.1 *Digital Oscilloscope* — The Digital Oscilloscope is used to measure the RF enable signal, the RF set point signal, and the RF power output signal. It shall have a digitization rate of at least 500 mega-samples per second per channel. The Digital Oscilloscope shall have an up-to-date calibration per the manufacturer.

6.2 *RF Rectifier/Diode Detector* — A device that converts an RF signal into a DC signal is used to measure a signal related to the output power of the RF generator. The input RF signal is produced by the RF Signal Sampler. The output DC signal goes to the Digital Oscilloscope.

6.3 *RF Signal Sampler* — A device that will detect RF voltage and/or current and produce a reduced-level RF signal is used for detection purposes. The sampler can be a non-directional coupler or a directional coupler that detects forward power. The reduced-level signal produced by the sampler is typically −40 to −50 dB (decibels) below the RF signal being detected.

6.4 *RF Set Point Signal Generator* — A device that will produce a DC signal that is used to set the desired RF generator output. The device is connected to the controller input of the RF Generator and is measured with the Digital Oscilloscope.

6.5 *RF Enable Signal Generator* — A device that will produce a DC signal that is used to turn-on and turn-off the RF generator output power. The device is connected to the controller input of the RF Generator and is measured with the Digital Oscilloscope.

6.6 *RF Power Meter* — A device that will measure the output power of the RF generator that is used. It shall have an absolute power accuracy of ± 3 percent and a measurement repeatability of ± 1 percent.

6.7 *RF Adapters and Terminations* — Various adapters may be necessary to convert between different types of coaxial connectors (e.g., type N to type HN adapters). All adapters used shall have the same nominal characteristic impedance as the system, which is typically 50 ohms. For some measurements, additional coaxial cable assemblies are used. These cable assemblies shall also be of the same nominal characteristic impedance as the system.

6.8 *High-Power RF Dummy Load* — A high power RF load is used to absorb the power produced by the generator. It shall have the same nominal characteristic impedance as the RF generator, which is typically 50 ohms. The RF dummy load shall have a power handling capability that is compatible with the RF generator being tested.

7 Safety Precautions

7.1 Work should be conducted in accordance with local safety requirements and test device manufacturer recommended safety procedures.

7.2 The area immediately surrounding the Test Setup shall be keep free and clear of unnecessary equipment and materials.

8 Test Setup for Measuring the Transient Response of the RF Generator as a Function of the Change in Set Point

8.1 The test setup for measuring the transient response of the RF generator consists of an RF Enable Signal Generator, an RF Set Point Signal Generator, a Digital Oscilloscope, the RF Generator (DUT), an RF Signal Sampler, an RF Rectifier/Diode Detector, an RF Power Meter, and a High-Power Dummy Load. A schematic of the test setup is shown in Figure 1. All signal cables that are used to connect to the Digital Oscilloscope should be of comparable length so that there is no significant time delay between the signals measured by the Digital Oscilloscope.

8.2 Prior to making any measurements, the Digital Oscilloscope and other electronic test equipment shall be turned on and allowed to warm up per the manufacturer's guidelines before the testing is to take place. This time will allow for electronics to come to a stable operating condition for the measurements.

9 Test Procedure for Measuring the Transient Response of the RF Generator as a Function of the Change in Set Point

9.1 The test procedure described below compares the change in the set point signal (produced by the RF Set Point Signal Generator) to the signal produced by the DUT. The Set Point signal is an input to the DUT and is used by the DUT to produce the desired output power level, per the DUT manufacturer's instructions. The DUT output power level is measured with the RF Signal Sampler. The signal from the RF Signal Sampler is used by the RF Rectifier/Diode Detector to produce a DC signal that corresponds to the RF output power from the DUT. The Digital Oscilloscope measures both the Set Point signal and the RF Detector signal.

9.2 *Test Method for Measuring the Transient Response of the RF Generator as a Function of the Change in Set Point*

9.2.1 Connect the outputs of the RF Enable Signal Generator and the RF Set Point Signal Generator to the controller input of the DUT. Connect the RF power output of the DUT to the input of the RF Signal

Sampler, and connect the output of the RF Signal Sampler to the High-Power RF Dummy Load. If any coaxial cable assemblies or adapters are used to make any of the connections between the output of the DUT and the High-Power RF Dummy Load, they shall have power handling capability that is consistent with the maximum output power of the DUT. Connect the reduced-level signal output of the RF Signal Sampler to the input of the RF Rectifier/Diode detector. Connect the output of the RF Set Point Signal Generator and the output of the RF Rectifier/Diode Detector to the input channels of the Digital Oscilloscope. Inspect all connections of the Test Setup to ensure proper contact.

9.2.2 Set up the Digital Oscilloscope to trigger off of the signal level change of the RF Set Point Signal Generator.

9.2.3 Turn on the RF Enable Signal Generator to a level that will allow the DUT to produce output power.

9.2.4 Change the RF Set Point Signal Generator output level to produce the desired change in RF output power. Measure and record the RF Set Point Signal Generator signal and the RF Rectifier/Diode Detector signal with the Digital Oscilloscope. Also record the indicated RF power levels from before and after the Set Point change as measured by the RF Power Meter. The measurement by the Digital Oscilloscope shall continue until the RF output power has stabilized, which typically takes a few milli-seconds.

9.2.5 The data shall be recorded and then presented in both graphical and tabular forms. An example of data collected from a Digital Oscilloscope for an RF generator test is shown in Figure 2, where the Set Point was changed from 3% to 33% of full power, and in Figure 3, where the Set Point was changed from 33% to 3% of full power.

10 Test Setup for Measuring the Transient Response of the RF Generator as a Function of the Change in RF Enable Signal

10.1 The Test Setup for the measuring the transient response of the RF generator as a function of the RF Enable signal consists of a RF Enable Signal Generator, a RF Set Point Signal Generator, a Digital Oscilloscope, the RF Generator (DUT), a RF Signal Sampler, a RF Rectifier/Diode Detector, a RF Power Meter, and a High-Power Dummy Load. A schematic of the Test Setup is shown in Figure 4. All signal cables that are used to connect to the Digital Oscilloscope should be of comparable length so that there is no significant time delay between the signals measured by the Oscilloscope.

10.2 Prior to making any measurements, the Digital Oscilloscope and other electronic test equipment shall be turned on and allowed to warm up per the manufacturer's guidelines before the testing is to take place. This time will allow for electronics to come to a stable operating condition for the measurements.

11 Test Procedure for Measuring the Transient Response of the RF Generator as a Function of the Change in RF Enable Signal

11.1 The test procedure described below compares the change in the RF Enable signal (produced by the RF Enable Signal Generator) to the signal produced by the DUT. The Enable signal is an input to the DUT and is used by the DUT to turn on and turn off the output power. The DUT output power level is measured with the RF Signal Sampler. The signal from the RF Signal Sampler is used by the RF Rectifier/Diode Detector to produce a DC signal that corresponds to the RF output power from the DUT. The Digital Oscilloscope measures both the RF Enable signal and the RF Detector signal.

11.2 *Test Method for Measuring the Transient Response of the RF Generator as a Function of the Change in RF Enable Signal*

11.2.1 Connect the outputs of the RF Enable Signal Generator and the RF Set Point Signal Generator to the controller input of the DUT. Connect the RF power output of the DUT to the input of the RF Signal Sampler, and connect the output of the RF Signal Sampler to the High-Power RF Dummy Load. If any coaxial cable assemblies or adapters are used to make any of the connections between the output of the DUT and the High-Power RF Dummy Load, they shall have power handling capability that is consistent with the maximum output power of the DUT. Connect the reduced-level signal output of the RF Signal Sampler to the input of the RF Rectifier/Diode detector. Connect the output of the RF Enable Signal Generator and the output of the RF Rectifier/Diode Detector to the input channels of the Digital Oscilloscope. Inspect all connections of the Test Setup to ensure proper contact.

11.2.2 Set up the Digital Oscilloscope to trigger off of the signal level change of the RF Enable Signal Generator.

11.2.3 Turn on the RF Set Point Signal Generator to a level that will produce the desired output power.

11.2.4 Change the RF Enable Signal Generator output to a level that will turn on the DUT (per the DUT manufacturer's specification). Measure and record the time delay between the RF Enable Signal Generator signal and the RF Rectifier/Diode Detector signal with the Digital Oscilloscope. Also record the indicated RF output power level as measured by the RF Power Meter. The measurement by the Digital Oscilloscope

shall continue until the RF output power has stabilized, which typically takes a few milli-seconds. An example of data collected from a Digital Oscilloscope for a RF generator test is shown in Figure 5. Repeat this measurement a minimum of 31 times and record each condition.

11.2.5 Report the average delay time and standard deviation between the RF Enable signal turn on signal and the RF output power signal.

11.2.6 Change the RF Enable Signal Generator output to a level that will turn off the DUT (per the DUT manufacturer's specification). Measure and record the time delay between the RF Enable Signal Generator signal and the RF Rectifier/Diode Detector signal with the Digital Oscilloscope. Also record the indicated RF output power level as measured by the RF Power Meter. The measurement by the Digital Oscilloscope shall continue until the RF output power has stabilized. Repeat this measurement a minimum of 31 times and record each condition.

11.2.7 Report the average delay time and standard deviation between the RF Enable signal turn off signal and the RF output power signal.

12 Reporting Test Results

12.1 Report the type of Digital Oscilloscope and the details of the Digital Oscilloscope parameters used for the tests, including the digitization rate used for the test.

12.2 Report the type of RF Signal Sampler used and the type of RF Rectifier/Diode Detector used for the test.

12.3 Report the transient response of the DUT as a function of RF Set Point change. The data shall be presented in both graphical and tabular forms. Report the power level changes measured for the test.

12.4 Report the average and standard deviation of the time delay for the RF Enable turn on and turn off conditions. Report the average and standard deviation of power level changes measured for the test.

13 Related Documents

13.1 *IEEE*

IEEE-STD-572 — IEEE Standard for Qualification of Class 1E Connection Assemblies for Nuclear Power Generating Stations

IEEE-STD-383 — IEEE Standard for Type Test of Class 1E Electrical Cables, Field Splices, and Connections for Nuclear Power Generating Stations

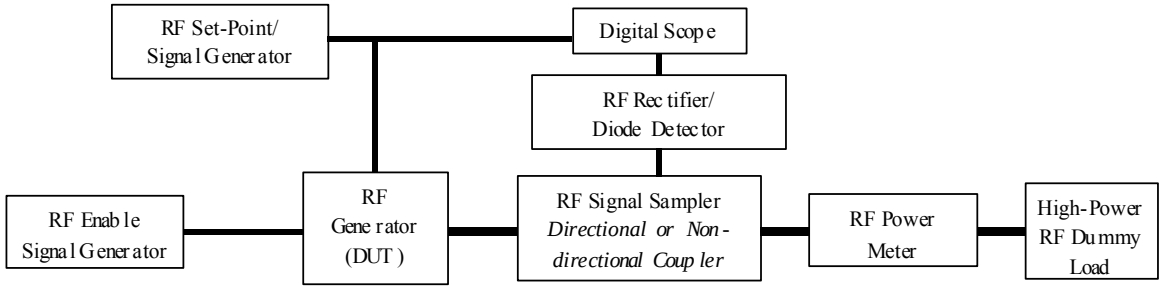
13.2 *MIL-Spec*

MIL-PRF-31031A — General Specification for Connectors, Electrical, Plugs and Receptacles, Coaxial, Radio Frequency, High Reliability, for Flexible and Semirigid Cables

MIL-PRF-39012D — General Specification for Connectors, Coaxial, Radio Frequency

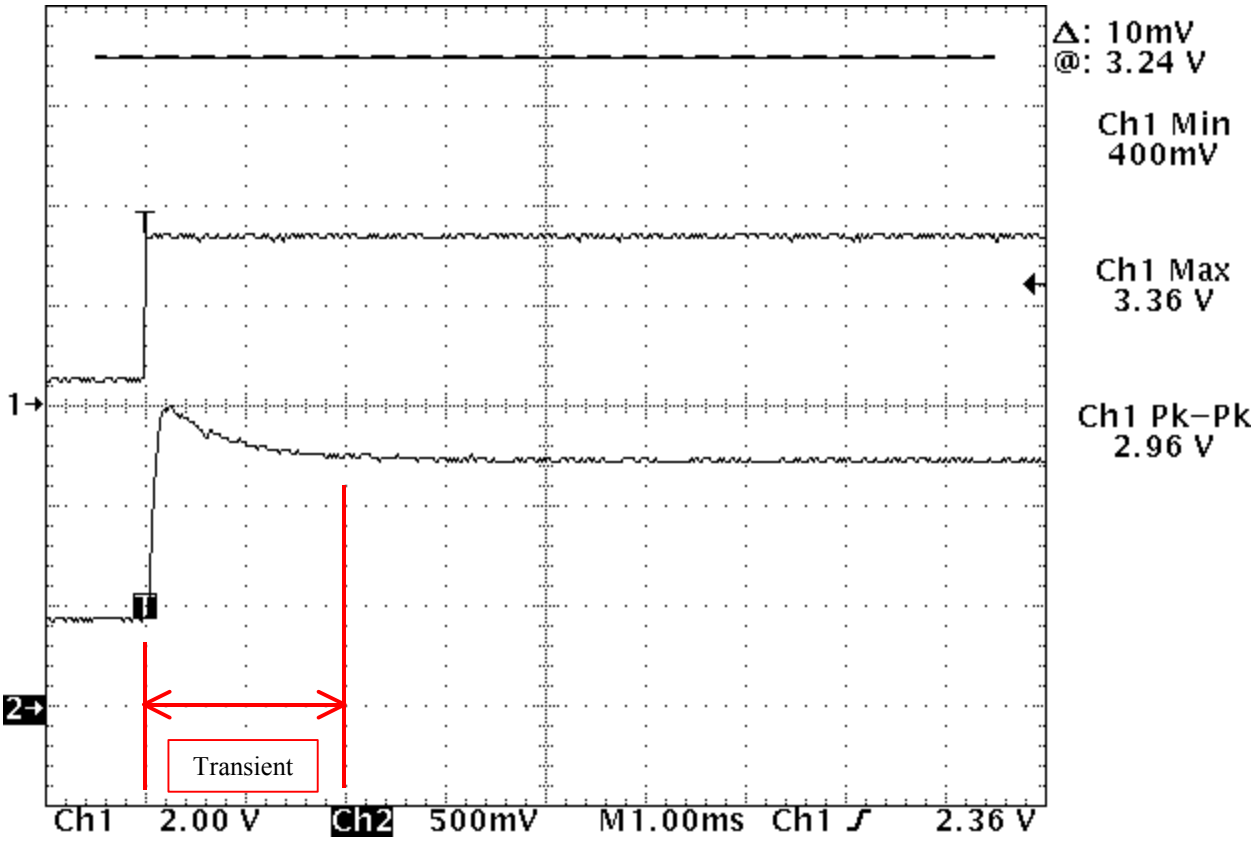
MIL-STD-348 — General Specification for Radio Frequency Connector Interfaces

MIL-STD-220B — Test Method Standard: Method of Insertion Loss Measurement



NOTE: If cable assemblies are used between the output of the RF Generator (DUT) and the High-Power Dummy Load, they shall have the same nominal impedance as the DUT and shall have a power handling capability that is consistent with the maximum output power of the RF Generator (DUT).

Figure 1
Schematic of the Test Setup for the Measuring the Transient Response of the RF Generator (DUT) as a Function of a Change in the Set Point



NOTE: These data are for conditions where the requested power went from 3% to 33% of the full power of the RF Generator being tested.

Figure 2
Example of Digital Oscilloscope Data that Shows the Transient Response of the RF Output Power (Lower Trace) Due to a Change in Set Point Signal (Upper Trace)