true size of LLSs other than PSL spheres (see Section 3.1).

2.8 This practice supports requirements listed in SEMI M52.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 LLSs are normally assigned only LSE sizes, not physical diameters, because the response of an SSIS to an LLS depends on the SSIS optical system characteristics as well as the size, shape, and composition of the LLS. The LSE size assigned to a particular LLS by an SSIS calibrated against PSL spheres may be different from that assigned to the same LLS by another similarly calibrated SSIS, because different SSISs have different optical system characteristics.

3.2 PSL spheres may have specified characteristics (mean diameter uncertainty, diameter distribution, spread between mean and modal diameter) that differ significantly from the characteristics of the resulting deposition due to the transfer function of the deposition system. For this reason the practice is limited to the use of PSL sphere depositions that are appropriately characterized. See Related Information 1.

3.3 If calibration points occur at, or near, dips in the response curve (see Section 5.3.17), the calibration curve will not be single valued; therefore dips must be avoided as calibration points if a monotonic calibration curve is to be obtained. However, if a complete calibration is desired, the locations and magnitudes of the dips must be determined. In this case there may not be a one-to-one correlation between SSIS response and LSE size; i.e., a particular instrument response may correspond to more than one LSE size.[1] (See Section 5.3.13.1.)

3.4 *Background Contamination*

3.4.1 The presence of localized light scatterers with LSE sizes near that of the nominal PSL diameter on the reference wafer may skew the results. This condition may result in a large error or poor equivalent sizing accuracy.

3.4.2 High levels of localized light scatterers on the reference wafer or wafers may overload the SSIS or obscure the peak of the deposited PSL sphere distribution. This condition may also result in a large error or poor equivalent sizing accuracy.

3.4.3 For these reasons, both the deposition process and calibration procedures must be carried out in a clean environment, and the reference wafers must be handled in such a way as to avoid contamination between deposition process and calibration.

3.5 If the surface roughness of the reference wafer or wafers is excessive, the peak of the PSL sphere distribution may be obscured or distorted.

3.6 If the SSIS being calibrated is not operating in a stable condition, the calibration may not be appropriate for subsequent use of the system. System stability can be evaluated by making repeated calibrations, in accordance with this practice, over suitable time periods.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI M1 — Specification for Polished Monocrystalline Silicon Wafers

SEMI M20 — Specification for Establishing a Wafer Coordinate System

SEMI M50 — Test Method for Determining Capture Rate and False Count Rate for Surface Scanning Inspection Systems by the Overlay Method

SEMI M52 — Guide for Specifying Surface Scanning Inspection Systems for Silicon Wafers for the 130-nm Technology Generation

SEMI MF1241 — Standard Terminology of Silicon Technology

4.2 *Federal Standard*[2]

Fed Std 209E — Airborne Particulate Cleanliness Classes in Cleanrooms and Clean Zones

1 See, for example, Locke, B. R., and Donovan, R. P., "Particle Sizing Uncertainties in Laser Scanning of Silicon Wafers," *Journal of The Electrochemical Society*, Vol 134, No. 7, 1987, pp. 1763–1771; or Liu, B. Y. H., Chae, S.-K., and Bae, G.-N., "Sizing Accuracy, Counting Efficiency, Lower Detection Limit and Repeatability of a Wafer Surface Scanner for Ideal and Real-World Particles," *ibid*., Vol 140, No. 5, 1993, pp. 1403–1409.

2 Standardization Documents Order Desk, Bldg. 4 Section D, 700 Robbins Ave., Philadelphia, PA 19111-5094, Attn: NPODS (This standard has been superseded by ISO 14644-1 and may no longer be available.)

4.3 *ISO Standards*[3]

ISO 14644-1 Cleanrooms and associated controlled environments — Part 1: Classification of airborne particulates

ISO Guide 30: 1992 Terms and definitions used in connection with reference materials

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 Definitions for general terms for silicon technology are found in SEMI MF1241.

5.2 Additional terminology is defined in SEMI M1.

5.3 *Definitions*

5.3.1 *capture rate* (*CR*) — the probability that a scanning surface inspection system (SSIS) detects a localized light scatterer (LLS) of latex sphere equivalent (LSE) signal value at some specified SSIS operational setting.

5.3.2 *certified reference material (CRM)* — a material accompanied by a certificate, one or more of whose property values are certified by a procedure that establishes its traceability to an accurate realization of the unit in which the property values are expressed, and for which each certified value is accompanied by an uncertainty at a stated level of confidence [ISO Guide 30].

5.3.2.1 *Discussion* — In the context of this practice, a CRM is a certified PSL sphere deposition on an unpatterned wafer with the same surface films and finish as the wafers to be examined by the calibrated SSIS. The deposition property values that must be certified are the peak sphere diameter and the diameter distribution on the wafer and are determined by both the PSL sphere source and the deposition process. The wafer may contain more than one CRM. See Related Information 1.

5.3.3 *coefficient of variation (CV)* — one standard deviation, σ, expressed as a percentage of the mean of a Gaussian distribution.

5.3.4 *deposition* — an approximately known number of PSL spheres of known size distribution placed in a known location on the surface of a reference wafer.

5.3.5 *deposition process* — the procedure used to place the PSL spheres on the reference wafer.

5.3.6 *dynamic range* — of a scanning surface inspection system, the signal range covered by an instrument with one set of measurement conditions.

5.3.6.1 *Discussion* — The useful dynamic range is limited on the small signal side by the background noise or the inherent resolution of the instrument and on the large signal side by saturation of the detector and/or the related electronics. The small signal limit is usually defined as the smallest PSL diameter than can be measured with a capture rate of at least 95%.

5.3.7 *false count* — a laser-light scattering event that arises from instrumental causes rather than from any feature on or near (in) the wafer surface; also called *false positive*; compare *nuisance count*.

5.3.7.1 *Discussion* — False counts would not be expected to occur at the same point on the wafer surface during multiple inspection scans, and hence they could be considered as random "noise" that could be identified by examining the results of repeated scans.

5.3.8 *histogram* — a representation of a partitioned (binned) data set as a bar graph in which the widths of the bars are proportional to the sizes of the bins of the data set variable, and the height of each bar is proportional to the frequency of occurrence of values of the variable within the bin.

5.3.8.1 *Discussion* — In presenting data for the size distribution of LLSs, the data set variable is usually the derived LLS size; in presenting haze data, the data set variable is usually the haze in ppm. The data set is usually partitioned into bins of equal size on either a linear or logarithmic scale, as appropriate. The bins at the low and high ends of the data set variable range are customarily plotted with the same width as the remainder of the histogram even though they may represent a larger or smaller range of the independent variable than the rest of the bins.

5.3.9 *laser-light scattering event* — a signal pulse that exceeds a preset amplitude threshold, generated by the interaction of a laser beam with an LLS at a wafer surface as sensed by a detector.

5.3.9.1 *Discussion* — The amplitude of the signal into a single detector, as measured for any combination of incident beam direction and collection optics, does not by itself convey topographic information, for example, whether the LLS is a pit or a particle. It does not allow the observer to deduce the size or origin of the scatterer without other detailed knowledge, such as its index of refraction and shape. In a scanning surface inspection system, laser-light scattering events and the background

3 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch; also available in the US from American National Standards Institute, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023 Website: www.ansi.org, and in other countries from ISO member organizations.

signal due to haze together comprise the signal due to light scattering from a wafer surface.

5.3.10 *latex sphere equivalent (LSE)* — the diameter of a monodisperse polystyrene latex sphere that, under identical test conditions, produces the same detected scattering intensity as the LLS under investigation.

5.3.10.1 *Discussion* — If the LLS is assumed to be due to a particle (or pit), the LSE size (diameter) of the particle (or pit) is given in units of length followed by LSE; for example, 0.12 μm, LSE. This unit varies in different ways for different materials from instrument to instrument because of differences in the optical systems and signal processing procedures of different instruments. Therefore a particular LLS generally does not have the same LSE size when measured on different model instruments or on different channels of the same instrument. If elements of the optical system, such as incidence angle, collection solid angle, or polarization, of an SSIS can be varied, the LSE size of a particular LLS will not necessarily be the same for each configuration of the optical system.

5.3.11 *localized light scatterer (LLS)* — an isolated feature, such as a particle or a pit, on or in a wafer surface, resulting in increased light scattering intensity relative to that of the surrounding wafer surface; historically called *light point defect* because under high intensity optical illumination features of sufficient size appear as an isolated point of light.

5.3.11.1 *Discussion* — Localized light scatterers are observed by automated inspection techniques as laser-light scattering events. Automated inspection techniques are quantitative in the sense that scatterers with different scattering intensities can be segregated. However, the amplitude of the scattered light intensity, or "laser-light scattering event", as measured by any combination of incident beam direction and collection optics, does not by itself convey topographical information about the LLS; particles and pits cannot be distinguished solely on the basis of single-channel amplitude data. Also, the observer cannot deduce the size, shape, or composition of the LLS from single-channel amplitude alone. The presence of LLSs does not necessarily decrease the utility of the wafer.

5.3.12 *missing count* — the case in which an LLS fails to produce a laser-light scattering event; also called *false negative*.

5.3.13 *multipoint calibration* — a procedure for calibrating the size response of an SSIS using a set of accurately sized polystyrene latex spheres, deposited on a wafer surface of the type to be inspected by the SSIS.

5.3.13.1 *Discussion* — The purpose of a calibration is to relate the amount of light captured by an SSIS to the physical size of the light scatterer. The amount of light scattered from a localized light scatterer (LLS) that is captured by the SSIS is a function of both the scattering characteristics of the LLS (including the directional dependence of the scattering) and the geometry of the collection optics of the SSIS. For a given wavelength of incident radiation, regular objects of certain sizes exhibit non-linearities, usually in the form of a dip, so that the curve of scattering amplitude as a function of physical size of the scatterer may not be monotonic. Thus, similar objects with modest variations in physical size can scatter the same amount of light. Different materials may exhibit non-linearities at different sizes. Because these effects tend to be less pronounced for irregular particles such as may be found on polished wafer surfaces, instrument calibration is usually carried out by avoiding the sizes of spheres that correspond to a dip. Sometimes, however, it is desired to fully characterize the response of the SSIS to a particular type of scatterer; in this case, the calibration can be carried out with a set of particles with sizes that cover the desired range with adequate density to ensure that any non-linearities in the scattering amplitude-size curve are detected.

5.3.14 *nominal sphere size distribution* — the stated diameter distribution of a suspension of PSL spheres of a certified diameter used in the calibration of SSISs.

5.3.14.1 *Discussion* — The nominal sphere size distribution is usually expressed as the standard deviation or the coefficient of variation of the distribution about the certified diameter. Depending on how the deposition is made, the size distribution of the deposited spheres may be equal to the distribution in the original suspension or it may be significantly narrowed by the deposition process.

5.3.15 *nuisance count* — a signal pulse that arises from discrete or area surface or near-surface features other than the localized light scatterers being investigated; compare *false count*.

5.3.15.1 *Discussion* — The presence of nuisance counts is dependent on the threshold and gain settings and may be a function of the optical configuration of the SSIS, the orientation of the wafer surface, or both.

5.3.16 *reference wafer* — for calibrating an SSIS in accordance with this practice, an unpatterned wafer with the same surface films and finish as the wafers to be examined by the calibrated SSIS and upon which one or more PSL sphere depositions have been certified to specified uncertainties for peak diameter and diameter distribution.

5.3.17 *response curve (RC)* — the modeled relation between measured scattered light intensity (or SSIS signal response) and PSL sphere peak diameters. The

RC depends on the light source used, is in general non-linear and may contain regions with dips that make the response/diameter relationship multi-valued. (See Section 3.3).

5.3.18 *scanning surface inspection system (SSIS)* — an instrument for rapid examination of the entire quality area of a wafer to detect the presence of localized light scatterers or haze or both; also called *particle counter* and *laser surface scanner.*

5.3.19 *threshold* — the level set on a scanning surface inspection system (SSIS) to discriminate between signal pulses of different size.

5.3.19.1 *Discussion* — Thresholds may be set to discriminate between true counts and surface or electrical noise (nuisance or false counts, respectively) or between different sizes of light scatterers. Because of spatial non-uniformity of the intensity of the scanning beam and the general use of overlapping scans in an SSIS, a localized light scatterer with equivalent size near the threshold may generate a signal greater than or less than the threshold depending on its location with respect to the path of the scanning beam. The former is identified as a true count and the latter is identified as a missing count.

5.3.20 *true count* — a laser-light scattering event that arises from the localized light scatterers being investigated.

5.3.21 *unimodal distribution* — a distribution represented by a histogram with constant bin size that has a single bell-shaped peak.

6 Summary of Practice

6.1 The range of LSE values to be used for calibration is defined for each dark channel that is to be calibrated.

6.2 The number of calibration points required is defined for each defined range.

6.3 Suitable reference wafers with certified PSL distributions are obtained.

6.4 The reference wafers are scanned by the SSIS being calibrated under machine conditions identical with those to be used in examining wafers with the calibrated SSIS.

6.5 The peak diameter of the PSL spheres deposited on each reference wafer is assigned to the peak value of the SSIS signal units.

6.6 An RC, the curve of SSIS channel response as a function of SSIS calibration PSL sphere diameter, is constructed through the data points obtained. A separate calibration curve is developed for each channel.

7 Apparatus

7.1 *Scanning Surface Inspection System* — designed to detect, size, and map localized light scatterers (LLSs) on unpatterned semiconductor wafers, that has the following capabilities:

7.1.1 Scans the entire fixed quality area of the surface of a wafer with a laser beam,

7.1.2 Detects localized light scatterers as laser-light scattering events,

7.1.3 Has a user definable sensitivity threshold,

7.1.4 Can generate a data set file of the distribution of the detected LLSs as a function of reported size (LSE),

7.1.5 Can generate a histogram from the data set file, or can output the data set file in a form that can be imported to a spreadsheet or other application program that can generate the histogram,

7.1.6 Is sufficiently repeatable for the intended application, and

7.1.7 Handles wafers in a Class 4 or better clean environment as defined in ISO 14644-1.

8 Reference Wafers

8.1 *Substrates* — Use bare semiconductor wafers with a native oxide (or other filmed) surface of the type intended to be tested with the SSIS to be calibrated as substrates for the certified depositions of the PSL spheres. This is particularly important because SSIS response is affected by the optical properties of the substrate. Semiconductor wafer surfaces, such as unpatterned polished, epitaxial, or film layers, have different optical properties. The wafers must meet the dimensional requirements of SEMI M1 for the appropriate nominal wafer diameter and must be laser marked in a manner agreed upon between supplier and user.

8.2 *Range of Calibration Diameters* — Choose the diameters of the PSL spheres so that the measurement range for the intended application is covered. Use spheres of size ranging from the largest measurable size down to a size with an estimated capture rate less than 50%. Do not exceed the dynamic range of the SSIS channel being calibrated. Use sufficient sphere diameters to achieve the required 5% PSL sphere sizing accuracy of the response curve between calibration points using a calibration curve that is produced by fitting the calibration points. In the absence of other criteria, choose spheres with diameter ratios of approximately 1.7.

8.2.1 To accomplish the accuracy check (see Section 10.4.2), choose an additional set of PSL spheres of size

approximately midway between adjacent pairs of the original set.

8.3 *Background Contamination*

8.3.1 Handle and store reference wafers with great care to avoid contamination and damage.

8.3.2 Establish that the bell-shaped peaks in the SSIS LLS histogram of each reference wafer to be used, which are generated from the PSL sphere depositions, are well defined and well above the background level over all of the response curve except near the threshold. Also verify that each unimodal bell-shaped curve extends to less than 50% of its peak value on both sides of the peak within a diameter range of ± 15% of the PSL sphere diameter at the peak of the distribution. If the deposition on any reference wafer fails either of these criteria, obtain a new reference wafer.

NOTE 3: In most cases, the LLS histogram peaks are wider than the actual deposition diameter distributions. See Related Information 1 for more details.

8.4 *Data to Accompany Reference Wafers* — A certificate with the following information must accompany each reference wafer.

8.4.1 For each CRM on the reference wafer provide:

8.4.1.1 The deposition peak diameter and the uncertainty in accordance with the requirements of Row 3.3 of Table 3 of SEMI M52.

8.4.1.2 The maximum possible value of the deposition diameter distribution full width at half max (FWHM) expressed as a percent of peak diameter. (See Related Information 1.)

8.4.1.3 The particle count of each CRM and the associated sample coefficient of variation.

8.4.1.4 The approximate location of each CRM on the reference wafer by the *x*- and *y*-coordinates (as specified in SEMI M20) of the center of the deposition area or by a map or drawing of the wafer.

8.4.2 Identification of the deposition system used for the deposition by model and serial number.

8.4.3 The date of production.

8.4.4 Wafer identification by laser mark on 200 mm and smaller wafers per SEMI M12 or 300 mm wafers per SEMI M1.15 including alpha numeric message.

8.4.5 Name and address of the reference wafer manufacturer.

8.4.6 Identification of the deposited PSL spheres by manufacturer, lot number and model.

9 Procedure

9.1 Set up the SSIS in accordance with the manufacturer's instructions for the wafer diameter, sizes of PSL spheres, and other machine conditions to be used during the calibration procedure. Ensure that machine conditions are identical with those to be used in examining wafers with the calibrated SSIS.

9.2 Ensure that the SSIS is operating properly for the selected machine conditions.

9.3 Load the first reference wafer into the SSIS.

9.4 Scan the wafer.

9.5 Generate a data set file of the distribution of localized light scatterers as a function of reported SSIS signal.

9.6 Repeat Sections 9.3 through 9.5 for each of the depositions on the remaining reference wafers and for all of the SSIS channels.

10 Interpretation of Data

10.1 Construct a histogram for the data set from each of the PSL sphere depositions used for the calibration.

10.2 Determine the standard deviation and peak value from curve fits to the histograms from each deposition.

10.3 Associate each peak value of reported SSIS signals determined in Section 10.2 to the certified value of PSL sphere diameter for that CRM deposited on that reference wafer.

10.4 Create and check the SSIS response curve.

10.4.1 To obtain the SSIS response curve make a fit to the set of peak values in such a manner that the response to PSL sphere deposition CRMs that size between calibration points meets the uncertainty requirements of SEMI M52.

10.4.2 Check the accuracy of the resulting SSIS response curve by either measuring PSL sphere deposition CRMs with locations mid-way between calibration points, or by comparison to a modeled result, or both.

10.4.3 If necessary repeat the curve fitting procedure until the required accuracy is met.

10.5 Use this fitted response curve to establish the LSE size of localized light scatterers with any particular machine response value.

11 Report

11.1 Report the following information:

11.1.1 Operator identification;

11.1.2 Date and location of measurement;

11.1.3 Manufacturer, model, serial number, and software version of the SSIS;

11.1.4 Reference wafer characteristics as outlined in the certificates accompanying the reference wafers (See Section 8.4);

11.1.5 Histogram for each data set and the assigned peak value of the distribution of reported diameters together with the certified peak diameter of the PSL sphere distributions used to generate the histogram; and

11.1.6 The curve fitted to the peak values and the associated certified PSL diameters.

APPENDIX 1
SINGLE-POINT CALIBRATION

NOTICE: The material in this appendix is an official part of SEMI M53 and was approved by full letter ballot procedures on November 22, 2002.

A1-1.1 Choose a single reference wafer with PSL sphere deposition CRM size near the LSE size of the smallest LLS to be tested for in meeting a wafer specification.

NOTE A1-1: Because of possible non-linearities in the SSIS, single-point calibration is not recommended except in the immediate vicinity of a single sphere size of interest, for example, the smallest size to be tested for in meeting a wafer specification.

A1-1.2 Set up the SSIS to be calibrated in accordance with Sections 9.1 and 9.2.

A1-1.3 Load the appropriate reference wafer into the SSIS.

A1-1.4 Scan the wafer.

A1-1.5 Generate a data set file of the distribution of localized light scatterers as a function of reported size (LSE).

A1-1.6 Construct a histogram for the distribution in the data set file.

A1-1.7 Determine the standard deviation and peak diameter value from curve fits of the histogram.

A1-1.8 Associate the peak value of reported size (LSE) found to the certified value of PSL sphere diameter deposited on the reference wafer.

RELATED INFORMATION 1
DEPOSITION ISSUES

NOTICE: This related information is not an official part of SEMI M53 and was derived from the work of the Automated Wafer Surface Inspection Task Force. This related information was approved for publication by full letter ballot on November 22, 2002.

R1-1.1 Both this practice and SEMI M52 introduce the notion that SSIS calibration should depend on the characteristics of PSL sphere depositions as they appear on the reference wafers, rather than the previous technique of using the bulk characteristics of the PSL spheres measured prior to being deposited. This change in philosophy has come about for two reasons. First, in many situations, there is actually some advantage to creating depositions with different characteristics from those of the bulk PSL spheres. For example, the deposition process may be used to narrow the diameter distribution thus creating a standard that more closely approximates a source of particles of a single known size. Secondly, most deposition systems produce at least minor changes in diameter distributions that are difficult to eliminate in any case. As a result, this philosophical change is being introduced to increase the accuracy with which SSIS calibration can be accomplished.

R1-1.2 Deposition systems generally consist of an atomizer (which takes the particles from a liquid suspension to an air droplet mist), followed by a dryer (so that droplets of the source liquid do not reach the wafer), and often include a bipolar charger and differential mobility analyzer (or DMA) to size and/or filter the particles. The changes in characteristics from source to deposition are due to at least three distinct causes. First, virtually all atomizers bias the diameter distribution slightly in favor of smaller particles. This is because the larger particles do not "fit" in the smaller droplets and as a result have a smaller probability of ending up in the airborne stream of particles headed towards the wafer. For narrow source distributions this is not much of an issue, but for wider source distributions it is. Secondly, the source liquid often contains non-volatile solids that may dry onto the particles, thus slightly changing their diameter. Although this is not as important for larger particles greater than 200 nm, it is highly recommended that a PSL suspension with low non-volatiles be used to reduce this source of error. If the DMA is operated in a manner that meets the requirement of this practice for distributions with full width at half maximum (FWHM) of no more than 5% of the peak diameter, then many source distributions are narrowed by the DMA. This is true because many PSL sphere sources with diameters less than 200 nm have FWHM values wider than 5% of peak value. The 5% FWHM value does not impose severe difficulties on the DMA design.

R1-1.3 In addition to narrowing the deposition diameter distributions, these standards address related accuracy issues. These are easily understood by considering the filtering process of the DMA on the source distribution as shown in Figure R1-1. The left hand side of the figure represents a rather broad PSL source diameter distribution. Notice that it is not symmetrical, which makes the mean (or average) diameter different from the modal (or peak) diameter. Typically PSL manufacturers have given the mean diameter with their product and industry users have assigned this value as the diameter for that deposition. Unfortunately depositions are generally made at the peak diameter. This is because the peak is easily found by scanning the DMA through the source distribution while counting the number of particles passing the DMA. The center section of the figure shows the ideal triangular transfer function of the DMA fixed at some center diameter. By adjusting airflows through the DMA, the FWHM can be changed. By adjusting an applied voltage, the center pass diameter of the transfer function can be changed. In effect, the deposition characteristics are formed through the multiplication of the transfer function with the source distribution as indicated on the right hand side of the figure.

R1-1.4 Notice that the shape of the deposition distribution is triangular with bowed in sides, because the source distribution is not flat. In effect, this is a safety factor for the 5% FWHM specification. Because the source distribution is not necessarily symmetrical, the deposition distribution may not be either; however, the mean and peak deposition diameters will be very close because the distribution is relatively narrow.

R1-1.5 The accuracy of the peak diameter, which is specified to have a relative expanded uncertainty at about 95% confidence level as small as possible but not greater than 3% in SEMI M52, is determined by either the accuracy with which the peak source diameter is known (or can be found), or by the accuracy of the DMA sweep voltage/diameter relationship. Unfortunately many PSL source bottles currently in use do not give the peak diameter, so this presents a difficulty for the first approach. The second approach, relying on DMA voltage accuracy, can be checked by using PSL sources that are known to be very narrow (to minimize differences between source and deposition peak diameter) with very accurate peak values.

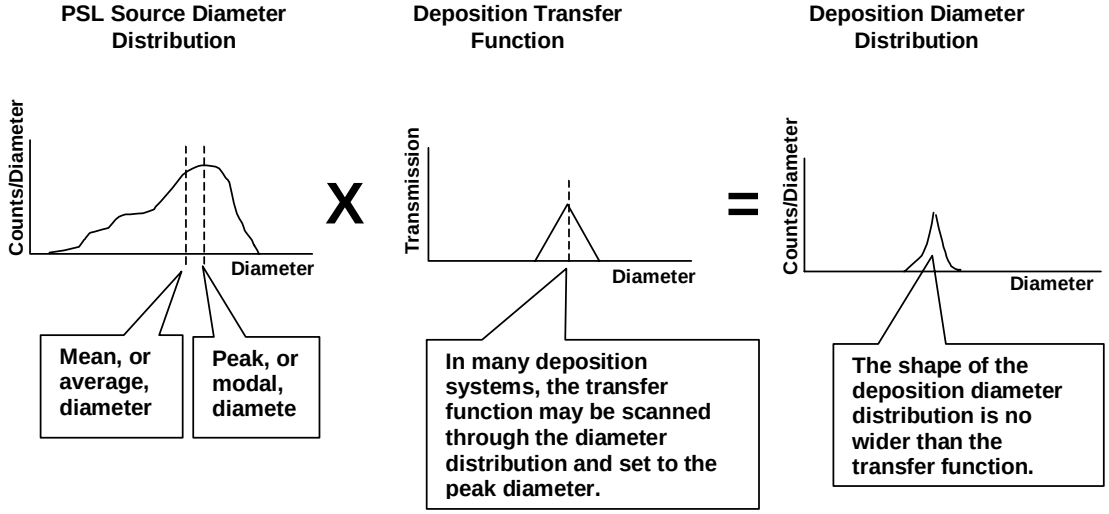

Figure R1-1
The Diameter Distribution of the Deposition is the Product of the Deposition System Transfer Function and the Source (or "Bottle") Distribution.

SEMI M54-0304
GUIDE FOR SEMI-INSULATING (SI) GaAs MATERIAL PARAMETERS

This guide was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the European Compound Semiconductor Materials Committee. Current edition approved by the European Regional Standards Committee on January 9, 2004. Initially available at www.semi.org February 2004; to be published March 2004. Originally published March 2003.

1 Purpose

1.1 Substrates with high electrical resistivity and electron drift mobility are needed to fabricate high performance digital and analog microelectronic devices and circuits. Semi-insulating n-type Gallium Arsenide, henceforth termed SI GaAs, has been established worldwide as a preferred substrate material for such applications.

1.2 The active layers needed for devices are generated either by ion implantation or by epitaxy. The quality of these layers, and hence the performance, yield and reliability of devices, strongly depends on the bulk and surface quality of the substrate.

1.3 This document provides a basis for specifying the material parameters of SI GaAs to support ordering agreements between suppliers and purchasers.

2 Scope

2.1 This document defines and describes the electrical, optical, structural, and surface properties of SI GaAs that are considered technically relevant according to the present status of scientific knowledge and material technology.

2.2 A specification of the material quality of SI GaAs substrates includes a number of the parameters described below. Depending on the intended application, a particular subset of properties and respective parameters will be considered relevant by the purchaser.

2.3 In order to enhance the clarity and applicability of the document, the ordering information in Section 6 subdivides the material parameters in respect of their relative importance, according to general industry perception.

2.4 Some material properties and parameters, while intensively discussed in the technical literature, are insufficiently established to allow an unambiguous specification. The available information is nevertheless included to support supplier-purchaser discussions and agreements on these issues.

2.5 Each parameter specification requires an agreement about verification. Appropriate information is summarized in Section 5. Available standard test methods elaborated by SEMI, ASTM, and DIN are referenced in Section 3.

2.6 A number of the required standard test methods do not exist at present. This document is expected to serve as a guideline and incentive for qualified ASTM, DIN, JEITA, and SEMI committees to develop the missing standard procedures. Conversely, if at present more than one standard test method for verification of a specific parameter exists (see Table 1), a global consensus procedure towards selecting or generating a unique standard is advocated.

2.7 The geometrical properties of wafers, in particular orientation, diameter, thickness, flatness and edge rounding, are covered by the series of SEMI M9 specifications and shall not be addressed here.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M9 — Specifications for Polished Monocrystalline Gallium Arsenide Slices

SEMI M10 — Standard Nomenclature for Identification of Structures and Features Seen on Gallium Arsenide

SEMI M15 — Polished Wafer Defect Limits Table for Polished Gallium Arsenide Wafers

SEMI M30 — Standard Test Method for Substitutional Atomic Carbon Concentration in GaAs by Fourier Transform Infrared Absorption

SEMI M36 — Test Method for Measuring Etch Pit Density (EPD) in Low Dislocation Density Gallium Arsenide Wafers

SEMI M39 — Test Method for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Semi-insulating GaAs Single Crystals

3.2 *ASTM Standards*[1]

ASTM F76 — Standard Test Methods for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Single-Crystal Semiconductors

ASTM F1404 — Test Method for Crystallographic Perfection of Gallium Arsenide by Molten Potassium Hydroxide (KOH) Etch Technique

3.3 *DIN Standards*[2]

DIN 50448 — Testing of materials for semiconductor technology - Contactless determination of the electrical resistivity of semi-insulation semiconductor slices using a capacitive probe

DIN 50449-1 — Testing of materials for semiconductor technology - Determination of impurity content in semiconductors by infrared absorption - Part 1: Carbon in gallium arsenide

DIN 50449-2 — Testing of materials for semiconductor technology - Determination of impurity content in semiconductors by infrared absorption - Part 2: Boron in gallium arsenide

DIN 50454-1 — Testing of materials for semiconductor technology - Determination of dislocations in monocrystals of III-V-compound semiconductors - Part 1: Gallium arsenide

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 SI GaAs

4.1 SI GaAs as described in this specification has n-type conductivity and an electrical resistivity ρ in the range $1 \times 10^6 – 5 \times 10^8$ Ωcm. It is characterized by fabrication procedures and material properties.

4.2 Synthesis of the compound GaAs from the elements gallium (Ga) and arsenic (As) may be done

- in the crystal growth chamber immediately prior to growth (in-situ synthesis)
- in separate equipment, independent of crystal growth (ex-situ synthesis)

4.3 The growth of SI GaAs single crystals involves one of the following procedures:

- Liquid Encapsulated Czochralski (LEC)
- LEC with controlled As vapor pressure (VCZ)
- Vertical Gradient Freeze (VGF)
- Vertical Bridgman (VB)

4.4 SI GaAs single crystal ingots are thermally treated after crystal growth. The annealing procedures are defined by heating rates, hold temperatures, hold times and cooling rates. Single step ingot annealing (one hold time at one temperature) or multi step ingot annealing (several hold times at different temperatures) may be applied. Wafers may be treated similarly by single step wafer annealing and multi step wafer annealing.

4.5 SI GaAs contains the intrinsic double donor point defect EL2, which involves an As atom on a Ga site (As_{Ga}). At room temperature the first ionization level $EL2^0/EL2^+$ is approximately at $\Delta E = 0.69$ eV below the conduction band. The concentration $[EL2^0]$ of the neutral defect is in the range of 5×10^{15} to 3×10^{16} cm^{-3}.

4.6 SI GaAs contains unintentionally incorporated impurities acting as donors. It may also contain intrinsic donor defects other than EL2. The total concentration [D] of donors other than EL2 should be low for optimal control of ion implantation activation and high electron mobility μ (see Section 4.12).

4.7 SI GaAs contains impurities acting as acceptors. It may also contain intrinsic acceptor defects. Usually the total concentration [A] of acceptors is adjusted by controlled incorporation of carbon (C) in the concentration range [C] 4×10^{14} cm^{-3} – 2×10^{16} cm^{-3}.

4.8 SI GaAs contains extrinsic and intrinsic point defects that do not participate in the compensation process (see Sections 4.10 and 4.11). These defects may be isoelectronic centers (e.g. boron (B) incorporated on the Ga site, B_{Ga}) or extremely deep donors and acceptors below and above the Fermi level, respectively. They may influence the material quality, for instance by degrading the activation efficiency of implanted dopants or by acting as transient carrier traps and nonradiative recombination centers (NRRC).

4.9 SI GaAs generally is nonstoichometric, containing excess As with a concentration of the order of 10^{18} cm^{-3}. The excess As is partly incorporated as lattice antisite defects (As_{Ga}), see Section 4.5. Other forms of point defect incorporation (e.g. interstitial As) are likely, but have not been positively identified. Excess As is attracted by dislocations (see Section 4.13) and is concentrated along these, forming decoration precipitates. Precipitates may also be generated away from dislocations, e.g. in the inner part of dislocation cells (see Section 4.14). They are referred to as matrix precipitates and are generally smaller than dislocation precipitates. The concentration and size of precipitates

1 Available from American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

2 Available from Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, website: www.din.de

strongly depend on the post growth annealing procedures (see Section 4.4).

4.10 To obtain SI GaAs, complete ionization of shallow donors and acceptors and partial single ionization of EL2 must be achieved, requiring that

$$[EL2] > [A] - [D] > 0 \quad \textbf{(1)}$$

The Fermi level is then pinned approximately at ΔE below the conduction band.

4.11 The resistivity of SI GaAs is given by

$$\rho = (e\,[n]\,\mu_n + e\,[p]\,\mu_p)^{-1} \quad \textbf{(2a)}$$

where e is the electron charge, [n] and [p] the concentration of electrons and holes and μ_n, μ_p the respective mobilities. For material with $\rho < 5 \times 10^8$ Ωcm and meeting condition (1), the second term may be neglected, hence

$$\rho = (e\,[n]\,\mu_n)^{-1} \quad \textbf{(2b)}$$

The electron concentration is given by

$$[n] \propto [EL2^0] / [EL2^+] \exp(-\Delta E / kT) \quad \textbf{(3)}$$

where T is temperature, k is Boltzmann' s constant and the concentration $[EL2^+]$ of the singly ionized defect is given by

$$[EL2^+] = [A] - [D] \quad \textbf{(4)}$$

Equation (3) may be used to normalize resistivity data ρ_M taken at a measurement temperature T_M. The normalized resistivity ρ_S at a standard reference temperature T_S is calculated according to

$$\rho_S = \rho_M \exp(\alpha \Delta T) \quad \textbf{(5)}$$

$$\text{where } \Delta T = T_M - T_S \quad \textbf{(6)}$$

and α depends on ΔE at T = 0 K (0.75 eV) and on T_S. For T_S = 296 K (23° C), one has $\alpha = 0.0994$.

4.12 Due to ionized impurity scattering μ decreases with the concentration [I] of ionized centers, given by

$$[I] = 2\,[A] = 2\,([EL2^+] + [D]). \quad \textbf{(7)}$$

Relations (3) and (7) imply that μ decreases with increasing resistivity. Relation (7) further implies that, for a given resistivity, low [D] is desirable to maximize μ .

4.13 SI GaAs ingots usually contain dislocations generated by thermal stress during crystal growth and postgrowth annealing. The dislocation density (DD), although a volume property, is evaluated by measuring the area density of dislocations threading a substrate surface. Structural etching with molten KOH generates characteristically shaped etch pits at the threading points. Hence the DD is characterized by quoting the etch pit density (EPD).

4.14 Depending on the growth method and the ingot diameter, the EPD may vary from essentially zero up to 2×10^5 cm^{-2}. The lateral variation of the EPD generally forms a pattern of globular dislocation-free "cells" surrounded by high DD "walls". The cell dimensions are on the order of 100 μm∅ for LEC grown material and about an order of magnitude larger for VGF grown material.

4.15 State-of-the-art SI GaAs substrates do not contain polycrystalline structure or twins.

4.16 The intensity of band-to-band and shallow donor/acceptor-related radiative carrier recombination luminescence depends on the minority carrier lifetime, which in turn is related to the distribution of NRRCs. These centers are generally believed to be intrinsic defects and appear to have a minor influence on the electrical properties.

4.17 The quality of the front surface of the wafer is mainly determined by global and local flatness (not addressed here in detail), surface contamination, light point defect (LPD)[3] density and micro-roughness (haze). Other surface irregularities to be considered in a supplier-purchaser agreement include stain, scratches, pits, orange peel and dimples as defined in SEMI M10.

4.18 The thickness and structure of the oxide on the surface of SI GaAs wafers to be used for epitaxy may be prepared to allow layer deposition without chemical pre-cleaning by the user. Generally this material property is guaranteed for a certain time interval only.

5 Parameter Verification

5.1 The material specification of SI GaAs according to Section 6 requires agreements on specification verification. Existing standard test methods are suggested and referenced in Section 3.

5.2 If a standard test method is not available, alternative verification methods are recommended and described in order to identify practicable characterization procedures that are consonant with industry practice and cost considerations.

5.3 Some characterization methods, while intensively used for exploratory material investigations, yield qualitative information only and are, therefore, inadequate for a specification verification. They are nevertheless included, with appropriate comment, to ensure comprehensiveness of this guideline and to facilitate respective supplier-purchaser agreements.

3 For silicon wafers, and sometimes for GaAs, the acronym LLS (localized light scatterer) is used.

5.4 The concentration of C incorporated on the As lattice site, [C_{AS}], is measured using the local vibrational mode (LVM) absorption with Fourier Transform Infrared Spectroscopy (FTIR). Presently two standard test methods (SEMI M30 and DIN 50449-1) are available. SEMI M30 is valid for measurement at room temperature and [C] > 10^{15} cm^{-3}. It requires individual instrument calibration with a set of secondary reference samples. DIN 50449-1 defines standardized FTIR measurement parameters and calibration factors for measurement at room temperature and at 77K, the latter having a detection limit [C] ≥ 10^{13} cm^{3}. For practically relevant concentrations (see Section 4.7) there is no evidence for carbon incorporation other than on the As lattice site. Hence the calibration factors quoted in SEMI M30 and DIN 50449-1 imply that [C] = [C_{As}]. The results obtained when using the two standard test methods presently are conflicting, hence a harmonizing activity is considered necessary.

5.5 The electrical resistivity ρ can be evaluated with contacting and noncontacting techniques. The contacting van der Pauw measurement is performed according to ASTM F76 or SEMI M39, the latter specifically addressing the measurement of SI GaAs. The noncontacting measurement using a capacitive probe is performed according to DIN 50448. This technique enables measurement of lateral variations of ρ. Resistivity will be quoted for an agreed standard temperature; 296K (23° C) is recommended. Measurements done at a different temperature must be normalized to the standard temperature as described in Section 4.11. The difference between the standard and measurement temperatures must not exceed 5° C.

5.6 The electron mobility μ is measured using the Hall effect and a van der Pauw structure. The evaluation is performed according to ASTM F76 or SEMI M39.

5.7 The etch pit density (EPD) of LEC grown SI GaAs is evaluated according to ASTM F1404 or DIN 50454-1. The documents describe the etching procedure and define test location plans linked to the crystallographic axes.

5.8 The EPD of VGF, VCZ and VB grown SI GaAs is 10^{4} cm^{-2} or below. The evaluation is performed according to DIN 50454-1 or SEMI M36. The test locations are defined by a fixed grid (SEMI M36) or by an adaptable grid generated by a standardized procedure (DIN 50454-1). Guidelines are given to assess the lateral variation of EPD.

5.9 The light point defect (LPD) density is a measure for the density of surface irregularities that are above a certain size limit (usually 300 nm in diameter). These irregularities may be foreign material deposited on the wafer surface (particles) or so-called crystal originating pits (COPs) caused by volume material inhomogeneities generated during the growth and/or annealing procedures and can be revealed by application of a light scattering technique. Depending on the mechano-chemical polishing processes and the light scattering technique employed, COPs may or may not be observed. At present no standard test method for LPD evaluation is available. Therefore, a supplier-purchaser agreement on e.g. the used measurement system, size restriction procedure, edge exclusion, inclusion or exclusion of COPs is necessary. To exclude an influence of different measuring systems the size of LPD's should be given in units of diameter, not of a scattering cross section.

5.10 The concentration of the neutral double donor [$EL2^{0}$] is measured using the optical absorption at about 1 μ m. An absolute determination is impossible because neither a generally accepted calibration standard nor a standardized test procedure is presently available[4]. Hence a supplier-purchaser agreement is necessary to ensure reproducibility. The relative lateral variation of [$EL2^{0}$] can be quantitatively assessed with high precision. The evaluation of [$EL2^{+}$] using optical absorption is presently considered unreliable.

5.11 The total concentration of impurities acting as donors is measured by Spark Source or Glow Discharge Mass Spectroscopy (SSMS, GDMS). The dominant contributions are Si, S, O, and Te. The analytical procedure is time-consuming and costly, hence it is generally confined to e.g. biannual control measurements of the supplier to ensure that raw material supply, synthesis and crystal growth procedures are stable. By virtue of the compensation process (see Section 4.11) the donor concentration [D], including intrinsic defects, is implicitly controlled by specifying [C], [EL2] and ρ.

5.12 The total concentration of impurities acting as acceptors is measured by SSMS or GDMS. The analytical procedure is time-consuming and costly, hence is generally confined to regular control measurements of the supplier to ensure that raw material supply and the synthesis and crystal growth procedures are stable. The dominant contribution usually is C, intentionally doped to control ρ. Hence it is generally sufficient to verify that the total concentration of acceptor impurities other than C is small compared to [C].

5.13 The concentration of B is measured using the local vibrational mode (LVM) absorption according to DIN 50449-2. Established, but non-standardized

4 A DIN standard test method to measure [EL2] is in preparation and is scheduled for publication in 2002.

methods include GDMS, SSMS, Secondary Ion Mass Spectroscopy (SIMS) and atomic absorption spectroscopy (AAS).

5.14 Surface contaminants are identified and quantified with Time-of-Flight-SIMS (TOF-SIMS) and Total Reflection X-Ray Fluorescence (TXRF). The latter technique is difficult to apply for impurities with atomic weight below those of the matrix elements Ga and As.

5.15 Deposition of high quality epitaxial layers without chemical pre-cleaning depends on the surface oxide structure of the substrate, as prepared by the supplier, as well as the thermal oxide desorption and the epitaxial deposition procedures of the purchaser. Hence an individual supplier-purchaser specific evaluation is necessary. Test epitaxy followed by layer quality assessment is recommended.

5.16 The lateral substrate homogeneity is assessed by automated analytic instrumentation elaborated to generate topographic images of important material parameters, including electrical resistivity, EL2 concentration, EPD and minority carrier lifetime. Macroscopic (e.g. radial) variations as well as mesoscopic fluctuations (generally correlated to the cellular dislocation structure) may be assessed. Such topographic analysis is provided, respectively, by contactless capacitive resistivity mapping (see DIN 50448), EL2 absorption topography (see footnote 3), specular light reflection topography and photoluminescence topography. The first three topography techniques provide quantitative data. Photoluminescence topography gives qualitative homogeneity information only, because the interrelations between the luminescence intensity and the various radiative and nonradiative recombination processes are only partially understood. The details of the topographic measurements, i.e. lateral resolution and edge exclusion, must be defined by individual supplier-purchaser agreement.

5.17 As precipitates, other inclusions and voids are visualized with light scattering tomography (LST). At present it is not possible to differentiate between these scattering centers and to obtain quantitative information concerning their concentration and size. Hence LST images provide a qualitative information only.

5.18 Micro-roughness, also referred to as haze, is indicated by a diffuse reflection of collimated, laterally extended high intensity illumination from the wafer surface. Localized haze and haze observed on particular wafers of a batch indicate potentially disadvantageous variations of surface quality. The agreement should specify the conditions of observation (e.g. illumination intensity).

5.19 Surface irregularities (stain, scratches, pits, orange peel, dimples) are identified by high intensity illumination or by standard and phase sensitive (Nomarski) microscopy. Individual agreement is recommended concerning the permitted surface density of these defects.

6 Ordering Information

6.1 The material properties of SI GaAs substrates, as described in Section 4, are addressed in the ordering agreement using the tables given below. The subdivisions into “important”, “optional” and “other” specifications are suggested only, i.e. supplier and purchaser may agree on an individual choice, taking into account the respective application as well as cost considerations.

6.2 In addition to specifying individual material properties as listed below, the purchase order may specify the fabrication procedures according to Sections 4.2 and 4.3.

6.3 Substrates are usually delivered in batches. The batch homogeneity is defined in the purchasing agreement by variation ranges of specified parameters. The ordering agreement shall also state whether batches must originate from one ingot or may be assembled from several specified or unspecified ingots. In either case the supplier guarantees compliance with the specified batch homogeneity by control of fabrication technology and appropriate test sample evaluations.

6.4 Table 1 lists the parameters that are considered important to specify the material quality of SI GaAs substrates. The level of importance may be adjusted individually by taking into account the intended use for implantation or epitaxy. The quoted absolute values suggest a customary material specification, to be adopted unless individual considerations warrant other choices.

6.5 Table 2 lists optional parameters that are important for specific applications only, hence may or may not be considered relevant for a particular supplier/purchaser agreement. For most of these parameters, standard test methods at present do not exist.

6.6 Table 3 lists other parameters which in general need not be specified, but are addressed for clarification and to provide a basis for agreement in the event that a purchaser desires to include such parameters into a purchasing specification.

7 Related Documents

7.1 *SEMI Standards*

SEMI M1 — Specification for Polished Monocrystalline Silicon Wafers

SEMI MF523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF1241 — Standard Terminology of Silicon Technology

7.2 *Other Docs*[5]

DIN 50443-2 — Testing of materials for semiconductor technology; recognition of defects and inhomogeneities in semiconductor single crystals by X-ray topography; III-V-semiconductor compounds

Table 1 Important SI GaAs Material Parameter Specifications and Suggested Standard Values

Parameter	*Section*	*Wafer Diameter*	*Suggested Value*	*Unit*	*Verification Technique*	*Standard Test Method*	*Section*
Carbon concentration	4.7	n.a.	1×10^{15}	cm^{-3}	LVM spectroscopy	SEMI M30 DIN 50449-1	5.4
Electrical resistivity	4.11	n.a.	$>1 \times 10^{7}$	Ωcm	Hall effect Capacitive probe	SEMI F76, M39 DIN 50448	5.5
Electron mobility	4.12	n.a.	> 6000	cm^2/Vs	Hall effect	SEMI F76, M39	5.6
EPD of LEC grown material	4.13	150 mm 100 mm 76 mm	$< 1.5 \times 10^{5}$ $< 1.0 \times 10^{5}$ $< 1.0 \times 10^{5}$	cm^{-2}	Structural etching + light reflection	ASTM F1404, DIN 50454-1	5.7
EPD of VGF and VB material	4.13	150 mm 100 mm 76 mm	$< 1 \times 10^{4}$ $< 5 \times 10^{3}$ $< 5 \times 10^{3}$	cm^{-2}	Structural etching, light reflection, microscopy	SEMI M36 DIN 50454-1	5.8
Particles with diameter ≥ 300 nm	4.17	150 mm 100 mm 76 mm	< 100 < 40 < 20	Wafer with edge exclusion	Laser scattering	none	5.9
Microroughness (haze)	4.17	n.a.	not visible	Wafer with edge exclusion	High intensity illumination	none	5.18

Table 2 Optional SI GaAs Material Parameter Specifications

Parameter	*Section*	*Verification Technique*	*Section*
Average $EL2^0$concentration	4.5	Optical absorption	5.10
Total concentration of impurities acting as donors	4.6	GDMS, SSMS	5.11
Total concentration of impurities acting as acceptors	4.7	GDMS, SSMS	5.12
Concentration of boron	4.9	DIN 50449-2, GDMS, SSMS, SIMS, AAS	5.13
Surface concentration of specified contaminants	4.17	TOF-SIMS, TXRF	5.14
Epi-ready qualification including shelf life	4.18	Supplier/purchaser specific	5.15
Surface irregularities (stain, scratches, pits, orange peel, dimples)	4.17	High intensity illumination or microscopic inspection (SEMI M15)	5.19

Table 3 Other SI GaAs Material Parameters

Parameter	*Section*	*Verification Technique*	*Section*
Lateral variation of $EL2^0$ concentration	4.5	Optical absorption topography	5.10
Lateral variation of resistivity	4.11	Transient capacitance, DIN 50448	5.5
Lateral variation of EPD	4.14	Structural etching and light reflection, DIN 50454-1	5.8

5 Available from Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, website: www.din.de

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SEMI M55-0705
SPECIFICATION FOR POLISHED MONOCRYSTALLINE SILICON CARBIDE WAFERS

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the European Compound Semiconductor Materials Committee. Current edition approved by the European Regional Standards Committee on January 8, 2003. Initially available at www.semi.org January 2003; to be published March 2003.

NOTICE: The designation of SEMI M55 was updated during the 0705 publishing cycle to reflect the creation of SEMI M55.2.

1 Purpose

1.1 These specifications cover substrate requirements for monocrystalline high-purity silicon carbide wafers of crystallographic polytype 6H and 4H used in semiconductor and electronic device manufacturing.

2 Scope

2.1 A complete purchase specification may require that additional physical, electrical, and bulk properties be defined. These properties are listed, together with test methods suitable for determining their magnitude where such procedures are documented.

2.2 These specifications are directed specifically to silicon carbide wafers with one or both sides polished. Unpolished wafers or wafers with epitaxial films are not covered; however, purchasers of such wafers may find these specifications helpful in defining their requirements.

2.3 The material is Single Crystal Silicon Carbide (SiC) existing in many crystallographically different polytypes. For the most common polytypes the following properties in Table 1 are listed for use as guidelines:

Table 1 Common Properties[1]

Polytype		*4H*	*6H*
Lattice Parameter	a c	3.076 Å 10.053 Å	3.073 Å 15.117 Å
Stacking Sequence		ABAC	ABCACB
Density		3.21 g/cm^3	3.21 g/cm^3
Melting Point		chemical decomposition above ca. 2800°C	chemical decomposition above ca. 2800°C
Dielectric Constant		9.7	9.7
Energy Gap		3.27 eV	3.02 eV

2.4 For referee purposes, SI (System International, commonly called metric) units shall be used.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specification for Polished Mono-crystalline Silicon Wafers

1 Data as reported in Landolt-Börnstein (Springer Verlag)

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

3.2 *ASTM Standards*[2]

ASTM E122 — Standard Practice for Calculating Sample Size to Estimate, With a Specified Tolerable Error, the Average for Characteristic of a Lot or Process

ASTM F26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

ASTM F154 — Standard Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

ASTM F523 — Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

ASTM F533 — Standard Test Method for Thickness and Thickness Variation of Silicon Wafers

ASTM F534 — Standard Test Method for Bow of Silicon Wafers

ASTM F657 — Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

ASTM F671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

ASTM F673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

ASTM F847 — Standard Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon and Wafers by X-Ray Techniques

ASTM F928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

ASTM F1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning

ASTM F1404 — Test Method for Crystallographic Perfection of Gallium Arsenide by Molten Potassium Hydroxide (KOH) Etch Technique

ASTM F1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

ASTM F2074 — Standard Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.3 *DIN Standards*[3]

DIN 50441/1 — Measurement of the Geometric Dimensions of Semiconductor Wafers: Thickness and Thickness Variation

DIN 50448 — Testing of materials for semiconductor technology - Contactless determination of the electrical resistivity of semi-insulating semiconductor slices using a capacitive probe

3.4 *JIS Standard*[4]

JIS H 0611 — Methods of Measurement of Thickness Taper and Bow for Silicon Wafers

3.5 *Other Standards*

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes[5]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

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2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

3 Available from Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, website: www.din.de

4 Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp

5 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202, USA

4 Terminology

NOTE 1: Many definitions and terms not given in this section can be found in SEMI M1, the SEMI Compilation of Terms, and ASTM F154.

4.1 *Definitions*

4.1.1 *bow* — of a semiconductor wafer, a measure of concave or convex deformation of the median surface of a wafer, independent of any thickness variation which may be present. Bow is a bulk property of the test specimen, not a property of an exposed surface. Generally, bow is determined with a test specimen in a free, unclamped condition. Units of bow are generally micrometers.

4.1.2 *crystallite* — any part of the wafer, having an arbitrary orientation of its crystallographic axis in respect to the monocrystalline part of the wafer.

4.1.3 *dopant* — a chemical element, usually from the third or fifth column of the periodic table for the case of IV-IV compounds, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity.

4.1.4 *edge contouring* — on wafers whose edges have been shaped by mechanical and/or chemical means, a description of the profile of the boundary of the wafer joining the front and back sides.

4.1.5 *edge exclusion* — the width X of a narrow band of wafer surface, located just inside the wafer edge, over which the values of the specified parameter do not apply. See definition of *fixed quality area* below.

4.1.6 *fixed quality area (FQA)* — The central area of a wafer surface, defined by a nominal *edge exclusion*, *X*, over which the specified values of a parameter apply.

4.1.6.1 *Discussion* — The boundary of the FQA is at all points the distance *X* away from the periphery of a wafer of nominal dimensions. (See Figure 1.) The size of the FQA is independent of wafer diameter and flat length tolerances.

4.1.7 *lot* — for the purpose of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above which have been identified by the supplier as constituting a lot.

4.1.8 *micropipe* — small hollow tube approximately parallel to the crystallographic c-axis and extending through the whole crystal.

4.1.9 *orthogonal misorientation* — in {0001} wafers cut intentionally “off-orientation”, the angle between the projection of the vector normal to the wafer surface onto the {0001} plane and the projection on that plane of the specified direction of tilt in the {0001} plane. (See Figure 2.)

4.1.10 *planar defect* — small cavity in a SiC bulk crystal with large width-to-height ratio roughly parallel to the {0001} lattice plane. The lateral boundaries are parallel to crystallographic directions. Often one or more micropipes are connected to a planar defect.

4.1.11 *polytype* — one possible crystallographic modification of a substance which shows the phenomenon of polytypism. All polytypes of a substance have the same lattice layers with nearly the same lattice constant in common. However the stacking sequence of these layers differs between different polytypes. Most commonly polytypes are named after a suggestion of Ramsdell[6]: A symbol like 6H gives the number of layers in one periodic stacking sequence (2, 3, 4, ...) and the symmetry of the resulting crystal (H = hexagonal, R = rhombohedral). The most common polytypes of SiC are 6H, 4H, 15R.

4.1.12 *surface orientation* — the tilt angle between the crystallographic c-axis and the wafer surface normal. (See Figure 2.)

4.1.13 *total indicator reading (TIR)* — the smallest perpendicular distance between two planes, both parallel with the reference plane, which encloses all points on the front surface of a wafer within the FQA, the site, or the subsite, depending on which is specified.

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6 L. S. Ramsdell, J. A. Kohn: Developments in Silicon Carbide Research, Acta Cryst. 5 (1952) 215 – 224

4.1.14 *total thickness variation* (TTV) — the difference between the maximum and minimum thickness values of a wafer encountered during a scan pattern or a series of point requirements. TTV is generally expressed in micrometers.

4.1.15 *warp* — of a semiconductor slice or wafer, the difference between the maximum and minimum distance of the median surface of the wafer from a reference plane, encountered during a scan pattern. Warp is a bulk property of the test specimen, not a property of an exposed surface. Warp is generally expressed in micrometers.

5 Ordering Information

5.1 Purchase orders for silicon carbide wafers furnished to this specification shall include the following items:

5.1.1 Polytype,

5.1.2 Nominal diameter (see applicable SEMI Standard for polished SiC wafers),

5.1.3 Thickness (see applicable SEMI Standard for polished SiC wafers),

5.1.4 Dopant (see applicable SEMI Standard for polished SiC wafers),

5.1.5 Resistivity or Carrier Concentration (see applicable SEMI Standard for polished SiC wafers),

5.1.6 Total Thickness Variation (see applicable SEMI Standard for polished SiC wafers),

5.1.7 Surface orientation (see applicable SEMI Standard for polished SiC wafers),

5.1.8 Polarity of Surfaces (see applicable SEMI Standard for polished SiC wafers),

5.1.9 Lot Acceptance Procedures (see §7),

5.1.10 Certification (see §11), and

5.1.11 Packing and Marking (see §12).

6 Dimensions and Permissible Variations

6.1 The material shall conform to the dimensions and dimensional tolerances as specified in the applicable polished silicon carbide wafer standard.

6.2 The material shall conform to the crystallographic orientation details as specified in the applicable polished silicon carbide wafer standard.

6.3 If edge contoured wafers are specified on the purchase order, the profile shall conform to the following requirements at all points on the wafer periphery.

6.3.1 When the wafer is aligned with the SEMI Wafer Edge Profile Template (see Figure 3) so that the x-axis of the template is coincident with the wafer surface and the y-axis of the template forms a tangent with the outermost radial portion of the contour, the wafer edge profile must be contained within the clear region of the template. (See Figure 4 for example of acceptable and unacceptable contours.)

6.3.2 Cosmetic attributes of the edge contour are not covered by this specification. They shall be agreed upon between supplier and purchaser.

6.4 Flats shall conform to the requirements of §9 and the appropriate polished silicon carbide wafer standard.

NOTE 2: For edge chips and indents see §10.

7 Sampling

7.1 Unless otherwise specified, ASTM Practice E122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

8 Test Methods

NOTE 3: SiC wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement methods.

8.1 *Test Plan for Crystal Quality within One Crystal* — Determine by a method agreed upon between the supplier and purchaser.

NOTE 4: The assessment of the crystal quality is a problem of great practical impact as it can be very time consuming and costly or even impossible in the case of destructive test methods to test every wafer. However in general crystal quality does not change abruptly in a crystal. The evaluation of a subset of all wafers from a given crystal will give sufficient information about the quality of the whole crystal.

8.2 *Polytype* — For nominally undoped material ($n < 10^{17}/cm^3$) determine by visual inspection at 77K (liquid nitrogen) under UV excitation. For doped material ($n > 10^{17}/cm^3$) determine by visual inspection of the colors of the doped material under diffuse lighting conditions.

8.3 *Diameter* — Determine by ASTM Test Method F2074.

8.4 *Thickness, Center Point* — Determine by ASTM Test Method F533.

8.5 *Flat Length* — Determine by ASTM Test Method F671.

8.6 *Bow and Warp* — Determine bow in accordance with ASTM Test Method F534 and warp in accordance with ASTM Test Method F657.

NOTE 5: ASTM has standardized two methods for measuring warp. ASTM Test Method F1390 is an automated, non-contact method which provides for correction of the wafer deflection due to gravitational effects. The scan pattern covers the entire fixed quality area. ASTM Test Method F657 is a manual, non-contact method which has a continuous, prescribed scan pattern which covers only a portion of the wafer surface. There is no provision for correction of the wafer deflection due to gravitational effects. As noted in Appendix 2, different reference planes are used for the two methods. Because Test Method F657 employs a back surface reference plane, the measured warp may include contributions from thickness variation of the wafer. Test Method F1390 employs a median surface reference plane and is not susceptible to interferences from thickness variations. In general, Test Method F1390 is preferred, especially for wafers 150 mm in diameter and larger.

8.7 *Total Thickness Variation* — Determine by ASTM Test Method F657.

NOTE 6: ASTM Test Method F533, DIN 50441/1 and JIS H 0611 are all 5 point methods, while Test Method F657 involves a continuous scan pattern over a portion of the wafer surface and Test Method F1530 involves an automated continuous scan pattern over the entire wafer surface. JIS H 0611 differs from ASTM Test Method F533 and DIN 50441/1, in that the measurements in JIS H 0611 are taken at the center and at 5 mm from the edge on diameters parallel and perpendicular to the primary orientation flat or notch bisector, while the measurements in ASTM Test Method F533 and DIN 50441/1 are taken at the center and at the same radial distance ($R_{nominal}$ -6 mm) on diameters 30° and 120° counterclockwise from the bisector to the primary orientation flat or notch (with the wafer facing front surface up).

8.8 *Surface Polarity* — Determine by a method agreed upon between the supplier and the purchaser.

NOTE 7: There are several destructive and non-destructive methods. Most common examples are a chemical etch of the surface (destructive), by comparing the differently reacting carbon and silicon faces, and wet oxidation (non-destructive) by comparing the different growth rates on both surfaces by measuring the oxide layer thickness.

8.9 *Flat Orientation* — Determine by ASTM Test Methods F847.

8.10 *Surface Orientation* — Determine by ASTM Test Methods F26.

8.11 *Orthogonal Misorientation* — Determined by a method agreed upon between the supplier and purchaser.

8.12 *Surface Defects and Contamination*

8.12.1 *Visually Observable Surface Defects* — Determined by ASTM Practice F523 or a method agreed upon between the supplier and purchaser.

8.13 *Edge Contour* — Determine by ASTM Test Method F928.

8.14 *Resistivity* — For conductive wafers determine by ASTM Test Method F43 or ASTM Test Method F673. For high-resistivity or semi-insulating material determine by DIN 50448.

NOTE 8: ASTM F43 is a four-point-probe technique whereas ASTM F673 is an inductive non-contact method. These methods are limited to some 10^2 Ωcm. DIN 50448 is a non-contact capacitive method suitable for the range 10^5 to 10^{11} Ωcm.

8.15 *Etch Pit Density* — Determine by ASTM Test Method F1404 or a method agreed upon between the supplier and purchaser.

NOTE 9: ASTM test method F1404 was intended only for use with gallium arsenide. Nevertheless it should serve as a guideline for determining the etch pit density of silicon carbide.

8.16 *Micropipe Density* — Determine by a method agreed upon between the supplier and purchaser.

8.17 *Crystal Perfection* — Determine by a method agreed upon between the supplier and purchaser.

9 Flat System

9.1 For silicon carbide wafers with the surface normal close to the crystallographic c-axis (small tilt angles, see Figure 2) one primary orientation flat and one secondary flat is specified. The primary flat always has a greater flat length compared to the secondary flat. (See Figure 6.)

9.2 The angle between primary and secondary flat is always 90° (see Figure 5). For the tolerance see the appropriate silicon carbide wafer standard.

9.3 The polarity of the wafer surfaces is indicated by the relative flat positions of primary and secondary flat as shown in Figure 5.

9.4 The edge of the primary flat is always parallel to the [11-20] direction (or, which is the same, parallel to the (1-100) lattice plane.) For tolerances see the appropriate silicon carbide wafer standard.

9.5 For the exact dimensions of the flat length and the tolerances see the appropriate silicon carbide wafer standard.

10 Standard Defect Limits

10.1 Minimal conditions or dimensions for surface defects are stated below. These limits shall be used for determining wafer acceptability; anomalies smaller than these limits shall not be considered as defects.

10.2 *Surface Defects*

10.2.1 *edge chip and indent* — Any edge anomaly including saw exit marks conforming to the definition (ASTM F154) and greater than 0.25 mm in radial depth and peripheral length. (See Figure 7.)

10.2.2 *orange peel* — Any visually detectable roughened surface conforming to the definition (ASTM F154) and observable under diffused illumination. Pits with a spacing of less than 2 mm are treated as orange peel.

10.2.3 *particles* — Distinct particles resting on the surface which are revealed under collimated intense light as bright points.

10.2.4 *pit* — Any individually distinguishable depression in the surface with a length-to-width ratio smaller than 5:1, visible when viewed under intense illumination.

NOTE 10: This definition is different from ASTM F154 in so far as the slope of the sides of the depression are not taken into account.

10.2.5 *scratch* — Any anomaly conforming to the definition (ASTM F154) and having a length-to-width ratio greater than 5:1 and visible under intense illumination.

10.3 *Bulk Defects*

10.3.1 *crack* — Any anomaly conforming to the definition (ASTM F154) and greater than 0.25 mm in total length.

10.3.2 *crystallite* — Any anomaly conforming to the definition (see §3) and having a misorientation of more than 1° to the main (monocrystalline) part of the wafer and having a maximum width larger than 0.20 mm.

10.3.3 *micropipe* — Any anomaly conforming to the definition (see §3) and visible by microscopic inspection in transmission mode at a magnification of 100× or after etching in molten KOH, which will reveal micropipes as hexagonal structures.

NOTE 11: For microscopic inspection the use of crossed polarisers is recommended. However not all micropipes will be visible under crossed polarisers.

10.3.4 *planar defect* — Any anomaly conforming to the definition (see §3) having a maximum width larger than 0.20 mm.

11 Certification

11.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification together, with a report of the test results, shall be furnished at the time of shipment.

11.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in §8. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

12 Packing and Marking

12.1 The wafers supplied under these specifications shall be identified by an individual laser marking consisting of the supplier assigned lot-number on the backside of each wafer. The laser marking consists of one line of characters parallel to the primary flat and must be readable with unaided eye. The top of the characters is directed towards the wafer center. All characters must be completely located within the marking window given in Figure 8. For details see the appropriate polished Silicon Carbide Wafer Standard.

NOTE 12: SEMI M12 is a standard for the *front side* marking of silicon wafers and, as a whole, is not applicable to Silicon Carbide wafers. It is referenced, because some elements of SEMI M12 (see the appropriate polished Silicon Carbide Wafer Standard) shall also be used for Silicon Carbide.

12.2 Special packing and marking requirements shall be subject to agreement between the supplier and the purchaser. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination in accordance with the best industry practices to provide ample protection against damage during shipment.

12.3 The wafers shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductive dopant, orientation, resistivity range, and lot number.

12.4 The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to slice manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least 10 years or as negotiated between vendor and user after that particular lot has been accepted by the purchaser.

13 Related Documents

13.1 *ASTM Standards*

ASTM F76 — Test Methods for Measuring Resistivity and Hall Coefficient and Determining Hall Mobility in Single-Crystal Semiconductors

ASTM F1241 — Terminology of Silicon Technology

13.2 *DIN-Standards*

DIN 50433/1 — Determination of the Orientation of Single Crystals by Means of X-Ray Diffraction

DIN 50433/3 — Determination of the Orientation of Single Crystals by Means of Laue Back Scattering

DIN 50441/2 — Measurement of the Geometric Dimensions of Semiconductor Wafers: Testing of Edge Profile

DIN 50441/4 — Measurement of the Geometrical Dimensions of Semiconductor Wafers: Slice Diameter, Diameter Variation, Flat Diameter, Flat Length, Flat Depth

DIN 50445 — Testing of materials for semiconductor technology; Contactless determination of the electrical resistivity of semiconductor slices with the eddy current method; Homogeneously doped semiconductor wafers

13.3 *ISO Standards*

ISO 4287 — Geometrical Product Specifications (GPS) -- Surface texture: Profile method -- Terms, definitions and surface texture parameters[7]

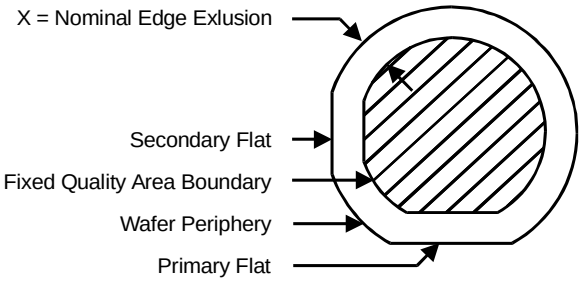


Figure 1
Fixed Quality Area

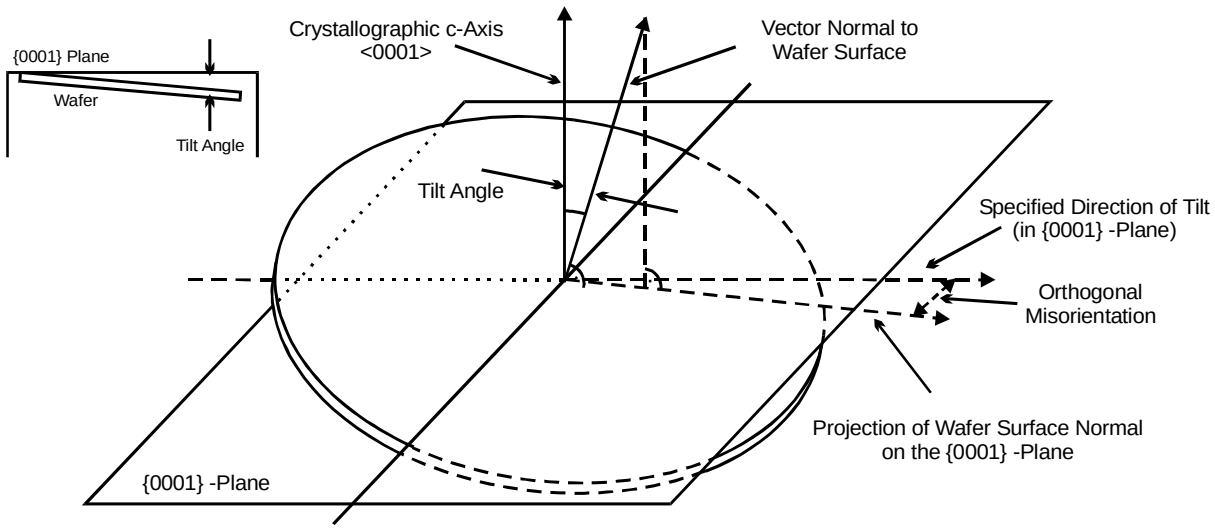


Figure 2
Orthogonal Misorientation

7 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch

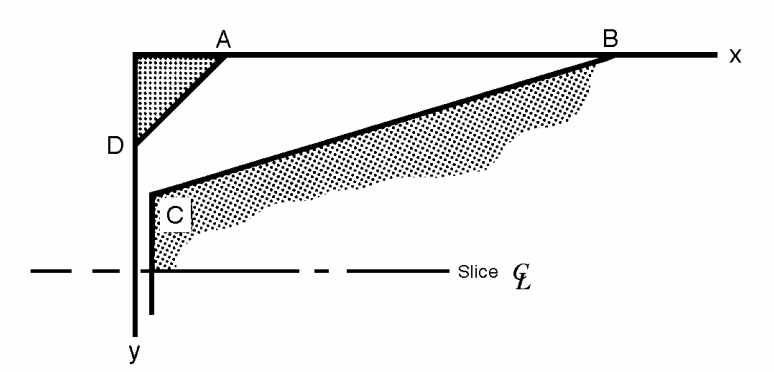


Figure 3
SEMI Wafer Edge Profile Template

NOTE 13: For the exact dimensions and coordinates of points A to D see the appropriate silicon carbide wafer standard.

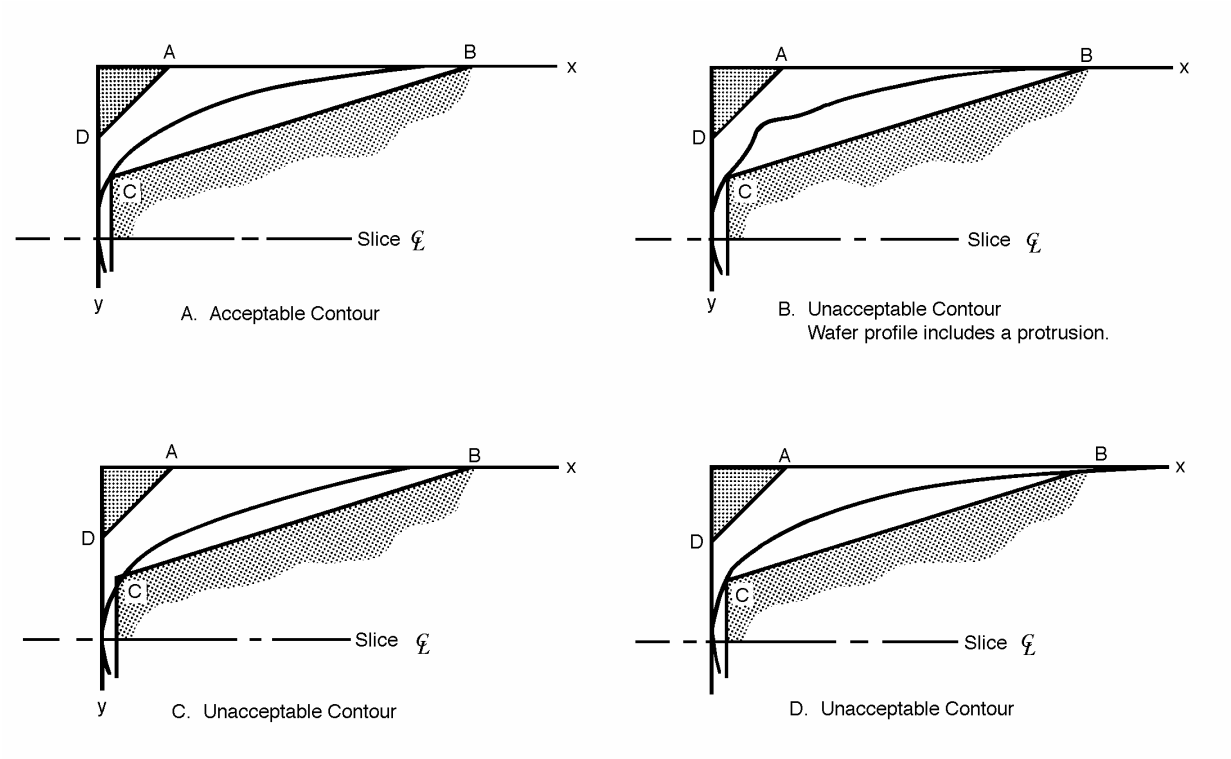


Figure 4
Examples of Acceptable and Unacceptable Wafer Edge Profiles

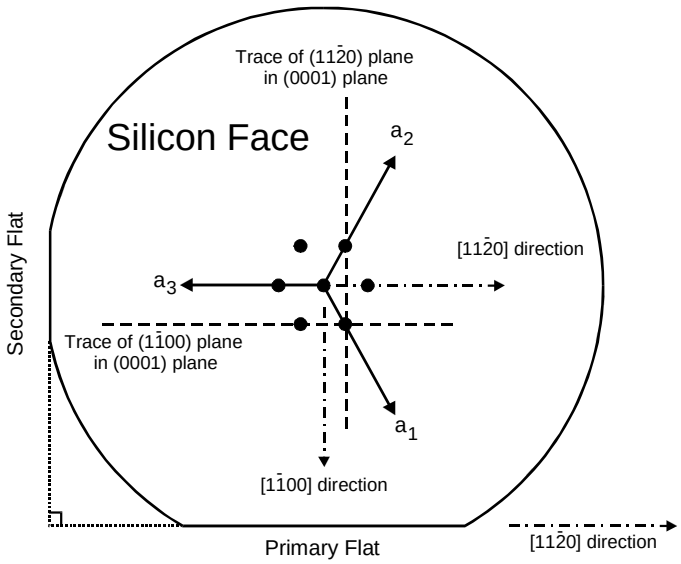


Figure 5
Relation of Lattice Sites, Crystallographic Planes and Flats (flat length not to scale)
The position of the secondary flat is shown for view on the Silicon face.

NOTE 14: For the exact dimensions and tolerances of primary and secondary flats see the appropriate polished silicon carbide wafer standard.

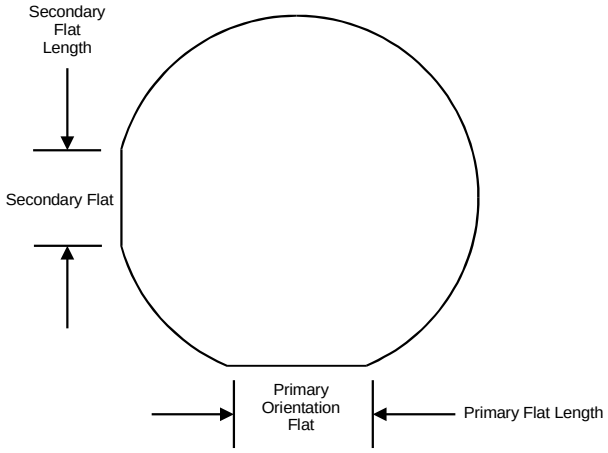


Figure 6
Flat Length of Primary Orientation Flat and Secondary Flat

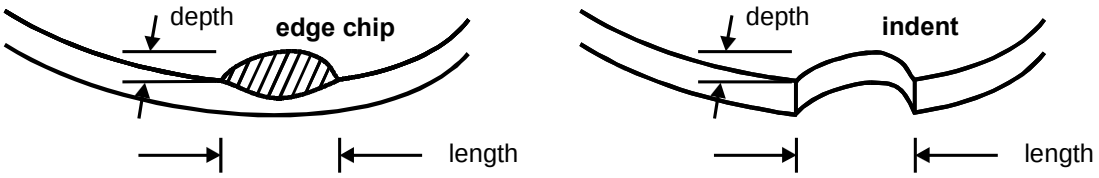


Figure 7
Depth and length of edge chip and indent

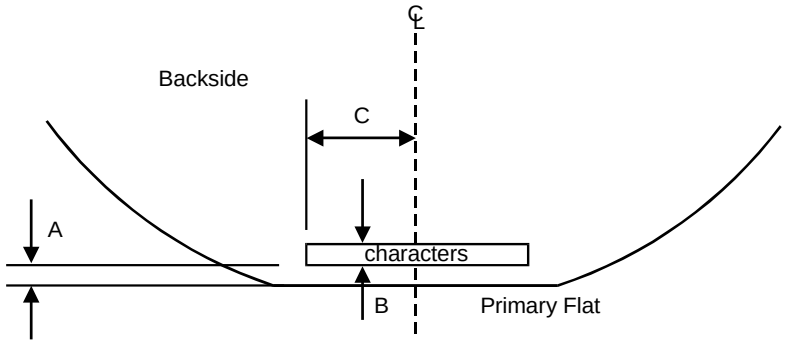


Figure 8
Definition of Window for Laser Marking
The width of the permitted window is twice dimension C.

NOTE 15: For the exact dimensions of A, B, and C, see the appropriate wafer standard.

SEMI M55.1-0304
SPECIFICATION FOR 50.8 mm ROUND POLISHED MONOCRYSTALLINE 4H AND 6H SILICON CARBIDE WAFERS

This specification was technically approved by the Global Compound Semiconductor Committee and is the direct responsibility of the European Compound Semiconductor Materials Committee. Current edition approved by the European Regional Standards Committee on October 29, 2003. Initially available at www.semi.org January 2004; to be published March 2004.

NOTE 1: This specification is intended to be a sub-document to SEMI M55, Specification For Polished Monocrystalline Silicon Carbide Wafers.

1 Purpose

1.1 This subordinate standard details the dimensional values and other information required for 50.8 mm polished monocrystalline silicon carbide wafers.

2 Scope

2.1 The complete specification for this product includes all general requirements of SEMI M55, Specification For Polished Monocrystalline Silicon Carbide Wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 The backside finish properties, dopant, and resistivity are not addressed, as currently these properties depend strongly on the quick evolving technology and suitable limits for a standard do not exist.

4 Requirements

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*
DIAMETER	50.8	± 0.25	mm
PRIMARY FLAT LENGTH	15.8	± 1.6	mm
SECONDARY FLAT LENGTH	8.0	± 1.6	mm
BOW	0	± 25	µ m
WARP	0	< 25	µ m
TOTAL THICKNESS VARIATION	0	< 25	µ m
TOTAL INDICATOR READING	0	< 25	µ m

Table 2 Thickness Requirements (Center Point)

	Dimension	*Tolerance*	*Units*
Option 1:	250	± 25	µ m
Option 2:	330	± 25	µ m

NOTE 1: As the industrial requirements for a unique thickness specification are not established at the time of creation of this standard, two values are defined. This is to be regarded as a preliminary in that way, that in a future revision of this standard these options can be expected to be replaced by a unique definition.

Table 3 Orientation and Flat Location Requirements

Property	*Dimension*
SURFACE ORIENTATION (see Note 1)	*Tilt angle* (see Figure 2 in SEMI M55)
Option 1: "on axis"	0 + 0.25°
Option 2: "off axis (11$\bar{2}$0)"	3.5° ± 0.5° parallel to edge of primary flat away from secondary flat (see Note 1)
Option 3: "off axis (11$\bar{2}$0)"	8.0° ± 0.5° parallel to edge of primary flat away from secondary flat (see Note 1)
Option 4: "off axis (1$\bar{1}$00)"	3.5° ± 0.5° parallel to edge of secondary flat away from primary flat (see Note 1)
Option 5: "off axis (1$\bar{1}$00)"	8.0° ± 0.5° parallel to edge of secondary flat away from primary flat (see Note 1)
ORTHOGONAL MISORIENTATION	± 5° (See Figure 2 in SEMI M55)
TOLERANCE OF PRIMARY FLAT ORIENTATION	± 1°
TOLERANCE OF SECONDARY FLAT ORIENTATION (see Note 4)	± 5° relative to primary flat

NOTE 1: The frame of reference is the (0001)-plane of the crystal. It is the wafer normal on the silicon-face that is tilted towards the given crystallographic direction. That means that the crystallographic c-axis lies between the secondary/primary flat (for the (11$\bar{2}$0)/(1$\bar{1}$00) option) and the silicon-face surface normal vector (See Figure 1 and 2).

NOTE 2: The angle between primary and secondary flat is defined in Figure 5 in SEMI M55.

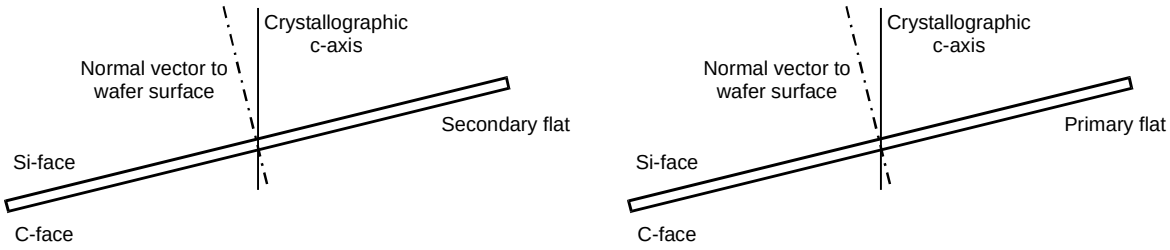


Figure 1
Definition of the Sign of the Tilt Angle (left: off axis (11$\bar{2}$0) -option, right off axis (1$\bar{1}$00) Option)

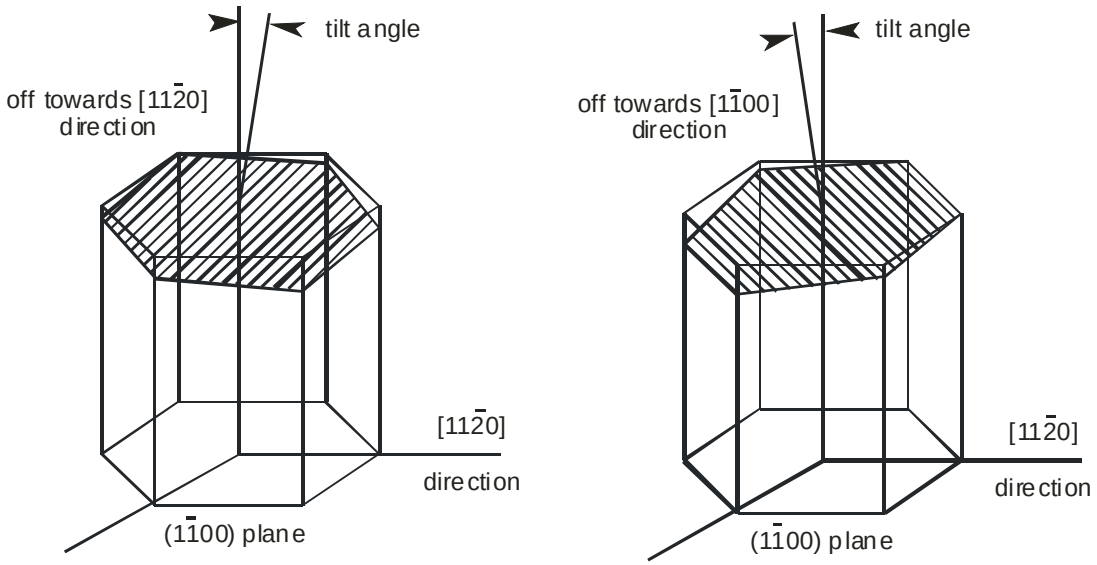


Figure 2
Direction of Tilt (left: (11$\bar{2}$0) option, right off axis (1$\bar{1}$00) option)

Table 4 Polished Wafer Defect Limits

Item	*Characteristics*	*Maximum Defect Limit*	*Test Condition*	*Note*
Front Surface				
1	visible scratches	none	high intensity, unaided eye	1
2	pits (number)	10	high intensity, unaided eye	1
3	orange peel (area)	10 %	diffuse, unaided eye	1
4	particles (number)	4	high intensity, unaided eye	1
5	edge chips and indents (number)	≤ 3 with maximum length and width 1.0 mm		
Back Surface				
6	edge chips (number)	≤ 3 with maximum length and width 1.0 mm		
Bulk				
7	cracks (number)	none	diffuse, unaided eye	
8	micropipes (mean density)	defined by customer and supplier		
9	planar defects, spacing >2 mm (number)	10	diffuse, unaided eye	1
10	planar defects, spacing ≤ 2 mm (affected area)	10 %	diffuse, unaided eye	1
11	crystallite (area)	5 %	diffuse, polarisers	1
12	foreign polytypes (area)	10 %	diffuse	1
Cumulative Defect Area				
12	all listed defects of type “area”	total 10 %		1

NOTE 1: The Edge-Exclusion X (See Figure 1 of SEMI M55) is 1 mm.

Table 5 Laser Marking Requirements (see figure 8 of SEMI M55)

Property	*Dimension*	*Units*	
GEOMETRY			
dimension A	0.5	mm	
dimension B	2.0	mm	
dimension C	7.5	mm	See Note 1.
CHARACTER DIMENSIONS AND OUTLINE	not defined		readable with unaided eye (SEMI M55)
CHARACTER SET	Defined by SEMI M12		
FORMAT OF ID-STRING (see Note 2)	NNNNNNNNNNSSCC		NNNNNNNNNN: (10 characters) supplier defined ID of wafer, with a dash as separator. Unused characters are filled with dash characters. Alphanumeric. SS: (2 characters) Supplier Code as defined in SEMI AUX001. Alpha only. CC: (2 characters) Checksum Characters generated by the algorithm defined in SEMI M12. The first character is alpha only, the second numeric only.

NOTE 1: The total width of the marking window is twice dimension C.

NOTE 2: This definition of the ID-string is intended to identify wafers from different suppliers and to support use of OCR-techniques. Both cannot be accomplished with the currently widely used proprietary formats for the ID-strings.

SEMI M55.2-0705
SPECIFICATION FOR 76.2 mm ROUND POLISHED MONOCRYSTALLINE 4H AND 6H SILICON CARBIDE WAFERS

This specification was technically approved by the global Compound Semiconductor Materials Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on May 20, 2005. It was available at www.semi.org in June 2005 and on CD-ROM in July 2005.

1 Purpose

1.1 This subordinate standard detail the dimensional values and other information required for 76.2mm polished monocrystalline silicon carbide wafers.

2 Scope

2.1 The complete specification for this product includes all general requirements of SEMI M55, Specification For Polished Monocrystalline Silicon Carbide Wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 The backside finish properties, dopant and resistivity are not addressed, as currently these properties depend strongly on the quick evolving technology and suitable limits for a standard do not exist.

4 Referenced Standards and Documents

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI AUX1 — List of Wafer Supplier Identification Codes

5 Terminology

5.1 None.

6 Requirements

Table 1 Dimension and Tolerance Requirements

Property	*Dimension*	*Tolerance*	*Units*
DIAMETER	76.2	±0.25	mm
PRIMARY FLAT LENGTH	22.0	±2.0	mm
SECONDARY FLAT LENGTH	11.0	±1.5	mm
BOW	0	±25	µm
WARP	0	<25	µm
TOTAL THICKNESS VARIATION	0	<25	µm
TOTAL INDICATOR READING	0	<25	µm
THICKNESS	350	±25	µm

Table 2 Orientation and Flat Location Requirements

Property	*Dimension*
SURFACE ORIENTATION [#1, #2]	*Tilt angle* (see Figure 2 in SEMI M55)
Option 1:"on axis"	0 + 0.25°

Property	*Dimension*
SURFACE ORIENTATION [#1, #2]	*Tilt angle* (see Figure 2 in SEMI M55)
Option 2:"off axis $(11\bar{2}0)$"	4.0° ± 0.5° parallel to edge of primary flat away from secondary flat [#3]
Option 3:"off axis $(11\bar{2}0)$"	8.0° ± 0.5° parallel to edge of primary flat away from secondary flat [#3]
Option 4:"off axis $(1\bar{1}00)$"	4.0° ± 0.5° parallel to edge of secondary flat away from primary flat [#3]
Option 5:"off axis $(1\bar{1}00)$"	8.0° ± 0.5° parallel to edge of secondary flat away from primary flat [#3]
ORTHOGONAL MISORIENTATION	±5° (See Figure 2 in SEMI M55)
TOLERANCE OF PRIMARY FLAT ORIENTATION	±2°
TOLERANCE OF SECONDARY FLAT ORIENTATION [#2]	±5° relative to primary flat

[#1] The frame of reference is the (0001)-plane of the crystal. It is the wafer normal on the silicon-face that is tilted towards the given crystallographic direction. That means that the crystallographic c-axis lies between the secondary/primary flat (for the $(11\bar{2}0)$ / $(1\bar{1}00)$ option respectively) and the silicon-face surface normal vector (See Figure 1 and 2).

[#2] Measured at the center of the wafer.

[#3] The angle between primary and secondary flat is defined in Figure 5 in SEMI M55.

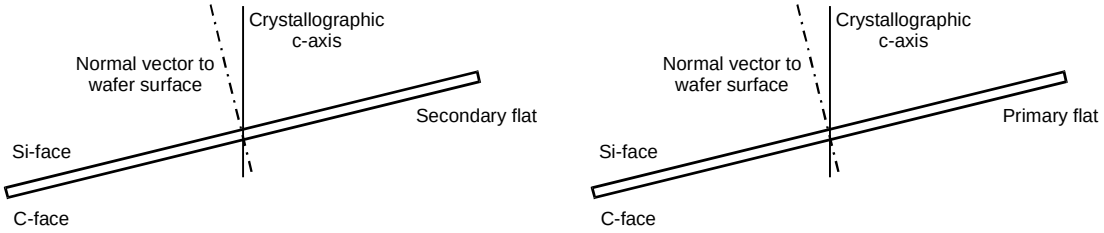


Figure 1

Definition of the Direction of the Tilt Angle (Left: Off Axis $(11\bar{2}0)$ -Option, Right Off Axis $(1\bar{1}00)$ Option)

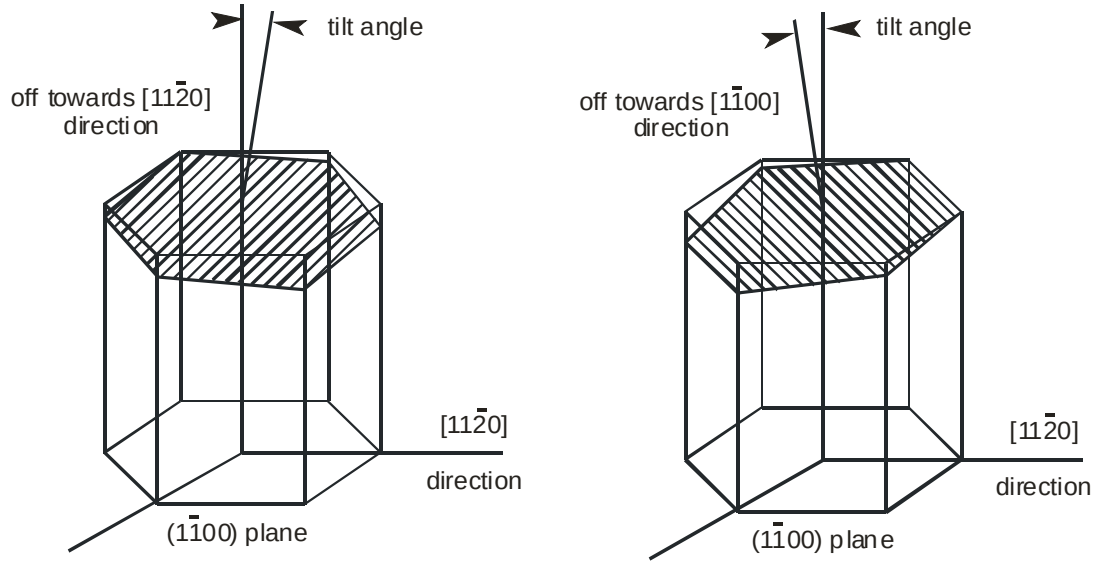


Figure 2

Direction of tilt (left: $(11\bar{2}0)$ option, right off axis $(1\bar{1}00)$ -option)

Table 3 Polished Wafer Defect Limits

Item	*Characteristics*	*Maximum Defect Limit*	*Test Condition*	*Note*
Front Surface				
1	visible scratches	None	high intensity, unaided eye	1
2	pits (number)	10	high intensity, unaided eye	1
3	orange peel (area)	10%	diffuse, unaided eye	1
4	particles (number)	6	high intensity, unaided eye	1
5	edge chips and indents (number)	≤3 with maximum length and width 1.0 mm		
Back Surface				3
6	edge chips (number)	≤3 with maximum length and width 1.0 mm		
7	visible surface inhomogeneity	defined by customer and supplier		2
Bulk				
8	cracks (number)	None	diffuse, unaided eye	
9	micropipes (mean density)	defined by customer and supplier		
10	planar defects, spacing >2 mm (number)	15	diffuse, unaided eye	1
11	planar defects, spacing ≤ 2 mm (affected area)	10%	diffuse, unaided eye	1
12	crystallite (area)	5%	diffuse, polarisers	1
13	foreign polytypes (area)	10%	diffuse	1
Cumulative Defect Area				
14	all listed defects of type “area”	total 10%		1

[#1] The Edge-Exclusion X (See Figure 1 of SEMI M55) is 1 mm.

[#2] Dependant on backside finish.

[#3] The back side finish properties are not specified.

Table 4 Laser Marking Requirements (see Figure 8 of SEMI M55)

Property	*Dimension*	*Units*	
GEOMETRY			
dimension A	0.5	mm	
dimension B	2.0	mm	
dimension C	10.0	mm	[#1]
MARKING DEPTH	≤ 100	µm	target value 30µm
CHARACTER SET	Defined by SEMI M12		character font and proportions (“SEMI OCR”), not font size
CHARACTER DIMENSIONS			
Option 1: “large”[#3, #4]			dimensions according to SEMI M12, readable with unaided eye
Character Height	1.624 ± 0.025	mm	width and thickness are defined by the proportions given in SEMI M12
Character Spacing	1.420 ± 0.025	mm	
Option 2: “small”[#2, #4]			dimensions according to SEMI M13, readable with unaided eye
Character Height	0.812 ± 0.025	mm	width and thickness are defined by the proportions given in SEMI M13
Character Spacing	0.710 ± 0.025	mm	

Property	*Dimension*	*Units*	
FORMAT OF ID-STRING			
Option 1:"OCR Checksum Character"[#2, #4]	NNNNNNNNNNSSCC (14 characters total)		NNNNNNNNNN: (10 characters) supplier defined ID of wafer, with a dash as separator. Unused characters are filled with dash characters. Alphanumeric. SS: (2 characters) Supplier Identification Code as defined in SEMI AUX1. Alpha only. CC: (2 characters) Checksum Characters generated by the algorithm defined in SEMI M12. The first character is alpha only, the second numeric only.
Option 2: "manual reading"[#3, #4]	NNNNSS to NNNNNNNNNNSS (6 to 12 characters total)		NNNNNNNNNN: (4 to 10 characters) supplier defined ID of wafer, with a dash as separator. Alphanumeric with a dash as fill character. SS: (2 characters) Supplier Identification Code as defined in SEMI AUX1. Alpha only.

[#1] The total width of the marking window is twice dimension C.

[#2] Option is intended for use with automated systems including OCR-techniques.

[#3] Option is intended primarily for manual reading of the wafer ID and allows shorter ID-strings which are preferable for manual reading. A Supplier Identification Code is mandatory as the last two characters.

[#4] Size and format options may be used in any combination.

SEMI M56-1103
PRACTICE FOR DETERMINING COST COMPONENTS FOR METROLOGY EQUIPMENT DUE TO MEASUREMENT VARIABILITY AND BIAS

This practice was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on September 3, 2003. Initially available at www.semi.org October 2003; to be published November 2003.

1 Purpose

1.1 In silicon manufacturing product disposition is typically contingent on metrology equipment output. For example, a piece of work may be shipped, scrapped, or reworked based on information from one or more measured output characteristics. A cost model provides a mechanism for estimating the costs associated with operating metrology equipment under certain sets of assumptions and conditions.

1.2 This practice provides a standard methodology for metrology equipment suppliers and users to determine the cost due to misclassification of product because of measurement variability and bias during testing of the product for conformance to a specification.

1.3 This practice is intended to be useful for pre-purchase evaluation of measurement equipment with different P/T (Precision/Tolerance) ratios. It is also intended to be useful when comparing the operation of a single measurement instrument in different throughput modes where P/T ratio changes with the throughput mode utilized or other equipment setup factors. This practice can help users select the optimum cost solution based on their specific process capability and requirements.

1.4 Neither traditional cost elements (e.g., equipment, maintenance, operational, and staffing cost) nor product cost data are included in the practice; it is intended that each user should utilize appropriate data based on the applicable business model for the facility.

2 Scope

2.1 This practice covers a methodology to determine the costs associated with misclassification of product due to variability and bias of measurement equipment. These costs are associated with failing product that conforms with specifications and passing product that does not conform with specifications.

2.2 This practice can be applied to make relative cost comparisons between two or more measurement gauges operating under conditions specified by the user. These conditions may include any aspects of the measurement system affecting the measurement results directly or indirectly (e.g., ambient conditions, throughput, recipe). This practice can also be used to compare the relative costs of a single instrument under different operating conditions.

2.2.1 A measurement gauge is defined by a specific realization of systems and subsystems required to make measurements. Gauges that differ in at least one system or subsystem may be considered different for the purpose of comparison.

2.3 This practice can be applied to any metrology equipment or to the metrology portion of any equipment that includes metrology.

2.4 This practice covers the case in which the metrology equipment is used to make binary decisions about the item being measured, that is, only two outcomes are possible (e.g., pass/fail, go/no-go, ship/scrap). Models for decisions with more than two outcomes, such as the binning of data, are beyond the scope of this practice.

2.5 To apply the formulae in this practice, the user must estimate either the probability density function (PDF) or cumulative distribution function (CDF) of the process characteristic or characteristics of interest. The distributions can be based on a theoretical model or on empirical information obtained from manufacturing data.

2.6 To apply the formulae in this practice, the user must be able to estimate all biases and variances associated with the equipment being compared under the specified operating conditions and with respect to the process characteristic(s) of interest. These values can be obtained from a measurement system capability analysis (see SEMI E89).

2.7 To apply the methodology of this practice, the user must estimate the costs of classification and misclassification due to decisions made as a result of measurements. Estimates of such costs are obtained from the business model used to describe the manufacturing process in which the measurements are performed. Consequently, different users may arrive at different estimates of costs because their computations may contain different elements.

2.8 The output of this practice is the cost component due to measurement variability and bias for each process characteristic and metrology system evaluated.

2.9 This practice does not consider costs associated with other components of uncertainty outside of measurement variability and bias.

2.10 Although it is focused on the issue of misclassification, the practice may be extended to include costs associated with correct classification by the metrology equipment.

2.11 This practice was developed to evaluate metrology equipment used in silicon wafer manufacturing, but it may be extended to other types of metrology equipment by making suitable modifications.

NOTICE: This practice does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 Application of this practice requires that all measurement variances and biases, process characteristic distributions, and costs of classification and misclassification be accurately characterized. If this is not done, the resulting calculation may be in error.

3.2 Application of this practice also requires that measurement variances and biases be constant over the measurement range interval of interest. If this is not the case, the resulting calculation may be in error.

3.3 This practice considers only the case of two convolved distributions, process characteristic variability and measurement variability; consideration of additional distributions (such as would be required if the measurement bias or variance were assumed to be a function of the measured value) is beyond the scope of this practice.

3.4 Extension of the model to the cases of decisions based on (1) measurements on multiple gauges, (2) multiple inspections with the same gauge or (3) on multiple characteristics is outside the scope of this practice, but information on such extensions is provided in Related Information 1 for the convenience of the user.

3.5 This model should not be confused with a cost-of-ownership model, such as that developed in SEMI E35, which explicitly includes information on the cost elements involved.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E35 — Cost of Ownership for Semiconductor Manufacturing Equipment Metrics

SEMI E89 — Guide for Measurement System Capability Analysis

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M27 — Practice for Determining the Precision over Tolerance Ratio of Test Equipment

4.2 *ISO Document*[1]

International Vocabulary of Basic and General Terms in Metrology, Second Edition [VIM]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 General terminology related to metrology is defined in VIM.

5.2 Terminology relating to measurement system capability analysis is defined in SEMI E89.

5.3 Terminology related to silicon wafer technology is defined in SEMI M1.

5.4 *Other Definitions*

5.4.1 *alpha error* — the error that occurs when a conforming item is incorrectly reported as non-conforming. This is also called Type I error.

5.4.2 *alpha probability,* α — the probability of an alpha error, also called the alpha error rate.

5.4.3 *beta error* — the error that occurs when a non-conforming item is incorrectly reported as conforming. This is also called Type II error.

5.4.4 *beta probability,* β — the probability of a beta error, also called the beta error rate.

5.4.5 *bias,* δ — the difference between the mean value of measurements made on the same object and a true value.

NOTE 1: Bias is illustrated in Related Information 2 (Figure R2-1). However, in many cases the true value is unknown. A value established by reference gauges or a consensus value may be used as a substitute.

[1] International Organization for Standardization: ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland, Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30, Web site: www.iso.ch.

5.4.6 *cumulative distribution function* (*CDF*) — a mathematical formula that describes the probability a measurable event occurs at or below a specific value.

5.4.7 *distribution* — a characterization of the probability of realization for a measurable event over the range of values that the measurements may assume.

5.4.8 *joint probability* — a probability density or cumulative distribution function comprised of two or more random variables.

5.4.9 *lower specification limit* (*LSL*) — value of a characteristic below which a product is said to be nonconforming.

5.4.10 *measurand* — particular attribute of a phenomenon, body, or substance subject to measurement [VIM].

5.4.11 *measurement variability* — differences associated with making multiple measurements on a given measurand under specific conditions.

NOTE 2: Measurement variability (its distribution) is illustrated in Related Information 2 (Figure R2-1). Common (general) estimators of measurement variability are the variance, standard deviation, and variance components. Specific estimators include repeatability and reproducibility.

5.4.12 *probability density function* (*PDF*) — a mathematical formula that specifies the relationship between values that a random variable may assume and their likelihood of occurrence. It is the first derivative of the CDF.

5.4.13 *random variable* — a measurable event occurring such that any value from its distribution is equally likely to take place.

5.4.14 *standard deviation,* σ — the positive square root of the variance.

NOTE 3: The standard deviation of a population may be estimated from experimentally obtained data by the sample standard deviation (*s*):

$$s = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(x_i - \bar{x})^2}$$

where:

n = number of data values,

x_i = value of the i^{th} data point, and

$\bar{x}$ = mean of the data distribution.

5.4.15 *upper specification limit* (*USL*) — value of a characteristic, above which a product is said to be nonconforming.

5.4.16 *variance* — a statistical estimator that quantifies spread around the mean of a PDF.

6 Summary of Practice

6.1 The process distribution for the characteristic of interest is estimated or determined.

6.2 The bias and standard deviation for the characteristic of interest are determined for each measurement instrument to be evaluated or compared.

6.3 The quantities α and β are calculated from the appropriate formula depending on the nature of the specification (LSL only, USL only, or both).

6.4 Costs, based on the applicable business model, are assigned to each of the four possible measurement outcomes.

6.5 The cost components arising from measurement variability are calculated for each measurement instrument being evaluated or compared.

6.6 The costs due to measurement variability are compared to establish the most cost effective measurement solution for the application.

7 Procedure

7.1 Estimate the PDF for the process characteristic to be studied. This can be done using empirical data that represents the process. Although actual data may be used to create a discrete PDF, it is sometimes convenient to use the data to parametrically fit a PDF model (e.g., log normal).

7.2 Unless already known, establish the bias and standard deviation for each measurement gauge to be compared in accordance with SEMI E89.

7.3 In all cases take the measurement influence into account so that it does not broaden the PDF. This may be done by taking repeated measurements at each point in the measurement range and calculating the mean, or by deconvolving the process characteristic PDF, $f(x)$, and the measurement variability CDF, $G(u)$, generally assumed to be a Gaussian (or normal) distribution with arithmetic mean equal to the bias, so that:

$$G(u) = \Phi(u) = \int_{-\infty}^{u} \frac{1}{\sqrt{2\pi\sigma_M}} \exp\left[-\frac{(x-\delta)^2}{2\sigma_M{}^2}\right] \mathrm{d}x \qquad (1)$$

where:

δ = bias,

σ_M = standard deviation of the measurement distribution.

NOTE 4: The quantity σ_M includes the effects of the change in bias over the time interval in which σ_M has been established.

7.4 Calculate α and β as follows (Note 4). Note that the symbols in the equations for α and β have the following meanings:

$f(x)$ = PDF of process characteristic x,

USL = upper specification limit,

LSL = lower specification limit, and

$\Phi(u)$ = Gaussian CDF (see Equation (1) in Section 7.3).

7.4.1 For a characteristic with only a USL, use the following equations to calculate α and β:

$$\alpha = \int_{-\infty}^{USL} \left[1 - \Phi\left(\frac{USL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

$$\beta = \int_{USL}^{\infty} \left[\Phi\left(\frac{USL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

7.4.2 For a characteristic with only an LSL, use the following equations to calculate α and β:

$$\alpha = \int_{LSL}^{\infty} \left[\Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

$$\beta = \int_{-\infty}^{LSL} \left[1 - \Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

7.4.3 For a characteristic with both upper and lower specifications limits, use the following equations to calculate α and β:

$$\alpha = \int_{LSL}^{USL} \left[1 - \Phi\left(\frac{USL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x + \int_{LSL}^{USL} \Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right) f(x)\mathrm{d}x$$

$$\beta = \int_{-\infty}^{LSL} \left[\Phi\left(\frac{USL - x + \delta}{\sigma_M}\right) - \Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x + \int_{USL}^{\infty} \left[\Phi\left(\frac{USL - x + \delta}{\sigma_M}\right) - \Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

NOTE 5: Background information related to the calculation of α and β is given in Related Information 3.

7.5 Use a binary decision model. If measurement-based decisions are labeled as pass or fail and items are inherently conforming or nonconforming, there are only four outcomes:

- pass a conforming item,
- fail a conforming item (α error),
- pass a nonconforming item (β error), and
- fail a nonconforming item.

The probabilities associated with these outcomes are $1-\alpha$, α, β, and $1-\beta$, respectively.

7.6 To define the cost model, assign costs to each of the four decisions above on the basis of the business model used for the manufacturing process as follows:

- c_{pc}: cost of passing a conforming item,
- c_{fc}: cost of failing a conforming item (α error),
- c_{pn}: cost of passing a non-conforming item (β error), and
- c_{fn}: cost of failing a non-conforming item.

7.6.1 Assign zero incremental cost to the two correct outcomes (c_{pc} and c_{fn}).

7.6.2 Assign the incremental costs for the error outcomes, c_{fc} and c_{pn}, on the basis of the business model used for the manufacturing process.

7.7 Calculate the cost due to misclassification resulting from measurement variability based on the assigned incremental costs given in Section 7.6 and the frequency of occurrence of α and β errors as follows:

$$\text{cost} = c_{fc}\alpha + c_{pn}\beta, \qquad (2)$$

using the appropriate equations for α and β as given in Section 7.4, depending on the nature of the specification (LSL only, USL only, or both).

NOTE 6: See Related Information 4 for an example of this calculation.

7.8 If it is desired to include costs for correct as well as incorrect classification, calculate the total cost resulting from measurement variability based on the assigned incremental costs given in Section 7.6 and the frequency of occurrence of α and β errors as follows:

$$\text{cost} = c_{pc}(1-\alpha) + c_{fc}\alpha + c_{pn}\beta + c_{fn}(1-\beta), \qquad (3)$$

using the appropriate equations for α and β as given in Section 7.4, depending on the nature of the specification (LSL only, USL only, or both).

RELATED INFORMATION 1
EXTENSIONS OF THE METHODOLOGY

NOTICE: This related information is not an official part of M56. It was derived from task force deliberations during the development of the document. This related information was approved for publication by full letter ballot procedures on September 3, 2003.

R1-1 Introduction

R1-1.1 In general, when a single characteristic on an item is measured once on a single gauge and 100% sampling is employed, the model will take the form described in this practice.

R1-1.2 If the situation is more complex, the nature of the model will be different. Factors that can affect the nature of the model include the following:

- number of items examined (lot acceptance sampling vs. 100% sampling),
- number of times an item is inspected (single vs. multiple),
- effect of the inspection process on the item (destructive vs. non-destructive),
- number of item characteristics examined for a single decision (one vs. many), and
- cost functions associated with the business decisions (fixed vs. variable).

R1-1.3 In addition, it is possible to have more than one set of cost functions for each type of item that is inspected by the metrology system. Because much of this is context specific, it would be impossible to cover all possible models. Other extensions to the model include relaxation of the assumption of constant variance, the introduction of variability in the bias, and the use of guard banding. The foundation of all these extensions, however, is the use of α and β.

R1-2 Extension to Multiple Gauges

R1-2.1 To extend the model to multiple gauges, one must make the additional assumption that all measuring gauges are measuring the same characteristic.

R1-2.1.1 In addition, define a conforming item as one that all gauges show the measured characteristic to be in specification.

R1-2.1.2 A non-conforming item is taken to be one in which at least one gauge shows the measured characteristic to be outside of specification.

R1-2.2 It is then possible to define a set of α and β error rates for each gauge. Let $\alpha_1, \alpha_2, \ldots, \alpha_n$ be the α values and $\beta_1, \beta_2, \ldots, \beta_n$ be the β values associated with the n different gauges.

R1-2.3 The overall α value, α_T, is calculated from the equation:

$$\alpha_T = \pi - \prod_{i-1}^{n} (1 - \alpha_i)$$

where:

$$\pi = \int_{-\infty}^{USL} f(x)\,dx, \text{ and}$$

$f(x) =$ PDF of the characteristic being measured.

NOTE 1: This equation is based on the probability P that the item is conforming but that one or more gauges give a conforming result:

$\alpha_T = P$[Item is conforming, ≥1 gauges show nonconforming]

$= P$[Item is conforming] –

P[Item is conforming, All gauges show conforming]

R1-2.4 The overall β value, β_T, is calculated from the equation:

$$\beta_T = \prod_{i=1}^{n} \beta_i .$$

NOTE 2: This equation is based on the probability P that the item is nonconforming but that all gauges give a conforming result:

$\beta_T = P$[Item is nonconforming, All gauges show pass]

R1-3 Extension to Multiple Inspections with the Same Metrology System

R1-3.1 Multiple inspection with the same metrology system is a special case of inspection with multiple gauges. If the same measurement system is used to measure the item characteristic repeatedly, one merely lets $\alpha_i = \alpha$ and $\beta_i = \beta$ for all i, as the α and β error rates will not change for the same gauge.

R1-4 Extension to Decisions Based on Multiple Characteristics

R1-4.1 It is also possible to develop a model where a decision is based on more than one characteristic. As with the case of multiple gauges, several assumptions must be made.

R1-4.1.1 The characteristics being measured are independent or an independent combination of their values is used.

R1-4.1.2 All tests are performed before a decision to reject or pass is made.

R1-4.1.3 *F(x)* has been deconvolved from *F·G*.

R1-4.1.4 A conforming item is defined as one in which all measured characteristics are shown to be in specification.

R1-4.1.5 A non-conforming item is taken to be one in which at least one characteristic is outside of specification.

R1-4.2 It is then possible to define a set of α and β errors for each gauge. Let α_1, α_2, …, α_n be the α values and β_1, β_2, …, β_n be the β values associated with the n different characteristics.

R1-4.3 The overall α value, α_T, is calculated from the equation:

$$\alpha_T = \prod_{i=1}^{n} \pi_i - \prod_{i=1}^{n} (1-\alpha_i)$$

where:

$$\pi_i = \int_{-\infty}^{USL} f_i(x)\,dx, \text{ and}$$

$f_i(x)$ = PDF of the characteristic i.

NOTE 3: This equation is based on the probability P that all characteristics conform, but that at least one test failed:

$\alpha_T = P$[All characteristics conform, At least one test failed]

$= P$[All characteristics conform] –

P[All characteristics conform, All tests passed]

R1-4.4 The overall β value, β_T, is calculated from the equation:

$$\beta_T = \prod_{i=1}^{n} p_i - \prod_{i=1}^{n} (1-\alpha_i)$$

where:

p_i = proportion of observations within specification for characteristic i.

NOTE 4: This equation is based on the probability P that one or more characteristics are nonconforming but that all tests passed:

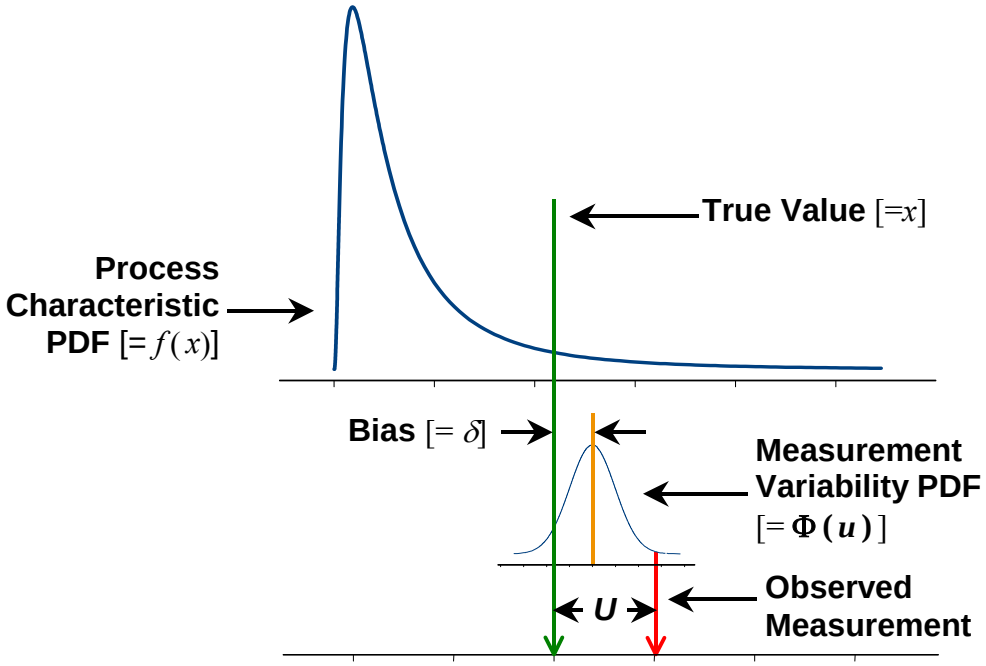
$\beta_T = P$[≥1 characteristic nonconforming, All tests passed]

$= P$[All pass] –

P[All characteristics conform, All tests passed]

RELATED INFORMATION 2
PICTORIAL REPRESENTATION OF PROCESS DISTRIBUTION AND MEASUREMENT VARIABILITY AND BIAS

NOTICE: This related information is not an official part of SEMI M56. It was derived from task force deliberations during the development of the document. This related information was approved for publication by full letter ballot procedures on September 3, 2003.



NOTE: The observed measurement is displaced from the true value, x, by an amount U with a frequency of occurrence for each value of U given by the measurement variability PDF.

Figure R2-1
Relationship of Process Characteristic PDF, Measurement Variability PDF, True Value, Bias, and an Observed Measurement

RELATED INFORMATION 3
BACKGROUND OF THE METHODOLOGY

NOTICE: This related information is not an official part of SEMI M56. It was derived from task force deliberations during the development of the document. This related information was approved for publication by full letter ballot procedures on September 3, 2003.

R3-1 The model in this practice is used to assign probabilities (risks) to specification-related events. In general, there are two probabilities that are of interest. The first is the probability of getting a measurement outside of the specification range for a conforming item. This is often called the producer's risk because conforming product would be needlessly rejected in this situation. The second probability is that of getting a measurement within specifications for a non-conforming item. Consumer's risk is the term applied to this probability, since there is a chance of non-conforming product being accepted.

R3-1.1 For the purposes of this standard, the event of rejecting an item whose true value lies inside of the specification limits is considered a Type I error with error rate (probability) α.

R3-1.2 The event of accepting an item whose true value lies outside of the specification limits is considered a Type II error with error rate (probability) β.

R3-1.3 One of the difficulties in formulating the statistical model is that there are two or more distributions involved, possibly in an interdependent fashion. Given a true underlying (fixed) value, x, a single measurement of that value produces the observation $Y = x + U$, where U is a random and unobservable value attributable to measurement variability. If one takes n measurements of the same value x, i.e., $Y_i = x + U_i$, where $i = 1,..., n$, Y and U are treated as random variables from the observation and measurement variability distributions, respectively. The situation is further complicated if several x values are measured. In this situation, the x values come from the process (or characteristic) distribution X such that $Y_{ij} = X_j + U_{ij}$, where $i = 1,..., n$ and $j = 1,..., m$. The relationship between X and U is known as a convolution. Additional distributions may be involved if one assumes that certain characteristics of the measurement process do not remain constant over the measurement range. For example, one may assume that bias is a function of the measured value. To model this a third distribution would be needed, but the scope of this practice is limited to the use of only two distributions (characteristic and measurement variability).

R3-2 The symbols in the equations derived for α and β have the following meanings:

X = random value attributable to the process characteristic,

U = random and unobservable value attributable to measurement variability,

$f(x)$ = process characteristic PDF,

$G(u)$ = measurement variability CDF,

USL = upper specification limit,

LSL = lower specification limit, and

$\Phi(u)$ = Gaussian CDF.

R3-3 The process characteristic PDF and measurement variability CDF are assumed to be independent of each other.

R3-4 For a process characteristic with only a USL:

R3-4.1 Define α as a joint probability:

$$\alpha = P\left[X \le USL, X + U > USL\right] = \int_{-\infty}^{USL} \left[1 - G\left(USL - x\right)\right] f\left(x\right) dx$$

R3-4.2 Similarly, define β as:

$$\beta = P\left[X > USL, X + U \le USL\right] = \int_{USL}^{\infty} G\left(USL - x\right) f\left(x\right) dx$$

R3-5 For a process characteristic with only an LSL, the formulae for α and β are:

$$\alpha = \int_{LSL}^{\infty} G\left(LSL - x\right) f\left(x\right) dx$$

$$\beta = \int_{-\infty}^{LSL} \left[1 - G\left(LSL - x\right)\right] f\left(x\right) dx$$

R3-6 For a process characteristic with both upper and lower specifications limits, the formulae for α and β are:

$$\alpha = \int_{LSL}^{USL} \left[1 - G(USL - x)\right] f(x)\,dx + \int_{LSL}^{USL} G(LSL - x) f(x)\,dx$$

$$\beta = \int_{-\infty}^{LSL} \left[G(USL - x) - G(LSL - x)\right] f(x)\,dx + \int_{USL}^{\infty} \left[G(USL - x) - G(LSL - x)\right] f(x)\,dx$$

R3-7 To use the above functions in practice, additional assumptions must be made:

R3-7.1 Equipment bias is treated as constant throughout the measurement range. This is needed to avoid a third function in the integral.

R3-7.2 In general, the distribution of the measurement variability is assumed Gaussian (or normal), with mean, μ, and variance, σ^2. For measurement gauges, $\mu = \delta$, the bias, and $\sigma^2 = \sigma_M{}^2$, the measurement system variance.

R3-7.3 The distribution of the parameter of interest has been characterized. This may be done by taking multiple measurements at each point in the measurement range and averaging, or by deconvolving $F(x)$ and $G(u)$.

R3-8 Given the assumptions above about the measurement system, the following relationships apply:

R3-8.1 When only a USL is given, the formulae for α and β are:

$$\alpha = \int_{-\infty}^{USL} \left[1 - \Phi\left(\frac{USL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

$$\beta = \int_{USL}^{\infty} \left[\Phi\left(\frac{USL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

R3-8.2 For a characteristic with only an LSL, use the following equations to calculate α and β:

$$\alpha = \int_{LSL}^{\infty} \left[\Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

$$\beta = \int_{-\infty}^{LSL} \left[1 - \Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

R3-8.3 For a characteristic with both upper and lower specifications limits, use the following equations to calculate α and β:

$$\alpha = \int_{LSL}^{USL} \left[1 - \Phi\left(\frac{USL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x + \int_{LSL}^{USL} \Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right) f(x)\mathrm{d}x$$

$$\beta = \int_{-\infty}^{LSL} \left[\Phi\left(\frac{USL - x + \delta}{\sigma_M}\right) - \Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x + \int_{USL}^{\infty} \left[\Phi\left(\frac{USL - x + \delta}{\sigma_M}\right) - \Phi\left(\frac{LSL - x + \delta}{\sigma_M}\right)\right] f(x)\mathrm{d}x$$

R3.9 The equations used in Section 7.4 are those in Sections R3-8.1 through R3-8.3.

RELATED INFORMATION 4
EXAMPLE OF CALCULATION ACCORDING TO PROCEDURE

NOTICE: This related information is not an official part of SEMI M56. It was derived from task force deliberations during the development of the document. This related information was approved for publication by full letter ballot procedures on September 3, 2003.

R4-1 This example relates to the calculation of the cost components due to misclassification caused by measurement variability in flatness measurement during wafer manufacturing. The following premises are made:

R4-1.1 A wafer manufacturer must supply a customer with a specific number of wafers that conform to a site flatness specification of 0.13 μm, SFQR as defined in SEMI M1.

R4-1.2 Most wafers produced do conform to the specification. Due to variability in the manufacturing process, some wafers do not conform to the specification.

R4-1.3 The flatness measurement step is near the end of the wafer manufacturing process. It follows surface polishing and precedes final cleaning, surface inspection, and packaging.

R4-1.4 All of the wafers are measured for site flatness. The measurement data is used to determine if wafers are passed for further processing and shipment or if they are failed and scrapped without further processing. This example premises no rework for failed wafers.

R4-1.5 The customer is always able to detect a non-conforming wafer. When a non-conforming wafer is detected, it is returned to the manufacturer and a replacement wafer must be supplied to satisfy the specified order quantity.

R4-2 The following steps follow the procedures outlined in Section 6.

R4-2.1 *Estimation of Process Distribution* — A total of 17,698 observations was made on flatness measurements. An empirical estimate of the flatness CDF was calculated from these data and is shown in the column of Table R4-1 labeled $F(x)$.

R4.2.2 *Estimation of Bias and Variance for Each Gauge Compared* — Two gauges are available. Gauge A has zero bias and a measurement variability of $\sigma_A = 0.00433$, which results in a P/T ratio of 10%, calculated in accordance with SEMI M27 for a single sided distribution. Gauge B also has zero bias, but has a measurement variability of $\sigma_B = 0.00867$ or a P/T ratio of 20%. Let the distribution of the measurement variability for the two gauges be normally distributed with a mean of zero and standard deviations given above.

R4-2.3 *Calculation of α and β* — To calculate α and β, one needs to estimate $f(x)$ and $\Phi(z)$, where

$$z = (USL - x)/\sigma_M.$$

The values in the column labeled $f(x)$ are derived by dividing the value in the count column by the total number of observations. $\sigma(z)$ is calculated from the normal CDF using the numbers in the first column as x, 0.13 as the USL, and either $\sigma_A = 0.00433$ or $\sigma_B = 0.00867$ for σ_M, depending on whether Gauge A or Gauge B is used. To calculate α, for each row multiply $f(x)$ by $1 - \Phi(z)$ and sum over all rows at or below the specification limit. To calculate β, for each row multiply $f(x)$ by $\Phi(z)$ and sum over all rows above the USL. The calculations for α and β for the two P/T ratios of 10% and 20% can also be found in Table R4-1.

R4-2.4 *Decision Model* — One of four situations may occur depending on the true flatness of the wafer, conforming or nonconforming, and the decision made based on the output from the metrology equipment, pass or fail. Two correspond to correct actions: passing a conforming item and failing a nonconforming item. Zero incremental cost is associated with correct classification. The two situations associated with misclassification, passing a nonconforming item and failing a conforming item, have actual incremental costs.

R4-2.5 *Estimation of Costs* — For purposes of illustration, let the cost of failing a conforming wafer (c_{fc}) be \$300 and the cost of passing a nonconforming (c_{pn}) wafer be \$220. The cost of ownership due to measurement variability and bias can then be calculated as:

$$\text{cost} = c_{fc}P(\text{fail,conforming}) + c_{pn}P(\text{pass, nonconforming})$$
$$= c_{fc}\alpha + c_{pn}\beta$$

R4-2.6 *Calculation of Costs* — The cost components due to measurement variability for Gauge A and Gauge B are:

$$\text{cost}_A = c_{fc}\alpha_A + c_{pn}\beta_A$$
$$=$$
$$(300)(0.01042530) + (220)(0.00011698) = 3.1533$$
$$\text{cost}_B = c_{fc}\alpha_B + c_{pn}\beta_B$$
$$=$$
$$(300)(0.01428055) + (220)(0.00145950) = 4.6053$$

The cost difference in operating Gauge A rather than Gauge B in this example is, on average, $1.45 per wafer.

Table R4-1 Empirical Distribution of SFQR Measurements and Calculations of α and β for Flatness Measuring Gauges with P/T = 10% and P/T = 20%

SFQR (μm)	Count	$f(x)$ (PDF)	$F(x)$ (CDF)	P/T = 10% z	P/T = 10% $\Phi(z)$	P/T = 10% $f(x)(1-\Phi(z))$	P/T = 10% $f(x)\Phi(z)$	P/T = 20% z	P/T = 20% $\Phi(z)$	P/T = 20% $f(x)(1-\Phi(z))$	P/T = 20% $f(x)\Phi(z)$
0.01	0	0.0000	0.0000	27.6923	1.0000E+00	0.0000E+00	0.0000E+00	13.8462	1.0000E+00	0.0000E+00	0.0000E+00
0.02	89	0.0050	0.0050	25.3846	1.0000E+00	0.0000E+00	5.0288E-03	12.6923	1.0000E+00	0.0000E+00	5.0288E-03
0.03	772	0.0436	0.0486	23.0769	1.0000E+00	0.0000E+00	4.3621E-02	11.5385	1.0000E+00	0.0000E+00	4.3621E-02
0.04	1,703	0.0962	0.1449	20.7692	1.0000E+00	0.0000E+00	9.6226E-02	10.3846	1.0000E+00	0.0000E+00	9.6226E-02
0.05	2,389	0.1350	0.2799	18.4615	1.0000E+00	0.0000E+00	1.3499E-01	9.2308	1.0000E+00	0.0000E+00	1.3499E-01
0.06	2,752	0.1555	0.4354	16.1538	1.0000E+00	0.0000E+00	1.5550E-01	8.0769	1.0000E+00	5.1791E-17	1.5550E-01
0.07	2,556	0.1444	0.5798	13.8462	1.0000E+00	0.0000E+00	1.4442E-01	6.9231	1.0000E+00	3.2112E-13	1.4442E-01
0.08	2,298	0.1298	0.7096	11.5385	1.0000E+00	0.0000E+00	1.2985E-01	5.7692	1.0000E+00	5.1858E-10	1.2985E-01
0.09	1,687	0.0953	0.8049	9.2308	1.0000E+00	0.0000E+00	9.5322E-02	4.6154	1.0000E+00	1.8720E-07	9.5321E-02
0.10	1,189	0.0672	0.8721	6.9231	1.0000E+00	1.4938E-13	6.7183E-02	3.4615	9.9973E-01	1.8045E-05	6.7165E-02
0.11	789	0.0446	0.9167	4.6154	1.0000E+00	8.7554E-08	4.4581E-02	2.3077	9.8949E-01	4.6846E-04	4.4113E-02
0.12	524	0.0296	0.9463	2.3077	9.8949E-01	3.1112E-04	2.9297E-02	1.1538	8.7572E-01	3.6797E-03	2.5928E-02
0.13	358	0.0202	0.9665	0.0000	5.0000E-01	1.0114E-02	1.0114E-02	0.0000	5.0000E-01	1.0114E-02	1.0114E-02
0.14	197	0.0111	0.9777	-2.3077	1.0508E-02	1.1014E-02	1.1697E-04	-1.1538	1.2428E-01	9.7478E-03	1.3834E-03
0.15	126	0.0071	0.9848	-4.6154	1.9639E-06	7.1194E-03	1.3982E-08	-2.3077	1.0508E-02	7.0446E-03	7.4812E-05
0.16	87	0.0049	0.9897	-6.9231	2.2234E-12	4.9158E-03	1.0930E-14	-3.4615	2.6860E-04	4.9145E-03	1.3204E-06
0.17	67	0.0038	0.9935	-9.2308	0.0000E+00	3.7857E-03	0.0000E+00	-4.6154	1.9639E-06	3.7857E-03	7.4348E-09
0.18	52	0.0029	0.9964	-11.5385	0.0000E+00	2.9382E-03	0.0000E+00	-5.7692	3.9938E-09	2.9382E-03	1.1735E-11
0.19	38	0.0021	0.9986	-13.8462	0.0000E+00	2.1471E-03	0.0000E+00	-6.9231	2.2234E-12	2.1471E-03	4.7740E-15
0.20	25	0.0014	1.0000	-16.1538	0.0000E+00	1.4126E-03	0.0000E+00	-8.0769	3.3307E-16	1.4126E-03	4.7049E-19
Sum =	17,698	1.0000									

USL = 0.13 μm

P/T = $3\sigma_M$/USL

For P/T = 10%, $\sigma_M = \sigma_A$ = 0.10 x 0.13/3 = 0.00433

α_A = 1.0425E-02

β_A = 1.1698E-04

For P/T = 20%, $\sigma_M = \sigma_B$ = 0.20 x 0.13/3 = 0.00867

α_B = 1.4281E-02

β_B = 1.4595E-03

SEMI M57-0705
GUIDE FOR SPECIFYING SILICON ANNEALED WAFERS

This guide was technically approved by the global Silicon Wafer Committee. This edition was approved for publication by the global Audits and Reviews Subcommittee on April 7, 2005. It was available at www.semi.org in June 2005 and on CD-ROM in July 2005. Originally published July 2004; previously published March 2005.

1 Purpose

1.1 A number of device manufacturers utilize silicon annealed wafers to gain improved device characteristics. This guide provides information for developing specifications for silicon annealed wafers used to fabricate semiconductor devices and integrated circuits.

2 Scope

2.1 This guide covers dimensional, electrical, chemical, and structural properties of silicon annealed wafers for 180 nm, 130 nm, and 90 nm device technology generations.

2.2 Based on the guidance herein, the user of the guide can generate specifications for silicon annealed wafers.

2.3 One of the reasons for using annealed wafers is to allow a reduction in the crystal originated particles (COP) near the top surface region of the wafer. Currently, only the COP surface density can be estimated.

2.4 The width of the denuded zone (DZ) free of bulk micro defects (BMD) is also an important parameter. However, there is no standardized method to evaluate this characteristic at the present time.

2.5 The complete EDI Code List for items in the Order Form appropriate to silicon wafers, including annealed wafers, can be found in SEMI M18.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M45 — Provisional Specification for 300 mm Wafer Shipping System

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI M58 — Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF391 — Test Methods for Minority-Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF951 — Test Method for Determination if Radial Interstitial Oxygen Variation in Silicon Wafers

SEMI MF1239 — Test Methods for Oxygen Precipitation Characteristics of Silicon Wafers by Measurement of Interstitial Oxygen Reduction

SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Total Thickness Variation on Silicon Wafers by Automated Noncontact Scanning

SEMI MF1535 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, Potassium, and Iron on Silicon and Epi Substrates by Secondary Ion Mass Spectroscopy

SEMI MF1726 — Practice for Analysis of Crystallographic Perfection of Silicon Wafers

SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers

SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon

SEMI T3 — Specification for Wafer Box Labels

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

3.2 *JIS Standards*[1]

H 0609 — Test Methods of Crystalline Defects in Silicon by Preferential Etch Techniques

H 0614 — Visual Inspection for Silicon Wafers with Specular Surfaces

Z 8741 — Specular Glossiness–Method of Measurement

3.3 *DIN Standards*[2]

50434 — Determination of Crystal Defects in Monocrystalline Silicon Using Etching Techniques on {111} and {100} Surfaces

50443/1 — Recognition of Defects and Inhomogenities in Semiconductor Single Crystals by X-Ray Topography: Silicon

3.4 *ISO Standard*[3]

ISO 14706 — Surface Chemical Analysis – Determination of Surface Elemental Contamination on Silicon Wafers by Total Reflection X-Ray Fluorescence Spectroscopy (TXRF) on silicon wafers by total reflection X-ray fluorescence spectroscopy (TXRF)

3.5 *ANSI Standards*[4]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

ANSI/EIA 556-B — Outer Shipping Container Standard

3.6 *ASTM Standards*[5]

D 523 — Standard Test Method for Specular Gloss

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

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1 Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp.

2 Deutches Institut für Normung e.V., standards are available in both English and German editions from Beuth Verlag GmbH, Burggrafenstrasse 6, 10787 Berlin, Germany, Telephone: 49.30.2601-0, Fax: 49.30.2601.1263, Website: www.beuth.de

3 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch.

4 American National Standards Institute, New York Office: 25 West 43rd Street, New York, NY 10036, USA. Telephone: 212.642.4900, Fax: 212.398.0023, Website: www.ansi.org

5 ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555, Website: www.astm.org

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Most general terms, acronyms, and symbols relating to silicon technology are defined in SEMI M59.

4.2 Terms specific to commonly-used annealed wafers are defined as follows:

4.2.1 *annealed wafer* — wafer that has a defect (COP) free zone near the surface resulting from high temperature annealing under a neutral or reducing atmosphere.

4.2.2 *argon annealed wafer* — annealed wafer produced under argon atmosphere.

4.2.3 *hydrogen annealed wafer* — annealed wafer produced under hydrogen atmosphere.

5 Ordering Information

5.1 Purchase orders for silicon annealed wafers furnished to this guide shall include the appropriate order entry information from Table 1, Polished Wafer Specification Format for Order Entry, in SEMI M1. All information in Part 1, General Information, and the following items from Part 2, Polished Wafer or Substrate, shall be included:

- 2-1.1 Growth Method
- 2-1.3 Crystal Orientation
- 2-1.4 Conductivity Type
- 2-1.5 Dopant
- 2-1.6 Nominal Edge Exclusion
- 2-1.7 Co-dopant in Crystal
- 2-1.8 Wafer Surface Orientation
- 2-2.1 Resistivity (Center point)
- 2-2.2 Radial Resistivity Variation
- 2-3.1 Oxygen Concentration/Calibration Factor
- 2-3.2 Radial Oxygen Variation
- 2-3.3 Carbon Concentration (Background)
- 2-4.3 Lineage
- 2-4.4 Twin Boundary
- 2-4.5 Swirl
- 2-5.1 Wafer ID Marking
- 2-5.2 Front Surface Thin Films
- 2-5.4 Extrinsic Gettering
- 2-5.5 Backseal
- 2-6.1 Diameter
- 2-6.6 Edge Profile
- 2-6.7 Thickness
- 2-6.8 Total Thickness Variation (TTV)
- 2-9.1 Edge Chips (Back Surface)
- 2-9.8 Brightness (Gloss) (Back Surface)
- 2-9.9 Scratches (Macro) (Back Surface)

Table 1 Silicon Wafer Specification Format for Order Entry, Part 5 Annealed Wafers

		ITEM	SPECIFICATION	MEASUREMENT METHOD
5-1. ANNEALING CONDITIONS				
	5-1.1	Annealing Atmosphere	[ ]Hydrogen; [ ]Argon; [ ]Other: (specify)_____	
5-2. POST-ANNEAL WAFER PREPARATION CHARACTERISTIC				
	5-2.1	Edge Surface Condition	[ ]Ground; [ ]Etched; [ ]Polished[A]	
5-3. POST-ANNEAL DIMENSIONAL CHARACTERISTICS				
	5-3.1	Warp	[ ] µm; max.	[ ]SEMI MF657; [ ]SEMI MF1390; [ ]Other: (specify)_____
	5-3.2	Flatness, Site	Acronym[#2]: [ ] [ ] [ ] [ ] Value: Not greater than [ ]µm Site Size ___ mm × ___ mm % Usable Area_____ [ ]Include partial sites; [ ]Do not include partial sites Offset: x = [ ] mm, y = [ ] mm	[ ]SEMI MF1530; [ ]Other: (specify)_____
5-4. POST-ANNEAL FRONT SURFACE CHEMISTRY				
	5-4.1	Surface Metal Contamination		
	5-4.1.1	Sodium	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	5-4.1.2	Aluminum	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]Other: (specify)_____
	5-4.1.3	Potassium	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.1.4	Chromium	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.1.5	Iron	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.1.6	Nickel	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.1.7	Copper	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____