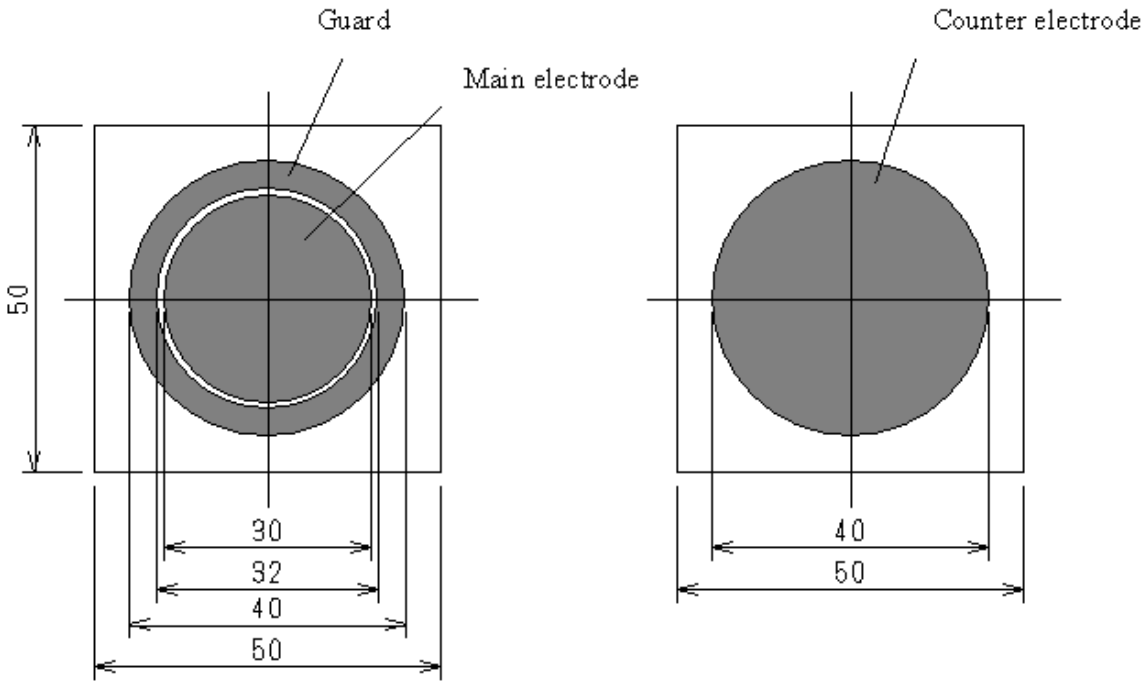

Figure 3
Electrodes for Measurement of Volume Resistivity

8.6.2 *Surface Resistivity*

(1) *Equipment* — Use the same equipment as in Section 8.6.1.

(2) *Material* — Use the same material as in Section 8.6.1.

(3) *Measurement* — To measure Surface Resistance in normal conditions, use the same method as described in Section 8.6.1.

(4) *Calculation* — Use the equation below.

$$\rho s = Rs \times \frac{P}{D_0}(\Omega)$$

Where ρs is Surface Resistance, Rs is resistance value, P is the actual circumference length of the guarded electrode, and D_0 is the distance between the main electrode and the guard electrode.

8.6.3 *Insulation Resistance*

(1) Equipment

(a) *Resistance Meter* — Use the same equipment as in Section 8.6.2.

(b) *Direct Current* — Use a stabilized direct power supply that can apply a stable 100 ± 5V to the sample.

(c) *Environmental Test Chamber* — Use an oven with terminal connectors on the outside which can maintain humidity at 30–85 ± 5°C and 60–90 ± 5% R.H.

(2) *Material* — Using the TCP polyimide adhesive tape as received from the vendor, laminate and cure it according to the method described in Section 8.2.

(3) Measurement

(a) *Normal Condition* — Apply direct voltage of 100 ± 5V to the sample and maintain for 1 minute. Keeping the voltage applied, measure the insulation resistance.

(b) *High Temperature, High Humidity* — After keeping the sample under 85 ± 5°C and 85 ± 5% R.H. for 24 ± 4 hours,

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perform the same measurement as in Section 8.6.3, (3)(a).

(c) *High Temperature, High Humidity, Under Bias* — After keeping the sample under 85 ± 5°C and 85 ± 5% R.H. for 24 ± 4 hours, apply direct voltage of 100 ± 5V and perform the same measurement as in Section 8.6.3, (3)(a). After this, follow the methods and conditions defined by the receiving parties.

8.6.4 *Inter-Layer Voltage Resistance*

(1) *Equipment* — Use the equipment which conforms to JIS C-2110, Section 6.2 or similar.

(2) *Material* — Use the same material prepared by the same method as in Section 8.6.1, (2).

(3) *Measurement* — To measure in normal conditions, perform the following steps: Using DC voltage, or a sine wave AC with 50 or 60 Hz frequency, apply 500V to the sample. Increase the applied voltage up to the defined voltage over 5 seconds, maintain it for 1 minute and determine whether there has been any mechanical damage, flash-over, spark-over, insulation breakdown or other abnormality.

8.6.5 *Relative Permittivity and Dielectric Dissipation Factor*

(1) Equipment

(a) *Power Source (see Figure 4 - S)* — Use a source which can emit a frequency of 1 MHz, has a sine wave with less than 5% distortion factor, can give a stable flow of the define voltage to the sample, and have electro-static and magnetic shielding to prevent direct coupling between the power source and bridge.

(b) *Shielded Transformer (see Figure 4 - T_1)* — Use a transformer with which the power source internal impedance and the bridge impedance can be adjusted, and one where the winding on the bridge inside the transformer is shielded with a grounded conductor.

(c) *Ratio Arm (see Figure 4 - T_2)* — Use a ratio arm with a winding ratio of 1:1 (tolerance of less than 0.2%). Make a non-inductive connection of the primary winding and secondary winding of a transformer with as little leakage inductance and winding resistance. Ground the connection point as shown in Figure 4 - e, and connect the other 2 terminals to l and r to make it unbalanced.

(d) *Variable Capacitor (see Figure 4 - Cs_1, Cs_2)* — Use two air capacitors with guards that have a capacity of approximately 200 pF, one being the standard capacitor Cs_1 and the other being the measuring capacitor Cs_2, and insert parallel with the sample Cx.

(e) *Conductance Shifter (see Figure 4 - g)* — Insert a resistor with a constant conductance in between m and d in Figure 4, where the resistance between l and m can be changed between 100–0 Ω, and the resistance between m and r can be changed between 100–200 Ω.

(f) *Balance Detector (see Figure 4 - g)* — Use a balance detector which responds only to the power source voltage base plate used in the bridge.

(2) *Material* — Prepare the samples according to the method described in Section 8.6.1, (3). Use Figure 3 for the shape of the electrode.

(3) *Measurement* — Use the following to measure under normal conditions: Measure the thickness of the samples in units of 1 μm, and measure the inner diameter of the gap in the circular upper electrode in units of 0.05 mm. Also, confirm that the circular gap between the main electrode and the guard electrode is 1 ± 0.1 mm. Connect the sample at position Cx, and by adjusting the measuring capacitor Cs_2 and the conductance shifter, with the bridge balanced, measure the standard capacitor Cs_1 value and the measuring capacitor Cs_2 value, the resistance value between conductance shifter m and d, and the resistance value between m and r. The measuring frequency is 1 MHz.

(4) *Calculation* — Use the equation below.

(a) Relative Permittivity

$$\varepsilon r = \frac{Cx}{C_0}(\Omega)$$

Where Cx is the difference in the capacitance values of standard capacitor Cs_1 and measuring capacitor Cs_2 (when the

bridge is balanced, and C_0 is the electrostatic capacity where εr = 1 calculated from the main electrode area and sample thickness according to the following formula):

$$C_0 = \frac{r^2}{3.6t}$$

(b) Dielectric Dissipation Factor

$$\tan\delta = \frac{Gx}{2\pi fCx}$$

$$Gx = G \times \frac{S}{100}$$

Where Gx is the sample conductance, G is the conductance between m and d, S is the resistance value between m and r, S/100 is the resistance factor, f is the measuring frequency, and π is pi.

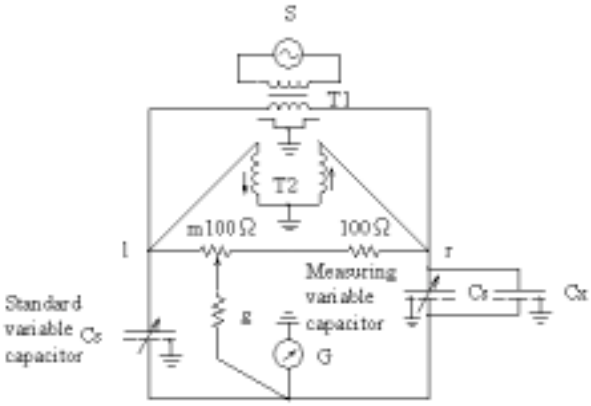

Figure 4
Measurement Circuit for Relative Permittivity and Dielectric Dissipation Factor

8.7 *Other Tests*

8.7.1 *Heat Resistance*

(1) Equipment

(a) *Solder* — Use Standard H60A or H63A under JIS Z-3282.

(b) *Solder Bath* — A vessel with a depth of more than 50 mm to hold the solder at between 200–300°C and can be adjusted ± 3°C.

(1) *Material* — Using the TCP polyimide adhesive tape as received from the vendor, laminate and cure it according to the method described in Section 8.2. Cut into 25 mm squares for samples.

(2) *Preparation* — Keep in 105 ± 5°C oven for 1 hour.

(3) *Test* — After preparation, quickly place in 260 ± 5°C solder bath and let float for 5^{+1}_{-0} seconds. Perform visual check for swelling.

8.7.2 *Water Absorption Test*

(1) Equipment

(a) *Scale* — Use a scale that can measure in 1 mg units.

(b) *Vessel* — Use a vessel in which the samples can be totally immersed.

(c) *Dessicator* — Use a dessicator which allows samples heated to 80°C to cool off.

(1) *Material* — Using the TCP polyimide adhesive tape as received from the vendor, laminate and cure it according to the method described in Section 8.2. In addition, remove all copper foil by etching, and dry for 30 minutes at 80 ± 5°C. Cool in the dessicator, and use samples cut into length 500 ± 5 mm, and width 20 ± 1 mm. Depending on the shape of the vessel to be used for immersion, it is feasible to several pieces of a suitable length.

(2) *Test* — Weigh the sample in increments of 1 mg. Place sample in 23 ± 2°C distilled water. After 24 ± 1 hours, wipe off water and measure sample again in increments of 1 mg.

(3) *Calculation* — Use the following formula:

$$\frac{W_2 - W_1}{W_2} \times 100 \qquad (\%)$$

Where W_1 and W_2 are the weight before and after immersion respectively.

8.7.3 *Heat Shrinkage* — Use the standard value of the base film and the various values for measuring conditions.

(1) *Equipment* — Use a measuring device with optical equipment which can read with at least 5/100,000 (0.005%) precision.

(2) *Material* — Mark three places along the width on a sample with size larger than 50 mm square.

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(3) *Preparation* — Place for more than 1 hour in a managed environment of room temperature ± 2°C, ± 5% R.H.

(4) *Measuring Method Before Heating* — Measure the distance between the marks with the equipment (1) on a sample that has been prepared according to (3) above.

(5) *Heating* — Keep the samples in an oven at 200 ± 3°C for more than an hour, making sure that it is not effected from the outside.

(6) *After-Processing* — Leave sample for more than 1 hour in the conditions described in (3) above.

(7) *Measuring Method After Heating* — Use the same method as (4) above.

(8) *Calculation* — Use the following formula, where L_1 is the dimension from (4), and L_2 is the dimension from (7):

$$\frac{L_1 - L_2}{L_1} \times 100 \qquad (\%)$$

8.7.4 *Coefficient of Thermal Expansion* — Use the standard value of the base film and the various values for measuring conditions.

(1) *Equipment* — Use TMA equipment.

(2) *Material* — Prepare sample with width of 3 mm and length of more than 15 mm.

(3) *Preparation* — To remove the effects of thermal shrinkage and moisture, heat at more than 300°C for 30 minutes.

(4) *Measuring Method* — With a sample that has been prepared according to (3) above, measure the stretching in the sample on a TMA, in the range between room temperature and 300°C, raising the temperature at less than 20°C/min.

(5) *Calculation* — Use the following formula, reading a gradient from an arbitrary scope, within the area between room temperature and 200°C (i.e., 50–200°C, 100–200°C):

$$\frac{L_1 - L_0}{L_0 (T_1 - T_0)} \times 100^{6} \qquad (ppm)$$

Where T_0 and T_1 are the temperatures in the area for Linear Expansion, L_0 is the length of the sample at T_0 (°C) and L_1 is the length of the sample at T_1 (°C).

8.7.5 *Tensile Strength, Elongation* — Use the standard value of the base film and the various values for measuring conditions.

(1) *Equipment* — Use a pull strength meter and recorder.

(2) *Material* — Use samples with a width of more than 10 mm and length of approximately 200 mm. The samples should be 3 pieces taken from the beginning, middle and end of the roll.

(3) *Measuring Method* — After measuring the width of the sample, fix it in the pull strength meter. Use a clamping distance of approximately 100 mm to test pull strength. Measure the pull load and stretch at point of breakage.

(4) *Calculation* — After measuring the pull strength and elasticity of each sample, calculate the average of each.

8.7.6 *Flammability*

(1) Equipment

(a) Sample box or draft chamber which can maintain calm conditions.

(b) Test stand and clamp.

(c) Bunsen burner with pipe length of approximately 100 mm, aperture diameter of 9.5 ± 0.5 mm, using methane gas or natural gas with a heat generation volume of approximately 37 MJ/m^3.

(d) Stop-watch or timer.

(e) Sheet of absorbent cotton 50 mm square with a maximum natural thickness of 6.4 mm.

(f) A dessicator with dehydrated hydrated calcium.

(g) A test oven which can maintain a temperature of 23 ± 2°C and R.H. of 50 ± 5%.

(h) A test oven which can maintain a temperature of 70 ± 1°C.

(i) A pole with a diameter of 13 ± 5 mm.

(2) *Material* — Using the TCP polyimide adhesive tape as received from the vendor, laminate and cure it according to the method described in Section 8.2. In addition, remove all copper foil by etching, and dry for 30 minutes at 80 ± 5°C. As shown in Figure 5,

use a sample with a length of 200 mm and width of 50 mm, and mark a line in the TD direction at 125 mm from the bottom. With the mark line facing outward, wrap the sample around the pole and hold in place with tape within 76 mm about the mark line. Remove the pole to leave a tube of the sample. Prepare 2 groups of 5 pieces each.

(3) *Preparation* — Leave one group of samples in normal condition for 48 hours. Heat the other group at 70 ± 1°C for 168 hours, place them in the dessicator with dehydrated hydrated calcium and keep for more than 4 hours at 23°C.

(4) *Test* — Perform the following test on the two groups of samples prepared as described in Section 8.7.6, (3) above:

(a) As shown in Figure 6, fix the sample perpendicular in the ring stand with the clamps, with the tip of the burner 10 mm below the edge of the sample, and the absorbent cotton placed horizontal at 300 mm below the edge.

(b) Light the burner away from the sample, and adjust to a blue flame of 20 ± 1 mm long. Keeping the length at 20 ± 1 mm, make sure there is no yellow flame at the tip.

(c) Apply the flame to the center of the edge of the sample for 3 seconds. Then remove the flame to more than 150 mm away, and record the flaming time. When the flame burns out, apply the flame to the edge of the sample for 3 seconds and pull away again. Measure the flaming time it takes to reach the clamp as well as the glowing time. Also, record whether the absorbent cotton has caught fire or not. When there are molten particles or burning material drippings from the sample, it is acceptable to tip the burner 45° and move the flame from the bottom edge to avoid material dripping on the burner. In this case, the distance from the bottom edge of the sample to the tip of the burner should still be 10 mm.

(5) Items to Record

(a) Flaming time after the first and second application.

(b) Sum of flaming and glowing time after second application.

(c) Flaming or glowing up to the clamp or mark line.

(d) Existence of dripping material which caused the absorbent cotton to burn.

8.8 *Test for External Defects*

8.8.1 *MD Curl*

(1) *Equipment* — Use a scale that measures at least 1 mm increments.

(2) *Material* — Cut a section of more than 30 cm, but less than 100 cm in length of TCP polyimide adhesive tape as received.

(3) Measurement — As shown in Figure 7, remove the cover film, place on a flat surface for more than 12 hours and measure the highest point on the tape from the flat surface in the MD direction.

8.8.2 *TD Curl*

(1) Equipment

(a) A scale that measures at least 1 mm increments.

(b) A square block with a base with a length of more than 15 cm and width of 2 cm, and a weight of more than 500 g.

(2) *Material* — Cut a section of more than 15 cm, but less than 30 cm in length of TCP polyimide adhesive tape as received.

(3) Measurement

(a) Remove the cover film and place on a flat surface for more than 12 hours.

(b) Use the block to hold down the sample tape on the edge without adhesive. The space held down should be more than 2 mm in from the edge, but before the adhesive material.

(c) As shown in Figure 8, on the opposite side of the tape for the block, measure the highest point from the flat surface.

8.8.3 *Wakame*

(1) *Equipment* — Use a scale that measures at least 1 mm increments.

(2) *Material* — Cut a section of more than 30 cm, but less than 100 cm in length of TCP polyimide adhesive tape as received.

(3) *Measurement* — As shown in Figure 9, place on a flat surface for more than 12 hours and calculate the number of points off the flat surface less than 2 mm high.

8.8.4 *Camber*

(1) *Equipment* — Use a scale that measures at least 1 mm increments.

(2) *Material* — Cut a section of more than 30 cm, but less than 100 cm in length of TCP polyimide adhesive tape as received.

(3) *Measurement* — As shown in Figure 10, connect corners of the tape in a straight line, and measure the deviation from the line to the edge of the tape at the center.

8.8.5 *Twist*

(1) *Equipment* — Use a protractor that measures at least 1 degree increments.

(2) *Material* — Cut a section of 1 meter in length of TCP polyimide adhesive tape as received.

(3) *Measurement* — Hang the tape vertically and measure the angle of twist of the bottom edge as opposed to the top edge.

8.8.6 *Defects*

(1) *Equipment* — Use a 10 power magnifying glass or naked eye.

(2) *Material* — Use TCP polyimide adhesive tape as received. The length should be determined between the user and supplier.

(3) *Measurement* — Perform a check on defects against a limit sample determined by the user and supplier. Unless otherwise specified, the " Admixture Measurement Table" from the JIS P-8101 standard (Finance Ministry Printing Press) is recommended.

9. Product Labeling

Note the following items on the product label:

(1) Type Name

(2) Product Width

(3) Product Length

(4) Lot Number

10. Packing and Package Labeling

10.1 *Packing* — Pack the product with sufficient packing material to prevent any effects from external impact, moisture, etc.

10.2 *Package Label* — Note the following items on the packaging label:

(1) Product Name

(2) Type Name

(3) Manufacturer' s Name

(4) Product Width

(5) Product Length

(6) Lot Number

(7) Storage Conditions

11. Related Documents

11.1 *JIS Standards*

C-6471 — Test Method of Copper-Clad Laminates Flexible Printed Wiring Boards

K-6911 — Testing Methods for Thermosetting Plastics

K-7209 — Testing Methods for Water and Boiling Water Absorption of Plastics

P-8145 — Testing Method of Dirt in Paper and Paperboard

P-8208 — Method of Testing Dirt, Sheaves and Specks of Paper Pulp

11.2 *ASTM Standards*[2]

D-150 — Standard Test Methods for A-C Loss Characteristics and Permittivity (Dielectric Constant) of Solid Electrical Insulating Materials

D-257 — Standard Test Methods for D-C Resistance or Conductance of Insulating Materials

D-570 — Standard Test Methods for Water Absorption of Plastics

D-638 — Test for Tensile Properties of Plastics

D-1825 — Standard Practice for Etching and Cleaning Copper-Clad Electrical Insulating Materials and Thermosetting Laminates for Electrical Testing

2 American Society for Testing Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959

11.3 *IEC Standards*[3]

249-1 — Base Materials for Printed Circuits, Part 1: Test Methods

326-2 — Printed Boards, Part 2: Test Methods

674-2 — Specification for Plastic Films for Electrical Purposes, Part 2: Method of Test

11.4 *UL Standard*[4]

94-1991 — Standard for Flammability Tests of Plastic Materials for Parts in Devices and Appliances

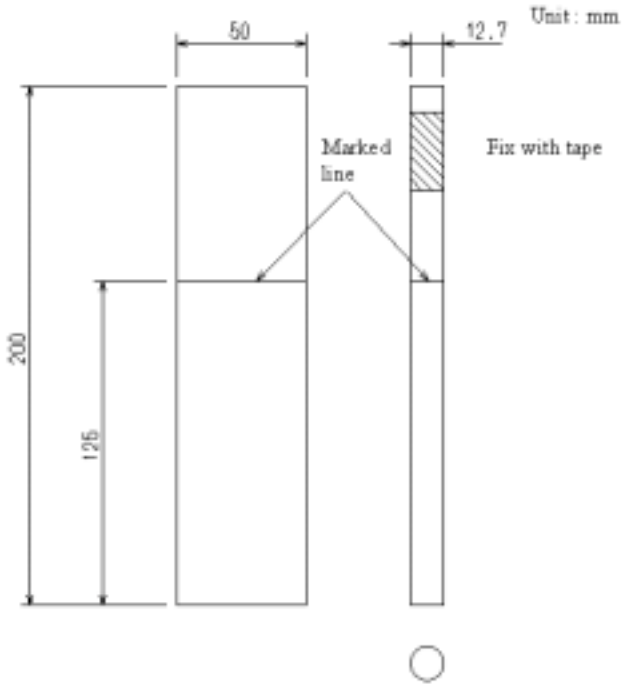

Figure 5
Test Specimen for Flammability

3 International Electrotechnical Commission, 3, rue de Varembé, P.O. Box 131, CH-1211 Geneva 20, Switzerland

4 Underwriters Laboratories, 333 Pfingsten Road, Northbrook, IL 60062-2096

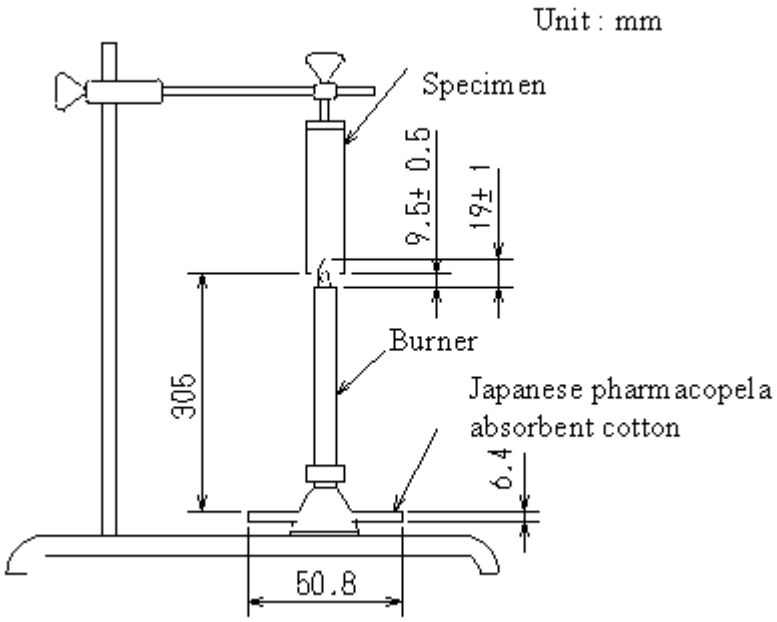

Figure 6
Measurement of Flammability

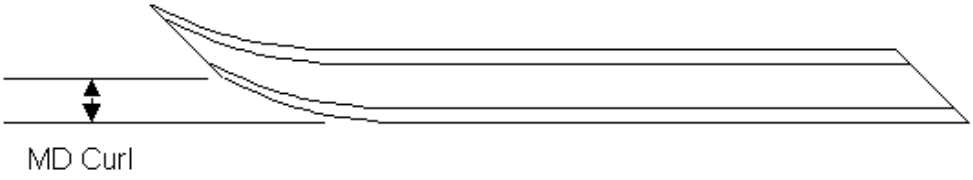

Figure 7
MD Curl

Figure 8
TD Curl

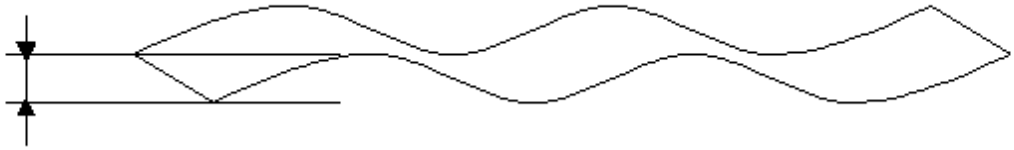

Figure 9
Wakame

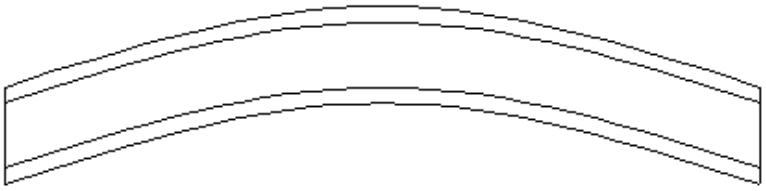

Figure 10
Camber

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SEMI G77-0699
SPECIFICATION FOR FRAME CASSETTE FOR 300 MM WAFERS

This test method was technically approved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on March 17, 1999. Initially available at www.semi.org May 1999; to be published June 1999.

1 Purpose

1.1 The purpose of this document is to specify the mechanical features for a 300 mm wafer frame cassette used between the wafer mounting process and the die-bonding process.

2 Scope

2.1 This standard is intended to set an appropriate level of specification that places minimal limits on innovation while ensuring modularity and interchangeability at all mechanical interfaces.

2.2 Only the physical interfaces for the frame cassette are specified; no materials requirements or micro-contamination limits are given. However, this specification was written to allow for both metal and plastic frame cassette designs.

2.3 This specification defines a 300 mm wafer frame cassette that is intended for both manual and automated transport. The frame cassette has the following components and sub-components (“ ” indicates an optional component):

2.3.1 Top

robotic handling flange (optional)

- top cover

2.3.2 Interior

- frame supports for 13 or 25 tape frames
- frame restraint

2.3.3 Sides

human handles (optional)

2.3.4 Rear

- rear cover

2.3.5 Bottom

- 2 bottom conveyor rails running along the sides of the frame cassette

3 features that mate with kinematic coupling pins and provide a 10 mm lead-in (optional)

4 frame cassette sending pads (optional)

3 Referenced Documents

3.1 *SEMI Standards*

SEMI E1.9 — Provisional Mechanical Specification for Cassettes Used to Transport and Store 300 mm Wafers

SEMI E15 — Specification for Tool Load Port

SEMI E47.1 — Provisional Mechanical Specification for Boxes and Pods Used to Transport and Store 300 mm Wafers

SEMI E57 — Provisional Mechanical Specification for Kinematic Couplings Used to Align and Support 300 mm Wafer Carriers

SEMI G74 — Specification for Tape Frame for 300 mm Wafers

SEMI S8 — Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment

4 Terminology

4.1 *bilaterial datum plane* — a vertical plane that bisects the tape frames and that is perpendicular to both the horizontal and facial datum planes (as defined in SEMI E57).

4.2 *conveyor rails* — parallel surfaces on the bottom of the cassette for supporting the cassette on roller conveyors.

4.3 *facial datum plane* — a vertical plane that bisects the tape frames and that is parallel to the front side of the frame cassette (where tape frames are removed or inserted). On tool load ports, it is also parallel to the load face plane specified in SEMI E15 on the side of the tool where the frame cassette is loaded and unloaded (as defined in SEMI E57).

4.4 *frame cassette* — an open structure that holds one or more tape frames.

4.5 *horizontal datum plane* — a horizontal plane from which projects the kinematic coupling pins on which the frame cassette sits. On tool load ports, it is at the load height specified in SEMI E15 and might not be physically realized as a surface (as defined in SEMI E57).

4.6 *robotic handling flange* — horizontal projection on the top of the frame cassette for lifting and rotating the frame cassette.

4.7 *tape frame* — the frame which applies the wafer tape to the wafer and retains the wafer.

4.8 *wafer tape* — an adhesive plastic tape which retains the wafer or diced chip. It is used between the mounting process and die-bonding process.

5 Ordering Information

5.1 *Intended use* — This document is intended to specify 300 mm wafer frame cassettes over a reasonable lifetime of use, not just those in new condition. For this reason, the purchaser needs to specify a time period as well as the number and type of uses to which the frame cassettes will be put. It is under these conditions that the frame cassettes must remain in compliance with the requirements listed in Section 6.

6 Requirements

6.1 *Dimensions* — The frame cassette dimensions are shown in Figures 1 through 5 and listed in Table 1. In all figures, the heaviest lines are used for surfaces that have tolerances (not surfaces that have only maximum or only minimum dimensions).

6.2 *Tape Frame Orientation* — The tape frames must be horizontal when the frame cassette is placed on the load port.

6.3 *Center of Tape Frames* — When a tape frame is stored in the frame cassette, the center of the tape frame should be within the radius of 2 mm from the center of the junction of the bilaterial datum plane and the facial datum plane.

6.4 *Top and Rear Covers* — Both top and rear covers are required. With the covers in place, the frame cassette must conform to all dimensions listed in Table 1.

6.5 *Number of Slots* — The frame cassette has an option of either 13 or 25 slots.

6.6 *Kinematic Couplings (optional)* — The physical alignment mechanism from the frame cassette to the tool load port (or a nest on a vehicle or in a stocker) consists of features (not specified in this document) on the top entity that mate with three or six pins underneath as defined in SEMI E57. Most of the dimensions of the frame cassette are determined with respect to the three orthogonal datum planes defined in that standard: the Horizontal Datum Plane, the facial datum plane, and the bilateral datum plane.

6.6.1 The three features that mate with the pins must provide a lead-in capability that corrects a frame cassette misalignment of up to 10 mm in any horizontal direction, although 15 mm is recommended for ergonomic reasons. However, it is recommended that robotics placing cassettes on kinematic couplings use as little of this lead-in capability as possible to avoid wear.

6.7 *Human Handles (optional)* — All handles for use by humans must either be contained within the maximum outer dimensions of the frame cassette, be detached when not in use, or be retractable into the maximum outer dimensions when not in use. Handles for use by humans (if present) must follow SEMI S8 and shall require the use of both hands (each using a full wrap-around grip, given the minimum clearance requirement in SEMI E15.1). Automation handling features shall not be considered for dual purpose unless they are designed to meet SEMI S8.

6.8 *Robotic Handling Flange (optional)* — On the top of the frame cassette is an optional robotic handling flange for manipulating the frame cassette.

6.9 *Bottom Rails* — On the bottom of the frame cassette are two rails, one on each side for use with roller conveyors.

6.10 *Frame Restraint* — The frame cassette must provide a feature that prevents tape frames from slipping out of the cassette during transport. The feature must conform to all dimensions listed in Table 1.

6.11 *Frame Cassette Sensing Pads (optional)* — When the cassette is fully down, the frame cassette sensing pads (see Figure 5) must be z2 above the horizontal datum plane. It is recommended that the areas surrounding all of the frame cassette sensing pads be designed in conjunction with the features that mate with the kinematic coupling pins so that a mechanical sensor pin cannot interfere with the lead-in function of the kinematic couplings.

6.12 *Cassette Stacking (optional)* — The frame cassette may have optional features to allow two 13 capacity cassettes to be stacked on top of each other. This option is only available for cassettes without a robotic handling flange.

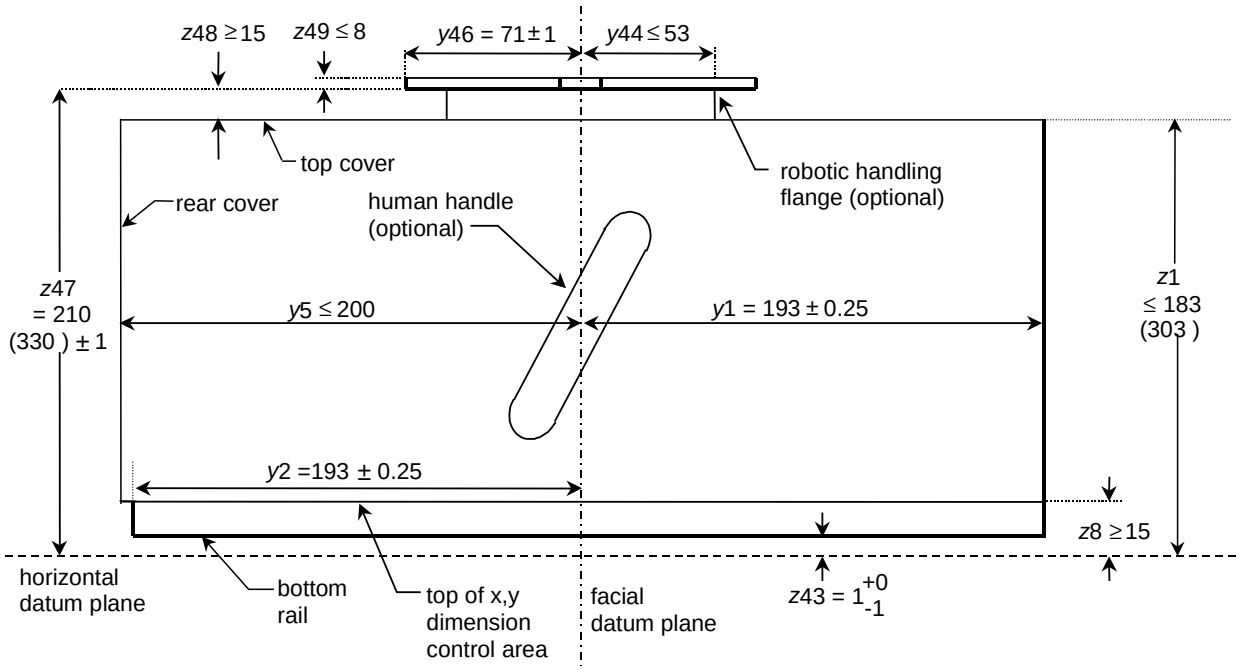

Figure 1

Side View of Frame Cassette

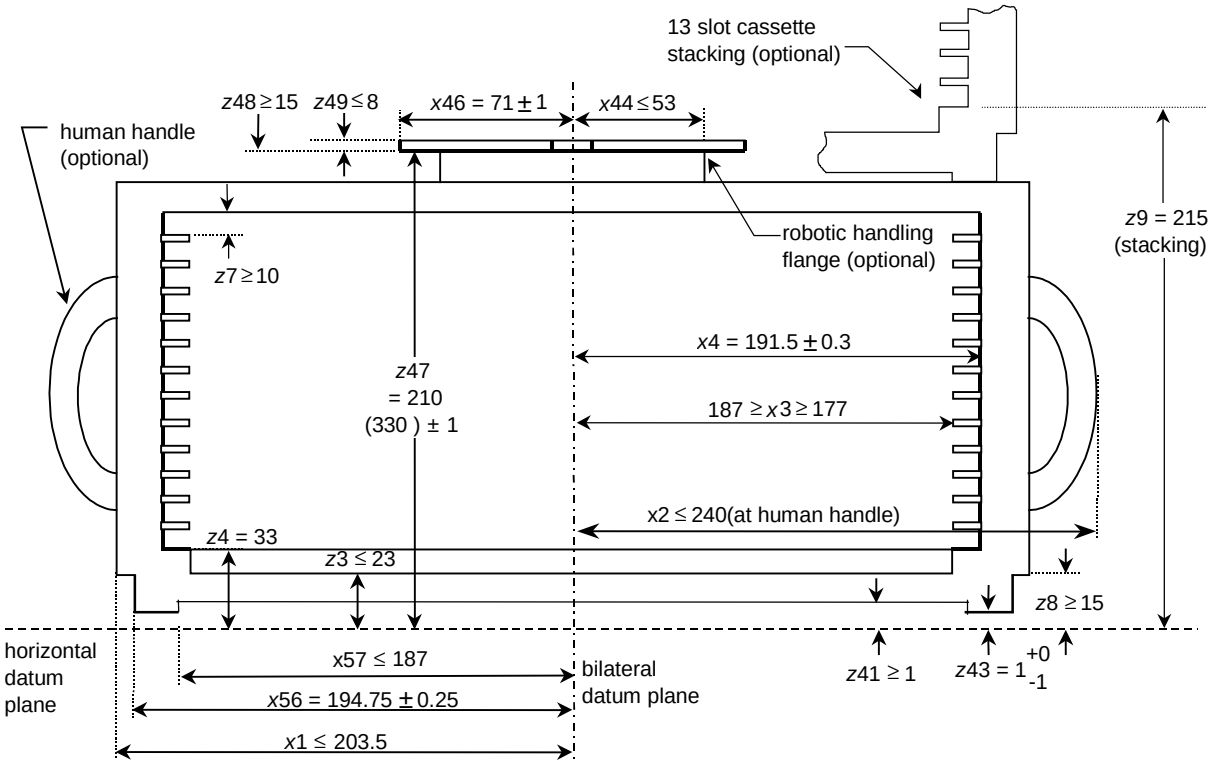

Figure 2

Front View of Frame Cassette

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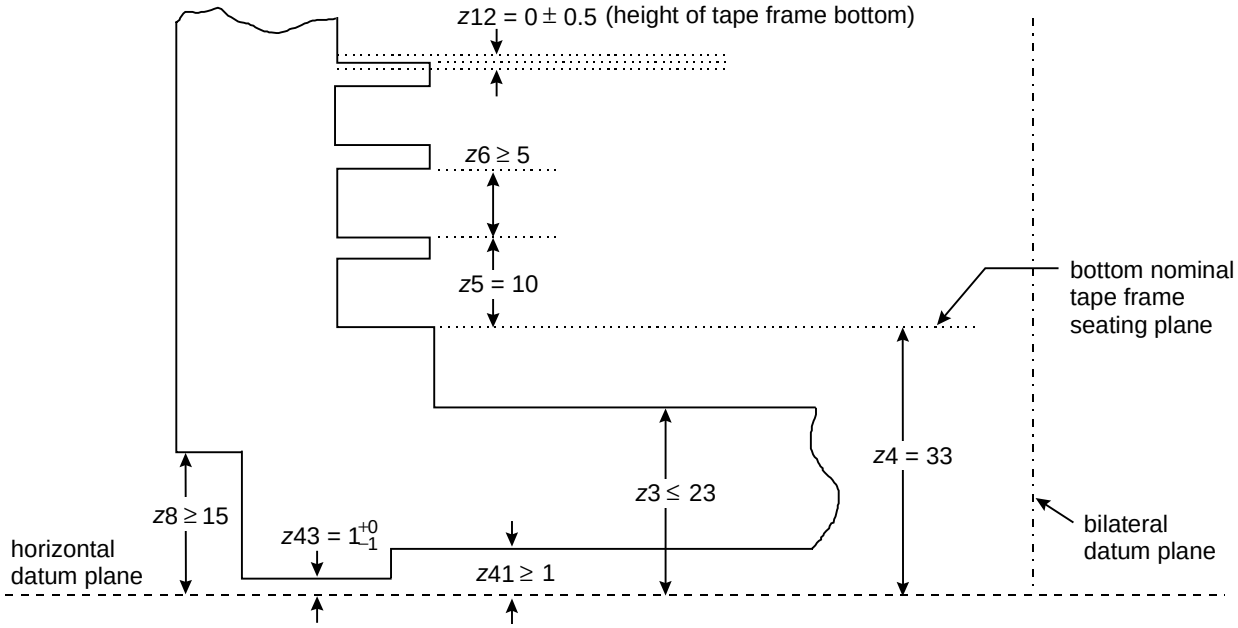

Figure 3

Detail of Film Frame Supports

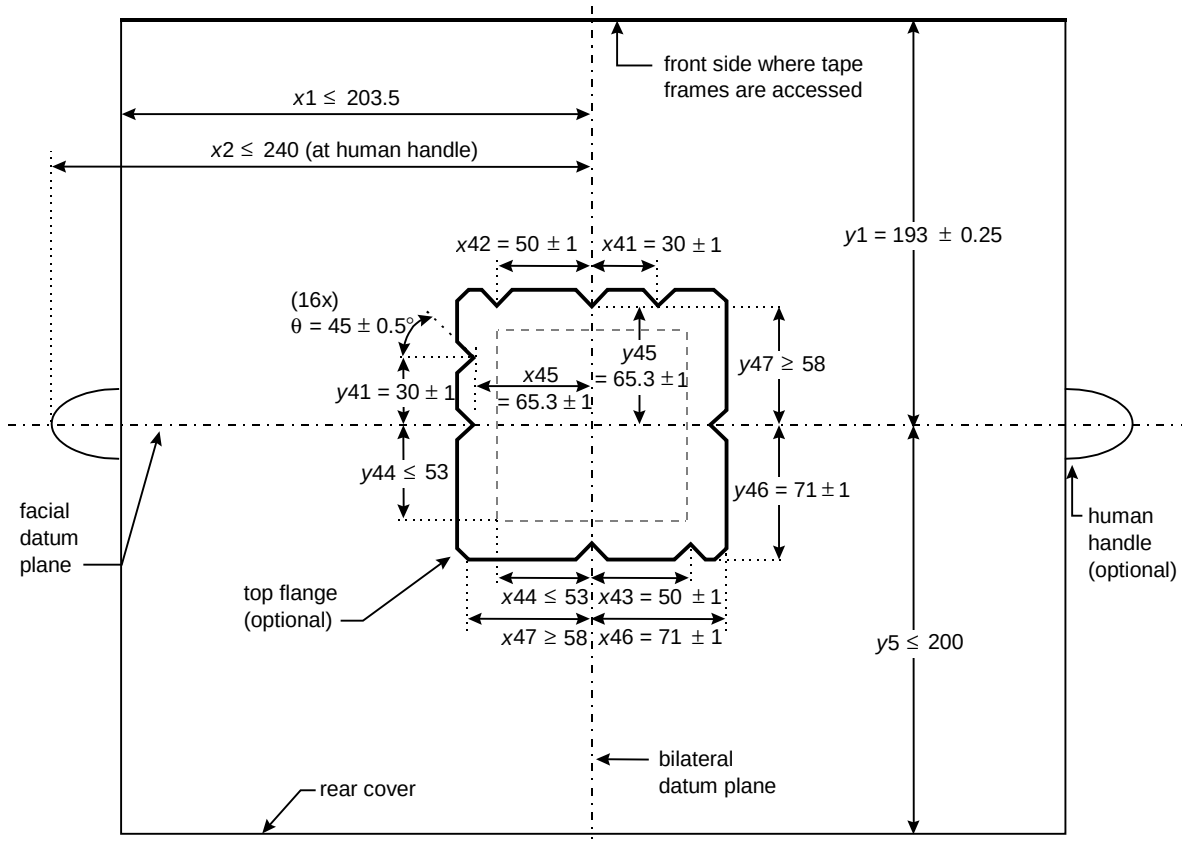

Figure 4

Top View of Frame Cassette

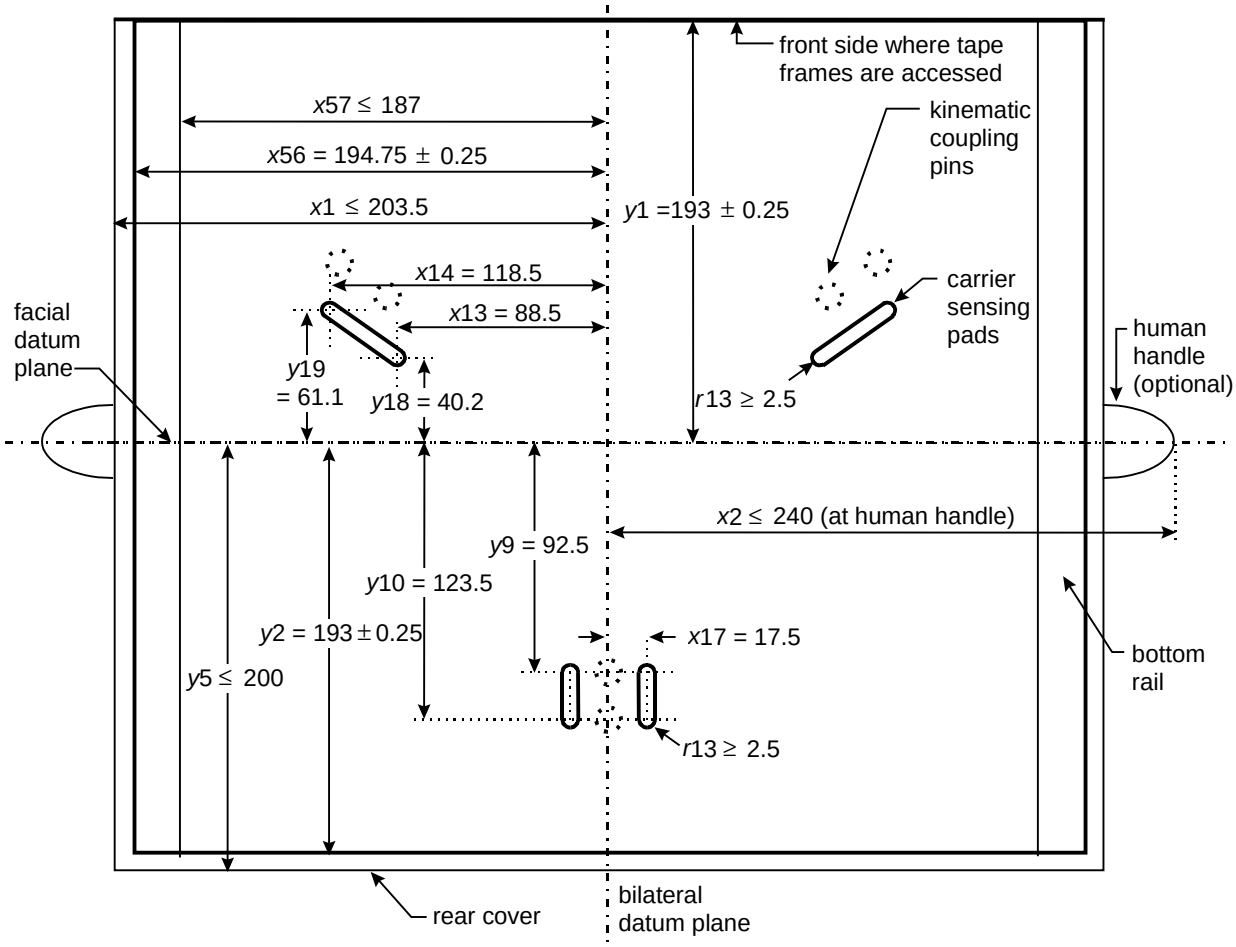

Figure 5

Bottom View of Frame Cassette

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Table 1 Dimensions for Frame Cassette

Symbol	*Value Specified*	*Datum Measured From*	*Feature Measured To*
θ‡	45 ± 0.5°	either vertical datum plane	sides of position and orientation notches
*r*13†	2.5 mm 2.6 minimum	line segment along center of cassette sensing pad	edge of cassette sensing pad
*x*1	203.5 mm maximum	bilateral datum plane	outer surface of frame cassette (without handles)
*x*2	240 mm maximum	bilateral datum plane	furthest reach of human handles
*x*3	177 mm minimum 187 mm maximum	bilateral datum plane	inside edge of tape frame support
*x*4	191.5 ± 0.3 mm	bilateral datum plane	inside wall of frame cassette
*x*13†	88.5 mm	bilateral datum plane	near end of line segment along center of front cassette sensing pads
*x*14†	118.5 mm	bilateral datum plane	far end of line segment along center of front cassette sensing pads
*x*17†	17.5 mm	bilateral datum plane	line segment along center of rear cassette sensing pads
*x*41‡	30 ± 1 mm	bilateral datum plane	front right orientation notch on robotic handling flange
*x*42‡	50 ± 1 mm	bilateral datum plane	front left orientation notch on robotic handling flange
*x*43‡	50 ± 1 mm	bilateral datum plane	rear orientation notch on robotic handling flange
*x*44‡	53 mm maximum	bilateral datum plane	encroachment of box underneath robotic handling flange
*x*45‡	65.3 ± 1 mm	bilateral datum plane	nearest point of side position and orientation notches on robotic handling flange
*x*46‡	71 ± 1 mm	bilateral datum plane	sides of robotic handling flange
*x*47‡	58 mm minimum	bilateral datum plane	end of robotic handling flange front and rear
*x*56‡	194.75 ± 0.25 mm	bilateral datum plane	outside edge of bottom rails
*x*57	187 mm maximum	bilateral datum plane	box sides underneath bottom rails
*y*1	193 ± 0.25 mm	facial datum plane	front outside edge of frame cassette
*y*2	193 ± 0.25 mm	facial datum plane	back outside bottom edge of frame cassette

Symbol	*Value Specified*	*Datum Measured From*	*Feature Measured To*
*y*5	200 mm maximum	facial datum plane	rear outside edge of frame cassette including rear cover
*y*9†	92.5 mm	facial datum plane	front end of line segment along center of rear cassette sensing pads
*y*10†	123.5 mm	facial datum plane	rear end of line segment along center of rear cassette sensing pads
*y*18†	40.2 mm	facial datum plane	near end of line segment along center of front cassette sensing pads
*y*19†	61.1 mm	facial datum plane	far end of line segment along center of front cassette sensing pads
*y*41‡	30 ± 1 mm	facial datum plane	left orientation notch on robotic handling flange
*y*44‡	53 mm maximum	facial datum plane	encroachment of frame cassette underneath robotic handling flange
*y*45‡	65.3 ± 1 mm	facial datum plane	nearest point of front and rear position and orientation notches on robotic handling flange
*y*46‡	71 ± 1 mm	facial datum plane	front and rear edge of robotic handling flange
*y*47‡	58 mm minimum	facial datum plane	end of robotic handling flange sides
*z*1	183 mm maximum 13-frame cassette 303 mm maximum 25-frame cassette	facial datum plane	top of frame cassette
*z*2†	2 mm maximum	horizontal datum plane	bottom of frame cassette sensing pads
*z*3	23 mm maximum	horizontal datum plane	internal floor of frame cassette
*z*4	33 mm	horizontal datum plane	bottom nominal film frame seating plane
*z*5	10 mm	each nominal film frame seating plane	adjacent nominal film frame seating planes
*z*6	5 mm minimum	bottom of film frame support	top of film frame support below
*z*7	10 mm minimum	top surface of the top frame support	internal ceiling of frame cassette
*z*8	15 mm minimum	horizontal datum plane	top of x56 and y1 dimension controlled area
*z*9	215 mm	horizontal datum plane	bottom nominal film frame seating plane of top stacked cassette (13 slot only)
*z*12	0 ± 0.5 mm	each nominal tape frame seating plane	bottom of the tape frame

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Symbol	*Value Specified*	*Datum Measured From*	*Feature Measured To*
*z*41	1 mm minimum	horizontal datum plane	bottom of frame cassette
*z*43	1 + 0 -1 mm	horizontal datum plane	bottom rails
*z*47‡	210 ± 1 mm 13-frame frame cassette 330 ± 1 mm 25-frame frame cassette	horizontal datum plane	bottom of robotic handling flange
*z*48‡	15 mm minimum	bottom of robotic handling flange	encroachment of frame cassette top underneath robotic handling flange
*z*49‡	8 mm maximum	bottom of robotic handling flange	top of robotic handling flange

† These dimensions match those of SEMI E1.9 with the same symbol.

‡ These dimensions match those of SEMI E47.1 with the same symbol.

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SEMI G78-0699
TEST METHOD FOR COMPARING AUTOMATED WAFER PROBE SYSTEMS UTILIZING PROCESS-SPECIFIC MEASUREMENTS

This test method was technically approved by the Global Automated Test Equipment Committee and is the direct responsibility of the North American Automated Test Equipment Committee. Current edition approved by the North American Regional Standards Committee on December 18, 1998. Initially available at www.semi.org April 1999; to be published June 1999.

1 Purpose

1.1 To define the terms and provide a means of comparative, or relative measurement for the automated wafer prober functions: Accuracy, Repeatability and Throughput.

2 Scope

2.1 This method may be used to evaluate the performance of a single automated wafer prober, or as a means to compare many probers. The probers that this document addresses are defined as fully automated; that is, having automatic material handling, alignment and probing capabilities.

3 Limitations

3.1 This test and comparison method is not intended to represent a statistically complete methodology for measuring the performance of an automated wafer prober. Its correct use is a practical means to compare the stepping capabilities of wafer probers within a specific end user's environment.

3.2 The definitions of the terms "Repeatability" and "Accuracy" as used in this document are not in accordance with those of the National Conference of Standards Laboratories (NCSL) nor are they intended to be. They are to be used solely for the purpose of this document and have no other intended uses.

3.3 It is difficult to characterize and eliminate high temperature contributions to positional error such as probe needle 'float'. Therefore, it is strongly recommended that the same probe card be used to evaluate all of the probers being considered.

3.4 It is recommended that the probe card is verified to be in the same condition (i.e. evaluated for positional accuracy and overall functional condition) both before and after the conclusion of each test.

3.5 Bump placement on a semiconductor device is generally located ± 0.001" with respect to their nominal location. Vertical probe cards used to probe bumps have an inherent amount of needle drift. Therefore care must be exercised in using vertical probe cards on bump devices as a means of prober accuracy measurement.

4 Referenced Documents

NOTE: As listed or revised, all documents cited shall be the latest publications of adopted standards.

4.1 *SEMI Documents*

SEMI E10 — Standard for Definition and Measurement of Equipment Reliability, Availability and Maintainability (RAM)

SEMI S2 — Safety Guidelines for Semiconductor Manufacturing Equipment

5 Terminology

5.1 *3σ limit* — a statistically derived measurement of process variation. A process that allows a ± 3σ deviation will allow 2.7 parts per thousand to be outside the established bounds.

5.2 *accuracy* — the ability of an automatic wafer prober to index its chuck, and attached wafer, from an initial position to a subsequent position and make contact with a static probe tip at a nominal location on the wafer. In the context of this method, accuracy is defined as average die offset.

5.2.1 Average die offset is the perpendicular distance measured from the centerline of the die pad to a parallel line that statistically represents the scrub mark data point distribution center (see Figure 1). Each data point shown in this figure represents only the center value of accumulated scrub marks produced by operation of this method.

5.2.2 It should be noted that accuracy established by this method is characteristic of the system, which in total represents both the automated prober as well as its probe card. Finally, this method establishes two accuracy values, a value for pads along the X and Y axes of the die. These axis directions are arbitrary.

5.2.3 It should be noted that if fully automated prober set-up modes are not used for probe-needle-to-pad alignment during testing, the possibility of operator error should be considered as a variable when evaluating system accuracy.

5.3 *automatic wafer prober* — device that automatically and repeatedly aligns the die bonding

pads or interconnect bumps on a semiconductor device to a set of test needles attached to a probe card.

5.4 *bonding pad* — exposed metallic contact area on a semiconductor device that is surrounded by dielectric passivation. This is the point at which a temporary interconnect is made for wafer level test, and permanent interconnect for packaging.

5.5 *bumps* — metallic elevated contact area on a semiconductor device that is used in place of a bonding pad. A die that is designed to use this type of connection is commonly called a 'flip chip' or direct chip attach.

5.6 *die* — individual semiconductor device. For the purposes of this method, the dice have not been singulated, and are still in the form of a wafer. Used interchangeably (in the context of wafer sort) with the acronym DUT (Device Under Test).

5.7 *overdrive* — distance in Z which the wafer is driven beyond a user defined initial contact point, typically 'first electrical contact'.

5.8 *overhead test* — semiconductor test method where the test head is mounted directly over the prober, with the goal of shortening the distance between the pin electronics and the probe card. The connection between the test head and the prober is generally through a device called a Prober Tester Interface (PTI)

5.9 *pin electronics* — tester hardware that creates the test signals used to challenge the DUT.

5.10 *probe card* — printed wiring board or ceramic substrate with permanently attached needles or contacts that are aligned at the time of manufacture to match the contact pattern on a Die. Common types of probe cards are:

- Blade
- Peripheral / Cantilever (AKA Epoxy Ring)
- Vertical (AKA Area Array or Cobra™)

5.11 *probe card planarity and alignment* — a user-specified position of the probe tips in 'x', 'y' and 'z'.

5.12 *probe needles* — the contact points between the probe card and the bonding pads. These are typically manufactured from one of the following materials:

- Beryllium copper
- Tungsten
- Tungsten-rhenium alloy
- Paliney

5.13 *prober tester interface (PTI)* — signal-transmitting electro-mechanical device that connects the pin cards in the tester to the probe card.

5.14 *repeatability* — Figure 1 is empirical data and represents a statistically significant sample of scrub marks. This data reveals that probe needles may not make contact consistently to the same point die to die. Recall that accuracy is defined in this method as average die offset. Thus, repeatability simply represents the three-sigma distribution value for average die offset. Repeatability will represent 99.7% or a three-sigma distribution value for the accumulated offset data points obtained through use of this method.

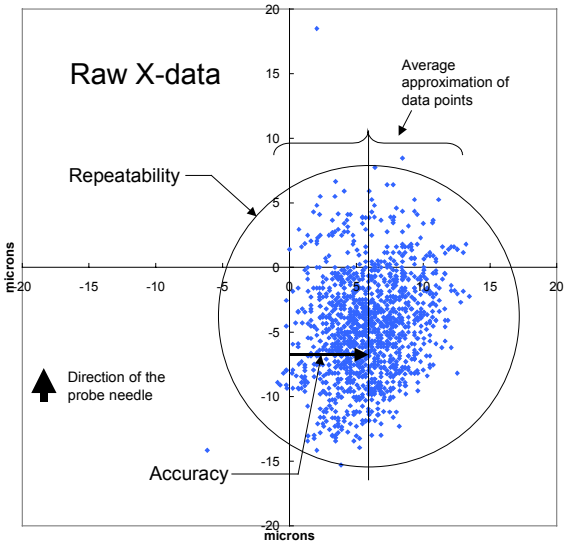

Figure 1

Raw X-Data

5.14.1 The X-Y plotted centroids of these scrub marks will be found to form a "cloud" of points, densest in the center, and thinning out towards the edges.

5.14.2 Repeatability is the radius of that cloud or "cluster" of probe marks, as defined by the 3 σ or other user defined limit of that cloud. The error in the placement of the center of that cloud, relative to its nominal target, is defined as the automatic wafer prober's "Accuracy". (See Figure 1)

5.15 *set point* — the value to which a control system's input device has been set, as opposed to the actual value to which the control system has driven the controlled variable. For example, the input setting to the wafer chuck temperature controller, as opposed to the actual, independently measured temperature of the wafer chuck.

5.16 *soak time* — time between a piece of equipment's reaching the set point temperature and use of that piece of equipment.

5.17 *scrub mark* — mark left by the probe in the bonding pad or bump after the probe card has touched down on the wafer.

5.18 *temperature testing* — testing of devices at a controlled temperature level other than ambient.

5.19 *test* — one complete run-through of the data collection portion of this document on one automated wafer prober.

5.20 *tester* — specialized computer controlled system designed to test integrated circuits.

5.21 *prober communications protocol (see Section 9.6)* — means of transmitting data between the tester and the prober. Common methods are:

- TTL
- RS-232c
- GPIB

5.22 *test head* — package of electronics (part of the Tester) which interacts both electrically and mechanically with the probe card, typically through the Prober Tester Interface (PTI).

5.23 *throughput* — rate at which die can be cycled, by the automatic wafer prober, for the purpose of being tested. It is inherent in the functionality of an automatic wafer prober (or any other motorized positioning device) that accuracy, repeatability and throughput are intimately and inseparably related.

5.24 *touch down* — contact between the probe card and the wafer. This user may choose to define this as either first electrical or first mechanical contact.

5.25 *wafer* — semiconductor substrate upon which multiple die are fabricated.

5.26 *wafer boat or wafer cassette* — carrier for multiple wafers.

5.27 *wafer chuck* — platform within an automatic wafer prober that supports and transports the wafer. The chuck may contain the means for controlled temperature testing.

5.28 *x, y, z and θ* — motions relative to the center of the Probe Card when standing in front of the Prober:

- Motion to the right is motion in the positive X-direction.
- Motion towards the back of the prober is motion in the positive Y-direction.
- Motion away from the floor is the positive Z-direction.
- Motion revolving around a Z-axis passing through the center of the probe card is θ-motion. Motion in the counter-clockwise direction when facing down from above the prober is motion in the positive θ-direction.

5.29 *z-clearance* — distance between the user defined initial contact point and the top surface of the wafer during that portion of the wafer prober's cycle when the wafer chuck is moving the wafer between DUTs.

6 Summary of Method

6.1 *Objective* – A SEMI Probe Standards Task Force has defined this method. That task force consisted of members from semiconductor wafer probe system users and wafer probe system suppliers. This method, in part a guide to collection of data, is aimed at a specific set of wafer probe system parameters: accuracy, repeatability and throughput. This method is a tool that creates comparative data. That data will act as a criterion by which multiple wafer probe systems can be judged competitively.

6.2 *Probe System Accuracy and Throughput* – A wafer probe system will have needle placement error due to the probe system electromechanical systems, and additional needle placement error due to the probe card physical alignment of the needles. The degree of accuracy to which the probe system can place the chuck, the effectiveness of the probe system's bond pad to needle alignment, the physical alignment of the probe card needles in their X and Y plane, and the probe system's vision resolution and accuracy (x microns of distance per pixel) will be the factors that influence a probe system's overall placement performance.

6.2.1 Probe system comparative accuracy and repeatability are established in this method using probe mark data acquired manually with a vision system or, if available, through use of an automated probe mark data analysis system. Acquired data is analyzed with the Probe Mark Data Analysis algorithm contained in this method.

6.2.1.1 The intention of this data collection exercise is not to make a deterministic conclusion establishing a probe system's accuracy. Data analysis results are only meaningful in the context of a comparative analysis of multiple probe systems.

6.2.2 Probe system throughput is best determined using time measurements made using a stopwatch. Other approaches can be applied, such as:

- the time stamp and log file (if available) on the probe system under evaluation.
- time tracking within the device test program employed for testing the prober.

6.2.3 Any of these approaches is viable for measuring time intervals during probe system operation. That data

is to be entered into the data collection table as part of the application of this method.

6.2.4 The algorithm collects data from 9 wafers out of a lot of 10. Three setups are performed using 3 wafers per setup. All dice will be probed, but data will be taken only on twelve of the die on each wafer. Twenty-four pads on each die are evaluated (see Figure 4). Overall, 2592 die pads are analyzed in a lot.

6.2.5 When all the data is collected and analyzed, each probe system will have an average die offset value. This will be a comparative representation of accuracy consisting of average offsets for all evaluated die. This comparative representation of accuracy is a measure of how accurate the probe systems place the chuck, and thus the probe needles, to the center point on the die pads, consistent with normal operation of the probe systems.

6.2.6 In general, when the probe marks are viewed across all dice, there will be a data spread, or distribution of error points for each wafer. Repeatability is the ± 3σ variation of all die offsets, identified in this method as the 3σ calculation of *Normalized Die Offset*.

6.3 *Probe Card Issues* – Probe card construction variability and probe card usage at temperatures other than ambient are important considerations. The following sources of error should be kept in mind:

- In a hot chuck environment the probe card and needles will experience a high percentage of the elevated chuck temperature. The material selection for the probe card will determine how it expands and contracts due to the temperatures applied. Probe systems can be equipped with programmable preheat (soak) times. Longer preheat times will reduce probe card variability while decreasing throughput.
- Needle construction can result in excessive error due to bending of the needles when excessive probe system z-stage overdrive is applied. The number of needles and the selection of needle technology, i.e., cantilever versus vertical, is another variable, having a noticeable influence on measurement results.
- Since each user of this method is not confined to a standard for probe card construction, the user of this method is advised to choose a probe card and vendor with good integrity, and to use that same probe card when evaluating multiple probe systems. The assertion here is that the same probe card used to evaluate multiple systems will react in a repeatable manner under varying environmental conditions. This assumes there is no excessive probe card needle wear during the multiple evaluations, and that needle alignment is verified or achieved before each execution of the procedure.

6.3.1 Probe mark scrub length can vary due to several factors including:

- variations in the flatness of the chuck and stage travel that are not compensated by the z-sensor mapping algorithms
- by hard spots in the aluminum pads, or
- by variations in probe tip geometry, etc.

6.3.2 To minimize the impact of this variation in the probe mark analysis algorithm, use only scrub mark location data that is taken normal to the direction of scrub. Distances measured normal to the orientation of the scrub mark are generally accepted to be significantly more stable than that which is taken parallel to the scrub mark (see Figure 2).

6.3.3 In summary, the probe card itself can be a limiting factor when making needle placement accuracy measurements, especially at varying environmental conditions. Material selection, vendor to vendor variation, construction of a probe card (blade, epoxy ring, vertical, etc.), especially with varying environmental conditions, will create inconsistent analysis results, unless care is taken with the application of this method. The precautions discussed here are meant to promote consistent and accurate evaluation results for this method.

6.3.4 Nevertheless, the precautions mentioned here could ALSO be an important basis for using this method. As an example, a probe card is typically designed for XY positional placement and planarity, and is expected to meet customer specification requirements in normal operation at room temperatures. This method could serve as a means of establishing numerical results that represents the effects that temperature or probe card construction variability have on probe card specification requirements.

6.4 *The PMA Algorithm* – A best-fit rectangle can be drawn around the scrub mark and the passivation opening for each pad, reference Figure 3.

NOTE: Applying a best-fit rectangle around the passivation opening may prove difficult for certain vision systems. Application of the best-fit rectangle around the die pad metal is an acceptable alternative. The center position of the best-fit rectangle around the scrub mark will represent the center of the scrub mark. The center of the die pad is the center of the best—fit rectangle around the passivation opening. The distance between the two centers is the pad offset. Pad offset is computed from the four values *left*, *right*, *top*, and *bottom*, reference Figure 2.

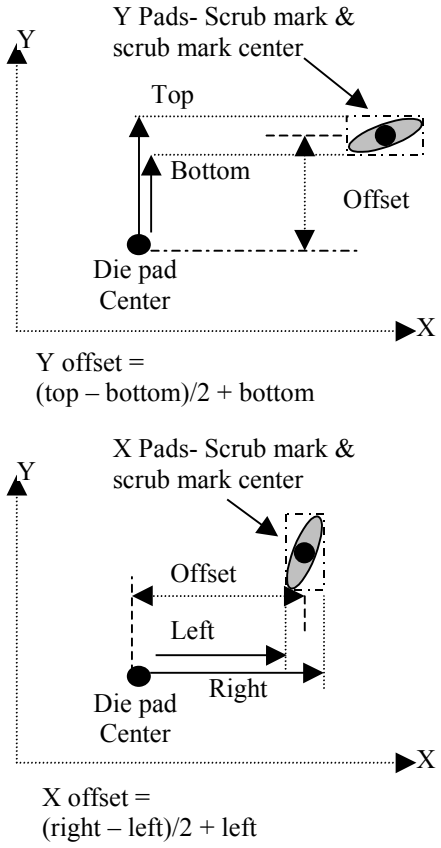

Figure 2

X and Y Offset

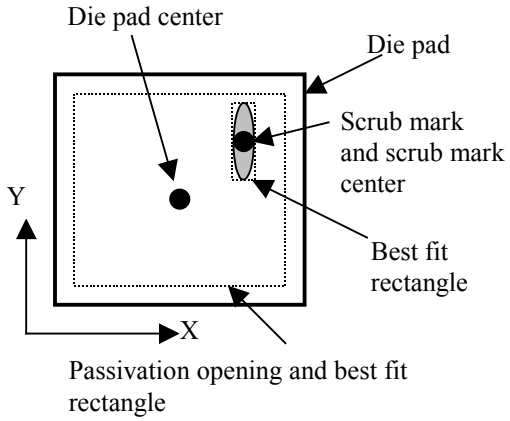

Figure 3

Scrub Mark Analysis

6.4.1 Vision system measurements will be made establishing offset distances from the die pad center to the scrub mark. The stability of the measurement is greater when made perpendicular to the direction of the scrub mark. This will establish X and Y offsets via measurement of offsets for pads in the X and Y plane of the die.

6.4.2 Once the offsets are established, a two-step procedure will manipulate 1296 X and 1296 Y offset values. The end result of the algorithm will be a relative measure of the total probe system accuracy and repeatability for the pads analyzed. Figure 5 represents a visual summary of the method.

6.5 *Considerations of Scale* — When evaluating the suitability of a particular probe system to probe a particular size of bond pad, or to probe accurately at a particular pad-to-pad pitch, a good rule of thumb is that the prober's positional accuracy, as stated in its specifications, should be 1/10 that of the scale of the features to be probed. For example, if the probe system being evaluated has an overall placement accuracy of 5µm, it would be inappropriate to analyze wafers using this method and this probe system for dice that have pads less than 50 µm square (this would be less than 10x).

6.5.1 Regardless, when this method is used for evaluation of multiple systems, it is essential that die and bond pad size/pitch consistency be maintained from evaluation to evaluation if the results are to be meaningful.

6.5.2 The same 10× rule applies to the vision system or automated Probe Mark Analysis system employed to make the pad offset measurements. These systems should have a pixel resolution that is at least 10× finer than the die pad dimensions associated with the scrub marks being measured.

6.6 *Conclusion* — It is assumed that the user of this method has a wafer probe system or systems, or is planning to make a selection from the various systems available in the market place, and requires objective comparative analysis for accuracy, repeatability and throughput.

6.6.1 It should be clear that this method employs a three-step process of probing, probe mark data collection, and data analysis.

6.6.2 When probing, every die on each of the ten wafers is to be "tested" and probed. Of those ten wafers, the last nine with 12 die per wafer will be used for scrub mark data collection. At least 24 pads per die will be used for the analysis. The first wafer is meant only to allow stabilization for the probe system and its probe card.

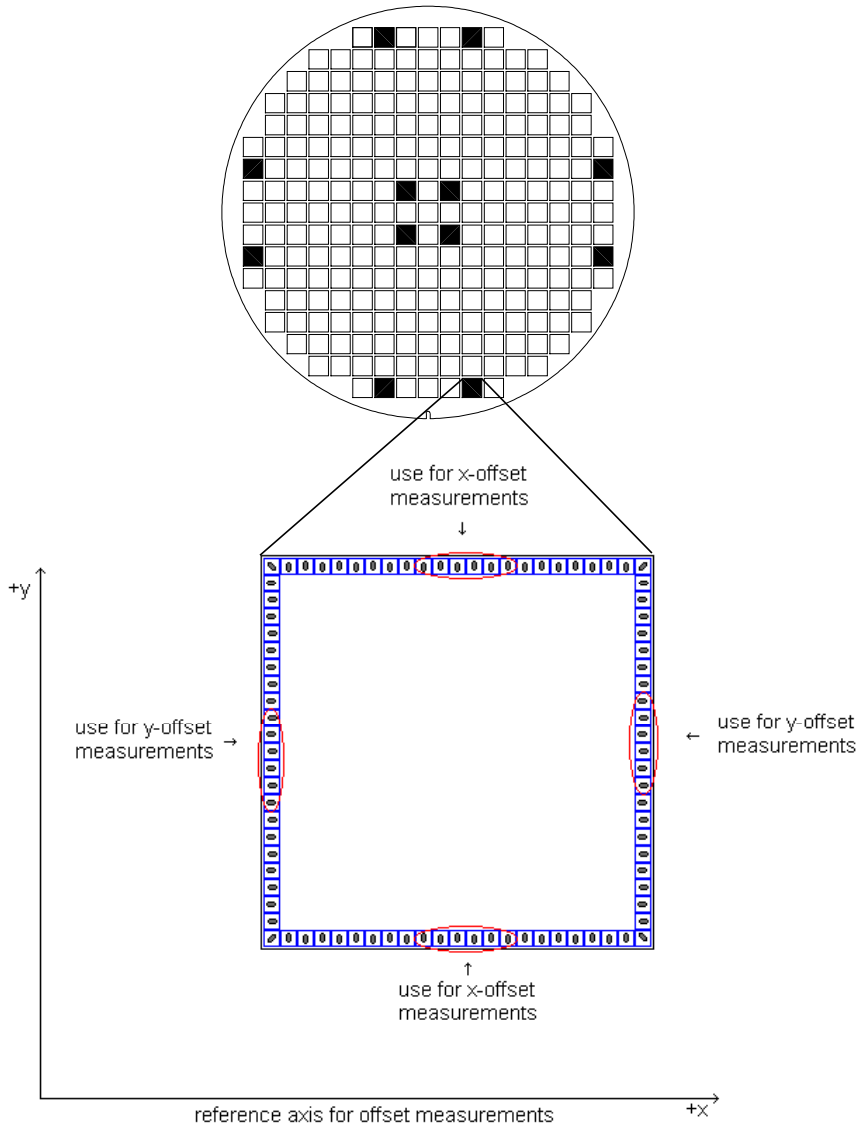

Figure 4

Recommended Dice and Pads to be used for Data Collection

6.6.3 It is important that the wafers used with this method are probed only once, or else multiple scrub marks may be difficult for the measurement system to deal with and will most likely influence the analysis results. This method assumes the wafer is ideal, having no die skew due to wafer process anomalies.

NOTE: It is possible that a not so perfect probe tip to pad alignment (PTTPA) may create misleading results for this method. It is recommended that PTTPA be done on die located at the edge of the wafer, as shown in Figure 4. This is opposed to having PTTPA done on die in the center of the wafer. An offset error incurred in the context of a PTTPA done in the center may result in an incremental and continuing error as testing moves across the wafer. With this method that error may be averaged-out.

6.6.4 Probe system index time is device and probe system dependent. Probe system index time is determined by acceleration, maximum achievable velocity, and distance traveled die to die by the chuck. Thus, the device type chosen for use with this method should be representative of typical die size if meaningful index time and throughput data are to be gathered.

6.6.5 If the results of this method turn out to be unfavorable, the user has the option of applying a more detailed, enhanced data analysis application of this method. That application is contained in Appendix 1. The enhanced method uses the same data, but it requires more manipulation of the data during data analysis. The detail contained in the enhanced algorithm will provide the user with greater insight as to the cause of unfavorable results related to the probe system under evaluation. A summary of the enhanced method is shown in Figure 6.

6.7 *Alternatives* — What has been left undefined to this point is availability of an automated approach to data collection per the requirements of this method. Regardless, data collection can be manually accomplished. The manual process is laborious and requires a video measuring system to make offset measurements on the die pads, and a spreadsheet to analyze the resulting data.

6.7.1 If manual operation is not desirable or practical, automated Probe Mark Analysis Systems do exist in the market place as an item to be purchased. Providers are also available to accept probed wafers and execute probe mark analysis under contract as a service.

NOTE: *A Final Note to the User of This Method* — This method provides sufficient data for sophisticated analysis of probe system performance across die-to-die, wafer-to-wafer, and setup-to-setup. It also provides a simple metric. It is easy to make comparisons with simple "single number" metrics, but that has the potential for oversight, distortion and subsequent inappropriate comparisons. The test engineer, working with the probe system supplier, must be the ultimate judge of the applicability of this method and the correct interpretation of the results.

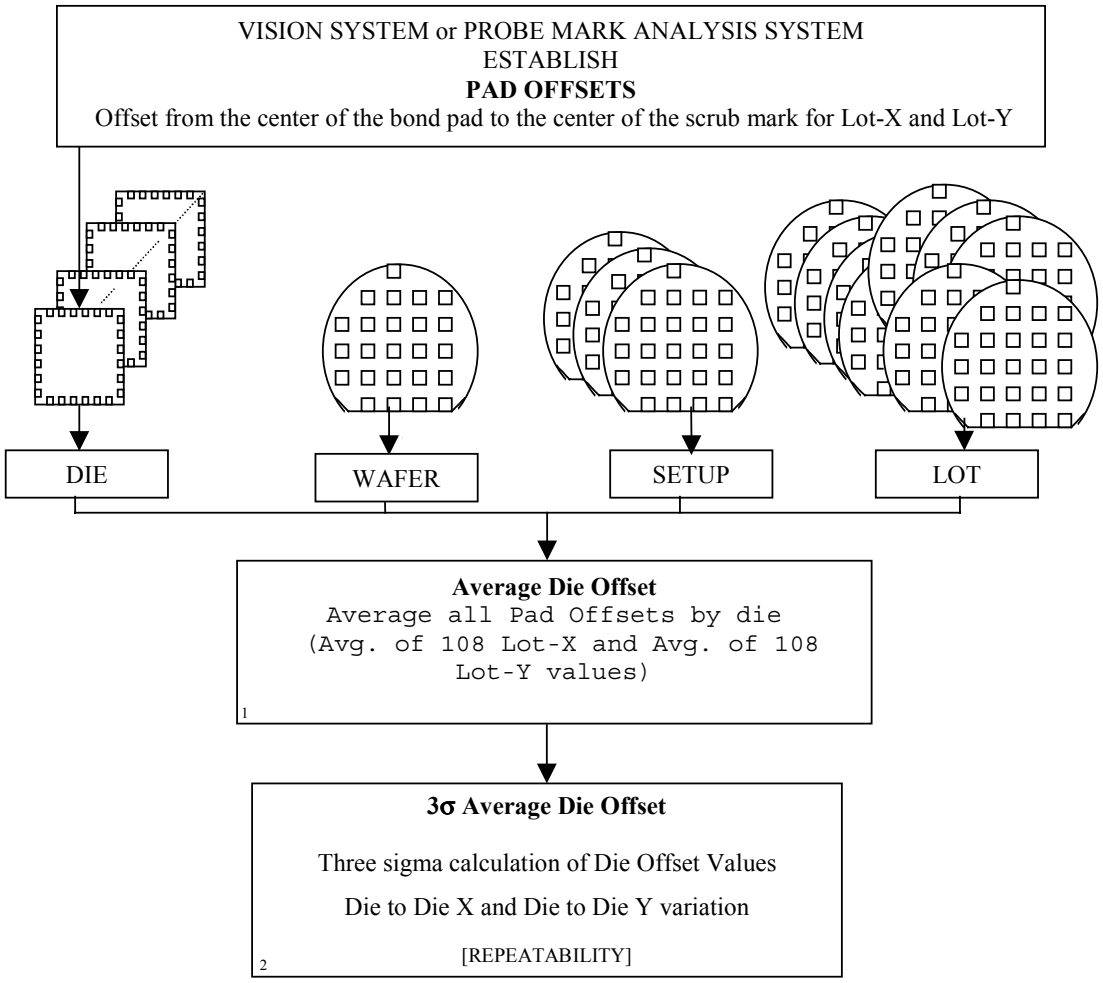

Figure 5

Pad Offset and Two-Step Analysis Algorithm for Determining Probe System Error

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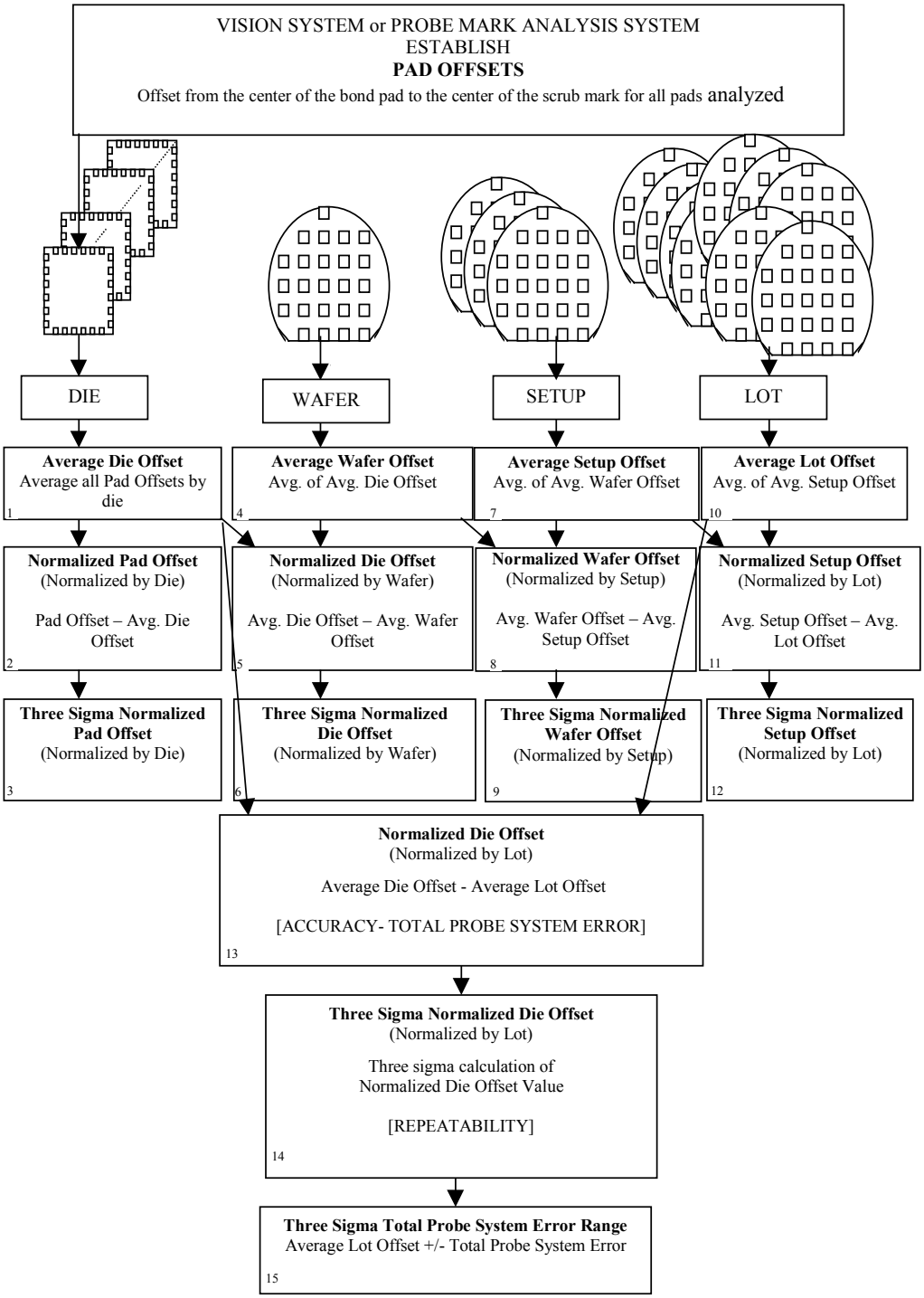

Figure 6

Pad Offsets and 15-Step Analysis Algorithm for Determining Probe System Error

7 Required Hardware Checklist (see Figure 7)

- Wafer prober (if the test plan includes either hot or cold chuck testing, the prober must be appropriately equipped).
- A planarized and aligned probe card which matches the selected wafers, accompanied by a metrology tool printout of the 'x', 'y' and 'z' positions of all of the probe tips to be used for probe mark analysis. Note: The probe card should be measured for alignment, but not "tweaked", immediately prior to and after the conclusion of each subsequent test.
- Untested wafers
- A special "test program" with a fixed "test" time.
- Tester or PC that will run the "test program". If a PC is used to simulate the tester, it must be equipped with the appropriate hardware for communication with the wafer prober.
- A stopwatch, with 0.1 second resolution. The stopwatch is to have "split" capability.

  Note that the user of this method may choose at their discretion to utilize any other time stamp logging technology at their disposal, so long as the computational overhead of this logging has no effect upon the throughput of the prober.

8 Requirements (see Figure 7)

8.1 *Qualified Prober* — Before initiating the test process, the wafer prober is to be certified by a representative of the prober manufacturer to be fully operational.

8.2 *Qualified Personnel* — The individual running the wafer prober for the test procedure must be certified or otherwise qualified to operate the prober being tested.

9 Test conditions (see Figure 7)

9.1 *Test Time* — a fixed "device test time" will be used during these tests. The recommended value for this test time is 1.0 seconds.

9.2 *Accuracy and Repeatability vs. Throughput* — The person or manufacturer running this test may make a choice (or choices) as to how they elect to balance accuracy and repeatability with throughput, but all three tests must be run simultaneously. This will generate a set of numbers defining a particular prober's accuracy and repeatability at a given throughput (or a throughput at a given accuracy and repeatability). All adjustments to the prober are to be made using standard, end-user-adjustable settings, and all prober settings associated with a particular throughput / accuracy and repeatability combination are to be included in the final report.

9.3 *Temperature* — This test can be conducted at any temperature, however, numerous variable can distort the results if run at a temperature other than ambient, i.e. probe tip drift due to an increase or decrease in temperature.

- *Cautionary Note: If the tests are performed at temperatures other than ambient, the user must use the same probe card and wafer type for all tests across all test platforms to ensure uniformity of results.*

9.4 *Probe Card Type* — All types of probe cards (blade, peripheral / cantilever or vertical) may be used, so long as they leave a visible scrub mark.

- *Cautionary note: Some vertical probe cards exhibit an inherent amount of 'x' - 'y' needle drift. The user should verify the intrinsic repeatability of the probe card before using it to characterize the prober.*

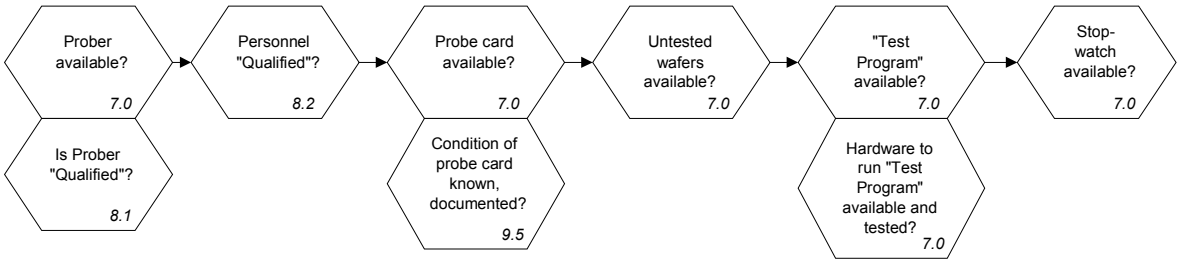

Figure 7

Preparation

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9.5 *Probe Card Condition* — a metrology tool printout verifying the 'x', 'y' and 'z' position of each probe is within the users specification must accompany the probe card.

9.6 *Tester – Prober Communications* — The type of communications method used between the prober and the tester is left up to the user of this test method. Because communication overhead varies with protocol, the same hardware and "test program" (modified as necessary to communicate to the prober under test) must be used for all tests.

9.7 *Presence of the PTI* — During the test, the probe card must have loading similar to that applied by the normal "in use" application such as a Probe Test Interface (PTI) or Direct Docking Pogo Stack. The force exerted on the probe card by the PTI will stabilize the probe card, improving the repeatability of the data collected.

9.8 *Wafer Cassette* — For the purposes of these tests, a cassette of wafers is defined as containing ten wafers. Ensure the wafers are placed in the same slots for each test.

10 Test Procedure (see Figures 8 and 9)

10.1 Load wafer cassette

10.2 Install probe card

10.3 Set probe mode to serpentine, set all other necessary prober parameters. NOTE THAT ALL DIE ON ALL WAFERS ARE TO BE "TESTED", NOT JUST THE 12 DIE FROM WHICH PROBE MARK DATA WILL BE ANALYZED.

10.4 Note all applicable parameters (see chart below)

10.5 If temperature testing, soak for a user-defined time (consistent with the user's test methodologies) that is equal on all corresponding tests on all probers being evaluated.

10.6 Start probing process and stopwatch simultaneously.

10.7 The "test program" must perform automatic alignment of the probe card to the wafer prior to wafer #'s 1, 2, 5, and 8.

NOTE: While not required, it is recommended that the PTI and Probe Card be removed and re-installed prior to each of the automatic alignment steps to simulate whatever locational error might be induced by manipulation of the interface and the probe card.

10.8 Record times of individual events (utilizing the stopwatch's "split" function) on the supplied chart or a similar form.

10.9 When the last wafer is finished and has been returned to wafer cassette, stop the stopwatch.

10.10 Collect the probe mark offset data from wafers.

10.11 Calculate Normalized (by lot) Die Offset [Accuracy] and 3σ of Normalized (by lot) Die Offset [Repeatability]:

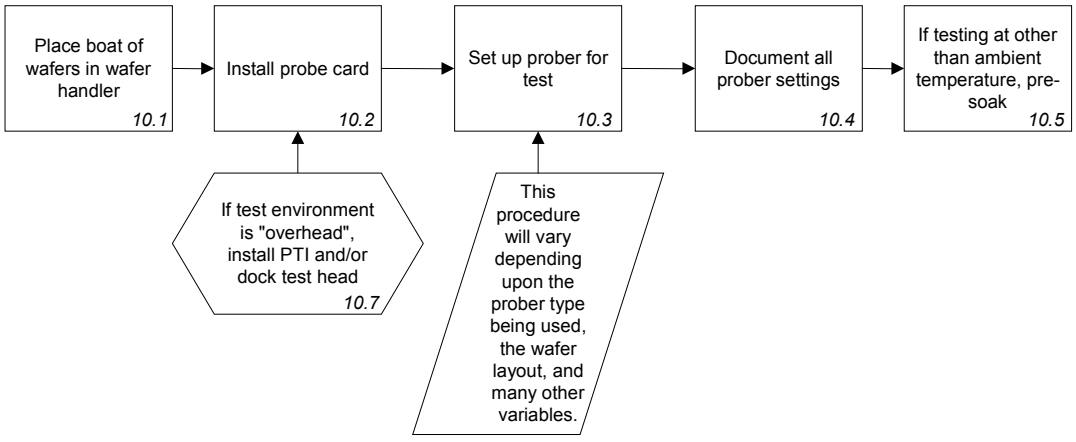

Figure 8

Setup

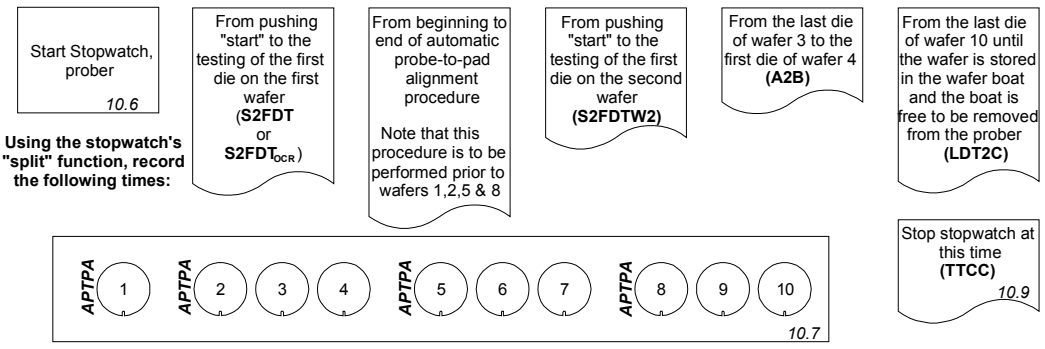

Figure 9

Timing Procedure

11 Introduction

11.1 The Probe Mark Analysis System recognizes the edge of the bond pad passivation opening and the probe mark, draws a best-fit rectangle around the probe mark and passivation opening, and returns the four distances, Left, Right, Bottom and Top to a text file. The center position of the best-fit rectangle can be used to represent the center of the scrub mark. An offset of this center of scrub mark from the center of the bond pad can be calculated as follows:

$$PadXoffset = (Left - Right)/2$$
$$PadYoffset = (Bottom - Top)/2 \qquad (1)$$

The variation of this offset from pad to pad, die to die, wafer to wafer and setup to setup captures most of the process variations.

11.2 *PMA Data Analysis*

11.2.1 We will use a sampling scheme of 9 wafers per lot, (3 setups per lot, 3 wafers per setup), 12 dies per wafer and 24 pads per die as an example for discussing the data analysis algorithm. The first step of doing data analysis is to obtain the offsets for all the pads that have been sampled using Eqn.(1). This means that the offsets

$$[\text{PadXoffset}]\, xoff_{loti,setj,wafk,diel,padm},\ [\text{PadYoffset}]\, yoff_{loti,setj,wafk,diel,padm} \qquad (2)$$

for a pad m on die l, wafer k, under setup j in lot i are known.

Step 1

Calculate ***Average Die Offset*** for the lot [LOTX or LOTY] (3)

$$xoff_{loti,setj,wafk,diel} = \frac{1}{12}\sum_{m=1}^{12} xoff_{loti,setj,wafk,diel,padm}$$
$$yoff_{loti,setj,wafk,diel} = \frac{1}{12}\sum_{m=1}^{12} yoff_{loti,setj,wafk,diel,padm} \qquad (3)$$

Step 2

Calculate D-D-X or D-D-Y = 3σ of ***Average Die Offset*** **[LOTX] and [LOTY]**(3)

These die offsets are again treated on the equal basis. A 3σ value is calculated and becomes our Die-to-Die Variation (D-D-X, D-D-Y) for the entire lot.

LOTX + D-D-X, LOTX - D-D-X = Total Prober X-Error Range (3σ)
LOTY + D-D-Y, LOTY - D-D-Y = Total Prober Y-Error Range (3σ)

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Suggested Graphs for X-Offset and Y-Offset (see Appendix 1 for examples):

X-Offset	**Y-Offset**
LOTX + D-D-X	LOTY + D-D-Y
LOTX	LOTY
LOTX - D-D-X	LOTY - D-D-Y
Average Die X-Offset (3)	Average Die Y-Offset (3)

12 Data Collection Table

12.1 The following data are to be recorded about the test environment:

Title	*Description*	*Values*	
Tester - Prober Interface	Installed (Yes/No)		
	If installed, Total Pogo® pin force (nominal, calculated)		kg
			pounds
Tester	Present [docked] (Yes/No)		
	If present, state manufacturer and model		
Wafer	Nominal Die Size (Small, Medium or Large)		
Probe Card	Needle count		
	Nominal force per needle		grams
			ounces
	Diameter of needle tip		microns
			mils
	Needle pitch (within a single row or column)		microns
			mils
	Number of needle tiers		
	Size of needle array in the X direction (left-to-right when facing prober (from the operator position))		mm
			inches
	Size of needle array in the Y direction (away and towards the operator relative to the center of the probe card)		mm
			inches
	Diameter of probe card		mm
			inches
Test Temperature	Set point / Temperature of chuck during test		ºC
			ºF
	Soak time, probe card (if test temperature is other than ambient)		minutes
	Soak time, prober (if other than ambient)		minutes

Title	*Description*	*Values*	
DUT spacing	X-direction		microns
			mils
	Y-direction		microns
			mils
Z clearance			microns
			mils
Overdrive			microns
			mils
Tester-Prober communications method			
OCR Variables	OCR on? (Y/N)		
	SEMI standard font? (Y/N)		
	# of retries allowed		

Definitions for formulae:

Variable	*Description*	*Values*	
DPW	Die Per Wafer		
TT	Test Time (minimum value of 1.0 seconds)		seconds

Data Collected	*Description*	*Values*	
A2B	Last die (Wafer A) to first die (Wafer B) time		seconds
S2FDT	Time from pushing "Start" to First Die Test with OCR turned off		seconds
$S2FDT_{OCR}$	Time from pushing "Start" to First Die Test with OCR turned on		seconds
S2FDTW2	Time from pushing “Start” to First Die Test, Wafer #2		seconds
LDT2C	Time from end of Last Die Test to Cassette free to remove from prober		seconds
TTCT	Total Time to Complete Test		seconds
TTAA	Time To Auto-Align the probe needles with the die bonding pads		seconds

$$D2D = \frac{TTCT - (TT \times DPW \times 9) - (A2B \times 8) - S2FDTW2 - LDT2C \; - \; (TTAA \times 3)}{DPW \times 9}$$

Calculated Results	*Values*	
D2D		seconds

APPENDIX 1
CALCULATION OF NORMALIZED DIE OFFSET AND TOTAL PROBER ERROR RANGE (3σ)

A1-1 Probe Mark Data Analysis Algorithm:

A1-1.1 *Introduction*

A1-1.1.1 The Probe Mark Analysis system recognizes the edge of the bond pad passivation opening and the probe mark, draws a best-fit rectangle around the probe mark and passivation opening, and returns the four distances, Left, Right, Bottom and Top to a text file. The center position of the best-fit rectangle can be used to represent the center of the scrub mark. An offset of this center of scrub mark from the center of the bond pad can be calculated as follows:

$$PadXoffset = (Left - Right)/2$$
$$PadYoffset = (Bottom - Top)/2 \quad (1)$$

A1-1.1.2 The variation of this offset from pad to pad, die to die, wafer to wafer and setup to setup captures most of the process variations.

A1-1.2 *PMA Data Analysis*

A1-1.2.1 We will use a sampling scheme of 9 wafers per lot, (3 setups per lot, 3 wafers per setup), 12 die per wafer and 24 pads per die. The first step of doing data analysis is to obtain the offsets for all the pads that have been sampled using Eqn.(1). This means that the offsets

$$[\text{PadXoffset}]\, xoff_{loti,setj,wafk,diel,padm},\ [\text{PadYoffset}]\, yoff_{loti,setj,wafk,diel,padm} \quad (2)$$

for a pad m on die l, wafer k, under setup j in lot i are known.

A1-1.3 Step 1 — Calculate Average Die Offset (3)

$$xoff_{loti,setj,wafk,diel} = \frac{1}{12}\sum_{m=1}^{12} xoff_{loti,setj,wafk,diel,padm}$$
$$yoff_{loti,setj,wafk,diel} = \frac{1}{12}\sum_{m=1}^{12} yoff_{loti,setj,wafk,diel,padm} \quad (3)$$

A1-1.3.1 *Discussion of Average Die Offset*

A1-1.3.1.1 Based on the sample described, there will be an Average Die Offset-X and Average Die Offset Y for each of the 108 die sampled. This value is probably the most descriptive, especially when graphed (see example graphs). Both X and Y-graphs will most likely resemble a sine wave. This is due to wafer rotation. As you serpentine across the wafer there will be a slight offset from die to die. Since the selected sample dice are in the center and around the edges of the wafer, you can see the progression of the offset as you move farther from the center of the wafer. The X and Y graphs are usually about 90º out of phase.

A1-1.3.1.2 Other qualitative information can also be gathered by visually looking at the graphs of this data. One can determine whether the accuracy is varying wafer to wafer (each set of 12 data points is a wafer) or set-up to set-up (each set of 36 data points is a set-up) or just drifting over time. Drift over time is sometimes caused by temperature stabilization issues within the prober mechanism. Subsequent steps will quantify how much variability is caused by each.

A1-1.4 Step 2 — Calculate Normalized (by die) Pad Offset (4) = (2) - Average Die Offset (3)

$$xnorm_{loti,setj,wafk,diel,padm} = xoff_{loti,setj,wafk,diel,padm} - xoff_{loti,setj,wafk,diel}$$
$$ynorm_{loti,setj,wafk,diel,padm} = yoff_{loti,setj,wafk,diel,padm} - yoff_{loti,setj,wafk,diel} \quad (4)$$

A1-1.4.1 *Discussion of Normalized (by die) Pad Offset*

A1-1.4.1.1 This step helps to quantify how much error is caused by the prober vs. the probe card. The probe card usually does NOT impact average offset of a die, just the variability within a die. In this equation, we subtract the average die offset (presumed prober error) from each pad in that die. This data is then used for the next step.

A1-1.5 Step 3 — Calculate P-P-X or P-P-Y = 3σ of Normalized (by die) Pad Offset (4).

A1-1.5.1 All the normalized pad offsets in the same lot (no matter on which die, on which wafer the pad resides) are treated on an equal basis. In our example, a total of 2592 pads are sampled in a lot. All 1296 x-direction and 1296 y-direction pads of ***Normalized (by die) Pad Offset*** will be used to calculate a 3σ variation which is called Pad-to-Pad variation (P-P-X and P-P-Y).

A1-1.5.2 *Discussion of P-P-X or P-P-Y (Pad-to-Pad Variation in the X-direction or Pad-to-Pad-Variation in the Y-direction)*

A1-1.5.2.1 These values describe how much variability there is within all the pads in the lot. This value is frequently attributed to probe tip variation in X, Y, and Z. Although probe tips do change and wear over time, their unloaded position usually does not change dramatically within one lot. This value does not help tremendously in describing prober accuracy nor should it be used for any sort of probecard metrology. However, be sure to perform a mental reality check to verify that it is somewhere near (within an order of magnitude of) your probe card X/Y probe needle position specification.

A1-1.6 Step 4 — Calculate Average Wafer Offset (5) = average of Average Die Offset (3).

$$xoff_{loti,setj,wafk} = \frac{1}{12}\sum_{l=1}^{12} xoff_{loti,setj,wafk,diel}$$
$$yoff_{loti,setj,wafk} = \frac{1}{12}\sum_{l=1}^{12} yoff_{loti,setj,wafk,diel} \quad (5)$$

A1-1.6.1 *Discussion of Average Wafer Offset*

A1-1.6.1.1 This equation will result in nine values for Average Wafer Offset-X and nine for Average Wafer Offset-Y. These numbers could also be graphed to look for trends from wafer to wafer (this is not included on the example graphs). If there is a consistent trend in one direction possible causes are:

- wafer loading error
- cumulative stepping error, and
- temperature stability errors

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A1-1.7 Step 5 — Calculate Normalized (by wafer) Die Offset (6) = Average Die Offset (3) - Average Wafer Offset (5)

$$xnorm_{loti,setj,wafk,diel} = xoff_{loti,setj,wafk,diel} - xoff_{loti,setj,wafk}$$
$$ynorm_{loti,setj,wafk,diel} = yoff_{loti,setj,wafk,diel} - yoff_{loti,setj,wafk} \quad (6)$$

A1-1.7.1 *Discussion of Normalized (by wafer) Die Offset*

A1-1.7.1.1 This normalization step is a precursor to calculating a 3σ variation value. To calculate the true Die-to-Die variation, any wafer-to-wafer induced error is subtracted out from the by-die-data. This data is used in the next step.

A1-1.8 Step 6 — Calculate D-D-X or D-D-Y = 3σ of Normalized (by wafer) Die Offset (6)

A1-1.8.1 These normalized die offsets are again treated on the equal basis. A 3σ value is calculated and becomes our Die-to-Die Variation (D-D-X, D-D-Y).

A1-1.8.2 *Discussion of D-D-X or D-D-Y (Die-to-Die 3σ variation in the X-direction, Die-to-Die 3σ variation in the Y-direction)*

A1-1.8.2.1 This equation will result in the 3σ variation of the average die offsets from Die-to-Die in both X- and Y-directions. If this number is very large, there should be concern about the repeatability of the prober.

A1-1.9 Step 7 — Calculate Average Setup Offset (7)

$$xoff_{loti,setj} = \frac{1}{3}\sum_{k=1}^{3} xoff_{loti,setj,wafk}$$
$$yoff_{loti,setj} = \frac{1}{3}\sum_{k=1}^{3} yoff_{loti,setj,wafk} \quad (7)$$

A1-1.9.1 *Discussion of Average Setup Offset*

A1-1.9.1.1 These equations will produce six values, three for Average- (by Setup) Offset-in-the-X-direction and three for Average- (by Setup) Offset-in-the-Y-direction. These values describe the average offset of all of the die "tested" with a particular setup.

A1-1.10 Step 8 — Calculate a Normalized (by setup) Wafer Offset (8) = Average Wafer Offset (5) - Average Setup Offset (7).

$$xnorm_{loti,setj,wafk} = xoff_{loti,setj,wafk} - xoff_{loti,setj}$$
$$ynorm_{loti,setj,wafk} = yoff_{loti,setj,wafk} - yoff_{loti,setj} \quad (8)$$

A1-1.10.1 *Discussion of Normalized (by setup) Wafer Offset*

A1-1.10.1.1 A normalizing step to help calculate the true wafer-to-wafer variation.

A1-1.11 Step 9 — Calculate W-W-X or W-W-Y = 3σ of Normalized (by setup) Wafer Offset (8).

A1-1.11.1 A 3σ variation will be calculated based on the normalized wafer offset and will be cited as the Wafer-to-Wafer variation (W-W-X, W-W-Y).

A1-1.11.2 *Discusssion of W-W-X or W-W-Y (Wafer-to-Wafer variation in the X-direction, Wafer-to-Wafer variation in the Y-direction)*

A1-1.11.2.1 This equation will produce a value for the 3σ variation from Wafer-to-Wafer in the X and Y directions. If this number were large, it would tend to indicate that the prober does not behave repeatably from wafer-to-wafer. Possible causes are:

- loading problems
- temperature stability issues, and
- wafer rotation issues

A1-1.12 Step 10 — Calculate Average Lot Offset (9) = average of Average Setup Offset (7).

$$LOTX = \frac{1}{3}\sum_{j=1}^{3} xoff_{loti,setj}$$
$$LOTY = \frac{1}{3}\sum_{j=1}^{3} yoff_{loti,setj} \qquad (9)$$

A1-1.12.1 *Discussion of Average Lot Offset (LOTX or LOTY)*

A1-1.12.1.1 This will be one of the values added to the graph. This is simply the average of all of the average die offsets in the X-direction and all of the average die offsets in the Y-direction. If one needed to pick a single number in X and Y to describe the accuracy of the prober – this is the one. This can be very misleading though – what this number really tells you is what value the distribution is centered around. Refer to the graph to get a visual sense of this data.

A1-1.13 Step 11 — Calculate Normalized (by lot) Setup Offset (10) = Average Setup Offset (7) - Average Lot Offset (9)

$$xnorm_{loti,setj} = xoff_{loti,setj} - LOTX$$
$$ynorm_{loti,setj} = yoff_{loti,setj} - LOTY \qquad (10)$$

A1-1.13.1 *Discussion of Normalized (by lot) Setup Offset*

A1-1.13.1.1 This is another normalization step used to calculate the true setup-to-setup error in X and Y.

A1-1.14 Step 12 — Calculate S-S-X or S-S-Y = 3σ of Normalized (by lot) Setup Offset (10).

A1-1.14.1 A 3σ variation will be calculated based on the normalized setup offset and will be cited as the Setup-to-Setup variation (S-S-X, S-S-Y).

A1-1.14.2 *Discussion of S-S-X or S-S-Y (Setup-to-Setup variability in the X-direction, Setup-to-Setup variability in the Y-direction)*

A1-1.14.2.1 These two values describe how much variability there is between setups.

A1-1.15 Step 13 — Calculate Normalized (by lot) Die Offset (11) = Average Die Offset (3) - Average Lot Offset (9) [Accuracy]

$$xn_{loti,setj,wafk,diel} = xoff_{loti,setj,wafk,diel} - LOTX$$
$$yn_{loti,setj,wafk,diel} = yoff_{loti,setj,wafk,diel} - LOTY \quad (11)$$

A1-1.15.1 *Discussion of Normalized (by lot) Die Offset*

A1-1.15.1.1 This step is useful if you need to compare the variation between several different lots. It is not completely necessary for the next step, since subtracting a constant from a string of numbers does not change the 3σ variation, only the center point.

A1-1.16 Step 14 — Calculate TTLX or TTLY = 3σ of Normalized (by lot) Die Offset (11) [Repeatability]

A1-1.16.1 *Discussion fo TTLX or TTLY*

A1-1.16.1.1 This is the value for determining (with 3σ confidence) whether your probe marks will always fall within your desired spec. They are the hatch-marked lines.

A1-1.17 Step 15 — This normalized die offset includes Die-to-Die, Wafer-to-Wafer, and Setup-to-Setup offsets thus a 3σ variation of this offset will be called Total Prober Variation (TTLX and TTLY).

A1-1.17.1 *Calculate Total Prober Error Range (3σ).*

LOTX + TTLX, LOTX - TTLX = Total Prober X-Error Range (3σ)
LOTY + TTLY, LOTY - TTLY = Total Prober Y-Error Range (3σ)

A1-1.17.2 Suggested Graphs:

X-Offset	Y-Offset
LOTX + TTLX	LOTY + TTLY
LOTX	LOTY
LOTX - TTLX	LOTY - TTLY
Average Die X-Offset (3)	Average Die Y-Offset (3)

A1-1.17.2.1 It is recommended to create one graph illustrating the prober accuracy in X and one graph for Y.

A1-1.18 *Discussion of Graphs (one example for X [Figure X] and one for Y [Figure Y])*

A1-1.18.1 Average Lot X-Offset is the value from Step 10. This number shows where the probe mark distribution is centered (the accuracy of the prober).

A1-1.18.2 Average Lot X-Offset +3σ is the result from step 10 + the result from step 14

A1-1.18.3 Average Lot X-Offset -3σ is the result from step 10 – the result from step 14

A1-1.18.4 These two lines show the ± 3σ range of your distribution. This describes the repeatability of the prober.

NOTE: There will always be explainable and unexplainable accuracy and repeatability errors on a prober. If these two lines fall within your desired specification, you will probably not have any problems. The example graph for X-offset illustrates a well-behaved, or "passing" prober. The example graph for Y-offset, on the other hand, is representative of a prober which failed to meet the desired accuracy specification.

A1-1.18.5 The upper and lower desired specification limits have been added to the graphs.

A1-1.18.6 The final piece of data added to the graph is the Average Die Offset. This, as stated in Step 1, is very good at illustrating any trends throughout the lot.

A1-1.18.7 Tips for graph making:

- Add gridlines across the X-axis to separate wafers.
- Print all graphs (X and Y, different lots, different probers) with the same scale in X and Y.
- Add a legend to your graphs, so that they will be readable by your "audience" as well as yourself.

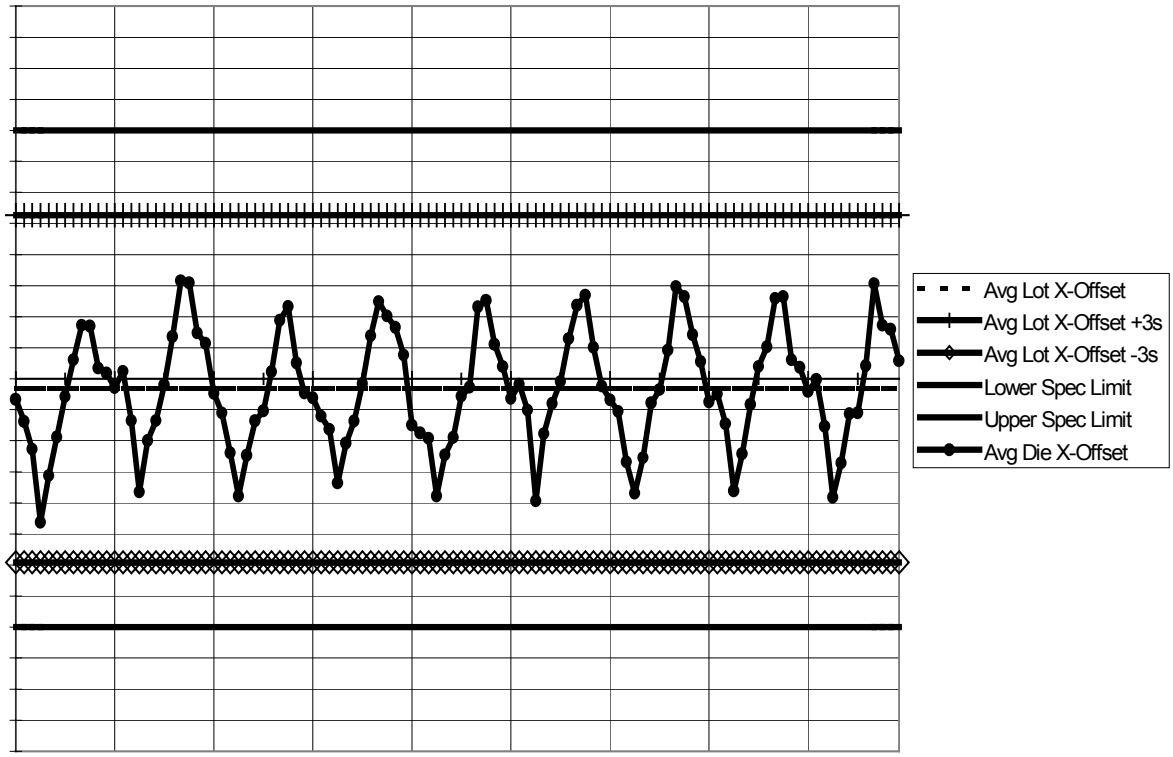

Figure 7

X-Offset

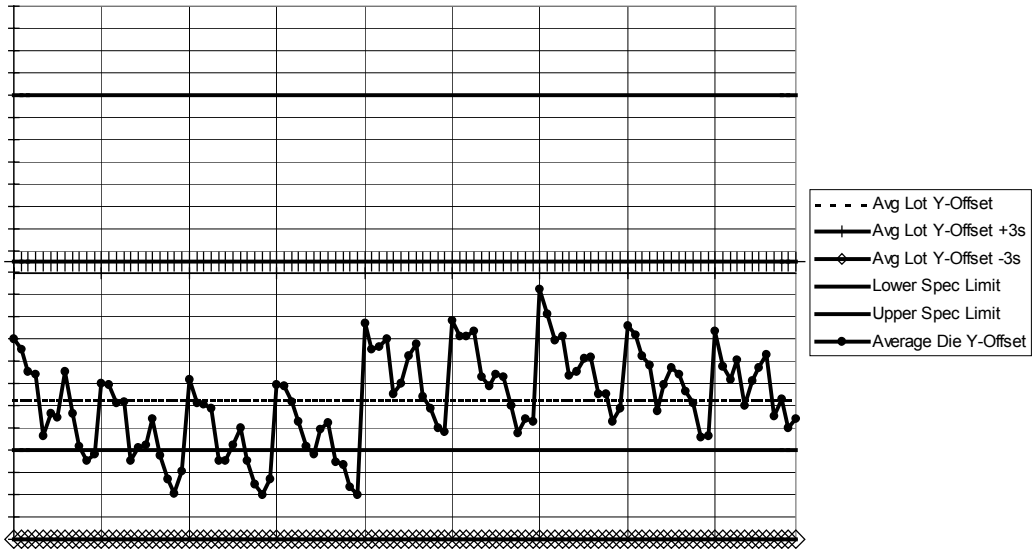

Figure 8

Y-Offset

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SEMI G79-0200
SPECIFICATION FOR OVERALL DIGITAL TIMING ACCURACY

This specification was technically approved by the Global Automated Test Equipment Committee and is the direct responsibility of the North American Automated Test Equipment Committee. Current edition approved by the North American Regional Standards Committee on September 3, 1999. Initially available at www.semi.org November 1999; to be published February 2000.

1 Purpose

1.1 This standard is intended to provide a minimum common definition of timing accuracy specifications for automatic semiconductor test equipment (ATE).

2 Scope

2.1 The scope of this standard includes all semiconductor ATE capable of digital functional testing. This standard does not include the following:

- test fixturing errors,
- device insertion errors, and
- ATE performance or capability beyond timing accuracy.

2.2 This standard's overall timing accuracy (OTA) definition serves to simplify automatic test equipment comparisons and reduce specification ambiguity.

2.3 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Limitations

3.1 Parameters associated with the following items are not covered by the Overall Digital Timing Accuracy Specification:

- minimum driver pulse width,
- comparator bandwidth,
- I/O round trip delay,
- test fixturing errors,
- device insertion errors,
- time measurement unit accuracy, and
- ATE capability or performance beyond timing accuracy.

4 Referenced Standards

None.

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *ATE* — automatic test equipment

5.1.2 *DUT* — device under test

5.1.3 *NR* — Non-return signal format

5.1.4 *RTx* — return to zero, one or complement signal format.

5.1.5 *SBx* — surround by zero, one or complement signal format.

5.1.6 *Z* — driver off (high impedance)

5.2 *Definitions*

5.2.1 *device insertion errors* — error influenced by device-input capacitance and/or terminations.

5.2.2 *edge* — time delay created by an ATE delay generation resource.

5.2.3 *performance board* — printed circuit board used to interface the tester channels to the device under test.

5.2.4 *pin* — tester channel

5.2.5 *reference load A* — 500 ohms in parallel with 2.5pf (± 0.5pf) to ground

5.2.6 *reference load B* — 50 ohms to ground

5.2.7 *reference load C* —

- 50 ohms to low (for driver z to high and high to z transitions).
- 50 ohms to high (for driver z to low and low to z transitions).

5.2.8 *strobe compare* — monitor DUT output at a single time point.

5.2.9 *test cycle* — inverse of test pattern execution frequency.

5.2.10 *test fixturing errors* — error influenced by mismatched signal path lengths, impedance discontinuities, lumped capacitance/inductance elements, and high frequency loss due to skin effect or interconnects.

5.2.11 *window compare* — monitor DUT continuously during a time interval.

NOTE 1: The term "input" as it appears in this document refers to the device under test.

6 Test Methods

6.1 See Figure 1.

NOTE 2: A verification procedure to complement this Overall Digital Timing Accuracy Specification is currently being developed as a SEMI draft document.

6.2 *Explanation of Figure 1* — This figure is meant to graphically describe Overall Timing Accuracy and its constituent components. Overall Timing Accuracy (OTA) is made up of three components, and by definition is the aggregate timing error comprised of input edge placement accuracy (see Section 7.1.1), output edge placement accuracy (see Section 7.1.2), and input to output timing accuracy (see Section 7.1.3). It's important to note that the OTA specification and associated graphical representation shown in Figure 1 is meant to encompass timing delay errors across multiple machines, as well as multiple calibrations for a single machine over time.

6.2.1 Our experience in dealing with multiple-pin automated test systems reveals that not all input drive circuits can place a drive edge at exactly the same point in time relative to a common reference. The same is true for output compare circuits when placing compare edges. Thus, these edges tend to have an (error) distribution around some average value relative to their intended placement. This is due in part to the inherent anomalies associated with electronic circuits that make-up these edge placement elements. The distribution of edge error is graphically shown for input (see Section 7.1.1) and output edge (see Section 7.1.2) signals in Figure 1.

6.2.2 Drive Input to Compare Output Timing Accuracy (Section 7.1.3) can be described in different ways. It is easy to think of this parameter, per the definition given in this document, Section 7.1.3, as simply the relative time difference (skew) between the drive delay timing error distribution and the compare delay timing error distribution for a particular machine. But this parameter, once established for a machine, is not necessarily constant. For example, this parameter can change from one calibration of a machine at a particular time, to something different, as a result of a subsequent calibration of that same machine. As well, this parameter can also be considered as a machine to machine accuracy parameter, not necessarily having the same value between any two machines of the same kind.

6.2.3 Thus, on each machine and at different points in time for the same machine the Drive Input to Compare Output Timing skew can be uniquely different per machine. That difference being influenced by the various machine anomalies that contribute to machine error including the not so perfect results of a periodic edge calibration.

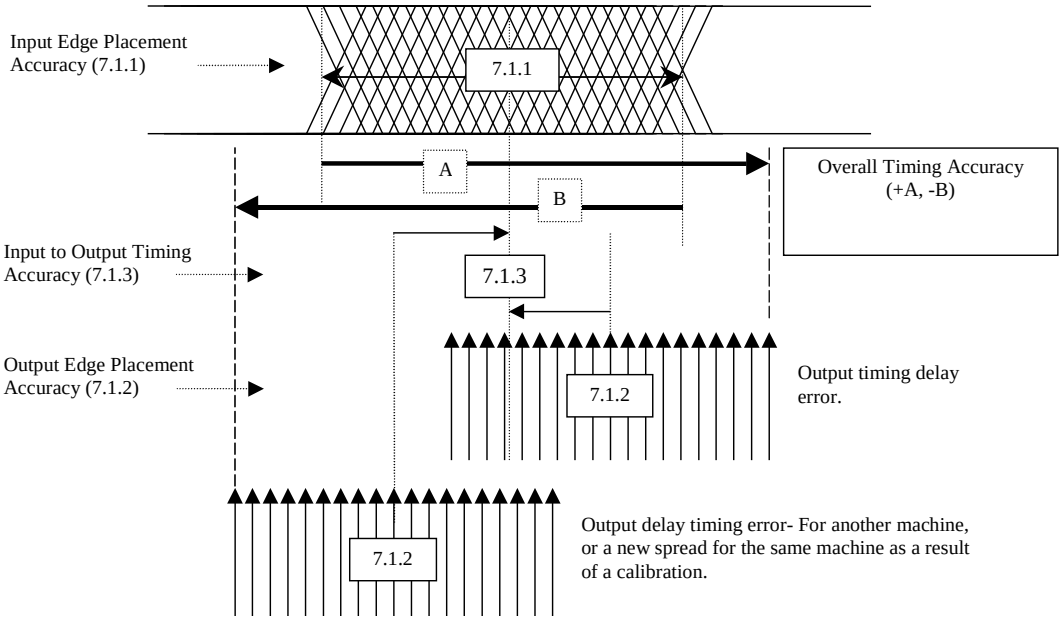

Figure 1
Overall Timing Accuracy

6.2.4 Examination of the OTA definition in the context of Figure 1, that being the general case and not a single point timing evaluation, reveals that the overall timing accuracy time value is the time line indicated by "A" and the time line indicated by "B". In a single point AC timing evaluation, OTA is determined as a distribution of edges associated with time line "A" or time line "B", depending upon the relationship between the drive edge values and compare edge values (see Section 7.1.3) at that point in time.

7 Definitions

7.1 *Overall Timing Accuracy* — aggregate timing error comprised of input edge placement accuracy, output edge placement accuracy and input to output timing accuracy. (See Figure 1.)

7.1.1 *Input Edge Placement Accuracy* — DUT input timing error comprised of input timing delay error, input timing jitter and input transition time variation.

7.1.1.1 *Input Timing Delay Error @ 5V* — time delay error at the midpoint of a 5V transition, with respect to an ideal delay (NIST traceable delay reference), using any pin, any delay value, any input timing edge, any format (NR, Rtx, SBx), positive or negative transition and any test cycle length.

Conditions:

- delays are normalized to pin 1 (first tester pin), rising edge, NR format, @ 0ns;
- errors are normalized to the average of minimum and maximum of the error distribution;[1]
- reference load A; and
- physical reference point is a zero length interconnect on the DUT side of a standard performance board.

7.1.1.2 *Input Timing Delay Error @ 3V* — (same as Section 7.1.1.1 @ 3V)

7.1.1.3 *Input Timing Delay Error @ 1V* — (same as Section 7.1.1.1 @ 1V)

7.1.1.4 *Input Timing Jitter* — short term (cycle to cycle) instability using any pin, any input timing edge, any format (NR, RTx, SBx).

Conditions:

- error expressed as RMS value;
- reference load B;
- physical reference point is a zero length interconnect on the DUT side of a standard performance board; and
- error referenced to corresponding transition of prior cycle.

7.1.1.5 *Input Transition Time Variation @ 5V* — minimum and maximum rise and fall times of a 5V input signal transition using any pin.

Conditions:

- referenced to the time variation between the 20% and 80% points of both positive and negative signal transitions;
- reference load A; and
- physical reference point is a zero length interconnect on the DUT side of a standard performance board.

7.1.1.6 *Input Transition Time Variation @ 3V* — (same as Section 7.1.1.5 @ 3V)

7.1.1.7 *Input Transition Time Variation @ 1V* — (same as Section 7.1.1.5 @ 1V)

7.1.2 *Output Edge Placement Accuracy* — DUT output compare timing error comprised of output timing delay error and output compare timing jitter.

7.1.2.1 *Output Timing Delay Error @ 5V* — time delay error at the detected midpoint of a 5V transition, with respect to an ideal delay (NIST traceable reference), using any pin, any delay value, any compare timing edge, window or strobe compare mode, expect H or L, positive or negative transition and any test cycle length.

Conditions:

- measured with load circuit "off" or high impedance;
- delays normalized to rising edge detected by pin 1 (first tester pin), using strobe compare format, expect H @ 0ns;
- error normalized to the average of minimum and maximum of the error distribution; and
- input signal: 50-ohm source, 0–5V step, > 1V/ns, inserted at a zero length interconnect on the DUT side of a standard performance board.

7.1.2.2 *Output Timing Delay Error @ 3V*— (same as Section 7.1.2.1 using 3V input signal)

7.1.2.3 *Output Timing Delay Error @ 1V* — (same as Section 7.1.2.1 using 1V input signal)

1 "Average of min and max of the error distribution" is defined as: (min error + max error)/2. This can also be referred to as "center of spread".

7.1.2.4 *Output Timing Jitter*— short term (cycle to cycle) instability using any pin, any compare timing edge, window or strobe compare mode, expect H or L.

Conditions:

- error expressed as RMS value;
- physical reference point is a zero length interconnect on the DUT side of a standard performance board; and
- jitter referenced to an independent synchronous trigger.

7.1.3 *Input to Output Timing Accuracy* — relative time difference between the average of minimum and maximum drive input delay timing and the average of minimum and maximum compare output delay timing.

7.1.3.1 *Input to Output Timing Error @ 5V* — relative time difference between the average of minimum and maximum input delay timing error @ 5V (Section 7.1.1.1) and the average of minimum and maximum output timing delay error @ 5V (Section 7.1.2.1).

Conditions:

- (same as Sections 7.1.1.1 and 7.1.2.1).

7.1.3.2 *Input to Output Timing Error @ 3V* — same as Section 7.1.3.1 using 3V input signal and definitions/ conditions specified in Sections 7.1.1.2 and 7.1.2.2.

7.1.3.3 *Input to Output Timing Error @ 1V* — same as Section 7.1.3.1 using 1V input signal and definitions/ conditions specified in Sections 7.1.1.3 and 7.1.2.3.

7.1.4 *High Speed Clock Accuracy* — DUT high speed clock input timing error (if different than normal tester input channels) comprised of high speed clock delay error, high speed clock self-trigger cycle jitter, high speed clock self-trigger phase jitter and high speed clock transition time variation.

7.1.4.1 *High Speed Clock Delay Error @ 5V* — time delay at the midpoint of a 5V transition, with respect to an ideal delay (NIST traceable delay reference), using any pin, any delay value, any input timing edge, RTZ format, and any test cycle length.

Conditions:

- delays are normalized to pin 1 (first tester pin), rising edge, NR format, @ 0ns;
- errors are normalized to the average of minimum and maximum of the error distribution;
- reference load A; and
- physical reference point is a zero length interconnect on the DUT side of a standard performance board.

7.1.4.2 *High Speed Clock Delay Error @ 3V* — (same as Section 7.1.4.1 @ 3V)

7.1.4.3 *High Speed Clock Delay Error @ 1V* — (same as 7.1.4.1 @ 1V)

7.1.4.4 *High Speed Clock Self-trigger Cycle Jitter* — short term instability using any high speed clock pin, from a rising clock edge to the next rising clock edge, or falling clock edge to the next falling clock edge.

Conditions:

- error expressed as RMS value;
- reference load B; and
- physical reference point is a zero length interconnect on the DUT side of a standard performance board.

7.1.4.5 *High Speed Clock Self-trigger Phase Jitter* — short term instability using any high speed clock pin, from a rising clock edge to the next falling clock edge, or falling clock edge to the next rising clock edge.

Conditions:

- error expressed as RMS value;
- reference load B; and
- physical reference point is a zero length interconnect on the DUT side of a standard performance board.

7.1.4.6 *High Speed Clock Transition Time Variation @ 5V* — minimum and maximum rise and fall times of a 5V input signal transition using any high speed clock pin.

Conditions:

- referenced to the 20% and 80% points of a positive and negative signal transition;
- reference load A; and
- physical reference point is a zero length interconnect on the DUT side of a standard.

7.1.4.7 *High Speed Clock Transition Time Variation @ 3V* — (same as Section 7.1.4.6 @ 3V)

7.1.4.8 *High Speed Clock Transition Time Variation @ 1V* — (same as Section 7.1.4.6 @ 1V)

7.1.5 *Input Timing Delay Error for Z to Drive High/Low* — Time delay error at the midpoint of a driver transition from Z to high/low, with respect to an ideal delay, using any pin, any delay value, any Z

control timing edge, any Z transition format, and any test cycle length.

NOTE 3: This definition does not include I/O timing restrictions imposed by the round trip delay between the tester electronics and the DUT.

Conditions:

- delays are normalized to pin1 (first tester pin), rising edge, NR format, 5V, @ 0ns;
- errors are normalized to the average of minimum and maximum of the error distribution;
- reference load C; and
- physical reference point is a zero length interconnect on the DUT side of a standard performance board.

7.1.6 *Input Timing Delay Error for Drive High/Low to Z* — Time delay error at the midpoint of a driver transition from high/low to Z, with respect to an ideal delay, using any pin, any delay value, any Z control timing edge, any Z transition format, and any test cycle length.

NOTE 4: This definition does not include I/O timing restrictions imposed by the round trip delay between the tester electronics and the DUT.

Conditions:

- delays are normalized to pin1 (first tester pin), rising edge, NR format, 5V, @ 0ns;
- errors are normalized to the average of minimum and maximum of the error distribution;
- reference load C; and
- physical reference point is a zero length interconnect on the DUT side of a standard performance board.

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SEMI G80-0200
TEST METHOD FOR THE ANALYSIS OF OVERALL DIGITAL TIMING ACCURACY FOR AUTOMATED TEST EQUIPMENT

This test method was technically approved by the Global Automated Test Equipment Committee and is the direct responsibility of the North American Automated Test Equipment Committee. Current edition approved by the North American Regional Standards Committee on September 3, 1999. Initially available at www.semi.org December 1999; to be published February 2000.

1 Purpose

1.1 This procedure will define a standard process whereby any logic integrated circuit (IC) ATE system can be evaluated for parameters that makeup an AC timing accuracy specification.

1.2 Application of this procedure will simplify ATE comparisons, reduce specification ambiguity, simplify user acceptance procedures, simplify ATE performance monitoring, and provide a common validation criteria for ATE suppliers.

2 Scope

2.1 This procedure is intended for analysis of timing accuracy specifications for all semiconductor automatic test equipment (ATE) capable of digital functional testing. The extent of the analysis includes overall timing accuracy and the primary components of overall timing accuracy as defined in the definition section of this document.

2.2 This procedure does not include analysis of the following parameters associated with ATE timing accuracy:

- minimum driver pulse width,
- comparator bandwidth,
- I/O round trip delay,
- test fixturing errors,
- device insertion errors,
- time measurement unit (TMU) accuracy, and
- ATE capability or performance beyond AC timing accuracy.

2.3 Application of this procedure can reduce equipment acceptance time resulting in savings for both the end-users and ATE suppliers.

2.4 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Limitations

3.1 The following limitations are inherent to this procedure:

3.1.1 The tolerances of each measurement used in the procedure are listed in each test, where appropriate.

3.1.2 The verification methods do not include varying environmental conditions, so results may not reflect performance at environmental limits.

3.1.2.1 Due to execution time limits, the verification procedure does not represent an exhaustive analysis. The number of data points analyzed is intended to provide a minimum representative assessment of AC timing accuracy parameters in a practical amount of time.

3.1.3 This method uses only edge compare mode and non-multiplexed operation in providing a minimum representative assessment of AC timing accuracy.

3.1.4 This method does not determine the effects that duty cycle variations have on AC timing accuracy.

3.1.5 Not being an exhaustive analysis this method avoids comprehensive testing as might be expected for complex AC timing functions such as on-the-fly (OTF) timing. This method was defined with the intention of keeping the data gathering practical such that meaningful results are obtained in a reasonable amount of time. In the case of timing-on-the fly a routine is contained in this method and can be used as a reference parameter for comparative purposes when systems with on-the-fly timing are analyzed. Thus only the most fundamental AC timing results are produced and OTF timing is not included as part of the overall timing accuracy (OTA) results.

3.1.6 Discretion is advised when interpreting OTA results obtained from this method. Self-analysis cannot allow for all error components to be isolated. Thus good (compliant) method results should be viewed with caution as potentially compliant. On the other hand, poor (non-compliant) method results are a strong indication that the system under evaluation is questionable regarding its accuracy and most likely non-compliant.

SEMI G80-0200 © SEMI 2000

4 Referenced Standards

4.1 *SEMI Standard*

SEMI G79 — Specification for Overall Digital Timing Accuracy

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *1*[1] — tester output driver high level

5.1.2 *0*[2] — tester output driver low level

5.1.3 *ATE* — automated test equipment

5.1.4 *DUT* — device under test

5.1.5 *H*[3] — tester input comparator expect high level.

5.1.6 *L*[4] — tester input comparator expect low level.

5.1.7 *n* — highest pin/channel number, and Pin 1 — refers to the lowest pin/channel number.

5.1.8 *NR* — non-return signal format

5.1.9 *RTO* — return to one signal format.

5.1.10 *RTZ* — return to zero signal format.

5.1.11 *SBC* — surround by complement signal format.

5.1.12 *Z* — tester output driver high impedance ("off") state.

5.2 *Definitions*

5.2.1 *device insertion errors* — error influenced by device-input capacitance and/or terminations.

5.2.2 *edge* — time delay created by an ATE delay generation resource.

5.2.3 *high bandwidth oscilloscope* — digital sampling oscilloscope with > 10 GHz bandwidth, using probes with > 1 GHz bandwidth, 500 ohm input impedance, 2.5pF ± 0.5pF input capacitance and < 0.125" ground lead.

5.2.4 *pin* — tester channel

5.2.5 *performance board* — printed circuit board used to interface the tester channels to the device under test.

5.2.6 *test fixturing errors* — error influenced by mismatched signal path lengths, impedance discontinuities, lumped capacitance/inductance elements, and high frequency loss due to skin effect or interconnects.

5.2.7 *window compare* — monitor device continuously during a time interval.

5.2.8 *zero_reference_measurement* — oscilloscope measurement of the midpoint of a 0–3v NR signal rising edge with delay = 0s. This is an arbitrary reference signal selected by the user of this method. The method user is free to choose a convenient reference signal that will allow consistent use of that signal for making edge placement timing measurements during tests described in level 2 of this procedure.

6 Summary of Method

6.1 This procedure provides a hierarchical, generic method of analyzing ATE timing accuracy. The hierarchy supports two levels of specification analysis. Broad, composite net results are available by using the ATE for self-analysis in Level 1.

6.2 At this level, a large amount of data can be efficiently collected, representing the net conformance to overall timing accuracy specifications. This technique, however, precludes isolation and detailed analysis of specific accuracy components. Therefore, a second level of analysis, incorporating external instruments is included. While the first level provides efficient, broad analysis, the second level provides less efficient, detailed analysis.

6.3 Results from the analyses are saved in a standard format to facilitate further use for application specific data reduction. The minimum format is:

test #, channel #, min value, max value

6.3.1 *Verification Procedure Summary*

6.3.1.1 *Level 1 ATE Self-Analysis*

- Highly Efficient
- Broad Scope
- Moderate Error Observability
- Drive Input to Compare Output Tests
  - 3 Voltages
  - 2 Pin Directions
  - 503 Test Cycles[5]
  - 503 Pulse Widths
  - 12 Transitions[6]
  - 4 Formats
- Extended Delay Tests

1 This convention is not universal. Sometimes a "H" is used.

2 This convention is not universal. Sometimes a "L" is used

3 This convention is not universal. Sometimes a "1" is used.

4 This convention is not universal. Sometimes a "0" is used.

5 Reference Figure 3.

6 Reference Figure 2.

- Drive Z-State Tests
- Multiple Period Tests

6.3.1.2 *Level 2 External Measurements*

- Inefficient w/o Automation
- Focused Scope
- Good Error Observability
  - Drive (input) Timing Test
  - Compare (output) Timing Test
  - Driver Rise Time Test
  - Drive (input) Timing Cycle Jitter Test
  - High Speed Clock Test

7 Requirements

7.1 *Acceptance Tests* — Before initiating the test process, the ATE under evaluation is to be certified by a representative of the manufacturer or end-user to be fully operational.

7.2 *Personnel Qualification* — The individual(s) operating the ATE under evaluation must be certified or otherwise qualified to operate this equipment, and be familiar with the procedures for performing the analysis called-out in this document.

7.3 *Supplemental Equipment* — The following equipment is required: A digital sampling oscilloscope with > 10 GHz bandwidth, probes with > 1 GHz bandwidth, 500 ohm input impedance, 2.5 pF ± 0.5pF input capacitance, and < 0.125" ground lead. It is important that this equipment requirement step be met. Tolerances called-out in various steps of this procedure were chosen to be consistent with the general equipment specified in this equipment specification requirement.

7.4 *This Procedure* — It is highly recommended that the user of this method read this document (SEMI G80) in its entirety.

7.5 *System* — Test system usage will be available on a continuous basis and uninterrupted during the allotted time needed to perform this timing analysis procedure.

7.6 *Application Program* — It is required that an application program be written to perform the steps called-out in this procedure. That program will act as a means of reliable and consistent interaction between the tester and supplemental equipment. In so executing, that program will also facilitate the data collection process that will ultimately lead to the timing analysis conclusions this procedure produces.

7.7 *The Method* — The recommended procedure, contained primarily in Section 10 of this document, is generically written and will serve as a guide in producing the required program, written in the test application software language of the system under evaluation.

7.8 *ATE System Performance (Load) Boards* — To collect data two performance/load boards will be required. For one of these performance boards it is recommended that adjacent tester channels be shorted together with minimum and equal length interconnections. This board will facilitate the data collection process for Level 1 and in part for Level 2. The second board is to have an open driver to comparator connection and will be used for Level 2 drive input timing tests. Reference Figures 1 and 4.

7.9 *Exceptions* — It is expected that the user of this method execute the procedures as described in this document. If the method user should choose to deviate from the procedures recommended in this document it is expected that an appropriate description of that deviation be entered in the EXCEPTIONS PAGE provided in Appendix 3.

8 Test Conditions

8.1 *Environmental* — It is a requirement that the procedure called-out in this document be executed within the intended environmental operating conditions specified by the equipment supplier. Operating temperature requirements specified by the equipment supplier must be maintained.

8.2 *Optional Execution* — The user of this procedure may consider rerunning this procedure at environmental (temperature) extremes other than nominal.

8.3 *Warm-up Period* — It is essential that all equipment used or under evaluation be allowed to warm-up in accordance with the manufacturer's specified requirements for equipment stabilization.

8.4 *Optional Data Collection* — Data may be taken immediately after equipment calibration. However, the user of this procedure may wish to take additional data at subsequent time intervals, but within the known good calibration window for the system under evaluation.

9 Preparation of Apparatus

9.1 *Equipment Configuration* — The equipment under evaluation must be configured for its normal and intended operation. No special considerations such as additional cooling or removal of equipment skins are to be undertaken.

9.2 *Equipment Calibration* — The equipment under evaluation must be fully calibrated before this procedure is executed. No special calibration is to be

performed and the equipment is to be configured for normal and intended operation.

9.3 *Supplemental Equipment Calibration* — External equipment used for level 2 data collection in this procedure must be verified for proper calibration.

10 Test Method Procedure

10.1 The procedure is comprised of Level 1 tests and Level 2 tests. Any ATE capability described in the following tests that is not available on the ATE under analysis is not required for compliance to the procedure, but should be noted in the verification results Table 1 and Table 2.

10.2 Each test system is different; thus this procedure is generic. Regardless, it will provide comprehensive results when the specific application is created using this procedure as a guide. Per the requirements, a load board and application program written to accommodate the procedure should be in place when the procedure is executed. This procedure is to be executed per the requirements outlined in Section 7 of this document. When these requirements are met, the following steps will comprise the step by step process for execution of this Test Method:

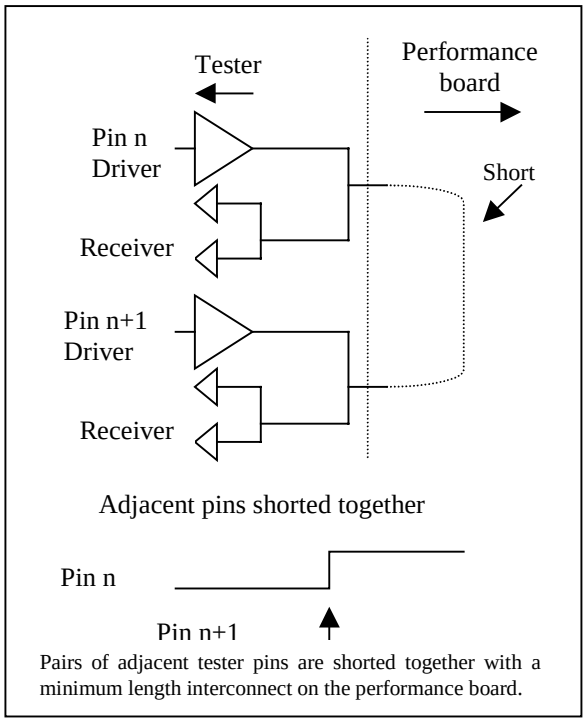

Figure 1
Level 1 Verification

1. Install the performance board.

2. Power up the system and supplemental equipment, allow adequate time for stabilization.

3. Load the appropriate application program that represents the embodiment of the procedure called out in Sections 10.3.1, 10.3.4, 10.3.5, and 10.3.6 for Level 1 as well as Sections 10.4.1, 10.4.2, 10.4.3, 10.4.4, 10.4.5, and 10.4.6 for Level 2.

4. Execute the method to completion. The application program can capture the data for Level 1 and Level 2 and store that for later analysis.

5. This procedure calls for various time measurements to be made at specified voltage points or signal levels. The user is encouraged to maintain these values to keep the method results constants when system to system comparisons are being made. Regardless, he is free to adjust these measurement points or levels to accommodate specific integrated circuit technology requirements important to that product and the system being analyzed. When that occurs documentation of those procedure variations must be entered in Appendix 3 (Exceptions Page).

6. Best results from this procedure are achieved if a consistent measurement methodology is maintained. This is important when making time measurements relative to a particular transition point on a signal edge. This method recommends that when signal measurements are specified at a particular transition point, i.e., 50%, that this point on the edge be determined relative to the 0% or 100% steady state levels displayed on the oscilloscope, after any aberrations due to the transition have expired. A tester reference channel, the lowest channel, should be used to set the measurement point(s) and then consistently used as the basis for subsequent measurements for the remaining tester channels.

7. *Data Analysis* — Analyze the captured data and make the appropriate data entries to Table 1, provided in this method document.

8. When this method execution is complete, document all method exceptions in the EXCEPTIONS section of this document (Appendix 3).

9. *Results* — Data entry to Table 2. Make the appropriate data entries to Table 2, provided in this method document and supplemented with examples contained in Appendix 2.

10.2.1 Level 1 requires no external equipment for completion, whereas Level 2 does require use of external equipment. The user is free to implement this procedure through total manual intervention. On the other hand, the user may choose to apply an automated or robotic approach to data collection for Level 2. Regardless, the user is advised that tester and external

equipment interaction accommodated by the application program is necessary for data collection at Level 2.

10.3 *Level 1 Tests* — Level 1 tests are intended to efficiently gather a large amount of data by taking advantage of the self-analysis ability of the ATE. This is accomplished by shorting adjacent tester channels together on a performance board with minimum, equal length interconnections, and using one channel to test the other. Reference Figure 1. Execution speed and system resource coverage are of primary importance for Level 1. Level 1 is intended to analyze specification conformance as opposed to diagnose system failures. All measurements are normalized to "zero" in order to facilitate subsequent data reduction/analysis. Level 1 is intended to collect data only. Data reduction and processing are to be done off-line in order to maximize data collection efficiency.

10.3.1 *Timing Linearity Test* — This test is used to establish drive input to compare output timing accuracy by "stretching" the test cycle in minimum cycle programming increments while using fixed percentage delays and pulse widths as the method sweeps through various timing conditions. The test pattern should be written to switch all even or odd pins simultaneously, and for all transitions and associated strobes to occur at least 100 times for each data point.

10.3.2 For clarification all drive edges are detected in parallel in pairs. The intention is to sweep the compare edge and detect the earliest occurrence of a drive edge with the latest compare edge, as well as detect the latest occurrence of a drive edge with the earliest compare edge.

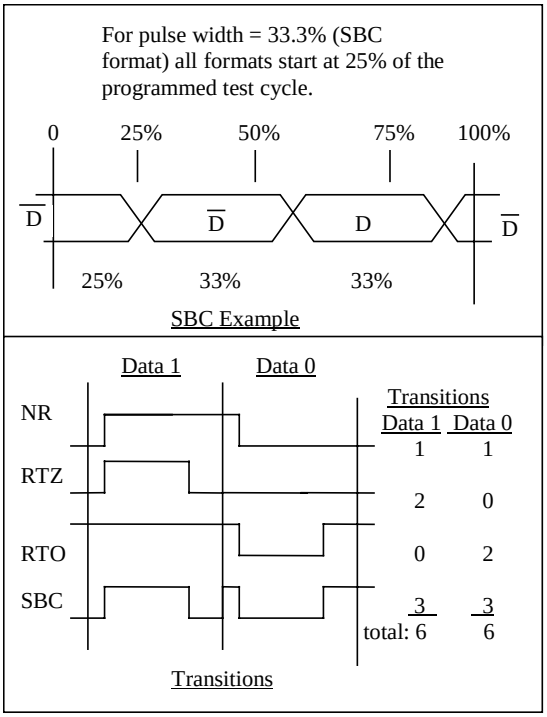

Figure 2
SBC Example and Transitions

10.3.3 The following Test Cycle Example and nested loop outline describes the test flow:

```
for amplitude = 1V, 3V, 5V
  for direction =
        odd_pins_drive_&_even_pins_compare to
        even_pins_drive_&_odd_pins_compare
    for test_cycle = min_cycle to [min_cycle +
        500*cycle_resolution] by
        cycle_resolution, 3x min_cycle, 10x min cycle
      for pulse width = 50% (RTZ/RTO formats)
                      = 33.3% (SBC format)
                      = don't care (NR format)
        for format = NR, RTZ, RTO, SBC (NOTE 1: all
            formats start at 25% of the programmed test
            cycle)
          for all format transitions (pattern data 0 and 1)
            detect earliest occurrence of format
                transition midpoint with the latest
                compare pin
            detect latest occurrence of format transition
                midpoint with the earliest compare pin
             error = (latest occurrence - earliest
                    occurrence)
          end transitions
        end format
      end pulse width
    end test_cycle
  end direction
end amplitude
```


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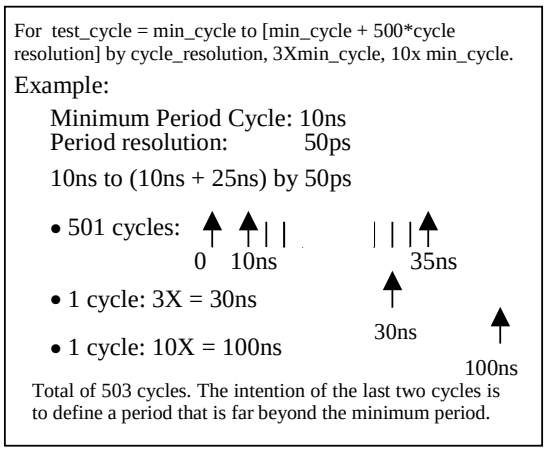


Figure 3
Test Cycle Example

10.3.4 *Extended Delay Test* — This test is used to establish drive input to compare output timing accuracy when timing generator delay values are programmed beyond the length of the test cycle. Driver input delays are programmed to occur in subsequent test cycles and detected with compare delays originating in the corresponding subsequent test cycle. The intention is the same as Section 10.3.1 with the exception that edges are programmed into a subsequent cycle. Conditions such as formats and voltages have been reduced to keep the amount of data collected down to a reasonable level.

10.3.4.1 The following nested loop outline describes the test flow:

```
for amplitude = 3V
 for direction =
      odd_pins_drive_&_even_pins_compare to
      even_pins_drive_&_odd_pins_compare
  for test_cycle = min to 10*min by 0.1*min
   for format = NR
    for format_delay = test_cycle to max_delay by
     0.25*test_cycle (max delay is beyond the cycle
                      boundary)
        detect earliest occurrence of format
             transition midpoint with the latest
             compare pin using pattern expect
             data shifted into the appropriate cycle
        detect latest occurrence of format transition
             midpoint with the earliest compare pin
             using pattern expect data shifted into
             the appropriate cycle
         error = (latest occurrence - earliest
                 occurrence)
           end delays
          end format
         end test cycles
        end directions
       end amplitude
```

10.3.5 *Driver Z State Test* — This test verifies the timing accuracy of tester driver transitions from Z to 1/0 and from 1/0 to Z. Driver inputs are programmed to transition to and from Z and 1/0 while being loaded with 50 ohms terminated to drive 1 for Z to 0 and 0 to Z, and 50 ohms terminated to drive 0 for Z to 1 and 1 to Z[7] (reference load C). The following nested loop outline describes the test flow:

```
for amplitude = 3V
 for direction =
   odd_pins_drive_&_even_pins_compare to
   even_pins_drive_&_odd_pins_compare
   for test_cycle = 5*min_cycle
    for format_delay = 50%
     for format = NR
      detect earliest occurrence of Z to low tran-
        sition at scaled midpoint with compare pins
      detect latest occurrence of Z to low tran-
        sition at scaled midpoint with compare pins
      error=(latest occurrence - earliest occurrence)
      detect earliest occurrence of Z to 1 tran-
        sition at scaled midpoint with compare pins
      detect latest occurrence of Z to 1 transition
        at scaled midpoint with compare pins
      error = (latest occurrence - earliest occur-
              rence)
      detect earliest occurrence of 0 to Z transition
        at scaled midpoint with compare pins
      detect latest occurrence of 0 to Z transition at
        scaled midpoint with compare pins
      error = (latest occurrence - earliest occur-
              rence)
      detect earliest occurrence of 1 to Z tran-
        sition at scaled midpoint with compare pins
      detect latest occurrence of 1 to Z transition
        at scaled midpoint with compare pins
      error = (latest occurrence - earliest occur-
              rence)
     end format
    end format_delay
   end test_cycle
  end direction
end amplitude
```

10.3.6 *Multiple Period Test*[8] — This is an optional test to be run only if the ATE supports dynamic (or "on-the-fly") time set switching. This test intention is similar to Section 10.3.1 and 10.3.4 (timing linearity and extended delay tests) except that the test period and delay changes are generated dynamically within a

7 Tying two drivers together or connecting a resistor to a logic point is acceptable. Note: Load "C": 50 ohms to low for driver z to high and high to z transitions. And 50 ohms to high for driver z to low and low to z transitions.

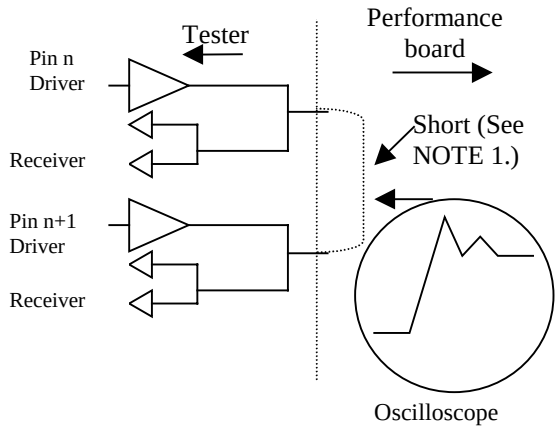
8 This algorithm requires 64 time sets. If the equipment does not have 64 time sets, adjust the algorithm to accommodate the amount available and note the differences on the exception page, Appendix 3.

single test pattern burst. The following nested loop outline describes the test flow:

for amplitude = 1V, 3V, 5V
  for direction =
        odd_pins_drive_&_even_pins_compare to
        even_pins_drive_&_odd_pins_compare
    execute single pattern with the following
    dynamic changes:

Test Cycle	*Drive Format*	*Format Offset*	*Pulse Width*	*Drive Data*	*Compare Offset*	*Expect Data*
min	SBC	20%	33%	1	53%	H
min	SBC	20%	33%	1	86%	L
min	SBC	20%	33%	0	53%	L
min	SBC	20%	33%	0	86%	H
min	SBC	20%	33%	1	20%	L
			.			
			.			
min	SBC	20%	33%	0	20%	H
64*min	SBC	20%	33%	1	53%	H
64*min	SBC	20%	33%	1	86%	L
64*min	SBC	20%	33%	0	53%	L
64*min	SBC	20%	33%	0	86%	H
64*min	SBC	20%	33%	1	20%	L
64*min	SBC	20%	33%	0	20%	H
2*min	SBC	20%	33%	1	53%	H
2*min	SBC	20%	33%	1	86%	L
2*min	SBC	20%	33%	0	53%	L
2*min	SBC	20%	33%	0	86%	H
2*min	SBC	20%	33%	1	20%	L
2*min	SBC	20%	33%	0	20%	H
63*min	SBC	20%	33%	1	53%	H
63*min	SBC	20%	33%	1	86%	L
63*min	SBC	20%	33%	0	53%	L
63*min	SBC	20%	33%	0	86%	H
63*min	SBC	20%	33%	1	20%	L
63*min	SBC	20%	33%	0	20%	H
			.			
			.			
32*min	SBC	20%	33%	1	53%	H
32*min	SBC	20%	33%	1	86%	L
32*min	SBC	20%	33%	0	53%	L
32*min	SBC	20%	33%	0	86%	H
32*min	SBC	20%	33%	1	20%	L
32*min	SBC	20%	33%	0	20%	H

      detect earliest occurrence of format
          transition midpoint with the latest
          compare pin
      detect latest occurrence of format transition
          midpoint with the earliest compare pin
      error = (latest occurrence - earliest occurrence)
  end direction
end amplitude



Pairs of adjacent tester pins can be shorted together with a minimum length interconnect on the performance board.

A reference for the oscilloscope measurement is required. That reference can be any signal synchronized to the test system's timing. The reference signal chosen should be consistent and stable. Examples of this may be another tester pin or master oscillator reference signal.

NOTE 1: The user of this method may find improved driver signal attributes using an open circuit performance board, versus the shorted board indicated here for Level 2 Drive Input Timing Error data collection. On the other hand the shorted performance board, using the driver as the signal source, is a viable approach for the Compare Output Timing Error Test. Regardless, the user may optionally choose to use a pulse generator as the signal source for the Compare Output Timing Error test. The 50-ohm pulse generator must have edge speeds that are comparable to the driver it is replacing. Test setup conditions and the pulse generator rise time employed must be documented on the exception page (Appendix 3).

Figure 4
Level 2 Verification

10.4 *Level 2 Tests* — The efficiency of data collection with Level 1 tests may preclude isolation of certain specification components. The self-analysis procedures may also mask some error terms that contribute to other specification components. Therefore, Level 2 modules are intended to supplement Level 1 results by using external instruments to distinguish individual specification components and provide detailed analysis

of potentially masked results. The use of external instruments facilitates independent observation of individual parameters, but requires physical movement of a probe (unless automated with robotics), which results in less efficient data collection. Reference Figure 4.

10.4.1 *Drive Input Timing Error Test* — Since the driver input timing error cannot be distinguished from compare output timing error with Level 1 tests[9] an external instrument must be used to isolate the driver input timing error from compare output timing error. An external instrument is also required to identify pin to pin "skew" beyond adjacent pins, since Level 1 only uses adjacent pin pairs for analysis. This requires independent measurements of representative driver input timing conditions. The reference for measurement of driver input timing error is a high bandwidth-digital sampling oscilloscope. Exhaustive testing of all pins is impractical, so a reduced set of representative conditions is used. A non-binary pin sampling increment is used to ensure that traditional binary architectural boundaries are crossed. The tolerance for the driver input timing error test is ± 20ps[10] due to the tester/instrument interaction using a generic measurement method. The following nested loop outline describes the test flow:

```
for amplitude = 3V
  for pin = 1 to n by 3
    for test_cycle = min, 2*min, 3*min, 10*min
      for format_delay = 50% of test cycle
          for format = NR, RTZ, RTO, SBC
            for all format transitions
              detect midpoint of drive transition with
                  oscilloscope  (averaging = 8)
              error = (measured_delay - pro-
                        grammed_format_edge_time -
                        zero_reference_measurement)
            end transitions
        end format
      end format_delay
    end test_cycle
  end pin
end amplitude
```

10.4.2 *Compare Output Timing Error Test* — Since the compare output timing error cannot be distinguished from driver input timing error with Level 1 tests, an external reference must be used to isolate compare output timing error from driver input timing error. This requires independent measurement of representative compare timing conditions. Each tester driver is used to provide a synchronous reference signal by shorting adjacent tester channels together on a performance board with minimum, equal length interconnections. The actual delay of the driver signal is verified with a high bandwidth-digital sampling oscilloscope. (See Figure 4.)

NOTE 2: If a signal reflection is present at the midpoint of the observed signal (due to a long distance from the performance board to the tester receiver), then the 25% point of the reference driver waveform should be used, instead of the midpoint - as specified below.

10.4.2.1 Exhaustive testing of all pins is impractical, so a reduced set of representative conditions are used. A non-binary pin sampling increment is used to ensure that traditional binary architectural boundaries are crossed.

10.4.2.2 The following nested loop outline describes the test flow:

```
for amplitude = 3V
  for pin = 1 to n by 3
    for test_cycle = min, 2*min, 3*min, 10*min
      for format_delay = 50% of test_cycle
        for format = NR
          for edge = rising, falling
            detect midpoint of NR drive signal with
              oscilloscope  (averaging = 8)
            detect midpoint of drive transition with
              comparator (strobe compare mode)
            error = (measured_delay - pro-
                      grammed_compare_delay -
                      zero_reference_measurement)
        end edge
      end format
    end format_delay
  end test_cycle
 end pin
end amplitude
```

NOTE 3: Midpoint detection of the NR drive signal should be done via a compare edge sweep technique.

10.4.3 *Driver Transition Time Test* — Since driver transition time errors can be masked by compare timing errors and comparator bandwidth limitations, an external instrument is required to measure driver transition time errors. The reference used for driver transition time measurements is a high bandwidth-digital sampling oscilloscope.

10.4.3.1 The tolerance for driver transition time measurements is ± 150ps[11] due to the tester/instrument

9 See APPENDIX 2, Section A2-1.3 and Appendix 2, Examples for an explanation.

10 When recording measurements, data log all measurements as they are taken from the measurement equipment and show the associated equipment tolerance as a separate entity.

11 This 150ps tolerance has been extended beyond 20ps due to level sensitivities associated with oscilloscopes and typical bandwidth variations in oscilloscope probes rendering transition time measurements less accurate.