RELATED INFORMATION 1
CMP PROCESS TEST GUIDE

NOTE: This related information is not an official part of SEMI M48, and is not intended to modify or supercede the proposed standard. It is provided for information purposes.

Table R1-1 Recommended Values for Wafer and Insulating Film Thickness for CMP Process Test

Item		*Guideline*
Wafer (See NOTE 1.)	Bow	–25 μm to +25 μm
	Warp	≤ 25 μm
	GBIR (previously called TTV)	≤ 4 μm
	SBIR (20 × 20 mm site)	≤ 0.5 μm
Starting Insulating Film Thickness		1000 – 1500 nm
Starting % WIWNU		≤ 2% of mean thickness
Final Insulating Film Thickness		50% of starting film thickness

NOTE 1: See SEMI M1 for definitions of listed wafer parameters.

Table R1-2 Recommended Values for Wafer and Metal Film Thickness for CMP Process Test

Item		*Guideline*
Wafer (See NOTE 1.)	Bow	–25 μm to +25 μm
	Warp	≤ 25 μm
	GBIR (previously called TTV)	≤ 4 μm
	SBIR (20 × 20 mm site)	≤ 0.5 μm
	Insulating Film Thickness	≤ 600–1000 nm
W Stack	Starting TiN Film Thickness	25–30 nm
	Starting W Film Thickness	800 nm
	Final W Thickness	50% of starting W film thickness
	W Stack % WIWNU	≤ 2% of mean thickness
Cu Stack	Starting Glue Layer (Ta or TaN) Thickness	20–50 nm
	Starting Cu Seed Layer Thickness	100–150 nm
	Plated Cu Film Thickness	As required by application
	Final Cu Film Thickness	50% of plated Cu film thickness
	Cu Stack % WIWNU	≤ 8% of mean thickness

NOTE 1: See SEMI M1 for definitions of listed wafer parameters.

SEMI M49-0704
GUIDE FOR SPECIFYING GEOMETRY MEASUREMENT EQUIPMENT FOR SILICON WAFERS FOR THE 130 nm TO 65 nm TECHNOLOGY GENERATIONS

This guide was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the European Silicon Wafer Committee. Current edition approved by the European Regional Standards Committee on May 14, 2004. Initially available at www.semi.org June 2004; to be published July 2004. Originally published November 2001; previously published March 2003.

1 Purpose

1.1 This document provides a guide for specifying measurement equipment for geometry and flatness of silicon wafers of the 130, 90, and 65 nm technology generation as anticipated by the International Technology Roadmap for Semiconductors (ITRS) and in the forecasts of the major manufacturers of semiconductor devices. Wafer parameters as defined by SEMI M1, SEMI M8, SEMI M11, SEMI M24, or SEMI M38 are specified by customers of Si wafer suppliers and are usually part of Certificates of Compliance. Suppliers of Si wafers and their customers might measure these parameters using equipment provided by different manufacturers of such equipment or using different generations of equipment of one supplier. Agreement on basic features and capability of such measurement equipment improves data exchange and interpretation of data as well as procurement of appropriate tools.

2 Scope

2.1 This guide outlines and recommends basic specifications for equipment for measuring geometry and flatness of Si wafers of 130, 90, and 65 nm technology generation.

2.2 The guide applies to measurement equipment used for verifying the quality parameters geometry and flatness in large scale production of bare polished or epitaxial Si wafers the backside of which may be acid etched and/or covered by unpatterned, homogeneous layers of e.g. poly-Si or LTO (low temperature oxide). Artifacts (e.g., reference materials) for calibrating measurement equipment might have different properties.

2.3 The guide also applies to measurement equipment that provides only a subset of the measurement features outlined in this guide.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 The document does not apply to measurement equipment used to control intermediate process steps during Si wafer manufacturing. However, it may be completely or partly used for measurement equipment for those applications provided corresponding constraints are appropriately identified.

3.2 The document also does not apply to measurement equipment for SOI wafers or patterned wafers.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E5 — SEMI Equipment Communications Standard 2 Message Content (SECS-II)

SEMI E10 — Specification for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM)

SEMI E14 — Measurement of Particle Contamination Contributed to the Product from the Process or Support Tool

SEMI E30 — Generic Model for Communications and Control of Manufacturing Equipment (GEM)

SEMI E37 — High Speed SECS Message Services (HSMS) Generic Services

SEMI E58 — Automated Reliability, Availability, and Maintainability Standard (ARAMS): Concepts, Behavior, and Services

SEMI E89 — Guide for Measurement System Capability Analysis

SEMI M1 — Specification for Polished Monocrystalline Silicon Wafers

SEMI M1.15 — Standard for 300 mm Polished Monocrystalline Silicon Wafers (Notched)

SEMI M8 — Specification for Polished Monocrystalline Test Wafers

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Integrated Circuit (IC) Applications

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M27 — Practice for Determining the Precision Over Tolerance (P/T) Ratio of Test Equipment

SEMI M38 — Specification for Polished Reclaimed Silicon Wafers

SEMI M43 — Guide for Reporting Wafer Nanotopography

SEMI MF42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

SEMI MF84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

SEMI MF534 — Standard Test Method for Bow of Silicon Wafers

SEMI MF657 — Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Non-contact Scanning

SEMI MF671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Non-contact Eddy-Current Gage

SEMI MF928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1152 — Standard Test Method for Dimensions of Notches on Silicon Wafers

SEMI MF1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1451 — Standard Test Method for Measuring Sori on Silicon Wafers by Automated Non-contact Scanning

SEMI MF1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Non-contact Scanning

SEMI MF2074 — Standard Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

4.2 *ISO Standards*[1]

ISO/IEC 8859 — Information technology – 8-bit single-byte coded graphic character sets

ISO 8879 — Information Processing – Text and office systems – Standard Generalized Markup Language (SGML)

ISO 9000 — Quality management systems – Fundamentals and vocabulary

ISO 9001 — Quality management systems – Requirements

ISO/IEC 10646-1 — Information technology – Universal multiple-octet character set (UCS) – Part 1: Architecture and basic multilingual plane

ISO/IEC 10918 — Information technology – Digital compression and coding of continuous-tone still images

ISO 14644-1 — Cleanroom and associated controlled environments – Part 1: Classification of air cleanliness

4.3 *JEITA Standards*[2]

JEIDA 43 — Terminology of silicon wafer flatness

4.4 *DIN Standards*[3]

50431 — Measurement of the electrical resistivity of silicon or germanium single crystals by means of the four-point-probe direct current method with collinear probe array

50432 — Determination of the conductivity type of silicon or germanium by means of rectification test or hot-probe

50441-1 — Determination of the geometric dimensions of semiconductor slices; measurement of thickness

50441-2 — Determination of the geometric dimensions of semiconductor slices; testing of edge rounding

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1 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch

2 Japanese Electronic and Information Technology Industries Association, Tokyo Chamber of Commerce and Industry Bldg. 2-2, Marunouchi 3-chome, Chiyoda-ku, Tokyo 100-0005, Japan. Website: www.jeita.or.jp

3 Available from Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany. Website: www.din.de

50441-4 — Determination of the geometric dimensions of semiconductor slices; diameter and flat depth of slices

50441-5 — Determination of the geometric dimensions of semiconductor wafers; terms of shape and flatness deviation

50445 — Contactless determination of the electrical resistivity of semiconductor wafers with the eddy current method

NOTE 1: Unless otherwise indicated, all documents cited shall be the latest published versions.

4.5 *IEEE Standards*[4]

IEEE 754 — IEEE Standard for Binary Floating-Point Arithmetic

IEEE 802 — IEEE Standard for Local and Metropolitan Networks: Overview and Architecture

IEEE 854 — IEEE Standard Radix-Independent Floating-Point Arithmetic

4.6 *Other Standards*

FED-STD 209E —Airborne Particulate Cleanliness Classes in Clean Rooms and Clean Zones[5]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *ARAMS* — Automated Reliability, Availability, and Maintainability Standard

5.1.2 *ASCII* — American Standard Code for Information Interchange

5.1.3 *FTP* — File Transfer Protocol

5.1.4 *GEM* — Generic Equipment Model

5.1.5 *HSMS* — High Speed SECS Messaging Service

5.1.6 *IEEE* — The Institute of Electrical and Electronics Engineers, Inc.

5.1.7 *JPEG* — Joint Photographics Expert Group

5.1.8 *SECS* — SEMI Equipment Communications Standard

5.1.9 *XML* — Extensible Markup Language

5.2 *Definitions*

4 Institute of Electrical and Electronics Engineers, IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331, USA. Telephone: 732.981.0060; Fax: 732.981.1721

6 General Services Administration, Federal Supply Service, FSS Acquisition Management Center, Environmental Programs and Engineering Policy Division (FCOE), Washington, D.C. 20406

5.2.1 *bias* — the difference between the average of measurements made on the same object and its true value. Sufficient measurements are needed to mitigate the effects of variability. (SEMI E89)

5.2.2 *calibration* — calibration is a measurement process that assigns value to the property of an artifact or to the response of an instrument relative to reference standards or to a designated measurement process.

NOTE 2: The purpose of calibration is to eliminate or reduce bias in the user's measurement system relative to the reference base. The calibration process compares an unknown or test item or instrument with reference standards according to a specific algorithm, often in the form of a specific calibration curve. (SEMI E89)

5.2.3 *compatibility* — the capability of measurement equipment to emulate the measurement process of other tools. Downward compatibility refers to former generation(s) of the same or similar type of equipment of an equipment supplier.

NOTE 3: Compatibility can be provided by a measurement mode in which filtering, spatial resolution, etc. of another, older, tool is imitated.

5.2.4 *correlation* — the relation of measurement results obtained by repeated measurements with the same set of test specimen(s) and any two measurement tools expressed in terms of a regression curve.

5.2.5 *level 1 variability* (σ_1) — the variation (standard deviation) of measurement results obtained by repeated measurements with the same test specimen(s) and the same measurement tool under nominally identical conditions without replacing the test specimen between subsequent measurement runs. σ_1 tests are performed with a single calibration in the shortest possible time interval.

5.2.6 *level 2 variability* (σ_2) — the variation (standard deviation) of measurement results obtained by repeated measurements with the same test specimen(s) and the same measurement tool with replacing the test specimen between subsequent measurement runs but otherwise under nominally identical conditions. σ_2 tests are performed with a single calibration in the shortest possible time interval.

5.2.7 *level 3 variability* (σ_3) — the variation (standard deviation) of measurement results obtained by repeated measurements with the same test specimen(s) and the same measurement tool with replacing the test specimen between subsequent measurement runs but otherwise under nominally identical conditions. σ_3 tests are performed over a time period greater than σ_2 tests without operator induced adjustment.

5.2.8 *matching tolerance* (Δ_m) — the difference in bias for any two measurement tools of the same kind.

Otherwise matching tolerance tests are performed under the conditions of σ_3 tests.

NOTE 4: In the absence of certified or standard reference materials matching may be tested by using appropriate wafers complying with 130 nm technology node specifications. It is recommended to test for matching with a set of samples covering the parameter range of interest.

5.2.9 *precision over tolerance (P/T) ratio* — the ratio of the precision of measurement equipment and a product's tolerance. (SEMI M27)

5.2.10 *sorting* — real and virtual separation of test specimens in different categories specified by one or multiple parameters.

5.2.11 *tolerance* — the absolute magnitude of the range of the product specification. (SEMI M27)

6 Specification for Geometry Measurement Equipment for Silicon Wafers

6.1 The specification is structured in three sections (Tables 1–3):

- Generic Equipment Characteristics (Table 1)
- Materials to be measured (Table 2)
- Metrology Specific Equipment Characteristics (Table 3)

6.2 Tables 1–3 contain the specifications, referenced documents, test methods, and comments. Additional explanations and discussions are provided in this section.

6.3 Generic Equipment Characteristics (Table 1)

6.3.1 The section "Generic Equipment Characteristics" consists of five subsections:

- Wafer handling
- Reliability
- Procedural
- Documentation
- Computer/User Interface/Connectivity

6.3.2 Subsections covering "Facilities Requirements" and "Safety/Legal/Regulatory" are not included in the present document as these issues are highly user specific and dependent on national regulations.

6.4 *Materials to be measured (Table 2)*

6.4.1 Table 2 specifies the parameters of Si wafers that the measurement equipment must be capable to handle and to measure.

6.5 *Metrology Specific Equipment Characteristics (Table 3)*

6.5.1 This section specifies the dimensional parameters of Si wafers to be measured and to be reported by equipment for measuring the geometry and flatness of wafers as well as the required spatial resolution, precision and accuracy of the measurement equipment.

6.5.2 The ability of a metrology tool to properly measure surface features of different spatial wavelengths is affected by the spatial bandwidth of the tool's response function. Spatial bandwidth can be defined in many ways and is influenced by many factors beyond the scope of this document. Some of these need to be standardized.

6.5.3 Spatial resolution is defined by the high spatial frequency limit of the bandwidth of the tool's response function.

6.5.4 Low and high cut-off frequency f_{min} and f_{max} define the bandwidth of the response function of measurement equipment. The cut-off frequencies correspond to an attenuation of 0.5 for the amplitude of a sinusoidal surface feature with the exception of a low pass filter ($f_{min} = 0$) for which the attenuation remains 1 at f_{min}.

6.5.5 The rate of change of the attenuation approaching the cut-off frequencies has to be larger than the rate of a Gaussian filter with the corresponding cut-off frequency.

6.5.6 The present document recommends f_{max} and f_{min} that must be measured by the instrument.

6.5.7 Any variations in filtering procedures applied near the FQA boundary must be described by the supplier of the equipment.

6.5.8 The bandwidth as specified in Table 3 is a nominal value.

6.5.9 In the present document a hierarchy of variability levels is used to describe the performance of measurement equipment which is calibrated and adjusted/aligned according to the supplier's procedures. The various terms are defined in section 5. These variability levels are consistent with terms defined in SEMI E89 but not fully interchangeable. Their relation is indicated in parentheses.

6.5.9.1 Level 1 variability: standard deviation σ_1 (SEMI E89 static repeatability)

6.5.9.2 Level 2 variability: standard deviation σ_2 (SEMI E89 dynamic repeatability)

6.5.9.3 Level 3 variability: standard deviation σ_3 (SEMI E89 reproducibility)

6.5.10 In addition two levels of systematic off-set between different tools are defined:

6.5.10.1 matching tolerance (difference of means Δ_m)

6.5.10.2 correlation (regression curve)

6.5.11 Explicitly specified in the present document are only level 3 variability σ_3 and matching tolerance Δ_m as they correspond to the utilization of measurement equipment for wafer manufacturing most closely. The supplier of a specific tool may optionally provide specifications for level 1 and/or level 2 variability, respectively.

6.5.12 Level 3 variability σ_3 and matching tolerance Δ_m are specified with respect to anticipated specifications for wafer geometry and flatness as given in Table 3 for a reference wafer.

6.5.13 In the present document P/T-ratios are used for specifying level 3 variability σ_3.

6.5.13.1 A precision-to-tolerance ration P/T less than 10% at 6σ is recommended in SEMI M27 for metrology equipment. This would be an extremely demanding specification for flatness and geometry measurement tools. In addition, flatness characterisitics of Si wafers are typically described by a single sided distribution with the median approaching zero, the lower specification boundary. Therefore two grades that are based on 3σ criteria, instead on 6σ, are recommended for such tools in the present document:

- grade A: P/T < 10%, $3\sigma_3$
- grade B: P/T < 20%, $3\sigma_3$

6.5.13.2 The individual measurement features a tool provides may be graded differently, e.g. SFQR might meet grade A, but SBIR only grade B. This has to be indicated appropriately in the tools' technical specifications.

6.5.14 Matching tolerance is specified to be less or equal to $1.5\sigma_3$ of level 3 variability. This corresponds to a greater than 99% probability that the difference of any individual measurement results obtained with two different tools is smaller or equal to $5\sigma_3$.

6.5.15 The target for bias is a range of $\pm 1.5\sigma_3$ with respect to a certified value provided appropriate reference materials are available. This corresponds to a greater than 99% probability that any individual measurement is in the range of $\pm 4\sigma_3$ around the certified value when a reference material is tested.

6.5.16 Reference material with a series of surface features with appropriate height and half width is required to verify bandwidth of a measurement tool. The height of the features corresponds to the wafer specification as outlined in Table 3.

6.5.17 The specifications of the measurement equipment are verified by using wafers the parameters of which are in a range, the upper limit of which corresponds to 1.5 times anticipated wafer specification, the lower limit to 0.5 of anticipated wafer specification. These are listed in Table 3 as Reference Wafer Specifications.

NOTE 5: The edge region of wafers represents the most challenging area for meeting the desired performance characteristics. This is because of the larger surface geometry variations in the region near the edge, e.g. from polishing roll-off.

6.5.18 *Reference Wafers* — The specifications of the measurement equipment are verified by using reference wafers with properties covering the range given in Section 1 of Table 3. All reference wafers shall meet the thickness and warp requirements listed in the table but different wafers may be used to meet the flatness and nanotopography requirements. For site related specifications not all sites must fall within the range, but the appropriate sites to be tested should be indicated. In all cases, at least three wafers in the range of values for each property shall be employed in the testing.

6.5.19 Verification of bias, matching tolerance and the various levels of variability are performed with equipment which is calibrated according to the supplier's procedures and which is under statistical process control.

6.5.20 Compatibility of two tools is considered to be satisfactory when the specifications of the older tool are met with the newer tool operating in the emulation mode.

6.5.21 The quality of a correlation between different measurement equipment is not specified in the present document.

7 Related Documents

7.1 *ASTM Documents*

E 177 — Standard Practice for Use of the Terms Precision and Bias in ASTM Test Methods

E 456 — Standard Terminology for Relating to Quality and Statistics

7.2 *Other Documents*

Evaluating Automated Wafer Measurement Instruments, SEMATECH[6], Technology Transfer 94112638A-XFR

Metrology Tool Gauge Study Procedure for the International 300 mm Initiative (I300I), International 300 mm Initiative[6], Technology Transfer #97063295A-XFR

International Technology Roadmap for Semiconductors: 1999 edition[7,8]

ISO 3274: 1996 — Geometrical Product Specifications (GPS) – Surface Texture: Profile method – Nominal characteristic of contact (stylus) instruments[1]

Table 1 Generic Equipment Characteristics

Item	*Recommended Specification*	*Comment*	*References*
1 WAFER HANDLING			
1.1 Robot End-Effector	optional wafer edge or backside contact	edge as defined by SEMI M1	
1.2 Scan Stage	optional wafer edge or backside contact	edge as defined by SEMI M1	
1.3 Wafer Contact Materials	contact materials to leave metals and organics on wafers < as defined in ITRS 99		
1.4 Wafer Detection	protection of accidental contact due to e.g., cross-slotting double slotting, protrusions, etc.		
1.5 Wafer Rotational Alignment	random in, aligned out		
1.6 Number of Cassette Stations	2–4, arbitrary sender/receiver assignment		
1.7 Type of Cassettes	open, FOUP/SMIF, FOSB	to be specified alternatively	
1.8 Cassette Loading	manual/guided vehicle, conveyor belt		
1.9 Automatic Cassette ID	user specific		
1.10 Wafer Seating	vertical or off-horizontal	during setting cassette on station by operator	
1.11 Cassette Filling Modes	random access and loading, programmable empty slot filling		
1.12 Automatic Wafer ID reading	user specific		
1.13 Particulate Contamination	< 0.001 PWP per cm^2, > 90 nm LSE front, and > 120 nm LSE backside (See NOTE 1.)	verify with mirror polished wafer surfaces	SEMI E14
2 RELIABILITY			
2.1 MTBF	> 2000 h		SEMI E10
2.2 MTTA	> 4 h		SEMI E10
2.3 MTTR	according to service contract		SEMI E10
2.4 Availability	> 98%	per year	
2.5 Uptime	> 160 h/w		
2.6 Response Time	according to service contract		
2.7 Statistical Process Control (SPC) performance	automated		

6 International Sematech, 2706 Montopolis Drive, Austin, Tx. 78741-6499, USA

7 SEMATECH, 3101 Industrial Terrace Suite 106, Austin TX 78758

8 More recent versions of the ITRS are available from the homepage of International Sematech: www.sematech.org

Item	*Recommended Specification*	*Comment*	*References*
2.8 Statistical Process Control (SPC) machine parameters	automated		
3 PROCEDURAL			
3.1 Acceptance Testing	user specific		
3.2 Transport and Assembly	user specific		
3.3 Quality Assurance	supplier conforming with ISO 9000/9001		ISO 9000/9001
3.4 Warranty	> 1 y		
3.5 Test Certificates	user specific		
3.6 Spares Availability	> 10 y		
3.7 Change Control	supplier conforming with ISO 9000/9001		ISO 9000/9001
4 DOCUMENTATION			
4.1 Installation	tbd		
4.2 Operation	tbd		
4.3 Service	tbd		
5 COMPUTER, USER INTERFACE, CONNECTIVITY			
5.1 Computer Operating System	- Microsoft Windows NT 4.0 or higher, or - Unix		
5.2 Display	cleanroom compatible, class 10 (Federal Standard) or class 4 (ISO), respectively		FED-STD 209E ISO 14644-1
5.3 Keyboard	cleanroom compatible, class 10 (Federal Standard) or class 4 (ISO), respectively		FED-STD 209E ISO 14644-1
5.4 Pointing Device	cleanroom compatible, class 10 (Federal Standard) or class 4 (ISO), respectively		FED-STD 209E ISO 14644-1
5.5 Printer	cleanroom compatible, class 10 (Federal Standard) or class 4 (ISO), respectively		FED-STD 209E ISO 14644-1
5.6 Data Processing	- reprocessing of data - parallel processing in different modes during measurement including sorting - multiprocessing: e.g. recipe editing, up/downloading during measurements	different modes refer to data evaluation e.g. for two different site patterns, or different emulation modes	
5.7 Data Access	- access to basic measurement results: e.g thickness map, height map - data available at SECS/GEM/HSMS interface in real time	refers to all functions as defined in Table 3	SEMI E5 SEMI E30 SEMI E37
5.8 Data Analysis (Online/Offline)	on-line/off-line		
5.9 Recipe Control	- complete recipe generation off-line without machine specific data (calibration curves) - off-line recipe editing - remote recipe control by host computer - recipes are compatible between different software versions		

Item	*Recommended Specification*	*Comment*	*References*
5.10 Operating Sequence	complete remote control : recipe download, start, stop, define data evaluation via SECS/GEM		SEMI E5
5.11 Data Interfaces	- SECS/GEM - optional additionally a mass data standard transfer protocol (e.g. FTP)		SEMI E5 www.w3.org/Protocols/rfc959
5.12 Material Tracking System Support	required, details user specific		
5.13 Output File Format	standardized formats: - ASCII or XML for measurement results - IEEE for raw data (floating point) - JPEG (or equivalent) for raw data (image data)		ISO/IEC 8859, ISO/IEC 10646-1 www.w3.org, ISO 8879 IEEE 754, IEEE 854 ISO/IEC 10918
5.14 Network Communications Standards Support	Ethernet, Fast Ethernet		IEEE 802
5.15 SECS/GEM	required		SEMI E5
5.16 ARAMS	required		SEMI E58

NOTE 1: The particulate contamination PWP value given for the backside has not been established in commercial practice and is under further consideration by the SEMI Silicon Wafer Committee.

Table 2 Materials to be Measured

Item	*Recommended Specification*	*Comments*	*References*
1 WAFERS			
1.1 Kind of Wafers	monocrystalline, unpatterned silicon wafers with layers as specified in Table 2, Item 1.3.4		SEMI M1 (SEMI M8) (SEMI M11)
1.2 Wafer Characteristics – dimensional			
1.2.1 Wafer Diameter	200 or 300 or 200+300 mm nominal		SEMI M1 SEMI MF2074 DIN 50441-4
1.2.2 Wafer Thickness	700–850 µm	For reclaim wafers (performance as outlined in Table 3 might be reduced): 200 mm: 600–850 µ 300 mm: 650–850 µm	SEMI MF1530 DIN 50441-1
1.2.3 Edge Shape	rounded		SEMI M1 DIN 50441-2 SEMI MF928
1.2.4 Wafer Shape Range	200 mm wfrs: warp <= 100 µm, 300 mm wfrs: warp <= 200 µm		SEMI M1 SEMI MF1390 DIN 50441-5
1.2.5 Fiducial	200 mm wfrs: notch or flat 300 mm wfrs: notch		SEMI M1 SEMI MF671 SEMI MF1152 (DIN 50441-4)
1.2.6 ID Mark(s)	200 mm wfrs: user specific 300 mm wfrs: according to SEMI standards	content, type location of ID mark to be specified	SEMI M1.15 SEMI M12 SEMI M13 SEMI T7

Item	*Recommended Specification*	*Comments*	*References*
1.3 Wafer Characteristics – electrical, optical			
1.3.1 Electrical Resistivity of Wafers, Conductivity Type	0.5 mΩcm – intrinsic, p-, n-type		Res: SEMI MF673 DIN 50445 SEMI MF84 DIN 50431 Type: SEMI MF42 or DIN50432
1.3.2 Thermal Donors	annealed and not annealed		
1.3.3 Wafer Charge	no effect with respect to measurement		
1.3.4 Layers (LTO, poly-Si), Epi	LTO: thickness: 150 – 900 nm uniformity: ≤ 10% poly-Si: thickness: ≤ 2 µm uniformity: < 20% Epitaxial layer: customer specific		
1.3.5 Wafer Surface Conditions	front surface: polished, annealed, or epitaxial layer back surface: polished, acid and/or caustic etched, layers according to Item 1.3.4	optional conditions of both surfaces: etched, lapped, as cut	

Table 3 Metrology Specific Equipment Characteristics

1. REFERENCE WAFER PROPERTIES (These wafer specifications refer only to wafers to be used for verifying the performance of the measurement equipment, see Section 6.5.18. They do not refer to product wafers.)

Property	*130 nm node*	*90 nm node*	*65 nm node*
	nominal	*nominal*	*nominal*
1.1 Thickness (200 mm wafers), µm	725	725	725
1.2 Thickness (300 mm wafers), µm	775	775	775
1.3 GBIR, nm	1000	1000	1000
1.4 Site Size local flatness, mm^2	25*25	26*8	26*8
1.4.1 SBIR, including partial sites, nm	250	140	125
1.4.2 SFQR, including partial sites, nm	130	60	45
1.5 Warp, µm	30	30	30
1.6 Nanotopography, 2 mm, P-V, nm, at 0.05% defective area	20	16	10
1.7 Nanotopography, 10 mm, P-V, nm, at 0.05% defective area	70	50	35

2. MEASUREMENT FUNCTIONS

Item	*Recommended Specification*						*Comments and References*
Technology Generation	*130 nm*		*90 nm*[9]		*65 nm*[9]		
Grade	*A*	*B*	*A*	*B*	*A*	*B*	
2.1.1 Thickness (Center Point Thickness)							SEMI M1, SEMI MF1530
2.1.1.1 Level 3 Variability σ_3 (µm, 1 σ)	≤ 0.5	≤ 1	≤ 0.5	≤ 1	≤ 0.5	≤ 1	
2.1.1.2 Matching Tolerance Δ_m (µm)	≤ 0.75	≤ 1.5	≤ 0.75	≤ 1.5	≤ 0.75	≤ 1.5	
2.1.1.3 Bias (µm)	≤ 0.75	≤1.5	≤ 0.75	≤ 1.5	≤ 0.75	≤ 1.5	target until certified reference materials are available
2.1.1.4 Spatial Bandwidth f_{min} (mm^{-1}) f_{max} (mm^{-1})	0 1						Nominal value ± 5% tolerance
2.1.2 Global Flatness (GBIR)							SEMI M1 Appendix 1; SEMI MF1530; JEIDA 43
2.1.2.1 Level 3 Variability σ_3 (nm, 1 σ)	≤ 30	≤ 65	≤ 30	≤ 65	≤ 30	≤ 65	
2.1.2.2 Matching Tolerance Δ_m (nm)	≤ 50	≤ 100	≤ 50	≤ 100	≤ 50	≤ 100	
2.1.2.3 Bias (nm)	≤ 50	≤ 100	≤ 50	≤ 100	≤ 50	≤ 100	target until certified reference materials are available
2.1.2.4 Spatial Bandwidth f_{min} (mm^{-1}) f_{max} (mm^{-1})	0 1						Nominal value ± 5% tolerance
2.1.3 Local Flatness (SBIR)							SEMI M1 Appendix 1; SEMI MF1530; JEIDA 43; DIN 50441-5
2.1.3.1 Level 3 Variability σ_3 (nm, 1 σ)	≤ 8	≤ 17	≤ 4.7	≤ 9.3	≤ 4.2	≤ 8.3	
2.1.3.2 Matching Tolerance Δ_m (nm)	≤ 12	≤ 26	≤ 7	≤ 14	≤ 6.3	≤ 12.5	
2.1.3.3 Bias (nm)	≤ 12	≤ 26	≤ 7	≤ 14	≤ 6.3	≤ 12.5	target until certified reference materials are available
2.1.3.4 Spatial Bandwidth f_{min} (mm^{-1}) f_{max} (mm^{-1})	0 1						Nominal value ± 5% tolerance
2.1.4 Local Flatness (SFQR)							Specifications apply on a site-by-site basis; SEMI M1 Appendix 1; SEMI MF1530; JEIDA 43; DIN 50441-5
2.1.4.1 Level 3 Variability σ_3 (nm, 1 σ)	≤ 4.5	≤ 9	≤ 2	≤ 4	≤ 1.5	≤ 3	
2.1.4.2 Matching Tolerance Δ_m (nm)	≤ 7	≤ 13	≤ 3	≤ 6	≤ 2.3	≤ 4.5	
2.1.4.3 Bias (nm)	≤ 7	≤ 13	≤ 3	≤ 6	≤ 2.3	≤ 4.5	target until certified reference materials are available
2.1.4.4 Spatial Bandwidth f_{min} (mm^{-1}) f_{max} (mm^{-1})	0 1						Nominal value ± 5% tolerance
2.1.5 Shape (Warp, GMLYMER)							SEMI M1 Appendix 2; SEMI MF1390; JEIDA 43; DIN 50441-5
2.1.5.1 Level 3 Variability σ_3 (µm, 1 σ)	≤ 1	≤ 2	≤ 1	≤ 2	≤ 1	≤ 2	
2.1.5.2 Matching Tolerance Δ_m (µm)	≤ 1.5	≤ 3	≤ 1.5	≤ 3	≤ 1.5	≤ 3	
2.1.5.3 Bias (µm)	≤ 1.5	≤ 3	≤ 1.5	≤ 3	≤ 1.5	≤ 3	

9 The values for variability, matching and bias for the 90 and 65 nm technology nodes are rounded to one significant decimal digit for those parameters which scale with the technology generations. Otherwise the values for the 130 nm genertaion are repeated.

2. MEASUREMENT FUNCTIONS

Item	*Recommended Specification*						*Comments and References*
Technology Generation	*130 nm*		*90 nm*[9]		*65 nm*[9]		
Grade	*A*	*B*	*A*	*B*	*A*	*B*	
2.1.5.4 Spatial Bandwidth f_{min} (mm^{-1}) f_{max} (mm^{-1})	0 1						Nominal value ± 5% tolerance
2.1.6 Other Global Flatness Parameters							SEMI M1 Appendix 1; SEMI MF1530; JEIDA 43; DIN 50441-5
2.1.6.1 GFLR, GFLD	required						
2.1.7 Other Local Flatness Parameters							SEMI M1 Appendix 1; SEMI MF1530; JEIDA 43; DIN 50441-5
2.1.7.1 SPID, SFLR, SFLD, SFQD, SFSR, SFSD	required						
2.1.8 Other Shape Parameters							SEMI M1 Appendix 2; SEMI MF1390; JEIDA 43; DIN 50441-5
2.1.8.1 Sori (GFLYFER), Bow (GM3YMCD), Warp (GB3NMPR)	required						
2.2 Nanotopography							These parameters refer to flatness measurement of individual surfaces; see SEMI M43.
2.2.1 Analysis Area Size = 2 mm							
2.2.1.1 Level 3 Variability σ_3 (nm, 1 σ)	≤ 0.7	≤ 1.3	≤ 0.5	≤ 1.1	≤ 0.3	≤ 0.7	
2.2.1.2 Matching Tolerance Δ_m (nm)	≤ 1	≤	≤ 0.8	≤ 1.6	≤ 0.5	≤ 1	
2.2.1.3 Bias (nm)	≤ 1	≤ 2	≤ 0.8	≤ 1.6	≤ 0.5	≤ 1	target until certified reference materials are available
2.2.1.4 Spatial Bandwidth f_{min} (mm^{-1}) f_{max} (mm^{-1})	0.05 2.5						Nominal value ± 5% tolerance; optionally a range of f_{min} = 0.25 mm^{-1} to f_{max} = 2.5 mm^{-1}
2.2.2 Analysis Area Size = 10 mm							
2.2.2.1 Level 3 Variability σ_3 (nm, 1 σ)	≤ 2.5	≤ 5	≤ 1.7	≤ 3.3	≤ 1.2	≤ 2.3	
2.2.2.2 Matching Tolerance Δ_m (nm)	≤ 3.8	≤ 7.5	≤ 2.5	≤ 5	≤ 1.8	≤ 3.5	
2.2.2.3 Bias (nm)	≤ 3.8	≤ 7.5	≤ 2.5	≤ 5	≤ 1.8	≤ 3.5	target until certified reference materials are available
2.2.2.4 Spatial Bandwidth f_{min} (mm^{-1}) f_{max} (mm^{-1})	0.05 2.5						Nominal value ± 5% tolerance; optionally a range of f_{min} = 0.05 mm^{-1} to f_{max} = 0.5 mm^{-1}
2.3 Other Parameters							
2.3.1 Waviness	user specific						
2.3.2 Height (individual wafer surfaces)	user specific						
2.3.3 Slope	user specific						
2.3.4 Curvature	user specific						
2.3.5 Line Scans	user specific						
2.3.6 Contour Maps	user specific						
2.3.7 Data Histogram	10 or more bins per channel, arbitrarily definable, cumulative differential						
2.3.8 Edge Roll-off	user specific						
2.3.9 Additional Parameters	user specific						

3. SETUP PARAMETERS

Item	*Recommended Specification*						*Comments and References*
Technology Generation	*130 nm*		*90 nm*		*65 nm*		
Grade	*A*	*B*	*A*	*B*	*A*	*B*	
3.1 Nominal Edge Exclusion defining FQA (mm)	≥ 2		≥		≥ 1		Performance parameters are to be verified with nominal edge exclusion ≥ 2 mm. Instrument must be capable of reporting to nominal edge exclusion ≥ 1 mm. As a guide, the extended performance for nominal edge exclusion < 2 mm should not exceed the performance (σ_3, matching, bias) by more than 100 % as compared to ≥2 mm edge exclusion given appropriate reference material.
3.2 Site Patterns	For local flatness: use any site pattern compatible with SEMI M1; for nanotopography use floating sites						Recommended range for site size: 5 – 40 mm, arbitrary combination of length of rectangular sides; see SEMI M1, SEMI M43
3.3 Sorting Criteria	Sorting is performed by using logical "AND/OR" combinations of multiple parameters						
3.4 Exclusion Windows	a) > 3, curved or linear boundaries with arbitrary position anywhere on the entire wafer surface b) perimeter exclusion windows: N zones with total area covered ≤ 0.001 of total wafer area in the range R – 2 mm to R, total perimeter excluded at R – 1 mm ≤ 4% of total wafer circumference, no single zone longer than 5 mm.						a) e.g., laser mark exclusion

4. PERFORMANCE

Item	*Recommended Specification*						*Comments and References*
Technology Generation	*130 nm*		*90 nm*		*65 nm*		
Grade	*A*	*B*	*A*	*B*	*A*	*B*	
4.1 Throughput							
4.1.1 200 mm Wafers	> 60 wafers per hour						
4.1.2 300 mm Wafers	> 40 wafers per hour						
4.2 Downward Compatibility	At least one previous tool generation of supplier						Specific tools involved need to be identified
4.3 Calibration	Automated method, Certified Reference Material (CRM) to be provided by equipment supplier.						
4.3.1 Level 3 Variability Test Interval	≥ 10 measurements over a period of not less than 2 weeks (See NOTE 1.)						To be performed with throughput mode used for qualifying product wafers, 95% confidence interval has to be less than the specified σ_3
4.4 Dependence of Results on Wafer Orientation	< 1 σ_3						

NOTE 1: This recommended specification is not intended to be a requirement for a two week pre-shipment test. Performance could be verified through routine SPC (Statistical Process Control).

APPENDIX 1
SCALING MODELS

NOTICE: The material in this appendix is an official part of SEMI M49 and was approved by full letter ballot procedures on May 14, 2004.

Table A1-1 Scaling models used in Tab. 3.1 for the technology nodes 130 to 65 nm

Property	*130 nm node*	*90 nm node*	*65 nm node*
	nominal	*nominal*	*nominal*
1.1 Thickness (200 mm wafers), µm	725	no scaling	no scaling
1.2 Thickness (300 mm wafers), µm	775	no scaling	no scaling
1.3 GBIR, nm	1000	no scaling	no scaling
1.4 Site Size local flatness, mm^2	25*25	26*8	26*8
1.4.1 SBIR, including partial sites, nm	250	2/3 of (120 nm + max. SFQR per ITRS)[10]	2/3 of (120 nm + max. SFQR per ITRS)[10]
1.4.2 SFQR, including partial sites, nm	130	2/3 of max value acc. to ITRS[11]	2/3 of max value acc. to ITRS[11]
1.5 Warp, µm	30	no scaling	no scaling
1.6 Nanotopography, 2 mm, P-V, nm, at 0.05% defective area	20	2/3 of max value acc. to ITRS[11]	2/3 of max value acc. to ITRS[11]
1.7 Nanotopography, 10 mm, P-V, nm, at 0.05% defective area	70	70% of previous generation[12]	70% of previous generation[12]

10 120 nm is calculated to be the average taper contribution to SBIR for 130 nm node (SBIR – SFQR). This value is kept constant for the 90 and 65 nm technology nodes.

11 ITRS provides maximum specifications regarding starting material requirements. This maximum value is assumed to be equivalent to the upper end of range recommended for reference wafers as defined in 6.5.17. The nominal value is then 2/3 of the maximum value.

12 ITRS provides no guidance regarding Nanotopography of 10 mm analysis area

SEMI M50-1104
TEST METHOD FOR DETERMINING CAPTURE RATE AND FALSE COUNT RATE FOR SURFACE SCANNING INSPECTION SYSTEMS BY THE OVERLAY METHOD

This test method was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on August 16, 2004. Initially available at www.semi.org September 2004; to be published November 2004. Originally published November 2001.

1 Purpose

1.1 SEMI M52 defines capture rate (CR) requirements to be met by a scanning surface inspection system (SSIS) to be used for the 130 nm technology generation. Similar requirements appear in specifications for SSISs to be used in other applications.

1.2 This test method provides a framework for the determination of the CR, false count rate (FCR) and cumulative false count rate (CFCR) of an SSIS as a function of latex sphere equivalent (LSE) size of localized light scatterers (LLS).

NOTE 1: In the context of this document the term "size" refers to the LSE diameter.

2 Scope

2.1 This test method defines the SSIS capture rate and discusses its usage in industry specifications.

2.2 This test method addresses calculating and reporting SSIS capture rate from measurements of either PSL depositions or other LLS on wafers in LSE units.

2.3 Specific wafer surfaces (by wafer product, type of film or type of polish) that may affect the measured capture rate and false count rate of an SSIS are to be agreed upon between suppliers and users.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This test method is limited to use on unpatterned wafers.

3.2 This test method is limited to use on calibrated scanners operated in a production mode.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E89 — Guide for Measurement System Capability Analysis

SEMI M52 — Guide for Specifying Scanning Surface Inspection Systems for Silicon Wafers for the 130-nm Technology Generation

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

4.2 *ISO Standard*[1]

ISO Guide 30:1992 — Terms and Definitions Used in Connection with Reference Materials

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Definitions*

5.1.1 *capture rate (CR)* — the probability that an SSIS detects an LLS of latex sphere equivalent (LSE) signal value at some specified SSIS operational setting.

5.1.2 *certified reference material (CRM*) — reference material, accompanied by a certificate, one or more of whose property values are certified by a procedure which establishes its traceability to an accurate realization of the unit in which the property values are expressed, and for which each certified value is accompanied by an uncertainty at a stated level of confidence. [ISO Guide 30:1992]

5.1.3 *cumulative false count rate (CFCR)* — number of false counts of size S_f, or larger, that are expected to be recorded by an SSIS at some specified operational setting as a function of S_f. CFCR may be found by averaging false counts over multiple scans.

1 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch

5.1.4 *false count (FC)* — laser-light scattering event that arises from instrumental causes rather than from any feature on or near the wafer surface; also called false positive.

5.1.4.1 *Discussion* — False counts would not be expected to occur at the same point on the wafer surface during multiple inspection scans, and hence they could be considered as random "noise" that could be identified by examining the results of repeated scans.

5.1.5 *false count rate (FCR)* — mean total number of false counts per wafer that an SSIS reports at some specified SSIS operational setting.

5.1.6 *repeat counts* — LLSs that are found in a later scan within the scanner *XY* uncertainty distance of their location as found on an earlier scan.

5.1.6.1 *Discussion* — The implication is that if defect density is low enough, then a repeat count results from detecting the same LLS event again and is not the result of SSIS noise. Besides the absolute position of the LLS, an additional matching condition may be the LSE signal of the LLS.

5.1.7 *scanner* XY *uncertainty* — square root of the sum of the squares of the one-sigma standard deviations in the reported *X* and *Y* locations of the SSIS under test, as determined under repeatability conditions.

5.1.8 *true count* — laser-light scattering event that arises from the localized light scatterers (LLS) being investigated.

6 Summary of Method

6.1 The *XY* coordinate uncertainty of the SSIS under test is either known or determined under repeatability conditions, without removing the wafer from the stage between scans.

6.2 The reference wafer to be used in this test is selected.

6.3 The selected wafer is scanned *Z* times on the SSIS under test. The first two scans are used to qualify the reference wafer before continuing with the remaining *Z*–2 scans.

NOTE 2: Typical values for *Z* are between 30 and 100 scans.

6.4 The scans are analyzed to determine and record the number of times each LLS event occurs in each location (to within a distance approximately six times the scanner *XY* uncertainty) during the *Z* scans. The capture rate, standard size deviation, false count rate, and cumulative false count rate are determined from this data set.

7 Apparatus

7.1 *SSIS under test* — installed in its position of use with clean room rating recommended by the manufacturer.

7.2 *Off-line analysis software program* — to track each observed count and determine the capture rate, standard size deviation, the number of false counts at each LLS size, the false count rate, and the cumulative false count rate.

NOTE 3: The analysis software may be incorporated into the SSIS, if desired.

8 Test Specimens

8.1 Use any wafer with (1) natural LLS with density <10 LLS/cm^2 and (2) a surface roughness typical of the wafers to be measured in production (see Section 2.3).

8.1.1 The minimum distance between any two LLS found during any one scan and used in the data set to be analyzed shall be larger than six times the scanner *XY* uncertainty. Clusters of LLS (found in any one scan and closer together than six times the scanner *XY* uncertainty) and scratches must be excluded during the analysis.

8.1.2 Determine the scanner *XY* uncertainty from previous knowledge, from the scanner manufacturer specifications, or from the positional accuracy determined under repeatability conditions in accordance with Appendix 1.

8.2 Alternatively, a wafer with deposited polystyrene latex spheres can be used to evaluate the capture rate more accurately at a specific particle size. The same particle density, particle spacing, and defect cluster conditions as in Section 8.1 should be observed.

NOTE 4: The wafer with deposited PSL spheres may or may not be certified reference material.

9 Procedure

9.1 Qualify the wafer for appropriate LLS number (see Section 8.1) prior to taking CR and CFCR data as follows:

9.1.1 Scan the wafer once and determine position, P_m, and size, S_m, of each of the M_1 detected LLS events with $m = [1, 2, \ldots M_1]$.

9.1.2 To determine that there are enough repeating LLS events to make the CR calculation meaningful, scan the wafer a second time and compare the detected LLS events with respect to the positions of those detected during the first scan. Define the total number of LLS events that repeat their position in the first scan to within six times the scanner *XY* uncertainty as M_2. Consider the wafer qualified for the test if the share of

repeat LLS events on the wafer, M_2, is larger than 0.75 M_1. Make certain that the conditions of Sections 8.1 and 8.1.1 are fulfilled for both wafer scans.

9.2 Scan the wafer a total of Z times to obtain CR, FCR, and CFCR data (see NOTES 3 and 6). Record each LLS event detected during the Z scans according to its position P and size S.

NOTE 5: The two scans obtained in Sections 9.1 through 9.1.2 can be used as part of this data set, but the wafer must remain on the scan stage during the entire set of Z scans to perform the measurement sequence under repeatability conditions.

10 Analysis

10.1 *Initial Analysis*

10.1.1 Determine the locations on the wafer where an LLS event has been detected at least once by comparing all recorded positions (within the constraint of the six-sigma XY uncertainty) of the multiple scans as reported by the SSIS. These locations, L_i, with i = [1, 2, …,N] represent the complete set of LLS events to be used in the analysis. Each location is characterized by the number of scans H_i, in which the LLS event at that position has been detected, and by the H_i reported sizes S_{ih}, where h = [1, 2, …,H_i], for the LLS event.

10.1.2 Consider those of the N events with H_i = 1, (i.e., events seen only once) as false counts. Order these events by decreasing size, S_i. Index them by f = [1, 2, ...,F], with f = 1 representing the largest size and f = F representing the smallest.

10.1.3 Consider those events that were seen at least twice during the Z scans ($H_i \geq 2$) to be true counts.

NOTE 6: The sequence of analysis steps given below is intended to be representative and illustrative. The actual algorithms used in the analysis software may differ from these as long as the same result is achieved.

10.2 *Analysis of True Counts*

10.2.1 Determine the average size $<S_i>$ of each true count ($H_i \geq 2$) as follows:

$$< S_i > = \frac{1}{H_i} \sum_{h=1}^{H_i} S_{ih} \tag{1}$$

10.2.2 Calculate the size dependent capture rate, $CR(<S_i>)$, for every true count as follows:

$$CR(< S_i >) = \frac{H_i}{Z} \tag{2}$$

10.2.3 Plot $CR(<S_i>)$ versus $<S_i>$ as in the example in Figure 1, and interpolate or fit the data to discriminate against outlying points.

NOTE 7: The following equation for c_s, in percent,

$$c_s = 100 \left[1 - \exp\left(\frac{s_0 - s}{c_0} \right) \right], \tag{2a}$$

may be used to fit the plotted $CR(<S_i>)$ data. Here, c_s is the fitted value of $CR(<S_i>)$, s is the size ($<S_i>$), s_0 is the size at zero probability of capture, and c_0 is a curvature factor that determines the point at which the probability of capture approaches 100%. As c_0 and s_0 constitute a sufficient parameter set to describe completely $CR(<S_i>)$, they can be used for reporting, together with the chi-square goodness of the fit test statistic result.

NOTE 8: Note that there are a few points below the principal curve in Figure 1. These points may have arisen from added particles that appeared on the wafer during the test. They should be neglected in fitting any curve to the capture rate data.

10.2.4 Calculate the standard deviation of size S_i for all true counts as follows:

$$\sigma(S_i) = \sqrt{\frac{1}{H_i - 1} \sum_{h=1}^{H_i} (S_{ih} - < S_i >)^2} \tag{3}$$

10.2.5 Plot the standard deviation of size, $\sigma(S_i)$, versus the mean size, $<S_i>$, for all true counts as shown in the example in Figure 2.

NOTE 9: Again, note the same outliers in Figure 2. These can be neglected in any analysis of the standard deviation data.

10.3 *Analysis of False Counts*

10.3.1 Divide the total number of false counts, F, by the number of scans, Z, to get the false count rate, FCR:

$$FCR = \frac{F}{Z} \tag{4}$$

10.3.2 Analyze the false count rate as a function of size to determine the cumulative false count rate, $CFCR(S_i)$, at each size, S_i, by taking the total number of false counts of size equal to or greater than S_i, and dividing by the number of scans, Z:

$$CFCR(S_i) = \frac{F_i}{Z}, \tag{5}$$

where F_i is the largest value of the index associated with the count (or counts) of size S_i.

10.3.3 Plot $CFCR(S_i)$ as a function of S_i as shown in the example in Figure 3.

11 Report

11.1 Report the following information:

11.1.1 Operator identification;

11.1.2 Date of test;

11.1.3 Manufacturer, model, serial number, and software version of the SSIS being tested,

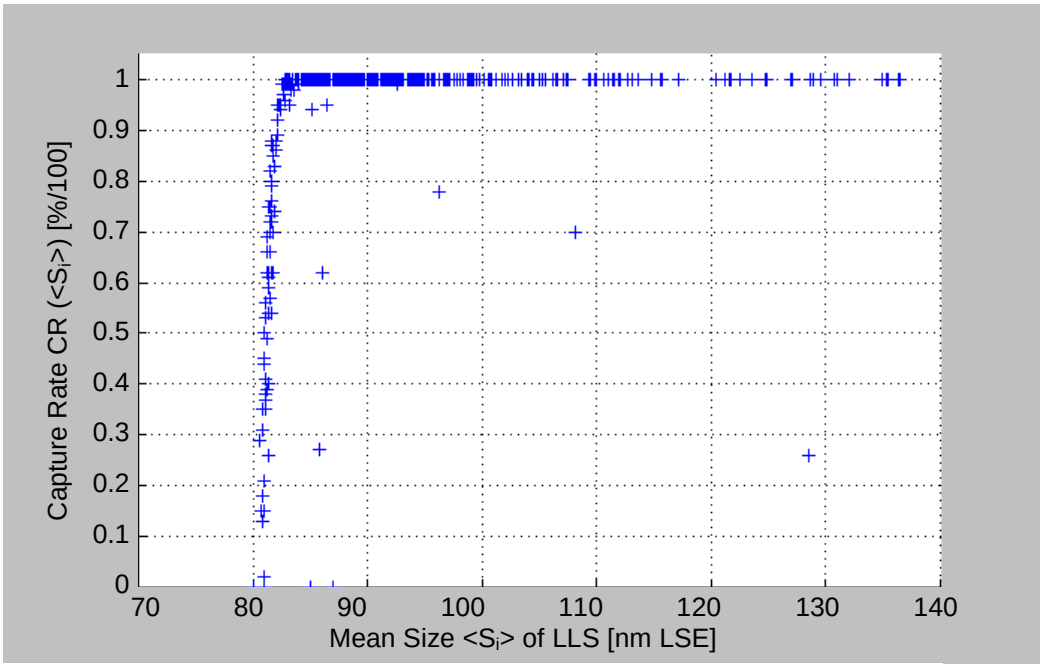
11.1.4 Description of the reference wafer used in the test.

11.1.5 Plot of the capture rate, $CR(\langle S_i \rangle)$, *vs.* the mean size, $\langle S_i \rangle$, similar to the example in Figure 1.

11.1.6 Plot of the standard deviation, $\sigma(S_i)$, of the LLS mean size, $\langle S_i \rangle$, similar to the example in Figure 2.

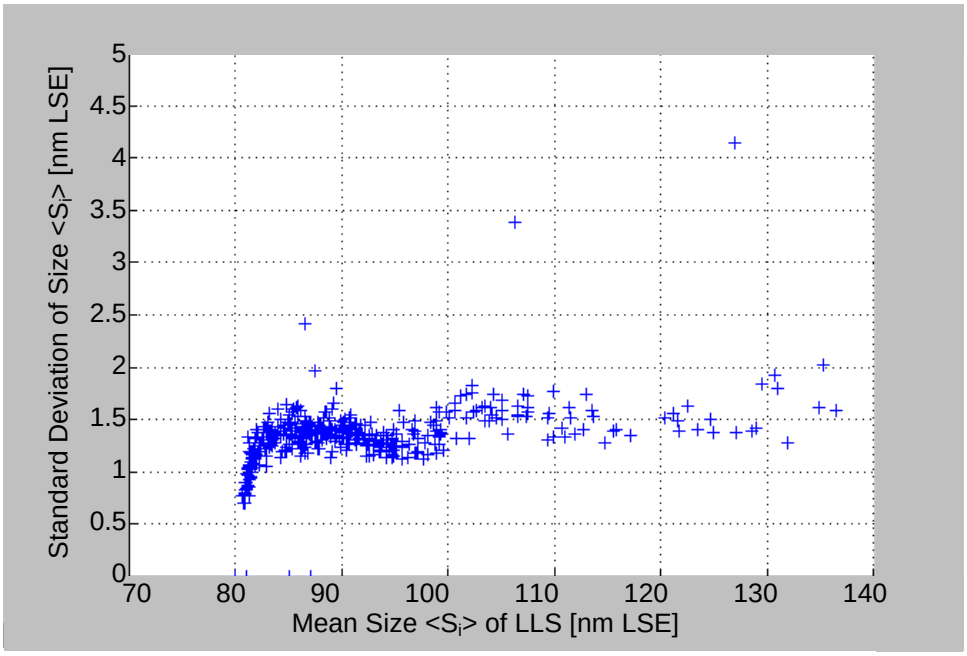
11.1.7 Calculated false count rate, *FCR*, as described in Section 10.3.2.

11.1.8 Plot of the cumulative false count rate, $CFCR(S_i)$, similar to the example in Figure 3.



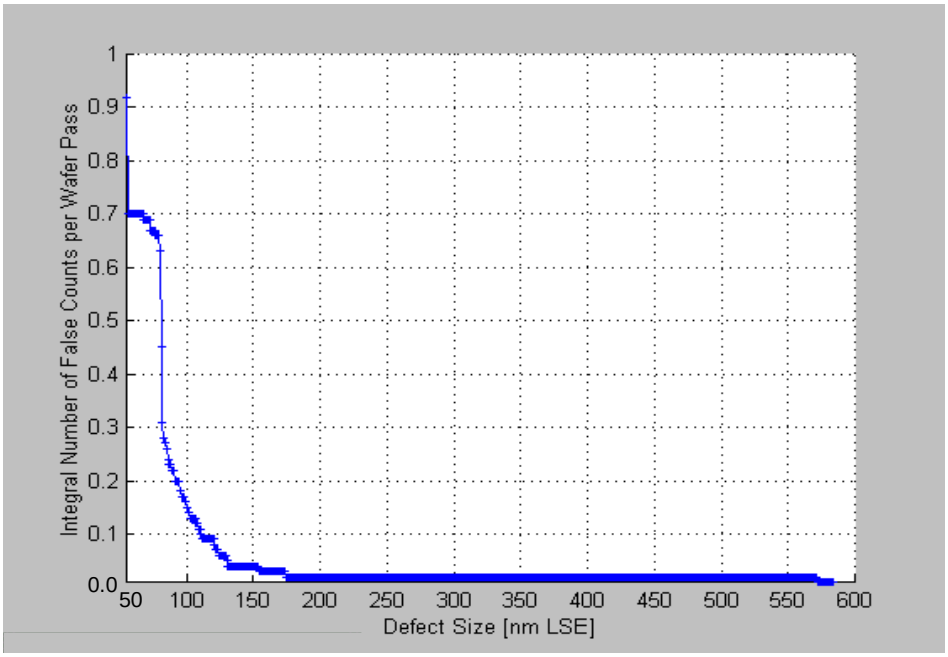
NOTE 1: This figure is an example plot of capture rate as determined in Sections 10.2.1 through 10.2.3. The measurements in this example are the result of 100 scans on a wafer with several natural LLS sites of different sizes. The SSIS noise floor was set at 80 nm LSE.

Figure 1
Capture Rate



NOTE 1: This figure is an example plot of the standard deviation of true count size as determined in Sections 10.2.4 and 10.2.5.

Figure 2
Standard Size Deviation



NOTE 1: This figure is an example plot of cumulative false count rate as determined in Sections 10.3.1 through 10.3.3. This is the same data set used for Figures 1 and 2; however, the horizontal scale has been expanded.

Figure 3
Cumulative False Count Rate (CFCR)

APPENDIX 1
DEFAULT PROCEDURE FOR DETERMINATION OF SCANNER *XY* UNCERTAINTY

NOTICE: The material in this appendix is an official part of SEMI M50 and was approved by full letter ballot procedures on April 22, 2004 by the North American Regional Standards Committee.

A1-1 Purpose

A1-1.1 This procedure is intended to be used for determining the scanner *XY* uncertainty for the scanning surface inspection system (SSIS) under test when this information is not otherwise available.

A1-2 Scope

A1-2.1 This appendix covers a procedure for determining ability of an SSIS to report the location of a localized light scatterer (LLS) on a silicon wafer surface under repeatability conditions.

NOTICE: This appendix does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this procedure to establish appropriate safety health practices and determine the applicability of regulatory or other limitations prior to use.

A1-3 Limitations

A1-3.1 If particles are used as the reference LLSs, care must be taken both to avoid contamination by interfering particles and to avoid removal of the reference particles.

A1-4 Referenced Standards

A1-4.1 *SEMI Standards*

SEMI E89 — Guide for Measurement System Capability Analysis

SEMI M1 — Specification for Monocrystalline Polished Silicon Wafers

SEMI M20 — Specification for Establishing a Wafer Coordinate System

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Polystyrene Latex Spheres on Unpatterned Semiconductor Wafer Surfaces

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

A1-5 Terminology

A1-5.1 Terms related to SSIS operation are defined in Section 5 of this standard and in SEMI M53.

A1-5.2 Terms related to uncertainty and repeatability are defined in SEMI E89.

NOTE 1: The current edition of SEMI M89 defines the repeatability used in this procedure as “static repeatability.”

A1-6 Summary of Procedure

A1-6.1 A reference silicon wafer with at least ten identifiable and stable LLSs (relatively large, isolated particles or pits) located on its polished surface is scanned ten times by the SSIS under test without removing it from the SSIS between scans.

A1-6.2 For each scan, a map of the positions associated with the specified laser light scattering events arising from scattering from the LLSs on the wafer surface is obtained and the coordinates of these events are recorded.

A1-6.3 The coordinate data set is filtered to remove coordinates not associated with the selected LLSs.

A1-6.4 The sample standard deviations (x and y) are used to estimate the repeatability of the reported locations, and the scanner *XY* uncertainty is calculated as the quadrature sum of the x- and y-sample standard deviations.

A1-7 Apparatus

A1-7.1 *SSIS under test* — as defined in Section 7 of this standard with characteristics as outlined in SEMI M53.

A1-8 Reference Wafer

A1-8.1 The reference wafer shall meet the dimensional requirements of SEMI M1 for the largest diameter of wafer to be inspected by the SSIS under test.

A1-8.2 The surface of the reference wafer shall contain at least ten LLSs (particles or pits) of a size (LSE) well above the threshold, so that the capture rate is ~100%.

A1-8.3 These ten or more LLSs must be distributed over the entire surface of the wafer.

A1-9 Procedure

A1-9.1 Load the reference wafer into the SSIS with the fiducial (flat or notch) located in accordance with customary operating procedures of the laboratory conducting the test.

A1-9.2 Scan the wafer and create a data set containing the reported *x* and *y* coordinates of each of the ten or more selected LLSs.

A1-9.3 Call this scan, Scan 1.

A1-9.4 Repeat the scans, nine more times, and create nine more data sets containing the reported *x* and *y* coordinates of each of the ten or more selected LLSs.

A1-10 Calculations

A1-10.1 Examine each of the data sets (either as wafer maps or mathematically) to determine that coordinate pairs for each of the ten or more LLSs being analyzed appear in each of the ten scans.

A1-10.2 Delete from the data any coordinate pair that does not appear in all ten data sets.

A1-10.3 Determine the average and the sample standard deviation of *x* and *y* coordinates of each of the *N* remaining coordinate pairs as follows:

$$\bar{x}_i = \frac{1}{10}\sum_{k=1}^{10} x_{ik} \text{ and } \bar{y}_i = \frac{1}{10}\sum_{k=1}^{10} y_{ik} \tag{A1}$$

$$s_{xi} = \frac{1}{3}\sqrt{\sum_{k=1}^{10}(x_{ik} - \bar{x}_i)^2} \text{ and } s_{yi} = \frac{1}{3}\sqrt{\sum_{k=1}^{10}(y_{ik} - \bar{y}_i)^2} \tag{A2}$$

where:

$\bar{x}_i$ = average of the ten *x* coordinates reported for the i^{th} LLS,
$\bar{y}_i$ = average of the ten *y* coordinates reported for the i^{th} LLS,
s_{xi} = sample standard deviation of the ten *x* coordinates reported for the i^{th} LLS,
s_{yi} = sample standard deviation of the ten *y* coordinates reported for the i^{th} LLS, and
k = scan number (from 1 to 10).

A1-10.4 Calculate the pooled sample standard deviations of the reported *x* and *y* coordinates as follows:

$$S_x = \sqrt{\left(\frac{1}{N}\right)\sum_{i=1}^{N} s_{xi}^2} \text{ and } S_y = \sqrt{\left(\frac{1}{N}\right)\sum_{i=1}^{N} s_{yi}^2} \tag{A3}$$

where:

S_x = pooled sample standard deviation of the ten *x* coordinates reported for the N LLSs,
S_y = pooled sample standard deviation of the ten *y* coordinates reported for the N LLSs, and
N = number of coordinate pairs appearing in all ten scans.

A1-10.5 Calculate and record the scanner *XY* uncertainty as follows:

$$S = \sqrt{(S_x^2 + S_y^2)} \tag{A4}$$

SEMI M51-0303
TEST METHOD FOR CHARACTERIZING SILICON WAFERS BY GATE OXIDE INTEGRITY

This test method was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved by the Japanese Regional Standards Committee on January 10, 2003. Initially available at www.semi.org January 2003; to be published March 2003. Originally published July 2002.

NOTICE: This document was rewritten in its entirety in 2002.

1 Purpose

1.1 This test method describes procedures for characterizing silicon wafers to determine Gate Oxide Integrity (GOI). This test method is effective in evaluating the density of Crystal Originated Particles (COP) in polished Czochralski (CZ) silicon wafers that influence GOI.

2 Scope

2.1 This test method provides detailed procedures for characterizing silicon wafers using GOI. This test method describes standard procedures for Metal Oxide Semiconductor (MOS) fabrication, electrical measurement, analysis, and reporting.

2.2 Thermally grown gate oxide films with gate oxide thicknesses ranging from 20–25 nm and polysilicon electrodes are used as MOS capacitors. Discussion of the gate oxide thickness is given in a later section.

2.3 Time Zero Dielectric Breakdown (TZDB) is used as the electrical characterization method of MOS capacitors.

2.4 It is well known that oxygen precipitates are also a source of gate oxide defects.[1] However, this is beyond the scope of this standard because the as-received wafers contain only a small amount of oxygen precipitate.

NOTE 1: The polysilicon film can make standard test results applicable to the testing of wafers used to fabricate integrated circuits rather than other metal electrodes because polysilicon electrodes are commonly used in actual devices.

NOTE 2: The TZDB method measures oxide breakdown electric fields using MOS capacitors. The density of COPs can be estimated from a histogram of the breakdown electric field.

NOTE 3: For a detailed discussion of sample structures for this test method, the reader is referred to EIA/JEDEC Standard 35-1. In general, the three most likely sample structures are simple planar MOS capacitors, MOS capacitors with various isolation structures (for example, local oxidation of silicon (LOCOS), shallow trench isolation (STI)), and field effect transistors (FET). For the purpose of silicon wafer characterization, the simple planar MOS capacitor structure is preferable. This is because with the various isolation structures and FET, silicon wafers sometimes receive thermal treatments during the complicated sample fabrication process. Therefore, it is questionable to look upon a measurement of one of the latter two wafers as the starting silicon wafer characterization.

NOTE 4: This standard is based on round robin results among silicon wafer manufacturers. In general, the COPs in the polished CZ silicon substrates strongly influence the TZDB histogram of the gate oxide. This GOI test method strongly depends on wafer-surface/near-surface crystal defects, contaminations, particles and cleanliness of the MOS fabrication processes environment. Cleanliness of the processes environment should be evaluated because it strongly affects the MOS characteristics. (See Section 5.2.1 and Related Information 1).

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI C3.6 — Standard for Phosphine in Cylinders 99.98% Quality (Provisional)

SEMI C3.21 — Standard for Carbon Tetrafluoride in Cylinders (Provisional)

SEMI C3.22 — Standard for Oxygen, 99.5% Quality

SEMI C3.23 — Standard for Oxygen, 99.98% Quality

SEMI C3.28 — Standard for Nitrogen, VLSI Grade in Cylinders, 99.9996% Quality

SEMI C3.41 — Standard for Oxygen, Bulk, 99.9998% Quality (Provisional)

SEMI C3.49 — Standard for Bulk Nitrogen, 99.99999% Quality (Provisional)

SEMI C3.54 — Gas Purity Guideline for Silane

1 K.Yamabe and K.Taniguchi, "Time-Dependent Dielectric Breakdown of Thin Thermally Grown SiO2 Films", *J. Solid St. Circuits*, SC-20, 343 (1983).

SEMI C21 — Specifications and Guidelines for Ammonium Hydroxide

SEMI C27 — Specifications and Guidelines for Hydrochloric Acid

SEMI C28 — Specifications and Guidelines for Hydrochloric Acid

SEMI C30 — Specifications and Guidelines for Hydrogen Peroxide

SEMI C35 — Specifications and Guidelines for Nitric Acid

SEMI C38 — Guideline for Phosphorus Oxychloride

SEMI C41 — Specifications and Guidelines for 2-Propanol

SEMI C44 — Specifications and Guidelines for Sulphuric Acid

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

3.2 *ASTM Standards*[2]

ASTM D5127 — Standard Guide for Ultra Pure Water Used in the Electronics and Semiconductor Industry

ASTM F1241 — Terminology of Silicon Technology

ASTM F1771 — Standard Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique

3.3 *EIA/JEDEC Standards*[3, 4]

EIA/JEDEC 35 — Procedure for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-1 — General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-2 — Test Criteria for the Wafer-Level Testing of Thin Dielectrics

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Abbreviations & Acronyms*

4.1.1 COPs — Crystal Originated Particles

4.1.2 GOI — Gate Oxide Integrity

4.1.3 LOCOS — LOCal Oxidation of Silicon

4.1.4 MOS — Metal Oxide Semiconductor

4.1.5 STI — Shallow Trench Isolation

4.1.6 TZDB — Time Zero Dielectric Breakdown

4.2 *Definitions*

4.2.1 Many terms relating to silicon technology are defined in ASTM Terminology F1241.

4.2.2 Definitions for some additional terms are given in SEMI M1 and ASTM F1771.

4.2.3 Other terms are defined as follows:

4.2.3.1 *crystal originated particles*[5] *(COPs)* — this is one of the grown-in defects of CZ silicon wafers with an octahedral structure. It was discovered as particles appeared on the silicon surface during repetitive RCA SC-1[6] cleaning.

NOTE 5: It has been thought that COPs are one of the main origins of GOI degradation. The gate oxide formed on the silicon surface at which the COPs appear breaks down easily at the corner of an octahedral shape like a silicon trench.[7, 8] The oxide electric field is enhanced at that place. The breakdown electric field is weakened.

4.2.3.2 *failure modes* — The breakdown failure results are summarized in terms of the range of the oxide electric field in which the breakdown occurred. One set of categories (A, B and C for TZDB) widely used[9, 10] is as follows:

- *A mode failure*: 0 MV/cm $\leq E_{bd} <$ 3 MV/cm
- *B mode failure*: 3 MV/cm $\leq E_{bd} <$ 8MV/cm
- *C mode failure*: 8 MV/cm $\leq E_{bd}$

NOTE 6: Discussion on failure modes:

- *A mode failure*: Initial short

2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

3 Electronic Industries Alliance, EIA Engineering Department, Standards Sales Office, 2001 Eye Street, NW, Washington, D.C. 20006, USA. Website: www.eia.org

4 Joint Electron Device Engineering Council, 2500 Wilson Blvd., Arlington, VA 22201, website: www.jedec.org

5 J. Ryuta, E. Morita, T. Tanaka and Y. Shimanuki, "Crystal – Originated Singularities on Si Wafer Surface after SC1 Cleaning", *Jpn. J. Appl. Phys*. 29(1990) L1947.

6 W. Kern and D. Puotinen, "Clean Solution Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology", *RCA Rev*., 31, 187(1970).

7 T. Mera, J. Jablonski, K. Nagai, and M. Watanabe, "Grown-in defects in silicon crystals responsible for gate oxide integrity deterioration", *Ohyo-Buturi*, 66(7), 728 (1997).

8 K.Yamabe and K.Imai, "Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation", *IEEE Trans. Electron Devices*, ED-34,1681 (1987) .

9 K. Yamabe, K. Taniguchi, and Y. Matsushita, "Thickness Dependence of Dielectric Breakdown Failure of Thermal SiO2 Films", *Reliability Physics – 21st Annual Proceedings*, 1983, p.184.

10 K. Yamabe, Y. Ozawa, S. Nadahara, and K. Imai, "Thermally Grown Silicon Dioxide with High Reliability", in "*Semiconductor Silicon 1990"*, ECS Proceedings Volume 90-1, pp. 349-363.

This failure mode is caused by pinholes of the oxide films formed in the gate oxide process. COPs do not cause these oxide pinholes.

- *B mode failure*: Accidental breakdown

COPs are a main origin of this failure. This failure mode influences reliability of MOS devices and MOS integrated circuits.

- *C mode failure*: Fatigue breakdown

This failure mode is partly caused by COPs, but is almost a wearout breakdown. These categories have traditionally been used for oxide thicknesses of about 20–25 nm. For thinner films, care must be taken in their use and in proper derivation of the oxide field strength as described in Related Information 1.

4.2.3.3 *time zero dielectric breakdown (TZDB)* — this is one of the electrical characteristics of dielectric films. This characteristic is contrasted with time dependent dielectric breakdown.[11, 12]

4.2.3.3.1 *Discussion* — An applied bias, for which the oxide leakage current goes over a predetermined value, I_{bd}, is measured as a breakdown gate voltage. The breakdown electric field is defined by the gate breakdown voltage normalized by the gate oxide thickness.

5 Summary of Method

5.1 *Overview* — This test method involves fabricating an array of many similar MOS capacitors on silicon wafers, measuring the TZDB voltage histogram by applying step voltage to the MOS capacitors while monitoring the oxide leakage current, and estimating the dielectric breakdown defect density caused by the silicon wafers. The defect is estimated from the B-mode failure fraction. This test is for characterizing silicon wafers and is very useful in evaluating the crystal defects (mainly COPs) of mirror-polished CZ silicon wafers.

5.2 *MOS Capacitor Fabrication Process* — Many MOS capacitors are formed on the test wafer. The MOS capacitor fabrication process consists of wafer cleaning, thermal oxidation, polysilicon deposition, phosphorous doping, activation heat treatment, photolithography and polysilicon etching.

5.2.1 *Fabrication Environment* — It is necessary to fabricate MOS capacitors in a clean room environment of 1000 class or better in total quality. That is, it needs to be confirmed that the A-mode failure rate is 10% or less. The A-mode failure depends not only on the particle density in the work environment atmosphere but also on ultra pure water, fixtures, process apparatus, clean cloths, operation rules, etc. Heavy contamination by alkaline metals, heavy metals and so on has an important effect on the TZDB of the oxide.

5.2.2 *Wafer Cleaning* — To characterize the as-received silicon wafers, the wafers shall not be cleaned. If they might contaminate a furnace, the wafers shall be cleaned before oxidation. In these cases, the wafers are generally cleaned by a modified RCA method[6]. The cleaning method shall be confirmed in advance so that the previously mentioned condition for the A-mode failure is met.

5.2.3 *Thermal Oxidation* — The gate oxide of the MOS capacitor is thermally grown. It is desirable to fix the oxidation conditions. Because the oxidation temperature influences the rate of oxidation,[13] which influences the oxide film thickness and thus the gate oxide quality, it is recommended that the gate oxide of 20-25 nm is grown in dry oxygen ambient at 850–950°C. The addition of HCl or water vapor to the oxidation ambient can cause underestimation of the oxide defect density. As a result, one evaluation result of a gate oxide formed under a special oxidation condition cannot be compared with another obtained under standard oxidation condition. To measure oxide film thickness, a monitor wafer is oxidized together with the sample wafers. An average value of 5 or more points on the monitor wafer is adopted as the oxide thickness.

5.2.4 *Electrode Formation* — A polysilicon layer with a thickness of 200~400 nm and a sheet resistance of 20-50 Ω/sq is formed by low-pressure chemical vapor deposition (LP-CVD). There are generally *in-situ* and *ex-situ* phosphorous doping methods.

5.2.5 *Ex-situ Phosphorous Doping* — After the undoped polysilicon film is formed by the LP-CVD method, phosphorous is diffused using $POCl_3$ as phosphorous source.

5.2.6 *In-situ Phosphorous Doping* — The phosphorous-doped polysilicon is deposited using an *in-situ* doping LP-CVD, followed by a heat treatment to activate the doped phosphorus.

NOTE 7: If the resistance of the polysilicon electrode films is too high, the voltage drop that results within the electrode cannot be neglected. In this case, the oxide leakage current is decreased in the range of the higher electric field. On the other hand, if the phosphorus doping is too high and the

11 D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown", Proc. *Int. Reliability Physics Symposium*, 1979, p.1

12 E. S. Anolick and G. R. Nelson, "Low Field Time Dependent Dielectric Integrity", Proc. *Int. Reliability Physics Symposium*, 1978, p.8

13 B.E.Deal and A.S.Grove, "General relationship for the thermal Oxidation of Silicon", J.Appl.Phys., 36, 3770 (1965).

resisitivity is too low, the gate oxide dielectric characteristics degrade. Too thin a polysilicon electrode makes self-healing of oxide weak spots easier. This self-healing causes the oxide breakdown defect density to be underestimated. Too thin polysilicon electrode also causes the TZDB measurement to be degraded by mechanical stress resulting from an exploring probe such as a tungsten probe. With too thick of a polysilicon electrode in the *ex-situ* doping technique, it is easy to induce a depletion layer of phosphorus near the polysilicon/SiO_2 interface that causes parasitic resistance and unnecessary voltage drop in the measurement circuit. It is desirable to monitor the thickness and sheet resistance of the polysilicon layers in every processing batch using a monitor wafer.

5.2.7 *Photolithography Process* — The MOS capacitors electrodes are formed by patterning in the photolithography. EIA/JEDEC Standards 35, 35-1, 35-2 are referred to regarding this mask design. The appropriate area and the appropriate number of MOS capacitors for each defect density shall be selected in order to detect crystal defects. For the evaluation of COPs, it is necessary to measure 100 or more MOS capacitors with a gate area of about 10 mm^2 on a wafer. (See Table R1-3 in Related Information 1.) For spares, it is desirable to prepare the plural MOS capacitors with the same gate area within each chip.

5.2.8 *Etching Processes* — The photo resist pattern formed by the photolithograph technique is used as a mask for polysilicon etching. Generally, either a wet etching method or a dry etching method is applied to polysilicon etching. If a wet etching method is applied, the etching rate shall be well controlled. If the peripheral oxide of the electrode is removed, it is sometimes difficult to accurately measure the TZDB. If a dry etching method is applied, especially RIE, care shall be taken with the charging-up of the MOS capacitors. In cases where the A-mode defect density is high, the MOS capacitors shall be confirmed not to be charged up during the etching process. If an ashing removal is carried out with the photo resist, care shall be taken with the charging-up of the MOS capacitors. As with RIE, in cases where the A-mode defect density is high, the MOS capacitors shall be confirmed not to be charged up during the ashing removal process. If there are oxide and polysilicon film on the backside of the wafer, those shall be removed.

5.3 *Measurement of the Electrical Characteristics of MOS Capacitors*

5.3.1 The dielectric breakdown defect density of silicon oxide is evaluated by the TZDB method for MOS capacitors. In the TZDB method, the gate oxide electric field of an MOS capacitor is continuously increased in stepwise fashion. The electric field applied to the gate oxide when the gate oxide leakage current exceeds the predetermined dielectric breakdown judgment value is defined as the oxide dielectric breakdown field. From a histogram of the breakdown fields for 100 or more MOS capacitors, the dielectric breakdown defect density is estimated.

5.3.2 We can see two characteristics of the formed MOS capacitors from the current-voltage (I–V) plots. Firstly, deviation of the gate oxide thickness appears in a loose distribution of the I-V plots. Secondly, if the I-V curves bend suddenly and have gentle slope in the high voltage region, there may be high parasitic resistance, for example, high resistance in the polysilicon electrode. In such a case, the reliable measurement demands the adjustment of the MOS preparation process.

5.3.3 *Applied Step Voltage*

NOTE 8: For a reliable measurement, a voltage source with a well-defined output shape shall be used. An overshooting of the applied step voltage decreases the apparent oxide breakdown voltage as compared with a real breakdown voltage. In the TZDB measurement, the constant voltage is held after a predetermined period and the oxide leakage current is measured. Next, the applied voltage increases stepwise. This procedure is repeated. If the holding time is shorter than 100 ms, the voltage may not be stable enough to allow the current to be measured. 800 ms may be enough to achieve a stable voltage. Especially, in the high electric field region, the gate oxide may receive electric stress similar to time dependent dielectric breakdown (TDDB). A holding time of 200 ms is recommended. Accordingly to the round robin result as described in Related Information 1, there are no problems in setting the holding time to 100–800 ms. The recommended step height of the applied voltage is between 0.1–0.5 MV/cm in electric field. The polarity of the voltage is selected for the Si surface so as to be in accumulation. That is, for p-type silicon wafers, the gate electrodes are negatively biased. The maximum electric field is 15 MV/cm. Even if a gate voltage corresponding to more than 15 MV/cm is applied, the voltage is not effectively applied to the gate oxide because of a voltage drop due to parasitic resistance. In the case of n-type silicon wafers, the applied electrodes shall be positively biased.

5.3.4 *Breakdown Judgment*

5.3.4.1 The oxide dielectric breakdown is judged by the predetermined oxide leakage current. That is, when the gate oxide leakage current exceeds the dielectric breakdown judgment current, the applied voltage is defined as the breakdown voltage. The breakdown electric field is the value that the breakdown voltage is normalized by the gate oxide thickness.

5.3.4.1.1 *Discussion* — If the dielectric breakdown judgment current is too high ($Ig > 10^{-3}$ A), some of the proper A-mode failures can be counted as B-mode failures because of the series resistance of the samples or measurement system. Otherwise, if the dielectric breakdown judgment current is too low ($Ig < 10^{-7}$ A),

some of the proper C-mode events in which the gate oxide was not broken down are counted B-mode failures. Both cases will be taken as a mistake in the classification of the failure modes, even if the measurement is accurately done and the appropriate I-V curves measurements are achieved. A dielectric breakdown judgment current of 10^{-5} A is recommended.

6 Significance and Use

6.1 This standard gives instructions of the procedure for characterizing mirror-polished, p-type CZ silicon wafers by measuring the dielectric breakdown defect density in the thermally grown gate oxide film using the MOS capacitors. The MOS capacitors must be formed in accordance with the fabrication process described in Section 5 that influences the oxide characteristics.

6.2 It is well known that both the silicon surface morphology and the cross-sectional structure at the pattern edge of the active region of the MOS devices influences the dielectric breakdown of the gate oxide. Various kinds of contaminations also influence the dielectric breakdown of the gate oxide. Contamination by alkaline or heavy metals and organic particles increases as the sample fabrication process progresses. Furthermore, COPs increase with increasing SC-1 treatment. These facts indicate that it is desirable to simplify the sample structure and its fabrication processes to characterize a silicon wafer by TZDB of the gate oxide. Thermal processes can cause growth of oxygen precipitates in a silicon wafer. This standard cannot be applied to silicon wafers that might receive such thermal processes.

6.3 The appropriate area and the appropriate total number of the tested MOS capacitors shall be chosen so as to answer the purpose of this standard test. For example, as shown in Table R1-3, it is suitable to select a gate electrode area of 10 mm^2 and a total number of capacitors of more than 100.

6.4 The electrode material of the MOS capacitors has a great influence on the dielectric breakdown of the gate oxide. Polysilicon is specified as the electrode material in this standard. It is applied to practical ultra large-scale integrated circuits (ULSI). The polysilicon electrode yields test results highly consistent with the actual ULSI performance.

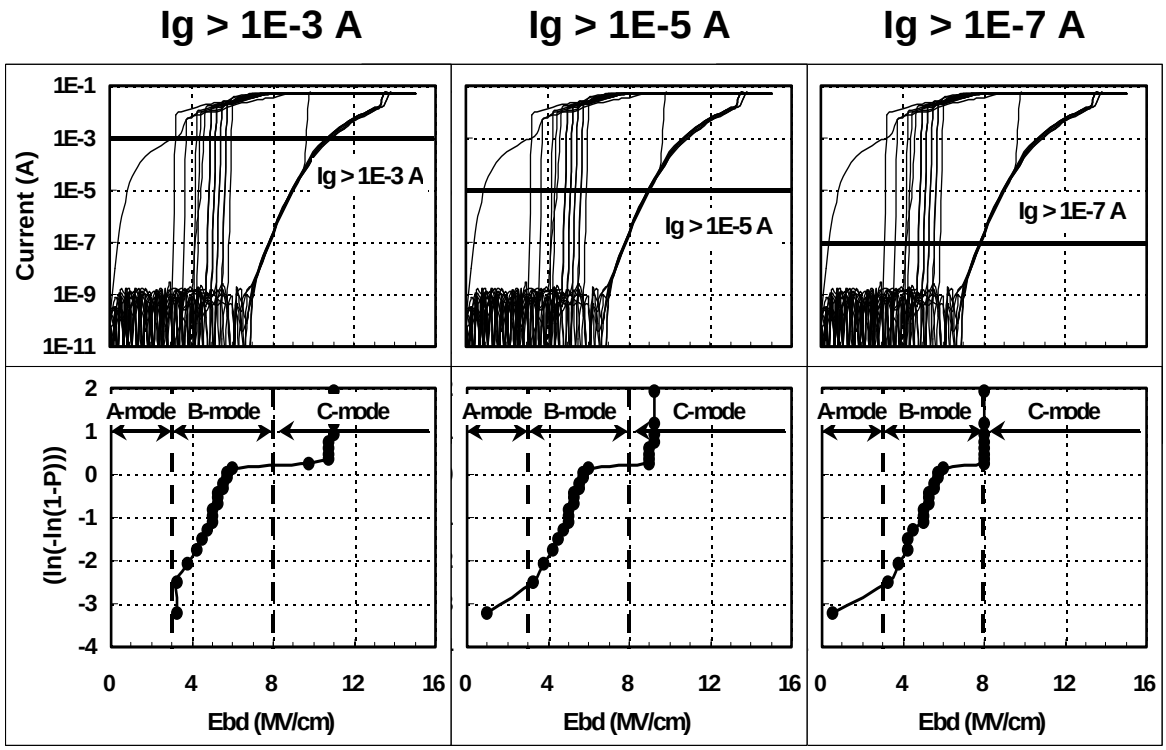


Figure 1
Comparison of Judgment Conditions

7 Interferences

7.1 Since this is a DC measurement, care must be taken to make sure that the silicon wafer has a low resistance ohmic contact. There must be no dielectric film on the back surface, e.g. silicon oxide, in order to effectively apply a voltage bias to the gate oxide. It is not necessary for this to be done with a metallic contact to the back surface of the wafer under test.

7.1.1 However, when the vacuum chucking is weak, care must be taken because of the possibility that the dielectric breakdown voltage of the gate oxide is not accurately measured due to an increase in parasitic resistance.

7.2 It is strongly suggested that testing be done with a voltage polarity such that the silicon surface will be in accumulation below the gate oxide, that is, negative voltages for p-type silicon wafers. If the polarity of the voltage is chosen to be in the reverse direction, the breakdown voltage may not be accurately measured due to the presence of a depletion layer below the gate oxide.

7.3 Evaluation and control of electrical noise in the current-voltage data, as part of this test method are crucial to the proper identification of the failure criteria.

7.4 In the TZDB measurement, lowering of the electrical noise under a low bias stress condition is made possible by the averaging of measurement data. While the required 100 ms holding time may be set using a delay in the measurement loop, an additional, uncontrolled delay may be incurred due to the autoranging of an electrometer. The effect is most pronounced for very low oxide leakage currents, where the measured value is several orders of magnitude below the minimum range set by the electrometer software.

7.5 Mechanical stress by the exploring probe can influence the measurement results, because the exploring probe is in contact with the gate electrode directly on the gate oxide.

7.6 The actual results obtained depend somewhat on the sample fabrication process. Care must be taken to ensure consistent processing.

7.7 Wafer temperature during testing shall be clearly defined. Large temperature variations might have an impact on results.

7.8 *Precaution* — Since the voltages and currents involved are potentially dangerous, appropriate means of preventing the operator from coming into contact with the exploring probe or other charge surfaces shall be in place before testing.

7.9 This standard does not include any clauses relating to the safety and sanitation of the environment. Those who intend to implement this standard shall consider appropriate means to prevent any accidents or disasters, as well as taking responsibility for maintaining a state of safety, health and hygiene for users.

8 Apparatus

8.1 The MOS capacitors shall be fabricated in an environment of 1000 class or better in total quality to prevent various contaminations. Contamination control in the processes from the wafer cleaning step to the polysilicon deposition step is especially important. Contamination during those processes has been reported to degrade GOI. Therefore, attention must be paid to those processes in particular.

8.2 High purity deionized water and high purity chemicals of electronics industry grade shall be used in the processes of wafer cleaning, wet etching, etc. The chemical/pure water grade and guide are referenced in SEMI Standards C21, C27, C28, C30, C35, C38, C41, and C44; and ASTM D5127.

8.3 In thermal processes such as gate oxidation, polysilicon deposition, and phosphorus doping, fluctuations in process temperature may affect the uniformity of oxide thickness, polysilicon thickness, and the concentration and distribution of doped phosphorus atoms. The temperature fluctuation of used furnaces shall be within ± 5°C at the most.

8.4 Quartz is very resistant to the strong acids—excluding hydrofluoric acid—and alkalis used in wet processes and at temperatures higher than 1000°C. Therefore, quartz vessels, tubes, and so on are quite frequently used in the ULSI manufacturing processes. High-purity quartz vessels and tubes of electronics industry grade shall also be used in this MOS capacitor fabrication process.

8.5 High-purity gases of electronics industry grade, such as N_2, O_2 and SiH_4, shall be used in the processes of thermal oxidation, polysilicon deposition, phosphorous doping, and so on to prevent contamination from the gases. The process gas grade and guide are referred in SEMI Standards C3.6, C3.21, C3.22, C3.23, C3.28, C3.41, C3.49, and C3.54.

8.6 A criterion for evaluating a clean room environment where MOS samples are fabricated for this test method is that the A-mode failure percent of the samples with 20–25 nm oxide is less than 10%. It is advisable that the level of cleanliness of the clean room environment where the tested MOS capacitors are fabricated is evaluated by TZDB measurement of the MOS capacitors on an epitaxial wafer.

8.7 ASTM standard F1771 shall be applied for measurement equipment such as voltage source units and manual probing machines.

9 Sampling

9.1 Sampling is the responsibility of the user of this test method. However, if testing is done as part of comparison or correlation, all participants shall agree upon sampling in advance.

NOTE 9: Refer to the appendix of JEDEC 35 for a good discussion of sampling plan statistics.

10 Procedure

10.1 *Fabrication of MOS Capacitors*

10.1.1 It shall be confirmed first that the environment for fabricating MOS capacitors is suitable for this test method. The environment includes clean room, chemicals, ultra pure deionized water, oxidation furnace, polysilicon deposition equipment, different kinds of quartz jigs, etc. As a criterion for evaluating the suitability of an environment, the A-mode failure percent of the MOS capacitors made in the environment shall be less than 10%.

10.1.2 To characterize proper silicon wafers, the wafers shall not be cleaned. If the wafers might contaminate a furnace, they shall be cleaned before oxidation. In these cases, the wafers are cleaned by a modified RCA method, in general.

10.1.3 Input oxidation parameters in the used furnace system. The parameters include oxidation temperature, ambient, gas flow rate, oxidation time, etc. A recommended oxidation temperature is 850–950°C. The appropriate parameters for obtaining the recommended oxide thickness (20–25 nm) shall be found out in advance by preliminary testing.

10.1.4 Oxidize the wafers into dry oxygen ambient. Some reference wafers shall be treated together with the sample wafers to monitor the oxide thickness and sheet resistance of polysilicon electrodes. The number of reference wafers shall be decided on by the users of this test method, taking into account of the quantity of the total wafers in the batch.

10.1.5 Measure the oxide thickness of the reference wafers by ellipsometry (or another optical method) to confirm the uniformity of the oxide thickness within the wafers. The average thickness shall be in the range 20–25 nm and the dispersion within a wafer shall be less than ± 3%.

10.1.6 Input deposition parameters of polysilicon into a used LP-CVD furnace system. The parameters include deposition temperature, pressure, gas flow rate, deposition time, etc. The appropriate conditions for obtaining the recommended polysilicon thickness (200–400 nm) shall be found out in advance by preliminary testing. If a doped polysilicon film will be deposited, corresponding deposition parameters shall be input.

10.1.7 Deposit a polysilicon film on the wafers oxidized. The recommended deposition temperature for this test method is 570–640°C. Some reference wafers with an oxide shall be treated together with the sample wafers to monitor the polysilicon thickness. The oxide thickness on the reference wafers shall be recommended by a vendor of equipment to measure the thickness of the polysilicon films. The number of reference wafers shall be decided on by the users of this test method taking into account the total quantity of wafers in the batch.

10.1.8 Measure the polysilicon thickness on the reference wafers using a spectroscopic reflectometer (or other optical film thickness measurement instruments) to confirm the uniformity of the polysilicon film thickness within a wafer and within a batch. The average polysilicon film thickness shall be 200–400 nm and dispersion within a batch shall be less than ± 10%. If doped polysilicon was deposited, proceed to Section 10.1.11.

10.1.9 Input the doping parameters to a phosphorus-doping furnace system. The parameters include doping temperature, ambient, phosphorous source, carrier gas flow rate, doping time, etc. $POCl_3$ is a well-known phosphorous source. Those process parameters will affect polysilicon resistance and uniformity. The appropriate process parameters for obtaining the recommended sheet resistance (20–50 Ω/sq) shall be found out in advance by preliminary testing.

10.1.10 Dope phosphorus into the polysilicon film on the silicon wafers. The reference wafers shall be doped together with the sample wafers to check the polysilicon film resistance.

10.1.11 Measure the sheet resistance of the reference wafers using a resistance meter to confirm the uniformity of resistance within a wafer and within a batch. The average resistance shall be 20–50 Ω/sq and the dispersion within the batch shall be less than ± 10%.

10.1.12 Make a resist mask pattern using photolithography techniques. The recommendation for the gate electrode pattern of the MOS capacitors in this test method is to form more than 100 capacitors with a gate electrode area of 10 mm^2 within a wafer.

10.1.13 Etch the polysilicon film to form MOS capacitors. At the same time, the backside polysilicon film shall be etched. If a dry etching method is used,

care must be taken to avoid plasma damage on the formed MOS capacitors.

10.1.14 Etch the backside oxide. Care must be taken to prevent damage to MOS capacitors during the etching process. For example, a coating resist on the front surface can prevent the gate oxide from sustaining damage in NH_4F etching.

10.1.15 Remove the resist on the sample silicon wafers. If a plasma ashing machine is used, attention must be paid because some kinds of ashing machines have been reported to damage MOS capacitors.

10.2 *Measurement*

10.2.1 Before the measurement, record the following information for each sample: date, time, operator, sample ID, oxide thickness, gate area, gate material, oxidation condition, conductivity type (p or n), equipment ID, and comments.

10.2.2 Decide on measurement parameters and record them. Stepwise voltage is applied in this test method. The parameters include maximum stress voltage (V_{max}), increment of step voltage (ΔV), step hold time (T_h), judgment current of breakdown (I_{bd}), measurement temperature, the number of capacitors to be measured and a map of the capacitors.

10.2.3 Set a tungsten exploring probe at the starting position.

10.2.4 Set the exploring probe on a new MOS capacitor at the next position.

10.2.5 Bias the applied voltage to zero volts (V_{app} (0) = 0). Record the oxide leakage current and the voltage.

10.2.6 Increase the applied voltage by a step increment ($V_{app}(n) = V_{app}(n-1) + \Delta V$). Measure the current I(n) and the voltage at the step after the hold time (T_h), and record them, where "n" is the step number. At the first step, $V_{app}(1) = V_{app}(0) + \Delta V$

10.2.7 If the applied voltage is equal to or greater than the maximum stress voltage ($V_{app}(n) \geq V_{max}$), record the maximum stress voltage (V_{max}) as the breakdown voltage (V_{bd}) along with the MOS address, and proceed to Section 10.2.9. If V_{app} is less than V_{max}, proceed to next step.

10.2.8 Check to see if the current I(n) has reached the judgment current of breakdown (I_{bd}). If so, record the applied voltage (V_{app}), along with each MOS address, as the breakdown voltage (V_{bd}), and proceed to Section 10.2.9. If not, repeat from Section 10.2.6.

10.2.9 Check to see if there are any more MOS capacitors to be measured. If so, repeat from Section 10.2.4 until all MOS capacitors have been tested.

10.2.10 Report the results.

10.2.11 The maximum stress electric field (E_{max}), increment of step field (ΔE) and applied field (E_{app}) can also be used as measurement parameters. They can be obtained by calculation as shown in Section 10.2.

10.2.12 Figure 2 is a flow diagram outlining the procedure for this test method.

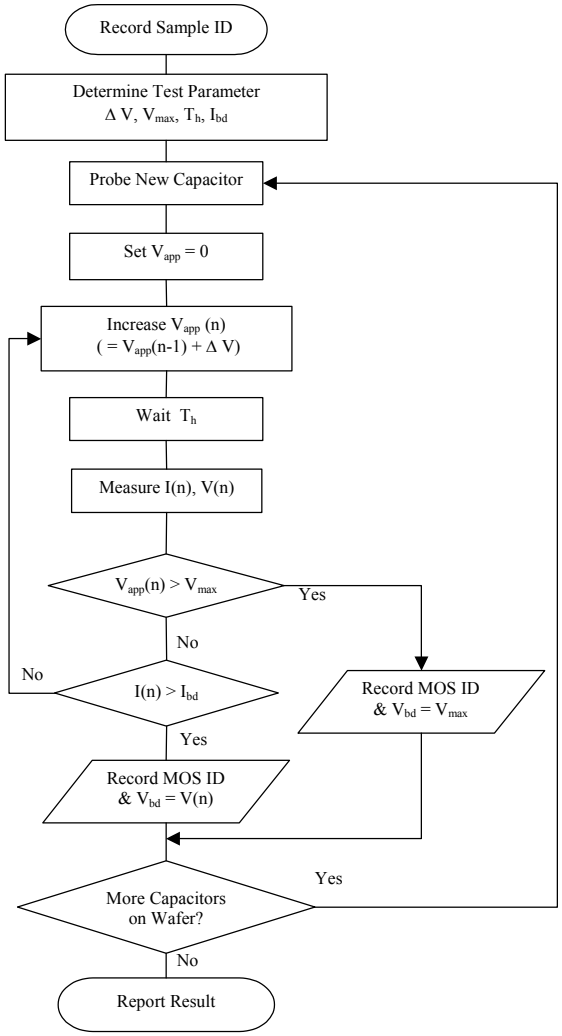


Figure 2
Flow Diagram Outline

11 Calculations

11.1 *Current and Current Density*

11.1.1 To calculate the oxide leakage current (I) from an oxide leakage current density (J), multiply the current density by the area of gate contact (S) as follows:

Symbolically:

$$I = J \times S \quad (1)$$

Example: Given a current density (J) of 1 μA/cm^2 and a gate area (S) of 10 mm^2, the current would be 100 nA.

Similarly, compute current density (J, [A/cm^2]) from measured current (I, [A]) and area (S, [cm^2]) using.

$$J = I / S \ [A/cm^2] \quad (2)$$

11.2 *Voltage and Electric Field Strength*

11.2.1 To calculate voltage (V) from an electric field (E), multiply the electric field strength by the gate oxide thickness (T_{ox}) as follows:

Symbolically:

$$V = E \times T_{ox} \quad (3)$$

where:

T_{ox} = Gate oxide thickness, cm

Example: Given an electric field (E) of 15 MV/cm and a gate oxide thickness ($T_{ox)}$ of 25 nm, the voltage would be 37.5 V.

Similarly, compute electric field (E, [MV/cm]) from measured voltage (V, [V]) and gate oxide thickness (T_{ox}, [cm]) using.

$$E = V / T_{ox} \ [MV/cm] \quad (4)$$

11.3 *Oxide Voltage*

11.3.1 Neglect the flatband voltage shift. The flatband voltage shift is due to gate-substrate work function difference [Φ_{ms}] and oxide fixed charge [Q_f]. Although it is better to consider this flatband voltage shift, its influence on the oxide film thickness in the range recommended is small.

11.4 *Calculation of Defect Density*

11.4.1 Calculate the defect density using the following equation based on the Poisson distribution assumption of the dielectric breakdown defects (see Standard EIA/JEDEC 35):

$$\rho_{ox} = -\ln(1-F)/S \quad (5)$$

where:

ρ_{ox} = Defect density (defects/cm^2)

F = Failure fraction for each oxide breakdown mode

S = Capacitor gate area (cm^2)

Example: Given a total of 100 MOS capacitors tested, with 30 B-mode-failed capacitors and a gate area of 10 mm^2, the defect density would be as follows:

$$\rho_{ox} = -\ln(1-(30/100))/0.1 = 3.6 \text{ defects/cm}^2 \quad (6)$$

11.5 *Weibull Distribution*

11.5.1 To convert cumulative percent to Weibull format (sometimes referred to as "smallest extreme value probability distribution III"), use the following equation:

$$\ln(-\ln(1-F)) \quad (7)$$

where ln is the natural log operator and F is a percent of the cumulative failures. Care shall be taken so that F is never exactly 1 since this will be in an undefined situation.

12 Report

12.1 Report the following for each wafer, as appropriate for the test conditions and as agreed upon by the parties to the test.

12.2 Test Description

12.2.1 Date

12.2.2 Time

12.2.3 Operator

12.2.4 Measurement system ID

12.2.5 Sample lot ID

12.2.6 Wafer ID

12.2.7 Average oxide thickness

12.2.8 Gate area (cm^2)

12.2.9 Gate material

12.2.10 Oxidation parameters

12.2.11 Type of wafer (Ex: n or p)

12.2.12 Applied stress parameters

12.2.13 Test temperature

12.2.14 Process comment

12.3 Report the following for each capacitor.

12.3.1 Capacitor ID such as address

12.3.2 I–V character data

12.3.3 Breakdown voltage or Breakdown electric field

12.4 Report the following for each wafer.

12.4.1 Histogram and Weibull plot of breakdown electric field

12.4.2 Average of breakdown voltage, breakdown electric field

12.4.3 Breakdown mode yield (A-mode, B-mode and C-mode)

12.4.4 Breakdown mode map or E_{bd} map

12.4.5 Result of calculated defect density

RELATED INFORMATION 1
OUTLINE OF ROUND ROBIN

NOTICE: This related information is not an official part of SEMI M51 and is not intended to modify or supersede the proposed standard. It is provided for information purposes.

R1-1 MOS Structure

R1-1.1 *Gate Oxide Thickness*

R1-1.1.1 In this round robin, we evaluated the GOI of MOS capacitors with a gate oxide film thickness of 25 nm on mirror-polished, p-type, CZ silicon wafers. In the TZDB evaluation, a negative electric field was applied step by step from 0 to 15 MV/cm, and an oxide leakage current value was measured. When the oxide leakage current first exceeded the dielectric breakdown judgment value, we judged that the gate oxide film dielectrically broke down.

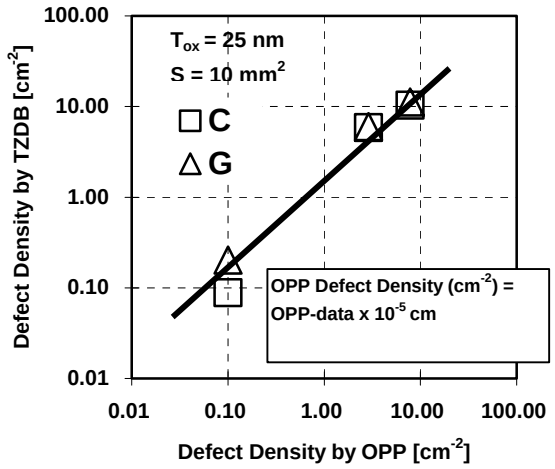


Figure R1-1
The Relationship between B-Mode Defect Density by TZDB and OPP

R1-1.1.2 The above graph shows the relationship between the B-mode defect density of 25 nm thick oxide by TZDB and the particles by optical precipitate profiler (OPP). Here, based on an assumption that the dielectric breakdown defect is in conformance with the Poisson distribution, the defect density by TZDB of 25 nm thick oxide, ρ, was calculated from the dielectric breakdown failure fraction of TZDB, F, as follows.

$$\rho_{ox} = -\ln(1 - F)/S \qquad (8)$$

Here, S is a gate electrode area of the evaluated MOS capacitors.

R1-1.1.3 The defect density was obtained by the B-mode failure percent, F, of TZDB. On the other hand, estimation of the defect density by OPP was carried out as follows. The OPP defects were measured in the wafers at the same position (ingot) of the same Si crystal as the sample wafers. The density of COPs which appeared on the silicon wafer surface was estimated from the volume defect density, n(cm^{-3}), and the COP diameter, L(cm). The area density of the defects which appear at the silicon surface can be estimated with n × L, assuming that the COP diameter, L, is almost uniform and the volume defect density, n, is uniformly distributed. Here, 0.1 μm was used as the L value[7] and the measurement results of the OPP technique as the n value. The resulting OPP defect densities, by which each of the three kinds of silicon wafers, H, M, and L, was characterized, were as follows.

$$\text{H: } n = 7.83 \times 10^5(\text{cm}^{-3}) \Rightarrow \rho_{ox} = 7.8(\text{cm}^{-2})$$

$$\text{M: } n = 2.89 \times 10^5(\text{cm}^{-3}) \Rightarrow \rho_{ox} = 2.9(\text{cm}^{-2})$$

$$\text{L: } n \leq 1 \times 10^4(\text{cm}^{-3}) \Rightarrow \rho_{ox} \leq 0.1(\text{cm}^{-2})$$

In the above graph, C and G are the measurement results for MOS capacitors made by two different wafer vendors. The defect density by TZDB and the defect density by OPP can be seen to be in a relation of almost 1:1 in this figure. These facts mean that the B mode failure of the 25 nm thick gate oxide is mainly attributable to the COPs that appear at the silicon wafer surface. Moreover, these results indicate that this standard test method can give us an evaluation of the oxide defect densities over the wide range of COP defect density with excellent reproducibility.

R1-1.2 *Total Number and Electrode Area of Measured MOS Capacitors*

R1-1.2.1 To measure the defect density with a high degree of accuracy, a large number of MOS capacitors with a large electrode area shall be measured. However, measurement of too large an area or too many MOS capacitors leads to unnecessary evaluation load. The appropriate area size and the total number of MOS capacitors needed to evaluate the defect density at the silicon wafer surface shall be selected according to the foreseen defect density and the purpose of the evaluation. For instance, if the purpose is to evaluate a conventional, mirror-polished, CZ silicon wafer with a defect density of 1–10/cm^2, about 100 MOS capacitors with an electrode area of 10–20 mm^2 must be measured.

R1-1.2.2 When the Poisson's distribution is assumed as a defect distribution, as mentioned above, the yield, Y,

of MOS capacitors with an electrode area of S and a defect density of ρ_{ox} is given by the following equation.

$$Y = 1 - F = \exp(-\rho_{ox} S)$$

R1-1.2.3 The failure fraction, F, is calculated using this expression. Here, the necessary MOS capacitor number, n, for the observation of one breakdown MOS capacitor is assumed to be 1/F. Thus, this n was calculated from the value of S and ρ_{ox} as shown in Table R1-1.

Table R1-1 Necessary number for observation of one breakdown MOS capacitor

1/F = Necessary number for observation of one breakdown MOS capacitor

S (mm^2)	*1*	*5*	*10*	*20*	*50*
$\rho_{ox} = 10\ cm^{-2}$	11	3	2	1	1
$\rho_{ox} = 1\ cm^{-2}$	101	21	11	6	3
$\rho_{ox} = 0.1\ cm^{-2}$	1001	201	101	51	21

R1-1.2.4 In the same way, the yield probability, Y, and necessary number, n, for observation of available MOS capacitors was calculated as indicated in Table R1-2.

Table R1-2 Necessary number for observation of available MOS capacitors

1/Y = Necessary number for observation of available MOS capacitors

S (mm^2)	*1*	*5*	*10*	*20*	*50*
$\rho_{ox} = 10\ cm^{-2}$	1	2	3	7	148
$\rho_{ox} = 1\ cm^{-2}$	1	1	1	1	2
$\rho_{ox} = 0.1\ cm^{-2}$	1	1	1	1	1

R1-1.2.5 The number of needed MOS capacitors is shown in Table R1-3 though both "1/F" and "1/Y" were done to one or more. To observe ten MOS capacitors or more respectively in an actual evaluation including reproducibility, the number of MOS capacitors required for the measurement will then be multiplied by ten and reaches the value shown in Table R1-3 below.

Table R1-3 Necessary number of MOS capacitors (in the case of ρ_{ox} = 1 or 10)

S (mm^2)	*1*	*5*	*10*	*20*	*50*
Confirmation of breakdown ($\rho_{ox} = 1$)	101	21	11	6	3
Confirmation of alive ($\rho_{ox} = 10$)	1	2	3	7	148
Necessary number (large one in above)	101	21	11	7	148
×10	1010	210	110	70	1480

R1-1.2.5.2 In Table R1-3, the term confirmation of breakdown ($\rho_{ox} = 1$) means the number of elements necessary to confirm at least one breakdown in the case of $\rho_{ox} = 1$, and the term of confirmation of alive ($\rho_{ox} = 10$) means the number of elements necessary to confirm at least one alive in the case of $\rho_{ox} = 10$.

R1-1.2.6 When a silicon wafer with a surface defect density of $10/cm^2$ is measured, if MOS capacitors with an electrode area of 50 mm^2 are used, it breaks down. Therefore, it is unsuitable for the comparative evaluation of the defect distribution as in this test.

R1-1.2.7 To confirm that 10 MOS capacitors are "alive" or "dead", it is necessary to measure 70 MOS capacitors with an electrode area of 20 mm^2, or 110 MOS capacitors of 10 mm^2, or 210 MOS capacitors of 5 mm^2.

R1-1.2.8 When the defect density of a sample wafer is $0.1/cm^2$, we can confirm broken 10 MOS capacitors of 50 mm^2 by measurement of only 210 MOS capacitors. For MOS capacitors of 1 mm^2, it will be necessary to measure about 10,000, and this is not realistic.

R1-1.3 *Recommended Measurement Condition*

R1-1.3.1 The electric field step, E_{step}, and hold time, T_{hold}, used in this round robin are shown in Figure R1-2.

R1-1.3.2 In TZDB measurement, the voltage is increased with each step. Then, the electric current is measured after a constant hold time. This hold time is usually initiated as a time period required for measurement stabilization. It is possible that measurement results are influenced by voltage instability when the hold time is shorter than 100 ms.

R1-1.3.3 On the other hand, because too long a hold time—that is, 800 ms or more—leads to a long total measurement time, the influence of TDDB becomes conspicuous in the high electrical field region, and it is possible that the breakdown failure fraction of the MOS capacitors increases.

R1-1.3.4 In Figure R1-2, the B-mode failure percents are shown as a function of the hold time of the applied electric field stress with a step height of 0.25 MV/cm. A hold time from 100 ms to 800 ms did not have any particular influence in the measurement results of this round robin. Thus, we have proposed 200 ms as a practicable recommended hold time.

R1-1.3.5 In this TZDB measurement, the applied electric field was increased each step directly after the current measurement. Too low a step height of the applied electric field, ΔE—that is, 0.1 MV/cm or less—leads to an unnecessarily long measurement time, and the influence of TDDB becomes conspicuous in the high electrical field region.

R1-1.3.6 On the other hand, too high a stepping-up of the applied electric field stress, for example, 1.0 MV/cm or more, leads to broadening of the dielectric breakdown electric field. That is, the reliability of the measurement result is decreased.

R1-1.3.7 In this round robin as shown in Figure R1-4, the B-mode failure percent did not depend on the step height of the applied electric field stress with a hold time of 200 ms. An electric field step height of 0.1-0.5 MV/cm did not cause any problems in the measurement results. Therefore, considering the above practical factors, a step height range of 0.1–0.5 MV/cm, and especially, 0.25 MV/cm are recommended.

TZDB(Step Voltage)

a) Group I: B, D, E b) Group II: A, F

		E_{step}(MV/cm)			
		0.1	0.25	0.5	1.0
T_{hold}(ms)	100	I	I	-	-
	200	II	I*, II	II	II
	800	-	I	I	-

(* E measured T_{hold} = 400ms)

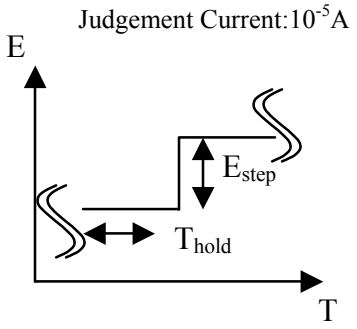


Figure R1-2
Applied Gate Electric Field Stress Condition in TZDB and Measurement Group Division

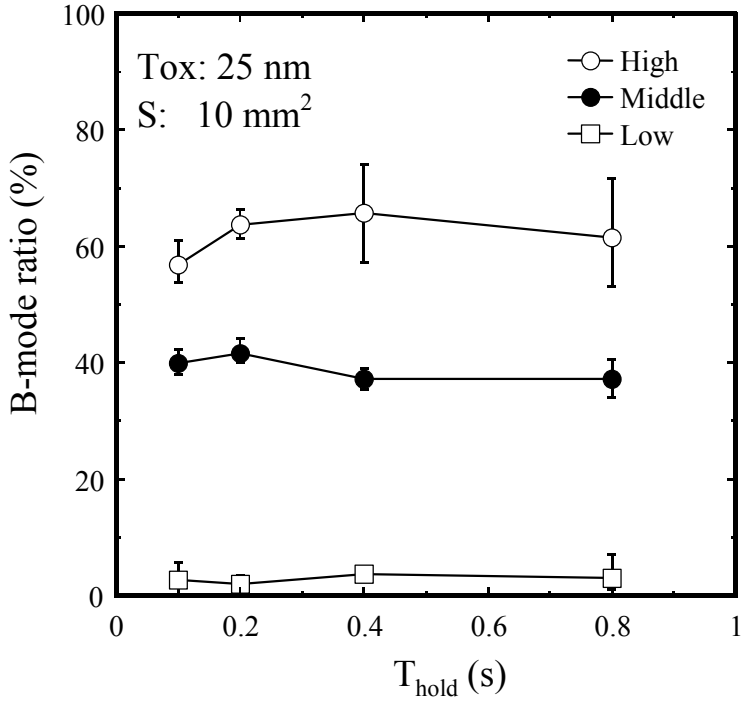


Figure R1-3
B-Mode Failure Percent vs. Hold Time of Applied Electric Field Stress with a Step Height of 0.25 MV/cm in TZDB

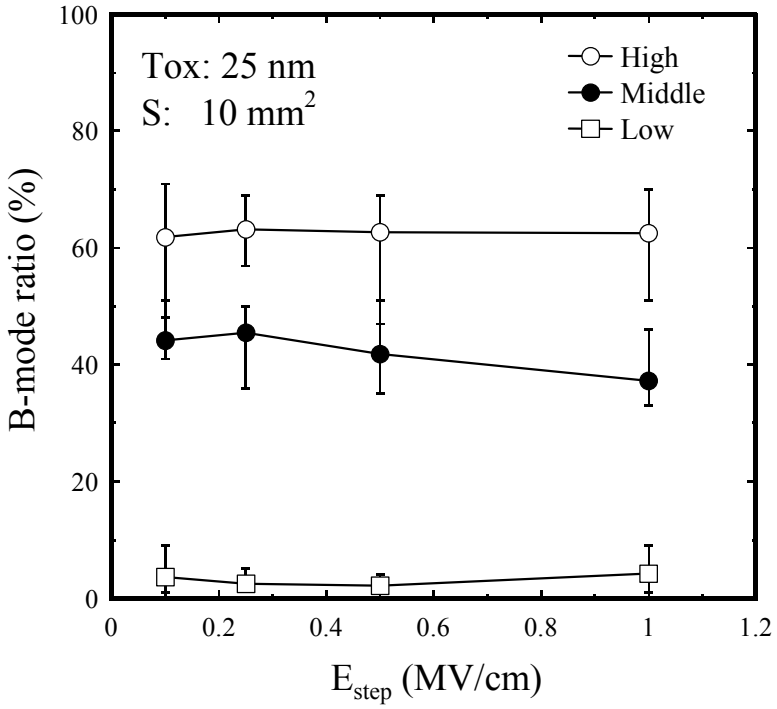


Figure R1-4
B-mode Failure Percent vs. Step Height of the Electric Field Stress with a Hold Time of 200 ms in TZDB

SEMI M52-0703
GUIDE FOR SPECIFYING SCANNING SURFACE INSPECTION SYSTEMS FOR SILICON WAFERS FOR THE 130-nm TECHNOLOGY GENERATION

This guide was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the European Silcon Wafer Committee. Current edition approved by the European Regional Standards Committee on April 3, 2003. Initially available at www.semi.org June 2003; to be published July 2003. Originally published November 2002; previously published March 2003.

1 Purpose

1.1 This guide provides recommendations for specifying Scanning Surface Inspection Systems (SSIS) for the 130-nm technology generation. The number and size of localized light scatterers (LLS) on silicon wafers are specified by customers of silicon wafer suppliers and are usually part of Certificates of Compliance. Suppliers of silicon wafers and their customers might measure these parameters using equipment provided by different manufacturers of such equipment or using different generations of equipment from one supplier. Therefore, standardization of various aspects of such measurement equipment both improves data exchange and data interpretation and aids in procurement of appropriate tools.

2 Scope

2.1 This guide outlines and recommends basic specifications for SSIS equipment used for the 130-nm technology generation as driven by the International Technology Roadmap for Semiconductors: 1999 edition (ITRS)[1,2] and in the forecasts of the major manufacturers of semiconductor devices.

NOTE 1: Future revisions of this Guide are expected to reflect changed requirements for the 130-nm node as well as requirements of other nodes.

2.2 The guide applies to measurement equipment used for verifying the quality parameter LLS counts per wafer in large scale production of bare polished or epitaxial surfaces of silicon wafers, the back surface of which may be polished or acid etched either bare or covered by an unpatterned, homogeneous layer of polysilicon or LTO (low temperature oxide). Artifacts (e.g reference materials) for calibrating measurement equipment might have different properties.

2.3 The guide also applies to measurement equipment that provides only a subset of the measurement features outlined in Table 3.

1 SEMATECH, 2706 Montopolis Drive, Austin, TX 78741-6499, USA Website : www.sematech.org

2 More recent versions of the ITRS are available from the homepage of International SEMATECH: www.sematech.org

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This guide does not apply to measurement equipment used to control intermediate process steps during silicon wafer manufacturing. However, it may be completely or partly used for measurement equipment for those applications provided corresponding constraints are appropriately identified.

3.2 This guide does not apply to measurement equipment for SOI wafers (Silicon on Insulators) or patterned wafers.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI E1.9 — Mechanical Specification for Cassettes Used to Transport and Store 300 mm Wafers

SEMI E5 — SEMI Equipment Commuications Standard 2 Message Content (SECS-II)

SEMI E10 — Specifcation for Definition and Measurement of Equipment Reliability, Availability, and Maintainability (RAM)

SEMI E19 — Standard Mechanical Interface (SMIF)

SEMI E30 — Generic Model for Communications and Control of Manufacturing Equipment (GEM)

SEMI E37 — High Speed SECS Message Services (HSMS) Generic Services

SEMI E47 — Specification for 150 mm/200 mm Pod Handles

SEMI E47.1 — Provisional Mechanical Specification for Boxes and Pods Used to Transport and Store 300 mm Wafers

SEMI E58 — Automated Reliability, Availability, and Maintainability Standard (ARAMS): Concepts, Behavior, and Services

SEMI E89 — Guide for Measurement System Capability Analysis

SEMI M1 — Specification for Polished Monocrystalline Silicon Wafers

SEMI M1.15 – Standard for 300 mm Polished Monocrystalline Silicon Wafers (Notched)

SEMI M8 — Specification for Polished Monocrystalline Silicon Test Wafers

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Integrated Circuit (IC) Applications

SEMI M12 — Specification for Serial Alphanumeric Marking of the Front Surface of Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M24 — Specification for Polished Monocrystalline Silicon Premium Wafers

SEMI M31 — Provisional Mechanical Specification for Front-Opening Shipping Box Used to Transport and Ship 300 mm Wafers

SEMI M35 — Guide for Developing Specifications for Silicon Wafer Surface Features Detected by Automated Inspection

SEMI M50 — Test Method for Determining Capture Rate and False Count Rate for Surface Scanning Inspection Systems by the Overlay Method

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI T7 — Specification for Back Surface Marking of Double-Side Polished Wafers with a Two-Dimensional Matrix Code Symbol

4.2 *ASTM Standards*[3]

ASTM F 42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

ASTM F 84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

ASTM F 154 — Practices and Nomenclature for Structures and Contaminants Seen on Specular Silicon Surfaces

ASTM F 671 — Standard Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

ASTM F 673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy Current Gage

ASTM F 928 — Standard Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

ASTM F 1152 — Standard Test Method for Dimensions of Notches on Silicon Wafers

ASTM F 1241 — Standard Terminology of Silicon Technology

ASTM F 1390 — Standard Test Method for Measuring Warp on Silicon Wafers by Automated Non-contact Scanning

ASTM F 1530 — Standard Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Non-contact Scanning

ASTM F 2074 — Standard Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

4.3 *ISO Standards*[4]

ISO 8859 — Information technology – 8-bit single-byte coded graphic character sets

ISO 8879 — Information Processing – Text and office systems – Standard Generalized Markup Language (SGML)

ISO Guide 30: 1992 — Terms and definitions used in connection with reference materials

ISO 9000 — Quality management systems – Fundamentals and vocabulary

ISO 9001 — Quality management systems – Requirements

ISO 10646-1 — Information technology – Universal multiple-octet character set (UCS) – Part 1: Architecture and basic multilingual plane

ISO 10918 — Information technology – Digital compression and coding of continuous-tone still images

3 ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

4 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch

ISO 14644-1 — Cleanroom and associated controlled environments – Part 1: Classification of air cleanliness

4.4 *DIN Standards*[5]

DIN 50431 — Measurement of the electrical resistivity of silicon or germanium single crystals by means of the four-point-probe direct current method with collinear probe array

DIN 50432 — Determination of the conductivity type of silicon or germanium by means of rectification test or hot-probe

DIN 50441-1 — Determination of the geometric dimensions of semiconductor slices; measurement of thickness

DIN 50441-2 — Determination of the geometric dimensions of semiconductor slices; testing of edge rounding

DIN 50441-4 — Determination of the geometric dimensions of semiconductor slices; diameter and flat depth of slices

DIN 50441-5 — Determination of the geometric dimensions of semiconductor wafers; terms of shape and flatness deviation

DIN 50445 — Contactless determination of the electrical resistivity of semiconductor wafers with the eddy current method

4.5 *Other Standards*

IEEE 754 — IEEE Standard for Binary Floating-Point Arithmetic[6]

IEEE 802 — IEEE Standard for Local and Metropolitan Networks: Overview and Architecture[6]

IEEE 854 — IEEE Standard Radix-Independent Floating-Point Arithmetic[6]

FED-STD 209E — Airborne Particulate Cleanliness Classes in Clean Rooms and Clean Zones[7]

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

5 Terminology

5.1 *Abbreviations and Acronyms*

5.1.1 *ARAMS* — Automated Reliability, Availability, and Maintainability Standard

5.1.2 *ASCII* — American Standard Code for Information Interchange

5.1.3 *COP* — Crystal Originated Particle/Pit

5.1.4 *CRM* — Certified Reference Material

5.1.5 *FTP* —File Transfer Protocol

5.1.6 *GEM* — Generic Model for Communications and Control of Manufacturing Equipment

5.1.7 *HSMS* — High Speed SECS Message Services

5.1.8 *IEEE* — The Institute of Electrical and Electronic Engineers

5.1.9 *JPEG* — Joint Photographics Expert Group

5.1.10 *LLS* — Localized Light Scatterer

5.1.11 *LSE* — Latex Sphere Equivalent

5.1.12 *PSL spheres* — Polystyrene Latex spheres

5.1.13 *SECS II* — SEMI Equipment Communications Standard II

5.1.14 *SSIS* — Scanning Surface Inspection System

5.1.15 *XLS* — Extended Light Scatterer

5.1.16 *XML* — Extensible Markup Language

5.2 *Terminology Regarding Defect Type*

5.2.1 *COP (Crystal Originated Particle/Pit)* — A pit of approximately 100 nm in size bounded by crystallographic planes, and formed by the intersection of the polished surface with voids in the crystal.

5.2.1.1 *Discussion* — When the surface is cleaned, etched, or oxidized the shape of the pit is modified and the light scattering characteristics change. The spatial distribution of scattered light from COPs and particles is different, and therefore these two classes of defects may be distinguished by an appropriately equipped SSIS. COPs were first detected by SSIS and believed to be small particles. It was also noticed that after repeated cleaning (etching) the number of the COPs increased as the etching process enlarged the pits and changed their scattering characteristics. Later these defects were identified as voids caused by the coalescence of vacancies during the cooling of the silicon crystal from its growth temperature. The term crystal originated particle had already become accepted, and even today many people still refer to COPs by their original, though incorrect name.

5 Available from Deutsches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany, Website: www.din.de

6 Institute of Electrical and Electronics Engineers, IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, New Jersey 08855-1331, USA. Telephone: 732.981.0060; Fax: 732.981.1721

7 General Services Administration, Federal Supply Service, FSS Acquisition Management Center, Environmental Programs and Engineering Policy Division (FCOE), Washington, D.C. 20406 [Withdrawn from use in 2001, replaced by ISO 14644-1 and associated standards.]

5.2.2 *dimple* — a shallow depression with gently sloping sides that exhibits a concave, spherical shape and is visible to the unaided eye under proper lighting conditions. [SEMI M1]

5.2.3 *haze* — non-localized light scattering resulting from surface topography (microroughness) or from dense concentrations of surface or near surface imperfections. [SEMI M1]

5.2.4 *mound (epitaxial wafer)* — regularly shaped bump on a semiconductor wafer surface, which may have one or more irregularly developed facets. [ASTM F 1241]

5.2.5 *mound (polished wafer)* — a defect characterized by small circular raised areas on the surface, typically 0.1 to 1.0 µm in height, 5 to 25 mm in diameter and located in random positions on the wafer.

5.2.6 *particle* — a small, discrete piece of foreign material or silicon not connected crystallographically to the wafer. [SEMI M1]

5.2.7 *pit* — a depression in a wafer surface that has steeply sloped sides that meet the surface in a distinguishable manner in contrast to the rounded sides of a dimple. [SEMATECH Technology Transfer 95082941A-TR]

5.2.8 *scratch* — a shallow groove or cut below the established plane of the wafer surface, with a length to width ratio greater than 5:1. [SEMATECH Technology Transfer 95082941A-TR

5.2.9 *slip* — a process of plastic deformation in which one part of a crystal undergoes a shear displacement relative to another in a fashion that preserves the crystallinity of the material. [ASTM F 1241]

5.2.10 *slurry ring* — a ring-shaped area, higher than the surrounding wafer surface caused by incomplete cleaning of slurry residue.

5.2.11 *spike* — in an epitaxial wafer, a tall thin dendrite of crystalline filament that often occurs at the center of a recess. [ASTM F 1241, see also ASTM F 154]

5.2.12 *stacking fault* — a two dimensional defect that results from a deviation from the normal stacking sequence of atoms in a crystal. [ASTM F 1241, see also ASTM F 154]

5.2.13 *stain* — area contamination that is chemical in nature and cannot be removed except through further lapping or polishing. [ASTM F 1241]

5.3 *Other Terminology*

5.3.1 *bias* — the difference between the average of measurements made on the same object and its true value. Sufficient measurements are needed to mitigate the effects of variability. [SEMI E89]

5.3.2 *calibration* — a measurement process that assigns a value to the property of an artifact or to the response of an instrument relative to reference standards or to a designated measurement process.

5.3.2.1 *Discussion* — The purpose of calibration is to eliminate or reduce bias in the user's measurement system relative to the reference base. The calibration process compares an unknown or test item or instrument with reference standards according to a specific algorithm, often in the form of a specific calibration curve. [SEMI E89]

5.3.3 *capture rate* — the probability that an SSIS detects an LLS of latex sphere equivalent (LSE) signal value at some specified SSIS operational setting.

5.3.4 *classification accuracy* — how many of a particular defect population are correctly classified.

5.3.4.1 *Discussion* — The accuracy of a classification system is expressed as an equation: Accuracy = A/H, where A is the total quantity of correctly classified defects (human and machine classification results agree) and H is the total quantity of human classified defects.

5.3.5 *classification purity* — how many of the defects classified by machine (SSIS) are properly classified.

5.3.5.1 *Discussion* — The purity of a classification system can be expressed as an equation: Purity = A/M, where A is the total quantity of correctly classified defects (human and machine classification results agree) and M is the total quantity of defects classified as a specific class by machine (SSIS).

5.3.6 *compatibility* — the capability of measurement equipment to emulate the measurement process of other tools. Downward compatibility refers to former generation(s) of the same or similar type of equipment of an equipment supplier.

5.3.7 *correlation* — the relation of measurement results obtained by repeated measurements with the same set of test specimen(s) and any two measurement tools expressed in terms of a regression curve.

5.3.8 *CRM (Certified Reference Material)* — reference material, accompanied by a certificate, one or more of whose property values are certified by a procedure which establishes its traceability to an accurate realization of the unit in which the property values are expressed, and for which each certified value is accompanied by an uncertainty at a stated level of confidence. [ISO Guide 30:1992]

5.3.9 *level 1 variability* (σ_1) — the variation of measurement results obtained by repeated measurements with the same test specimen(s) and the same measurement tool under nominally identical conditions without replacing the test specimen between subsequent measurement runs. σ_1 tests are performed with a single calibration in the shortest possible time interval.

5.3.10 *level 2 variability* (σ_2) — the variation of measurement results obtained by repeated measurements with the same test specimen(s) and the same measurement tool with replacing the test specimen between subsequent measurement runs but otherwise under nominally identical conditions. σ_2 tests are performed with a single calibration in the shortest possible time interval.

5.3.11 *level 3 variability* (σ_3) — the variation of measurement results obtained by repeated measurements with the same test specimen(s) and the same measurement tool with replacing the test specimen between subsequent measurement runs but otherwise under nominally identical conditions. σ_3 tests are performed over a time period greater than σ_2 tests without operator induced adjustment.

5.3.12 *matching tolerance* (Δ_m) — the difference in bias for any two measurement tools of the same kind. Otherwise matching tolerance tests are performed under the conditions of σ_3 tests.

5.3.13 *scanning surface inspection system (SSIS)* — An instrument for rapid examination of the entire quality area on a wafer to detect the presence of localized light scatterers or haze or both; also called *particle counter* and *laser surface scanner*.

5.3.14 *sorting* — real and virtual separation of test specimens in different categories specified by one or multiple parameters.

6 Recommended Specification for Measurement Equipment for Silicon Wafers of the 130-nm Technology Generation

6.1 The recommended specification is structured in three sections (Tables 1–3):

- Generic Equipment Characteristics (Table 1)
- Materials to be measured (Table 2)
- Metrology Specific Equipment Characteristics (Table 3)

6.1.1 Tables 1–3 contain the recommended specifications, referenced documents, test methods, and comments. Additional explanations and discussions are provided in this section.

6.2 *Generic Equipment Characteristics (Table 1)*

6.2.1 The section "Generic Equipment Characteristics" consists of five subsections:

- Wafer handling
- Reliability
- Procedural
- Documentation
- Computer/User Interface/Connectivity

6.2.2 Subsections covering "Facilities Requirements" and "Safety/Legal/Regulatory" are not included in the present guide as these issues are highly user specific and dependent on national regulations.

6.3 *Materials to be measured (Table 2)*

6.3.1 Table 2 specifies the parameters of silicon wafers that the measurement equipment must be capable to handle and to measure.

6.4 *Metrology Specific Equipment Characteristics (Table 3)*

6.4.1 This section specifies the measurement functions of the SSIS, the setup parameters of the SSIS and the performance of the SSIS. Specifications in Table 3 apply to wafer front side surface inspection only.

6.4.1.1 For back surface inspection, particles, scratches, and haze are required to be detected.

6.4.2 The surface defects to be detected by the SSIS are listed in Table 3, lines 1.1.1 to 1.1.14. They are reported as LLS or XLS. The measurement performance of the equipment is verified with PSL sphere depositions on wafers that meet the COP and haze requirements of the 130-nm technology generation.

6.4.3 All size units of LLS are given in [length unit] LSE, e.g., nm LSE, and refer to a nominal diameter.

6.4.4 The geometrical size of a defect (LLS) may differ considerably from its size as reported in LSE units, as the cross section for light scattering of a defect depends sensitively on the properties of the LLS.

6.4.5 PSL depositions used as reference materials are required to be CRMs, traceable to a National Standards Laboratory.

6.4.6 For COPs and particles, classification accuracy and purity are specified.

6.4.7 In this guide, a hierarchy of variability levels is used to describe the performance of measurement equipment that is calibrated and adjusted/aligned according to the supplier's procedures. The various terms are defined in Section 5. These variability levels are consistent with terms defined in SEMI E89 but not fully interchangeable. Their relation is indicated in parentheses.

6.4.7.1 Level 1 variability: standard deviation σ_1 (SEMI E89 static repeatability)

6.4.7.2 Level 2 variability: standard deviation σ_2 (SEMI E89 dynamic repeatability)

6.4.7.3 Level 3 variability: standard deviation σ_3 (SEMI E89 reproducibility)

6.4.7.4 In addition two levels of systematic off-set between different tools are defined:

6.4.7.5 Matching tolerance (difference of means Δ_m)

6.4.7.6 Correlation (regression curve)

6.4.8 Explicitly specified in the present guide is mainly level 3 variability and matching tolerance.

6.4.9 For SSIS, downward compatibility is subject to limitations imposed by changes in geometry and number of detectors.

6.4.10 For sizing calibration, deposition CRMs are available from a variety of sources. On the other hand, a reference standard for the defect coordinate performance is not available.

7 Related Documents

7.1 *Glossary of Terms Related to Particle Counting and Surface Microroughness of Silicon Wafers,* SEMATECH Technology Transfer 95082941A-TR[8]

7.2 *International Technology Roadmap for Semiconductors*: 1999 edition[1]

Table 1 Generic Equipment Characteristics

Item	*Recommended Specification*	*Comment*	*References*
1 WAFER HANDLING			
1.1 Robot End-Effector	optional wafer edge or backside contact	edge as defined by SEMI M1	
1.2 Scan Stage	optional wafer edge or backside contact	edge as defined by SEMI M1	
1.3 Wafer Contact Materials	contact materials to leave metals and organics on wafers less than as defined in ITRS 99.		
1.4 Wafer Detection	protection of accidental contact due to e.g. cross-slotting double slotting, etc.		
1.5 Wafer Rotational Alignment	random in, aligned out		
1.6 Number of Cassette Stations	2-4, arbitrary sender/receiver assignment		
1.7 Type of Cassettes	open, FOUP/SMIF, FOSB	to be specified alternatively	SEMI E1.9, SEMI E19, SEMI E47, SEMI E47.1, SEMI M31
1.8 Cassette Loading	manual/guided vehicle, conveyor belt		
1.9 Automatic Cassette ID	user specific		
1.10 Wafer Seating	vertical or off-horizontal	during setting cassette on station by operator	

8 International SEMATECH, 2706 Montopolis Drive, Austin, TX 78741-6499, USA Website: www.sematech.org

Item	*Recommended Specification*	*Comment*	*References*
1.11 Cassette Filling Modes	random access and loading, programmable empty slot filling		
1.12 Automatic Wafer ID reading	user specific		
1.13 Particulate Contamination	front surface: <0.001 PWP per cm^2, >90 nm LSE back surface: <0.001 PWP per cm^2 >120 nm LSE, 0 PWP >250 nm LSE, 0 scratches >120 nm LSE	verify with mirror polished wafer surfaces for front and backside excluding contamination from cassette	
2 RELIABILITY			
2.1 E-$MTBF_p$	>2000 h		SEMI E10
2.2 E-MTTR	according to service contract		SEMI E10
2.3 Equipment Dependent Uptime	>95 %	per year	SEMI E10
2.4 Response Time	<1 day		
2.5 Statistical Process Control (SPC) performance	automated		
2.6 Statistical Process Control (SPC) machine parameters	automated		
3 PROCEDURAL			
3.1 Acceptance Testing	user specific		
3.2 Transport and Assembly	user specific		
3.3 Quality Assurance	supplier conforming with ISO 9000/9001		ISO9000/9001
3.4 Warranty	>1 year		
3.5 Test certificates	user specific		
3.6 Spares Availability	>5 years	after notification from supplier	
3.7 Change Control	supplier conforming with ISO 9000/9001		ISO9000/9001
4 DOCUMENTATION			
4.1 Installation	required		
4.2 Operation	required		
4.3 Service	required		
5 COMPUTER, USER INTERFACE, CONNECTIVITY			
5.1 Computer Operating System	- Microsoft Windows NT 4.0 or higher, or Unix		

Item	*Recommended Specification*	*Comment*	*References*
5.2 Display	cleanroom compatible, class 10 (Federal Standard) or class 4 (ISO)		FED-STD 209E ISO 14644-1
5.3 Keyboard	cleanroom compatible, class 10 (Federal Standard) or class 4 (ISO)		FED-STD 209E ISO 14644-1
5.4 Pointing Device	cleanroom compatible, class 10 (Federal Standard) or class 4 (ISO)		FED-STD 209E ISO 14644-1
5.5 Printer	cleanroom compatible, class 10 (Federal Standard) or class 4 (ISO)		FED-STD 209E ISO 14644-1
5.6 Data Processing	- reprocessing of data - parallel processing in different modes during measurement including sorting - multiprocessing: e.g. recipe editing, up/downloading during measurements	different modes refer to data evaluation	
5.7 Data Access	- access to basic measurement results: - data available at SECS/GEM/HSMS interface in real time	refers to all functions as defined in Table 3	SEMI E5 SEMI E30 SEMI E37
5.8 Data Analysis (Online/Offline)	on-line/off-line		
5.9 Recipe Control	- complete recipe generation off-line without machine specific data (calibration curves) - off-line recipe editing - remote recipe control by host computer - recipes are compatible between different software versions		
5.10 Operating Sequence	complete remote control: recipe download, start, stop, define data evaluation via SECS/GEM		SEMI E5 SEMI E30
5.11 Data Interfaces	- SECS/ - GEM - optional additionally a mass data standard transfer protocol (e.g. FTP)		SEMI E5 SEMI E30 www.w3.org/Protocols/rfc959
5.12 Material Tracking System Support	required, details user specific		
5.13 Output File Format	standardized formats: - ASCII or XML for measurement results and optional for raw data - IEEE for raw data (floating point) - JPEG (or equivalent) for raw data (image data)		ISO/IEC 8859, ISO 8879 ISO/IEC 10646-1 www.w3.org IEEE 754, IEEE 854 ISO/IEC 10918
5.14 Network Communications Standards Support	Ethernet, Fast Ethernet		IEEE 802 and subsequent standards
5.15 SECS/GEM (SEMI Equipment Communication Standard II/Generic Model for Communications and Control of Manufacturing Equipment)	required		SEMI E5 SEMI E30

Item	Recommended Specification	Comment	References
5.16 ARAMS (Automated Reliability, Availability, and Maintainability Standard)	required		SEMI E58

Table 2 Materials to be measured

Item	Recommended Specification	Comments	References
1. WAFERS			
1.1 Kind of Wafers	monocrystalline, unpatterned silicon wafers with layers as specified in Table 2, 1.3.4		SEMI M1 (SEMI M8) (SEMI M11) (SEMI M24)
1.2 Wafer Characteristics - dimensional			
1.2.1 Wafer Diameter	200 or 300 or 200 and 300 mm nominal		SEMI M1 ASTM F 2074 DIN 50441-4
1.2.2 Wafer Thickness	700–850 µm	For reclaim wafers, performance as outlined in Table 3 might be reduced. 200 mm: 600–850 µm 300 mm: 650–850 µm	ASTM F 1530 DIN 50441-1
1.2.3 Edge Shape	rounded		SEMI M1 DIN 50441-2 ASTM F 928
1.2.4 Wafer Shape Range	200 mm wfrs: warp ≤100 µm, 300 mm wfrs: warp ≤200 µm		SEMI M1 ASTM F 1390 DIN 50441-5
1.2.5 Fiducial	flat or notch		SEMI M1 ASTM F 671 ASTM F 1152 (DIN 50441-4)
1.2.6 ID Mark(s)	200 mm wfrs: user specific 300 mm wfrs: according to SEMI standards	content, type location of ID mark to be specified	SEMI M12 SEMI M13 SEMI M1.15 SEMI T7
1.3 Wafer Characteristics - electrical, optical			
1.3.1 Electrical resistivity of wafers, conductivity type	0.5 mΩ·cm – intrinsic, p-, n-type		Res: ASTM F 673 DIN 50445 ASTM F 84 DIN 50431 Type: ASTM F 42 or DIN50432
1.3.2 Thermal donors	annealed and not annealed		
1.3.3 Wafer charge	no effect with respect to measurement		

Item	*Recommended Specification*	*Comments*	*References*
1.3.4 Layers (LTO, poly-Si), Epi	LTO: thickness: 150–900 nm uniformity: ≤10% Poly-si: thickness: ≤2 μm, uniformity: <20 % Epitaxial layer: customer specific		
1.3.5 Wafer surface conditions	front side: polished, annealed, epitaxial layer backside: polished, acid and/or caustic etched, layers according to 1.3.4	Annealing may affect the surface roughness of a Si wafer. Evaluation of capture rate with such a wafer may not achieve the specifications as defined in Section 2.2 and Table 3, 1.2.1.	

Table 3 Metrology Specific Equipment Characteristics

Item	*Recommended Specification*	*Comments*	*References*
1. MEASUREMENT FUNCTIONS			
1.1 Defect type			
1.1.1 PSL sphere	required	For reference	SEMI M35
1.1.2 Particle	required		SEMI M1 SEMI M35
1.1.3 COP	required		SEMATECH TT 95082941A-TR
1.1.4 Mound (epi)	required		ASTM F 1241
1.1.5 Mound (pw)	required		
1.1.6 Pit	required		SEMI M35 SEMATECH TT 95082941A-TR
1.1.7 Spike (epi)	required		ASTM F 154
1.1.8 Stacking Fault (epi)	required		ASTM F 154
1.1.9 Scratch	required		SEMI M35 SEMATECH TT 95082941A TR
1.1.10 Slip	required		ASTM F 1241
1.1.11 Dimple	required		SEMI M1
1.1.12 Haze	required		SEMI M1, M35
1.1.13 Slurry Ring	required		
1.1.14 Stain	required		ASTM F 1241

Item	*Recommended Specification*	*Comments*	*References*
1.1.15 Other defects	not required	Protrusion, Flake, Chuck Mark, Misfit, Twin, Tweezer, Edge Chip, Edge Chip(peripheral), Edge Crack, Edge Crown, Nodule, Dopant striation, Gloss(specular), Growth Ring, Microroughness, Orange Peel, Polishing line, Saw Mark	
1.2 System Performance for PSL Spheres			
1.2.1 Capture Rate	≥95%, 65 nm LSE and higher	Wafer surface quality must meet ITRS requirements for 130 nm node.	SEMI M50
1.2.2 Sizing Dimension	65–2000 nm	Dynamic Range	
1.2.3 Count Level 3 Variability σ_3	<2.3%, 1 σ	>50, <150 LLS count/wafer required	
1.2.4 Count Matching Tolerance Δ_m	<2.6%	>50, <150 LLS count/wafer required	
1.2.5 Sizing error from interpolation	≤2% of mean diameter	65–200 nm LSE see NOTE 1	
1.2.6 Sizing Level 3 Variability σ_3	<2.3%, 1σ	65–200 nm LSE	
1.2.7 Sizing Matching Tolerance	<2.3%	65–200 nm LSE	
1.3 Threshold values for various defects			
1.3.1 COP/Particle Classification			
1.3.1.1 Classification Accuracy	≥90%	For ≥80 nm LSE	
1.3.1.2 Classification purity	≥95%	For ≥80 nm LSE	
1.4 Haze			SEMI M1
1.4.1 Level 3 Variability σ_3	<2%, 1σ	For polished and epi wafers, average haze	
1.4.2 Matching Tolerance Δ_m	<2.6%	For polished and epi wafers, average haze	
1.5 Defect Coordinate, Inscribed Reference			
1.5.1 Bias	±20 µm	At minimum pitch	
1.5.2 Level 3 Variability σ_3	10 µm, 1σ	At minimum pitch	
1.5.3 Matching Tolerance Δ_m	13 µm	At minimum pitch	
1.6 Inspection Surface			
1.6.1 Front side	User specific/selectable		
1.6.2 Backside	User specific/selectable		

Item	*Recommended Specification*	*Comments*	*References*
1.6.3 Wafer edge/ Bevel	User specific/selectable		
2. SETUP PARAMETERS			
2.1 FQA/edge exclusion	EE ≥1 mm, 200 and 300 mm wafers FQA 200 mm wfrs: ≤198 mm FQA 300 mm wfrs: ≤298 mm	performance parameters to be verified with EE ≥2 mm	
2.2 Number of classification bins		arbitrary, definable, cumulative, differential	
2.2.1 LLS	10/channel		
2.2.2 Bright Field Defects	10/channel		
2.2.3 Haze	10/channel		
2.2.4 Scratches	4/channel		
2.2.5 Area Defects	4/channel		
2.3 Sorting criteria	all parameters, all bins, separately and combined		
2.4 Exclusion windows	a) >5, curved/linear boundaries, arbitrary position on entire wafer surface b)perimeter exclusion windows: N zones with total area covered ≤0.001 of total wafer area in the radial range R-2 mm to R, total perimeter excluded at R-1 mm ≤4% of total wafer circumference, no single zone longer than 5 mm.	a) e.g. laser mark exclusion b) e.g. edge gripping exclusion	
3. PERFORMANCE			
3.1 Throughput		CoO issue	
3.1.1 200 mm wafers	>140 wph	for LLS ≥65 nm LSE and ≥95% capture rate	
3.1.2 300 mm wafers	>100 wph	for LLS ≥65 nm LSE and ≥95% capture rate	
3.2 Downward compatibility	one generation	Subject to limitations imposed by changes in geometry and number of detectors.	

Item	*Recommended Specification*	*Comments*	*References*
3.3 Calibration	automated,	In order to reduce PSL sphere sizing uncertainty in the 65 nm to 200 nm range, the diameter distribution should have a full width at half maximum (FWHM) ≤5%. In addition, it is desirable that the peak PSL diameter as deposited on the wafer have a relative expanded uncertainty at about 95% confidence level as small as possible but not greater than 3%. See NOTE 2.	SEMI M53

NOTE 1: At the calibration points, if it is assumed that the SSIS sizing of PSL spheres is exactly correct, then the sizing error is caused by differences between the response predicted by the calibration curve and the exact response of the SSIS away from calibration points. Details for calculating this error are being developed for another standard.

NOTE 2: This specification limits the width of the diameter distribution of PSL spheres as they appear on the wafer in the calibration deposition. The deposition system transfer function (often nominally triangular in shape) times the actual PSL diameter distribution shape presented to the system defines the deposition width. Thus the width of the deposition on the wafer is no larger than the width of the transfer function. A narrow width decreases calibration uncertainty in three ways. First, in the presence of background noise, it makes the distribution peak signal easier to locate. Second, a narrow transfer function makes the deposition distribution peak easier to determine. Third, a narrow transfer function reduces the deposition distribution asymmetry if the input PSL distribution is not symmetrical about the peak value.

SEMI M53-1103
PRACTICE FOR CALIBRATING SCANNING SURFACE INSPECTION SYSTEMS USING DEPOSITIONS OF MONODISPERSE POLYSTYRENE LATEX SPHERE ON UNPATTERNED SEMICONDUCTOR WAFER SURFACES

This practice was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on July 25, 2003. Initially available at www.semi.org October 2003; to be published November 2003. Originally published March 2003.

1 Purpose

1.1 Calibration of a scanning surface inspection system (SSIS) using a deposition of polystyrene latex (PSL) spheres as a known source of scatter signal is a necessary step in matching the responses of SSISs. However, the measured amplitude of the light scatter signal depends on both the characteristics of the SSIS and the characteristics of the scatter source. The use of a deposition of polystyrene latex (PSL) spheres (see Section 5.3.4) as a known source of scatter signal allows meaningful comparisons to be made between scatter signals from PSL spheres as measured by dark field detection systems of different designs. On the other hand, calibration with PSL spheres alone does not guarantee meaningful performance comparisons to be made between dark field detection SSISs of the same or different designs when detecting either real particles of materials different from PSL spheres or other surface defects.

1.2 This practice describes calibration of SSIS dark field channels so that the SSIS accurately sizes PSL spheres deposited on unpatterned polished, epitaxial, or filmed semiconductor wafer surfaces (see Related Information 1).

1.3 This practice defines the use of latex sphere equivalent (LSE) signals as a means of reporting real surface defects whose identity and true size are unknown.

1.4 This practice provides a basis for quantifying SSIS performance as used in related standards concerned with parameters such as sensitivity, repeatability and capture rate.

2 Scope

2.1 This practice covers

- Requirements for the surface and other characteristics of the semiconductor substrates on which the PSL spheres are deposited to form reference wafers (see Section 8.1),
- Selection of appropriate certified depositions of PSL spheres for SSIS calibration (see Section 8.2),
- Size distribution requirements to be met by the PSL sphere depositions (but not the deposition method), and
- Multipoint calibration procedures for dark field channels.

2.2 Appendix 1 covers a single-point calibration procedure that may be used in limited production applications.

2.3 PSL spheres from 10 μm to the smallest size that can be detected by the SSIS being calibrated can be used in this practice.

NOTE 1: At the time of development of this edition of the practice, the smallest practical deposited PSL spheres have diameters approaching 30 nm, but as IC technology evolves to smaller and smaller critical dimensions it is expected that depositions of smaller diameter PSL spheres will become available.

2.4 Background information to enable an understanding of the need for the various requirements imposed on the PSL sphere depositions is provided in Related Information 1.

2.5 Both the deposition process and calibration procedures must be carried out in a Class 4 or better environment as defined in ISO 14644-1.

NOTE 2: ISO class 4 is approximately the same as Class M2.5 (Class 10) as defined in Federal Standard 209E.

2.6 Although it was developed primarily for use in evaluation of SSISs to be used for detection of localized light scatterers (LLSs) on polished silicon wafers with geometrical characteristics as specified in SEMI M1, this practice can be applied to SSISs to be used for detection of LLSs on other unpatterned semiconductor surfaces provided that suitable reference wafers are employed.

2.7 This practice does not in any way attempt to define the manner in which LSE values are used to define the