ITEM			SPECIFICATION	MEASUREMENT METHOD
	5-4.1.8	Zinc	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
	5-4.2	Other Surface Metals (List Separately)		
	5-4.2.1	Calcium	[ ]Not greater than [× 10]atoms/cm^2	[ ]ICP/MS; [ ]AAS; [ ]SEMI MF1617 (SIMS); [ ]SEMI M33 (TXRF); [ ]ISO 14706 (TXRF); [ ]Other: (specify)_____
5-5. POST-ANNEAL FRONT SURFACE INSPECTION CHARACTERISTICS				
	5-5.1	Slip	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF1809; [ ]JIS H 0609; [ ]DIN 50434; [ ]DIN 50443/1; [ ]Other: (specify)_____
	5-5.2	Oxidation Induced Stacking Faults (OSF)	[ ]None; [ ]Not greater than [ ] per cm^2	Test Cycle: [ ]SEMI MF1727; [ ]JIS H 0609; [ ]Other: (specify)____ Observation Method: [ ]SEMI MF1726; [ ]JIS H 0609; [ ]DIN 50443/1; [ ]Other: (specify)_____
	5-5.3	Scratches – Macro	[ ]None; Total Length = [ ]mm	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#3] [ ]Other: (specify)_____
	5-5.4	Scratches – Micro	[ ]None; [ ]Total Length = [ ]mm	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#3] [ ]Other: (specify)_____
	5-5.5	Haze	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#3] [ ]Other: (specify)_____
	5-5.6	Localized Light Scatterers (Total LLS)	Size: ≥[ ] μm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2 Size: ≥[ ] μm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#3] [ ]Other: (specify)_____
	5-5.7	Localized Light Scatterers (COP only)	Size: ≥[ ] μm (LSE) Count: ≤[ ] [ ] per wafer; [ ] per cm^2	[ ]SEMI MF523; [ ]JIS H 0614; [ ]SSIS;[#3] [ ]Other: (specify)_____
	5-5.8	Other Front Surface Defects	Terracing, Surface microroughness, Nanotopography, and other attributes as discussed between supplier and customer	As discussed between supplier and customer.
5-6. POST- ANNEAL BACK SURFACE INSPECTION CHARACTERISTICS				
	5-6.1	Contamination/Area	[ ]None; [ ]Other: (specify)_____	[ ]SEMI MF 523; [ ]JIS H 0614; [ ]Other: (specify)_____
	5-6.2	Other Back Surface Defects	Support-related back surface defects as discussed between supplier and customer	As discussed between supplier and customer.
5-7. OTHER POST-ANNEAL CHARACTERISTICS				
	5-7.1	Bulk Iron (Fe)	[ ]Not greater than [ ] × 10$^{[\ ]}$ atoms/cm^3	[ ]SEMI MF391; [ ]SEMI MF1535; [ ]Other: (specify)_____
	5-7.2	Depth of BMD Denuded Zone	[ ]more than [ ] μm	As agreed between supplier and customer

ITEM			SPECIFICATION	MEASUREMENT METHOD
	5-7.3	BMD Density	Range [ ] × $10^{[\ ]}$ to [ ] × $10^{[\ ]}$ Unit Unit: [ ]cm^{-2}; [ ]cm^{-3}	Test Cycle: SEMI MF1239 [ ]A, [ ]B; Other: (specify)_____
	5-7.4	Other Post-Anneal Characteristics	Surface boron depletion, dissolved hydrogen in the case of hydrogen annealed wafer, post-annealed oxygen, and silicon nitride precipitates and defects in the case of nitrogen-doped silicon may be discussed between supplier and customer.	As discussed between supplier and customer.

[#1] If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

[#2] Flatness Acronyms are defined in the Flatness Decision Tree in Appendix 1 of SEMI M1.

[#3] In today's technology, it may be possible to inspect for some of these items using automated surface scanning inspection systems (SSIS). Such systems should be calibrated according to SEMI M53 using polystyrene latex spheres deposited in accordance with SEMI M58. Some indication of the defects separable by such instruments is provided in SEMI M35; however, a standard test procedure has yet to be developed. Application of automated inspection with the use of an SSIS must be agreed upon between supplier and customer.

5.2 Purchase orders furnished to this guide shall also include the items shown in Table 1 for the finished annealed wafers, and other items as agreed between supplier and customer.

5.3 In addition, the purchase order must indicate the test method to be used in evaluating each of those items for which alternate test procedures exist.

5.4 The following items must also be included in the purchase order:

5.4.1 Lot acceptance procedures.

5.4.2 Certification (if required).

5.4.3 Packing and shipping container labeling requirements.

6 Requirements Specifying Silicon Annealed Wafers

6.1 Table 2 provides a guide for specifying polished silicon annealed wafers for the 180 nm, 130 nm, and 90 nm technology generations. A parameter not listed in this table need not be specified.

6.2 It is also essential to specify appropriate test methods in each case. Defaults for test method selection are given in §8.

6.2.1 The line items with numbers beginning with "2-" are listed in Part 2 of the Silicon Wafer Specification Format for Order Entry, SEMI M1, Table 1. The line items with numbers beginning with "5-" are listed in Part 5 of this format, included herein as Table 1.

Table 2 Guide for Specifying Polished Silicon Annealed Wafers for the 180 nm, 130 nm and 90 nm Technology Generations

Item		*180 nm Technology Generation*	*130 nm Technology Generation*	*90 nm Technology Generation*
PRE-ANNEAL STATE (POLISHED WAFER)				
2-1 GENERAL CHARACTERISTICS				
2-1.1	Growth Method	Cz or MCz	Cz or MCz	Cz or MCz
2-1.3	Crystal Orientation	(100)	(100)	(100)
2-1.4	Conductivity Type	*p*-type	*p*-type	*p*-type
2-1.5	Dopant	Boron	Boron	Boron
2-1.6	Nominal Edge Exclusion	3 mm	3 mm	2 mm
2-1.7	Co-dopant in Crystal	None, Nitrogen and/or Carbon (as agreed between supplier & customer).	None, Nitrogen and/or Carbon (as agreed between supplier & customer).	None, Nitrogen and/or Carbon (as agreed between supplier & customer).
2-1.8	Wafer Surface Orientation	On-orientation: 0.00° ± 1.00°	On-orientation: 0.00° ± 1.00°	On-orientation: 0.00° ± 1.00°
2-2 ELECTRICAL CHARACTERISTICS				
2-2.1	Resistivity (Center point)	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
2-2.2	Radial Resistivity Variation[#1]	≤20%	≤20%	≤20%
2-3 CHEMICAL CHARACTERISTICS				
2-3.1	Oxygen Concentration/ Calibration Factor	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
2-3.2	Radial Oxygen Variation[#2]	±10%, 10 mm from the edge	±10%, 10 mm from the edge	±10%, 10 mm from the edge

Item		180 nm Technology Generation	130 nm Technology Generation	90 nm Technology Generation
2-3.3	Carbon Concentration (Background[#3])	≤0.5 ppma	≤0.5 ppma	≤0.5 ppma
2-4 STRUCTURAL CHARACTERISTICS				
2-4.3	Lineage	None	None	None
2-4.4	Twin Boundary	None	None	None
2-4.5	Swirl	None	None	None
2-5 WAFER PREPARATION CHARACTERISTICS				
2-5.1	Wafer ID Marking	As agreed between supplier and customer.	SEMI T7 plus optional alphanumeric mark.	SEMI T7 plus optional alphanumeric mark.
2-5.2	Front Surface Thin Films	None	None	None
2-5.4	Extrinsic Gettering	None	None	None
2-5.5	Backseal	None	None	None
2-6 DIMENSIONAL CHARACTERISTICS				
2-6.1	Diameter	200.00 mm ± 0.20 mm	300.00 mm ± 0.20 mm[#4]	300.00 mm ± 0.20 mm[#4]
2-6.6	Edge Profile	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
2-6.7	Thickness	725 µm ± 20 µm (Notched type wafers) or 675 µm ± 15 µm (Flatted type wafers)	775 µm ± 20 µm	775 µm ± 20 µm
2-6.8	Total Thickness Variation (TTV)	10 µm, max	10 µm, max	10 µm, max
2-9 BACK SURFACE INSPECTION CHARACTERISTICS				
2-9.1	Edge Chips	None	None	None
2-9.8	Brightness (Gloss)	Not specified	0.80[#5]	0.80[#5]
2-9.9	Scratches (macro) — cumulative length	0.25 × diameter	0.25 × diameter	0.25 × diameter
5-1 ANNEALING CONDITIONS				
5-1.1	Annealing Atmosphere	Hydrogen, Argon, or Other (as agreed between supplier & customer).	Hydrogen, Argon, or Other (as agreed between supplier & customer).	Hydrogen, Argon, or Other (as agreed between supplier & customer).
POST-ANNEAL STATE				
5-2 POST-ANNEAL WAFER PREPARATION CHARACTERISTIC				
5-2.1	Edge Surface Condition	Acid Etched or Polished[#6] (as agreed between supplier & customer).	Acid Etched or Polished[#6] (as agreed between supplier & customer).	Acid Etched or Polished[#6] (as agreed between supplier & customer).
5-3 POST ANNEAL DIMENSIONAL-CHARACTERISTICS				
5-3.1	Warp	75 µm	100 µm[#7]	100 µm[#7]
5-3.2	Site Flatness[#8]	SFQR ≤ 180 nm	SFQR ≤ 130 nm	SFQR ≤ 90 nm

Item		*180 nm Technology Generation*	*130 nm Technology Generation*	*90 nm Technology Generation*
5-4 POST-ANNEAL FRONT SURFACE CHEMISTRY[#9] (Surface Metal Concentration)				
5-4.1.1	Sodium	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-4.1.2	Aluminum	$\leq 1 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-4.1.3	Potassium	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-4.1.4	Chromium	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-4.1.5	Iron	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-4.1.6	Nickel	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-4.1.7	Copper	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-4.1.8	Zinc	$\leq 1 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{11}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-4.2.1	Calcium	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1.3 \times 10^{10}$ cm^{-2}	$\leq 1 \times 10^{10}$ cm^{-2}
5-5 POST-ANNEAL FRONT SURFACE-INSPECTION CHARACTERISTICS				
5-5.1	Slip	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5-5.2	Oxidation-Induced Stacking Faults	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5-5.3	Scratches (macro)	None	None	None
5-5.4	Scratches (micro) – total length	0.25 × diameter	0.25 × diameter	0.25 × diameter
5-5.5	Haze	None by Bright Light Inspection.	None by Bright Light Inspection.	None by Bright Light Inspection.
5-5.6	Total Localized Light Scatterers, cm^{-2}	≤0.382 @ ≥120 nm LSE	≤0.270 @ ≥90 nm LSE	≤0.270 @ ≥90 nm LSE
5.5.7	Localized Light Scatterers (COP only), cm^{-2}	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5.5.8	Other Front Surface Defects[#10]	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5-6 POST-ANNEAL BACK SURFACE-INSPECTION CHARACTERISTICS				
5-6.1	Contamination/Area	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5-6.2	Other Back Surface Defects[#11]	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5-7 POST-ANNEAL OTHER CHARACTERISTICS				
5-7.1	Bulk[#12]	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5-7.2	Depth of BMD Denuded Zone	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5-7.3	BMD Density	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.
5-7.4	Other Characteristics[#13]	As agreed between supplier & customer.	As agreed between supplier & customer.	As agreed between supplier & customer.

[#1] Test in accordance with SEMI MF81, Plan B.

[#2] Test in accordance with SEMI MF951, Plan A1, A2, or A3, as agreed between supplier and customer.

[#3] The value of background carbon concentration is valid only if the crystal is not intentionally co-doped with carbon (see Item 2-1.7).

[#4] 200 mm diameter wafers may be used, as agreed between supplier & customer.

[#5] Gloss as measured in accordance with ASTM Test Method D 523 or JIS Z 8741 with visible illumination at a 60° angle of incidence referenced to a mirror polished silicon wafer front surface. This metric may not describe the back surface finish adequately to establish detectability of small localized light scatterers (LLSs). If it is necessary to detect LLSs smaller than 0.25 µm LSE, another quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures shall be agreed upon between supplier and customer.

[#6] If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and purchaser.

[#7] Warp corrected for gravitational effects. However, warp is not an adequate wafer shape specification for all applications.

[#8] Determine in accordance with SEMI MF1530 with the following set up parameters: Site size, 26 mm × 8 mm; x-offset = 0 mm; and either % usable area = 100% with full sites only or % usable area ≥95% with partial sites included, as per agreement between supplier and customer. SFQR with a site size of 26 mm × 8 mm is approximately equal to SFSR with a site size of 26 mm × 32 mm. The smaller site allows more coverage of the FQA than the larger site. The value of site flatness is taken from the ITRS Starting Materials Table.

[#9] Surface metal measurement variation can be significant. Measurement results are frequently larger than the actual value. Processes are normally controlled with median values to reduce the impact of the measurement variation.

[#10] Haze, Terracing, Surface micro-roughness, Nanotopography, shallow pits, and other attributes.

[#11] Back surface defects that relate to the support (such as, chuck etc.) provided to the back surface of the wafer.

[#12] Bulk iron (Fe) may be characterized by SPV technique. For details, refer to SEMI MF391.

[#13] Surface boron depletion, dissolved hydrogen in the case of hydrogen annealed wafer, post-annealed oxygen, silicon nitride precipitates and defects in the case of nitrogen-doped silicon.

7 Sampling

7.1 Unless otherwise specified, ASTM Practice E 122 shall be used to define the sampling plan. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

8 Test Methods

8.1 Measurements shall be made or certifiable to one of the SEMI, ASTM, JEITA, JIS, or DIN standard test methods for the item as selected from the Silicon Wafer Specification Format for Order Entry, Parts 2 and 5, located in Table 1 of SEMI M1 and Table 1 herein, respectively, and specified in the purchase order.

8.2 If several different standard test methods for an item are commonly used within a region, it is particularly important that the applicable method of test be identified in the purchase order.

8.3 If no method of test is specified in the purchase order and if standard test methods from different geographic regions are available, the default method shall be a method in common usage for the region of the purchaser of the wafer.

8.4 If no standard test method for an item is available, the test procedure to be used must be agreed upon between supplier and customer.

8.5 Information about the various test methods cited is provided in Related Information 2 of SEMI M1 together with information about some additional test methods no longer in wide use throughout the industry.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 In the interest of controlling inspection costs, the supplier and the customer may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the

supplier is not required to perform the appropriate tests in §7. However, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Product Labeling

10.1 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductivity type, dopant, orientation, resistivity range, and lot number. The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one month after that particular lot has been accepted by the customer.

10.2 Alternatively, if agreed upon between supplier and customer, one of the box labeling schemes in SEMI T3 shall be used and the information listed in ¶10.1 that is not included on the label shall be retained in the supplier's data base for at least one month after that particular lot has been accepted by the customer.

10.3 Wafers of 300 mm diameter shall be shipped in packages labeled in accordance with SEMI M45.

11 Packing and Shipping Container Labeling

11.1 Special packing requirements shall be subject to agreement between the supplier and customer. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination and in accordance with the best industry practices to provide ample protection against damage during shipment.

11.2 Wafers of 300 mm diameter shall be shipped in accordance with SEMI M45.

11.3 Unless otherwise indicated in the purchase order, all outside wafer shipping containers shall be labeled in accordance with ANSI/EIA 556-B.

SEMI M58-0704
TEST METHOD FOR EVALUATING DMA BASED PARTICLE DEPOSITION SYSTEMS AND PROCESSES

This test method was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on April 22, 2004. Initially available at www.semi.org May 2004; to be published July 2004.

1 Purpose

1.1 SEMI M52 requires the use of certified reference materials (CRMs) for calibration of scanning surface inspection systems (SSISs). The calibration method is defined in SEMI M53. This test method provides the procedure to determine whether a specific particle deposition system, using a differential mobility analyzer (DMA), can produce the required CRMs.

1.2 Both organizations producing depositions internally for in-house use and companies manufacturing depositions for sale can apply this test method to ensure that their particle deposition systems provide depositions that meet the requirements of SEMI M52.

2 Scope

2.1 This test method covers determination of the deposition peak diameter and the associated expanded relative combined peak diameter uncertainty produced by a particle deposition system and its associated deposition procedures for comparison to the 3% requirement of SEMI M52.

2.2 This test method also covers determination of the ability of the deposition system to produce depositions with diameter distributions that are less than 5% full width at half maximum (FWHM) as required by SEMI M52 even when using a particle source with a much wider distribution.

2.3 These tests require that the deposition system employ a DMA (or an equivalent programmable filtering system) to accomplish both peak diameter determination and narrowing of particle source distributions (see Related Information 1).

2.4 This test method covers determination of repeatability over a period of one week. Tests can be repeated periodically to determine long term stability. Long term stability of most DMA-based particle deposition systems is believed to be on the order of a year or more, but it is recommended that the tests be repeated on an annual basis or whenever the instrument appears to be out of control.

2.5 This test method requires the use of three different kinds of particle distributions with specified characteristics and wafers that have surface characteristics adequate to allow detection of the smallest particles utilized with a capture rate of greater than 95%.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Limitations

3.1 This test method is limited to use of depositions of PSL spheres, even though the deposition system under test may be capable of depositing particles of other materials.

3.2 When used to make a deposition from a suspension of PSL spheres that does not have an observable certified peak diameter (or if the deposition is made at a size away from the peak of the distribution in the suspension), the uncertainty with which the deposition system evaluates a peak deposition diameter includes bias information determined from measurements on a known standard or standards with extremely narrow distributions. At the time when this test method was developed, only one such standard existed. Therefore if the bias contribution to uncertainty is a function of the peak diameter in the suspension, the determination may be in error at peak diameters away from that of the known standard.

3.3 There is the possibility that the deposited particle diameter may differ slightly from the certified value for the bottle containing the suspension because the surfactant in the suspension and contaminants in the water may cause an increase in particle size. This limitation can be avoided by using DMAs with the same spray system, the same purity of dilution water, and the same suspension concentration both to size the particles in the bottle and make the deposition. This possibility may be minimized by using PSL suspension fluids with low non-volatile content to reduce the possibility of non-volatile materials drying onto the particles in the suspension.

4 Referenced Standards

4.1 *SEMI Standards*

SEMI M50 — Test Method for Determining Capture Rate for Surface Scanning Inspection Systems by the Overlay Method

SEMI M52 — Guide for Specifying Scanning Surface Inspection Systems for Silicon Wafers for the 130-nm Technology Generation

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems using Depositions of Monodisperse Polystyrene Latex Sphere on Unpatterned Semiconductor Wafer Surfaces

SEMI MF1241 — Terminology of Silicon Technology

4.2 *ISO Standard*[1]

ISO 14644-1 Cleanrooms and associated controlled environments — Part 1: Classification of airborne particulates

NOTICE: As listed or revised, all documents cited shall be the latest publications of adopted standards.

5 Terminology

5.1 Definitions for terms related to surface scanning inspection systems are found in SEMI M50, SEMI M52, and SEMI M53.

5.2 Additional terminology related to silicon wafer technology is defined in SEMI MF1241.

6 Summary of Method

6.1 Three bottles (A, B and C) of PSL sphere suspensions meeting specific requirements are obtained. Bottle A is a CRM with a certified peak diameter and a very narrow diameter distribution so that no matter how the deposition system functions, the deposition will meet the requirements of SEMI M52. Bottles B (smaller diameters) and C (larger diameters) have much wider distributions and there are no restrictions on peak diameter accuracy.

6.2 Over a five day period, spot depositions of the same number of each of the three PSL sphere sizes are made each morning on one or more wafers and a final scan check of the diameter of spheres in Bottle A is made late in the day.

6.3 The deposited diameters from each bottle, as determined by the deposition system, are recorded on a data sheet.

6.4 At the end of the week the spot depositions are scanned with an SSIS to obtain a histogram for each spot deposition. The FWHM values are obtained from these histograms and recorded. The peak diameter values and particle counts found from the SSIS may also be recorded, but these values are not required to verify the requirements of SEMI M52.

6.5 The results for each bottle are analyzed to determine if the deposition system has a peak diameter expanded relative combined standard uncertainty less than 3% and a deposited FWHM on the wafer of less than 5%, as required by SEMI M52.

7 Apparatus

7.1 *Particle Deposition System*

7.1.1 The particle deposition system to be evaluated must be available in a clean room of class 4 or better as defined in ISO 14644-1.

7.1.2 The deposition system must have an atomizer that takes the particles from the liquid suspension to an air droplet mist.

7.1.3 The particle deposition system must have a DMA (or an equivalent programmable filtering system) to accomplish both peak diameter determination and narrowing of particle source distributions.

7.1.4 The deposition system must have wafer handling equipment appropriate for the wafers on which the depositions are being made.

7.2 *Surface Scanning Inspection System*

7.2.1 An SSIS appropriate for use with the wafers used and the PSL spheres deposited must be capable of determining the FWHM of each of the depositions made.

7.2.2 The SSIS does not have to be calibrated in accordance with SEMI M53 in order to be used in this test method, but the results obtained when the test method is performed can give an indication of the calibration of the SSIS in the size region of the test.

8 Reagents and Materials

8.1 *PSL Spheres*

8.1.1 Three types of PSL liquid sphere suspensions are used in this test method.

8.1.1.1 Bottle A is a CRM that contains a suspension of PSL spheres with a relative expanded peak diameter uncertainty much less than 3% and a FWHM less than

1 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch; also available in the US from American National Standards Institute, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023 Website: www.ansi.org, and in other countries from ISO member organizations.

5%. It is used in the measurement of (1) peak diameter repeatability and (2) peak diameter bias of the deposition system.[2]

8.1.1.2 Bottle B contains a suspension of PSL spheres with a single well defined peak diameter that is at least 20% smaller than that of the spheres in Bottle A, and a FWHM that is significantly larger than 5%. It is used in the measurement of (1) peak diameter repeatability and (2) FWHM of the deposition system when filtering a smaller diameter with a broad diameter distribution.

8.1.1.3 Bottle C contains a suspension of PSL spheres with a single well defined peak diameter that is at least 30% larger than Bottle A, and a FWHM that, if possible, is larger than 5%. It is used in the measurement of (1) peak diameter repeatability and (2) FWHM of the deposition system when filtering a larger diameter with a broad diameter distribution.

NOTE 1: Because spheres with peak diameters larger than 100 nm often have a FWHM smaller than 5% it may not be possible to secure a bottle with FWHM greater than 5%; in this case use a bottle with as large a FWHM as possible.

8.2 *Wafers*

8.2.1 One or more polished silicon wafers of appropriate diameter that have a high enough surface quality that the smallest PSL spheres deposited can be detected on the SSIS with a capture rate greater than 95% as determined in accordance with SEMI M53.

9 Preparation and Control of Apparatus

9.1 The deposition system under test must be available to run without scheduled, or unscheduled, maintenance or other interruption for the full five day test period.

9.2 Maintain a control chart of the voltage(s) associated with one or more peak diameters on a daily or weekly basis to ensure that the deposition system is under control.

9.3 Repeat the entire test procedure, calculations, and interpretation of results (see Sections 10 through 12) on an annual basis or whenever the control chart shows out of control conditions.

10 Procedure

10.1 Obtain three bottles of suspensions of PSL spheres (A, B and C) as described in Section 8.1. Record the peak diameter certified 1σ relative uncertainty, and %FWHM of the particle distribution in Bottle A on the data sheet. Record the supplier, part number, and lot number for each bottle of suspensions. If available, record the same information for Bottles B and C. An example data sheet is shown in Figure 1 and a completed example is shown in Figure R2-1.

NOTE 2: If desired, the data sheet can be set up as a spreadsheet that automatically completes the calculations discussed in Section 11. This spreadsheet is outlined in Related Information 2. If this is done, error messages will appear in the cells that contain the equations to perform the calculations until the data has been entered.

10.2 Record on the data sheet the laboratory name, the contact for the test, the address, telephone number, and e-mail address by which the contact can be reached, and the dates of the test.

10.3 Record on the data sheet the identification of the deposition system under test, including supplier and model number, serial number, and software revision. If the test has been performed previously on this deposition system, enter the date of the last previous test.

10.4 Choose one or more wafers upon which to make the depositions and load the first wafer into the deposition system.

10.5 Choose a value of *N* (between 1000 and 3000) particles for the deposition count and record this value on the data sheet. Use the same value of *N* for all depositions.

10.6 *Depositions on the First Day*

10.6.1 On the morning of the first day of a five day period, scan the particles from Bottle A in the deposition system to find the peak diameter. Record the peak diameter as found by the deposition system in the Day 1 row of the first Bottle A column of the Deposition System Diameter portion of the data sheet. Then use the deposition system, centered at the peak diameter, to make a deposition of *N* particles at a location on the first wafer.

10.6.2 Repeat this procedure for bottles B and C, recording the peak diameter as found by the deposition system in the appropriate Day 1 columns of the Deposition System Diameter portion of the data sheet.

10.6.3 Near the end of the day, make a final peak diameter scan (but not an additional deposition) of bottle A. Record the peak diameter as found by the deposition system in the Day 1 row of the second Bottle A column of the Deposition System Diameter portion of the data sheet.

10.7 Repeat the procedures of subsection 10.6 for the next four days, using additional locations on the wafer or on additional wafers.

10.8 At the end of the five days run the wafer (or wafers) on an SSIS, to obtain a histogram for each of the 15 depositions.

2 At the present time, NIST SRM 1963 meets these requirements.

10.8.1 Determine the FWHM values in nm obtained from the histograms and record these in the FWHM on Wafer columns of the SSIS Data portions of the data sheet.

10.8.2 If desired, enter the peak diameter values and counts found from the SSIS histograms in the Measured Peak and Count columns of the SSIS Data portions of the data sheet. These values may be used to evaluate SSIS calibration and deposition system count accuracy, respectively, but they are not used to evaluate the deposition system against the requirements of SEMI M52.

11 Calculations (see Note 2)

11.1 Calculate and record the mean diameter in nm to one decimal place and the relative standard deviation as a percentage of the mean of each of the four columns of the Deposition System Diameter portion of the data sheet.

11.2 Calculate and record the Relative FWHM in each appropriate column of the SSIS Data portions of the data sheet by dividing the FWHM in nm by the measured peak diameter in nm and converting to percent with two decimal places.

11.3 Calculate the mean and standard deviation of each of the columns in the three SSIS Data portions of the data sheet.

11.4 Calculate the expanded relative combined standard uncertainty, U_{relA}, for the peak diameter associated with the deposition from Bottle A as follows:

$$U_{relA} = 2\sqrt{s_{DepA}^2 + u_{BottleA}^2} \quad (1)$$

where:

s_{DepA} = pooled relative standard deviation for system repeatability associated with the deposition from Bottle A taken from the Deposition System Diameter Data portion of the data sheet by adding the square of the standard deviation from the five depositions made at the beginning of each day to the square of the standard deviation from the five scans made at the end of each day, dividing by 2, and taking the square root.

$u_{BottleA}$ = 1σ relative combined standard uncertainty of the peak diameter of the particle distribution in Bottle A as certified by the manufacturer found in the Bottle Peak Diameter portion of the data sheet.

Record the result as a percentage to one decimal place in the Bottle A column of the Dep Peak Uncertainty row of the Analysis portion of the data sheet. Take the certified value of the peak diameter of the deposition as the peak diameter of the deposition from Bottle A.

11.5 Calculate the expanded relative combined standard uncertainty, U_{relB}, for the peak diameter associated with the deposition from Bottle B as follows:

$$U_{relB} = 2\sqrt{s_{DepB}^2 + u_{BottleA}^2} \quad (2)$$

where:

s_{DepB} = relative standard deviation of the measured peak from Bottle B taken from the Deposition System Diameter Data: Bottle B portion of the data sheet, and

$u_{BottleA}$ has the same meaning as in Equation (1). The first term of this equation accounts for the variation due to the uncertainty in the finding of the peak diameter of Bottle B by the DMA and the second term accounts for the uncertainty in the certified peak diameter of the suspension in Bottle A, which is used to correct the peak diameter of Bottle B as found by the DMA. Record the result as a percentage to one decimal place in the Bottle B column of the Dep Peak Uncertainty row of the Analysis portion of the data sheet. Determine the peak diameter of the deposition from Bottle B as follows:

$$PeakDia_B = Mean_B\left(1 + \frac{Cert_A - Mean_A}{Cert_A}\right) \quad (3)$$

where:

$Mean_B$ = value of the mean deposition diameter from Bottle B taken from the Deposition System Diameter Data portion of the data sheet, and

$Mean_A$ = average mean deposition diameter from Bottle A taken from the Deposition System Diameter Data portion of the data sheet by adding the mean from the depositions at the beginning of the day to the mean from the scans at the end of the day, and

$Cert_A$ = value of the peak diameter in the suspension in Bottle A as certified by the manufacturer found in the Bottle Peak Diameter portion of the data sheet.

Record $PeakDia_B$ in the Bottle B column of the Peak(DepSysCorrected) row of the Analysis portion of the data sheet.

11.6 Calculate the expanded relative combined standard uncertainty, U_{relC}, for the peak diameter associated with the deposition from Bottle C as follows:

$$U_{relC} = 2\sqrt{s_{DepC}^2 + u_{BottleA}^2} \quad (4)$$

where:

s_{DepC} = relative standard deviation of the measured peak from Bottle C taken from the Deposition System Diameter Data: Bottle C portion of the data sheet, and

$u_{BottleA}$ has the same meaning as in Equation (1). Again, the first term of this equation accounts for the variation due to the uncertainty in the finding of the peak diameter of Bottle C by the DMA and the second term accounts for the uncertainty in the certified peak diameter of the suspension in Bottle A, which is used to correct the peak diameter of Bottle C as found by the DMA. Record the result as a percentage to one decimal place in the Bottle C column of the Dep Peak Uncertainty row of the Analysis portion of the data sheet. Take the peak height of the deposition as the chosen value of deposition diameter corrected as follows:

$$PeakDia_C = Mean_C\left(1+\frac{Cert_A - Mean_A}{Cert_A}\right) \qquad (5)$$

where:

$Mean_C$ = value of the mean chosen deposition diameter from Bottle C taken from the Deposition System Diameter Data portion of the data sheet, and

$Mean_A$ and $Cert_A$ have the same meaning as in Equation (3). Record $PeakDia_C$ in the Bottle C column of the Peak(DepSysCorrected) row of the Analysis portion of the data sheet.

11.7 Record the Mean Relative FWHM values for each of the three bottles in the SSIS Data sections as percentages with one decimal place in the FWHM SSIS row of the Analysis portion of the data sheet.

11.8 Average the two mean deposition system diameters for Bottle A found in the Deposition System Diameter data and record this average and the mean deposition system diameters for Bottles B and C in the Peak (Dep System) row of the Analysis portion of the data sheet. This is additional information only.

11.9 Record the Mean Measured Peak from the three SSIS Data sections for each of the three Bottles in the Peak (SSIS) row of the Analysis portion of the data sheet. This is additional information only.

11.10 Record the value of *N* (Particles Deposited) in the Count row of the Analysis portion of the data sheet.

12 Interpretation of Results

12.1 If a value for Bottle A, B, or C in the Dep Peak Uncertainty row of the Analysis portion of the data sheet is greater than 3.0%, the deposition system cannot be used with this bottle or these settings to produce calibration standards that meet the uncertainty requirements of SEMI M52.

12.2 If a value for Bottle A, B, or C in the FWHM row of the Analysis portion of the data sheet is greater than 5.0%, the deposition system cannot be used with this bottle or these settings to produce calibration standards that meet the FWHM requirements of SEMI M52.

12.3 Although it is not required by SEMI M52, the mean for the deposited diameters determined by the SSIS can be compared to the values found by the deposition system and the PSL sphere manufacturer. A significant difference in mean may imply that the SSIS is not properly calibrated.

12.4 Although it is not required by SEMI M52, the mean count values determined by the SSIS may be compared to the count value set by the deposition system. A significant difference may imply that the deposition system needs to be adjusted.

13 Report

13.1 Report all the information, data, and calculations recorded on the data sheet. A completed example of such a report is provided in Related Information 2.

14 Precision and Bias

14.1 No data regarding precision and bias are presently available. At present there are no plans to develop such data, but should such data become available, it will be added to this test method.

Lab:						**Identification of deposition system used:**						1
Contact						Supplier/Model #						2
Address						System S/N						3
						System S/W Revision						4
Phone						Date of Test						5
email						Date of Last Previous Test						6
												7
Characteristics of Suspensions Used for Test												8
Suspension	*Peak Diameter*						$u_{Bottle\ i}$		$\%FWHM_i$			9
Bottle A, Certified		nm	±		nm (1σ) or							10
Bottle B		nm	±		nm (1σ) or							11
Bottle C		nm	±		nm (1σ) or							12
Particles Deposited (*N*)												13
							Supplier	***Part No.***	***Lot No.***			14
Deposition System Diameters (nm)						*Bottle A*						15
	Bottle A	*Bottle B*	*Bottle C*	*Bottle A*		*Bottle B*						16
Day	nm	nm	nm	nm		*Bottle C*						17
1												18
2												19
3						**SSIS Data: Bottle C**						20
4							*Measured Peak*	*FWHM on Wafer*	*Relative FWHM*	*Count*		21
5												22
Mean						*Day*	nm	nm	%			23
s_{Dep}						*1*						24
						2						25
Dep System Sizing Corrections						*3*						26
$Mean_A$ =		nm				*4*						27
s_{DepA} =						*5*						28
$Cert_A - Mean_A$ =		nm				*Mean*						29
						Std Dev						30
SSIS Data: Bottle A												31
	Measured Peak	*FWHM on Wafer*	*Relative FWHM*	*Count*		**Analysis**						32
								Bottle A	*Bottle B*	*Bottle C*		33
Day	nm	nm	%			*Dep Peak Uncertainty*						34
1						*FWHM (SSIS)*						35
2						*Peak (Dep System)*						36
3						*Peak (Dep Sys Corrected)*						37
4						*Peak (SSIS)*						38
5						*Measured Count*						39
Mean												40
Std Dev						**Compare Quantity with Limit**						41
						Quantity		*Limit*				42
SSIS Data: Bottle B						*Uncertainty Limit*		3.0% (SEMI M52)				43
	Measured Peak	*FWHM on Wafer*	*Relative FWHM*	*Count*		*FWHM Limit*		5.0% (SEMI M52)				44
						SSIS Peak		Dep Sys Corrected Peak (Info only)				45
Day	nm	nm	%			*SSIS Count*		Dep System Count (Info only)				46
1												47
2						**Interpretation of Results**						48
3								*Bottle A*	*Bottle B*	*Bottle C*		49
4						*Uncertainty*						50
5						*FWHM*						51
Mean						*SSIS/Dep Peak Comp*						52
Std Dev						*SSIS/Dep Count Comp*						53
A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**		

Figure 1
Example of Data, Calculation, and Analysis Sheet for Test Procedure

RELATED INFORMATION 1
BACKGROUND INFORMATION ON THE OPERATION OF A DIFFERENTIAL MOBILITY ANALYZER

NOTICE: This related information is not an official part of SEMI M58 and was derived from information developed during drafting of the standard. This related information was approved for publication by full letter ballot procedures on April 22, 2004.

R1-1 Deposition systems include a nebulizer for producing a PSL sphere aerosol by spraying and evaporating a suspension of PSL spheres in high purity water, a differential mobility analyzer (DMA) for selecting a monodisperse fraction of the aerosol, and then a chamber to electrostatically deposit the spheres onto wafers. Here we focus on the DMA, which is used for both isolating a monodisperse size fraction and for sizing the particles. A brief description of the instrumentation and methodology is given below; a detailed description is given by Kinney *et al*.[3]

R1-2 The particles leaving the nebulizer pass through a bipolar charger that produces a charge distribution that depends only on the size of the particles and not on their initial charge. For 100 nm particles, about 45% of the particles are uncharged, about 20% have + 1 electron charge, another 20% have –1 electron charge, and much smaller fractions have multiple charges. As illustrated in Figure R1-1, the DMA consists of an inner cylindrical rod connected to a variable high voltage dc power supply and an outer annular tube connected to ground. Clean sheath air flows through the axial region, while the charged aerosol enters through an axisymmetric opening along the outer cylinder. The positively charged PSL spheres move radially towards the center rod under the influence of the electric field. Near the bottom of the classifying region, a fraction of the air flow consisting of near-monodisperse aerosol exits through a slit in the center rod. The quantity measured by the DMA is the electrical mobility, $Z_{p,}$ defined as the velocity a particle attains under a unit electric field. Knutson and Whitby[4] derived an expression for the average value of Z_p for particles entering the slit involving the peak electrode voltage, V, the sheath air flow rate, Q_c, the inner and outer radii of the cylinders, r_1 and r_2 , and the length of the central electrode down to the slit, L:

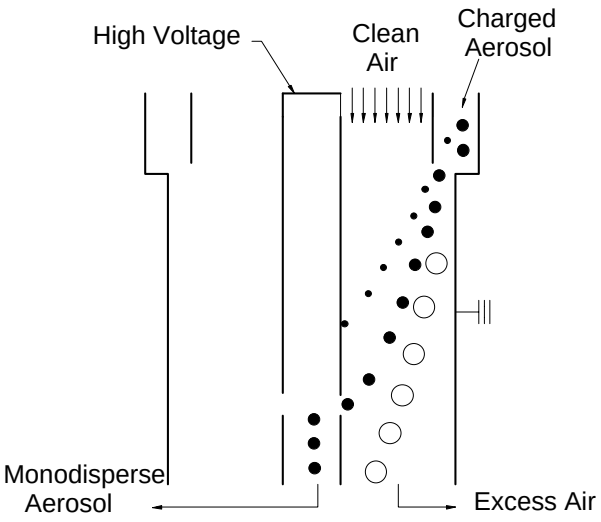


Figure R1-1
Monodisperse Aerosol Selected in a Differential Mobility Analyzer from a Polydisperse Aerosol Based on the Size Dependence of the Electrical Mobility

$$Z_p = \frac{Q_c}{2\pi VL}\ln\left(\frac{r_2}{r_1}\right) \qquad \text{(R1-1)}$$

R1-3 This equation is valid provided the sheath air flow, Q_c, is equal to the excess flow, Q_m, leaving the classifier. They derived an expression for the transfer function, defined as the probability that a particle will leave the sampling slit. The transfer function is of great importance, because the size distribution of the aerosol exiting the DMA is proportional to the convolution of the transfer function with the particle size distribution function. The transfer function has a triangular shape with a peak value of 1. The ratio of the base of the transfer function triangle in terms of voltage divided by the peak voltage is predicted to be $2(Q_s/Qc)$, where Q_s is the flow of monodisperse aerosol.

R1-4 This ratio is also equal to the ratio of the full width of the mobility distribution to the peak value. For a flow ratio of 1 to 20, one finds that the full width at half maximum of the peak mobility (FWHM) is equal to 5% of the peak mobility. For 100 nm particle

3 Kinney, P.D., Pui, D. Y. H., Mulholland, G. W., and Bryner, N., "Use of the Electrostatic Classification Method to Size 0.1 μm SRM® Particles – A Feasibility Study," *J. Res. Natl. Inst. Technol.,* **96**, 147–176 (1991).

4 Knutson, E. O., and Whitby, K. T. "Aerosol Classification by Electric Mobility: Apparatus, Theory, and Applications," *J. Aer. Sci.* **6**: 443–451 (1975).

size, the corresponding FWHM in terms of particle diameter is about 3%.

R1-5 The relationship between electrical mobility and particle diameter, D_p, is obtained by equating the electric field force of a singly charged particle with the Stokes friction force,

$$Z_p = \frac{e\,C(D_p)}{3\pi\mu D_p} \qquad \text{(R1-2)}$$

where μ is the dynamic viscosity of air, and e is the electron charge. The Cunningham slip correction, $C(D_p)$, corrects for the non-continuum gas behavior on the motion of small particles.

R1-6 For increased accuracy, the DMA can be calibrated using the NIST SRM® 1963 (100 nm) PSL spheres.[5] The voltage corresponding to the peak particle concentration for the 100.7 nm SRM is determined and then the peak voltage is determined for the unknown. The electrical mobility of the 100.7 nm SRM®, Z_{SRM}, is computed from Equation (R1-2) using the best available values for the viscosity, Cunningham slip correction, and the electron charge.[6] The mobility of the unknown particle, Z_x, is then computed based on the voltage ratio and the mobility of the 100.7 nm SRM, Z_{SRM}:

$$Z_x = \frac{V_{SRM}}{V_x} Z_{SRM} \qquad \text{(R1-3)}$$

The peak particle diameter is computed using Equation (R1-2). Because the slip correction is a function of the diameter, an iterative process is used. In cases where samples have a broad size distribution, a correction factor is used that is based on the instrument convolution integral and involves the product of the transfer function times, the charging probability, and the size distribution (see Related Information 1 of SEMI M53 for a further discussion of the effect of the transfer function).

5 Donnelly, M. K., Mulholland, G. W., and Winchester, M. R., "NIST Calibration Facility for Sizing Spheres Suspended in Liquids," *Characterization and Metrology for ULSI Technology* (AIP, Mellville, N. Y., 2003), pp. xxx–yyy..

6 Donnelly, M. K., and Mulholland, G. W., "Particle Size Measurements for Spheres with Diameters of 50 nm to 400 nm," U.S. Department of Commerce, NISTIR 6935, National Institute of Standards and Technology, Gaithersburg, November 2002.

RELATED INFORMATION 2
EXAMPLE OF A COMPLETED DATA AND ANALYSIS SHEET

NOTICE: This related information is not an official part of SEMI M58 and was derived from information developed during drafting of the standard. This related information was approved for publication by full letter ballot procedures on April 22, 2004.

R2-1 Figure R2-1 shows an example of a completed data set. This example is the result of using a spreadsheet that automates the calculations of Section 11. If such a spreadsheet is constructed, once the data is input as described in Section 10 the results of the test are found by spreadsheet calculation.

R2-2 In this example the results obtained indicate that the deposition system is capable of meeting the requirements of SEMI M52 for all three bottles. Note that the test was done with an SSIS that was not calibrated according to SEMI M53.

R2-3 The following sections detail the spreadsheet example in Figure R2-1 in order to allow it to be easily duplicated for use with this test method. Information in the shaded cells is entered in accordance with the procedures given in Section 10.

R2-3.1 At the top of the spreadsheet, the entries in rows 1 through 13 are obvious except for those in cells H10 through H12. Here, the uncertainties on the bottle are converted to %. In this example, Bottle C does not have a peak diameter uncertainty given. This is true for many older bottles where diameters were given in terms of mean, rather than peak, diameters. To avoid returning an error result, the formula for the percentage is =IF(SUM(E*i*>0,E*i*/C*i*," not available"), where *i* = 10, 11, or 12 for Bottle A, B, or C, respectively. The cell is formatted for % with one decimal place.

R2-3.2 In the section on Deposition System Diameters and the three SSIS Data sections the inputs are taken directly from the instrumentation as directed in Section 10. As an example, the equation to compute mean in B23 is: =AVERAGE(B18:B22). The equation to compute s_{Dep} in B24 is: =STDEV(B18:B22)/B23 and is formatted for % with one decimal place.

R2-3.3 The portion of the data sheet labeled “Dep System Sizing Corrections” starting at A26 uses all Bottle A results to correct any offset in the mean diameter found by deposition system and to evaluate the pooled relative standard deviation for system repeatability. $Mean_A$ is given by: =(B23+ E23)/2. s_{DepA} is given by: =SQRT((B24^ 2+ E24^ 2)/2), and includes day long contributions from system stability. The bias correction $Cert_A – Mean_A$ is given by: =C10-C27.

R2-3.4 *Analysis*

R2-3.4.1 The value for Dep Peak Uncertainty (row 34) for Bottle A (or U_{relA}) is given by: =2*SQRT(C28^ 2+ H10^ 2). This combines the uncertainty in the certified bottle with the uncertainty in the deposition system at the diameter of Bottle A. The factor of 2 is needed for expanded uncertainty.

R2-3.4.2 The expanded uncertainty equations for Bottles B and C are slightly different and are the combination of the relative uncertainty in the certified value A (as a percent) and the relative uncertainty of the deposition system at the broader distribution of diameter B or C. The equation for the expanded relative combined standard uncertainty of the depositions of Bottle B is: =2*SQRT(C24^ 2+ H10^ 2), and of those of Bottle C is: =2*SQRT(D24^ 2+ H10^ 2). As noted in the standard (see 11.5 and 11.6), the first term of this equation accounts for the variation due to the uncertainty in the finding of the peak diameter of Bottle B or C by the DMA and the second term accounts for the uncertainty in the certified peak diameter of the suspension in Bottle A, which is used to correct the peak diameter of Bottle B or C as found by the DMA.

R2-3.4.3 The FWHM (SSIS) values for Bottles A, B, and C (row 35) are taken directly from D40, D52 and J29, respectively.

R2-3.4.4 The uncorrected Peak (Dep System) diameters for Bottles A, B, and C (row 36) are taken directly from C27, C23, and D23 respectively.

R2-3.4.5 The corrections made in the next row (37) employ the percentage error found by comparing the certified peak diameter of Bottle A to the mean peak diameter found by the deposition system. For Bottle A this is: =C27+ C29. For Bottle B it is: =C23*(1+ (C29/C10), and for Bottle C it is: =D23*(1+ (C29/C10).

R2-3.4.6 The Peak (SSIS) values Bottles A, B, and C (row 38) are taken directly from B40, B52, and H29, respectively.

R2-3.4.7 The Measured Counts (row 39) are taken directly from the SSIS data averages, E40, E52, or K29, for Bottles A, B, and C, respectively.

R2-3.5 *Interpretation of Results*

R2-3.5.1 A conditional command is used to automatically grade results for Uncertainty and FWHM.

R2-3.5.1.1 The equation for Bottle B Uncertainty (row 50) is: =IF(J34>0.03," Fail" ," Pass"), and the others are similar.

R2-3.5.1.2 The equation for Bottle B FWHM (row 51) is =IF(J35>0.05," Fail" ," Pass"), and the others are similar.

R2-3.5.2 These are the only two requirements of SEMI M52 verified by this test method. Two additional comparisons are made for information only:

R2-3.5.2.1 The SSIS Peak diameter is compared with the corrected deposition system peak diameter (row 52). For Bottle B the equation is =B52/J37, and the others are similar.

R2-3.5.3 Finally, the SSIS mean count is compared with the count from the deposition system (row 53). The equation for Bottle B is =E52/$ D$ 13, and the others are similar.

Lab:	Company ABC					**Identification of deposition system used:**						1
Contact	N. P. Tester					Supplier/Model #	Dep Sys/45U					2
Address	456 Main Street					System S/N	12345					3
	Anywhere, CA, USA					System S/W Revision	3					4
Phone	782-555-5555					Date of Test	August 20, 2003					5
email	nptester@abcco.com					Date of Last Previous Test	Not applicable					6
												7
Characteristics of Suspensions Used for Test												8
Suspension	*Peak Diameter*						$u_{Bottle\ i}$		$\%FWHM_i$			9
Bottle A, Certified	100.7	nm	±	0.5	nm (1σ)	or	0.5%		2.0%			10
Bottle B	79	nm	±	2.6	nm (1σ)	or	3.3%		10.0%			11
Bottle C	145	nm	±	nominal	nm (1σ)	or	not available		unknown			12
Particles Deposited (*N*)	3000											13
							Supplier	***Part No.***	***Lot No.***			14
Deposition System Diameters (nm)						*Bottle A*	NIST	SRM 1963	? ?			15
	Bottle A	*Bottle B*	*Bottle C*	*Bottle A*		*Bottle B*	? ?	? ?	? ?			16
Day	nm	nm	nm	nm		*Bottle C*	? ?	? ?	? ?			17
1	101.5	79.6	155.6	101.0								18
2	100.5	79.0	153.9	101.0								19
3	101.0	78.2	154.6	102.0		**SSIS Data: Bottle C**						20
4	102.0	78.5	155.9	102.0			*Measured Peak*	*FWHM on Wafer*	*Relative FWHM*	*Count*		21
5	101.0	78.1	154.3	102.0								22
Mean	101.2	78.7	154.9	101.6		*Day*	nm	nm	%			23
s_{Dep}	0.6%	0.8%	0.6%	0.5%		*1*	149.2	3.3	2.21%	2815		24
						2	148.9	3.6	2.42%	2548		25
Dep System Sizing Corrections						*3*	150.9	3.4	2.25%	2720		26
$Mean_A$ =	101.4	nm				*4*	151.1	3.6	2.38%	2716		27
s_{DepA} =	0.6%					*5*	149.7	3.4	2.27%	2178		28
$Cert_A - Mean_A$ =	-0.7	nm				*Mean*	150.0	3.5	2.31%	2595		29
						Std Dev	0.994	0.134	0.088%	252.4		30
SSIS Data: Bottle A												31
	Measured Peak	*FWHM on Wafer*	*Relative FWHM*	*Count*		**Analysis**						32
							Bottle A	*Bottle B*	*Bottle C*			33
Day	nm	nm	%			*Dep Peak Uncertainty*	1.5%	1.9%	1.5%			34
1	95.6	2.1	2.20%	2178		*FWHM (SSIS)*	2.3%	3.3%	2.3%			35
2	95.9	2.2	2.29%	2418		*Peak (Dep System)*	101.4	78.7	154.9			36
3	96.1	2.3	2.39%	2555		*Peak (Dep Sys Corrected)*	100.7	78.1	153.8			37
4	96.1	2.2	2.29%	2512		*Peak (SSIS)*	96	72	150			38
5	96.2	2.2	2.29%	1929		*Measured Count*	2318	2524	2595			39
Mean	96.0	2.2	2.29%	2318								40
Std Dev	0.239	0.071	0.070%	262.1		**Compare Quantity with Limit**						41
						Quantity	*Limit*					42
SSIS Data: Bottle B						*Uncertainty Limit*	3.0% (SEMI M52)					43
	Measured Peak	*FWHM on Wafer*	*Relative FWHM*	*Count*		*FWHM Limit*	5.0% (SEMI M52)					44
						SSIS Peak	Dep Sys Corrected Peak (Info only)					45
Day	nm	nm	%			*SSIS Count*	Dep System Count (Info only)					46
1	72.6	2.4	3.31%	2297								47
2	71.6	2.3	3.21%	2690		**Interpretation of Results**						48
3	72.2	2.3	3.19%	2742			*Bottle A*	*Bottle B*	*Bottle C*			49
4	72.2	2.3	3.19%	2735		*Uncertainty*	Pass	Pass	Pass			50
5	71.2	2.5	3.51%	2156		*FWHM*	Pass	Pass	Pass			51
Mean	72.0	2.4	3.28%	2524		*SSIS/Dep Peak Comp*	0.95	0.92	0.98			52
Std Dev	0.555	0.089	0.138%	276.8		*SSIS/Dep Count Comp*	0.77	0.84	0.87			53
A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**		

Figure R2-1
Example Test Results

NOTICE: SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer' s instructions, product labels, product data sheets, and other relevant literature, respecting any materials or equipment mentioned herein. These standards are subject to change without notice.

By publication of this standard, Semiconductor Equipment and Materials International (SEMI) takes no position respecting the validity of any patent rights or copyrights asserted in connection with any items mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights are entirely their own responsibility.

SEMI M59-0305
TERMINOLOGY FOR SILICON TECHNOLOGY

This standard was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on December 10, 2004. Initially available at www.semi.org February 2005; to be published March 2005.

NOTICE: This document replaces SEMI MF1241.

1 Purpose

1.1 Silicon technology underlies the integrated circuit and device industry. To promote common understanding and correct communication between suppliers and customers and others in the field, terms used in this field should be defined.

1.2 This terminology document covers definitions of terms used in relation to semiconductor silicon crystals and wafers.

2 Scope

2.1 This terminology covers terms describing attributes of silicon wafers as specified in SEMI M1 and other SEMI standards as outlined in SEMI M1. These attributes include electrical, structural, chemical, and dimensional characteristics of polished and other types of silicon wafers as well as surface defects and contamination.

2.2 This terminology is applicable for use in connection with research, development, process control, inspection, and procurement of silicon material.

2.3 Almost all of the terms for which definitions are listed are nouns. Unless the part of speech is given for any particular term, it can be assumed that the term is a noun.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standard*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

3.2 *ISO Standard*[1]

ISO 4287/1 — Surface Roughness – Terminology – Part 1: Surface and its Parameters

3.3 *ANSI Standard*[2]

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Abbreviations and Acronyms

4.1 *AAS* — atomic absorption spectroscopy, a method for analyzing for impurities.

4.2 *AFM* — atomic force microscope, an instrument for measuring microroughness.

4.3 *A/N* — alphanumeric.

4.4 *ANSI* — American National Standards Institute[2], the American member of ISO.

---

1 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30 Website: www.iso.ch.

2 American National Standards Institute, New York Office: 25 West 43rd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023 Website: www.ansi.org.

4.5 *As* — arsenic, an *n*-type dopant in silicon.

4.6 *ASTM* — ASTM International,[3] previously the American Society for Testing and Materials, an American organization that developed standards for silicon technology between 1964 and 2002; these standards, though developed primarily by American experts have been used world-wide.

4.7 *B* — boron, a *p*-type dopant in silicon.

4.8 *BMD* — bulk micro defect.

4.9 *BRDF* — bi-directional reflectance distribution function.

4.10 *CCW* — counterclockwise, rotation in the direction opposite to that of the hands of a clock.

4.11 *COP* — crystal originated pit, a small pit or plurality of small pits introduced during crystal growth that act as an LLS.

4.12 *CRM* — certified reference material.

4.13 *CVD* — chemical vapor deposition, a method for producing epitaxial films.

4.14 *CW* — clockwise, rotation in the direction of the hands of a clock.

4.15 *Cz* — Czochralski, a type of crystal growth.

4.16 *DDS* — difference data set, the difference between the reference data set and the sample data set.

4.17 *DI* — deionized, generally referred to in connection with electronic grade water.

4.18 *DIN* — Deutches Institut für Normung,[4] the German national standards organization, which has developed numerous standards for silicon during the last three decades.

4.19 *FPD* — focal plane deviation.

4.20 *FQA* — fixed quality area of a silicon wafer.

4.21 *FZ* — float zone, a type of crystal growth.

4.22 *GBIR* — the most common type of global flatness, see Appendix 1 of SEMI M1 for other types of global flatness.

4.23 *GFA* — gas fusion analysis, a method for measuring total oxygen in silicon.

4.24 *GRR* — grand round robin, the international interlaboratory experiment that established IOC-88.

4.25 *IC* — integrated circuit.

4.26 *ICP/MS* — inductively coupled plasma mass spectroscopy, a method for analysis of impurities, not yet standardized.

4.27 *IOC-88* — international oxygen conversion factor-1988, the currently universally adopted conversion factor between the infrared absorption peak and the interstitial oxygen content in silicon.

4.28 *ID* — identification, referring to the laser mark on silicon and other semiconductor wafers.

4.29 *ISO* — International Organization for Standardization,[1] a body recognized by the World Trade Organization as a developer of international standards, including a few applicable to silicon technology.

4.30 *JEIDA* — Japan Electronic Industry Development Association, now JEITA

4.31 *JEITA* — Japanese Electronic and Information Technology Industries Association,[5] successor to JEIDA upon the merging of JEIDA and the Electronic Industries Association of Japan (EIAJ), which has a committee that develops standards for silicon materials and technology.

---

3 ASTM International, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org.

4 Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D 10787 Berlin, Germany, website: www.din.de.

5 Japan Electronics and Information Technology Industries Association, 3rd floor, Mitsui Sumitomo Kaijo Bldg. Annex, 11, Kanda-Surugadai 3-chome, Chiyoda-ku, Tokyo 101-0062, Japan, Website: www.jeita.or.jp.

4.32 *JIS* — Japan Industrial Standard, standards published by the Japanese Standards Association.[6]

4.33 *LLS* — localized light scatterer.

4.34 *LPD* — light point defect, a term formerly widely used, but now superseded by the term LLS.

4.35 *MAE* — mixed acid etchant.

4.36 *MCz* — magnetic Czochralski, a type of crystal growth that generally yields crystals with lower oxygen content than Cz growth.

4.37 *NTD* — neutron transmutation doped, a method for forming high resistivity *n*-type silicon.

4.38 *OSF* — oxidation induced stacking fault, a defect in silicon wafers.

4.39 *P* — phosphorus, an *n*-type dopant in silicon.

4.40 *ppba* — parts per billion atomic.

4.41 *ppbw* — parts per billion by weight.

4.42 *ppma* — parts per million atomic.

4.43 *ppmw* — parts per million by weight.

4.44 *PSD* — power spectral density.

4.45 *PTFE* — polytetrafluoroethylene, an HF-resistant material for sample bottles, lids, and tongs.

4.46 *RDS* — reference data set.

4.47 *rf* — radio frequency.

4.48 *RPD* — reference plane deviation.

4.49 *RSF* — relative sensitivity factor, used in TXRF analysis of surface metals to relate the concentrations of a variety of elements to the calibration element.

4.50 *Sb* — antimony, an *n*-type dopant in silicon.

4.51 *SCFM* — standard cubic feet per minute.

4.52 *SDS* — sample data set.

4.53 *SFQR* — the most commonly used type of site flatness, see Appendix 1 of SEMI M1 for other types of site flatness.

4.54 *Si* — silicon.

4.55 *SIMS* — secondary ion mass spectroscopy, a method for analysis of impurities.

4.56 *SPC* — statistical process control.

4.57 *SRM* — registered trademark for a CRM produced by the National Institute for Standards and Technology.

4.58 *SSIS* — scanning surface inspection system, an automated instrument for examining the surface of silicon wafers for LLSs and XLSs.

4.59 *TIR* — total indicator reading (also known as total indicator runout).

4.60 *TTV* — total thickness variation.

4.61 *TXRF* — total reflection x-ray reflectance spectroscopy, a surface metal analysis technique.

4.62 *VPD* — vapor phase decomposition, a method for dissolving an oxide film containing impurities to be examined by means of hydrofluoric (HF) acid vapor.

---

6 Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp.

4.63 *XLS* — extended light scatterer, a relatively large surface defect on silicon wafers, such as scratches and regions of high surface roughness.

5 Definitions

5.1 *acceptor* — an impurity in a semiconductor that accepts electrons excited from the valence band, leading to hole conduction.

5.2 *anisotropic, adj.* — exhibiting different physical properties in differing crystallographic directions.

5.3 *anisotropic etch* — a selective etch that exhibits an accelerated etch rate along specific crystallographic directions.

5.3.1 *Discussion* — Anisotropic etches are used to determine crystal orientation, to fabricate micromechanical structures, and to facilitate dielectric component isolation.

5.4 *annealed wafer* — wafer that has a defect (COP) free zone near the surface resulting from high temperature annealing under a neutral or reducing atmosphere.

5.5 *back surface* — the exposed surface opposite to that upon which active semiconductor devices have been or will be fabricated.

5.6 *backseal* — a film of silicon dioxide or other insulator placed over the back surface of a silicon wafer to inhibit outdiffusion of the majority dopant impurity.

5.7 *backside* — not preferred, use *back surface*.

5.8 *bow* — the deviation of the center point of the median surface of a free, unclamped wafer from a median-surface reference plane established by three points equally spaced on a circle with diameter a specified amount less than the nominal diameter of the wafer.

5.9 *carrier* — an entity capable of carrying electric charge through a solid, for example, valence holes and conduction electrons in semiconductors; also known as *charge carrier*.

5.10 *chem-mechanical polish* — a process for the removal of surface material from the wafer that uses chemical and mechanical actions to achieve a mirror-like surface for subsequent processing.

5.11 *chip* — region where material has been unintentionally removed from the surface or edge of the wafer.

5.12 *cleavage plane* — a crystallographically preferred fracture plane.

5.13 *concentration* — relative amount of a minority constituent of a mixture to the majority constituent (for example parts per million, parts per billion, or percent) by either volume or weight.

5.14 *conductivity* (*electrical*), σ $[(\Omega \cdot cm)^{-1}]$ — a measure of the ease with which charge carriers flow in a material; the reciprocal of *resistivity.*

5.14.1 *Discussion* — In a semiconductor, the conductivity is proportional to the product of free carrier density, electron electrical charge, and carrier mobility. Most variant of all crystal properties, conductivity can range over 13 orders of magnitude. Conductivity can be locally modified by temperature, carrier injection, irradiation, or magnetic field.

5.15 *conductivity type* — a property that identifies the majority charge carrier in the semiconductor; see also *n-type*, *p-type*.

5.16 *contaminant, particulate* — see *localized light scatterer*.

5.17 *contamination, area* — matter, unintentionally added to the surface of a wafer, of extent greater than a single localized light scatterer.

5.17.1 *Discussion* — Area contamination, a type of extended light scatterer, may be foreign matter on the wafer surface resulting from chuck marks, finger or glove prints, stains, wax or solvent residues, etc.

5.18 *contamination, particulate* — a particle or particles on the surface of a wafer, see *localized light scatterer*.

5.19 *crack* — cleavage or fracture that extends to the surface of a wafer.

5.20 *crater* — surface feature with irregular closed ridges and smooth central regions.

5.21 *Crow's foot* — intersecting cracks in a pattern resembling a "crow's foot" (*Y*) on (111) surfaces and a cross (+) on (100) surfaces.

5.22 *crystal defect* — departure from the ideal arrangement of atoms in a crystal.

5.23 *crystal indices* — see *Miller indices*.

5.24 *crystal originated pit, COP* — a small pit or plurality of small pits introduced during crystal growth that act as an LLS when they intersect the surface of a wafer.

5.24.1 *Discussion* — Because they act in some ways similarly to particles when viewed with an SSIS, this defect was originally called a crystal originated particle. Modern SSISs can, however, generally distinguish COPs from particles. Surface cleaning or light etching frequently increases the size and number of COPs observed, when they are present.

5.25 *crystallographic notation* — a symbolism based on Miller indices used to label planes and directions in a crystal as follows:

- plane (111)
- family of planes {111}
- direction [111]
- family of directions <111>

5.26 *denuded zone* — a volume in a wafer, usually located just under the front surface, in which the oxygen content has been lowered so that the bulk microdefect (oxide precipitate) density is reduced.

5.27 *diameter, of a semiconductor wafer* — the linear dimension across the surface of a circular wafer that contains the wafer center and excludes flats or other peripheral fiduciary geometries.

5.28 *dimple* — a shallow depression with gently sloping sides that exhibits a concave, spheroidal shape and is visible to the unaided eye under proper lighting conditions.

5.29 *dislocation etch pit* — a pit generated by a preferential etch where a dislocation meets the surface of a wafer.

5.30 *donor* — an impurity or imperfection in a semiconductor that donates electrons to the conduction band, leading to electron conduction.

5.31 *dopant* — a chemical element, usually from the third or fifth columns of the periodic table, incorporated in trace amounts in a silicon crystal to establish its conductivity type and resistivity.

5.32 *dopant striation rings* — helical features on the surface of a silicon wafer associated with local variations in impurity concentration.

5.33 *doping, v.* — addition of specific impurities to a semiconductor to control the electrical resistivity.

5.34 *edge exclusion, nominal, EE* — the distance from the FQA boundary to the periphery of a wafer of nominal dimensions.

5.35 *edge profile* — on edge contoured wafers (whose edges have been shaped chemically or mechanically), a description of the contour of the boundary of the wafer that joins the front and back surfaces.

5.36 *etch* — a solution, a mixture of solutions, or a mixture of gases that attacks the surfaces of a film or substrate, removing material either selectively or nonselectively.

5.37 *etch pit* — a pit, resulting from preferential etching, localized on the surface of a wafer at a crystal defect or stressed region.

5.38 *extended light scatterer (XLS)* — a feature larger than the spatial resolution of the inspection equipment, on or in a wafer surface, resulting in increased light scattering intensity relative to that of the surrounding wafer surface.

5.38.1 *Discussion* — Origins of XLSs include area contamination and unresolved clusters of localized light scatterers, such as particles or COPs. When oberved by the unaided eye, an XLS can usually be seen under high

intensity illumination. Some SSISs have sensors for reporting XLSs. XLSs can be observed as increased haze under dark field conditions. Under bright field conditions, an XLS can be observed as a decrease in the intensity of the specularly reflected beam, sometimes called a light channel defect.

5.39 *extrinsic, adj.* — (1) the region in the conductivity-temperature curve where the conduction in a wafer is dominated by holes or electrons from dopant atoms; (2) a process, such as extrinsic gettering, caused by factors outside the crystal of the wafer itself.

5.40 *fiducial* — a flat or a notch on a wafer intended to provide a location referenced to its crystallographic axes.

5.41 *fixed quality area, FQA* — the central area of a wafer surface, defined by a nominal edge exclusion, *EE*, over which the specified values of a parameter apply.

5.41.1 *Discussion* — The boundary of the FQA is at all points the distance *EE* away from the periphery of a wafer of nominal dimensions. The size of the FQA is independent of wafer diameter and flat length tolerances. For the purposes of defining the FQA, the periphery of a wafer of nominal dimensions at a location with a notch is assumed to follow the circumference of a circle with diameter equal to the nominal wafer diameter. It may be necessary to specify exclusion areas where the values of a specified parameter do not apply for regions like: the notch, laser marks, or where handling/gripping devices contact the wafer.

5.42 *flat* — a portion of the periphery of a circular wafer that has been removed to a chord; see also *primary flat*, *secondary flat*.

5.43 *flat diameter* — the linear dimension across the surface of a semiconductor wafer from the center of the flat through the wafer center to the circumference of the wafer on the opposite edge along the diameter perpendicular to the flat.

5.43.1 *Discussion* — The flat diameter is most often associated with the primary flat. In the case of opposing primary and secondary flats, as occurs on {100} *n*-type wafers 125 mm and smaller in diameter, the concept of flat diameter does not apply because the diameter perpendicular to the flats does not intersect the wafer circumference.

5.44 *flatness* — for wafer surfaces, the deviation of the front surface, expressed in TIR or maximum FPD relative to a specified reference plane when the back surface of the wafer is ideally flat, as when pulled down by a vacuum onto an ideally clean flat chuck.

5.44.1 *Discussion* — The flatness of a wafer may be described as either:

- the global flatness,
- the maximum value of site flatness as measured on all sites, or
- the percentage of sites that have a site flatness equal to or less than a specified value.

NOTE 1: See Appendix 1 of SEMI M1 for a complete discussion of flatness parameters.

5.45 *focal plane* — the plane perpendicular to the optical axis of an imaging system that contains the focal point of the imaging system.

5.45.1 *Discussion* — The reference plane used by an imaging system is coincident with or parallel with the focal plane. Full field imaging systems employ coincident global focal and reference planes. Partial field imaging systems employ either coincident site focal and reference planes or displaced site focal and global reference planes. If the reference plane is not coincident with the focal plane, it is displaced from the focal plane so that the point on the front surface at a site center lies in the focal plane.

5.46 *focal plane deviation*, *FPD* — the distance parallel to the optical axis from a point on the wafer surface to the focal plane.

5.47 *four-point probe* — an electrical probe arrangement for determining the resistivity of a material in which separate pairs of contacts are used (1) for passing current through the specimen and (2) measuring the potential drop caused by the current.

5.48 *front side* — not preferred; use *front surface*.

5.49 *front surface* — the exposed surface upon which active semiconductor devices have been or will be fabricated.

5.50 *gettering* — the process that immobilizes impurities at locations away from the region of the specimen to be investigated.

5.51 *global flatness* — the TIR or the maximum FPD relative to a specified reference plane within the FQA.

5.52 *gradient, resistivity* — not preferred; use *resistivity variation*.

5.53 *groove* — a shallow scratch with rounded edges that is usually the remnant of a scratch not completely removed by polishing.

5.54 *haze* — non-localized light-scattering resulting from surface topography (microroughness) or from dense concentrations of surface or near-surface imperfections; see also *laser light-scattering event*.

5.54.1 *Discussion* — Haze due to the existence of a collection of imperfections is a mass effect; individual imperfections of the type that result in haze cannot be readily distinguished by the eye or other optical detection system without magnification. In a scanning surface inspection system, haze results in a background signal; this signal and laser light-scattering events together comprise the signal due to light-scattering from a wafer surface.

5.55 *hole* — a mobile vacancy in the electronic valence structure of a semiconductor that acts like a positive electron charge with positive mass; the majority carrier in *p*-type material.

5.56 *indent* — an edge defect that extends from the front surface to the back surface of a silicon wafer.

5.57 *ingot* — a cylinder or rectangular solid of polycrystalline or single crystal silicon, generally of slightly irregular dimensions.

5.57.1 *Discussion* — Silicon wafers are usually sliced from cylindrical single-crystal ingots that have been ground to a uniform diameter prior to slicing.

5.58 *intrinsic, adj.* — (1) the region in the conductivity-temperature curve where the conduction in a wafer is dominated by hole-electron pairs excited across the forbidden energy gap; (2) a process, such as intrinsic gettering, caused by factors within the crystal of the wafer itself.

5.59 *laser light-scattering event* — a signal pulse that exceeds a preset threshold, generated by the interaction of a laser beam with a discrete scatterer at a wafer surface as sensed by a detector; see also *haze*.

5.59.1 *Discussion* — In a scanning surface inspection system, the background signal due to haze and laser light-scattering events together comprise the signal due to light-scattering from a wafer surface.

5.60 *lay* — the predominant direction of the surface texture.

5.60.1 *Discussion* — Although the texture of polished silicon wafers is generally isotropic, some epitaxial wafers exhibit a pattern of steps and ledges when examined by atomic force microscopy at near atomic resolution. Contoured wafer edges may also exhibit lay even after polishing.

5.61 *light point defect, LPD* — not preferred, use localized light-scatterer, LLS.

5.61.1 *Discussion* — To some, the term light point defect implies a defective part; hence, a search was undertaken for a more neutral term. Several were tried, and finally, despite some objection to the difficulty of saying the code, the term localized light scatterer was approved as a replacement. This term is general in nature and can refer to features detected both visual inspection and by automated inspection using a scanning surface inspection system.

5.62 *lineage* — a low-angle grain boundary resulting from an array of dislocations.

5.63 *localized light-scatterer, LLS* — an isolated feature, such as a particle or a pit, on or in a wafer surface, resulting in increased light-scattering intensity relative to that of the surrounding wafer surface; sometimes called light point defect.

5.63.1 *Discussion* — Localized light scatterers of sufficient size appear as points of light under high intensity optical illumination; these points of light can be observed visually, but the observation is a qualitative one. Localized light scatterers are observed by automated inspection techniques as laser-light scattering events. Automated inspection techniques are quantitative in the sense that scatterers with different scattering intensities can be segregated. The presence of LLS's does not necessarily decrease the utility of the wafer.

5.64 *lot* — for the purposes of commercial exchange of silicon wafers, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as above that have been identified by the supplier as constituting a lot.

5.65 *macroscratch* — a scratch that is visible to the unaided eye under either incandescent (high intensity) or fluorescent (diffuse) illumination.

5.65.1 *Discussion* — The number of macroscratches on a wafer is equal to the count of scratches seen under diffuse illumination.

5.66 *majority carrier* — type of charge carrier constituting more than one half the total charge-carrier concentration (e.g., holes in *p*-type material).

5.67 *maximum FPD* — the largest of the absolute values of the focal plane deviations.

5.68 *microroughness* — surface roughness components with spacing between irregularities (spatial wavelength) less than about 100 μm.

5.69 *microscratch* — a scratch that is not visible to the unaided eye under fluorescent (diffuse) illumination but is visible to the unaided eye under incandescent (high intensity) illumination.

5.69.1 *Discussion* — The number of microscratches on a wafer is the difference of the count of scratches seen under high intensity illumination and the count of scratches seen under diffuse illumination.

5.70 *Miller indices, of a crystallographic plane* — the smallest integers proportional to the reciprocals of the intercepts of the plane on the three crystal axes of unit length.

5.71 *minority carrier* — type of charge carrier constituting less than one half the total charge-carrier concentration (e.g., electrons in *p*-type material).

5.72 *mound* — on a semiconductor wafer surface, irregularly shaped projection with one or more irregularly developed facets.

5.73 *nanotopography* — the non-planar deviation of a wafer surface within a spatial wavelength range of approximately 0.2 mm to 20 mm.

5.74 *notch* — an intentionally fabricated indent of specified shape and dimensions on a silicon wafer oriented such that the diameter passing through the center of the notch is parallel with a specified low index crystal direction.

5.75 *orange peel* — large-featured, roughened type of wafer surface visible to the unaided eye.

5.76 *orientation*, *of a single crystal surface* — the crystallographic plane, described in terms of its Miller indices, with which the surface is ideally coincident.

5.76.1 *Discussion* — In semiconductor single crystals, where the surface of a wafer cut from the crystal usually corresponds closely (within a degree or several degrees) to a low index plane, such as a (100) or (111) plane, the surface orientation is frequently described in terms of the maximum angular deviation of the mechanically prepared surface from the low index crystallographic plane.

5.77 *orthogonal misorientation*—in wafers cut intentionally "off orientation," the angle between the projection of the vector normal to the wafer surface onto a {111} plane and the projection on that plane of the nearest <110> direction.

5.78 *particle* — a small, discrete piece of foreign material or silicon not connected crystallographically to the wafer.

5.78.1 *Discussion* — Particles may be pieces of solid material or condensate from liquids or gases. Particles are observed by automated inspection as laser light-scattering events, but they may also be observed visually under high intensity illumination as points of light or studied by other methods, including scanning electron microscopy. Particles on wafer surfaces can usually be removed by non-etching cleaning.

5.79 *pit* — a depression in a wafer surface where sloped sides of the depression meet the surface in a distinguishable manner in contrast to the sides of a dimple, which are rounded.

5.80 *point defect* — a localized crystal defect such as a lattice vacancy, interstitial atom, or substitutional impurity. Contrast with *light point defect*.

5.81 *preferential etch* — a selective etch that etches regions of different crystal strain or conductivity at different rates, used to delineate crystal defects or regions of differing conductivity on wafer surfaces.

5.82 *primary flat* — the flat of longest length on the wafer, oriented such that the chord is parallel with a specified low index crystal plane; sometimes called *major flat*.

5.83 *radial gradient* — not preferred; use *resistivity variation*.

5.84 *reference plane* — a plane defined by one of the following:

- three points at specified locations on the front or back surface of the wafer,
- the least squares fit to the front or median surface of the wafer using all points within the FQA,
- the least squares fit to the front surface of the wafer using all points within a site, or
- an ideal back surface (equivalent to the ideally flat chuck surface that contacts the wafer).

5.84.1 *Discussion* — For flatness measurement, the specified reference plane is chosen with due regard for the capabilities of the imaging system. Front surface or back surface reference planes should be selected depending on the wafer mounting system. If the wafer cannot be gimbaled in the imaging system, a back surface reference plane should be specified. For shape measurement, the reference plane to be used is spelled out in the applicable test method.

5.85 *reference plane deviation, RPD* — the distance perpendicular to the reference plane between the reference plane and the wafer surface being measured.

5.86 *resistivity, (electrical),* σ, [Ω·cm] — the measure of difficulty with which charged carriers flow through a material; the reciprocal of *conductivity*.

5.86.1 *Discussion* — the resistivity of a semiconductor or other material is the ratio of the potential gradient (electric field) parallel with the current to the current density.

5.87 *rms area microroughness,* R_{qA} — the root mean square of the topographic deviations of a surface $Z(x,y)$ from the mean surface taken within the (rectangular) evaluation area $A_e = L_x L_y$.

5.87.1 *Discussion* — The rms area microroughness is one of several statistical metrics that can be used to describe surface topography; definitions for other metrics and for such concepts as mean surface and evaluation area may be found in ANSI/ASME B46.1 and ISO 4287/1.

5.87.2 The function R_{qA} is related to a two-dimensional measurement of the surface profile as follows:

$$R_{qA} = \left[\frac{1}{A_e} \int_0^{L_x} \int_0^{L_y} Z(x,y)^2 \, dx dy \right]^{1/2} \tag{1}$$

The digital approximation of R_{qA} for a surface profile consisting of N by M data points equally spaced along the x and y directions, respectively, is:

$$R_{qA} = \left[\frac{1}{NM} \sum_{i=1}^{M} \sum_{j=1}^{N} Z_{ij}^2 \right]^{1/2} \tag{2}$$

5.87.3 Experimentally, the profile is always limited by the spatial bandwidth of the measurement. In the x direction, the profile length is L_x divided into N equally spaced points; the lower spatial frequency limit for f_x can never be less than $1/L_x$ and the upper spatial frequency limit can never be greater than the Nyquist limit, $N/2L_x$. Similarly, in the y direction, the profile length is L_y divided into M equally spaced points; the lower frequency limit for f_y can never be less than $1/L_y$ and the upper spatial frequency limit can never be greater than the Nyquist limit, $M/2L_y$. Practical limits to the spatial bandwidth are governed by considerations similar to those for the one-dimensional case (see ¶5.88.4).

5.87.4 R_{qA} can also be estimated by integrating the two-dimensional power spectral density (PSD) function, $PSD(f_x, f_y)$, over the spatial frequency range between spatial frequencies that lie within the bandwidth of the measurement:

$$R_{qA} = \left[\int_{f_{x1}}^{f_{x2}} \int_{f_{y1}}^{f_{y2}} PSD_A(f_x, f_y) \mathrm{d}f_x \mathrm{d}f_y \right]^{1/2} \tag{3}$$

5.87.5 If the surface is assumed to be isotropic and the instrument response function is neglected, the rms microroughness over the spatial frequency range between f_1 and f_2 can also be obtained by integrating the isotropic PSD function:

$$R_{qA} = \left[\int_{f_1}^{f_2} PSD_{iso}(f) \mathrm{d}f \right]^{1/2} \tag{4}$$

where:

$$PSD_{iso}(f) = \int_0^{2\pi} PSD_A(f_x, f_y) f \, \mathrm{d}\beta$$

$$= 2\pi f PSD_A(f_x, f_y), \text{ and}$$

$$f = (f_x^2 + f_y^2)^{1/2}$$

5.88 *rms microroughness, R_q* — the root mean square of the surface profile height deviations $Z(x)$ from the mean line taken within the evaluation length L.

5.88.1 *Discussion* — R_q is one of several statistical metrics that can be used to describe a surface profile; definitions for other metrics and for such concepts as mean line, evaluation length, and power spectral density function, may be found in ANSI/ASME B46.1 and ISO 4287/1.

5.88.2 The function R_q is related to a one-dimensional measurement of the surface profile as follows:

$$R_q = \left[\frac{1}{L} \int_0^L Z(x)^2 \mathrm{d}x \right]^{1/2} \tag{5}$$

5.88.3 The digital approximation of R_q for a profile consisting of N equally spaced points is:

$$R_q = \left[\frac{1}{N} \sum_{i=1}^{N} Z_i^2 \right]^{1/2} \tag{6}$$

5.88.4 Experimentally, the profile is always limited by the spatial bandwidth of the measurement. For a profile of length L, consisting of N equally spaced points, the lower spatial frequency limit f_1 can never be less than $1/L$ and the upper spatial frequency limit f_2 can never be greater than the Nyquist limit, $N/2L$. In practical cases, $f_1 \approx 2/L$; the achievable value of f_2 depends on instrumental parameters.

5.88.5 R_q can also be estimated by integrating the one-dimensional power spectral density (PSD) function, *PSD(f)*, over the spatial frequency range between two spatial frequencies, f_1 and f_2, that lie within the bandwidth of the measurement:

$$R_q = \left[\int_{f_1}^{f_2} PSD(f) \mathrm{d}f \right]^{1/2} \tag{7}$$

5.88.6 In all cases, R_q must be reported together with the lower and upper limits, f_1 and f_2, respectively, of the spatial frequency bandwidth over which it has been determined. Alternatively, the spatial bandwidth may be expressed in terms of the upper and lower spatial wavelengths, λ_2 (= $1/f_2$) and λ_1 (= $1/f_1$), respectively.

5.89 *roughness* — the more narrowly spaced components of surface texture.

5.89.1 *Discussion* —These components are considered within defined limits of spatial wavelength (or frequency).

5.90 *scan direction* — the direction of successive subsites in a scanner site flatness calculation.

5.90.1 *Discussion* — The scanner site flatness value obtained for a site may depend on scan direction.

5.91 *scanner site flatness* — the maximum subsite TIR or the maximum subsite FPD, of a site.

5.91.1 *Discussion* — The subsite TIR is the TIR of the portion of the subsite that falls within the FQA and within the site; the subsite FPD is the maximum FPD of the portion of the subsite that falls within the FQA and within the site. The reference plane is calculated using all points within the subsite that fall within the FQA.

5.91.2 Precise scanner site flatness measurement requires measurement points located closely enough to reveal the surface topography in detail. It is recommended that the scanner site flatness be measured using a data point array with adjacent points separated by 1 mm or less.

5.92 *scratch* — a shallow groove or cut below the established plane of the surface of a semiconductor wafer, with a length to width ratio greater than 5:1.

5.93 *secondary flat* — a flat of length shorter than the primary orientation flat, whose position with respect to the primary orientation flat identifies the type and orientation of the wafer.

5.94 *shallow etch pits* — etch pits that are small and shallow in depth under high magnification, > 200×. Also known as *saucer pits* (see also *haze*).

5.95 *shape* — for wafer surfaces, the deviation of a specified wafer surface relative to a specified reference plane when the wafer is in an unclamped condition, expressed as the range or total indicator reading (TIR) or as the maximum reference plane deviation (maximum RPD) within the specified fixed quality area.

5.95.1 *Discussion* — This definition is analogous to the definition of flatness, which applies to the front surface geometry when the wafer is in the clamped condition.

5.96 *site* — a rectangular area, on the front surface of a wafer, whose sides are parallel and perpendicular to the primary orientation flat or to the notch bisector, and whose center falls within the FQA.

5.97 *site array* — a set of contiguous sites.

5.98 *site flatness* — the TIR or the maximum FPD of the portion of a site that falls within the FQA.

5.98.1 *Discussion* — Precise site flatness measurement requires measurement points located closely enough to reveal the surface topology in detail. It is recommended that site flatness be measured using a data point array with adjacent points separated by 2 mm or less. It is also recommended that the data set used to calculate site flatness have data at each site corner and along each site boundary. This makes the effective site measurement area equal to the site size.

5.99 *slip* — a process of plastic deformation in which one part of a crystal undergoes a shear displacement relative to another in a fashion that preserves the crystallinity of the material.

5.99.1 *Discussion* — After preferential etching, slip lines are evidenced by a pattern of one or more parallel straight lines of dislocation etch pits that do not necessarily touch each other. On {111} surfaces, groups of lines are inclined at 60° to each other; on {100} surfaces, they are inclined at 90° to each other.

5.100 *sori* — the difference between the maximum positive and maximum negative deviations of the front surface of a wafer that is not chucked from a reference plane that is a least-squares fit to the front surface.

5.101 *stain* — area contamination that is chemical in nature and cannot be removed except through further lapping or polishing.

5.101.1 *Discussion* — Included in this category are “white” stains that are seen after chemical etching as white or brown streaks. Not included in this category are non-removable artifacts not caused by contaminants; such artifacts are frequently localized differences in surface texture.

5.102 *subsite, of a site* — a rectangular area, $L_{ss} \times W_{ss}$, on the front surface of a wafer, associated with a particular site. The center of the subsite must be within the site. Some part of the subsite must be within or on the FQA boundary. A subsite corresponds to the instantaneous area exposed by a scanning stepper.

5.103 *surface texture* — the topographic deviations of a real surface from a reference surface.

5.103.1 *Discussion* — Surface texture includes roughness, waviness, and lay.

5.104 *swirl* — helical or concentric features that are visible to the unaided eye after preferential etch, and appear to be discontinuous under 100× magnification.

5.105 *terracing* — a network of contours that are associated with pyramid-like defects on epitaxially deposited surfaces and are related to the orientation of the surface.

5.106 *thermal emf* — the net emf set up in a thermocouple under conditions of zero current. Also known as *Seebeck emf*.

5.107 *thickness, of a semiconductor wafer* — the distance through the wafer between corresponding points on the front and back surfaces.

5.108 *thickness, of an epitaxial layer* — the distance from the surface of a wafer to the layer-substrate interface.

5.109 *tolerance* — the allowable range of a specification parameter on either side of the nominal or target value.

5.110 *total indicator reading, TIR* — the smallest perpendicular distance between two planes, both parallel with the reference plane, that encloses all points on the front surface of a wafer within the FQA, the site, or the subsite, depending on which is specified.

5.111 *total thickness variation, TTV* — the difference between the maximum and minimum values of the thickness of a wafer.

5.111.1 *Discussion* — Initially, the TTV was determined by measurement at a small number of points, generally five or nine, but modern measurement equipment samples the wafer at relatively small intervals over its entire extent.

5.112 *twin boundary* — a coherent planar interface that separates two parts of a crystal lattice that are related to each other in orientation as mirror images.

5.113 *warp, of a semiconductor wafer* — the difference between the maximum and minimum distances of the median surface of a free, unclamped wafer from a reference plane.

5.114 *waviness* — the more widely spaced component of surface texture.

5.114.1 *Discussion* — Waviness may be caused by such factors as machine or work piece deflections, vibration, and chatter. Roughness may be considered as superimposed on a wavy surface

6 Symbols

6.1 *English Alphabetical Symbols*

6.1.1 *r* — radial dimension of wafer coordinate system with origin at the wafer center.

6.1.1.1 *Discussion* — Note that the radial dimension associated with the edge profile template in SEMI M1 is called *x* and that this dimension is positive away from the actual edge of the wafer.

6.1.2 *t* — wafer thickness.

6.1.2.1 *Discussion* — The wafer thickness is sometimes indicated with a capital *T*, but this usage is to be discouraged because *T* also stands for temperature.

6.1.3 *x* — direction of the wafer coordinate system along the diameter perpendicular to the bisector of the primary fiducial with origin at the center and positive direction to the right when the top surface is up and the primary fiducial is toward the operator.

NOTE 2: See also ¶6.1.1.1.

6.1.4 *y* — direction of the wafer coordinate system along the diameter that is the bisector of the primary fiducial with origin at the center and positive direction to the top (away from the fiducial) when the top surface is up and the primary fiducial is toward the operator.

6.1.4.1 *Discussion* — Note that the *y*-direction associated with the edge profile template in SEMI M1 is in the vertical direction through the wafer and that this dimension is positive away from the actual surface of the wafer.

6.1.5 *z* — direction of the wafer coordinate system through the bulk of wafer with the positive direction upwards when the top surface is up.

NOTE 3: See also ¶6.1.4.1.

6.2 *Greek letters*

6.2.1 Δ — delta, difference.

6.2.2 θ — angular direction in a counter clockwise direction from the diameter perpendicular to the bisector of the primary fiducial in the wafer coordinate system.

6.2.3 μ — micro, one millionth, usually associated with meters (m) or seconds (s).

6.2.4 μ — carrier mobility as of an electron or hole in a semiconductor.

6.2.5 ρ — resistivity.

6.2.6 σ — conductivity.

6.2.7 Ω — ohm, the unit of resistance, combined with a linear dimension, usually centimeter, to be the unit of resistivity.

6.3 *Mathematical symbol*

6.3.1 × — multiplication sign, also sometimes indicated by a center dot (·) especially when separating various units in a group of units such as Ω·cm.

SEMI M60-0305
TEST METHOD FOR TIME DEPENDENT DIELECTRIC BREAKDOWN CHARACTERISTICS OF SiO2 FILMS FOR Si WAFER EVALUATION

This test method was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the Japanese Silicon Wafer Committee. Current edition approved by the Japanese Regional Standards Committee on January 11, 2005. Initially available at www.semi.org January 2005; to be published March 2005.

1 Purpose

1.1 The technique outlined in this test method is for the purpose of standardizing silicon wafer characterization by GOI (Gate Oxide Integrity). For more detailed discussion of the general characterizing methods for this test, the reader is referred to §3. TZDB technique as SEMI M51 is advantageous to estimate failure rate by intrinsic breakdown as the C mode and an accidental breakdown as the B mode. However, this test method has a higher sensitivity for detecting the accidental breakdown mode than TZDB.

2 Scope

2.1 This test method is for the purpose of the characterization method of silicon wafer by GOI. This characterization method is outlined below

2.1.1 *MOS (Metal Oxide Semiconductor) — capacitor fabrication* — A gate oxide film is thermally grown on a silicon wafer surface. Then, poly-Si electrodes are formed on the gate oxide film. Other metals, other than poly-silicon electrode materials, can be used, however, it shall be desirable to use an electrode that has been confirmed to have sufficiently good characteristics for application as a gate electrode as described below.

2.1.2 *Electrical Characterization Evaluation* — The TDDB (Time Dependent Dielectric Breakdown) characteristics of the MOS capacitors are measured. The presence of COPs (Crystal Originated Particles) at the surface of the polished Si substrates influences the TDDB characteristics of the gate oxide. That is, the silicon wafer is evaluated in terms of the TDDB characteristics of the gate oxide. The test method outlined in this test method is for the purpose of standardizing the procedure of MOS fabrication, measurement, analyses, and the report of the GOI data to interested parties. This test method is based on the results of round robin among the silicon wafer manufacturers. In general, GOI strongly depends on crystal defects, contaminations and particles on/near wafer surface. GOI also depends on the fabrication environment. The cleanliness of the process environment in which the MOS capacitors are fabricated shall be evaluated to be acceptable (see ¶5.3).

2.2 The target of this test method is to characterize silicon wafers, that is, evaluate COPs near the silicon wafer surface. The proper gate oxide thickness of the MOS samples is 20–25 nm. A discussion on gate oxide thickness is given in a later section. Oxygen precipitates are also one of the gate oxide defect origins, however, this is beyond the scope of this test method because the as-received wafers contain only a small amount of oxygen precipitates. Near-surface quality can be evaluated in this test. In this case, it is assumed that an oxide film thickness of approximately 10 nm is used. It is more difficult to categorize the accidental and intrinsic breakdowns in TZDB, as the gate oxide thickness becomes thinner. Therefore mode classification in TDDB is more effective.

2.3 For detailed discussion on sample structures used in this test method, the reader shall refer to EIA/JEDEC Standard 35-1. In general, the most likely sample structures are a simple planar MOS (Metal Oxide Semiconductor) capacitor structure, various isolation structures (for example, LOCOS (LOCal Oxidation of Silicon), STI (Shallow Trench Isolation)), and FET (Field-Effect Transistor) structures. For the purpose of silicon wafer characterization, the simple planar MOS capacitor structure is the most desirable. In the case of the various isolation and FET structures, the silicon wafer receives thermal treatments several times in the complicated sample fabrication process. Therefore, in this case it is questionable whether the characteristics of the starting Si wafer are reflected in this test measurement results.

2.4 In this evaluation method, a constant current stress is applied to the gate oxide and time to breakdown is measured. The amount of charge injected until dielectric breakdown (Q_{bd}) is also calculated. (Constant-current TDDB: detail of measurement condition is described in a later section). The dielectric breakdown by the COPs and other defects can be evaluated from the accumulated failure distribution of Q_{bd}. In addition, a constant-voltage

TDDB method can be used as an evaluation of gate oxide lifetime. In this test method, the constant-current TDDB method is chosen, because the constant current TDDB method has less influence on parasitic resistance in a measurement circuit than the constant-voltage TDDB method.

2.5 This test method gives instructions for the procedure for characterizing mirror-polished, p-type CZ silicon wafers. Gate electrodes were negatively biased so that the silicon surface is in accumulation. Stress current shall be sufficient for the gate oxide to be broken down within a finite measurement time. In addition, it is desirable to have an applied current density J within 0.01 and 0.1A/cm^2.

2.6 The stress gate current has to be reversed for the n-type silicon wafer.

2.7 The poly-silicon film is used as gate electrode of measured MOS capacitors. The poly-silicon film can make standard test results applicable to the testing of wafers used to fabricate integrated circuits rather than other metal electrodes because poly-silicon electrodes are commonly used in actual devices. However, a gate electrode other than poly-silicon gate electrode shall be studied for applications in advanced ultralarge-scale integrated circuits. In this case, the new electrode material shall have the same detection sensitivity to silicon wafer defects as poly-silicon electrode.

NOTICE: This test method does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this test method to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

NOTE 1: When there is no special direction, all the quoted documents are the newest editions.

NOTE 2: When a material other than poly-silicon is used for electrodes, refer to the standard suitable for individual process.

3.1 *SEMI Standards*

SEMI C3.6 — Standard for Phosphine (PH_3) in Cylinders, 99.98% Quality

SEMI C3.54 — Gas Purity Guideline for Silane (SiH_4)

SEMI C21 — Specifications and Guideline for Ammonium Hydroxide

SEMI C27 — Specifications and Guidelines for Hydrochloric Acid

SEMI C28 — Specifications and Guidelines for Hydrochloric Acid

SEMI C30 — Specifications and Guidelines for Hydrogen Peroxide

SEMI C35 — Specifications and Guideline for Nitric Acid

SEMI C38 — Guideline for Phosphorus Oxychloride

SEMI C41 — Specifications and Guidelines for 2-Propanol

SEMI C44 — Specifications and Guidelines for Sulfuric Acid

SEMI C54 — Specifications and Guidelines for Oxygen

SEMI C59 — Specifications and Guidelines for Nitrogen

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M51 — Test Method For Characterizing Silicon Wafers by Gate Oxide Integrity.

SEMI MF1241 — Terminology of Silicon Technology (Reapprpved2000)

SEMI MF1771 — Standard Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique

3.2 *ASTM Standards*[1]

ASTM D5127 — Standard Guide for Ultra Pure Water Used in the Electronics and Semiconductor for Industry.

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555 Website: www.astm.org

3.3 *EIA/JEDEC Standards*[2, 3]

EIA/JEDEC 35 — Procedure for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-1 — General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics

EIA/JEDEC 35-2 — Test Criteria for the Wafer-Level Testing of Thin Dielectric

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Abbreviations & Acronyms*

4.1.1 *COP* — Crystal Originated Particles

4.1.2 *GOI* — Gate Oxide Integrity

4.1.3 *LOCOS* — Local Oxidation of Silicon

4.1.4 *MOS* — Metal Oxide Semiconductor

4.1.5 *STI* — Shallow Trench Isolation

4.1.6 *TZDB* — Time Zero Dielectric Breakdown

4.2 *Definitions*

4.2.1 Many terms relating to silicon technology are defined in SEMI MF1241.

4.2.2 Definitions for some additional terms are given in SEMI M1 and SEMI MF1771.

4.2.3 Other terms are defined as follows:

4.2.3.1 *Crystal Originated Particles*[4] *(COP)* — This is the one of grown-in defects in the CZ Si wafers with an octahedral structure. This was found as particles appeared on the silicon surface by repetition SC-1[5] of RCA cleaning.

4.2.3.1.1 *Discussion* — It has been thought that the COP is one of the main origins of the GOI. The gate oxide formed on the Si surface at which the COP appears easily breaks down at the corner of the octahedral shape like at a Si trench corner[6,7,8]. This corner of octahedral structures is thinning the oxide films. The oxide electric field enhances at that place. The breakdown electric field is decreased.

4.2.3.2 *Failure Modes* — The TDDB Weibull plot[9, 10] is classified to three modes. A typical plot is shown in Figure 1.

Accidental failure — A-A mode
Accidental failure — A-B mode
Wearout breakdown — W mode

2 Electronic Industries Alliance, EIA Engineering Department, Standards Sales Office, 2001 Eye Street, NW, Washington, D.C. 20006, USA. Website: www.eia.org

3 Joint Electron Device Engineering Council, 2500 Wilson Blvd., Arlington, VA 22201, website: www.jedec.org

4 J. Ryuta, E. Morita, T. Tanaka and Y. Shimanuki, "Crystal – Originated Singularities on Si Wafer Surface after SC1 Cleaning", *Jpn. J. Appl. Phys*. 29(1990) L947.

5 W. Kern and D. Puotinen, "Clean Solution Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology", *RCA Rev*., 31, 187(1970).

6 T. Mera, J. Jablonski, K. Nagai, and M. Watanabe, "Grown-in defects in silicon crystals responsible for gate oxide integrity deterioration", *Ohyo-Buturi*, 66(7), 728 (1997).

7 K.Yamabe and K.Imai,"Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation", IEEE Trans. Electron Devices, ED–34, 1681(1987).

8 K.Yamabe, Y.Shimada, M.Piao, T.Yamazaki, T.Otsuki, R.Takeda, Y.Ohta, S.Jimbo, and M.Watanabe, "Effect of SiO_2 Thickness on Dielectric Breakdown Defect Density Due to Surface Crystal–Originated Particles", J.Electrochem.Soc., 150, F42(2003).

9 D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Dielectric Breakdown", Proc. *Int. Reliability Physics Symposium*, 1979, p.1.

10 E. S. Anolick and G. R. Nelson, "Low Field Time Dependent Dielectric Integrity", Proc. *Int. Reliability Physics Symposium*, 1978, p.8.

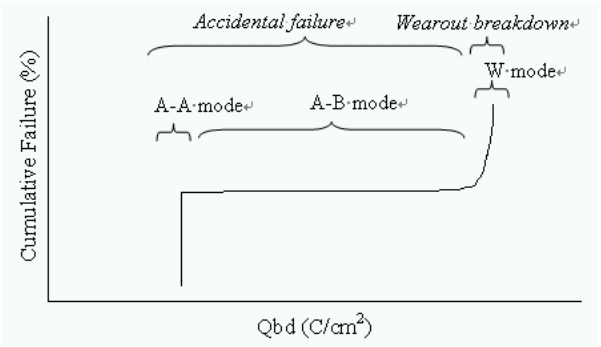


Figure 1
Classification in Weibull plot of TDDB result.

4.2.3.2.1 Discussion on failure modes:

- *A-A Mode*: Initial breakdown failure
  - This failure is caused by defects generated during gate oxide formation process such as pinholes and also by crystal defects such as COPs. This failure corresponds to the A mode and partly B mode failures of TZDB.
- *A-B Mode*: Intermediate breakdown failure
  - This failure is caused by extrinsic defects which are not serious enough to cause the A-A mode. This failure corresponds to the B mode and partly C mode failure of TZDB.
- *W Mode*: Wearout breakdown
  - This breakdown is also called intrinsic breakdown or fatigue breakdown, and relates to the intrinsic lifetime of oxide films. The measurement of this breakdown shall be performed carefully because the result depends on measurement conditions.
  - Response rapidity of the measurement system has a great influence on A-A mode detection. The total number of A-A and A-B mode failures is related to the crystal quality of the mirror-polished CZ Si wafers.

4.2.3.3 *Categorization of Breakdown Modes* — boundaries of A-A/A-B modes and A-B/W modes shall be defined in advance.

4.2.3.3.1 *A-A/A-B Mode Boundary*

- The detectable minimum Q_{bd} values depend on the stress current and response speed of the measurement systems. As stress current density increases, the charge density of the A-A/A-B mode boundary may also increases. This effect shall be considered when defining the A-A/A-B mode boundary. Based on these round robin results, the charge density range from 0.0001C/cm^2 to 0.01 C/cm^2 is recommended as the A-A/A-B mode boundary.

4.2.3.3.2 *A-B/W mode boundary*

- The A-B/W mode boundary is defined in terms of Weibull plots as shown in Figure RI-3. Ideally, it shall be determined by the intercept point of two approximation lines in the A-B and W mode ranges. If the boundary charge density is too low ($Q < 1$ C/cm^2), one part of the A-B mode breakdown can be counted as the W mode. Otherwise, if the boundary charge density is too high ($Q > 4$ C/cm^2), one part of the W mode breakdown can be counted as the A-B mode.
- In both cases, we have errors in the classification of the failure mode categories, even if the measurement is accurately carried out and appropriate Weibull plots are obtained. So, the results of this round robin indicate that the charge density of 2 C/cm^2 is recommended as the A-B/W mode boundary. To measure the failure rates at the boundary charge density of the A-B/W modes, all samples are not necessarily broken down. If the determination procedure of the boundary charge density is clear, the application of a predetermined charge

density will give us the approximate failure rate by the A-B mode breakdown. It is necessary to determine the classification of failure modes in advance. This is because reliabilities depend on the devices fabricated on the Si wafer (electrode material, gate oxide thickness, operating voltage, etc.). Refer to an example of mode classification described in Figure RI-2.

4.2.3.4 *Time Zero Dielectric Breakdown (TZDB)* — one of the dielectric breakdown characteristic of the gate oxide.

4.2.3.4.1 *Discussion* — To measure TZDB, oxide leakage current is monitored with an electric field applied to the MOS capacitor stepwise from 0 to 15MV/cm (for example in the case of a 25 nm-thick oxide, actual applied voltage would be from 0 to 37.5V). The electrode is negatively biased so that the Si surface is in accumulation and the electric field is applied effectively. Applied electric field (or voltage) is measured when the oxide leakage current reaches a predetermined value (judgment current), in other words when the gate oxide breaks down. The influence of COPs on gate oxide breakdown can be estimated from the distribution of breakdown electric field.

5 Summary of Method

5.1 *Overview* — This test method consists of two parts. The first one is the fabrication of a number of similar MOS capacitors on silicon wafers, and the second one is the measurement of the electric charge injected just before the dielectric breakdown of the MOS capacitors. To measure the injected electric charge, the voltage applied to a MOS capacitor is controlled so that the current is kept constant. The voltage is monitored throughout the test, and the time from the beginning to a sudden voltage drop which results from the dielectric breakdown of the silicon dioxide film is measured. The injected electric charge is the product of the measured time and the gate current density.

5.2 *MOS Capacitor Fabrication Process* — Many MOS capacitors are formed on the test wafer. The MOS fabrication process consists of wafer cleaning, thermal oxidation, poly-Si deposition, phosphorous doping, activation heat treatment, photolithography and etching, in the case of using poly-Si electrodes. The details of the MOS capacitor fabrication process are shown in SEMI M51. When materials other than poly-silicon are used for electrodes, the process shall be adjusted to the material used. Although thermally grown 20–25 nm-thick gate oxide films are recommended in SEMI M51, oxide films as thin as 10 nm can be used depending on the situation. However, measurement shall be performed carefully for oxide films thinner than 3 nm, because breakdown judgment becomes difficult under the influence of direct tunneling current. See SEMI C3.6, SEMI C3.54, SEMI C21, SEMI C27, SEMI C28, SEMI C30, SEMI C35, SEMI C38, SEMI C41, SEMI C44, SEMI C54, SEMI C59.

5.3 *Fabrication Environment* — It is necessary to fabricate MOS capacitors in a clean room environment of 1000 or better class in total quality. That is, it needs to be confirmed that the A mode failure rate is 10% or less by TZDB evaluation. The A mode failure depends not only on the particle of work environment atmosphere but also on the ultrapure water, fixtures, process apparatus, clean clothes, operation rules etc. Heavily contamination such as alkaline or heavy metal has an important negative effect on the GOI of the oxide.

5.4 *Measurement of Electric Characteristic of MOS Capacitors*

5.4.1 The dielectric breakdown defect density of the silicon oxide film is evaluated by constant current TDDB measurement of the MOS capacitors. The evaluation consists of the measurement of charge injected before the dielectric breakdown of the MOS capacitors. To measure the injected charge, voltage applied to a MOS capacitor is controlled so that the current is kept constant. The applied voltage is monitored throughout the test, and the time to sudden voltage drop which results from dielectric breakdown of the silicon dioxide film is measured. The amount of the injected charge is the product of the measured time and gate current density. The defect density of the oxide film is evaluated from the Weibull plot (cumulative failure rate) of the dielectric breakdown data of approximately 100 MOS capacitors.

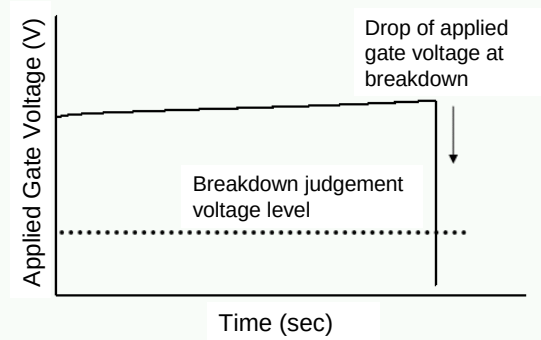
5.4.2 *Stress Current Density* — For reliable measurement, a voltage/current source with a stable output wave shape shall be used. It is necessary to stabilize the output as much as possible. In the constant current TDDB measurement, a constant current is continuously applied, and voltage is monitored. The dielectric breakdown is judged by a sudden drop in the voltage monitored. If the applied stress current density is too low, the time to breakdown will be too long to be realistic. Contrarily, too a high current density is also unsuitable because the voltage drop in the oxide breakdown instant becomes small. Considering these factors, the recommended stress current density range is from 0.01 to 0.1A/cm^2.

5.5 *Measurement Temperature* — Besides current density, the measurement temperature is also an important parameter which determines measurement time. It is appropriate to measure in the temperature range of room temperature to 150ºC, taking into consideration the temperature tolerance of the measurement equipment. In addition, there are cases that since silicon wafer, stage chuck, probe, and so on, expand at a high temperature, the probe deviates from the predetermined position, thus consideration is required when selecting probing machines.

5.6 *Breakdown Judgment* — To measure the dielectric breakdown lifetime of an oxide film, the voltage applied to a MOS capacitor is controlled so that a current is kept constant. The applied voltage is monitored throughout the test. The dielectric breakdown of the oxide is judged by sudden voltage drop. In practice, at the dielectric breakdown the applied voltage becomes lower than the criterion voltage defined before. The dielectric breakdown lifetime is the stress application time till breakdown. If the criterion voltage is too low, it can easily affected by noise. In contrast, the chance of missing breakdown events is increased if the criterion voltage is too high. The changes in two continuous measured gate voltages can be used to judge the oxide breakdown. The instant at which the voltage change became larger than the criterion value is defined as dielectric breakdown. The same caution mentioned above is also required in this case. In this round robin, the current density is from 0.01 to 0.1A/cm^2, the sheet resistance of the poly-silicon electrode is approximately 50 ohm/sq, gate electrode area is from 1mm^2 to 10mm^2, gate oxide thickness is 25nm and measurement temperature is from room temperature to 150ºC. In this case dielectric breakdown is determined from the changes in two continuous measured gate voltages. For example, the change in gate voltage is larger than $X_{criterion}$(%) of the former gate voltage value. $X_{criterion}$ is higher than 10%. Alternatively, dielectric breakdown is determined with the measured electric field, E_{ox}. It is considered that dielectric breakdown does not happen until E_{ox} becomes $E_{criterion}$ or lower. $E_{criterion}$ is higher than 4MV/cm. Stable measurement results are obtained in both cases. Of course, these criterion electric fields depend on gate oxide thickness, sheet resistance and area of gate electrode, stress current, stress temperature, and so on. To detect the dielectric breakdown with the change in gate voltage as shown in Figure 2, it is desirable to determine the criterion under each condition in advance.

5.7 *Estimation of Accidental Failure Rate* — As mentioned before, the total number of A-A and A-B mode failures is related to the crystal quality of the mirror polished CZ Si wafers. It takes a long time to measure the wearout lifetime of all the MOS capacitors. If a requirement is only measurement of the accidental failure rates of the MOS capacitors on silicon wafer surface, TDDB measurement can be finished without detecting the wearout lifetimes. That is, maximum stress time, T_{max}, is determined to be Q_{bd} in the A-B mode range in advance. The cumulative failure rate at T_{max} is the total failure rate of the A-A and A-B modes. If the rough shapes of the Weibull plots of the TDDB measurement can be predicted in advance, T_{max} shall be determined as to be the maximum Q_{bd} in the relatively flat range of the A-B mode. This reason is that variation of T_{max} has little influence on the evaluation of total accidental failure rates. This method has an advantage of that the failure rate of the A-A and A-B modes is evaluated very quickly.

5.8 *Constant-Voltage TDDB* — The constant-voltage TDDB method is also used for a lifetime test. Measurement conditions shall be optimized for each purpose. For TDDB, an average electric field of approximately 10MV/cm is required. Therefore, the effective electric field applied to an oxide film is influenced by a series resistance. Thus, the constant current TDDB is more suitable.



NOTE: A typical applied gate voltage as a function of stress time and a relationship between a drop of the applied gate voltage at dielectric break-down and breakdown judgment voltage level.

Figure 2

6 Significance and Use

6.1 This standard gives the procedure for characterizing mirror-polished, p-type CZ silicon wafers using the dielectric breakdown defect densities of the gate oxide thermally grown on them. The MOS capacitors shall be formed in accordance with the fabrication processes described in §5 and SEMI M51. This reason is because the oxide characteristics depend on the fabrication processes. If MOS capacitors would be formed with different fabrication processes, it is desirable to confirm that these GOI results are similar to those of the MOS capacitors formed by the fabrication processes described above. Particularly, the electrode material of the MOS capacitors has a great influence on the dielectric breakdown of the gate oxide. Poly-silicon is specified as the electrode material in this standard. The test with the poly-silicon gate electrode gives us the test results directly applicable to the wafers for the integrated circuits rather than other metal electrodes, because poly-silicon electrodes are commonly used in actual devices. Of course other materials are also available for electrodes. Where other electrode material is used, an appropriate method for each case and the correlation data between poly-silicon and the other material shall be prepared.

6.2 It is well known that both the silicon surface morphology and the cross-sectional structure at the pattern edge of the active region of the MOS devices influence the dielectric breakdown of the gate oxide. Various types of contaminants also influence the dielectric breakdown of the gate oxide. The extent of contamination by alkaline metals, heavy metals or organic particles increases, as the sample fabrication process progresses.

6.2.1 The electrode area and total number of MOS capacitors shall be chosen to be suitable for the purpose of the test. The suitable gate area for the constant current TDDB measurement depends on the applied stress (i.e. induced current). If the gate electrode area is too large, parasitic resistance of the gate electrode disturbs uniform application of stress current to gate oxide. That is, too a high current density leads to nonuniform stress on gate oxide. As a result, the reliability of the measurement is reduced. The gate oxide with a defect density is able to be evaluated using two sets of MOS capacitors. Although the gate area and total number of MOS capacitors have the same product, one set consists of many capacitors with a small gate area and the other set consists of a few of capacitors with a large gate area. The TDDB evaluations using the former are more desirable than those using the latter. In this round robin, where a polycrystalline silicon thickness is 300 nm, sheet resistance is 50Ω/□ and gate area is smaller than 5 mm^2, reasonable TDDB results were obtained.

7 Interferences

7.1 Since this is a DC measurement, care must be taken to make sure that the silicon wafer has a low-resistance ohmic contact. There must be no dielectric film on the back surface, e.g., silicon oxide, in order to effectively apply a voltage bias to the gate oxide. It is not necessary for this to be carried out with a metallic contact on the back surface of the wafer under test. However, when the vacuum chucking is weak, care must be taken because of the possibility that the dielectric breakdown of the gate oxide is not accurately judged due to an increase in parasitic resistance. It is strongly suggested that testing be carried out with a current polarity such that the silicon surface will be in accumulation below the gate oxide, that is, negative voltages for *p*-type silicon wafers. If the polarity of the voltage is chosen to be in the reverse direction, the breakdown voltage may not be accurately measured due to the presence of a depletion layer below the gate oxide. Controls of electrical noise in this test method are crucial to the

proper identification of the failure criteria. It is possible that rapid voltage changes at the dielectric breakdown of the gate oxide cause electrical noise. There is a possibility that this noise leads to misjudgments of the oxide breakdown. So it is desirable to confirm that oxide breakdown occurred. For example after the TDDB measurement has been completed, the samples are measured to confirm their insulation. Mechanical stress due to the exploring probe can influence the measurement results, because the exploring probe is in contact with the gate electrode directly on the gate oxide. The actual results obtained depend somewhat on the sample fabrication process. Care must be taken to ensure consistent processing. Wafer temperature during testing shall be clearly defined. Large temperature variations might have an impact on results.

7.1.1 *Precaution* — Since the voltages and currents involved are potentially dangerous, appropriate means of preventing the operator from coming into contact with the exploring probe or other charge surfaces shall be in place before testing. This standard does not include any clauses relating to the safety and sanitation of the environment. Those who intend to implement this standard shall consider appropriate means to prevent any accidents or disasters, as well as taking responsibility for maintaining a state of safety, health and hygiene for users.

8 Sampling

8.1 Sampling is the responsibility of the user of this test method. However, if testing is carried out as part of a comparison or a correlation, all participants shall agree upon sampling in advance.

NOTE 3: Refer to the appendix of JEDEC standard No.35 for good discussion of sampling plan statistics.

9 Apparatus

9.1 SEMI M51 and SEMI M1771 shall be applied for measurement equipment such as current/voltage source units and manual probing machines

10 Procedure

10.1 *Fabrication of MOS Capacitors*

10.1.1 Refer to SEMI M51, introducing poly-silicon as an electrode material. Where another electrode material is used, an appropriate method for each case and the correlation data between poly-silicon and the other material shall be prepared.

10.2 *Measurement*

10.2.1 Before measurement, record the following information for each sample: date, time, operator, sample ID, oxide thickness, gate area, gate material, oxidation condition, conductivity type (p or n), equipment ID, and comments.

10.2.2 Decide on measurement parameters and record them. Constant current is applied in this test method. The parameters include stress current density (J), measurement interval (T_{int}), maximum stress time (T_{max}), gate area (S), judgment voltage of breakdown (V_{bd}), measurement temperature, the number of capacitors to be measured and a map of the capacitors.

10.2.3 Set a tungsten exploring probe at the starting position.

10.2.4 Set the exploring probe on a new MOS capacitor at the next position.

10.2.5 Set the accumulated time to zero (T (0) = 0). Record the oxide leakage current and the voltage.

10.2.6 Set the stress current to the designated point. Monitor the time (t) and the voltage (V_t) from the start.

10.2.7 If the applied time is equal to or greater than the maximum stress time($t \geq T_{max}$), record the maximum stress time (T_{max}) as the breakdown time (T_{bd}) along with the MOS address, and proceed to ¶10.2.8. If t is less than T_{max}, proceed to the next step.

10.2.8 Check to see if the voltage Vt has reached the judgment voltage of breakdown (V_{bd}). If so, record the time (t), along with each MOS address, as the breakdown time (T_{bd}), stop applying the stress current, and proceed to ¶10.2.9. If not, repeat from ¶10.2.6.

10.2.9 Check to see if there are any more MOS capacitors to be measured. If so, repeat from ¶10.2.4 until all MOS capacitors have been tested. A contact probe for all measuring points eliminates the need for repeat of the measurement, and proceeds to the next wafer.

10.2.10 Report the results.

10.2.11 Figure 3 shows a flow diagram outlining the procedure for this test method.

10.2.12 For the judgment method of breakdown, not only fixed V_{bd} but variation in voltage (ΔV) monitored could be used.

10.2.13 Figure 4 shows a flow diagram outlining the procedure for the test method when the judgment of breakdown by drop in voltage (ΔV) is adopted.

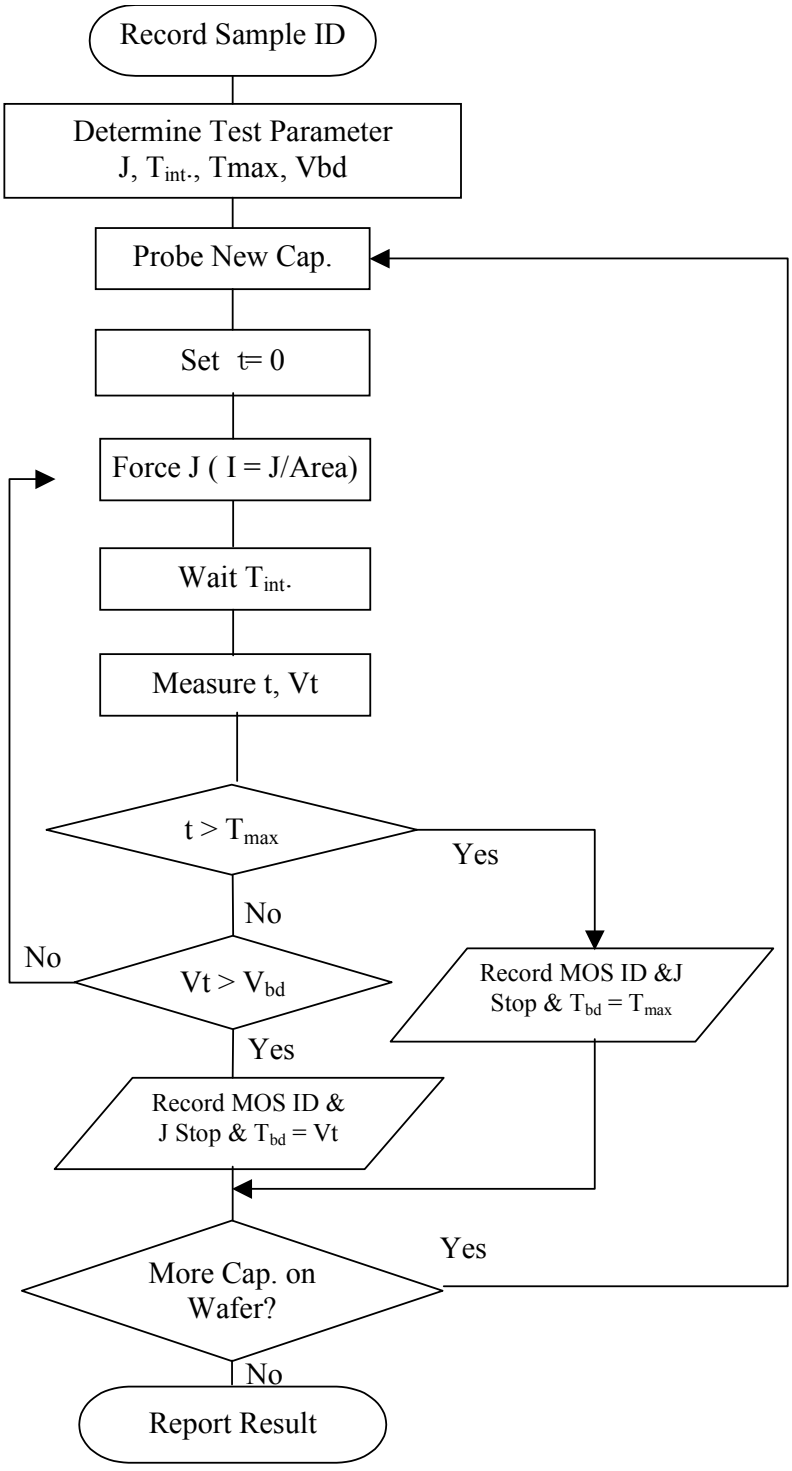


Figure 3
Flow Diagram Outline (1)

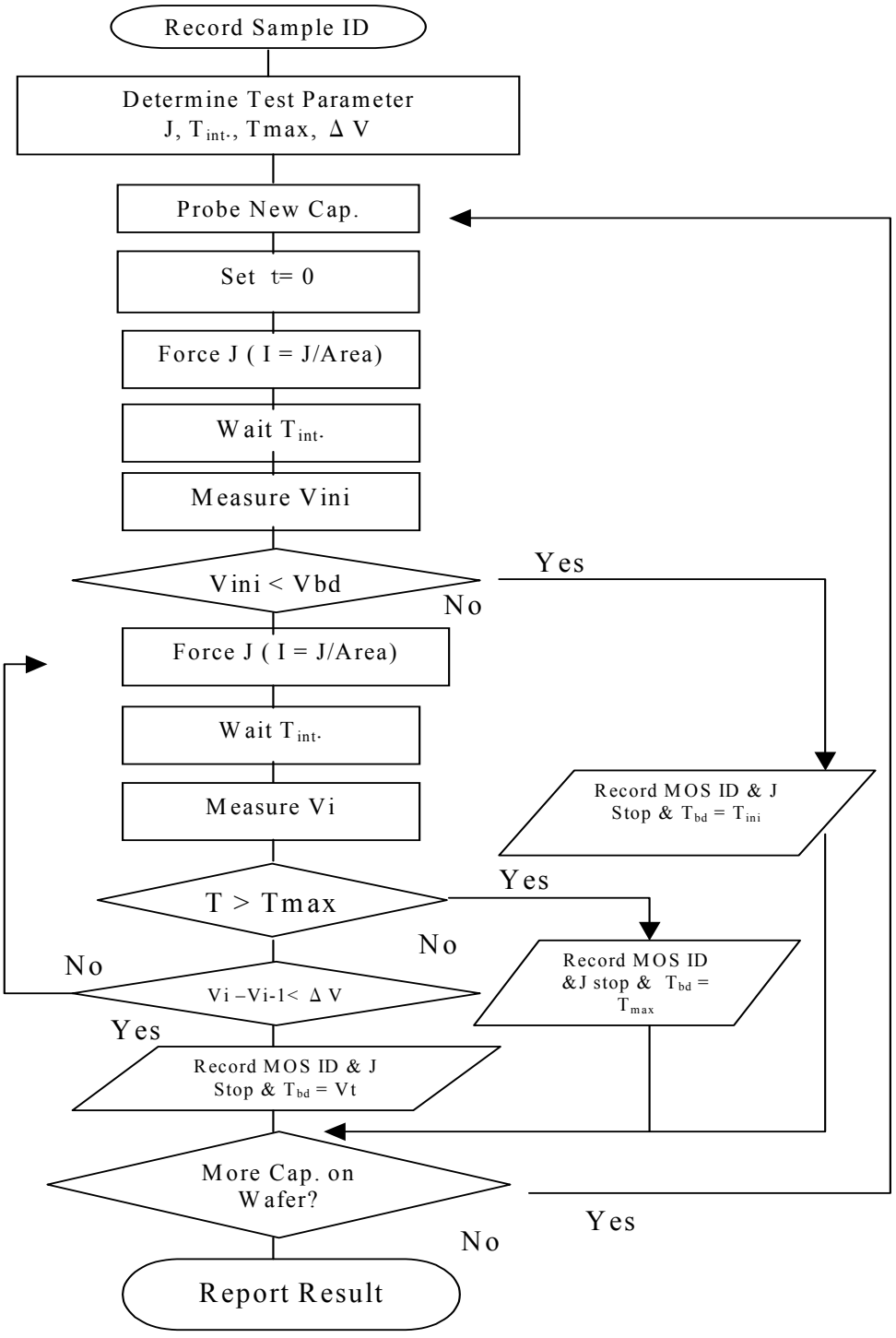


Figure 4
Flow Diagram Outline (2)

11 Calculations

11.1 *Current and Current Density*

11.1.1 To calculate current(I) from current density(J), multiply the current density by the area of gate area(S) as follows:

Symbolically:

$$I = J \times S \tag{1}$$

Example: Given a current density(J) of 1μA/cm^2 and a gate area(S) of 10 mm^2 , the current would be 100nA.

Similarly, compute current density(J, [A/cm^2]) from measured current(I, [A]) and area (S, [cm^2]) using.

$$J = I / S \text{ [A/cm}^2\text{]} \tag{2}$$

11.2 *Voltage and Electric Field Strength*

11.2.1 To calculate voltage(V) from an electric field(E), multiply the electric field strength by the gate oxide thickness(T_{ox}) as follows:

Symbolically:

$$V = E \times T_{ox} \tag{3}$$

where:

T_{ox} = Gate oxide thickness, cm.

Example: Given an electric field(E) of 15 MV/cm and a gate oxide thickness(T_{ox}) of 25nm, the voltage would be 37.5 V.

Similarly, compute electric field (E, [MV/cm]) from measured voltage(V, [V]) and gate oxide thickness(T_{ox}, [cm]) using.

$$E = V / T_{ox} \text{ [MV/cm]} \tag{4}$$

11.3 *Oxide Voltage*

11.3.1 Neglect the flatband voltage shift. The flatband voltage shift is due to gate-substrate work function difference[Φ_{ms}] and oxide fixed charge[Q_f]. Although it is better to consider this flatband voltage shift, its influence on the oxide film thickness in the range recommended in this test method is small.

11.4 *Calculation of Defect Density*

11.4.1 Calculate the defect density using the following equation based on the Poisson distribution assumption of the dielectric breakdown defects (see Standard EIA/JEDEC 35):

$$\rho_{ox} = - \ln (1 - F) / S \tag{5}$$

Here

ρ_{ox} = Defect density (defects/cm^2) ,

F = Failure fraction for each oxide breakdown mode ,

and S = Capacitor gate area (cm^2).

Example: Given a total of 100 MOS capacitors tested, with 30 accidental-mode-failed capacitors and a gate area of 10 mm^2, the defect density would be as follows:

$$\rho_{ox} = - \ln (1 - (30 / 100)) / 0.1$$

$$= 3.6 \text{ defects/cm}^2 \tag{6}$$

11.5 *Weibull Distribution*

11.5.1 To convert cumulative percent to Weibull format (sometimes referred to as "smallest extreme value probability distribution III"), use the following equation:

$$\ln (- \ln (1 - F)) \quad (7)$$

11.6 Where ln is the natural log operator and F is a percent of the cumulative failures. Care shall be taken so that F is never exactly 1 since this will be in an undefined situation.

12 Report

12.1 Report the following for each wafer, as appropriate for the test conditions and as agreed upon by the parties to the test.

12.1.1 Test Description

12.1.2 Date

12.1.3 Time

12.1.4 Operator

12.1.5 Measurement system ID

12.1.6 Sample lot ID

12.1.7 Wafer ID

12.1.8 Average oxide thickness

12.1.9 Gate area (cm^2)

12.1.10 Gate material

12.1.11 Oxidation parameters

12.1.12 Type of wafer (Ex: n or p)

12.1.13 Applied stress parameters

12.1.14 Test temperature

12.1.15 Process comment

12.1.16 Capacitor ID such as adress

12.1.17 V-T characteristic data

12.1.18 Breakdown time

12.1.19 Weibull plot of Q_{bd}

12.1.20 Average, median and maximum Q_{bd}

12.1.21 Breakdown mode yield

12.1.22 Breakdown mode map or Tbd / Q_{bd} map

12.1.23 Result of calculated defect density

RELATED INFORMATION 1
OUTLINE OF ROUND ROBIN

NOTICE: This related information is not an official part of SEMI M60 and was derived from the GOI Task Force. This round robin was conducted among Shin-Etsu Handotai Co., Ltd., Komatsu Electronic Metals Co., Ltd., Toshiba Ceramics Co., Ltd., Sumitomo Mitsubishi Silicon Corporation and MEMC Japan Ltd.

R1-1 MOS Structure

R1-1.1 *Gate Oxide Thickness*

R1-1.1.1 In this round robin, we evaluated the constant current TDDB (TDDB) of MOS capacitors with a gate oxide film thickness of 25 nm on mirror-polished, p-type, CZ silicon wafers. In the TDDB evaluation, a negative constant current was applied, and T_{bd} was measured.

R1-2 Correlation between TZDB and TDDB

R1-2.1 *Correlation Between TZDB and TDDB*

R1-2.1.1 A correlation between TZDB and TDDB is shown in Figure RI-1. This result is based on round robin. This figure is shown by defect densities of the TZDB and TDDB measurements. The defect densities of TDDB are generally higher than those of TZDB. This result is shown that the sensitivity to dielectric breakdown defect of TDDB measurement is higher than that of TZDB measurement.

R1-3 Classification of Breakdown mode

R1-3.1 In Figure RI-2, a typical cumulative failure fraction is shown as a function of charge injected before breakdown. Such a plot is called the TDDB Weibull plot. In the Weibull plot of the TDDB result, the breakdown events are categorized into the following three modes.

R1-3.2 *A-A Mode — Initial Breakdown Failure*

R1-3.2.1 Integrity of the oxide films in this mode is very low. There are COPs or oxygen precipitates other than particles, alkaline and metallic contamination at the Si surface of the MOS capacitors in this category. Classification of this mode with the following A-B mode is performed at a small amount of injected charge, Q_a, as illustrated in Fig RI-2. For example, the classification charge, Q_a, was $0.01C/cm^2$ in this round robin. This failure is caused by defects generated during formation of the gate oxide such as pinholes and also by crystal defects such as COPs. That is, this failure corresponds to the A mode and partial B mode failure of TZDB.

R1-3.3 *A-B Mode — Intermediate Breakdown Failure*

R1-3.3.1 This failure occurs in the intermediate time range from initial breakdown failure to wearout breakdown. This failure is caused by extrinsic defects. This failure corresponds to the B mode and partial C-mode failure of TZDB.

R1-3.4 *W Mode — Wearout Breakdown*

R1-3.4.1 This breakdown is also called intrinsic breakdown or wearout breakdown, and related to the intrinsic lifetime of oxide films. The failure fraction steeply increases as shown in Figure R1-2. The measurement of this breakdown should be performed carefully because the result depends on measurement conditions.

R1-3.4.2 Classification of the accidental and wearout modes, that is, the A-B and W modes, is far from easy because the W mode gradually shifts toward the A-B mode as shown in Figures R1-3, R1-5 and R1-6. It is statistically supported that the Weibull plot is straight in the W mode region. The regression straight line has the correlation coefficient higher than 0.9 with the experimental data. When the A-B mode breakdown events are added to the breakdown data, a correlation coefficient of the data and its straight line approximation decreases. This characteristic to determine the classification of the accidental and wearout modes can be used. In this round robin, the classification of the injected charge density, Q_w, was determined as follows. A regression straight line in the injected charge density range of higher than Q_w was obtained by the least square method. The recommended correlation coefficient is higher than 0.95. Q_w is $2C/cm^2$ in Figure R1-4. In a different manner, the cross point of two regression straight lines in the A-B and W mode breakdown ranges was read as Q_w.

R1-4 Dependence of Stress Current Density

R1-4.1 In this TDDB measurement, the stress electric field was applied so as to keep the oxide leakage current constant. The applied voltage was monitored at the constant time interval. A stress current of 0.001 A/cm^2 or less leads to uselessly long measurement time.

R1-4.2 On the other hand, too high a current density leads to nonuniform application of the stress voltage to the gate oxide. That is, the reliability of the measurement is reduced.

R1-4.3 In this round robin, the applied stress condition is shown in Table R1-1.

R1-4.4 The Weibull plot obtained in this round robin is shown in Figure R1-5. The Q_{bd} values and the accidental failure rates are shown in Table R1-2. The Q_{bd} clearly depended on the stress current in the stress range of this round robin. The Q_{bd} decreased with increasing stress current density, though the difference of the failure rates is slight. The failure rates in this result were defined by the sum of the accidental initial and intermediate modes in Figure R1-2. The classification between intermediate (A-B mode) and wearout (W mode) breakdowns was performed at the injected charge density of 2C/cm^2.

R1-4.5 The total accidental failure rates, that is, the sum of the A-A and A-B modes, were not influenced by the current density in this round robin condition. Therefore, the recommended stress current density range is from 0.1 to 0.01A/cm^2.

R1-5 Dependence of Measurement Temperature

R1-5.1 On the other hand, in this TDDB measurement, the stress temperature is an important parameter. The Q_{bd} depended on the stress temperature. Too high a temperature degrades the measurement system. In the stress temperature range of room temperature to 125ºC, systematic TDDB data were obtained. The recommended stress temperature is 125ºC or less.

R1-5.2 The stress conditions in this round robin are shown in Table R1-1. In this table, the accidental failure rate was defined by the sum of the initial and intermediate breakdowns in Figure R1-2. In this case, the classifications of the A-B and W modes were defined as follows:

125ºC–2C/cm^2

85ºC–5C/cm^2

25ºC (r.t.)–10C/cm^2

R1-5.3 The Q_{bd} depended on the stress temperature in this round robin condition. However, the sum of the accidental A-A and A-B breakdown modes was independent of stress temperature. Therefore, taking into consideration the above practical factors, the reasonable stress temperature range is from room temperature to 125ºC.

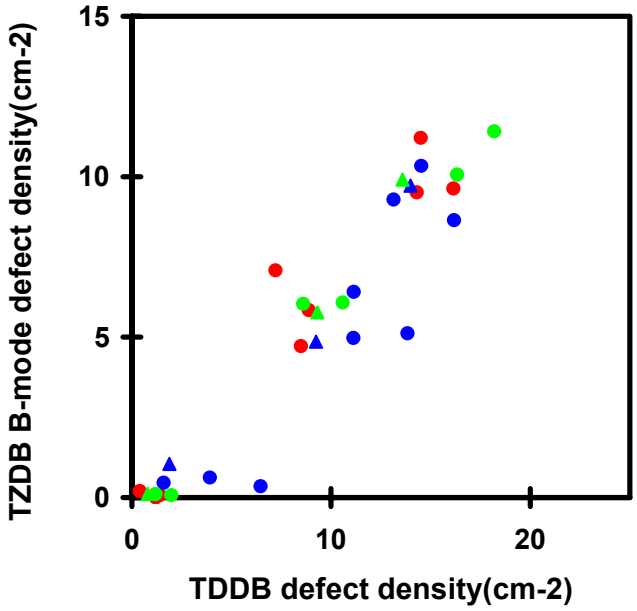


Figure R1-1
Correlation of Defect Densities of TZDB and TDDB Measurements

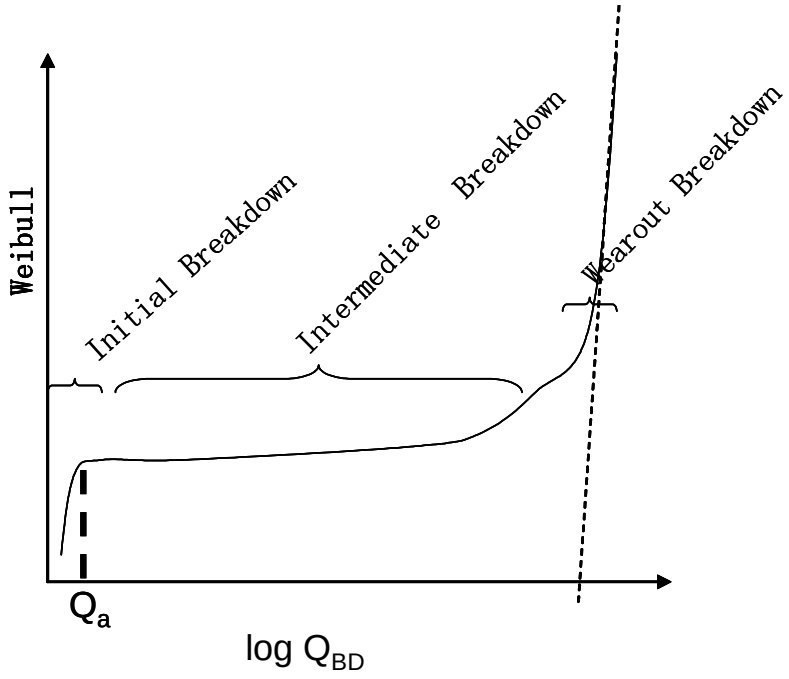


Figure R1-2
Classification of TDDB Breakdown Mode

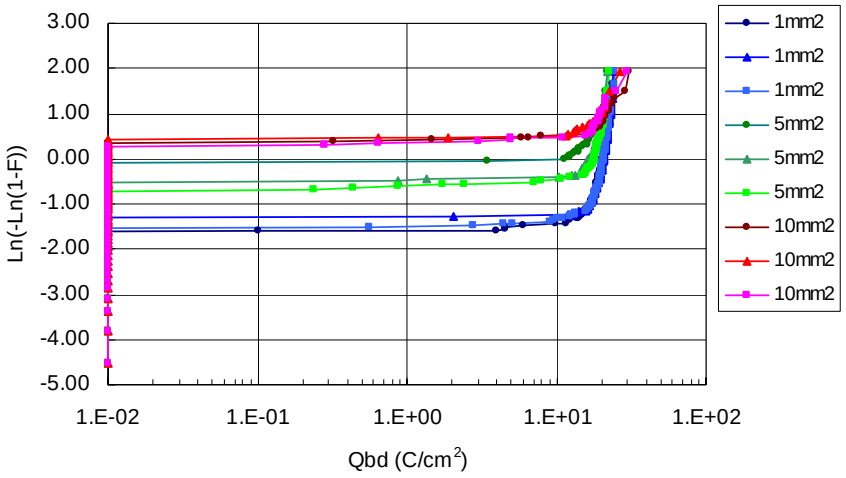


Figure R1-3
Capacitor Area Dependence of Q_{BD}. J=0.1A/cm^2, 125ºC.

Table R1-1 Measurement Condition of Constant Current Stress TDDB for Round Robin.

J_{stress} ($A \cdot cm^2$)	Temp.(ºC)
0.1	RT/80/125
0.05	125
0.01	125

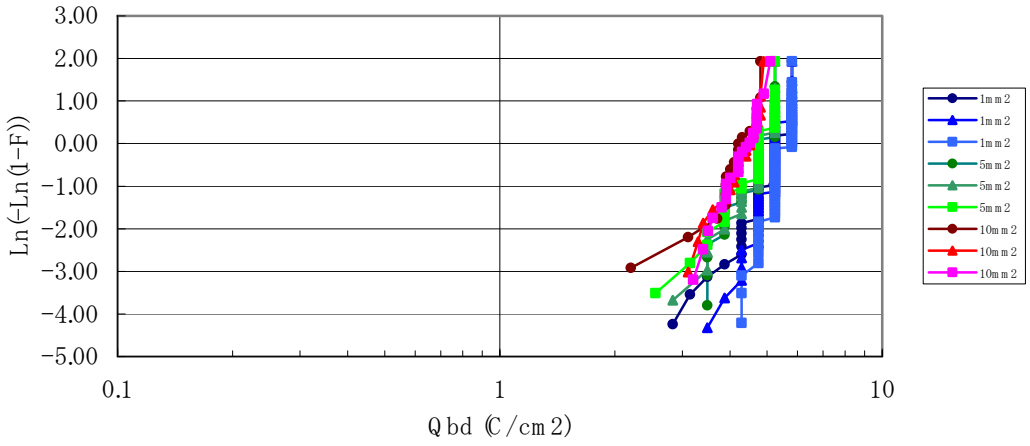


Figure R1-4
Gate Area Dependence of CCS-TDDB Measurement at 125ºC, 100mA/cm^2 in the W-mode Range of 2C/cm^2 or more. High Linearity in All TDDB Results Was Obtained in the W-mode Region.

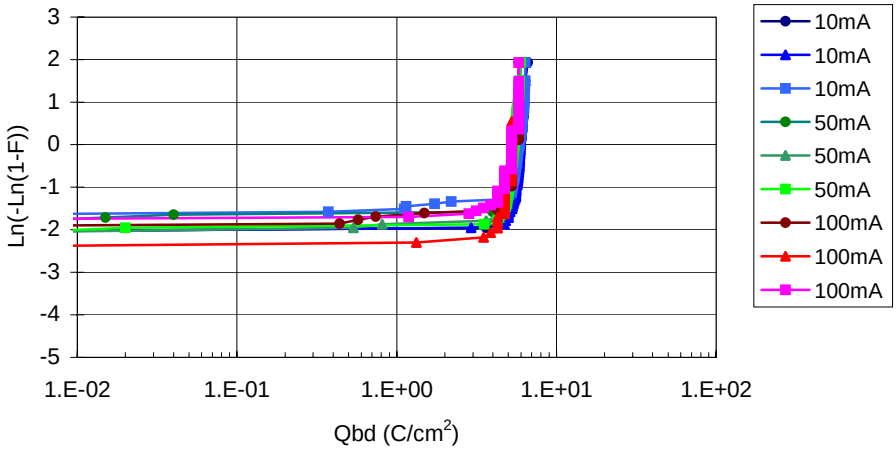


Figure R1-5
Current Density Dependence of Q_{BD}. 1mm^2, 125ºC

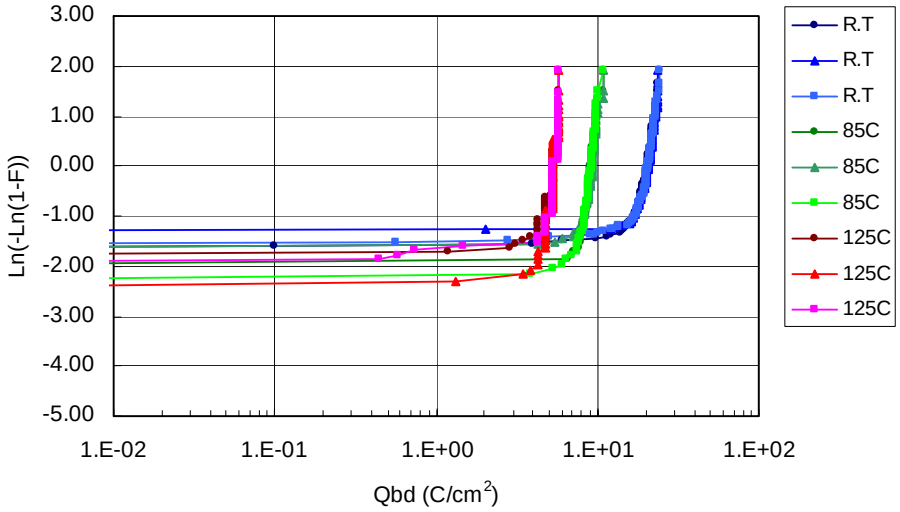


Figure R1-6
Temperature Dependence of Q_{BD}. J=0.1A/cm^2, 125ºC

Table R1-2 Current Density Dependence of Q_{BD}. (Area = 1mm^2, Temperature = 125ºC)

J (A/cm^2)	Failure (%)	Qbd (C/cm^2) at Weibull = 0
0.01	15.4	5.9
0.05	15.0	5.4
0.1	14.7	5.2