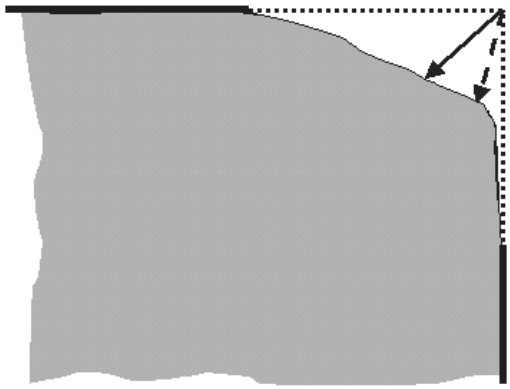


Figure 14
Corner Pull-Back: Bisectric (Full Line Arrow) vs. Minimum (Dotted Arrow)

8.2.4 *Specific Case of Line-End Shortening*

8.2.4.1 *line-end shortening* — deviation of the actual feature from the nominal feature at the nominal line-end. This is still qualitative, and can be quantified in general cases by overlaying the actual line contour to the nominal line (see Section 8.4). Alternatively, a test pattern such as Figure 17 may overcome the need to overlay to the nominal case.

NOTE 28: "line-end" is also used for the darkfield case (for spaces).

NOTE 29: In non-corrected isolated cases normally there is **only** a loss (or shortening). In other cases (i.e., corrected line-ends) there may be a loss and a gain (or extension), which makes it necessary to also define the difference and deviation, as done below.

NOTE 30: The minimum (= DEFAULT) region of interest must include all feature area divergence until the feature can be treated as one-dimensional (see Sections 5.3 and 5.4).

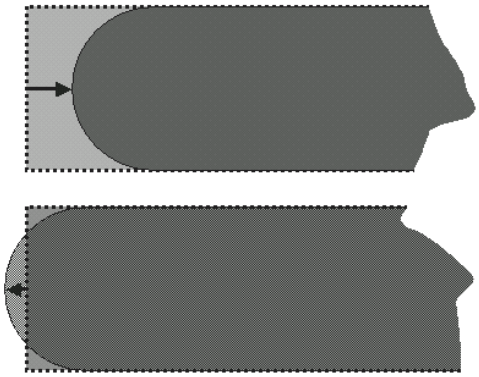


Figure 15
Quantification of line-end shortening by pull-back (arrow) or area comparison. Top: shortening case, below: extended case (e.g., caused by overcompensation)

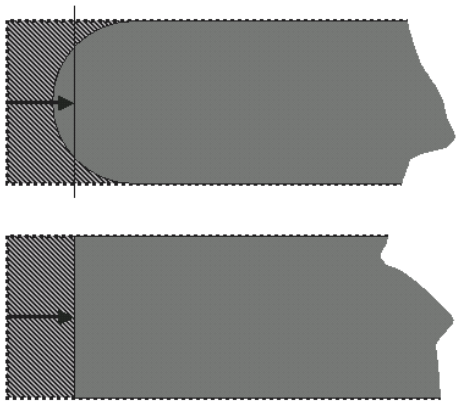


Figure 16
Quantification of line-end shortening by equivalent line-end shortening (shaded area is equal in the two figure halves)

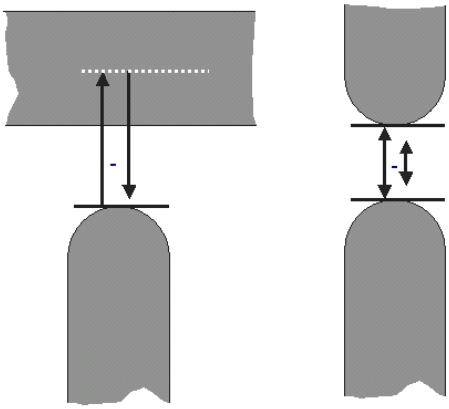


Figure 17
Proposed test patterns to overcome the need to overlay to the nominal case for the determination of line-end shortening

8.2.4.2 *line-end area gain* — special case of *clipped feature area gain*, in which the region of interest contains a line-end.

8.2.4.3 *line-end area loss* — special case of *clipped feature area loss*, in which the region of interest contains a line-end.

8.2.4.4 *line-end area difference* — *line-end area gain* minus *line-end area loss*. As such it becomes a special case of *clipped feature area difference*, in which the region of interest contains a line-end.

8.2.4.5 *line-end area deviation* — the sum of *line-end area gain* and *line-end area loss*. As such it becomes a special case of *clipped feature area deviation*, in which

the region of interest contains a line-end. Mandatory information for each of the 4 above:

- actual and nominal width,
- tone, pitch (or surrounding area), and
- orientation.

DEFAULT: isolated feature (line or space).

NOTE 31: As the line-end shape is expected not to be decisive for its printability, but rather the balance between area gain and loss, it is recommended to use *area difference* for line-end qualification rather than *area deviation*.

8.2.4.6 *line-end pull-back* (LEPB) — the distance, parallel to the line center, between the line-ends of the nominal and the actual features (see Figure 15). This distance may be determined along the line center (*center LEPB*), or alternatively it may be determined by the distance between the extreme point of the actual line and the nominal line-end (*minimum LEPB*), in analogy to corner *pull-back*. Mandatory information is:

- actual and nominal width,
- tone, pitch (or surrounding area),
- orientation, and
- choice of LEPB technique (*center* or *minimum*).

DEFAULT: isolated feature.

NOTE 32: Edge roughness may have an important influence on the *line-end pull-back*, such that contour averaging may be necessary to produce a meaningful result. The contour averaging method is mandatory info for LEPB, if done.

8.2.4.7 *equivalent line-end pull-back* (ELEPB) — defined as the negative *line-end area difference* divided by the nominal line width (see Figure 16), assuming accurate 1D control (see Section 8.1).

NOTE 33: This definition actually gives a 1D representation for a 2D quality assessement, but it is found useful when comparing mask quality to wafer printing results, which are typically characterized by 1D measurements, such that a dimensionless MEEF (mask error enhancement factor) can be used. As with area based assessment, also this term disregards the shape at the line-end.

NOTE 34: LEPB and ELES are positive when the actual line is shorter than the nominal line. A negative sign is added in case of over-correction, when the actual line becomes longer than the nominal line.

8.2.5 *Specific Case of Contacts and Dots*

NOTE 35: This sub-section explains terminology for contacts in full detail. This terminology can analogously be extended to dots.

8.2.5.1 *contact area* — special case of *feature area*, in which the feature is a contact (see Figure 18a).

8.2.5.2 *contact area gain* — special case of *feature area gain*, in which the region of interest contains a contact (see Figure 18b).

8.2.5.3 *contact area loss* — special case of *feature area loss*, in which the region of interest contains a contact (see Figure 18b).

8.2.5.4 *contact area difference* — *contact area gain* minus *contact area loss*. As such it becomes a special case of *feature area difference*, in which region of interest contains a contact.

8.2.5.5 *contact area deviation* — the sum of *contact area gain* and *contact area loss*. As such it becomes a special case of *feature area deviation*, in which the region of interest contains a contact. Mandatory information for each of the 4 above:

- nominal width in X and Y (Y not required for square contacts),
- nominal area (not required for square or rectangular contacts), and
- pitch (or the surroundings).

NOTE 36: The absolute value of the above qualification parameters can be normalized to the nominal contact area, i.e., *normalized contact area deviation and normalized contact area difference.*

NOTE 37: As the contact shape is expected not to be decisive for its printability, but rather the balance between area gain and loss, it is recommended to use *area difference* for contact qualification rather than *area deviation.*

8.2.5.6 *contact X-width* (or *contact Y-width*) — width in X (or Y) of the smallest rectangle along X (or Y) encompassing the contact (see Figure18c).

8.2.5.7 *contact diagonal widths* — widths determined using the smallest rectangle encompassing the contact confined along the directions $\pm \arctan(W_{Y,nominal}/W_{X,nominal})$ (see Figure 18d), which is ± 45degrees for square contacts.

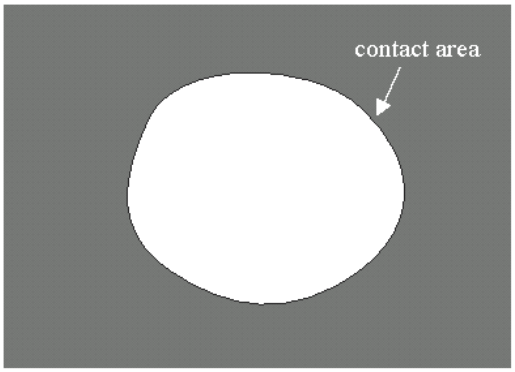
NOTE 38: Edge roughness may have an important influence on the 1D determination of *contact width (X-, Y-, diagonal-)*, such that contour averaging may be necessary to produce a meaningful result. The contour averaging method used is mandatory information for contact width and contact diagonal width, as its influence is increasingly important for smaller contacts (see Note 43 in Section 8.5).

8.2.6 *Specific Case of Optical Proximity Correction (OPC)*

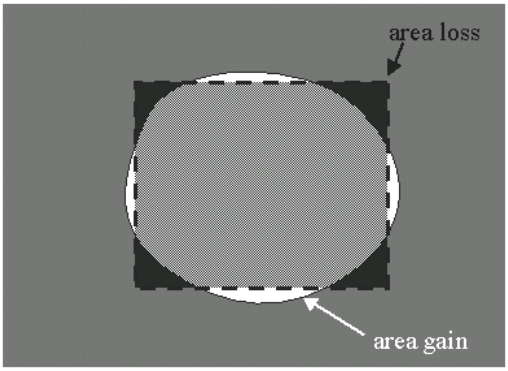
8.2.6.1 This document recommends to treat OPC'd features or patterns as a special case of Section 8.2.1 (based on area). OPC fidelity is based on normalized pattern area deviation and normalized pattern area difference.

8.2.6.2 1D metrology techniques for measuring OPC are not considered within this document's scope. As a good reference the reader is referred to for example Yonekura et al., (Toppan, PMJ2001, SPIE Proceeding Vol. 4409 p. 204)

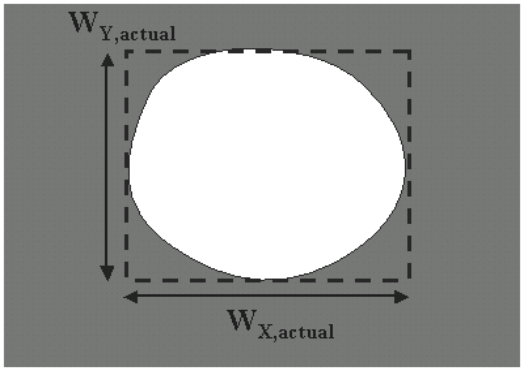
NOTE 39: Edge roughness may have an important influence on the 1D determination of OPC'd features, such that contour averaging may be necessary to produce a meaningful result.



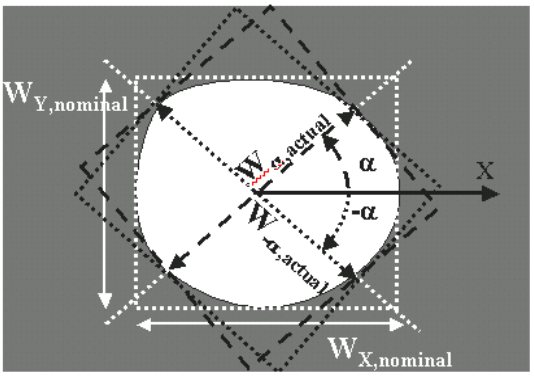
(a)



(b)



(c)



(d)

Figure 18
2D Quantification of a contact hole
by contact area,
by area gain and area loss
(dotted line is nominal contact),
by X and Y width (dashed line is smallest rectangle encompassing the actual contact),
by diagonal width (white dotted lines are the nominal contact and its diagonals confined by ± α,
where $\alpha = \arctan(W_{Y,nominal}/W_{X,nominal})$)

8.2.7 *Uniformity of 2D Qualification Parameters*

8.2.7.1 In principle all 2D qualification parameters, as defined above, may vary across the mask. By analogy to the transition from *feature width* to *feature width uniformity*, any 2D qualification parameter may be additionally characterized by uniformity. Below, as an example, *corner area difference uniformity* is elaborated.

8.2.7.2 *corner area difference uniformity* — the spread of the distribution of the *corner area difference* of all mask features selected as described below. To be stated as mandatory information in addition to that of *corner rounding* (Section 8.2.3.1) and also adopting the same DEFAULTS:

- the criterion used (range, 3-sigma, maximum area difference, etc.), where sigma stands for standard deviation.
  (Recommendation: before 3-sigma is relevant, the distribution needs to be "normal" or "near normal", and the number of measurements should be > 30.)
- The considered area of interest on the mask.

8.3 *Corrected True Values*

8.3.1 Some 2D measurements and definitions require that the mask is on target from a 1D-viewpoint, i.e., nominal and actual size coincide for semi-infinitely long features present in the region of interest. It is recommended to limit 2D characterization to features

with approximately the same width, such that 1D-linearity does not significantly affect the 2D value.

8.3.1.1 As an example, Figure 19 illustrates how a feature width deviation could affect the line-end.

8.3.1.2 Correction is required for benchmarking purposes, as described below.

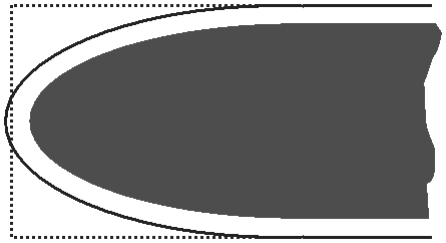


Figure 19
Example where correction of 2D-measurement (here shown for line-end shortening) for 1D-errors (full line) provides a different result

8.3.2 2D qualification may be refined by customer/vendor agreement (or by the user of this document) by compensating for

- the feature misplacement by alignment (see Section 8.4),

  NOTE 40: Pattern alignment is often required and affects the obtained values. Recommendations on pattern alignment for 2D qualification will be addressed in Section 8.4.

- the linewidth deviation (see Figure 20)

  b1) by a sizing correction based on the CD mean-to-target. This correction should be done before 2D-parameter determination,

  or

  b2) by a sizing correction based on the feature mean-to-target of the feature considered. This correction should be done before 2D-parameter determination, and

- feature linearity errors (feature proximity errors), using the same sizing corrections as in 8.3.2b, but based on specific feature width deviation.

8.3.2.1 What was modified and how it was done, is mandatory information.

NOTE 41: Scaling is not permitted.

NOTE 42: Sizing algorithm to be mentioned: orthogonally, by circular brush, perpendicularly, etc. (see Figure 21).

DEFAULT is compensation a and b1.

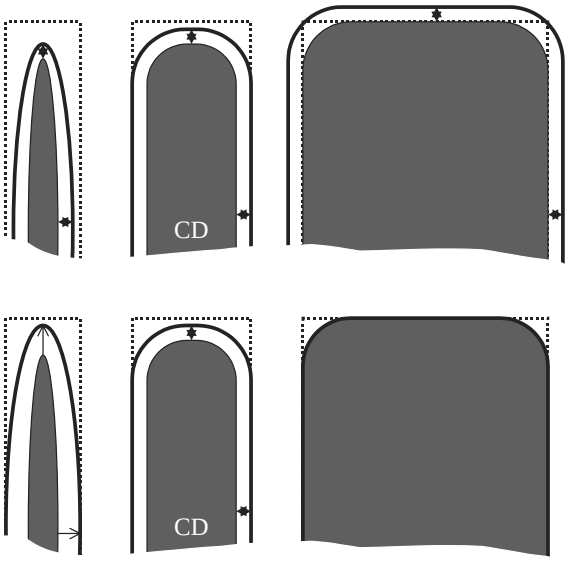


Figure 20
Illustration of correction for 2D features for 1D-error, according to techniques described under Section 8.3.2: b1 (upper) and b2 (lower)

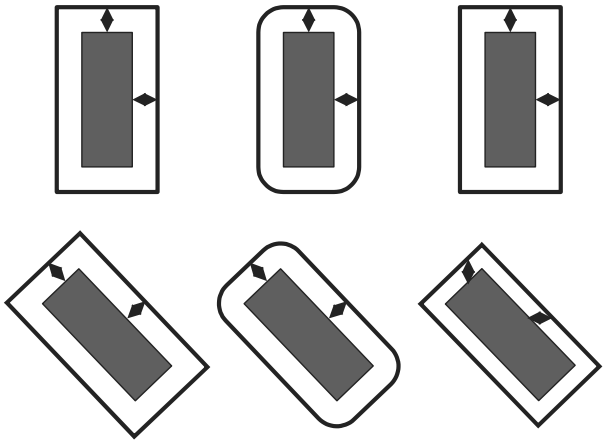


Figure 21
Examples of sizing rules for correction: from left to right: perpendicularly, by circular brush, orthogonally

8.4 *Alignment*

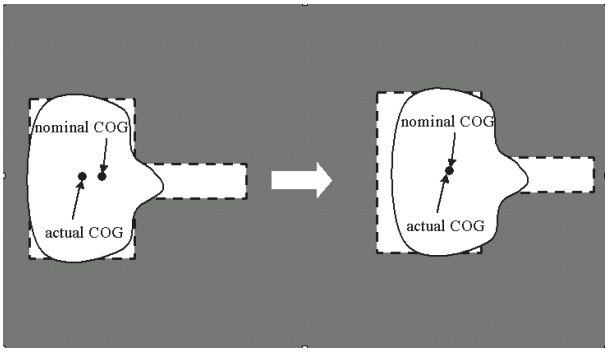
8.4.1 Alignment of nominal and actual feature (or pattern) is only practical when the ROI includes features where the actual case is a fairly good approximation to the nominal one.

8.4.2 Alignment can be done by one or more of the methods shown below. The result obtained by the different methods may differ. The method is mandatory information (see Figure 22).

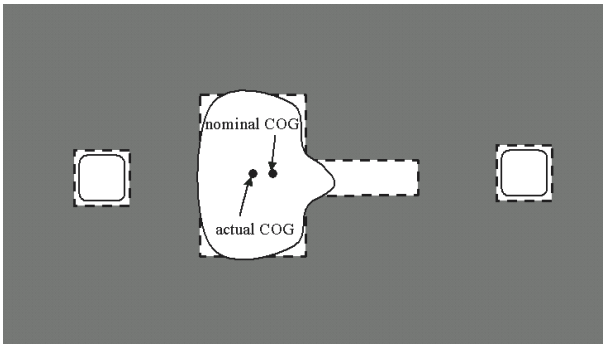
8.4.2.1 In the center-of-gravity (COG) method the COG of actual and nominal features are superimposed.

8.4.2.2 In the area based method the *absolute feature area deviation* between the actual and nominal features is minimized.

8.4.2.3 In the line-edge based method, alignment is performed by minimizing the distance between multiple actual and nominal edges.



(a)



(b)

Figure 22
Alignment of nominal and actual feature
(a) by center of gravity (COG) only, left is the intended overlay, right is actual overlay from the COG method, leading to an incorrect result.
(b) by the use of alignment markers.

8.4.3 Alignment is preferably done on dedicated alignment features (markers), which are symmetric and not clipped, and their position does not suffer from the resolution of the imaging process. Crosses are typically used, as they have X and Y components, which can be used to correct for rotational error if only one marker were present.

8.4.4 Additional markers allow for more accurate rotational compensation and decouple magnification errors of the feature to be measured from sizing errors.

8.4.5 If no markers are present, one of the methods above can be attempted on the feature to be measured or on other features in the ROI, but in such situation alignment may be less accurate, especially if these features are clipped (see Figure 22).

8.5 *Measured Values*

8.5.1 By analogy to Section 7 (1D Mask Qualification Terminology) a measured qualification parameter can be defined for every 2D (true) qualification parameter defined in Section 8.2. In Section 7 this was done immediately after the definition of the true parameter, whereas here the measured parameter is treated in a generic way. Thereby, one 2D qualification parameter is used for the explanation, i.e., *measured corner area difference* and its uniformity, as examples for all other 2D qualification parameters and their uniformity.

NOTE 43: The most critical feature in terms of impact of the measurement details to the measured values is the size of a contact near the resolution limit of the metrology tool and of the mask patterning process.

8.5.2 *measured corner area difference* — measured value of *corner area difference*, stating as mandatory information, in addition to that of *corner rounding* (Section 8.2.3.1):

- calibration method used[4],
- measurement method used (SEM, optical reflection, optical transmission, AFM, etc.) and its resolution limit,
- edge detection algorithm and parameters,
- precision (SEMI P24),

and as optional information :

- measurement tool (vendor, model or any tool specific options).

8.5.3 *measured corner area difference uniformity* — measured value of *corner area difference uniformity*, thereby stating as mandatory information in addition to that of *corner area difference uniformity* and of *measured corner area difference*:

- the number of measurement points used,

and as optional information:

- the spatial distribution of measurement locations, e.g., by coordinates of measurement locations. DEFAULT is spread evenly over the measurement area.

NOTE 44: Edge roughness, either originating from the process (Note 19 in Section 8.2.2) or from the measurement technique used, may influence the measurement result. This is not the case for the two examples treated above, as the *difference* parameter filters out the effect of roughness by

4 See reference document in Section 4.2.

allowing compensation of area gain and area loss. In case of, e.g., *corner area devation uniformity*, line-edge roughness will influence the measurement result.

NOTICE: SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature, respecting any materials or equipment mentioned herein. These standards are subject to change without notice.

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SEMI INTERNATIONAL STANDARDS

PACKAGING

Semiconductor Equipment and Materials International

SEMI G1-96
SPECIFICATION FOR CERDIP PACKAGE CONSTRUCTIONS

NOTE: This entire document was revised in 1996.

1 Purpose

This specification defines the materials and acceptance criteria for the components (bases, window frames, and caps) or sub-assemblies (leadframes mounted in a sandwich between bases and window frames) used for cerdip package constructions.

NOTE 1: Materials and acceptance criteria for leadframes, purchased separately for these constructions, are described in SEMI G2.

2 Scope

This specification applies to all cerdip (dual-in-line) packages which have either:

- A leadframe sandwiched between two ceramic pieces — the base and a window frame — and sealed by a solder glass layer, and a cap with a similar seal; or,
- A leadframe mounted into a solder glass layer on a ceramic base, and a cap with a similar glass seal layer.

NOTE 2: The base, leadframe, and, if required, the window frame may be purchased as separate components or as a sub-assembly.

3 Units

This specification uses U.S. Customary (inch pound) units as the prime unit.

4 Referenced Documents

4.1 *Order of Precedence*

To avoid conflicts, the order of precedence when ordering components or sub-assemblies for cerdip packages shall be as follows:

- Purchase order
- User's package drawings
- This specification
- Reference documents
- Related documents

4.2 *Referenced Documents*

4.3 *SEMI Specifications*

SEMI G2 — Specification Metallic Leadframes for Cer-Dip Packages

SEMI G20 — Specification Lead Finishes for Plastic Packages (Active Devices only)

SEMI G23 — Test Method Measuring the Inductance of Package Leads

SEMI G24 — Test Method Measuring the Lead-to-Lead and Loading Capacitance of Package Leads

SEMI G25 — Test Method Measuring the Resistance of Package Leads

SEMI G30 — Test Method Junction-to-Case Thermal Resistance Measurements of Ceramic Packages

4.4 *ANSI Specification*[1]

ANSI Y14.5M — Dimensioning and Tolerancing

4.5 *JEDEC Publication*[2]

JEDEC Publication 95 — Registered and Standard Outlines for Semiconductor Devices

4.6 *Military and Federal Specifications*[3]

MIL-STD-105D — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-STD-1835 — Microcircuit Case Outlines

MIL-I-38535 — General Specifications for Microcircuits

5 Terminology

5.1 *blister (bubble) metallization* — An enclosed, localized separation of the metallization from its base material (such as ceramic or other metallization layer component) that does not expose the underlying layer.

5.2 *burr* — An adherent fragment of parent material at a component edge. In leadframes, the metal burr, due to the stamping operation, may be in the horizontal or vertical direction to the surface. In ceramic packages, this type of characteristic is called a fin.

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1 American National Standards Institute, 1430 Broadway, New York, NY 10018

2 Joint Electronic Development Engineering Council, 2001 Eye Street, N.W., Washington, D.C. 20006

3 Military Standards, Naval Publications and Form Center, 5801 Tabor Avenue, Philadelphia, PA 19120

5.3 *camber (ceramic)* — Arching of a nominally flat ceramic body.

5.4 *chip* — A region of material missing from a component (e.g., ceramic from a package, or solder from a preform). The region does not progress completely through the component and is formed after the component is manufactured. Chip size is defined by its length, width, and depth from a projection of the design planform. Also called chipout (see Figure 1).

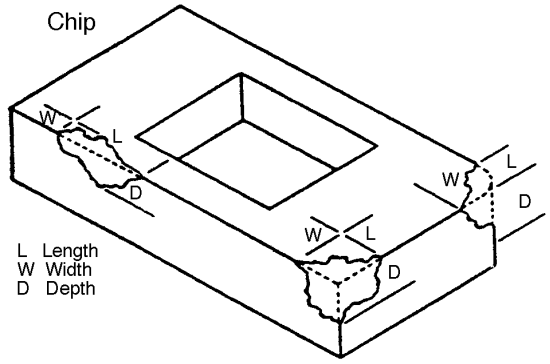

Figure 1

5.5 *crack* — A cleavage or fracture that extends to the surface of a semiconductor package or solder preform.The crack may or may not pass through the entire thickness of the package or preform.

5.6 *critical seal area* — On a semiconductor package, the area bounded by the shortest nominal design distance from the largest cavity, usually the wire bond cavity, to the edge of the package or ceramic layer forming the seal area (see Figure 2).

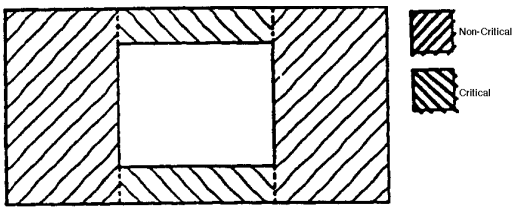

Figure 2
Critical and Non-Critical Seal Area

5.7 *fin* — On a ceramic package or cap, a fine feathery-edged projection of parent ceramic material on the corner of the ceramic body.

5.8 *foreign material* — An adherent particle that is not parent material of the component. Adherence means that the particle cannot be removed by an air or nitrogen blast at 20 psi.

5.9 *glass flow* — On a semiconductor package or cap, the heating process which just removes all the screen printing mesh marks in the sealing glass when viewed at 10× magnification.

5.10 *glass void* — The absence of a sealing glass layer from a designated area.

5.11 *metallization void* — The absence of a clad, evaporated, plated, or screen-printed metal layer or braze from a designated area.

5.12 *non-critical seal area* — On a semiconductor package that uses a lid, cap, or cover to effect the seal, the area of the sealing surface outside the critical sealing area (see Figure 2).

5.13 *overhang* — On a semiconductor package, the horizontal extension of the sealing glass past the vertical wall of a cavity cut into the ceramic layer on which the glass is printed (see Figure 3).

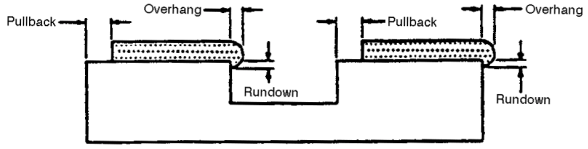

Figure 3
Glass Misalignment

5.14 *peeling (flaking)* — Any separation of a plated, vacuum-deposited, or clad metal layer from the base metal of a leadframe, pin heatsink, or seal ring, from an underplate or from a refractory metal on a ceramic package. Peeling exposes the underlying metal.

5.15 *projection* — On a semiconductor package (plastic or ceramic) leadframe or preform, an irregularly raised portion of a surface indigenous to the parent material.

5.16 *pullback* — On a semiconductor package, the linear distance between the edge of a cavity cut into a ceramic layer and the first measurable glass or metallization layer interface coated onto the top surface of that layer. The total pullback may be the result of the high-temperature processing required to manufacture the package or to coat the surface. It may also be the result of design considerations (see Figure 3).

5.17 *rundown* — On a semiconductor package, the linear distance from the upper surface of a ceramic cavity layer to the bottom point of the overhang into the cavity, of a sealing glass or metallization layer that has been screened onto that surface (see Figure 3).

5.18 *seal area* — On a semiconductor package, the area designated for sealing a cover or lid to a cofired ceramic package, to a cap to a cer-pack base.

5.19 *void* — An absence of metallization or glass from a designated metallized or glassed area on a ceramic surface.

6 Ordering Information

Purchase orders for cerdip components or sub-assemblies furnished to this specification shall include the following items:

6.1 Current drawing revision detailing:

6.1.1 All dimensions and tolerances per ANSI Y14.5M practices

6.1.2 Type and color of ceramic

6.1.3 Type and thickness of glass

6.1.4 Type and thickness of die pad metallization

NOTE 3: If sub-assemblies are purchased, the leadframe details shall be as described in SEMI G2. In some cases, unlike the frames described in SEMI G2, the leadframes may also have a die-attach pad. If required, the external lead plating requirements for these sub-assemblies shall also be specified. (See SEMI G20 for general details of lead finishes.) If sub-assemblies are purchased, leadframe inspection shall follow the requirements detailed in Section 9.

6.2 *Incoming Inspection and Functional Tests* — See Sections 9 and 10.

6.3 *Incoming Sampling Procedures* — See Section 11.

6.4 *Packaging and Marking Requirements* — See Section 12.

6.5 *Vendor Certification Requirements* — See Section 13.

6.6 Any additions to, or variations from, this specification.

7 Dimensions

The components or sub-assemblies described in this specification shall produce packaged devices that conform to the outline dimensions and lead numbering for cerdip package constructions detailed in:

— JEDEC Publication 95 and

— MIL-STD-1835.

Package manufacturing tolerances shall be agreed upon between user and supplier and detailed in the drawings.

Typical dimensions and tolerances for standard bases and caps are shown in the appendices at the end of this specification.

8 Materials

The definitions defect criteria and functional tests described in this specification relate to package components made with the following materials:

8.1 *Bases, Window Frames, and Caps*

8.1.1 *Material* — Ceramic with 90% alumina, minimum content.

8.1.2 *Color* — Black, dark brown, or dark violet.

8.2 *Sealing Material*

8.2.1 *Material* — Solder glass designed to seal metal (typically Iron-Nickel-Cobalt alloy per MIL-M-38150, Type A or Iron-Nickel alloy per MIL-M-38150 Type B) to ceramic.

8.3 *Die-Attach Pad*

8.3.1 *Material* — Thick film gold or other specified material.

8.4 *Leadframe*

8.4.1 Leadframes, whether purchased as component or in sub-assemblies, shall conform to the requirements of SEMI G2 as required.

9 Defect Limits

The following defects shall be cause for rejection if the limits shown are exceeded:

NOTE 4: The criteria apply to purchased components and pre-assemblies, as applicable, or, where applicable, to units assembled by the user to process conditions agreed upon between the user and supplier.

9.1 *Ceramic Components*

9.1.1 *Cracks* — Any crack.

9.1.2 *Chips* — See Figures 1 and 2.

9.1.2.1 *Corner Chips* — 0.030" (0.762 mm) × 0.030" (0.726mm) × 25% of the package element thickness.

9.1.2.2 *Edge Chips* — 0.100" (2.54 mm) × 0.030" (0.726mm) × 25% of the package element thickness.

9.1.2.3 *Critical Seal Area* — Chips shall not reduce the critical seal path, at any point, more than 30%. No more than four chips are allowed in this area, regardless of loss of seal length.

9.1.3 *Burrs, Projection (Fins), and Blisters*

9.1.3.1 *Bases, Caps, and Window Frames* — 0.005" (0.127 mm) maximum allowable dimension in the plane of the component, or greater than 0.003" (0.076 mm) in height.

9.1.3.2 *Die-Attach Surface (on Base Ceramic)* — 0.005" (0.127 mm) dimension in the plane of the component, or greater than 0.001" (0.254 mm) above the surface of the metallization excluding a zone, 0.010" (0.254 mm) wide, around the periphery of the cavity.

9.1.4 *Camber* — Shall be agreed upon between user and supplier and specified on the component or sub-assembly drawing. Standard limits shall be 0.003"/inch (0.003 mm/mm), maximum, with a minimum allowable camber of 0.002" (0.051 mm).

9.1.5 *Foreign Material* — 0.020" (0.508 mm) maximum allowable surface dimension or 0.005" (0.127 mm) in height. No more than three sites allowed and a minimum separation of 0.030" (0.762 mm) between sites.

9.2 *Glass Sealant*

9.2.1 *Chips and Voids* — 0.010" (0.025 mm) maximum allowable dimension. In the critical seal, there shall be no more than four acceptable chips or voids. In critical and non-critical seal areas, there shall be no voids after a glass flow cycle.

9.2.2 *Glass Misalignment* — (After glass flow on components, see Figure 3, or on sub-assemblies.)

9.2.2.1 *Glass Overhang* — 0.015" (0.381 mm) maximum extension from the ceramic edge.

9.2.2.2 *Glass Rundown* — 50% of the package element thickness.

9.2.2.3 *Glass Rundown into the Die-Attach Cavity* — 0.010" (0.254 mm) maximum extension from the ceramic surface into the cavity.

9.2.2.4 *Glass Pullback (After Glass Flow)* — See Table 1 and Figure 3.

Table 1 Maximum Allowable Pullback

Area of Package	*Package Row Spacing*	*Package Row Spacing*
	0.300" (7.500 mm) and 0.400"(10.16 mm)	0.600" (15.24 mm) and larger
Side external (critical seal area)	0.010" (0.254 mm)	0.015" (0.381 mm)
Side external (non-critical seal area)	0.015" (0.381 mm)	0.015" (0.381 mm)
End external	0.020" (0.508 mm)	0.020" (0.508 mm)
Side cavity	0.010" (0.254 mm)	0.015" (0.381 mm)
End cavity	0.010" (0.254 mm)	0.015" (0.381 mm)
Maximum allowable critical seal length reduction on any one side, as measured between the cavity and the external side	0.015" (0.381 mm)	0.020" (0.508 mm)

NOTE 5: Regardless of the maximum criteria noted in Table 1, the critical seal length at any point shall not be reduced any more than 30%.

9.2.2.5 *Foreign Material* — 0.020" (0.508 mm) maximum allowable surface dimension in the plane of the glass, but 0.010" (0.254 mm) in the critical seal area, with no more than three sites allowed and a minimum separation of 0.030" (0.762 mm) between sites.

9.3 *Die-Attach Cavity Metallization (0n Ceramic Base)* — Excluding a 0.010" (0.254 mm) wide zone around the periphery of the cavity, the following criteria shall apply:

9.3.1 *Foreign Material, Including Glass Splatters* — 0.005" (0.130 mm) maximum in the plane of the metallization or greater than 0.001" (0.025 mm) in height with no more than three sites allowed and a minimum separation of 0.030" (0.763 mm) between sites.

9.3.2 *Metallization Nodules* — No more than three allowed. If the metallization is gold and gold-silicon eutectic die attach is to be used, the bumps may not exceed 0.010" (0.254 mm) in the surface dimension or 0.005" (0.130 mm) in height. If silver glass or resin bonding is to be used, the nodules shall be treated as foreign material per Section 9.3

9.4 *Leadframe*

NOTE 6: The criteria described in this section generally apply to leadframe inspection for purchased sub-assemblies. Where appropriate, the criteria may be used for sub-assemblies manufactured in-house with purchased components. For information on the criteria for leadframes purchased separately, see SEMI G2.

9.4.1 *Lead Bond Areas* — The minimum lead bond area on the lead tip is defined in Figure 4.

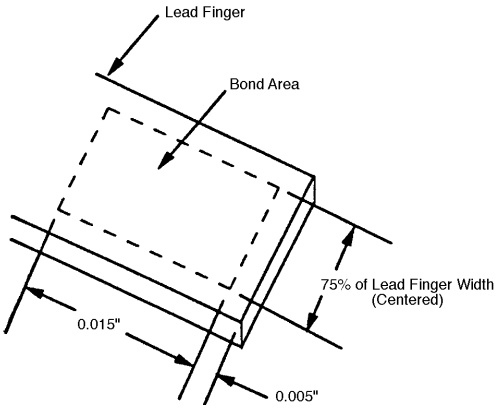

Figure 4

9.4.1.1 *Voids or Pits* — Exposure of base metal with any dimension greater than 0.001" (0.025 mm).

9.4.1.2 *Discoloration, Blistering, or Peeling of the Metallization*

9.4.1.3 *Scratches or Scrapes* — Any build-up of metallization or exposure of base metal.

9.4.1.4 *Foreign Material, Including Glass Splatter or Projections* — No more than three sites, each with a maximum dimension in any plane of 0.001" (0.025 mm).

9.4.1.5 *Glass Wetting or Cracking* — For purchased sub-assemblies, any lead finger which is not firmly embedded in the glass.

9.4.1.6 *Glass Pullback from the Lead Tip* — 0.010" (0.254 mm) maximum.

9.4.1.7 *Glass Bulge between Lead Fingers (Purchased or In-House Sub-Assemblies)* — 0.005" (0.127 mm) height above the fingers except as agreed upon between user and supplier for narrow pitch leads where this limit may cause wire bond interference problems.

9.4.1.8 *Lead Tip Coplanarity* — 0.006" (0.15 mm) maximum allowable difference in the position of the top surface of the lead from highest lead to lowest lead.

9.4.1.9 *Lead Tip Pitch* — ± 0.002" (0.508 mm) maximum allowable variation from true position.

9.4.2 *Internal Lead Areas, Excluding Lead Bond Areas*

9.4.2.1 *Burrs, Projections, and Pits* — 0.002" (0.508 mm) maximum allowable depth or height.

9.4.2.2 *Foreign Material, Including Plating Discoloration* — 0.015" (0.381 mm) maximum surface dimension or exceeding 0.002" (0.508 mm) in height.

9.4.2.3 *Voids* — Any exposure of base metal with a major dimension greater than 0.002" (0.508 mm).

9.4.2.4 *Blistering or Peeling of Metallization*

9.4.2.5 *Scratches and Scrapes* — Any build-up of metallization or exposure of base metal.

9.4.3 *External Lead Areas — Unplated*

NOTE 7: Non-functional areas of the leadframe, such as tie bars, shall not be subjected to inspection unless they interfere with handling equipment.

9.4.3.1 *Scratches* — Any scratch causing a loss of more than 25% of the leadframe thickness.

9.4.3.2 *Voids* — Any void which violates the criteria of Section 9.4.3.1 or causes a loss of more than 10% of the design width of a leadframe detail.

9.4.3.3 *Burrs* — In excess of 0.002" (0.051 mm) in height and 0.005" (0.127 mm) in the major dimension.

9.4.4 *External Leads — Plated*

NOTE 8: Non-functional areas of the leadframe, such as tie bars, shall not be subjected to inspection unless they interfere with handling equipment.

9.4.4.1 *Scratches* — Any scratch causing a loss of more than 25% of the leadframe thickness.

9.4.4.2 *Voids* — Any void which violates the criteria of Section 9.4.3.1 or causes a loss of more than 10% of the design width of leadframe detail.

9.4.4.3 *Burrs* — In excess of 0.002" (0.051 mm) in height and 0.005" (0.127 mm) in the major dimension.

9.4.4.4 *Scratches and Scrapes* — Any exposure of the base metal or loss of plating integrity over more than 5% of a lead finger.

9.4.4.5 *Voids* — Any exposure of base metal.

9.4.4.6 *Blistering or Peeling*

9.4.5 *Leadframe/Base/Window Assembly*

9.4.5.1 *Lead Tip Overhang* — 0.010" (0.254 mm) maximum from the cavity wall (see Figure 5).

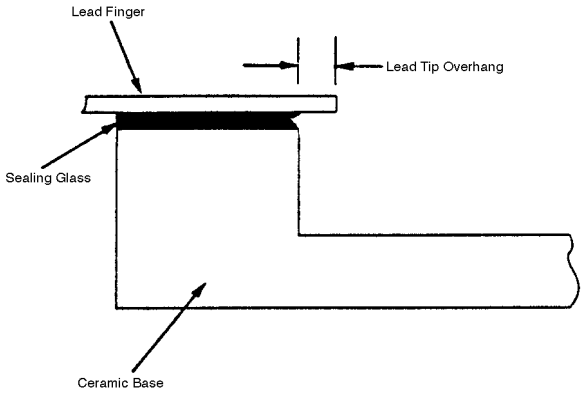

Figure 5

9.4.5.2 *Lead Misalignment to Ceramic Base* — 0.010" (0.254 mm) maximum (see Figure 6).

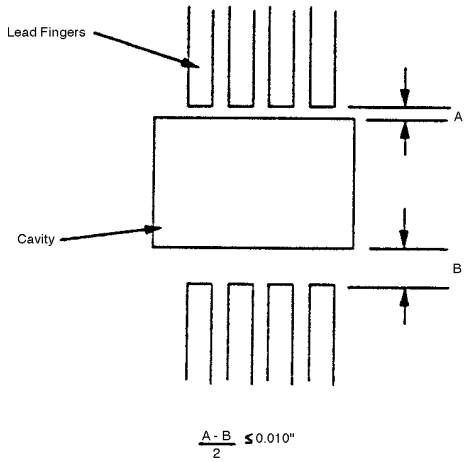

Figure 6

9.4.5.3 *Window Assembly Misalignment* — 0.015" (0.358 mm) maximum (see Figure 7).

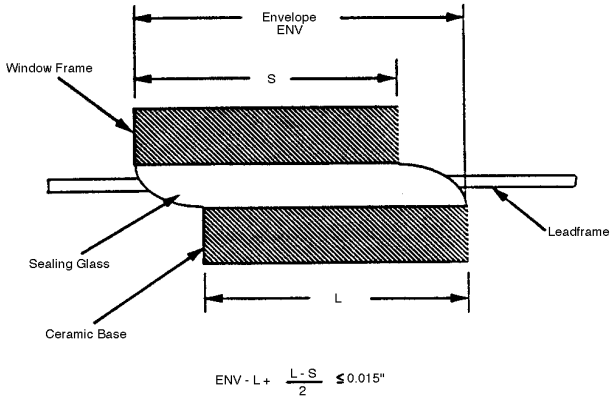

Figure 7

9.4.6 *Die-Attach Pad (Leadframe)*

9.4.6.1 Flatness across the pad and parallelism to the base and window shall be agreed upon between user and supplier.

9.4.6.2 *Voids or Pits* — Exposure of base metal with any dimension greater than 0.001" (0.025 mm).

9.4.6.3 *Discoloration, Blistering, or Peeling of the Metallization*

9.4.6.4 *Scratches or Scrapes* — Any build-up of metallization or exposure of base metal.

9.4.6.5 *Foreign Material, Including Glass Splatter or Projections* — No more than three sites, each with a maximum dimension in any plane of 0.001" (0.025 mm).

9.4.7 *Mechanical Damage — Leads*

9.4.7.1 *Broken, Kinked, or Missing Leads*

9.4.7.2 *Twist* — Any lead twisted by more than 10° from the untwisted condition.

9.4.7.3 *Bottom-Formed Width* — Any sub-assembly with the bottom-formed width of the leadframe exceeding ± 0.010" (0.254 mm).

9.4.7.4 *Top-Formed Width* — Any sub-assembly with the top-formed width of the leadframe exceeding ± 0.010" (0.254 mm).

10 Incoming Inspection and Functional Tests

10.1 *Incoming Inspection*

10.1.1 Dimensional Inspection per Section 7.

10.1.2 Visual inspection per Section 9 at 10× magnification with vertical lighting.

10.1.3 *Metallization*

10.1.3.1 *Die-Attach Metallization* — Thickness shall be measured by standard cross-sectioning without smearing or by X-ray fluorescence.

10.1.3.2 *Lead Bond Metallization* — Thickness shall be measured by X-ray fluorescence.

10.1.3.3 *External Lead Plating (If Applicable)* — Thickness shall be measured by X-ray fluorescence.

10.1.4 *Lead Solderability (If Applicable)* — Tested in accordance with MIL-STD-883, Method 2003.

10.2 *Functional Testing*

NOTE 9: All procedures to functionally test the components or sub-assemblies shall be agreed upon between user and supplier.

The sequence of functional testing (and subsequent environmental testing) shall be as shown in Figure 8.

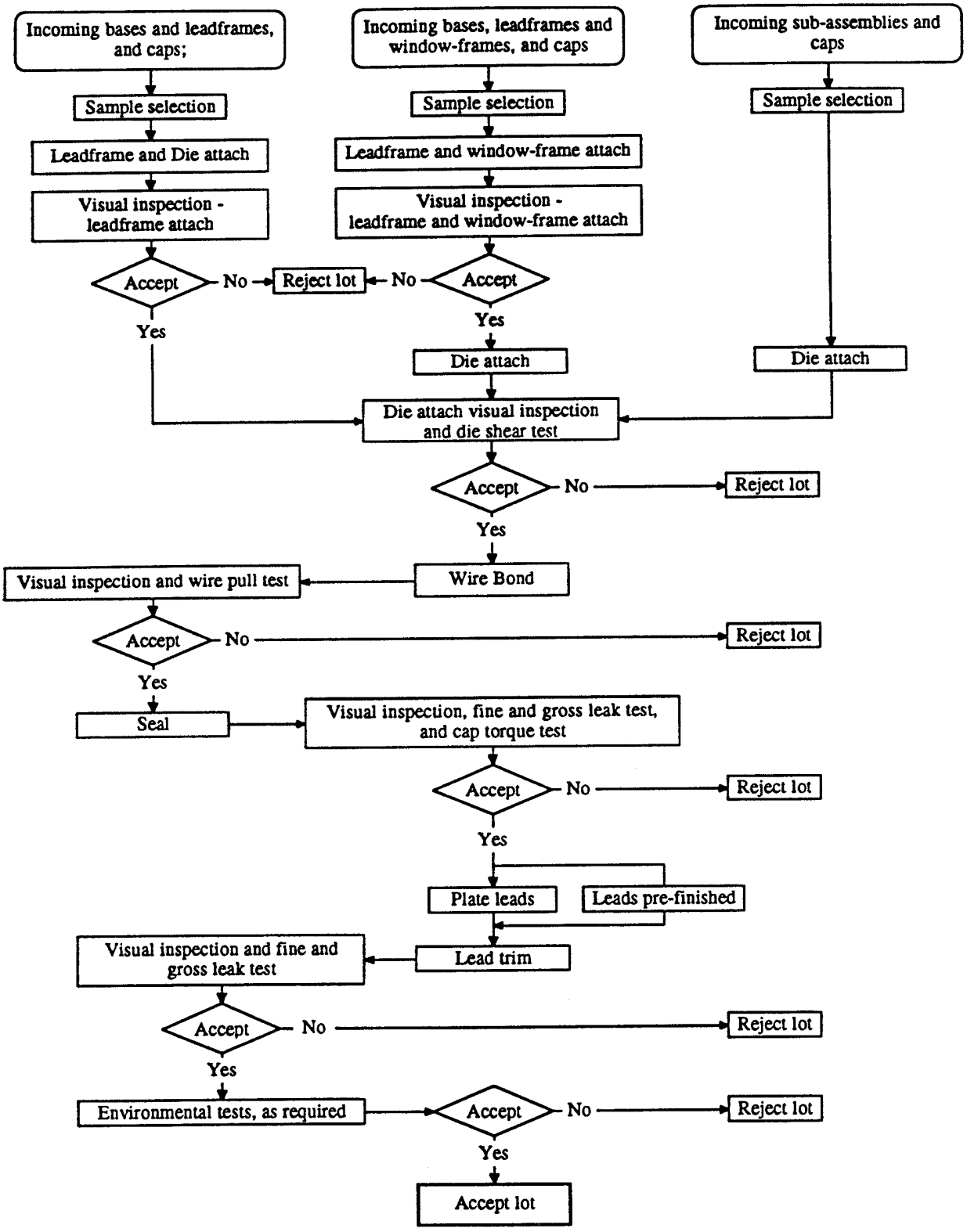
Incoming bases and leadframes, and caps;
Sample selection
Leadframe and Die attach
Visual inspection - leadframe attach
Accept
No
Reject lot
Yes
Incoming bases, leadframes and window-frames, and caps
Sample selection
Leadframe and window-frame attach
Visual inspection - leadframe and window-frame attach
No
Accept
Yes
Die attach
Incoming sub-assemblies and caps
Sample selection
Die attach
Die attach visual inspection and die shear test
Accept
No
Reject lot
Yes
Wire Bond
Visual inspection and wire pull test
Accept
No
Reject lot
Yes
Seal
Visual inspection, fine and gross leak test, and cap torque test
Accept
No
Reject lot
Yes
Plate leads
Leads pre-finished
Lead trim
Visual inspection and fine and gross leak test
Accept
No
Reject lot
Yes
Environmental tests, as required
Accept
No
Reject lot
Yes
Accept lot

Figure 8

10.2.1 *Die Attach*

10.2.1.1 *Visual Inspection*

- Eutectic Bonding — Visually inspect the alloy wet-out after die attach. The minimum wet out requirement shall be 100% of the die perimeter.
- Silver Glass or Resin Bonding — 100% die perimeter coverage shall be required.

NOTE 10: 100% coverage for silver glass or resin bonding is not a function of base acceptability but is required to standardize die shear testing. The inability of the resins to wet the surface of the die attach area due to contamination is cause for rejection.

10.2.1.2 *Die Shear Test* — Perform destructive testing in accordance with MIL-STD-883, Method 2019.

NOTE 11: Test may also be performed after environmental testing. In the case of very large die, this test may not be appropriate to fully evaluate the package. In these cases, die sizes agreed upon between user and supplier shall be used. Alternatively, die pull testing may be used by agreement between user and supplier. Inspection for die attach voids may be performed radiographically in accordance with Section 10.2.1.3 in order to ensure that the die attach process does not contribute to an incorrect evaluation of the shear or pull test results. In the case of eutectic die attach, the results from these methods may also be indicative of poor functionality of the gold die-attach metallization.

10.2.1.3 *Void Inspection* — Inspection for die-attach voids may be performed radiographically in accordance with MIL-STD-883. Method 2012 or ultrasonically in accordance with MIL-STD 883, Method 2030.

10.2.2 *Wire Bond* — On wire bonds which meet the requirements of MIL-STD-883, Method 2010, perform destructive pull testing in accordance with MIL-STD-883, Method 2011, Test Condition D.

NOTE 12: Bonds which cause lifted metallization from the lead fingers shall also be cause for rejection.

NOTE 13: This test may be performed at pre seal and post-seal.

10.2.3 *Seal*

10.2.3.1 *Visual Inspection* — The glass sealant appearance and flow shall be visually inspected for conformance to criteria agreed upon between user and supplier.

10.2.3.2 *Hermeticity* — Performed in accordance with MIL-STD-883, Method 1014, Test Condition A or B and C, the package must maintain hermetic integrity after each environmental test or sequence of tests.

NOTE 14: Internal water-vapor content may also be measured in accordance with MIL-STD-883, Method 1018.

10.2.3.3 *Cap Torque Test* — The failure criteria shall be agreed upon between user and supplier.

10.2.4 *Lead Finish* — Plate according to a process agreed upon between user and supplier.

10.2.5 *Lead Trim*

10.3 *Environmental Testing* — Environmental evaluation shall include, but not be limited to, the following tests:

NOTE 15: The sequence of testing and the sample sizes for each sub-group shall be agreed upon between user and supplier.

10.3.1 *Temperature Cycle* — In accordance with MIL-STD-883, Method 1010, Condition C.

10.3.2 *Thermal Shock* — Per MIL-STD-883, Method 1011, Condition B.

10.3.3 *Vibration Fatigue* — In accordance with MIL-STD-883, Method 2005, Test Condition B.

10.3.4 *Mechanical Shock* — In accordance with MIL-STD-883, Method 2002, Test Condition B.

10.3.5 *Constant Acceleration* — In accordance with MIL-STD-883, Method 2001, Test Condition A.

10.3.6 *Moisture Resistance* — In accordance with MIL-STD-883, Method 1004.

10.3.7 *Additional Testing* — Additional tests performed during package qualification may include evaluation of electrical and thermal characteristics, corrosion resistance and alpha particle emissions. These tests may be performed on a periodic basis to maintain package qualification. These tests may include, but are not limited to, the following:

10.3.7.1 *Insulation Resistance* — In accordance with MIL-STD-883, Method 1003, to test conditions agreed upon between user and supplier.

10.3.7.2 *Lead Inductance* — In accordance with SEMI G23 or using an impedance analyzer by a method agreed upon between user and supplier.

10.3.7.3 *Lead-to-Lead Capacitance* — Per SEMI G24.

10.3.7.4 *Lead Resistance* — Per SEMI G25.

10.3.7.5 *Junction-to-Case Thermal Resistance* — In accordance with SEMI G30 or a wind tunnel method agreed upon between user and supplier.

10.3.7.6 Alpha particle emission shall be tested by a method and to limits agreed upon between user and supplier.

10.3.7.7 *Salt Atmosphere (Corrosion) Testing* — In accordance with MIL-STD-883, Method 1009,

10.3.7.8 Condition A shall be performed to conditions agreed upon between user and supplier.

11 Sampling

The sampling plan used at incoming inspection shall be based on MIL-STD-105 and agreed upon between user and supplier (see Figure 8).

12 Packaging, Marking, and Packing List

12.1 *Packaging* — The shipping containers and materials shall be suitably designed to provide the components or sub-assemblies with protection against normal transportation damage risks which include crushing, spillage, and exposure to moisture and other corrosive gases.

The inner packaging materials must not cause particulate contamination of the components or sub-assemblies and shall be cleanroom compatible as defined by the user. The components or sub-assemblies, in packing trays, shall be vacuum-sealed in a bag with a desiccant.

12.2 *Marking*

12.2.1 *Internal Packages* — Each internal package shall be clearly marked with the following information, as appropriate:

- User's part number,
- User's purchase order number,
- Drawing number (user's and/or supplier's, as requested by user),
- Quantity, and
- Date of manufacture.

The package shall also contain any agreed upon certification data.

12.2.2 *External Packages* — The packing list on the outside of the external package shall contain the following information:

- User's part number,
- User's purchase order number,
- Quantity,
- Shipping date, and
- Any specific instructions for receiving dock personnel.

13 Certification

13.1 Upon request of the user in the contract or purchase order, a supplier's certification that the product was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment. However, if the user does perform inspection and test on a certified shipment, and the product fails to meet the requirements, the product shall be subject to rejection.

13.2 If the user and supplier agree, the product may be certified as capable of meeting this specification. In this context, capable of meeting signifies that the supplier is not required to perform all the inspections and tests. However, if the user does perform inspection and test on a certified shipment, and the product fails to meet the requirements, the product shall be subject to rejection.

APPENDIX 1
CERAMIC CERDIP BASE DIMENSIONS AND TOLERANCE REQUIREMENTS — STANDARD OUTLINES

Table 2 Ceramic Cerdip Base Dimensions and Tolerance Requirements

Lead Count	*Min. Length*	*Max. Length*	*Min. Width*	*Max. Width*	*Min. Cavity Length*	*Max. Cavity Length*	*Min. Cavity Length*	*Max. Cavity Length*	*Units*
8	0.380	0.400	0.248	0.288	0.140	0.220	0.120	0.380	in
	9.65	10.16	6.29	7.31	3.55	5.58	3.04	9.65	mm
14	0.760	0.750	0.248	0.288	0.140	0.250	0.110	0.150	in
	19.30	19.30	6.29	7.31	3.55	6.35	2.79	3.81	mm
16	0.760	0.760	0.248	0.288	0.140	0.400	0.110	0.193	in
	19.30	19.30	6.28	7.31	3.55	10.16	2.79	4.90	mm
18	0.890	0.890	0.268	0.288	0.140	0.400	0.110	0.193	in
	22.60	22.60	6.80	7.31	3.55	10.16	2.79	4.90	mm
20	0.950	0.970	0.268	0.288	0.250	0.330	0.140	0.193	in
	24.13	24.63	6.80	7.31	6.35	8.38	3.55	4.90	mm
22	1.070	1.070	0.288	0.380	0.200	0.410	0.170	0.230	in
	27.17	27.17	7.31	9.65	5.08	10.41	4.31	5.84	mm
24	1.193	1.250	0.275	0.577	0.198	0.440	0.130	0.380	in
	30.30	31.75	6.98	14.65	5.02	11.17	3.30	9.65	mm
28	1.450	1.450	0.520	0.577	0.250	0.500	0.170	0.340	in
	36.83	36.83	13.20	14.65	6.35	12.70	4.31	8.63	mm
32	1.650	1.650	0.577	0.577	0.370	0.710	0.325	0.380	in
	41.91	41.91	14.65	14.65	9.39	18.03	8.25	9.65	mm
40	2.050	2.050	0.520	0.577	0.260	0.800	0.250	0.415	in
	52.07	52.07	13.20	14.65	6.60	20.32	6.35	10.54	mm
48	2.450	2.450	0.588	0.588	0.250	0.300	0.250	0.300	in
	62.23	62.23	14.93	14.93	6.35	7.62	6.35	7.62	mm

NOTE 1: All categories in above table are min./max. tolerance requirements. In normal manufacturing specifications, tolerances and ± 1%.

NOTE 2: Ceramic body thickness range is 0.075 – 0.080 inches (1.88 - 2.03 mm).

NOTE 3: Cavity depth to be agreed upon between purchaser and supplier.

Table 3 Package Styles

Package Designation	*Definition*
LSI	Large scale integration
MSI	Medium scale integration
SD	Small (skinny) dual-in-line package
SSI	Small scale integration
SLSI	Super large scale integration
VLSI	Very large scale integration

APPENDIX 2
CERAMIC CERDIP CAP DIMENSIONS AND TOLERANCE REQUIREMENTS — STANDARD OUTLINES

Table 4 Ceramic Cerdip Cap Dimensions and Tolerance Requirements

Description	*Body Length*	*Body Width*	*Thickness* Min.	Max.	*Cavity Length*	*Cavity Width*	*Cavity Depth (Measured at Cavity Bottom)*	*Units*
8SSI	0.380 ± 0.004	0.248 ± 0.003	0.050	0.055	0.260 ± 0.004	0.157 ± 0.003	0.018 ± 0.003	in
	9.65 ± 0.102	6.30 ± 0.076	1.27	1.40	6.60 ± 0.102	6.60 ± 0.102	3.99 ± 0.076	mm
8LSI	0.380 ± 0.004	0.288 ± 0.003	0.050	0.055	0.260 ± 0.004	0.185 ± 0.003	0.018 ± 0.003	in
	9.65 ± 0.012	7.32 ± 0.076	1.27	1.40	6.60 ± 0.102	4.70 ± 0.076	0.457 ± 0.076	mm
14/16SSI	0.760 ± 0.007	0.248 ± 0.004	0.050	0.055	0.350 ± 0.004	0.157 ± 0.003	0.018 ± 0.003	in
	19.30 ± 0.178	6.81 ± 0.076	1.27	1.40	8.89 ± 0.102	4.32 ± 0.076	0.457 ± 0.076	mm
16SLI/VLSI	0.760 ± 0.007	0.288 ± 0.003	0.050	0.055	0.450 ± 0.005	0.195 ± 0.003	0.018 ± 0.003	in
	19.30 ± 0.178	7.32 ± 0.076	1.27	1.40	10.67 ± 0.127	4.95 ± 0.076	0.457 ± 0.076	mm
18MSI	0.890 ± 0.008	0.268 ± 0.003	0.050	0.055	0.350 ± 0.004	0.170 ± 0.003	0.018 ± 0.003	in
	22.61 ± 0.203	6.81 ± 0.076	1.27	1.40	8.89 ± 0.102	4.32 ± 0.076	0.457 ± 0.076	mm
18LSI	0.890 ± 0.008	0.288 ± 0.003	0.050	0.055	0.350 ± 0.004	0.185 ± 0.003	0.018 ± 0.003	in
	22.61 ± 0.203	7.32 ± 0.076	1.27	1.40	8.89 ± 0.102	4.70 ± 0.076	0.457 ± 0.076	mm
18VLSI	0.890 ± 0.008	0.288 ± 0.003	0.050	0.055	0.420 ± 0.004	0.195 ± 0.003	0.018 ± 0.003	in
	22.61 ± 0.203	7.32 ± 0.076	1.27	1.40	10.67 ± 0.102	4.95 ± 0.076	0.457 ± 0.076	mm
20MSI	0.950 ± 0.010	0.268 ± 0.003	0.050 ± 0.055		0.300 ± 0.004	0.170 ± 0.003	0.018 ± 0.003	in
	24.13 ± 0.254	6.81 ± 0.076	1.27	1.40	7.62 ± 0.102	4.32 ± 0.076	4.57 ± 0.076	mm
20LSI/VLSI	0.950 ± 0.010	0.288 ± 0.003	0.050	0.055	0.380 ± 0.004	0.190 ± 0.003	0.018 ± 0.003	in
	24.13 ± 0.254	7.32 ± 0.076	1.27	1.40	9.65 ± 0.102	4.83 ± 0.076	0.457 ± 0.076	mm
22MSI/LSI/VLSI	1.070 ± 0.010	0.380 ± 0.004	0.050	0.055	0.370 ± 0.005	0.275 ± 0.004	0.018 ± 0.003	in
	27.17 ± 0.254	9.65 ± 0.102	1.27	1.40	9.40 ± 0.127	6.99 ± 0.102	0.457 ± 0.076	mm
24MSI/LSI	1.250 ± 0.010	0.520 ± 0.006	0.050	0.055	0.400 ± 0.005	0.330 ± 0.005	0.018 ± 0.003	in
	31.75 ± 0.254	13.21 ± 0.152	1.27	1.40	10.16 ± 0.127	8.38 ± 0.127	0.457 ± 0.076	mm
24VLSI	1.250 ± 0.010	0.577 ± 0.006	0.050	0.056	0.560 ± 0.006	0.380 ± 0.005	0.018 ± 0.003	in
	31.75 ± 0.254	14.65 ± 0.152	1.27	1.42	14.22 ± 0.152	9.65 ± 0.127	0.457 ± 0.076	mm
24SD3S	1.250 ± 0.010	0.288 ± 0.003	0.050	0.055	0.350 ± 0.004	0.190 ± 0.003	0.018 ± 0.003	in
	31.75 ± 0.254	7.32 ± 0.076	1.27	1.40	8.89 ± 0.102	4.83 ± 0.076	0.457 ± 0.076	mm
24SD3M	1.250 ± 0.010	0.288 ± 0.003	0.050	0.055	0.490 ± 0.005	0.195 ± 0.003	0.018 ± 0.003	in
	31.75 ± 0.254	7.32 ± 0.076	1.27	1.40	12.45 ± 0.127	4.95 ± 0.076	0.457 ± 0.076	mm
24SD4M	1.250 ± 0.010	0.380 ± 0.004	0.050	0.055	0.235 ± 0.004	0.235 ± 0.004	0.018 ± 0.003	in
	31.75 ± 0.254	9.65 ± 0.102	1.27	1.40	5.97 ± 0.102	5.97 ± 0.102	0.457 ± 0.076	mm
28MSI/LSI	1.450 ± 0.010	0.520 ± 0.006	0.050	0.055	0.400 ± 0.005	0.330 ± 0.005	0.018 ± 0.003	in
	36.83 ± 0.254	13.21 ± 0.152	1.27	1.40	10.16 ± 0.127	8.38 ± 0.127	0.457 ± 0.076	mm
28VLSI	1.450 ± 0.010	0.577 ± 0.006	0.050	0.056	0.560 ± 0.005	0.380 ± 0.005	0.018 ± 0.003	in
	36.83 ± 0.254	14.65 ± 0.152	1.27	1.42	14.22 ± 0.127	9.65 ± 0.127	0.457 ± 0.076	mm
40 MSI/LSI	2.050 ± 0.012	0.520 ± 0.006	0.050	0.055	0.475 ± 0.005	0.365 ± 0.005	0.018 ± 0.003	in
	52.07 ± 0.305	13.21 ± 0.152	1.27	1.40	12.07 ± 0.127	9.27 ± 0.127	0.457 ± 0.076	mm
48MSI	2.450 ± 0.015	0.577 ± 0.006	0.050	0.056	0.400 ± 0.005	0.400 ± 0.005	0.018 ± 0.003	in
	14.65 ± 0.152	14.65 ± 0.152	1.27	1.42	10.16 ± 0.127	10.16 ± 0.127	0.457 ± 0.076	mm

NOTICE: These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI G2-94
SPECIFICATION FOR METALLIC LEADFRAMES FOR CER-DIP PACKAGES

1 Preface

1.1 *Purpose* — This specification defines the materials and dimensions for the metallic leadframe (stamped or etched) used in the construction of Cer-DIP Package.

1.2 *Scope* — The criteria detailed in this document applies to the iron-nickel leadframe (MIL-M-38510 Type A or Type B) used in Cer-DIP packages.

1.3 *Units* — U.S. Customary (inch-pound) or metric (SI) units may be used at the customer's discretion. This specification uses the U.S. Customary units as the prime unit.

2 Referenced Documents[1]

2.1 This document specifically refers to:

MIL-I-23011 — Iron/Nickel Alloys for Sealing to Glasses and Ceramics

MIL-M-38510 — General Specifications for Microcircuits

MIL-STD-883 — Test Methods and Procedures for Microelectronics

2.2 Related information may also be found in:

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

3 Terminology

bonding area — Coined area on bond fingers within a distance of 0.762 mm (0.030") from lead tips.

bottom formed width — See Figure 3.

bow — Curvature of the leadframe strip in the vertical plane; see Figure 1.

burr — Fragment of excess parent material attached to the leadframe edges.

camber — Curvature of the leadframe strip edge in the horizontal plane; see Figure 2.

coined area — The area of the bond fingers planished to produce a flattened area for functional use; see Figure 3.

coplanarity — The total indicator reading difference of the lead tips in the Z direction.

datum plane — M is datum plane; see Figure 3.

discoloration — A darkening or staining of the aluminum (metallization).

foreign material — Any adhering residue which is not part of the leadframe composition.

pit — A shallow surface depression or crater with a visible edge.

planarity — Total indicator reading of the lead tips in the Z direction relative to datum M.

projection — A raised portion of the surface indigenous with the parent material, other than a burr.

slug marks — Random dents in the leadframe.

stamped leadframe terminology — See Figure 3.

tilt — The deviation of the plane of the coined area from a condition parallel to the plane on datum M.

top formed width — See Figure 3.

twist — The angular rotation of one end of the leadframe or strip with reference to the other end; see Figure 4.

void — An absence of aluminization from a designated area of the leadframe.

4 Ordering Information

Purchase order for Cer-DIP metallic leadframes furnished to this specification shall include the following items:

4.1 Current drawing of the leadframe showing all dimensions and tolerances, including the location of the metallization layer.

4.2 Material,

4.3 Number of leads,

4.4 Material tensile strength,

4.5 Metallization thickness and type,

4.6 Form of leadframes (i.e., singles, scored strips, or unscored strips),

4.7 Number of frames per strip; as applicable,

4.8 Material certification,

4.9 Packaging and marking.

1 Military Standards, Naval Publications and Form Center, 5801 Tabor Ave., Philadelphia, PA 19120

5 Dimensions

All Dimensioning and tolerancing shall conform to Y14.5. Table 1 presents standard leadframe dimensions.

6 Materials

6.1 *Leadframe Base Material* — Tensile strength shall be specified per MIL-I-23011.

6.1.1 *Chemical Composition* — Shall conform to the requirements of MIL-M-385l0, Type A or B.

6.1.2 *Material Tensile Strength* — Shall be supplied per MIL-I-23011.

6.2 *Metallization* — Aluminum

6.2.1 *Thickness* — 100 microinches minimum, 600 microinches maximum (micromin, micromaximum).

6.2.2 *Coverage* — 0.030" (0.762 mm) minimum; measured from lead tip. Maximum to be determined by ceramic size.

6.2.3 *Composition*

6.2.3.1 *Clad Material* — 99.4% minimum aluminum.

6.2.3.2 *Vapor Deposition* — 99.9% minimum aluminum.

NOTE: The two types of aluminum may exhibit different visual appearances and non-functional characteristics after processing.

7 Defect Limits

7.1 *Burrs*

7.1.1 *Horizontal*

7.1.1.1 *Bonding Area* — 0.001" (0.025 mm) max.

7.1.1.2 *Other Areas* — 0.002" (0.051 mm) max.

7.1.2 *Vertical*

7.1.2.1 *Bonding Area* — 0.001" (0.025 mm) max.

7.1.2.2 *Other Areas* — 0.002" (0.051 mm) max.

7.2 *Planarity/Coplanarity* — Shall not exceed the limits shown in Table 2.

7.3 *Foreign Materials* — Leadframes shall be clean and free from foreign material such as photoresist, lubricants, solvent residue, water marks, and rust spots. Protective coatings acceptable to both vendor and user are not considered foreign material.

7.4 *Pits and Slug Marks*

7.4.1.1 *Bonding Area* — 0.001" (0.025 mm) max. surface dimension × 0.0005" (0.013 mm) maximum depth.

7.4.1.2 *Other Areas* — 0.010" (0.254 mm) max. surface dimension × 0.0005" (0.013 mm) maximum depth.

7.5 *Projections*

7.5.1 *Bonding Area* — None allowed.

7.5.2 *Other Areas* — .010" (.254 mm) max. surface dimension × 0.002" (0.015 mm) maximum height.

7.6 *Scratches* — There shall be no scratches in the aluminum metallization that penetrate to the underlying base material.

7.7 *Voids* — All metallized areas of the leadframe within the bonding area shall have no voids larger than 0.001" (0.025 mm) in any dimension.

7.8 *Twist* (formed leadframe strip) — 0.004 inch per inch (0.102 mm).

7.9 *Coining*

7.9.1 *Coined Depth* — Minimum 0.0005" (0.013 mm); maximum 0.002" (0.051 mm). Minimum coined depth may be controlled by minimum flat area.

7.9.2 *Coined Flat Area* — Minimum of 80% of normal lead width; measured 0.005" (0.127 mm) back from lead tip.

7.9.3 *Coined Length* — Minimum 0.025" (0.635 mm) from lead tip.

7.10 *Lead Position*

7.10.1 *Lead Position* — A 0.007" (0.178 mm) diameter circle must be 100% within nominal lead position when centered at lead nominal centerline and 0.007" (0.178 mm) back from lead tip.

7.10.2 *Minimum Spacing* — 0.006" (0.152 mm) minimum.

7.11 *Bowing*

7.11.1 *Convex* — 0.0025 inch per inch (0.0025 mm per mm) maximum.

7.11.2 *Concave* — 0.0025 inch per inch (0.0025 mm per mm) maximum.

7.12 *Camber* — 0.005 inch per inch (0.005 mm per mm) maximum.

NOTE: Items 7.11 and 7.12 refer to scored strips only.

8 Sampling

Sampling will be determined between vendor and customer.

9 Test Methods

9.1 *Sequence of Events and Tests*

The sequence of testing should be:

9.1.1 Degrease

9.1.2 Metallurgical Bond Adhesion (Section 9.3.1)

9.1.3 Frame Attach

9.1.4 Die Attach

9.1.5 Bond

9.1.6 Pre-Seal Bond Pull (Section 9.3.2)

9.1.7 Seal

9.1.8 Mechanical Testing (Section 9.2)

9.1.9 Lead Trim

9.1.10 Post-Seal Bond Pull (Section 9.3.2)

NOTE: It is acknowledged that the leadframe manufacturer may not perform all these tests due to equipment and component limitations. Regardless, leadframes must fulfill these requirements, subject to the influence of the testing facility and associated components.

9.2 *Mechanical and Thermal*

9.2.1 *Temperature Cycling* — Per MIL-STD-883, Method 1010.4, Condition C.

9.2.2 *Thermal Shock* — Per MIL-STD-883, Method 1011.2, Condition C.

9.2.3 *Centrifuge* — Per MIL-STD-883, Method 2001.2, Condition E.

9.2.4 *Lead Integrity*

9.2.4.1 A 500°C ± 20° - 55% R.H. heat soak for 15 minutes ± 1 minute. Cooled at no more than 50°C per minute. Afterwards the frame is clamped between plates of a suitable size for the lead spacing (see Section 9.2.4.2). Then (3) 90° cycles are performed. Frames are examined at 20× magnification and if cracks are observed at the Apex A (Figure 3), then the frame is rejected.

9.2.4.2 Plate shall be of equivalent plan-form to the ceramic being employed for the particular frame. An edge radius equivalent to 2T, where T is the leadframe thickness, shall be on the contacting surface of the plate.

9.3 *Functional Test Methods*

9.3.1 *Metallurgical Bond Adhesion Aluminization* — The metallurgical bond between the aluminization and the base metal shall permit the leadframe to be heated in air to 525°C ± 10°C for five (5) minutes minimum without evidence of aluminum peeling, blistering, or discoloring when viewed at 20× magnification. (Discoloration must not jeopardize the user's standard part reliability.) Subsequently, the aluminized layer must pass the following two adhesion tests:

9.3.1.1 A cellophane type adhesive tape is firmly applied to the aluminization and removed toward the center of the cavity in a continuous rapid motion. This test is to be performed over the same area three times. No evidence of aluminum separation from the base metal shall be visible at 20× magnification

9.3.1.2 The aluminization shall be capable of passing a functional wirebond test without separating.

9.3.2 *Lead Bond Quality* — Minimum pre-seal and post-seal bond strength test per MIL-STD-883, Method 2011.2, Test Condition D. Applicable failure categories: A-4 and A-6.

10 Packaging and Marking

10.1 *Packaging* — The shipping containers and materials shall be suitably designed to provide the singulated components with protection against normal transportation damage risks which include crushing, abrasion and spillage, and exposure to moisture and other corrosive gases. The inner packing materials must not cause particulate contamination on the components and shall be clean-room compatible as defined by the customer. The components, in packing trays, shall be sealed in a vacuum bag with a dessicant.

10.2 *Packing List*

10.2.1 *Internal Packages* — Each internal package shall be marked as follows:

User Part Number

User Purchase Order Number

Drawing Number (User's and Supplier's, if appropriate)

Supplier Shipping Lot Number

Quantity

Date of Manufacture

10.2.2 *External Packages* — The Packing List, located on the outside of the container, shall provide the following information:

User's Part Number

User's Purchase Order Number

Quantity

Shipping Date

Any specific instructions for receiving dock personnel.

Table 1 Typical Ceramic Cer-DIP Metallic Leadframes Dimension and Tolerance Requirements

Description	*Cavity Length*	*Cavity Width*	*Lead-Formed Width, Top*	*Bond Finger Layout End vs. Side*		*Nominal Progression*	*Unit*
8SSI	-	0.120 ± 0.007	0.311 ± 0.003	0	4	0.945	in
		3.05 ± 0.178	7.90 ± 0.076			24.00	mm
8MSI	-	0.140 ± 0.007	0.311 ± 0.003	0	4	0.945	in
		3.56 ± 0.178	7.90 ± 0.076			24.00	mm
8LSI	-	0.160 ± 0.007	0.311 ± 0.003	0	4	0.945	in
		4.06 ± 0.178	7.90 ± 0.076			24.00	mm
14SSI	0.160 ± 0.007	0.120 ± 0.007	0.311 ± 0.003	4	3	0.945	in
	4.06 ± 0.178	3.05 ± 0.178	7.90 ± 0.076			24.00	mm
14MSI	0.260 ± 0.007	0.140 ± 0.007	0.311 ± 0.003	4	3	0.945	in
	6.60 ± 0.178	3.56 ± 0.178	7.90 ± 0.076			24.00	mm
16SSI	0.160 ± 0.007	0.120 ± 0.007	0.311 ± 0.003	4	4	0.945	in
	4.06 ± 0.178	3.05 ± 0.178	7.90 ± 0.076			24.00	mm
16MSI	0.260 ± 0.007	0.140 ± 0.007	0.311 ± 0.003	4	4	0.945	in
	6.60 ± 0.178	3.56 ± 0.178	7.90 ± 0.076			24.00	mm
16LSI	0.260 ± 0.007	0.170 ± 0.007	0.311 ± 0.003	4	4	0.945	in
	6.60 ± 0.178	4.32 ± 0.178	7.90 ± 0.076			24.00	mm
16SLSI	0.360 ± 0.007	0.170 ± 0.007	0.311 ± 0.003	4	4	0.945	in
	9.14 ± 0.178	4.32 ± 0.178	7.90 ± 0.076			24.00	mm
16VLSI	0.330 ± 0.007	0.180 ± 0.007	0.311 ± 0.003	6	2	0.945	in
	8.38 ± 0.178	4.57 ± 0.178	7.90 ± 0.076			24.00	mm
18MSI	0.260 ± 0.008	0.140 ± 0.008	0.311 ± 0.003	4	5	1.061	in
	6.60 ± 0.203	3.56 ± 0.203	7.90 ± 0.076			26.95	mm
18LSI	0.260 ± 0.008	0.170 ± 0.008	0.311 ± 0.003	6	3	1.061	in
	6.60 ± 0.203	4.32 ± 0.203	7.90 ± 0.076			26.95	mm
18VLSI	0.330 ± 0.008	0.180 ± 0.008	0.311 ± 0.003	6	3	1.061	in
	8.38 ± 0.203	4.57 ± 0.203	7.90 ± 0.076			26.95	mm
20MSI	0.210 ± 0.008	0.140 ± 0.008	0.311 ± 0.003	4	6	1.175	in
	5.33 ± 0.203	3.56 ± 0.203	7.90 ± 0.076			29.85	mm
20LSI	0.260 ± 0.008	0.170 ± 0.008	0.311 ± 0.003	6	4	1.175	in
	6.60 ± 0.203	4.32 ± 0.203	7.90 ± 0.076			29.85	mm
20VLSI	0.330 ± 0.008	0.175 ± 0.008	0.311 ± 0.003	6	4	1.175	in
	8.38 ± 0.203	4.45 ± 0.203	7.90 ± 0.076			29.85	mm
22MSI	0.270 ± 0.010	2.10 ± 0.010	0.411 ± 0.003	6	5	1.250	in
	6.86 ± 0.254	5.33 ± 0.254	10.44 ± 0.076			31.75	mm
22LSI	0.310 ± 0.010	0.240 ± 0.010	0.411 ± 0.003	6	5	1.250	in
	7.87 ± 0.254	6.10 ± 0.254	10.44 ± 0.076			31.75	mm
22VLSI	0.350 ± 0.010	0.260 ± 0.010	0.411 ± 0.003	8	3	1.250	in
	8.89 ± 0.254	6.60 ± 0.254	10.44 ± 0.076			31.75	mm
24MSI	0.260 ± 0.010	0.260 ± 0.010	0.611 ± 0.003	6	6	1.510	in
	8.38 ± 0.254	6.60 ± 0.254	15.01 ± 0.076			38.35	mm
24LSI	0.330 ± 0.010	0.285 ± 0.010	0.611 ± 0.003	6	6	1.510	in
	8.38 ± 0.254	7.24 ± 0.254	15.01 ± 0.076			38.35	mm
24VLSI	0.420 ± 0.010	0.290 ± 0.010	0.611 ± 0.003	6	6	1.510	in
	10.67 ± 0.254	7.37 ± 0.254	15.01 ± 0.076			38.35	mm
24SD3S	0.260 ± 0.010	0.170 ± 0.010	0.311 ± 0.003	6	6	1.510	in
	6.60 ± 0.254	4.32 ± 0.254	7.90 ± 0.076			38.35	mm

Description	*Cavity Length*	*Cavity Width*	*Lead-Formed Width, Top*	*Bond Finger Layout End vs. Side*		*Nominal Progression*	*Unit*
24SD3M	0.430 ± 0.010	0.180 ± 0.010	0.311 ± 0.003	8	4	1.510	in
	10.92 ± 0.254	4.57 ± 0.254	7.90 ± 0.076			38.35	mm
24SD4M	0.210 ± 0.010	0.210 ± 0.010	0.411 ± 0.003	6	6	1.510	in
	5.33 ± 0.254	5.33 ± 0.254	10.44 ± 0.076			38.35	mm
28MSI	0.260 ± 0.011	0.260 ± 0.011	0.611 ± 0.003	8	6	1.724	in
	6.60 ± 0.279	6.60 ± 0.279	15.01 ± 0.076			43.79	mm
28LSI	0.325 ± 0.011	0.275 ± 0.011	0.611 ± 0.003	8	6	1.724	in
	8.26 ± 0.279	6.99 ± 0.279	15.01 ± 0.076			43.79	mm
28VLSI	0.420 ± 0.011	0.280 ± 0.011	0.611 ± 0.003	8	6	1.724	in
	10.67 ± 0.279	7.11 ± 0.279	15.01 ± 0.076			43.79	mm
40MSI	0.270 ± 0.012	0.260 ± 0.012	0.611 ± 0.003	10	10	2.300	in
	6.86 ± 0.305	6.60 ± 0.305	15.01 ± 0.076			58.42	mm
40LSI	0.375 ± 0.012	0.295 ± 0.012	0.611 ± 0.003	12	8	2.300	in
	9.53 ± 0.305	7.49 ± 0.305	15.01 ± 0.076			58.42	mm

NOTE: While a 0.311 top form is still currently being used, numerous users have changed to a 0.314 top form to prevent interference between the Cer-DIP base and leadframe.

Table 2

Leads	*Planarity*		*Coplanarity*
8–14–16	+0.003"/–0.004"	(+ 0.076 mm/–0.102 mm)	0.004" (0.102 mm)
18	+0.004"/–0.005"	(+0.102 mm/–0.127 mm)	0.005" (0.127 mm)
20	+0.004"/–0.005"	(+0.102 mm/–0.127 mm)	0.006" (0.152 mm)
22	+0.004"/–0.006"	(+0.102 mm/–0.152 mm)	0.006" (0.152 mm)
24	+0.004"/–0.006"	(+0.102 mm/–0.152 mm)	0.007" (0.178 mm)
28	+0.005"/–0.007"	(+0.127 mm/–0.178 mm)	0.008" (0.203 mm)
40	+0.006"/–0.008"	(+0.152 mm/–0.203 mm)	0.010" (0.254 mm)

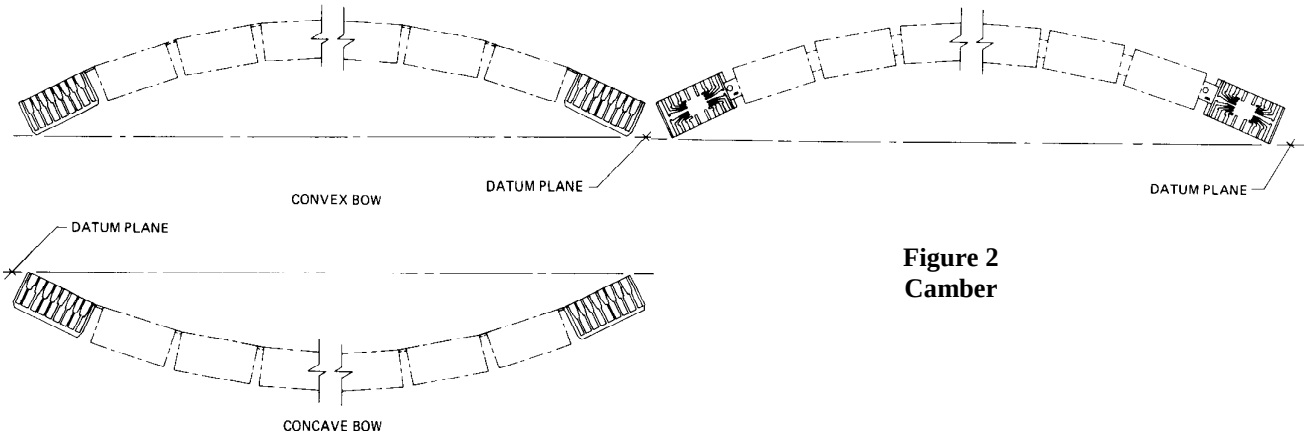

Figure 1
Bow

Figure 2
Camber

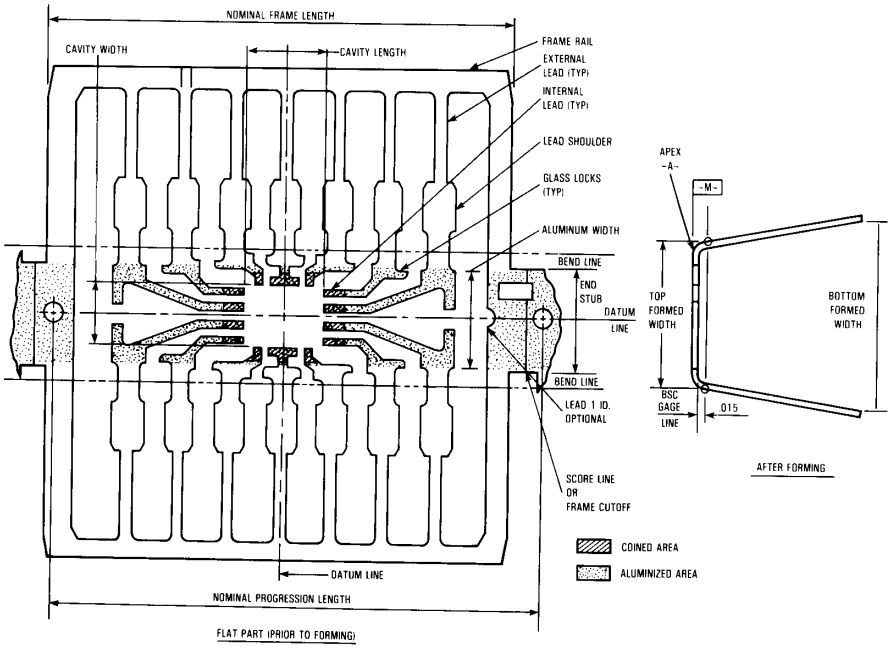

Figure 3
Stamped Leadframe Terminology

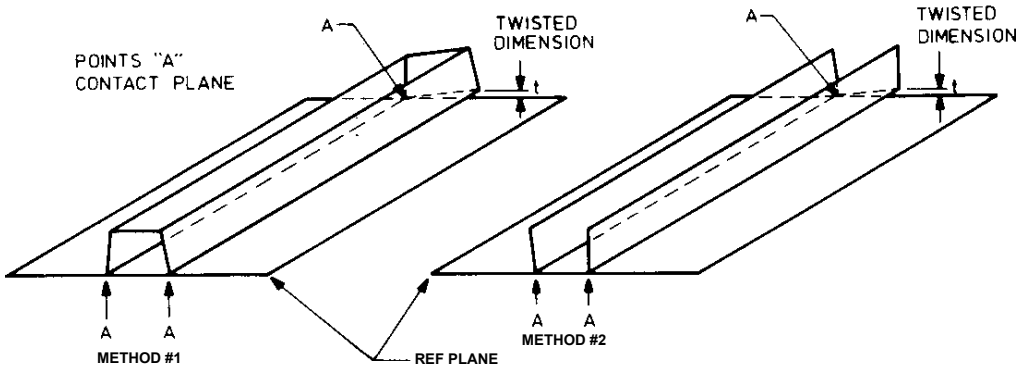

Figure 4
Twist Strip

Using surface plate, establish a reference plane the whole length of the frame strip. Place frame strip, either method 1 or 2, whichever method gives a 3 point contact with reference plane A, using thickness gauges to determine height between reference plane and 4th point noted as t. This measurement will determine frame twist over entire length.

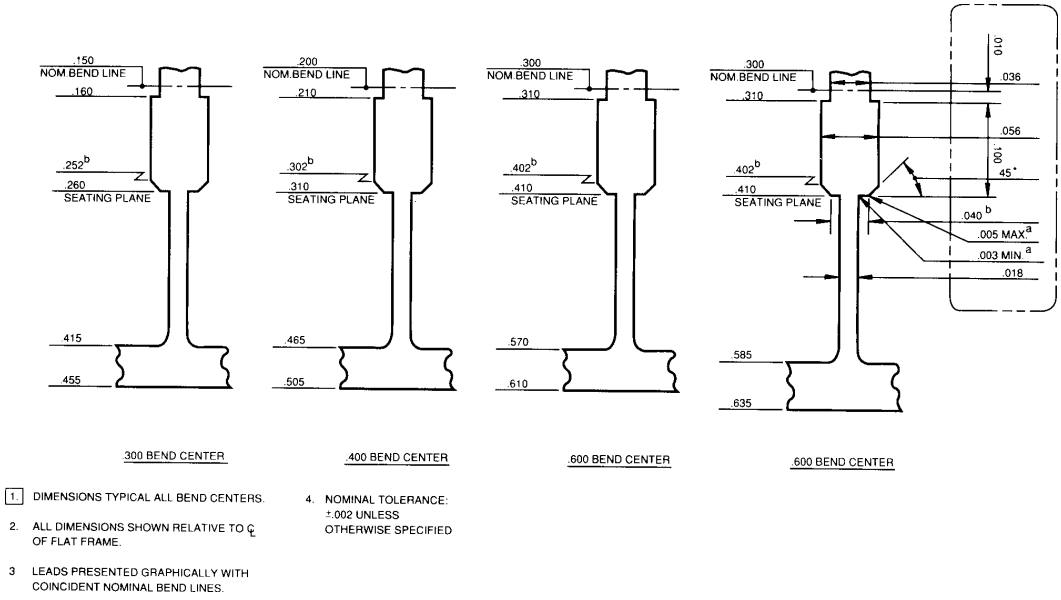

Figure 5
Standoff Lead Length

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SEMI G3-90
SPECIFICATION FOR SIDEBRAZED LAMINATES

1 Preface

This specification covers laminated ceramic sidebrazed packages of 7.62 mm (0.003"), 10.16 mm (0.400"), 15.24 mm (0.600") and 22.86 mm (0.900") nominal widths. The leadframe which is brazed to this type of package is included in this specification.

2 Applicable Documents[1]

2.1 This following applicable documents, of the revision currently in effect, are part of this specification to the extent referenced herein.

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-G-45204 — Gold Plating, Electro-Deposited

MIL-M-38510 — General Specification for Microcircuits

3 Selected Definitions

burr — An adherent fragment of excess parent material at the component edge.

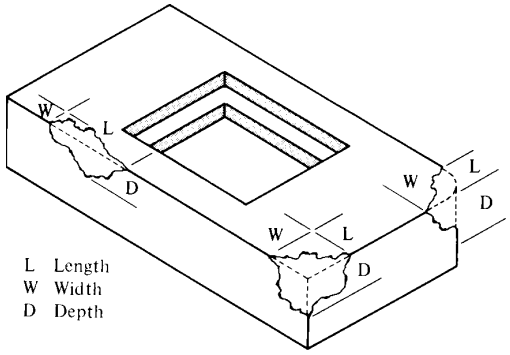
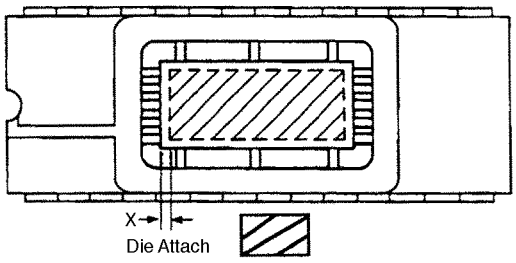


Figure 1
Chip Illustration

chip — A region of ceramic missing from the surface or edge of a package which does not go completely through the package. Chip size is given by its length, width and depth from a projection of the design plan-form. (See Figure 1.)

crack — A cleavage or fracture that extends to the surface of a package. It may or may not pass through the entire thickness of the package.

die attach surface — See Figure 2.



Package Row Spacing			
7.62 mm (.300")	10.16 mm (.400")	15.24 mm (.600")	22.86 mm (.900")
X = .203 mm (.008")	X = .254 mm (.010")	X = .381 mm (.015")	X = .508 mm (.020")

Figure 2
Die Attach Surface

discoloration — Any change in the color of the package plating as detected by the unaided eye after the application of heat per Section 9.1.1.

foreign material — An adherent particle other than parent material of that component.

LSI — Large scale integration.

layer — A ceramic or metallized layer that performs a discrete function as a part of the package. Should a layer be comprised of more than one ceramic laminate, all of those laminates shall be considered as comprising one layer if all are common in both plan-form and function. Leadframes shall not be considered as layers.

MSI — Medium scale integration.

projection — An adherent fragment of excess material on the component surface.

pullback — The linear distance between the edge of the ceramic and the first measurable metallization interface. (See Figure 3.)

rundown — See Figure 3.

1 Military Standards, Naval Publications and Form Center, 5801 Tabor Ave., Philadelphia, PA 19120

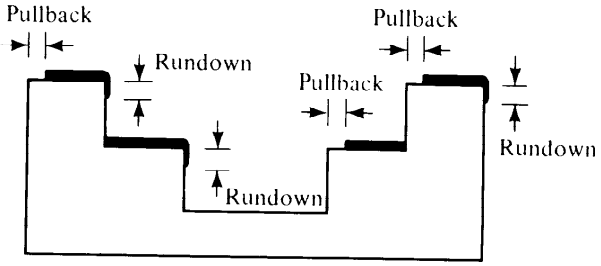


Figure 3
Metallization Misalignment

SSI — Small scale integration.

seal area — A dimensional outline area designated for either metallization or bare ceramic to provide a surface area for sealing. (See Figure 4.)

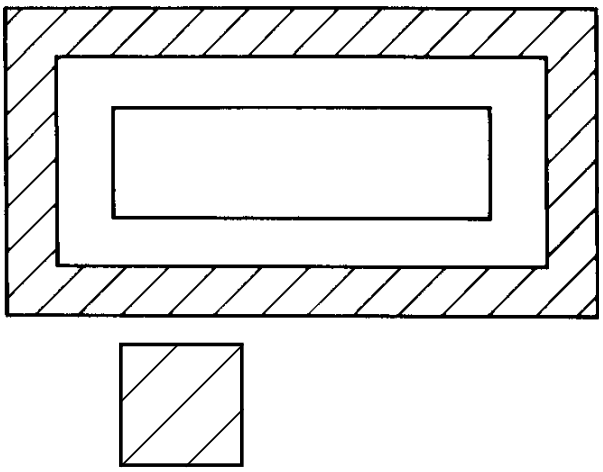
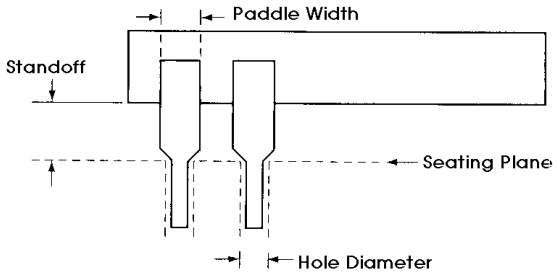


Figure 4
Seal Area

seating plane — See Figure 5.

standoff — Residual air gap after inserting the leads into a ground steel plate with a specific size hole and applying a specified downward pressure. (See Figure 5.)



NOTE: When determining the seating plane a downward of 10 grams is to be applied to the package.

Figure 5
Leadframe Paddle Width and Standoff

TIR — Total indicator reading.

VLSI — Very large scale integration.

void — An absence of metallization or plating from a designated area.

4 Ordering Information

Purchase orders for sidebrazed laminated packages furnished to this specification shall include the following items:

1. Drawing number and revision level
2. Number of leads and lead series spacing
3. Type and color of ceramic
4. Type and thickness of plating
5. Description (See Table 1.)
6. Thickness of individual layers of ceramic
7. Internal finger bonding pattern layout
8. Minimum exposed metallized bond finger length and width
9. Leads common to die attach area and/or seal ring
10. Sealing dimensions and flatness
11. Certification
12. Method of test and measurements (See Section 9.)
13. Lot acceptance procedures (See Section 8.)
14. Packaging and Marking (See Section 10.)

5 Dimensions and Permissible Variations

The dimensions of the sidebraze laminate packages shall conform as specified in Table 1.

6 Materials

6.1 *Ceramic*

6.1.1 Alumina content 90% minimum.

6.1.2 *Color* — Opaque or white.

6.2 *Metallization*

6.2.1 Refractory metallization (provide adequate bond strength to ceramic).

6.2.2 Nickel plating (if designated).

6.2.3 Precious or noble metal plating.

6.2.4 Nickel/gold per MIL-M-38510 except gold plating shall conform to MIL-G-45204, Type III and have a thickness of 60 microinches minimum.

6.3 *Braze Material* — An alloy with a melting point equal to or greater than 750°C which will provide specified bond strength of the lead to the ceramic.

6.4 *Lead Material*

6.4.1 Iron nickel cobalt alloy per MIL-M-38510, Type A.

6.4.2 Iron nickel alloy per MIL-M-38510, Type B.

7 Defect Limits

7.1 *Ceramic*

7.1.1 *Cracks* — None allowed.

7.1.2 *Chips*

7.1.2.1 *Corner* — 0.762 mm (0.030") × 0.762 mm (0.030") × 0.762 mm (0.030") max.

7.1.2.2 *Edge* — 2.54 mm (0.100") × 0.762 mm (0.030") × 0.762 mm (0.030") max. (Chips can not be encroached or exposed any metallized area.)

7.1.2.3 *Seal Area*

7.1.2.3.1 7.62 mm (0.300") and 10.16 mm (0.400") Row Spacing Parts — .762 mm (0.030") × 2.54 mm (0.100")

7.1.2.3.2 *15.24 mm (0.600") Row Spacing Parts* — 1.27 mm (0.050") × 0.381 mm (0.015") × 0.381 mm (0.015") max.

7.1.2.3.3 *22.86 mm (0.900") Rowing Spacing Parts* — 1.52 mm (0.060") × 0.508 mm (0.020") × 0.508 mm (0.020") max.

7.1.2.3.4 Chips cannot reduce the seal width by more than 1/3 of the design width.

7.1.3 *Burrs and Projections*

7.1.3.1 *Top Plane Excluding Seal Area* — 0.102 mm (0.004") max.

7.1.3.2 *Seal Area* — 0.025 mm (0.001") max. above metallization.

7.1.3.3 *Wire Bond Finger Areas* — 0.025 mm (0.001") max. above metallization.

7.1.3.4 *Die Attach Surface* — 0.025 mm (0.001") max. above metallization excluding a 0.203 mm (0.008") perimeter on 7.62 mm (0.300") centerline packages, 0.254 mm (0.010") perimeter on 10.16 mm (0.400") centerline packages and 0.381 mm (0.015") perimeter on 15.24 mm (0.600") centerline packages, 0.508 mm (0.020") perimeter on 22.86 mm (0.900") row center package.

7.1.4 *Camber* — Ceramic-maximum of 0.004 inch/inch (mm/mm).

7.1.5 *Flatness*

7.1.5.1 *Seal Area* — 0.050 mm (0.002") TIR on 7.62 mm (0.300") row center packages, 0.0635 mm (0.0025") TIR on 10.16 mm (0.400") and 15.24 mm (0.600") row center packages.

7.1.5.2 *Die Attach* — Die attach pad to be flat to within 0.051 mm (0.002") TIR to exclude a 0.203 mm (0.008") perimeter on 7.62 mm (0.300") centerline packages, 0.254 mm (0.010") perimeter on 10.16 mm (0.400") centerline packages and 0.381 mm (0.015") perimeter on 15.24 mm (0.600") centerline packages.

7.2 *Metallization*

7.2.1 *Voids*

7.2.1.1 *Seal Area* — On the outer half of the seal area width, maximum of 3 voids no larger than 0.127 mm (0.005") in diameter are permissible. On the inner half, maximum of 3 voids no larger than 0.381 mm (0.015") in diameter or larger than 1/3 of the seal area width, whichever is the smaller. The distance between any 2 voids shall be at least 0.762 mm (0.030").

7.2.1.2 *Wire Bond Fingers* — A 0.254 mm (0.010") × 0.010" (0.254 mm) void free area within the specified wire bond finger area as defined be the procurement drawing.

7.2.1.3 *Die Attach Surface* — Maximum 0.010" (0.254 mm) diameter by a distance greater than 0.030" (0.762 mm) with no more than 3 voids.

7.2.2 *Metallization Misalignment* — See Figure 3.

7.2.2.1 *Seal Plane Rundown* — Internal cavity — not to exceed 25% of the cavity layer thickness. External cavity — not to be less than 0.010" (0.254 mm) outside the cavity.

7.2.2.2 *Wire Bond Finger Pullback* — A 0.010" (0.254 mm) maximum from the cavity edge and the minimum exposed wire bond lead length must meet the dimension on the procurement drawing or specification.

7.2.2.3 *Wire Bond Finger Rundown* — Not to exceed 25% of the ceramic layer thickness or 0.005" (0.127 mm), whichever is the smaller.

7.3 *Lead Attachment*

7.3.1 *Voids in Braze*

7.3.1.1 *Gold Plated Leadframes* — 75% of the braze fillet will be void free.

7.3.1.2 *Nickel or Bare Leadframes* — 75% of the braze fillet will be void free.

7.3.2 *Lead Alignment*

7.3.2.1 *Misalignment Leads to Braze Pads* — The leads shall not overhang the braze pads by more than 25% of the measured paddle width nor reduce the clearance between adjacent pad or lead to less than 50% of the clearance between adjacent metallizations.

7.3.2.2 *Lead Offset* — Lead centerlines must be aligned to within 0.015" (0.381 mm) relative to the position of the leads on the opposite side of the package.

7.3.2.3 *Lead-to-Lead Alignment* — 0.010" ± 0.010" (0.254 mm ± 0.254 mm) measured at the base of the ceramic on the same side.

8 Sampling

Sampling sizes must meet the requirements of MIL-STD-105; although single, double, or multiple samples may be used.

9 Test Methods

9.1 *Mechanical, Electrical and Thermal Test Methods*

9.1.1 *Gold Plating Quality*

9.1.1.1 Purity and adhesion of the gold plated package shall be tested by placing parts on a calibrated heater block at:

Condition A — 450°C ± 10°C for two minutes in air, or

Condition B — 470°C ± 10°C for one minute in nitrogen.

9.1.1.2 After cooling at room temperature the packages will be visually examined for the following criteria:

9.1.1.2.1 Blisters on the leadframe are acceptable only on the tie bar (that portion removed during trim). Blisters on the bonding fingers shall not exceed 0.003" (0.076 mm) diameter with a maximum of 1 blister per finger and 5 blisters per package of any size. Blisters on the seal ring shall not exceed 0.005" (0.127 mm) diameter. Blisters on the die attach pad shall not exceed 0.010" (0.254 mm) diameter with a maximum of 5 blisters per package greater than 0.005" (0.127 mm) diameter.

9.1.1.2.2 Slight discoloration of the gold at the die attach pad edges up to 0.025" (0.635 mm) from the cavity walls is acceptable. Discoloration of the bonding fingers, seal ring surface or external leads is not acceptable.

9.1.1.2.3 There shall be no flaking or peeling of the package plating when viewed at 15× magnification.

9.1.1.2.4 Superficial stains left during drying or prior operations is not cause for rejection.

9.1.2 *Lead Pull* — Four pounds (1.8 kg) minimum at a 45° angle from the lead's original plane.

9.1.3 *Lead Fatigue* — Test per MIL-STD-883, Method 2004.2, Test Condition B2, Section 3.2.

9.1.4 *Thermal Characteristics* — Test per MIL-STD-883, Method 1012, Test Conditions A, B, C, D, and E.

9.2 *Functional Test Methods*

9.2.1 *Die Attach Quality* — Perform destructive die shear test post environmental testing per MIL-STD-883, Method 2019.1, Section 3.2C.

9.2.2 *Wire Bond Quality* — Perform minimum pre-seal and post-seal bond strength test per MIL-STD-883, Method 2011.2, Test Condition D. Reject for bonds which cause plating to lift from the base metal of the die attach surface or bonding fingers.

9.2.3 *Solderability* — Test per MIL-STD-883, Method 2003.2.

9.2.4 *Insulation Resistance* — Test per MIL-STD-883, Method 1003.

9.2.5 *Hermetic and Environmental Testing*

9.2.5.1 The hermetic integrity of the package must be maintained after all environmental testing. Hermetic checks shall comply with MIL-STD-883, Method 1014.3, Test Condition A_1 or B and C.

9.2.5.2 Environmental testing shall include, but not be limited to, the following:

1. *Temperature Cycle* — MIL-STD-883, Method 1010.2 Condition C
2. *Thermal Shock* — MIL-STD-883, Method 1011.2, Condition C

3. *Centrifuge* — MIL-STD-883, Method 2001.2, Condition E
4. *Mechanical Shock* — MIL-STD-883, Method 2002.2, Condition B

9.2.6 *Sequence of Events and Incoming Testing* — During incoming inspection the sequence of testing shall be:

1. Die Attach
2. Wire Bond
3. Pre-Seal Bond Pull
4. Seal
5. Environmental Test
6. Fine Leak
7. Gross Leak
8. Trim
9. Post-Seal Bond Pull
10. Radiography
11. Die Shear
12. Solderability

NOTE: An initial vendor qualification on the thermal and electrical characteristics of the package may be performed. The characteristics tested will be:

1. *Insulation Resistance* — MIL-STD-883, Method 1003, Test Condition D
2. *Thermal Dissipation* — MIL-STD-883, Method 1012

10 Packaging and Marking

10.1 *Packaging* — Containers selected shall be strong enough and suitably designed to provide maximum protection against crushing, spillage, and other forms of damage to the container or its contents. Containers shall afford protection of the contents to contamination from exposure to excessive moisture or oxidation by gases. Packaging materials shall be so selected to prevent any contamination of the ceramic component parts with paper fibers or organic particles.

10.2 *Marking* — The outer containers shall be clearly marked to identify the user stock number, user purchase order number, drawing number, quantity, and vendor lot number.

11 Product Design

11.1 *Leadframe Paddle Width and Standoff* — (See Figure 5.)

NOTE: A geometric symbol adjacent to an identifying lead number 1 shall be considered appropriate for packages with all leads isolated from the die attach.

NOTE: Lead number 14 is common to die attach surface and is identified by placing this number where lead number 1 is located.

11.1.1 Leadframe paddle width shall be 1.14 mm (0.045") ± 0.178 mm (0.007").

11.1.2 Standoff shall be 1.02 mm ± 0.254 mm (0.040" ± 0.010").

11.1.3 Hole Diameter shall be 0.032" – 0.033" (0.813 mm – 0.838 mm).

11.2 *Substrate/Terminal Commonality on Sidebrazed Laminate Packages* — If no leads are common to the die attach surface, the lead one identification shall be a geometric symbol (Figure 6).

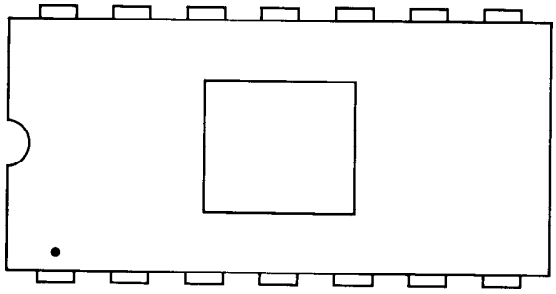


Figure 6
Lead Identification

Layers shall be designated by letter beginning with “A” as that layer nearest terminal insertion plane. Layers, regardless of function, shall be designated by succeeding letters, (B, C, D, etc.) as being progressively remote from the terminal insertion plane.

Should any lead be common to the die attach surface, that lead number will serve both as lead one identificationand as an indicator as to the lead that is common to the die attach surface (Figure 7).

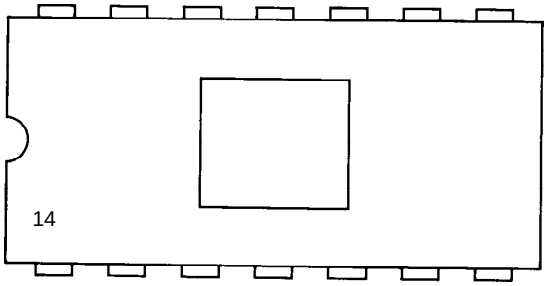


Figure 7
Lead Identification

11.3 *Sidebraze Ceramic Package Layer Design* — (See Figure 8).

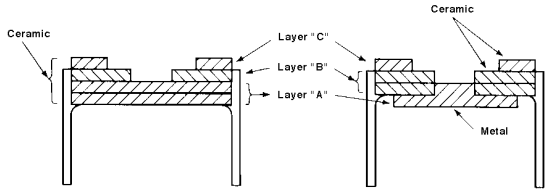


Figure 8
Layer Designation

Table 1 Sidebrazed Laminate Packages Dimensions and Tolerance Requirements

Desription	*Package Length*	*Package Width (Inc. Leadframe)*	*Package Thickness Min. Max.*	*Cavity Length (Measured at Cavity Bottom)*	*Cavity Width (Measured at Cavity Bottom)*	*Units*
8MSI	0.520 ± 0.008	0.310 + 0.010 - 0.015	0.076 – 0.094	0.180 ± 0.005	0.150 ± 0.005	in
	13.21 ± 0.203	7.87 + 0.254 - 0.381	1.93 – 2.39	4.57 ± 0.127	3.81 ± 0.127	mm
8LSI	0.520 ± 0.008	0.310 + 0.010 – 0.015	0.076 - 0.094	0.220 ± 0.005	0.175 ± 0.005	in
	13.21 ± 0.203	7.87 + 0.254 - 0.381	1.93 - 2.39	5.59 ± 0.127	4.45 ± 0.127	mm
8VLSI	0.520 ± 0.008	0.310 + 0.010 – 0.015	0.076 - 0.094	0.260 ± 0.005	0.175 ± 0.005	in
	13.21 ± 0.203	7.87 + 0.254 - 0.381	1.93 - 2.39	6.60 ± 0.127	4.45 ± 0.127	mm
14MSI	0.750 ± 0.010	0.310 + 0.010 – 0.015	0.076 – 0.094	0.180 ± 0.005	0.150 ± 0.005	in
	19.05 ± 0.254	7.87 + 0.254 - 0.381	1.93 – 2.39	4.57 ± 0.127	3.81 ± 0.127	mm
14LSI	0.750 ± 0.010	0.310 + 0.010 – 0.015	0.076 - 0.094	0.220 ± 0.006	0.175 ± 0.005	in
	19.05 ± 0.254	7.87 + 0.254 - 0.381	1.93 - 2.39	5.59 ± 0.152	4.45 ± 0.127	mm
14VLSI	0.750 ± .010	0.310 + 0.010 – 0.015	0.076 – 0.094	0.260 ± 0.006	0.175 ± 0.005	in
	19.05 ± 0.254	7.87 + 0.254 - 0.381	1.93 – 2.39	6.60 ± 0.152	4.45 ± 0.127	mm
16MSI	0.800 ± 0.010	0.310 + 0.010 – 0.015	0.076 - 0.094	0.220 ± 0.006	0.175 ± 0.005	in
	20.32 ± 0.254	7.87 + 0.254 - 0.381	1.93 - 2.39	5.59 ± 0.152	4.45 ± 0.127	mm
16LSI	0.800 ± 0.010	0.310 + 0.010 – 0.015	0.076 – 0.094	0.240 ± 0.006	0.175 ± 0.005	in
	20.32 ± 0.254	7.87 + 0.254 - 0.381	1.93 – 2.39	6.10 ± 0.152	4.45 ± 0.127	mm
16VLSI	0.800 ± 0.010	0.310 + 0.010 – 0.015	0.076 - 0.094	0.320 ± 0.007	0.175 ± 0.005	in
	20.32 ± 0.254	7.87 + 0.254 - 0.381	1.93 - 2.39	8.13 ± 0.178	4.45 ± 0.127	mm
18MSI	0.900 ± 0.010	0.310 + 0.010 – 0.015	0.076 – 0.094	0.220 ± 0.006	0.175 ± 0.005	in
	22.86 ± 0.254	7.87 + 0.254 - 0.381	1.93 – 2.39	5.59 ± 0.152	4.45 ± 0.127	mm
18LSI	0.900 ± 0.010	0.310 + 0.010 – 0.015	0.076 - 0.094	0.265 ± 0.006	0.175 ± 0.005	in
	22.86 ± 0.254	7.87 + 0.254 - 0.381	1.93 - 2.39	6.73 ± 0.152	4.45 ± 0.127	mm
18VLSI	0.900 ± 0.010	0.310 + 0.010 – 0.015	0.076 – 0.094	0.320 ± 0.007	0.175 ± 0.005	in
	22.86 ± 0.254	7.87 + 0.254 - 0.381	1.93 – 2.39	8.13 ± 0.178	4.45 ± 0.127	mm
20MSI	1.000 ± 0.010	0.310 + 0.010 – 0.015	0.076 - 0.094	0.215 ± 0.005	0.175 ± 0.005	in
	24.89 ± 0.254	7.87 + 0.254 - 0.381	1.93 - 2.39	5.46 ± 0.127	4.45 ± 0.127	mm
20LSI	1.000 ± 0.010	0.310 + 0.010 – 0.015	0.076 – 0.094	0.265 ± 0.006	0.175 ± 0.005	in
	24.89 ± 0.254	7.87 + 0.254 - 0.381	1.93 – 2.39	6.73 ± 0.152	4.45 ± 0.127	mm
20VLSI	1.000 ± 0.010	0.310 + 0.010 – 0.015	0.076 - 0.094	0.320 ± 0.007	0.175 ± 0.005	in
	24.89 ± 0.254	7.87 + 0.254 - 0.381	1.93 - 2.39	8.13 ± 0.178	4.45 ± 0.127	mm
22MSI	1.08 ± 0.011	0.410 + 0.010 – 0.015	0.076 – 0.094	0.250 ± 0.006	0.220 ± 0.006	in
	27.34 ± 0.279	10.41 + 0.254 - 0.381	1.93 – 2.39	6.35 ± 0.152	5.59 ± 0.152	mm
22LSI	1.08 ± 0.011	0.410 + 0.010 – 0.015	0.076 - 0.094	0.285 ± 0.006	2.20 ± 0.006	in
	27.34 ± 0.279	10.41 + 0.254 - 0.381	1.93 - 2.39	7.24 ± 0.152	5.59 ± 0.152	mm
22VLSI	1.08 ± 0.011	0.410 + 0.010 – 0.015	0.076 – 0.094	0.280 ± 0.006	0.260 ± 0.006	in
	27.34 ± 0.279	10.41 + 0.254 - 0.381	1.93 - 2.39	7.11 ± 0.152	6.60 ± 0.152	mm
24MSI	1.20 ± 0.012	0.610 + 0.010 – 0.015	0.076 - 0.094	0.250 ± 0.006	0.250 ± 0.006	in
	30.48 ± 0.305	15.49 + 0.254 - 0.381	1.93 - 2.39	6.35 ± 0.152	6.35 ± 0.152	mm
24LSI	1.20 ± 0.012	0.610 + 0.010 – 0.015	0.076 – 0.094	0.305 ± 0.010	0.305 ± 0.010	in
	30.48 ± 0.305	15.49 + 0.254 - 0.381	1.93 – 2.39	7.75 ± 0.254	7.75 ± 0.254	mm
24VLSI	1.20 ± 0.012	0.610 + 0.010 – 0.015	0.076 - 0.094	0.340 ± 0.008	0.340 ± 0.008	in
	30.48 ± 0.305	15.49 + 0.254 - 0.381	1.93 - 2.39	8.64 ± 0.203	8.64 ± 0.203	mm
28MSI	1.40 ± 0.014	0.610 + 0.010 – 0.015	0.076 – 0.094	0.250 ± 0.006	0.250 ± 0.006	in
	35.56 ± 0.356	15.49 + 0.254 - 0.381	1.93 – 2.39	6.35 ± 0.152	6.35 ± 0.152	mm
28LSI	1.40 ± 0.014	0.610 + 0.010 – 0.015	0.076 - 0.094	0.305 ± 0.010	0.305 ± 0.010	in

	35.56 ± 0.356	15.49 + 0.254 - 0.381	1.93 - 2.39	7.75 ± 0.254	7.75 ± 0.254	mm
28VLSI	1.40 ± 0.014	0.610 + 0.010 – 0.015	0.076 – 0.094	0.340 ± 0.008	0.340 ± 0.008	in
	35.56 ± 0.356	15.49 + 0.254 - 0.381	1.93 – 2.39	8.64 ± 0.203	8.64 ± 0.203	mm
40MSI	2.00 ± 0.020	0.610 + 0.010 – 0.015	0.076 - 0.094	0.250 ± 0.006	0.250 ± 0.006	in
	50.8 ± 0.508	15.49 + 0.254 - 0.381	1.93 - 2.39	6.35 ± 0.152	6.35 ± 0.152	mm
40LSI	2.00 ± 0.020	0.610 + 0.010 – 0.015	0.076 – 0.094	0.305 ± 0.010	0.305 ± 0.010	in
	50.8 ± 0.508	15.49 + 0.254 - 0.381	1.93 – 2.39	7.75 ± 0.254	7.75 ± 0.254	mm
40VLSI	2.00 ± 0.020	0.610 + 0.010 – 0.015	0.076 - 0.094	0.340 ± 0.008	0.340 ± 0.008	in
	50.8 ± 0.508	15.49 + 0.254 - 0.381	1.93 - 2.39	8.64 ± 0.203	8.64 ± 0.203	mm
48LSI	2.40 ± 0.025	0.610 + 0.010 – 0.015	0.076 – 0.094	0.305 ± 0.010	0.305 ± 0.010	in
	60.96 ± 0.635	15.49 + 0.254 – 0.381	1.93 – 2.39	7.75 ± 0.254	7.75 ± 0.254	mm
48VLSI	2.40 ± 0.025	0.610 + 0.010 - 0.015	0.076 - 0.094	0.340 ± 0.008	0.340 ± 0.008	in
	60.96 ± 0.635	15.49 + 0.254 – 0.381	1.93 - 2.39	8.64 ± 0.203	8.64 ± 0.203	mm

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SEMI G4-0302
SPECIFICATION FOR INTEGRATED CIRCUIT LEADFRAME MATERIALS USED IN THE PRODUCTION OF STAMPED LEADFRAMES

This specification was technically approved by the Gobal Assembly and Packaging Committtee and is the direct responsibility of the Japanese Assembly and Packaging Committee. Current edition approved by the Japanese Regional Standards Committtee on November 26, 2001. Initially available at www.semi.org December 2001; to be published March 2002. Originally published in 1994.

1 Scope

1.1 This specification covers the special requirements for a metal strip to be used to fabricate integrated circuit leadframes by stamping.

2 Applicable Documents

Regional standards such as ANSI/ASTM,CEN, EN ISO, JIS, and MIL.

2.1 *ANSI*[1]*/ASTMStandard*[2]

ASTM B 193 — Test Method for Resistivity of Electrical Conductor Materials

ASTM B 601 — Standard Practice for Temper Designations for Copper and Copper Alloys — Wrought and Cast

ASTM E 8 — Standard Test Methods of Tension Testing of Metallic Materials

ASTM E 228 — Standard Test Method for Linear Thermal Expansion of Solid Materials with a Vitreous Silica Delatometer

ASTM E 290 — Test Method for Semi-Guided Bend Test for Ductility of Metallic Materials

ASTM E 384 — Test Method for Microhardness of Materials

ASTM E 527 — Practice for Numbering Metals and Alloys (UNS)

2.2 *CES Standard*

CES M0002-5 — Method of W-Bend Test for Metallic Materials

2.3 *EN Standard*

EN 10 002 Part 1 — Metallic Materials, Tensile Testing, Part 1: Method of Testing (at ambient temperature)

EN 133/10 — Copper and Copper Alloys: Plate, Sheet, Strip, and Circles for General Purposes

EN 133/12 — Copper and Copper Alloys: Plate, Sheet, and Circles for Boilers, Pressure Vessels, and Hot Water Storage Units

2.4 *ISO Standard*[3]

ISO 197-3 — Copper and Copper Alloys, Terms, and Definitions, Part 3: Wrought Products

ISO 1190 Part 1 — Copper and Copper Alloys, Code of Designation, Part 1: Designation of Materials

ISO 4287 Part 1 — Surface Roughness, Terminology, Part 1: Surface and Its Parameters Trilingual Edition

ISO 6507 Part 1 — Metallic Materials, Hardness Test, Vickers Test, Part 1: HV 5 to HV 100

ISO 6507 Part 2 — Metallic Materials, Hardness Test, Vickers Test, Part 2: HV 0.2 to less than HV 5.

ISO 7438 — Metallic Materials, Bend Test

2.5 *JIS Standard*[4]

JIS B0601 — Definitions and Designation of Surface Roughness

JIS H0505 — Measuring Methods for Electrical Resistivity and Conductivity of Non-Ferrous Materials

JIS H3100 — Copper and Copper Alloy: Plates, Sheets, Strips

JIS H3110 — Phosphor Bronze and Nickel Silver: Plates, Sheets, Strips

JIS Z2201 — Test Pieces for Tensile Test for Metallic Materials

JIS Z2241 — Method of Tensile Test for Metallic Materials

JIS Z2244 — Method of Vickers Hardness Test

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1 ANSI, 1430 Broadway, New York, NY 10018

2 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959

3 ISO, 1 rue de Varembe, Case postale 56, CH01211 Geneva 20, Switzerland

4 JIS, 4-1-24 Akasaka Minato-ku Tokyo, Japan

JIS Z2251 — Method of Micro Hardness Test for Vickers and Knoop Hardness

3 Ordering Information

Orders for material under this specification shall include the following information:

1. Quantity of each size

2. Alloy name and number (see Section 4)

3. Temper or mechanical properties (see Section 4)

4. Dimensions: thickness and width (see Section 5)

5. How furnished: coils and coil size (see Section 10)

6. Special processing requirements

7. Certification or test report requirements (see Section 11).

4 Designations

4.1 Material designations shall be based on appropriate area standards based on country or area of material origin.

4.1.1 Europe ISO 1190 Part 1

4.1.2 Japan JIS H3100, JIS H3110

4.1.3 United States ASTM E 5.27

4.2 Temper designations shall be based on appropriate area standards based on country or area of material origin.

4.2.1 Europe EN133/10 and 133/12

4.2.2 Japan JIS H3100, JIS H 3110

4.2.3 United States ASTM B 601

5 Requirements

5.1 *General Requirements*

5.1.1 The materials covered by this specification shall conform to the requirements detailed herein, unless otherwise agreed upon by supplier and purchaser.

5.2 *Mechanical Properties*

5.2.1 The preferred method of designating mechanical properties of material covered under this specification is tensile strength. In addition to tensile strength, the 0.2% offset yield strength and percent elongation in 50 mm may be required if agreed between supplier and purchaser. The test shall conform to the appropriate area standards based on country or area of material origin.

5.2.1.1 Europe EN10 002 Part 1

5.2.1.2 Japan JIS Z2201, Z2241

5.2.1.3 United States ASTM E8

5.2.2 Should supplier and purchaser agree, microhardness may be used in lieu of tensile strength as the test for mechanical property. The test shall conform to the appropriate area standard based on country or area of material origin.

5.2.2.1 Europe ISO 6507 Part 1 and Part 2

5.2.2.2 Japan JIS Z2251, Z2244 (Test load shall be chosen from Table 1).

5.2.2.3 United States ASTM E 384

Table 1

Thickness of Metal Strip (mm)	*Test Load of Vickers Hardness*
0.100 to 0.160	1.961 N (200 gf)
over 0.160 to 0.500	4.903 N (500 gf)
over 0.500	9.807 N (1 Kgf)

5.3 *Thickness and Width Tolerance*

5.3.1 Thickness tolerance for material covered under this specification shall be chosen from Tables 2 and 3.

Table 2

Thickness	*Tolerance*
0.10 mm to 0.15 mm	± 0.005 mm
over 0.15 mm to 2.0 mm	± 3% of the ordered material thickness

Table 3

Thickness	*Tolerance*
0.10 mm up to 0.15 mm	± 0.005 mm
0.15 mm up to 0.3 mm	± 0.008 mm
0.3 mm up to 0.5 mm	± 0.010 mm
0.5 mm up to 0.8 mm	± 0.013 mm
0.8 mm up to 1.0 mm	± 0.015 mm
1.0 mm up to 1.5 mm	± 0.020 mm
1.5 mm up to 2.0 mm	±0.025 mm

* Table 3 is used in Europe.

5.3.2 Width tolerance shall be as shown in Tables 4 and 5.

Table 4

Width	*Thickness*	*Tolerance*
under 15 mm to 55 mm	0.1 mm to under 0.3 mm	± 0.05 mm
	0.3 mm to under 1.0 mm	± 0.08 mm
	1.0 mm to 2.0 mm	± 0.15 mm
over 55 mm to 100 mm	0.1 mm to under 0.3 mm	± 0.08 mm
	0.3 mm to under 1.0 mm	± 0.12 mm
	1.0 mm to 2.0 mm	± 0.15 mm

Table 5

Width	*Thickness*	*Tolerance*
under 15 mm	over 0.1 mm to 0.3 mm	± 0.05 mm
	over 0.3 mm to 1.0 mm	± 0.08 mm
	over 1.0 mm to 2.0 mm	± 0.15 mm
15 mm to 55 mm	over 0.1 mm to 0.3 mm	± 0.05 mm
	over 0.3 mm to 1.0 mm	± 0.08 mm
	over 1.0 mm to 2.0 mm	± 0.15 mm
Over 55 mm to 100 mm	over 0.1 mm to 0.3 mm	± 0.08 mm
	over 0.3 mm to 1.0 mm	± 0.12 mm
	over 1.0 mm to 2.0 mm	± 0.15 mm

* Table 5 is used in Europe.

5.4 *Surface Finish*

5.4.1 The material shall be commercially free of surface imperfections such as pits, nicks, dents, gouges, scratches, laminations, or inclusions.

5.4.2 The surface roughness of both sides shall be measured perpendicular to the direction of rolling and indicated as the arithmetic average height (R_a) and the maximum peak-to-valley roughness height (R_{max}).

5.4.2.1 Measurement and designations of surface roughness shall conform to appropriate area standards based on country or area of material origin.

5.4.2.1.1 Europe ISO 4287 Part 1

5.4.2.1.2 Japan JIS B0601

5.4.2.1.3 United States ANSI/ASME B46.1

5.4.2.2 Conditions for the measurement are shown in Table 6.

Table 6

Radius of Diamond Stylus: Less than 5mm	*(Record Actual Size)*
Cut Off:	0.8 mm
Stroke:	4 mm

5.4.2.3 Maximum acceptable values for surface roughness are shown in Table 7.

Table 7

Thickness	R_a	R_{max}
0.1 mm to under 0.3 mm	0.15 µm	1.0 µm (1.5 µm)
0.3 mm to 2 mm	0.20 µm	1.5 µm (2.0 µm)

* Values in parentheses are used in Europe.

5.5 *Camber (Edgewise Curvature)*

5.5.1 Camber is measured by placing a length of strip on a flat surface against the edge of a straight edge, as shown in Figure 1. The straight edge shall be of sufficient length to equal or exceed the length traditionally used in the area or country of origin of the material. The largest amount of separation of the strip sample from the straight edge shall be measured. Extreme care must be exercised with this test to ensure that the sample illustrates a uniform camber (no reverse curvature should be present in the sample), and also that it is not bent or kinked, as this could result in a grossly inaccurate measurement. The maximum camber per length allowable are shown in Table 8.

Table 8

Width	*Thickness*	*Max camber allowed in 1 meter*
Under 15 mm	0.1 mm to under 0.3 mm	1.8 mm (2.0 mm)
	0.3 mm to under 1.0 mm	2.2 mm (2.5 mm)
	1.0 mm to 2.0 mm	4.0 mm
15 mm to 55 mm	0.1 mm to under 0.3 mm	1.3 mm
	0.3 mm to under 1.0 mm	2.0 mm
	1.0 mm to 2.0 mm	3.0 mm
Over 55 mm to 100 mm	0.1 mm to under 0.3 mm	1.0 mm
	0.3 mm to under 1.0 mm	1.5 mm
	1.0 mm to 2.0 mm	2.5 mm

5.6 *Flatness*

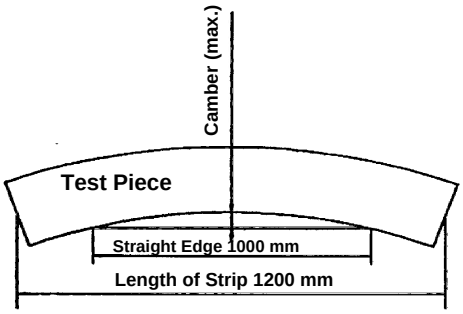


Figure 1
Camber

5.6.1 *Coil Set (Longitudinal Curl)*

5.6.1.1 Coil set shall be measured by attaching a length of strip, appropriate to the country or area of material origin, to a flat vertical surface as shown in Figure 2. The attachment shall be with a rigid block, wider than the strip. The block shall be so rigid as to ensure complete contact of the strip with the vertical surface. The distance between the flat surface and the free-hanging end of the strip (that is positioned for maximum distance from the flat vertical surface) shall be measured. The coil set shall be uniformly in the direction of coiling. Lengths shall be appropriate to the country or area of material origin. Maximum coil set for appropriate lengths are shown in Tables 9 and 10.

Table 9

Inside Diameter of Coil	*Thickness*	*Width*	*Max Coil Set in 1 m*
400 mm	under 0.3 mm	under 100 mm	100 mm

Table 10

Thickness	*Width*	*Max Coil Set in 0.3 m*
Under 0.3 mm	up to 15 mm	60 mm
	over 15 to 24 mm	50 mm
	over 24 to 55 mm	45 mm
	over 55 to 100 mm	40 mm
0.3 mm to 0.5 mm	up to 15 mm	70 mm
	over 15 to 24 mm	60 mm
	over 24 to 55 mm	55 mm
	over 55 to 100 mm	50 mm

* Table 10 is used in Europe.

5.6.2 *Crossbow (Dish)*

5.6.2.1 Crossbow shall be measured across the width of the strip, as shown in Figure 3. Burrs shall be removed or burr height excluded from this measurement. Crossbow shall be measured with a tool maker's microscope or equivalent. Crossbow maxima are listed in Tables 11 and 12.

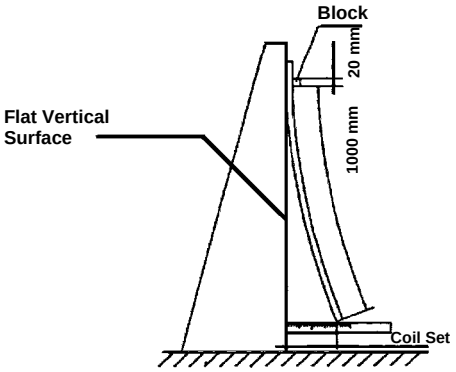


Figure 2
Coil Set

Table 11

Width	*Thickness*	*Crossbow Limit*
under 15 mm	0.1 mm to under 0.3 mm	0.5% of width
	0.3 mm to under 1.0 mm	1.0% of width
	1.0 mm to 2.0 mm	1.5% of width
15 mm to 55 mm	0.1 mm to under 0.3 mm	0.5% of width
	0.3 mm to under 1.0 mm	0.5% of width
	1.0 mm to 2.0 mm	0.5% of width
over 55 mm to 100 mm	0.1 mm to under 0.3 mm	0.4% of width
	0.3 mm to under 1.0 mm	0.4% of width
	1.0 mm to 2.0 mm	0.4% of width

Table 12

Width	*Thickness*	*Crossbow Limit*
from 15 mm to 24 mm	0.1 mm to under 0.3 mm	0.10 mm
	0.3 mm to under 1.0 mm	0.15 mm
	1.0 mm to 2.0 mm	0.20 mm
over 24 mm to 55 mm	0.1 mm to under 0.3 mm	0.15 mm
	0.3 mm to under 1.0 mm	0.20 mm
	1.0 mm to 2.0 mm	0.25 mm
over 55 mm to 100 mm	0.1 mm to under 0.3 mm	0.25 mm
	0.3 mm to under 1.0 mm	0.30 mm
	1.0 mm to 2.0 mm	0.35 mm

* Table 12 is used in Europe.

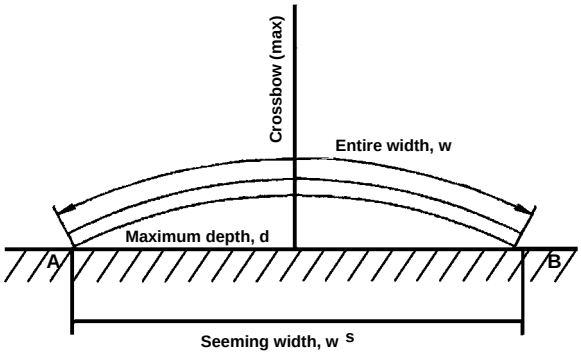


Figure 3
Crossbow

5.6.3 *Twist*

5.6.3.1 Twist shall be measured in a fashion similar to coil set, as shown in Figure 4A or Figure 4B. A length of strip, appropriate to the country or area of material origin, shall be attached at one end to a flat vertical surface. The attachment shall be with a rigid block, wider than the strip. The block shall be so rigid as to ensure complete contact of the strip with the vertical surface. At the free end of the strip, the distance from the vertical surface and both edges of the free strip end shall be measured. The maximum difference in these dimensions is shown in Table 13.

Table 13

Thickness	*Twist Maximum (Difference in Edge Distance)*
0.1 mm to 0.5 mm	Width × 0.2823 for 1000mm (Width × 0.2823 for 300mm)

* Value in parentheses is used in Europe.

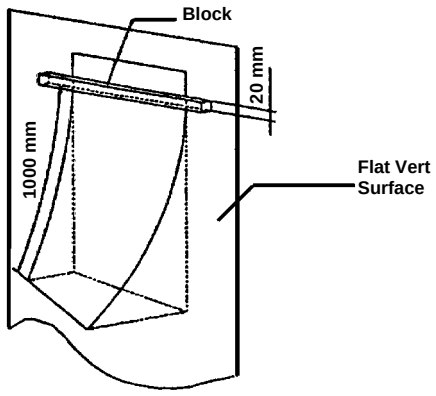


Figure 4
Twist Test

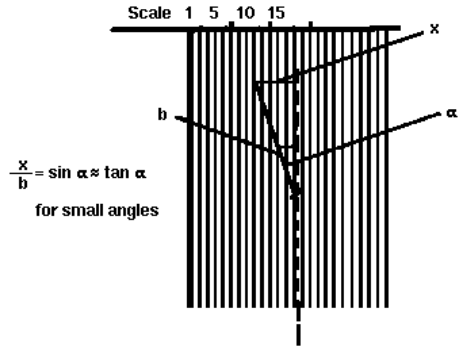


Figure 4B
Twist Test

5.7 *Burrs*

5.7.1 Edge burrs shall not exceed the values in Table 14 and 15. As shown in Figure 5, a-b shall be measured.

Table 14

Thickness	*Maximum Allowed Edge Burr*
0.1 mm to under 0.3 mm	Thickness x 10%
0.3 mm to under 1.0 mm	Thickness x 7%
1.0 mm to under 2.0 mm	Thickness x 5%

Table 15

Thickness	*Maximum Allowed Edge Burr Height*
0.1 mm to 0.3 mm	0.02 mm
Over 0.3 mm to 1.0 mm	0.03 mm
Over 1.0 mm to 2.0 mm	0.04 mm

* Table 15 is used in Europe.

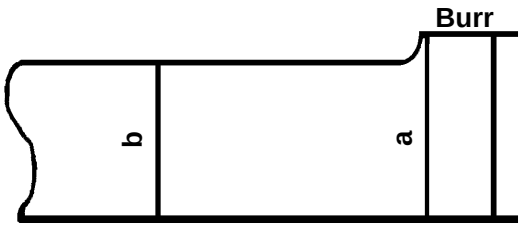


Figure 5
Burr

5.8 *Corrosion*

5.8.1 Visual inspection shall be performed within 60 days of receipt of material. The material shall be free of objectionable surface oxides which would render the product unusable for the intended application. The material shall have been stored for this period in the original supplier's package.

6 Bend Formability

6.1 When agreed between supplier and purchaser, a bend formability test shall be performed. This test shall be based on area standards based on country or area of material origin.

6.1.1 *Europe ISO 7438* — (Test jig is shown in Figure 2 of ISO 7438.)

6.1.2 *Japan CES M0002-5* — The test piece which shall be 10 mm wide and a minimum of 30 mm long will be put on the B type test jig with a bend radial of 0.15 mm and 0.25 mm and from 0–2.0 mm at interval of 0.2 mm. In this case, die pressure shall be 807N (1000Kgf) and over. The B type test jig is shown in Figure 2 of CES M0002-5.

6.1.3 *United States* — ASTM E 290.

7 Lead Bend Fatigue

7.1 When agreed between supplier and purchaser, a lead bend fatigue test shall be performed. This test shall be conform to the appropriate area standards based on the country or area of material origin.

7.1.1 *Europe* — MIL-STD-883.

7.1.2 *Japan* — Appendix 1

7.1.3 *United States* — MIL-STD-883.

8 Physical Properties

8.1 When agreed between supplier and purchaser, tests on physical properties shall be performed based on appropriate area standards based on country or area of material origin.

8.1.1 *Chemistry*

8.1.1.1 Chemical analysis of material shall be performed using accepted procedures such as X-Ray fluorescence spectroscopy, optical emission spectroscopy, and atomic absorption spectroscopy. These tests shall be performed based on appropriate area standards based on country or area of material origin.

8.1.1.1.1 *Europe* — ISO.

8.1.1.1.2 *Japan* — JIS.

8.1.1.1.3 *United States* — ASTM standards under preparation.

8.1.2 *Electrical Conductivity*

8.1.2.1 The test for electrical resistivity and conductivity shall be performed based on appropriate area standards based on country or area of material origin.

8.1.2.1.1 *Europe* — ASTM B193.

8.1.2.1.2 *Japan* — JIS H0505.

8.1.2.1.3 *United States* — ASTM B193.

8.1.2.2 Thermal conductivity shall be calculated from electrical conductivity using the law of Wiedemann and Franz, which is described as:

$k/\sigma T = L$, where:

k = thermal conductivity
σ = electrical conductivity
T = absolute temperature
L = Lorenz number = $2.44 \times 10^{-8}(V/K)^2$
where : V = voltage and K = Kelvin scale

8.1.3 *Coefficient of Thermal Expansion*

8.1.3.1 T he coefficient of thermal expansion shall be measured between 20°C and 300°C. The test shall be based on the appropriate area standard based on the country or area of material origin.

8.1.3.1.1 *Europe* — ASTM E 228.

8.1.3.1.2 *Japan* — ASTM E 228.

8.1.3.1.3 *United States* — ASTM E 228.

9 Silt Strain (Stress)

9.1 When agreed upon between supplier and purchaser, a test to determine internal stress distribution shall be performed. The test should be based on some form of chemical milling, sawing, or wire cutting to remove portions of the strip to form a pattern in the strip. As a guide to preparation of such tests, a procedure is shown in Appendix 2 or 3.

10 Coils

10.1 Unless otherwise specified, coils shall be supplied with an inside diameter that provides for good packing practice without resulting in excessive coil set.

10.2 All coils supplied shall be continuous, uniform lengths, and free of welds. Autogenous welds made at heavy gauge, prior to finish reductions that ultimately provide homogeneous structures, are allowed.

11 Certification or Test Reports

11.1 Requests for certifications or test reports shall be made at the time of order entry or contract agreement. They shall be furnished by the manufacturer within one week of date of shipment.

11.2 When certifications are required, the following information shall be supplied as a minimum:

1. Vendor name
2. Purchase order number
3. Vendor order number
4. Alloy name and number
5. Chemical analysis
6. Temper designation, reference only (for copper base alloys only)
7. Tensile strength
8. Elongation percent in 50 mm
9. Electrical conductivity % IACS (for copper base alloys only)

11.3 In the event of a disagreement between supplier and purchaser, an independent test shall be conducted on strip to verify the data provided in the certification.

12 Packaging and Marking

12.1 The material shall be separated by size, composition, and temper, and prepared for shipment in such a manner as to ensure acceptance by a common carrier for transportation at the lowest applicable rate.

12.2 The material shall be suitably packaged to protect from condensation, contamination, etc., and to afford protection from the normal hazards of transportation.

12.3 Each shipping unit shall be legibly marked with the purchase order number, alloy name or number, temper, size, gross and net weight, and name of the supplier. The specification number shall be shown when specified on the purchase order.

12.4 Any special packaging or shipping requirements shall be agreed upon between supplier and purchaser at the time of purchase.

13 Basis for Rejection

13.1 For the purposes of determining conformance with the requirements prescribed in the specifications, any measured value outside the specified limiting values shall be cause for rejection.

13.2 If objectionable material is found and rejected, samples of the questionable material, with the defects identified and marked, should be sent to the supplier along with information as to order number, quantity originally received, date received, and quantity rejected. Rejected material should be held with adequate protection and identification by the purchaser for a reasonable amount of time, pending investigation by the supplier.

APPENDIX 1
TEST METHOD FOR LEAD BEND FATIGUE OF METAL STRIPS

NOTE: The material in this appendix is an official part of SEMI G4.

A1-1 Preface

This is related to the test method for lead bend fatigue of metal strips of leadframe materials improving MIL-STD-883. Results of this test suggest the lead bend fatigue resistance of leadframes.

The following method is set up especially for the strips with the thickness of 0.25 mm ± 0.008 mm.

A1-2 Method of Measurement

A1-2.1 *Equipment* — Automatic or manual lead bend fatigue tester as shown in Figure A1-1.

A1-2.2 *Preparation of Specimen* — The specimen with the width of 0.5 mm ± 0.05 mm is made by either etching or stamping method. A wider portion on one end is recommended for a good grip as shown in Figure A1-2.

A1-2.3 *Procedure* — The specimen is clamped on both ends with clamp and weight as shown in Figure A1-3 and tested under the conditions listed in Table A1-1. The number of bending cycles (*) and other information (**) should be recorded.

*The number of bending cycles: The cycles until specimen breaks, and weight drops into pan.

0° – 90° – 0° bend on one side is counted as 1 cycle.

0° – 90° is counted as 0.5 cycle.

**Other information:

1. Rolling direction on the specimen.
2. Actually measured dimensional data of thickness and width.
3. Burr side related to bending corner (for stamped specimen only).

A1-3 Reference

SEMI G10 — Standard Method for Mechanical Measurement of Plastic Package Leadframes

Table A1-1

Bend Angle (set)	90° ± 2°
Rate of Cycle	2–5 sec/cycle
Weight	2.206–2.452N (225–250 gf)
Bend Radius: R (see Fig. A4)	0.15–0.20 mm

Note 1: In other cross sectional areas (thickness and width) of leads, the weight to be used shall be agreed upon between supplier and purchaser.

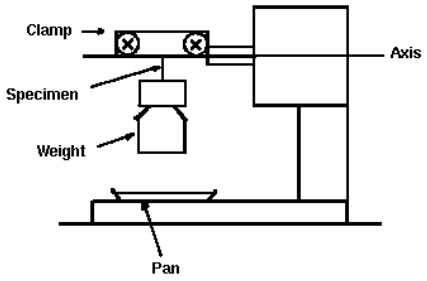


Figure A1-1
Lead Bend Fatigue Tester

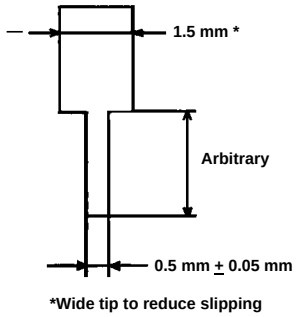


Figure A1-2
Shape of Specimen

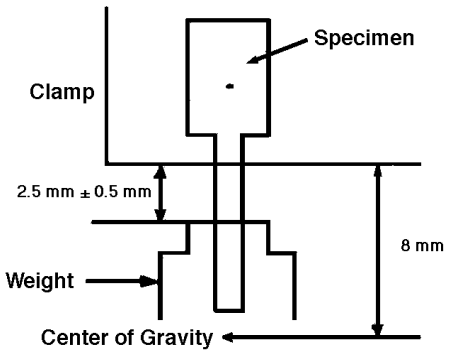


Figure A1-3
Clamping

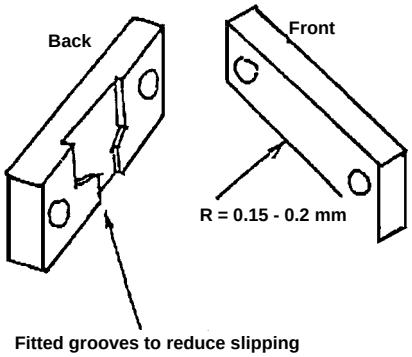


Figure A1-4
Inside of Clamp (Example)

APPENDIX 2
TEST METHOD FOR SLITTER STRAIN OF STRIPS USED FOR LEADFRAME STAMPING

NOTE: The material in this appendix is an official part of SEMI G4.

A2-1 Preface

This is related to the general evaluation method for slitter strain of strips used for leadframe stamping. Such distortion could result in adverse effects on leadframes, such as coil set, lead twist, and camber.

A2-2 Evaluation Method

A2-2.1 *Equipment* — Tool microscope (×100).

A2-2.2 *Procedure*

A2-2.2.1 Collect flat samples approximately 150 mm in length from strips in a way that residual distortion can be overlooked. (Collection methods include wire cutting, etching, refined cutting, etc.) Thickness of samples should be either 0.25 mm, 0.20 mm, or 0.15 mm.

A2-2.2.2 Fashion each sample to the shape shown in Figure A2-1 by etching or wire cutting. Measure with the tool microscope to obtain coordinates of the leg end corner. The reading accuracy is to 0.1 mm (see Note 1).

A2-2.2.3 Using the coordinates of the leg end corner, for each leg obtain longitudinal curvature "A", lead twist "B", and camber "C", as shown in Figure A2-2 (see Note 2).

Note 1: Specify the direction of slit burr, and for legs in which the longitudinal curvature A is reversed, measure by reversing the sample itself.

Note 2: Measured values are marked as shown in Figure A2-2.

Note 3: This method should be applied to only slitter strain. Do not apply to any other kind of strain (e.g., thermal inner strain).

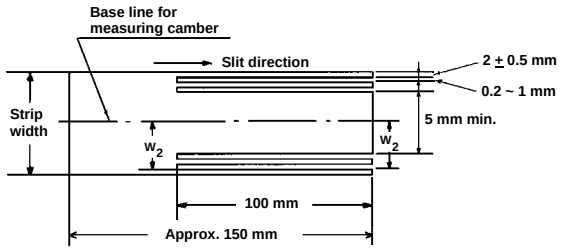


Figure A2-1
Shape for Evaluation of Slitter Strain

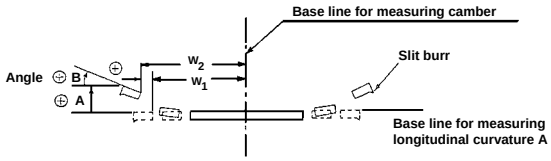


Figure A2-2
Evaluation Items

APPENDIX 3
TEST METHOD FOR SLIT STRAIN OF LEADFRAME STRIPS USED FOR STAMPING

NOTE: The material in this appendix is an official part of SEMI G4.

A3-1 Preface

A3-1.1 The method is used to evaluate the edge stress caused by slitting.

A3-1.2 This method is applied to thickness between 0.1 mm and 0.3 mm.

A3-2 Evaluation Method

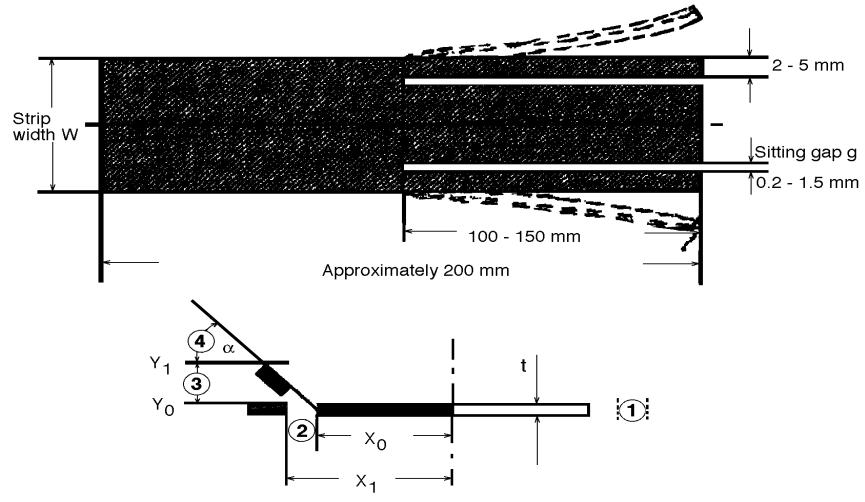
A3-2.1 *Equipment* — Tool microscope (×100).

A3-2.2 *Procedure*

A3-2.2.1 A test piece of approximately 200 mm length is sawn, stamped, etched, wire cut, refined cut, etc., over a length of 100–150 mm parallel to the rolling direction of a distance of 2–5 mm from the edge of the strip. (See Figure A1-7.)

A3-2.2.2 The dislocation of the outer strips relative to the plane of the test piece measured as camber c, longitudinal curvature L, and twist T characterize the internal edge stress. (Note 1)

Note 1: The details of the test method and the maximum admissible values of c, L, and T shall be agreed between purchaser and supplier.



① free of any residual stress

chamber ② $c=X_1-X_{o-g}=X_1-(W/2+g)$

longitudinal curvature ③ $L=Y_1-Y_o=Y_1-t/2$

twist ④ $T=\alpha$

Figure A1-7
Test Method of Slit Stress

NOTICE: These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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SEMI G5-87
STANDARD FOR CERAMIC CHIP CARRIERS

1 Scope

This specification defines the acceptance criteria for co-fired, ceramic chip carriers both leaded and lead-less.

2 Applicable Documents

2.1 *ANSI Specification*[1]

S Y 14.5 — Dimensioning and Tolerancing

2.2 *Federal Specification*[2]

QQ-N-290 — Nickel Plating

2.3 *JEDEC Specification*[3]

Pub. No. 95 — Registered and Standard Outline for Solid State Products

2.4 *Military Specifications*[4]

MIL-STD-105 — Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-883 — Test Methods and Procedures for Microelectronics

MIL-STD-7883 — Brazing

MIL-M-38510 — General Specification for Microcircuits

MIL-STD-45204 — Gold Plating, Electrodeposited

2.5 *SEMI Specifications*

SEMI G8 — Test Method for Gold Plating Quality

SEMI G25 — Test Method for Measuring the Resistance of Package Leads

SEMI G6 — Test Method for Seal Ring Flatness

3 Selected Definitions

braze — An alloy with a melting point equal to or greater than 600°C.

castellation — That series of ribs and metallized indentations that define edge contact regions (see Figure 1).

fired — A process or technology to manufacture products in which the ceramic and refractory metallization are fired simultaneously.

contact pad — That metallized pattern that provides mechanical or electrical connection to the external circuitry.

die attach surface — See Figure 3.

footprint — Contact pad pattern.

layer — A dielectric sheet with or without metallization that performs a discrete function as a part of the package.

lead offset — Alignment of leads across the package.

pullback — The linear distance between the edge of the ceramic and the first measurable metallization and/or glass interface (see Figures 4 and 5).

rundown — See Figures 4 and 5.

seal-area — A dimensional outline area designated for either metallization or bare ceramic to provide a surface area for sealing (see Figure 3).

terminal — Case outline at point of entry or exit of an electrical contact.

TIR — Total Indicator Reading.

4 Ordering Information

Purchase order for ceramic chip carriers furnished to this specification shall include the following items:

1. Quantity
2. Drawing — The drawing(s) for ceramic chip carriers shall specify the following information:
   a. Drawing number and revision level.
   b. Number of terminals and terminal center line spacing.
   c. Lead material and dimensions.
   d. Critical material properties.
   e. Type and thickness of plating.
   f. Package dimensions per ANSI Y14.5.
   g. Internal bonding patterns.
   h. Minimum exposed metallized bond finger length and width.

1 ANSI, 1430 Broadway, New York, NY 10018

2 Military Standards, Naval Publications and Form Center, 5801 Tabor Ave., Philadelphia, PA 19120

3 JEDEC, 2001 Eye Street, N.W., Washington, D.C. 20006

4 General Services Administrator, 4th and D Streets, SW, Room 6039, Washington, D.C. 20407

i. Portion of external footprints connected to die attach area and/or seal ring.

j. Terminal #1 position, internal and external.

k. Certification (optional).

l. Method of test and measurements.

m. Electrical, mechanical, environmental requirements.

3. Reference to this specification

4. Any exception to print or specification

5 Dimensions and Permissible Variations

5.1 The dimensions of ceramic chip carriers shall conform to those specified in the customer drawing, and be within the outline of JEDEC Publication No. 95.

NOTE: A dimensioning scheme and measurement fixture are under task force review.

5.2 *Critical Material Parameters*

5.2.1 *Ceramic*

5.2.1.1 Alumina, content 90% minimum.

5.2.1.2 *Color* — Dark or white.

5.2.2 *Metallization*

5.2.2.1 Refractory metallization.

5.2.2.2 Plating (if designated) per MIL-M-38510.

5.2.2.3 Nickel per QQ-N-290

5.2.2.4 Gold per MIL-STD-45204, Type III.

5.2.2.5 Gold Plating Quality see SEMI G8.

5.2.3 Braze per MIL-STD-7883.

5.2.4 Lead per MIL-STD-23011.

5.2.4.1 Iron Nickel Cobalt alloy per MIL-M-38510, Type A.

5.2.4.2 Iron Nickel alloy per MIL-M-38510, Type B.

6 Functional Testing

The following tests are recommended for functional evaluation of ceramic chip carriers. (The conditions of acceptance to be negotiated between the customer and the vendor.)

6.1 *Die Attach*

6.2 *Pre-Seal Die Shear* — (See Section 10.1.6.)

6.3 *Wire Bond*

6.4 *Pre-Seal Bond Pull* — (See Section 10.1.7.)

6.5 *Seal*

6.6 *Environmental Test* — (See Sections 10.1.1 through 10.1.13.)

6.7 *Hermeticity* — (See Section 10.1.14) Lid Torque or Shear (for glass seal parts).

6.8 *Post-Seal Bond Pull* — (See Section 10.1.7.)

6.9 *Post-Seal Die Shear* — (See Section 10.1.6.)

7 Incoming Testing

7.1 *Visual* — (See Section 8.)

7.2 *Dimensions*

7.3 *Functional* — (See Section 6.)

7.4 *Standard Tests*

7.4.1 *Electrical* — (See SEMI G25.)

7.4.2 *Gold Plating Quality* — (See SEMI G8.)

7.4.3 *Trim*

7.4.4 *Lead Integrity* —(See Section 10.1.15.)

7.4.5 *Solderability* — (See Section 10.1.16.)

8 Visual

8.1 *Applicable Definitions*

blister (bubble) ceramic — Any separation within the ceramic which does not expose underlying ceramic material.

blister (bubble) metal — Any localized separation within the metallization or between the metallization and ceramic which does not expose underlying metal or ceramic material.

burr — An adherent fragment of excess parent material at the component edge.

chip — A region of ceramic missing from the surface or edge of a package which does not go completely through the package. Chip size is given by its length, width, and depth from a projection of the design plan-form (see Figure 2).

crack — A cleavage or fracture, internal or external.

die attach surface — See Figure 3.

discoloration — Any non-uniform color change of the package plating.

foreign material — An adherent particle other than parent material of that component.

LSI — Large scale integration.