# SEMI G61-94
# SPECIFICATION FOR COFIRED CERAMIC PACKAGES

## 1 Preface

1.1 *Purpose* — This specification defines the materials and acceptance criteria for high-temperature, cofired ceramic packages.

1.2 *Scope* — The criteria detailed in this specifiication apply to the following package outlines registered with, or specified by JEDEC (see Publication 95), EIAJ, or MIL-STD-1835 specifications:

Chip Carriers (Leadless or Leaded)

Dual-in-Line Packages (Sidebrazed)

Flat Packs (Top or Bottom Brazed)

Grid Arrays (Land/Ball or Pin)

NOTE 1: Packages not meeting these specifications may also use the criteria as appropriate.

This document consolidates the criteria for all cofired packages so that package amnufacturing and inspection may be simplified and costs reduced.

1.3 *Units* — U.S. Customary (inch-pound) or metric (SI) units may be used at the customer's discretion. This specification uses U.S. Customary units as the prime unit. In the drawings, only U.S. Customary units are detailed.

## 2 Applicable Documents

2.1 *Order of Precedence* — To avoid conflicts, the order of precedence when ordering packages shall be as follows:

Purchase Order

Customer's Package Drawings

This Specification

Reference Documents

Related Documents

2.2 *Referenced Documents*

2.2.1 *SEMI Specifications*

*SEMI G6* — Seal Ring Flatness

*SEMI G8* — Gold Plating — Temperature Resistance

*SEMI G23* — Measuring the Inductance of Package Leads

*SEMI G24* — Measuring the Lead-to-Lead and Loading Capacitance of Package Leads

*SEMI G25* — Measuring the Resistance of Package Leads

*SEMI G30* — Test Method, Junction-to-Case Thermal Resistance Measurements on Ceramic Packages

*SEMI G35* — Test Methods for Lead Finishes on Semiconductor (Acitve) Devices

2.2.2 *ANSI Specifications*[1]

*ANSI Y14.5M* — Dimensioning and Tolerancing

2.2.3 *ASTM Specifications*[2]

*ASTM B 568* — Measurement of Coating Thickness by X-Ray Spectrometry

*ASTM E 18* — Test Methods for Rockwell Hardness and Rockwell Superficial Hardness of Metallic Materials

*ASTM E 165* — Liquid Penetrant Inspection Method

*ASTM E 384* — Test Method for Microhardness of Materials

*ASTM F 109* — Surface Imperfections on Ceramics

2.2.4 *JEDEC Specifications*[3]

*Pub. No. 95* — Registered and Standard Outlines for Semiconductor Devices

2.2.5 *Military and Federal Specifications*[4]

*MIL-STD-7883 — Brazing*

*MIL-STD-38510 — General Spec. for Microcircuits*

*MIL-G-45204 — Gold Plating — Electrodeposited*

*QQ-N-290A — Nickel Plating (Electrodeposited)*

2.2.6 *EIAJ Specifications*

2.3 *Related Documents*

2.3.1 *Military and Federal Specifications*

*MIL-STD-105* — Sampling Procedures and Tables for Inspection by Attributes

1 ANSI, 1430 Broadway, New York, NY 10018

2 American Society of Testing Materials, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959

3 JEDEC, 2001 Eye Street N.W., Washington D.C. 20006

4 Military Standards, Naval Publications and Form Center, 5801 Tabor Avenue, Philadelphia, PA 19120

## 3 Definition of Terms

3.1 *blister (bubble) ceramic* — an enclosed, localized separation within or between the layers of a ceramic package that does not expose an underlying layer of ceramic or metallization.

3.2 *blister (bubble) metallization* — an enclosed, localized separation of a metallization layer from its base material (such as ceramic or another metal layer) that does not expose the underlying layer.

3.3 *braze* — in semiconductor packages, an alloy used to attach pins, leads, seal rings and heat sinks/studs to the package.

3.4 *burr* — an adherent fragment of parent material at a component edge. In leadframes, the metal burr, due to the stamping operation, may be in the horizontal or vertical direction to the surface. In ceramic packages, this type of characteristic is called a fin.

3.5 *castellations* — metallized semi-circular channels on chip carrier edges which provide contact between internal package metallization traces and the external test pads. These castellations provide for improved solder fillets during attachment to a circuit board (see Figure 1).

3.6 *cavity-down packages* — packages where the die surface faces the mounting board. (See Figure 2 for the pin grid array packages in the cavity-down configuration. It is more usual to refer to the chip carrier mounting surfaces as the seating planes. In this cavity orientation, the seating plane is Seating Plane 2 per JEDEC JC-11.)

3.7 *cavity-up packages* — packages where the die surface faces away from the mounting board (see Figure 2 or Seating Plane 1 for chip carriers).

3.8 *chip* — region of material missing from a component (e.g., ceramic from a package, or solder from a preform). The region does not progress completely through the component and is formed after the component is manufactured. Chip size is defined by its length, width and depth from a projection of the design platform. Also called chipout (see Figure 1).

3.9 *co-fired* — in the manufacturing of some types of ceramic packages, the technology used to join together various ceramic layers and metallization patterns screened onto those layers by simultaneous firing at high temperature.

3.10 *contact pad* — in a leadless chip carrier or land grid array, the metallized areas on the bottom of the package that provide contact point between the internal leads and connecting external circuitry. They are also used for electrical test pads.

3.11 *crack* — a cleavage or fracture that extends to the surface of a semiconductor package or solder preform. The crack may or may not pass through the entire thickness of the package or preform.

3.12 *critical seal area (ceramic)* — on a semiconductor package, the area bounded by the shortest nominal design distance from the largest cavity, usually the wire bond cavity, to the edge of the package or ceramic layer forming the seal area.

3.13 *critical seal area* — metallization or metal ring — The entire area of the seal ring; it applies to plated refractory metal or a metal ring.

3.14 *critical seal path (ceramic)* — on a semiconductor package, the shortest nominal design distance from the largest cavity, usually the wire bond cavity, to the edge of the package or ceramic layer forming the seal area.

3.15 *delamination* — in a co-fired ceramic package, chip carrier, pin grid array, etc., the separation of one ceramic layer from another.

3.16 *element (packaging)* — part of a semiconductor package feature (e.g., package leads have braze paddle/stand-off and contact elements, pins have the nail head/braze area and contact elements).

3.17 *fin* — on a ceramic package or cap, a fine feathery-edged projection of parent ceramic material on the corner of the ceramic body.

3.18 *flatness* — in a ceramic package or leadframe, the allowable deviation of a surface from a defined reference plane. The tolerance zone is defined by two parallel planes within which the surface must lie.

3.19 *foreign material* — an adherent particle that is not parent material of the component. Adherence means that the particle cannot be removed by an air or nitrogen blast at 20 psi.

3.20 *heat exchange area* — a metallized region on one major surface of the package to which heat sinks may be attached by brazing, soldering, or adhesive resin.

3.21 *layer* — on a cofired ceramic package, the body is made from layers of ceramic or metallized ceramic. The layers are defined by their functionality, and several ceramic layers may be described as comprising one functional layer if all are common in plan-form and function (e.g., die attach cavity) (see Figure 4).

3.22 *lead offset* — in brazed lead ceramic packages, the variation in position of the centerline of the lead with reference to the centerline of the braze pad to which it is mounted.

3.23 *lead sweep* — lead movement, measured with respect to a datum, perpendicular to the top or bottom of the package that passes through the designed mid-point of the lead where the lead is attached to the package (e.g., side-brazed laminates), or where the lead exits the package body (e.g., plastic dual-in-line packages). The movement is viewed from the side of the package, not the ends.

3.24 *lead-to-lead separation* — the distance between adjacent leads when measured from their centerlines at the point of connection to the package.

3.25 *lead tweeze* — lead movement, measured with respect to a datum, perpendicular to the top or bottom of the package that passes through the designed mid-point of the lead where the lead is attached to the package (e.g., side-brazed laminates), or where the lead exits the package body (e.g., plastic dual-in-line packages). The movement is viewed from the ends of the package, not the side and the lead movement is from the edges of the package in toward the centerline of the package.

3.26 *metallization void* — the absence of a clad, evaporated, plated or screen-printed metal layer or braze from a designated area. Also called metal or plating void.

3.27 *peeling (flaking)* — any separation of a plated, vacuum-deposited, or clad metal layer from the base metal of a leadframe, pin heatsink, or seal ring, from an underplate, or from a refractory metal on a ceramic package. Peeling exposes the underlying metal.

3.28 *pin offset* — the variation in position from the centerline of the pin to the centerline of the braze pad to which it is mounted.

3.29 *pin sweep* — pin movement, measured with respect to a datum, perpendicular to the top or bottom of the package that passes through the designed mid-point of pin where the pin is attached to the package (e.g., pin grid arrays). The movement is viewed form the side of the package, not the ends.

3.30 *pin-to-pin separation* — the distance between adjacent pins when measured from their centerlines at the point of connection to the package.

3.31 *pin tweeze* — pin movement, measured with respect to a datum, perpendicular to the top or bottom of the package that passes through the designed mid-point of pin where the pin is attached to the package (e.g., pin grid arrays). The movement is viewed form the ends of the package, not the side and the pin movement is from the edges of the package in toward the centerline of the package.

3.32 *pit* — in semiconductor packages, plastic or ceramic, or in the leadframes, a shallow depression or crater. The bottom of the depression must be visible in order for the term to apply. A pit is formed during component manufacture (see Figure 3).

3.33 *porous surface* — an uncompacted ceramic surface often showing fine pits.

3.34 *projection* — on a semiconductor package (plastic or ceramic), leadframe or preform, and irregularly raised portion of a surface indigenous to the parent material.

3.35 *pullback* — on a semiconductor package, the linear distance between the edge of a cavity cut into a ceramic layer and the first measurable glass or metallization layer interface coated onto the top surface of that layer. The total pullback may be the result of the high temperature processing required to manufacture the package or to coat the surface. It may also be the result of design considerations (see Figure 5).

3.36 *rundown* — on a semiconductor package, the linear distance from the upper surface of a ceramic cavity layer to the bottom point of the overhang into the cavity, of a sealing glass or metallization layer that has been screened onto that surface (see Figure 5).

3.37 *scrape* — the irregular removal of a deposited layer from a base material by a shearing action from another surface such that the base material is exposed over an extended area. It can also apply to the removal of surface layers from a material. The material removed from the scraped area may build up at the edges of the scrape. The deposited layer may be a metal or glass.

3.38 *seal area* — on a semiconductor package, the area designated for sealing a cover or lid to a cofired ceramic package, or a cap to a cer-DIP or cer-pack base. In the case of a co-fired ceramic package the seal area may be either bare ceramic for glass sealing or a metallized area for solder sealing. The metallized seal area may be a plating over refractory metallization or a metal ring, usually iron-nickel-cobalt or iron-nickel alloys, brazed to the refractory metal.

3.39 *seating plane* — in plug-in packages such as dual-in-line (side-brazed or cer-DIP) or pin grid arrays, the plane defined by the three lowest stand-off features on the lead or pins as measured from the bottom of the package, or in the absence of these features, by the package base or mounting plane (see Figure 6). The features, such as shoulders or projections, hold the package off the circuit board to which it is mounted. This gap allows solder flux and residues to be cleaned after soldering the device and, in some cases, to allow for sufficient cooling air flow around the device. A prescribed force is used to hold the device in the mounting holes when the seating plane is to be measured.

3.40 *side-to-side misalignment* — the offset of the center lines of corresponding leads or pins from one side of the package to another side.

3.41 *stand-off* — the separation between the base plane and the seating plane that is created by physical features that are usually formed into the pins or leads (see Figure 6). The features may also be called stand-offs.

3.42 *TIR* — total Indicator Reading.

## 4 Ordering Information

Purchase orders for packages furnished to this specification shall include the following items.

4.1 *Current Drawing Revision Detailing*

4.1.1 All dimensions and tolerances per ANSI Y14.5M practices.

4.1.2 Internal metallization trace pattern.

4.1.3 Type and color of ceramic.

4.1.4 *Pin or Lead Material and Hardness* — If applicable.

4.1.5 *Heat Sink/Stud Material and Hardness* — If applicable.

4.1.6 Type, hardness, and thickness of plating in the die and wire bond areas and contact pads.

4.1.7 *Type, Hardness, and Thickness of Plating on Pins or Leads and Heat Sink/Stud* — If applicable.

4.1.8 *Lead Number 1 Identification* — (See Figure 7.)

4.2 Vendor certification requirements.

4.3 Reference to this specification.

4.4 Any additions to, or variations from, this specification.

4.5 Quantity.

## 5 Dimensions

Package dimensions and lead numbering shall conform to the outlines registered with or specified by JEDEC (see Publication 95), EIAJ or MIL-STD-1835, as appropriate. Package manufacturing tolerances shall be agreed between user and supplier.

## 6 Materials

The definitions, defect criteria, and functional tests described in this specification relate to packages made with the following materials.

6.1 *Ceramic Body*

6.1.1 *Material* — Alumina, beryllia, aluminum nitride, or mullite as specified on the package drawing.

6.1.1.1 *Alumina* — Content to be 90% minimum.

6.1.1.2 *Beryllia* — Content to be 99% minimum. (Packages shall be marked BeO.)

6.1.1.3 *Aluminum nitride* — Content to be agreed between user and supplier.

6.1.1.4 *Mullite* — Content to be agreed between user and supplier.

6.1.2 *Color*

6.1.2.1 *Alumina* — White, black, dark brown, or violet.

6.1.2.2 *Beryllia* — White.

6.1.2.3 *Aluminum Nitride* — White, black, dark brown, or violet.

6.1.2.4 *Mullite* — White, black, dark brown, or violet.

*6.2 Die Attach Pad, Wire Bond Fingers, Contact Pads, and Circuit Trace Metallization*

6.2.1 *Base Material* — Refractory tungsten per MIL-M-38510, Type C. Thickness shall be 0.0003" (0.0076 mm) minimum.

6.2.2 *Finish* — Shall meet the requirements of MIL-M-38510.

6.2.2.1 *Nickel Under Plate (if specified)* — Shall be per QQ-N-290A. Thickness shall be 50 – 350 micro-inches (0.0013 – 0.0089 mm).

6.2.2.2 *Gold Plate* — Shall be per MIL-G-45204, Type III. Thickness shall be 50 – 225 micro-inches (0.0013 – 0.005715 mm).

6.3 *Pins, Leads, and Seal Ring*

6.3.1 *Base Material* — Iron-nickel-cobalt alloy per MIL-M-38150, Type A or iron-nickel alloy per MIL-M-38150, Type B shall be specified on the package drawing.

6.3.2 *Hardness* — 70–85 Rockwell-B for Type A material, 60–80 Rockwell-B for Type B material.

6.3.3 *Finish* — Shall meet the requirements of MIL-M-38510 per Section 6.2.2.

6.4 *Heat Sink/Stud*

6.4.1 *Material*

6.4.1.1 *Heat Sink* — (Forming at least part of the package base and the die attach area) tungsten-copper (composition to be defined on the drawing), iron-nickel (cobalt) alloy per Section 6.3.1 or molybdenum as specified on the package drawing.

6.4.1.2 *Stud* — (Brazed to a metallized area of the ceramic base layer or the heatsink of the package) — copper, tungsten-copper, or kovar as specified on the package drawing.

6.4.2 *Hardness* — Shall be specified on the drawing by agreement between user and supplier.

6.4.3 *Finish* — Shall meet the requirements of MIL-M-38510 per Section 6.2.2.

6.5 *Braze*

6.5.1 *Material* — Silver/copper (72%/28%) or equivalent shall meet the general requirements of MIL-STD-7883.

6.5.2 *Finish* — Shall meet the requirements of MIL-M-38510 per Section 6.2.2.

## 7 Defect Limits

Inspection shall be carried out at 10× magnification with vertical lighting.

The following conditions are cause for rejection.

7.1 *Ceramic Components*

7.1.1 *Cracks* — Any crack is cause for rejection.

7.1.2 *Chips* — See Figure 3.

7.1.2.1 *Corner Chips* — Chip sizes exceeding the limits shown in Table 1. No chip may be deeper than 50% of the package element (the ceramic functional layer) thickness.

**Table 1**

| *Package Dimension inch (mm)* | *Maximum Corner Chip Dimensions (either direction) inch (mm)* |
|---|---|
| ≤0.250 (≤6.35) | 0.020 (0.508) |
| >0.250 – ≤0.500 (>6.35 – ≤12.7) | 0.040 (1.016) |
| >0.500 – ≤1.000 (>12.7 – ≤25.4) | 0.080 (2.032) |
| >1.000 (>25.4) | 0.100 (2.54) |

7.1.2.2 *Edge Chips* — Chip sizes exceeding the limits shown in Table 2. No chip may be deeper than 50% of the package element (the ceramic functional layer) thickness.

**Table 2**

| *Package Dimension in which Chip Occurs inch (mm)* | *Maximum Chip Length and Width inch (mm)* |
|---|---|
| ≤0.250 (≤6.35) | 0.020 (0.508) |
| >0.250 – ≤0.500 (>6.35 – ≤12.7) | 0.040 (1.016) |
| >0.500 – ≤1.000 (>12.7 – ≤25.4) | 0.080 (2.032) |
| >1.000 (>25.4) | 0.100 (2.54) |

7.1.2.3 Chips exposing a buried metallized area excluding the plating buses which are exposed when packages are separated from the manufacturing arrays.

7.1.2.4 *Critical Seal Area (ceramic)* — Any chip reducing the critical seal path length, at any point, by more than 30% of the nominal design dimension.

No more than three chips, each of which reduces the seal path length by more than 10% but less than 30%, are allowed in this area. Each chip's length shall not exceed the limits shown in Table 3.

**Table 3**

| *Seal Ring Dimension in which Chip Occurs inch (mm)* | *Maximum Chip Length inch (mm)* |
|---|---|
| ≤0.250 (≤6.35) | 0.020 (0.508) |
| >0.250 – ≤0.500 (>6.35 – ≤12.7) | 0.040 (1.016) |
| >0.500 – ≤1.000 (>12.7 – ≤25.4) | 0.080 (2.032) |
| >1.000 (>25.4) | 0.100 (2.54) |

7.1.3 *Ceramic Projections* — (bumps and blisters)

7.1.3.1 *Body (non-critical surfaces)* — Any projection, including fins, exceeding 0.005" (0.127 mm) in height, or exceeding 0.002" (0.051 mm) in height and with a surface dimension greater than 0.010" (0.254 mm).

NOTE 2: On surface mount packages, the bottom of the package shall not have any projections exceeding 0.002" (0.051 mm) in height.

7.1.3.2 *Die Attach Areas* — (bare ceramic or screen printed metal area) — Excluding a zone, 0.015" (0.381 mm) wide, around the periphery of the cavity, any projection exceeding 0.001" (0.025 mm) in height or a surface dimension of 0.010" (0.254 mm).

NOTE 3: Exclusion zones around the periphery of die attach areas may be wider on larger packages or when a metal heat sink or stud is brazed to the package and forms the die attach area (Section 7.3). The width of such zones shall be defined on the package drawing by agreement between user and supplier. This note applies to all criteria affecting die attach areas.

7.1.3.3 *Critical Seal Area (printed metal area)* — Any projection exceeding 0.001" (0.025 mm) in height or with a surface dimension exceeding 0.010" (0.254 mm) or 30% of the critical seal length, whichever is the larger.

7.1.3.4 *Critical Seal Area (bare ceramic)* — Any projection exceeding 0.001" (0.025 mm) in height or with a surface dimension exceeding 0.010" (0.254 mm) or 30% of the critical seal path, whichever is the larger.

7.1.3.5 *Wire Bond Fingers* — Any projection in the critical area defined in Figure 8 exceeding 0.0005" (0.0127 mm) in height or a surface dimension of 0.004" (0.102 mm).

7.1.3.6 *Solder Pads, Contact Pads, and Heat Exchange Areas* — Any projection exceeding 0.002" (0.051 mm) in height above the pad, or a surface dimension of 0.010" (0.254 mm).

NOTE 4: Castellation areas of chip carriers are excluded from these criteria because of the manufacturing process. (Layer misalignments, separation techniques, etc. may cause projections which do not affect package quality.

7.1.4 *Pits*

7.1.4.1 *Body (non-critical surfaces)* — Pits exceeding 0.003" (0.076 mm) in depth or a surface dimension of 0.020" (0.508 mm).

7.1.4.2 *Die Attach Areas (bare ceramic or screen printed metal area)* — Excluding a zone, 0.015" (0.381 mm) wide, around the periphery of the cavity, pits exceeding 0.001" (0.025 mm) depth below the surface or a surface dimension of 0.010" (0.254 mm). Acceptable pits shall not cover more than 10% of the surface area.

NOTE 5: Ceramic pits in metallized areas may be covered by metallization, but remain cause for rejection.

NOTE 6: Pits with a depth not exceeding 0.0005" (0.0127 mm) are not rejectable.

7.1.4.3 *Critical Seal Area (bare ceramic or metallized area)* — Pits exceeding 0.001" (.025 mm) depth below the ceramic surface or a surface dimension of 0.010" (0.254 mm). No more than three acceptable pits allowed in this area with a minimum separation of 0.030" (0.762 mm) required between sites. The seal ring width must not be reduced by more than 30% of its designed width at any point. Acceptable pits shall not cover more than 10% of the critical seal area.

7.1.4.4 *Wire Bond Fingers* — Any pit in the critical area defined in Figure 8 exceeding 0.0005" (0.0127 mm) in depth, or any pit exeeding 0.004" (0.102 mm) in a surface dimension.

7.1.4.5 *Solder Pads, Contact Pads, and Heat Exchange Areas* — Pits exceeding 0.002" (0.051 mm) depth below the pad or a surface dimension of 0.010" (0.254 mm). Acceptable pits shall not cover more than 10% of the surface area.

NOTE 7: Pits with a depth not exceeding 0.0005" (0.0127 mm) are not included in this evaluation, regardless of surface dimension.

NOTE 8: Pits in castellation areas are exluded from these criteria because of the manufacturing process.

7.1.5 *Flatness (Camber)*

7.1.5.1 *Package Flatness* — Flatness variation exceeding 0.004 inch/inch (0.004 mm/mm), with a minimum camber specification of 0.002" (0.051 mm).

7.1.5.2 *Die Attach Area Flatness* — Any flatness variations exceeding the limits shown in Table 4.

NOTE 9: These criteria apply to any die attach area ceramic, metallized ceramic, or a heat sink which forms the die attach area.

**Table 4**

| *Die Attach Area (Major Dimension) inch (mm)* | *Flatness (Maximum Allowable TIR) inch (mm)* |
|---|---|
| 0.750 (# 19.05) | 0.002 (0.051) |
| >0.750 (>19.05) | 0.003 inch ( 0.0762 mm) |

7.1.5.3 *Seal Area Flatness* — See Table 5.

NOTE 10: These criteria apply to packages with bare ceramic, metallized ceramic, or a metal ring. Flatness to be measured per SEMI G6.

**Table 5**

| *Seal Ring (Major Dimension) inch (mm)* | *Flatness (Maximum Allowable TIR) inch (mm)* |
|---|---|
| ≤0.500 (≤12.7) | 0.002 (0.051) |
| >0.500 (>12.7 ) | 0.003 (0.076) |

7.1.6 *Delamination* — Any evidence of delamination between ceramic layers which exceeds 0.030" (0.762 mm), in a major dimension, in more than two locations.

NOTE 11: Inspection may also be made by scanning acoustic microscopy per MIL-STD-883, Method 2030, if internal delamination is suspected. Vendor and customer shall agree that such inspection is necessary for package integrity.

7.1.7 *Foreign Material* — Any particulate or film-like foreign material exceeding 0.005" (0.127 mm) height or a surface dimension of 0.020" (0.508 mm). No more than three acceptable sites allowed on the body with a minimum separation of 0.030" (0.762 mm) required between sites.

7.1.8 *Porous Surface* — Packages showing surface poro-sity per ASTM F 109 shall be subjected to seal testing per Section 8.2.4 to verify acceptance.

NOTE 12: Surface porosity may cause inconsistent results at hermeticity testing. Packages which show porosity and fail a hermeticity test may be evaluated per ASTM E 165 to verify the acceptance. Inspection may also be made by scanning acoustic microscopy per MIL-STD-883, Method 2030.

7.2 *Metallized Areas on Ceramic*

7.2.1 *Plating Voids* — (Includes voids due to refractory metal printing defects.)

7.2.1.1 *Die Attach Areas* — Excluding a 0.015" (0.381 mm) wide zone around the periphery of the cavity, voids exceeding a surface dimension of 0.020" (0.508 mm). Acceptable voids shall not cover more than 10% of the surface area.

7.2.1.2 *Seal Ring Area* — Voids exceeding a surface dimension of 0.020" (0.508 mm). The seal ring width must not be reduced by more than 30% of its designed width at any point. Acceptable voids shall not cover more than 10% of the seal ring area.

7.2.1.3 *Wire Bond Fingers* — Any void in the critical area defined in Figure 8.

7.2.1.4 *Internal Lead Traces* — Any void which reduces the width of the trace by more than 50% of its designed width.

NOTE 13: X-ray radiography per MIL-STD-883, Method 2012, or scanning acoustic microscopy per MIL-STD-883, Method 2030, may be used to verify the integrity of covered traces.

NOTE 14: Pits are not cause for rejection, providing any metallization loss does not exceed the 50% criteria.

7.2.1.5 *Solder Pads/Castellations or Contact Pads* — Voids with any dimension larger than 0.010" (0.254 mm) or loss of area exceeding 25%. The connection between a solder pad and the castellation must not be reduced in width by more than 50% of its design width.

7.2.1.6 *Braze Pads* — Voids with any dimension larger than 0.010" (0.254 mm). No more than one visible, acceptable void per pad is allowable after pin or lead attachment.

7.2.1.7 *Heat Exchange Area* — Voids with a surface dimension larger than 0.020" (0.508 mm). Acceptable voids shall not cover more than 10% of the heat exchange area.

7.2.2 *Scratches and Scrapes*

7.2.2.1 *Die Attach Areas* — Excluding a 0.015" (0.381 mm) wide zone around the periphery of the cavity, any buildup of material exceeding 0.001" (0.0254 mm) in height or exposing base metallization (refractory or underplate) so that void criteria are violated.

7.2.2.2 *Seal Ring Areas* — Any buildup of material exceeding 0.001" (0.0254 mm) in height or exposing base metallization (refractory or underplate) so that void criteria are violated.

7.2.2.3 *Wire Bond Fingers* — Any scratch in the critical area defined in Figure 8, which causes metallization build-up exceeding 0.0005" (0.0127 mm) in height or a surface dimension of 0.004" (0.102 mm). In non-critical lead trace areas, any scratch which exposes base metallization (refractory or underplate) across more than 50% of the designed trace width.

7.2.2.4 *Solder Pads/Castellations* — Any scratch which isolates more than 25% of a pad from the castellation by exposure of refractory metallization. Scrapes must not violate the void criteria of Section 7.2.1.5.

7.2.2.5 *Heat Exchange Areas* — Any scratches and scrapes which cause void criteria to be violated (see Section 7.2.1.7).

7.2.3 *Blistering or Peeling of the Metallization* — Any evidence of blistering or peeling.

NOTE 15: Discoloration is not a defect unless a functional test is affected (e.g., wire bonding) (see Section 8).

7.2.4 *Plating Nodules* — Nodules exceeding the criteria for bumps in Sections 7.1.3.2, 7.1.3.3, 7.1.3.4, and 7.1.3.5.

7.2.5 *Refractory Metallization* — Printing and firing defects (see Figure 5).

7.2.5.1 *Metallized Seal Ring Rundown* — Rundown exceeding 25% of the adjacent internal cavity's depth.

7.2.5.2 *Wire Bond Finger Rundown* — Rundown exceeding 25% of the cavity depth or 0.005" (0.127 mm), whichever is smaller.

7.2.5.3 *Wire Bond Finger Pullback* — Pullback exceeding 0.006" (0.152 mm).

7.2.5.4 *Metallization Pattern Separation* — A reduction in pattern separation by more than 50% of the designed separation.

NOTE 16: Pattern separation for chip carrier solder pads may be further specified by agreement between supplier and customer to avoid solder shorting during circuit board assembly.

7.2.5.5 *Seal Ring Pullback* — Pullback exceeding 0.006" (0.152 mm) from the nominal design location from both the cavity and package edge directions.

7.2.6 *Foreign Material* — (Particulate or film-like)

7.2.6.1 *Die Attach Areas (includes bare ceramic die attach areas)* — Excluding a 0.015" (0.381 mm) wide zone around the periphery of the cavity, any foreign material exceeding 0.001" (0.0254 mm) in height or a surface dimension of 0.020" (0.508 mm). Acceptable foreign material shall not cover more than 5% of the die attach area.

7.2.6.2 *Seal Area (includes bare ceramic die attach areas)* — Any foreign material exceeding 0.001" (0.0254 mm) in height or a surface dimension of 0.020" (0.508 mm). The seal ring width shall not be reduced by more than 30% of its width at any point by foreign material. Acceptable foreign material shall not cover more than a total of 10% of the seal ring area.

7.2.6.3 *Wire Bond Fingers* — Any foreign material in the critical area defined in Figure 8.

7.2.6.4 *Solder Pads/Castellations, Contact Pads, and Heat Exchange Areas* — Any foreign material exceeding 0.001" (0.0254 mm) in height or a surface dimension of 0.010" (0.254 mm). Acceptable foreign material shall not cover more than 10% of these areas.

7.3 *Pins, Leads, Metal Seal Rings, or Heat Sinks/Studs*

NOTE 17: If the heat sink is used as the die attach area, the following conditions must not violate the criteria in Sections 7.1 and 7.2 for defect size and accumulation.

7.3.1 *Plating Voids* — Voids, exposing base material or underplate, with any dimension exceeding 0.005" (0.127 mm) or with a total accumulation of more than 5% of the surface area of any pin, lead, heat sink/stud, or braze. If the total accumulation of voids is less than 5% of the area of an element of a package feature, a sample of the defective units shall be submitted to Salt Atmosphere testing per MIL-STD-883, Method 1009, Condition A. If the sample passes this test, the lot shall be acceptable

Voids, exposing base material or underplate, in the seal ring plating violating the criteria of Section 7.2.

7.3.2 *Scratches or Scrapes* — Any buildup of the metallization, or exposure of the base material or underplate, which exceeds 5% of the surface area of any pin, lead, heat sink/stud, or braze. If the total accumulation of scratches or scrapes is less than 5% of the area of an element of the package feature, a sample of the defective units shall be submitted to salt atmosphere testing per MIL-STD-883, Method 1009, Condition A. If the sample passes this test, the lot shall be acceptable.

7.3.3 *Nicks*

7.3.3.1 Any nick in pins or leads exceeding 10% of the diameter or thickness.

7.3.3.2 Any nick in the heat sink/stud which violates void or pit criteria.

7.3.3.3 Any nicks in the seal ring area which violate the criteria of Section 7.2.

7.3.4 *Pits*

7.3.4.1 *External Surfaces* — Any pit exceeding 0.005" (0.127 mm) in depth or 0.010" (0.0254 mm) in a surface dimension.

Metal seal rings shall have no more than three acceptable sites, and there must be a minimum separation of 0.030" (0.762 mm) required between acceptable sites. The width of the seal ring must not be reduced by more than 30% of its designed width at any point. Acceptable pits shall not cover more than 5% of heat sinks/studs. Acceptable pits shall not cover more than 25% of pins or leads.

7.3.4.2 *Internal Surfaces* (Die Attach Areas) — Any pit exceeding 0.001" (0.0254 mm) in depth and violating the plating void criteria per Section 7.2.1.1.

7.3.5 *Plating Nodules* — Any nodule exceeding the criteria for burrs in Section 7.3.7.

7.3.6 *Foreign Material* — Any particulate or film-like (stain) foreign material exceeding 0.001" (0.025 mm) in height or an accumulation of sites in excess of 5% of the surface area of any pin, lead, or heat sink/stud. Any foreign material reducing the separation between two active metal areas to less than 50% of the designed separation.

7.3.7 *Burrs* — Any burr in excess of 0.002" (0.051 mm) height or 0.005" (0.127 mm) in a major dimension.

7.3.8 *Blistering or Peeling* — Any evidence of blistering or peeling.

NOTE 18: Blistering and peeling on a lead frame tie-bar are acceptable. Discoloration is not cause for rejection unless a functional test is affected (e.g., solderability).

7.3.9 *Corrosion* — Any evidence of corrosion.

7.3.10 *Braze*

7.3.10.1 *Excessive Braze* — Any separation between active metal areas which is reduced to less than 50% of the designed separation.

Any excessive braze which interferes with the intended use of the package (e.g., excessive braze height which prevents proper seating of a package).

7.3.10.2 *Insufficient Fillet* — Pin, lead, heat sink/stud braze areas where more than 25% of the periphery is not covered by the braze fillet, provided the voided areas do not extend under the brazed component.

Any pin, lead, heat sink/stud braze areas where more than 5% of the periphery is not covered by the braze fillet and any voids extend under the brazed element.

7.3.11 *Mechanical Damage*

7.3.11.1 Broken, Kinked, or Missing Pins or Leads

7.3.11.2 *Twist* — Any pin or lead twisted by more than 10° from the untwisted condition.

7.3.11.3 *Pin or Lead Sweep* — Any location of the tip of the pin or lead exceeding 0.010" (0.0254 mm) away from the vertical (or horizontal, for flat packs) datum passing through the mid-point of the pin or lead at the point of brazing to the contact pad.

7.3.11.4 *Pin or Lead Tweeze* — Any location of the tip of the pin or lead exceeding 0.010" (0.0254 mm) away from the vertical datum passing through the mid-point of the pin or lead at the point of brazing to the contact pad.

7.3.11.5 *Threads* — Any damage to the threads on studs.

7.4 *Package Construction*

7.4.1 *Pins and Leads* — Location.

7.4.1.1 *Pin or Lead Offset* — Any offset from the pin or lead true position exceeding 0.005" (0.127 mm).

7.4.1.2 *Lead-to-Lead or Pin-to-Pin Separation* — Any separation exceeding 10% of the designed separation, up to an allowable maximum of 0.010" (0.254 mm).

7.4.1.3 *Side-to-Side Misalignment* — Any misalignment exceeding the limits shown in Table 6.

**Table 6**

| *Package Type* | *Maximum Allowable Side-to-Side Misalignment inch (mm)* |
|---|---|
| Dual-in-Line | 0.010 (0.254) |
| Flat Packs | 0.005 (0.127) |
| Leaded Chip Carriers | 0.005 (0.127) |
| Pin Grid Arrays | 0.005 (0.127) |

NOTE 19: During inspection, the combination of offset, separation, and side-to-side misalignment shall also meet limits agreed between user and supplier.

7.4.2 *Ceramic Layer Misalignment* — Any misalignment between layers exceeding 0.005" (0.127 mm) in either the X or Y planes.

7.4.3 *Metallization Alignment to Ceramic* — Any misalignment exceeding the limits defined on the package drawing.

## 8 Incoming Inspection and Functional Tests

8.1 *Incoming Inspection* — Packages shall be inspected in the following sequence.

8.1.1 Dimensional inspection to the requirements of Section 5. All dimensions shall be measured by techniques agreed between supplier and customer except as follows:

8.1.1.1 Seal ring flatness shall be measured per SEMI G6.

8.1.2 Visual inspection per Section 7.

8.1.3 *Metallization* — Plating.

8.1.3.1 *Thickness* — Shall be measured by x-ray fluorescence per ASTM B 568. The location of the areas to be measured, which include die and wire bond and seal ring areas, the tolerance and acceptable standards shall be agreed between user and supplier.

8.1.3.2 *Temperature Resistance* — Shall be evaluated per SEMI G8.

8.1.3.3 *Plating Hardness* — Die and wire bond and seal ring areas — shall be measured per ASTM B 578 to limits defined by MIL-G-45204 if specified by agreement between vendor and customer.

8.1.3.4 *Pin, Lead, Solder Castellation, or Solder Pad Solderability* — Shall be tested per SEMI G35.

8.1.4 *Pin, Lead, Seal Ring, or Heat Sink/Stud Hardness* — Shall be measured per ASTM E 18 if specified by agreement between vendor and customer.

8.1.5 *Pin or Lead Integrity* — Shall be evaluated per MIL-STD-883, Method 2004.

NOTE 20: After each test, the plating shall be evaluated for continuity per SEMI G35.

8.1.5.1 *Tension* — Per Test Condition A except as shown in Table 7.

**Table 7**

| *Pin/Lead Dimension inches (mm)* | *Minimum Tension lbs (kg)* |
|---|---|
| Round Pin | |
| 0.008 (0.203) | 1.0 (0.455) |
| 0.018 (0.457) | 10.0 (4.55) |
| Rectangular Lead | |
| $0.018 \times 0.010$ ($0.457 \times 0.254$) | 10.0 (4.55) |

8.1.5.2 *Fatigue* — Per Test Condition B2 if specified by agreement between user and supplier.

8.1.5.3 *Torque* — Per Test Condition C1 if specified by agreement between user and supplier.

8.1.5.4 *Solder Pad Adhesion* — Per Test Condition D if specified by agreement between vendor and customer.

8.1.6 *Stud Integrity* — Shall be evaluated per MIL-STD-883, Method 2004, Test Condition C2. Torque to be agreed between user and supplier.

8.1.7 *Heat Sink Integrity* — Test shall be agreed between user and supplier.

8.2 *Functional Testing* — The sequence of functional testing shall be as shown in Figure 9. (Packages shall be sequentially subjected to all tests.)

NOTE 21: All procedures used to functionally test the components shall be agreed between user and supplier.

8.2.1 *Die Attach*

8.2.1.1 *Visual Inspection*

*Eutectic Bonding* — Visually inspect the alloy wet-out after die attach. The minimum wet-out requirement shall be 100% of the die perimeter.

*Silver Glass, Epoxy, or Polyimide Bonding* — 100% die perimeter coverage shall be required.

NOTE 22: 100% coverage for resin bonding is not a function of package acceptability but is required to standardize die testing. The inability of the resins to wet the surface of the die attach area due to contamination is cause for rejection.

8.2.1.2 *Die Shear Test* — Perform destructive testing per MIL-STD-883, Method 2019.

8.2.1.3 *Radiographic Inspection for Voids* — Perform inspection per MIL-STD-883, Method 2012.

8.2.1.4 *Ultrasonic Inspection for Voids, Delamination, and Cracks* — Perform inspection per MIL-STD-883, Method 2030.

NOTE 23: These tests may also be performed after environmental testing. In the case of very large die, the die shear test may not be appropriate to fully evaluate the package. In these cases, die sizes or alternative tests agreed between user and supplier shall be used. In the case of eutectic die attach, the results from these tests may also be indicative of poor functionality of the gold die attach metallization.

8.2.2 *Wire Bond* — On wire bonds that meet the requirements of MIL-STD-883, Method 2010, perform destructive testing per MIL-STD-883, Method 2011, Test Condition D. Bonds which cause lifted metallization from the wire bond fingers or which fail the pull test criteria shall be cause for package rejection.

NOTE 24: The inspection level A or B, for Method 2010, shall be agreed between vendor and customer. The pull test shall be performed at pre-seal and post-seal. The minimum average pull strength, standard deviation, and acceptable rupture modes shall be agreed between user and supplier.

8.2.3 *Seal*

8.2.3.1 *Visual Inspection* — Criteria shall be agreed between user and supplier.

8.2.4 *Hermeticity* — Performed per MIL-STD-883, Method 1014, Test Condition A or B and C, the package must maintain hermetic integrity after each environmental test or sequence of tests.

NOTE 25: Internal water-vapor content may also be measured per MIL-STD-883, Method 1018.

8.2.5 *Environmental Testing* — Environmental evaluation shall include, but not be limited to, the following tests.

NOTE 26: The sequence of testing and the sample sizes for each sub-group shall be agreed between user and supplier. Packages with heat sinks or studs require the environmental tests to be evaluated on an individual basis. The materials, form factor, and method of attachment may not be suitable for the tests noted due to the generation of overly severe stresses. The appropriate tests shall be agreed between user and supplier.

8.2.5.1 *Temperature Cycle* — Per MIL-STD-883, Method 1010, Condition C on packages without a heat sink or stud, or Condition B for packages with a heat sink or stud.

8.2.5.2 *Thermal Shock* — Per MIL-STD-883, Method 1011, Condition C.

8.2.5.3 *Vibration Fatigue* — Per MIL-STD-883, Method 2005, Test Condition B for packages without a heatsink.

8.2.5.4 *Mechanical Shock* — Per MIL-STD-883, Method 2002, Test Condition B for packages without a heatsink.

8.2.5.5 *Constant Acceleration* — Per MIL-STD-883, Method 2001, Test Condition A for packages without a heatsink.

NOTE 27: Y1 axis only for cavity-up packages, Y2 axis only for cavity-down packages.

8.2.5.6 *Additional Testing* — Additional tests performed during package qualification may include evaluation of electrical and thermal characteristics, corrosion resistance, and alpha particle emissions. These tests may be performed on a periodic basis to maintain package qualification. These tests may include, but are not limited to, the following.

*Insulation Resistance* — Per MIL-STD-883, Method 1003, to test conditions agreed between user and supplier.

*Lead Inductance* — Per SEMI Test Method G23 or using an impedance analyzer by a method agreed between user and supplier.

*Lead-to-Lead Capacitance* — Per SEMI Test Method G24.

*Lead Resistance* — Per SEMI Test Method G25.

*Junction-to-Case Thermal Resistance* — Per SEMI G30 or a wind tunnel method agreed between user and supplier.

Alpha particle emission shall be tested by a method and to limits agreed between user and supplier.

*Salt Atmosphere (Corrosion) Testing* — Per MIL-STD-883, Method 1009, Condition A.

## 9 Sampling

The sampling plans shall be agreed between user and supplier.

## 10 Packaging and Packing List

10.1 *Packaging* — The shipping containers and materials shall be suitably designed to provide the components with protection against normal transportation damage risks which include crushing, abrasion, and spillage and exposure to moisture and other corrosive gases.

The inner packing materials must not cause particulate contamination on the components and shall be clean-room compatible as defined by the user. The components, in packing trays, shall be sealed in a vacuum bag with a dessicant.

10.2 *Packing List*

10.2.1 *Internal Packages* — Each internal package shall be marked as follows.

Customer's Part Number

Customer's Purchase Order Number

Drawing Number (user's and supplier's, if appropriate)

Supplier Shipping Lot Number

Quantity

Date of Manufacture

10.2.2 *External Packages* — The packing list, located on the outside of the container, shall provide the following information.

User's Part Number

User's Purchase Order Number

Quantity

Shipping Date

Any specific instructions for receiving dock personnel.

## 11 Certification

11.1 Upon request of the user in the contract or purchase order, a supplier's certification that the product was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment. However, if the user does perform inspection and tests on a certified shipment and the product fails to meet the requirements, the product is subject to rejection.

11.2 If the user and supplier agree, the product may be certified as capable of meeting this specification. In this context, capable of meeting signifies that the vendor is not required to perform all the inspections and tests. However, if the user does perform inspection and tests on such product and it fails to meet the requirements, the product is subject to rejection.

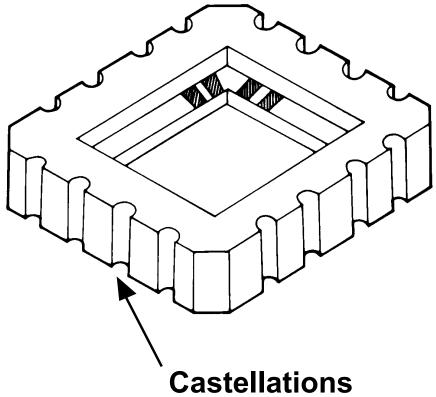



**Figure 1**

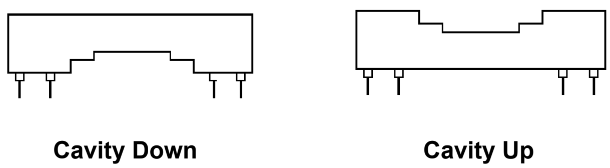



**Figure 2**

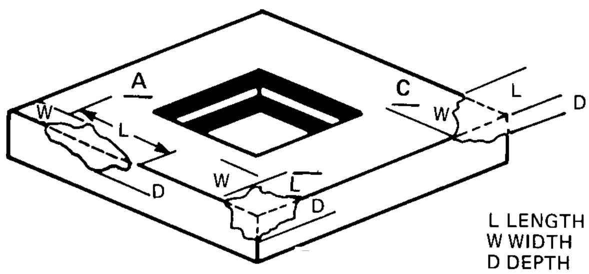
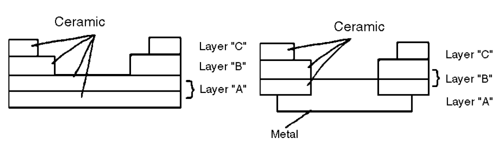



**Figure 3**




Functional layers shall be designated by letter beginning with "A" as the layer nearest the terminal insertion plane. Layers, regardless of function, shall be designated by succeeding letter (B, C, D, etc.) as they are progressively remote from the insertion plane. Functional layers may be manufactured from two or more ceramic layers.

**Figure 4**

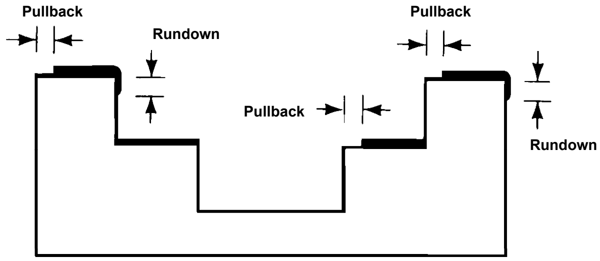



**Figure 5**

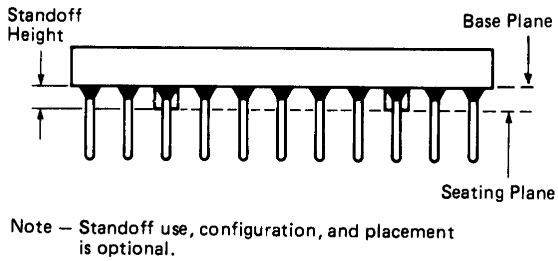
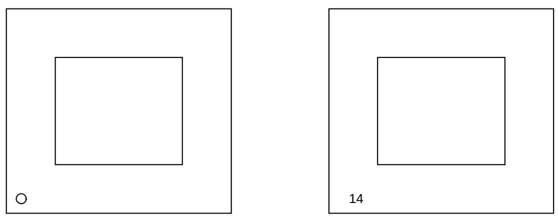



**Figure 6**




NOTE: A geometric symbol used to indicate lead number 1 indicates that all leads are isolated from the die attach pad.

NOTE: Lead Number 14 is common to the die attach pad and indicates the position of lead number 1.

**Figure 7**

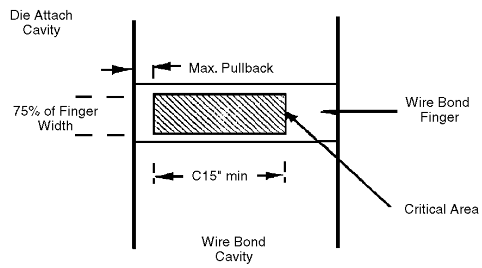
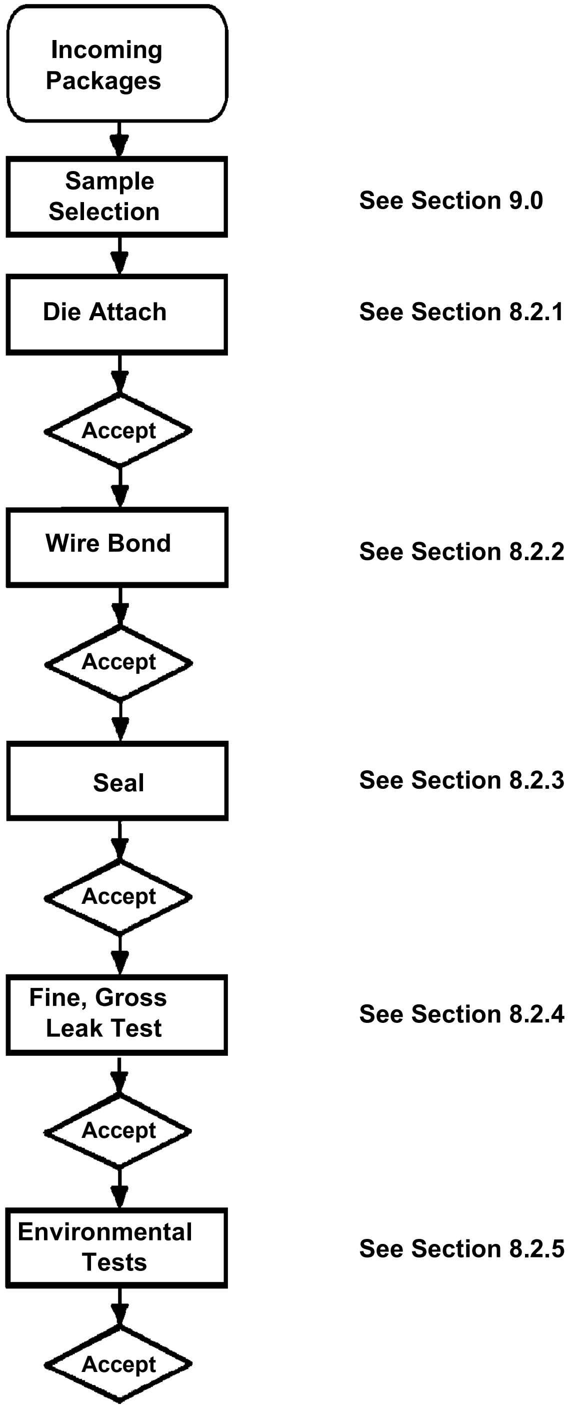



**Figure 8**



Incoming Packages
Sample Selection
See Section 9.0
Die Attach
See Section 8.2.1
Accept
Wire Bond
See Section 8.2.2
Accept
Seal
See Section 8.2.3
Accept
Fine, Gross Leak Test
See Section 8.2.4
Accept
Environmental Tests
See Section 8.2.5
Accept


**Figure 9**

**NOTICE:** These standards do not purport to address safety issues, if any, associated with their use. It is the responsibility of the user of these standards to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use. SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

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# SEMI G62-95 (Reapproved 0302)
# TEST METHOD FOR SILVER PLATING QUALITY

This test method was technically appoved by the Global Physical Interfaces and Carriers Committee and is the direct responsibility of the Japanese Physical Interfaces and Carriers Committee. Current edition approved by the Japanese Regional Standard Committee on November 26, 2001. Initially available at www.semi.org December 2001; to be published March 2002. Originally published in 1995.

## 1 Purpose

1.1 This test method describes procedures to determine silver plating quality.

## 2 Scope

2.1 These methods apply to silver plating on leadframes for plastic packages. Applicable plating styles are listed in Table 1.

**Table 1 Plating Style**

| *Plating Style* | *Description* |
|---|---|
| Overall Plating | Plating covers the whole leadframe area. In some situations, the leadframe may be quoted as having overall plating, but the rails will be unplated in order to save plating costs. |
| Ring Plating | Only inner leads plated on top surface. |
| Ring-Tip Plating | Only wire bonding areas of inner leads plated. |
| Spot Plating | Only die pad and inner leads plated on top surface. |
| Spot Plating (both sides) | Die pad and inner leads are plated on both the top and bottom surfaces of the leadframe. |
| Tip Plating | Only die pad and wire bonding areas plated. |
| W-Ring Plating | Only inner leads plated on top surface and around die pad. |

2.2 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability or regulatory limitations prior to use.

## 3 Units

3.1 This test method uses SI units.

## 4 Referenced Standards

4.1 *SEMI Documents*

SEMI G55 — Test Method for Measurement of Silver Plating Brightness

SEMI G56 — Test Method for Measurement of Silver Plating Thickness

4.2 *Military Specifications*[1]

MIL-M-38510 — General Specification for Microcircuits

## 5 Terminology

5.1 *area variation* — The variation between the defined and actual plated area.

NOTE 1: Oversized plating area is an area larger than the specified area. Undersized plating area is an area smaller than the specified area.

5.2 *attached silver particles* — Small silver particles which are attached to the normal plated surface during the plating process.

5.3 *bleed out, back side* — Plating on the back of leadframe caused by seepage of the plating solution beyond the mask.

5.4 *bleed out, side* — Plating occurring on the sides of leadframe features.

5.5 *bleed out, surface* — Seepage of the plating solution beyond the mask on the top surface of the leadframe increasing the plated area.

5.6 *bleed out, epoxy* — The separation of the resin component from the filled epoxy resin such that it creeps on the die pad beyond the outline of resin fillet.

5.7 *blister (metal)* — An enclosed, localized separation of the plating metallization from the base material or from another layer of plating which can be depressed with a sharp instrument.

NOTE 2: This may occur during plating or after application of heat.

5.8 *burnt deposit* — Plated surface is too rough.

5.9 *contamination* — Three-dimensional alien material adhering to a surface.

5.10 *corrosion* — Electrochemical degradation of the material usually exhibited by discoloration such as rust.

1 Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA. Telephone: 215.697.3321

5.11 *discoloration* — Any change in the color of the metallization, as detected by the naked eye. This may occur on as plated or after application of heat.

5.12 *excessive plating* — Plating exists outside the specified area.

5.13 *foreign material* — An adherent particle other than parent material of the component.

NOTE 3: Adherent denotes inability to be removed with an air or nitrogen blow-off at 20 psi.

5.14 *incomplete plating* — Plating is missing from any part of the designated area.

5.15 *leadframe top surface* — The active side of the leadframe, the surface used for die attach and wire bonding.

5.16 *nodule (of plated particle)* — A protrusion or lump of plating material above the plated surface.

5.17 *plating nonuniformity* — The lack of consistency of brightness of silver as plated, or after the application of heat. These changes in the plated grain structure causes the inconsistency.

5.18 *peeling* — The lifting of metallization from a surface.

5.19 *pit (of plating)* — A hole or depression extending below the surface of the plating.

5.20 *scratch (on plating)* — A surface deformation which exposes underlying metallization.

5.21 *spot-sparing* — A stain-like discoloration occurring after the application of heat.

5.22 *step plating* — Plateau-like plating having more than one level.

5.23 *spot plating misalignment* — The variation between the defined and actual center lines of the plated area.

5.24 *tape test* — A metallization layer adhesion test technique using adhesive tape to apply a peel force to the layer. This test may be applied on plated material or after the application of heat.

5.25 *whisker* — A plating metal burr-like filament attached to the surface of the plating.

## 6 Summary of Method

6.1 Various test methods are described or referenced to determine silver plating quality for the following items:

- Plating Area
- Plating Thickness
- Plating Brightness
- Visual Inspection
- Functional Test

## 7 Interferences

7.1 Avoid contaminating the silver plated surface prior to performing the test. Such contamination may affect visual appearance and die attach, wire bonding, and solderability functional tests.

## 8 Equipment

8.1 GAM densitometer or equivalent

8.2 X-Ray Fluorescence

8.3 Microscope with a 40× maximum magnification.

8.4 Heater block, hot plate or oven (furnace)

## 9 Sampling

9.1 Sampling plans shall be agreed between user and supplier.

## 10 Test Sequence

10.1 When the test methods are used at incoming inspection, the sequence of tests shall be as follows:

10.1.1 *Plating Area* — See Section 11.1.

10.1.2 *Plating Thickness* — See Section 11.2.

10.1.3 *Plating Brightness* — See Section 11.3.

10.1.4 *Visual Inspection* — See Section 11.4.

10.1.5 *Heat Test* — See Section 11.5.

10.1.6 *Functional Test* — See Section 11.6.

## 11 Test Procedures

11.1 *Plating Area*

11.1.1 Measurements may be made by using a glass scale, shadow scope, or microscope.

11.1.2 Measurement items are listed below:

11.1.2.1 Area variation

11.1.2.2 Spot plating misalignment

11.2 *Plating Thickness*

11.2.1 Plating thickness shall be measured at a point on the inner lead or the center point of the die pad.

NOTE 4: The location of the thickness test shall be agreed between user and supplier.

11.2.2 Thickness measurements may be made using X-Ray Fluorescence per SEMI G56.

11.3 *Plating Brightness*

11.3.1 Plating brightness shall be measured at the center point of the die pad.

NOTE 5: If leadframes do not have a plated die pad, the location of the brightness test shall be agreed between user and supplier.

Plating brightness shall be measured using a GAM densitometer or equivalent per SEMI G55.

11.4 *Visual Inspection*

11.4.1 Visual inspection may be performed with the naked eye or a microscope with up to 40× maximum magnification, as required to confirm results.

11.4.2 Visual inspection shall be performed before and after functional testing.

11.4.3 Inspection items are listed below.

1. attached silver particles
2. blister
3. bleed-out
4. burnt deposit
5. contamination
6. corrosion
7. discoloration
8. excessive plating
9. foreign material
10. incomplete plating
11. nodule
12. plating nonuniformity
13. peeling
14. pit
15. scratch
16. spot-sparing
17. step plating
18. whisker

11.5 *Heat Test*

11.5.1 *Conditions* — The conditions in Table 2 shall be used to heat test silver plated leadframes.

**Table 2 Heat Test Condition**

| *Leadframe Material* | *Bake Temperature* | *Bake Time (min.)* |
|---|---|---|
| Iron-Nickel Alloy per MIL-STD-38510, Type B | 400° C ± 5° C | 3 min. + 10 (-0) sec. |
| Cu Alloy | 300° C ± 5° C | 3 min. + 10 (-0) sec. |
| Taped Leadframe | 275° C ± 5° C | 3 min. + 10 (-0) sec. |

11.5.2 The test may be carried out on a heater block or hot plate, or in an oven (furnace). The heat capacity of the test equipment must be sufficient to avoid temperature swings outside the specified limits when the test is started.

NOTE 6: When using a heater block or hot plate, ensure that air flow does not affect the bake temperature.

11.6 *Functional Test*

11.6.1 *Epoxy Die Bonding* — Processes and test procedures shall be agreed upon between user and supplier.

11.6.2 *Gold Wire Bonding* — Processes and test procedures shall be agreed upon between user and supplier.

11.6.3 *Solderability* — Processes and test procedures shall be agreed upon between user and supplier.

## 12 Related Documents

12.1 *SEMI Specifications*

SEMI G8 — Test Method for Gold Plating Quality

SEMI G21 — Specification Plating Integrated Circuit Leadframes

12.2 *JIS Specifications*[2]

JIS H8501 — Methods of Thickness Test for Metallic Coatings

JIS H8621 — Electroplated Coatings of Silver for Engineering Purpose

JIS Z8722 — Methods of Measurement for Color of Reflecting or Transmitting Objects

JIS Z8741 — Method of Measurement for Specular Glossiness



2 Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014 Website: www.jsa.or.jp

forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copyrighted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their responsibility.

# SEMI G63-95 (Reapproved 0302)
# TEST METHOD FOR MEASUREMENT OF DIE SHEAR STRENGTH

This test method was technically approved by the Global Assembly and Packaging Committee and is the direct responsibility of the Japanese Assembly and Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on November 26, 2001. Initially available at www.semi.org December 2001; to be published March 2002. Originally published in 1995.

## 1 Purpose

1.1 The purpose of this test method is to determine procedures for die shear strength testing.

## 2 Scope

2.1 This test method shall be used for the measurement of the die shear strength when die attach paste is used to bond a die to a leadframe bond pad.

2.2 This test method shall be used for quality control and development at die attach paste suppliers and for incoming inspection and selection of the die attach paste at die attach paste users.

2.3 This test method can be applicable to die attach material besides paste material and may be used to evaluate leadframe bond pad quality.

2.4 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability or regulatory limitations prior to use.

## 3 Referenced Standards

3.1 *Military Specification*[1]

MIL-STD-883 — Method 2019, Die Shear Strength

## 4 Terminology

4.1 *die* — Semiconductor device or an imitation.

4.2 *die attach* — Bond die and substrate such as leadframe pad.

4.3 *die contact tool* — Tool for applying load to the die for shearing.

4.4 *dispense* — Deal out paste.

4.5 *fillet* — Height and shape of die attach paste in contact with or surrounding the die kerf.

4.6 *shear* — Have forced completely in X-Y direction.

## 5 Summary of Method

5.1 This method is based on measuring the shear strength between die and leadframe pad bonded by die attach paste using die shear tester.

## 6 Equipment

6.1 *Die Shear Tester*

6.1.1 ± 5% accuracy of full scale

6.1.2 Die contact tool can be in contact with die edge from end-to-end.

6.2 *Hot Plate* — optional

6.3 *Microscope* — optional

## 7 Material

7.1 *Silicon Die* — 2 mm × 2 mm × 0.3 to 0.5 mm

7.2 *Leadframe*

7.3 *Die Attach Paste*

## 8 Test Specimen

8.1 Dispense die attach paste by dispensing, stamping, or screen printing.

8.2 Bond die and leadframe pad.

8.3 Cure the paste per recommendation and allow to cool to ambient.

NOTE 1: Height of fillet shall be less than half of the thickness of the die.

NOTE 2: Thickness of die attach paste shall be within the range of 5 to 30 μ m before or after cure.

NOTE 3: Assembled parts shall not be exposed to a curing temperature higher than the peak recommended temperature for more than 30 seconds.

## 9 Sampling Plan

9.1 Number of specimens tested shall be 5 or more.

1 Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA. Telephone: 215.697.3321

## 10 Procedure

10.1 Set a test specimen on the die shear tester.

10.2 Confirm that the die contact tool contacts the die side in half of the area or more and that the die contact tool does not touch the fillet.

10.3 Shear the specimen with the tester.

10.4 Record the strength.

10.5 Observe failed parts and classify in the following modes:

Mode 1: Die breakage

Mode 2: Adhesive failure between die and die attach paste

Mode 3: Cohesive failure

Mode 4: Adhesive failure between die attach paste and substrate

Mode 5: Substrate deformation

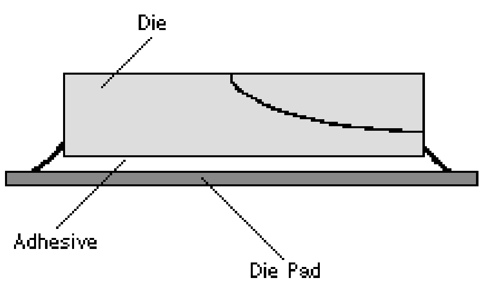



**Figure 1**
**Mode 1 — Break-In Die**

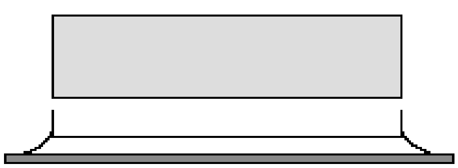


**Figure 2**
**Mode 2 — Interface Failure: Die-to-Adhesives**

**Figure 3**
**Mode 3 — Break-In Adhesives**

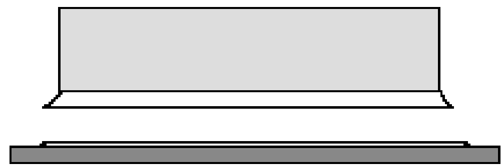


**Figure 4**
**Mode 4 — Interface Failure:Adhesives-to-Die Pad**

NOTE 4: In the case of hot die shear strength testing, the hot temperature shall be agreed between user and supplier.

Procedure is as follows:

1. Set and raise the hot plate temperature
2. Confirm that actual temperature is within the range of ± 10° C at the set temperature.
3. Put a specimen on the hot plate and follow Section 10.3 after 10 to 20 seconds.

## 11 Calculation of Result

11.1 Average strength and standard deviation shall be calculated if required.

## 12 Report

12.1 The following information shall be reported in the attached form:

12.1.1 Type of die attach paste

12.1.2 Type of leadframe and leadframe plating

12.1.3 Thickness of die and surface condition (attached side) of the die.

12.1.4 Cure schedule and atmosphere (air or nitrogen)

12.1.5 Information about die attach paste thickness, dispense weight, or bond line thickness before and after cure.

12.1.6 Die shear speed

12.1.7 Die shear strength in N (kgf)/die unit (complete data or an average)

12.1.7.1 Standard deviation when number of specimens tested is adequate.

12.1.8 Temperature in hot die shear testing.

| | |
|---|---|
| Die Attach Paste (Material) | |
| Leadframe Type | |
| Leadframe Plating | |
| Die Thickness | |
| Die Surface Condition | |
| Cure Schedule | Time ____________ Temp. ___________ in air or $N_2$ |
| Thickness or Dispense Weight | |
| Shear Speed | |

| | *RT* | | *Hot Temperature* | |
|---|---|---|---|---|
| | *Strength (N (kgf)/chip)* | *Failure Mode* | *Strength (N (kgf)/chip)* | *Failure Mode* |
| Sample 1 | | | | |
| Sample 2 | | | | |
| Sample 3 | | | | |
| Sample 4 | | | | |
| Sample 5 | | | | |
| Sample 6 | | | | |
| Sample 7 | | | | |
| Sample 8 | | | | |
| Sample 9 | | | | |
| Sample 10 | | | | |
| Sample 11 | | | | |
| Sample 12 | | | | |
| Average | | | | |
| Standard Deviation | | | | |

# APPENDIX 1

NOTE: The material in this appendix is an official part of SEMI G63 and was approved by full letter ballot procedures in 1995.

## A1-1 Purpose

The purpose of this appendix is to indicate that speed and height of the die contact tool affect die shear strength results.

## A1-2 Test Results

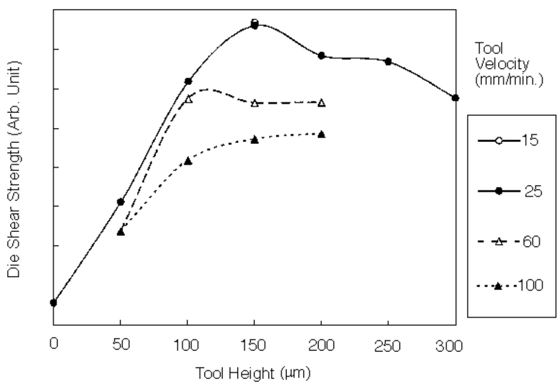



**Figure A1-1**
**Tool Velocity Test Results**

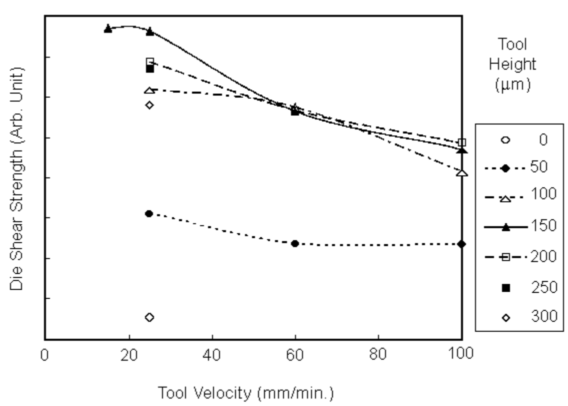



**Figure A1-2**
**Tool Height Test Results**

A1-2.1 *Summary*

A1-2.1.1 *Shear Speed*

a. Some adhesive might yield variable results due to the relationship of the shear speed and failure speed.

b. Some equipment with high shear speed could yield low strength due to poor sensitivity at the peak of the load.

A1-2.1.2 *Height of the Die Contact Tool*

a. In case of low height, fillet level might affect the strength.

b. In case of high height, a variable result might be obtained since the tool pulls the die and it tears the adhesive.

# SEMI G64-96 (Reapproved 1104)
# SPECIFICATION FOR FULL-PLATED INTEGRATED CIRCUIT LEADFRAMES (Au, Ag, Cu, Ni, Pd/Ni, Pd)

This specification was technically reapproved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on July 23, 2004. Initially available at www.semi.org September 2004; to be published November 2004. Originally published in 1996.

## 1 Purpose

1.1 This specification is intended as a guideline for evaluating plating layer characteristics required by users of full-plated leadframes for plastic semiconductor packages.

1.2 *Background* — Full-plated leadframes have received attention in recent years as a possible solution to challenges and restrictions resulting from the effects of Pb on the environment, package reliability improvement due to the P.P.F. process, lead coplanarity on fine-pitched leadframes, and lead bridges with solder plating.

## 2 Scope

2.1 The specification and test procedures detailed in this document apply to full-plated leadframes.

2.2 *Units* — SI units are used in this document.

**NOTICE:** This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

## 3 Referenced Standards

3.1 *SEMI Standards*

SEMI G4 — Specification for Integrated Circuit Leadframe Materials Used in the Production of Stamped Leadframes

SEMI G18 — Specification Integrated Circuit Leadframe Material Used in the Production of Etched Leadframes

SEMI G21 — Specification for Plating Integrated Circuit Leadframes

SEMI G52 — Standard Test Method for Measurement of Ionic Contamination on Semiconductor Leadframes (Proposed)

SEMI G55 — Test Method for Measurement of Silver Plating Brightness

SEMI G56 — Test Method forMeasurement of Silver Plating Thickness

3.2 *ISO Standards*[1]

ISO-3497 — Metallic Coating Measurement of Coating Thicknesses, X-Ray Spectrometer Method

ISO-9227 — Corrosion Tests in Artifical Atmospheres - Salt Spray Tests

3.3 *JIS Standard*[2]

JIS-C-0053 — Solderability Testing by the Wetting Balance Method

3.4 *Military and Federal Standards*[3]

MIL-C-14550 — Copper Plating-Electrodeposited

MIL-F-14256 — Flux, Soldering, Liquid, Paste Flux, Solder Paste, and Solder Paste Flux

MIL-G-45204 — Gold Plating-Electrodeposited

MIL-STD-883D — Method 2003.7, Solderability

QQ-N-290 — Nickel Plating-Electrodeposited

QQ-S-365 — General Requirements for Electrodeposited Silver Plating

QQ-S-571 — Solder Composition

**NOTICE:** Unless otherwise indicated, all documents cited shall be the latest published versions.

## 4 Terminology

4.1 *Definitions*

4.1.1 *finish plating* — final plating layer whose electrodeposits fulfill the main purpose of the required characteristic.

1 International Organization for Standardization, ISO Central Secretariat, 1, rue de Varembé, Case postale 56, CH-1211 Geneva 20, Switzerland. Telephone: 41.22.749.01.11; Fax: 41.22.733.34.30, Website: www.iso.ch

2 Japanese Industrial Standards, Available through the Japanese Standards Association, 1-24, Akasaka 4-Chome, Minato-ku, Tokyo 107-8440, Japan. Telephone: 81.3.3583.8005; Fax: 81.3.3586.2014, Website: www.jsa.or.jp

3 United States Military Standards, Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA. Telephone: 215.697.3321

4.1.2 *solderability* — an index of the wettability and coverage with solder of lead surface.

4.1.3 *underplating* — plating layers that complete the required characteristics of the final plating layer and lies between the base material and final plating layer.

## 5 Ordering Information

5.1 *Priority*

5.1.1 To avoid confusion, the order of precedence when ordering leadframes shall be as follows:

1. Purchase Order (agreed between user and supplier)
2. This Specification
3. Referenced Documents

## 6 Materials

6.1 *Base Material* — Cu alloys or Fe/Ni alloys.

6.2 *Plating Material* — Underplating and Finish plating are shown in Table 1.

**Table 1 Table 1 Underplating and Finish Plating**

| *Finish Plating* | *Underplating* | *Base Material* | |
|---|---|---|---|
| | | *Cu-Alloys* | *Fe, Ni-Alloys* |
| Au (MIL-G-45204) | - | N/A | X |
| | Ni | X | X |
| Ag (QQS-365) | - | X | N/A |
| | Cu | X | X |
| Cu (MIL-C-14550) | - | X | X |
| | Ni | X | X |
| Ni (QQN-290) | - | X | X |
| | Cu | X | X |
| Pd/Ni-Alloy | - | X | X |
| | Ni | X | X |
| | Cu | X | X |
| Pd | - | X | X |
| | Ni | X | X |
| | Cu | X | X |
| | Pd/Ni-Alloy | X | X |

## 7 Plating Specification

7.1 *Plating Thickness* — For full-plated leadframes, the designed thickness including under plating is restricted as follows to limit the effects of thickness variation on coplanarity and outer lead width.

- Designed thickness including under plating-1 / Ag-plating: 5 µm MAX
- Designed thickness including under plating-2 / Au, Cu, Ni, Pd/Ni-Alloy, Pd plating: 2 µm MAX

7.2 *Visual Inspection* — Rejectable conditions are as follows:

1. Any bare spots, or missing plating in critical area as defined the coined areas or minimum flat wire bond area in the appropriate leadframe specification.
2. Any peeling or blistered plating.
3. Any nodules in critical area as defined the coined areas or minimum flat wire bond area in the appropriate leadframe specification.

   NOTE 1: Nodules not exceeding 0.0381 mm in a surface dimension and 0.0127 mm in height, in non-critical areas are allowed providing there are no more than one per internal lead finger or six (6) per leadframe.

4. Any pits which exceed 0.008 mm in depth or 0.0127 mm in a surface dimension in critical areas or 0.0254 mm in depth or 0.051 mm in a surface dimension in non-critical areas.
5. Any scratches or scrapes in the metallization plating which expose underplating or base material.
6. Any scratches or scrapes in critical area which cause a build up of material in excess of 0.0127 mm in height.
7. Any foreign material, contamination, or tarnish.
8. Non-uniformity or rough-plated surface.

7.3 *Visual Inspection after Baking* — The test procedure is described in Section 9.3. Visual inspection after baking shall be performed according to the procedure in Section 9.2.1.

7.4 *Corrosion Resistance (not applicable to Cu plating)* — In the test result, allowable corrosion specification shall be agreed upon between user and supplier.

7.5 *Surface Ion Contamination* — Allowable ion species and ion concentration shall be agreed upon between user and supplier.

7.6 *Adhesion* — If there is any plating film on the test tape, the component shall be rejected. Adhesive test should be performed according to the procedure in Section 9.6.

7.7 *Functional Tests*

7.7.1 *Die Attach* — Agreed upon between user and supplier.

7.7.2 *Wire Bond* — Agreed upon between user and supplier.

7.7.3 *Solderability* — The criteria for acceptable solderability are as follows:

1. The dipped portion of the samples is at least 95% covered by a continuous solder coating.
2. Pinholes, voids, porosity, non-wetting, or dewetting do not exceed 5% of total area.

NOTE 2: Solderability criteria for Ni and Cu plating are established by the user and supplier and are excluded here.

## 8 Equipment

8.1 Fluorescent X-ray spectremeter

8.2 Binocular-microscope, 10–30× magnification

8.3 Neutral salt spray test equipment

8.4 Ion chromatography (Anion, Cation)

8.5 Hot plate or Heater block

8.6 Solder pot

8.7 Meniscograph

## 9 Sampling

9.1 Sampling plan shall be agreed upon between user and supplier.

## 10 Test Methods

10.1 *Thickness* — Plating thickness shall be measured by fluorescent X-ray spectrometer.

10.2 *Visual Inspection*

10.2.1 *Magnification* — Unless otherwise specified, visually inspect the plating surface under a microscope at 10× magnification. 30× magnification shall be used for confirmation.

10.3 *Baking Test*

10.3.1 *Baking Conditions* — Samples are heated in air on hot plates or heater block.

**Table 2**

| *Finish Plating/Base Material* | *Cu-Alloys* | *Fe/Ni-Alloys* |
|---|---|---|
| Au* | 450°C × 3 min. | 450°C × 3 min. |
| Ag | 300°C × 3 min. | 400°C × 3 min. |
| Cu** | 200°C × 1 hour | 200°C × 1 hour |
| Ni** | 400°C × 3 min. | 400°C × 3 min. |
| Ni/Pd Alloy | 200°C × 1 min. | 200°C × 1 min. |
| Pd | 300°C × 1 min. | 300°C × 1 min. |

* May be changed by agreement between user and supplier to 400°C × 1 min or 450°C × 2 min or less, to account for changes in plating thickness, base material, or other plating parameters.

** Surface oxidation and discoloration detected by visual inspection are acceptable. Furthermore, parameter of solderbility evaluation for flux, dipping method, etc. are to be determined by agreement between user and supplier.

10.3.2 Visual inspection after baking shall be performed according to the procedure in Section 9.2.1.

10.4 *Corrosion Test* — Atomize the test sample in a test container using a 5% neutral sodium chloride solution of 8.8–7.2pH at 35 ± 1°C for 24 hours. This test follows ISO-9227.

10.5 *Surface Ion Contamination* — The measurement follows SEMI G52.

10.6 *Adhesion Test* — Place the strip of tape (SCOTCH[a] #540, #610, #810, or equivalent) across the plated area. Press firmly with fingertips or other smooth object. Peel the tape quickly off the plated surface. The plating surface may be scored before the tape test in accordance with the joint agreement between user and supplier.

10.7 *Functional Tests*

10.7.1 *Die Attach* — Agreed upon between user and supplier.

10.7.2 *Wire Bond* — Agreed upon between user and supplier.

10.7.3 *Solderability* — The procedure for accelated aging test shall be agreed upon between user and supplier (see Appendix 1).

# APPENDIX 1
# SOLDERABILITY TEST

**NOTICE**: The material in this appendix is an official part of SEMI G64 and was approved by full letter ballot procedures.

## A1-1 Accelerated Environment Simulation

A1-1.1 Determination, due to the environment, may be simulated by exposure to a hot plate that reproduces the heat characteristics of assembly (a), and by steam aging to simulate the storage environment. The following are methods for accelerated environment simulations (b):

a. Place samples in air on a hot plate or a heat block. Temperature and duration are detailed in Section 9.3, and represent the heat characteristics of assembly.

b. Steam aging test is based on MIL-STD-883D, Method 2003.7, and simulates environmental conditions.

## A1-2 Soldering Parameter

A1-1.2 Baked test specimens shall be dipped into flux conforming to MIL-P-14256, type-R, for 5 to 10 seconds, and then dipped in a solder bath conforming to QQ-S-571 for 10 ± 1 seconds at a solder pot temperature of 230 ± 5°C.

## A1-3 Evaluation of Solderability

A1-3.1 *Wetting Area* — After cleaning solder dipped specimen with alcohol to remove flux, visually inspect under a microscope at 10× magnification. Solder must cover 95% or more of surface area, based on MIL-STD-883D, Method 2003.7.

A1-3.2 *Wetting Time (zero-cross-time)* — Solder that conforms to conditions below is evaluated according to JIS-C-0053, or may be evaluated by a method determined by user and supplier for certain leadframe shapes.

1. Temperature: 230 ± 5°C
2. Dipping speed: 2 mm/second
3. Dipping depth: 2 mm
4. Flux: Rosin flux (MIL-F-14256, type-R)
5. Solder composition: 63 Sn / 37 Pb (QQ-S-571)

# SEMI G65-96 (Reapproved 1104)
# TEST METHOD FOR EVALUATION OF LEADFRAME MATERIALS USED FOR L-LEADED (GULL WING TYPE) PACKAGES

This test method was technically approved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on July 23, 2004. Initially available at www.semi.org September 2004; to be published November 2004. Originally published in 1996.

## 1 Purpose

1.1 This test method describes an evaluation method for bending characteristics of leadframe materials used for L-leaded packages.

NOTE 1: The lead fatigue test described in MIL-STD-883/2004 is not suitable for evaluating the bending characteristics of fine pitch leadframes or leadframes used for L-leaded packages because the method is based on reforming the leads.

## 2 Scope

2.1 This test method may be applied to leadframes for L-leaded packages such as QFP, SOP, TSOP, etc.

2.2 This test method may also be applied to any leadframe materials with thickness ≤ 0.15 mm.

2.3 The test method may be used in trim and form tool suppliers, leadframe material suppliers, leadframe manufacturers, and package engineers.

**NOTICE:** This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

## 3 Referenced Standards

3.1 *Military Standard*[1]

MIL-STD-983 — Method 2004, Lead Integrity

**NOTICE:** Unless otherwise indicated, all documents cited shall be the latest published versions.

## 4 Terminology

4.1 *Definitions*

4.1.1 *crack (of leadframe)* — Micro cleavage or fracture on surface of outside of lead which is caused by bending (see Figure 1).

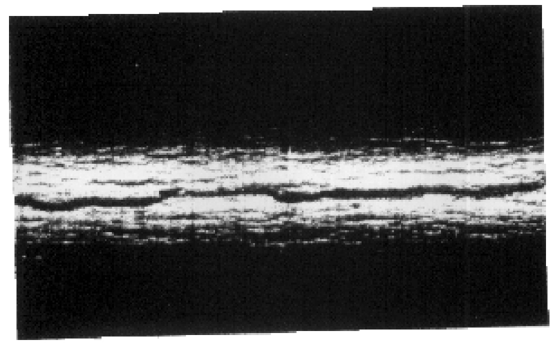


**Figure 1**
**Crack**

4.1.2 *orange peel (of leadframe)* — Micro roughness on surface of outside of lead caused by bending (see Figure 2).

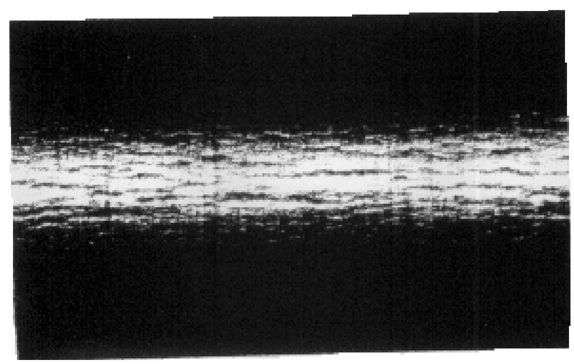


**Figure 2**
**Orange Peel**

4.1.3 *spring back* — Difference between designed angle of forming tool and actual lead form angle.

NOTE 2: In this method, the angle of forming tool is 90°. The value is defined by: Actual lead bend angle 90°.

1 United States Military Standards, Available through the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120-5099, USA. Telephone: 215.697.3321

## 5 Summary of Method

5.1 The leadframe samples (etched using a standard mask agreed between user and supplier) will be formed using a "W" forming tool. The resulting form angle is to be measured and surface characteristics such as cracking and orange peel are to be visible for compliance to the agreed upon specification.

## 6 Interference

6.1 If the forming tool does not meet the specification, lead movement during forming may result in poor repeatability.

## 7 Significance

7.1 Devices manufactured with leadframes of different spring back characteristics may cause board assembly problems, due to lead positional differences.

7.2 Crack in the leadframe may cause poor contact reliability with board.

## 8 Equipment

8.1 *Tensile Tester* — With minimum 9800N force and 1% accuracy.

8.2 *"W" Forming Tool* — With R = 0, 0.1 and 0.2 and form angle of 90°. The dimension and configuration are shown in Figures 3–7.

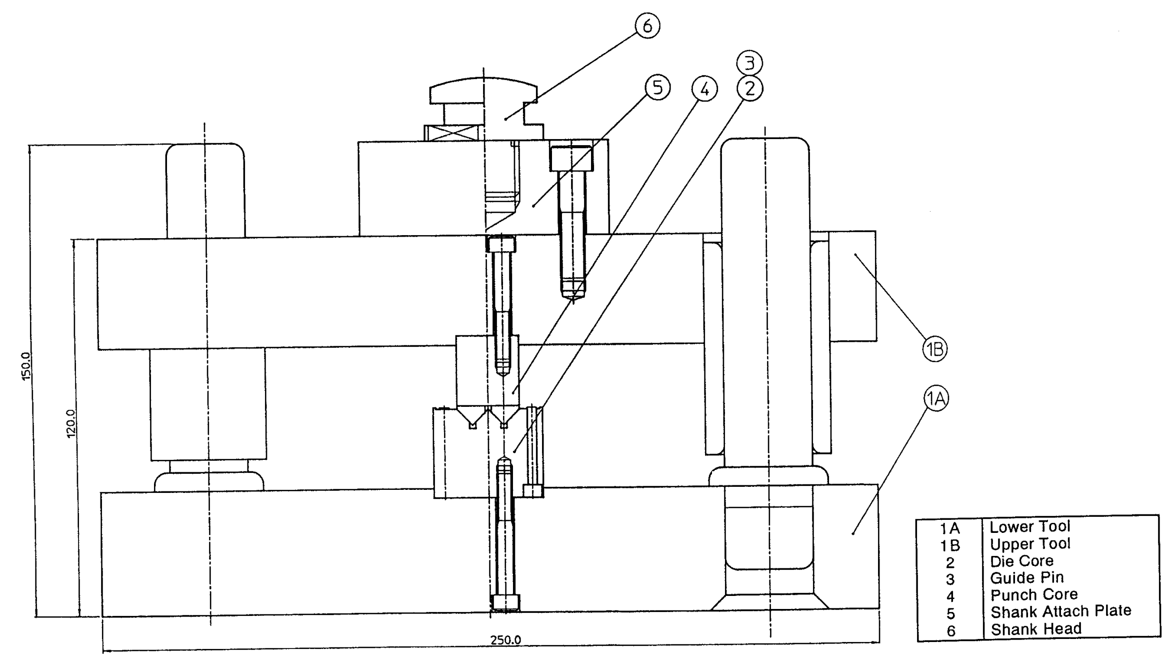



**Figure 3**
**W-Bending Test Tool**

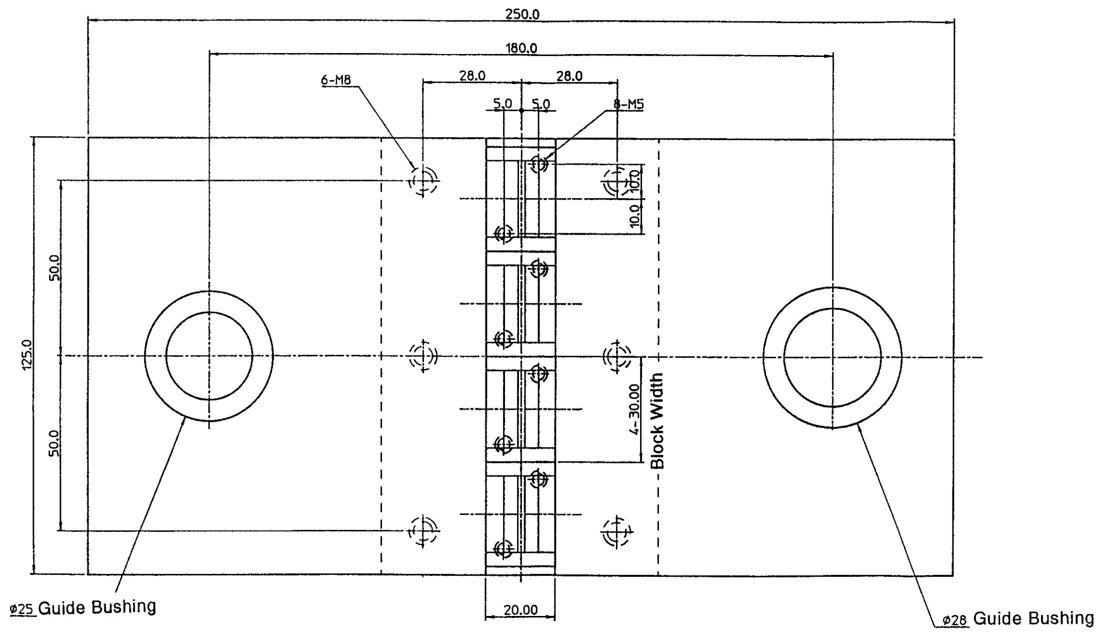



**Figure 4**
**Upper Tool Detail**

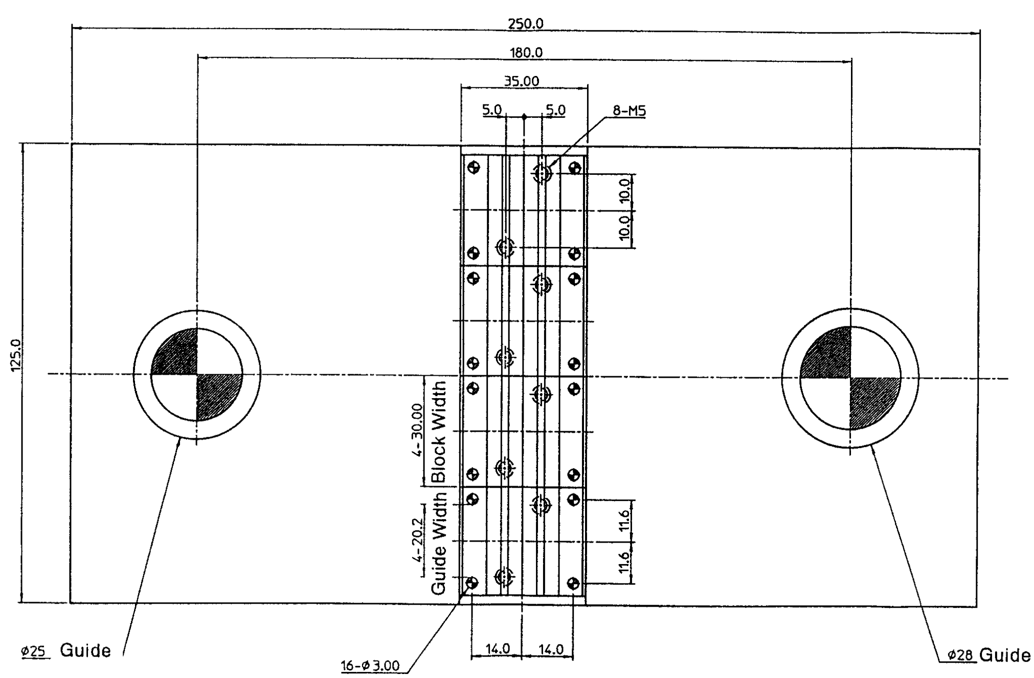



**Figure 5**
**Lower Tool Detail**

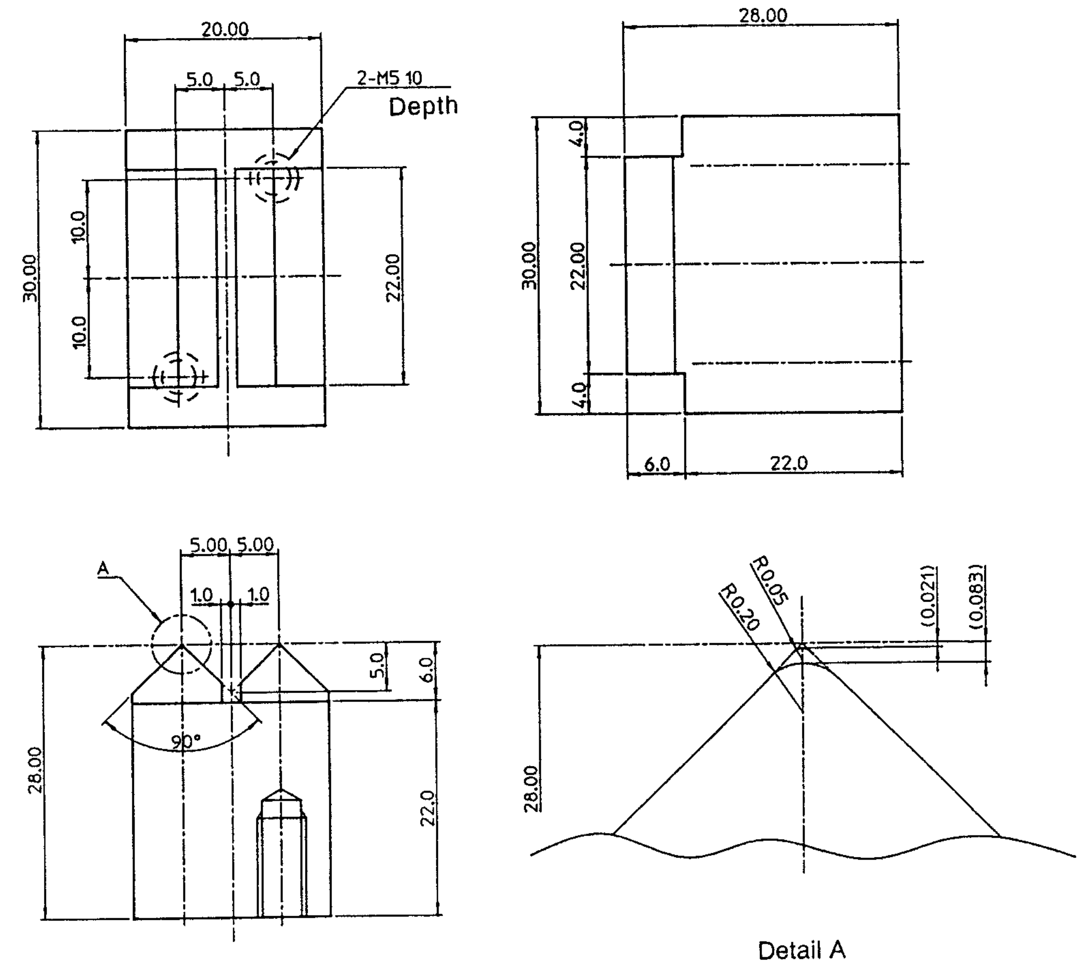



**Figure 6**
**Punch Core Detail**

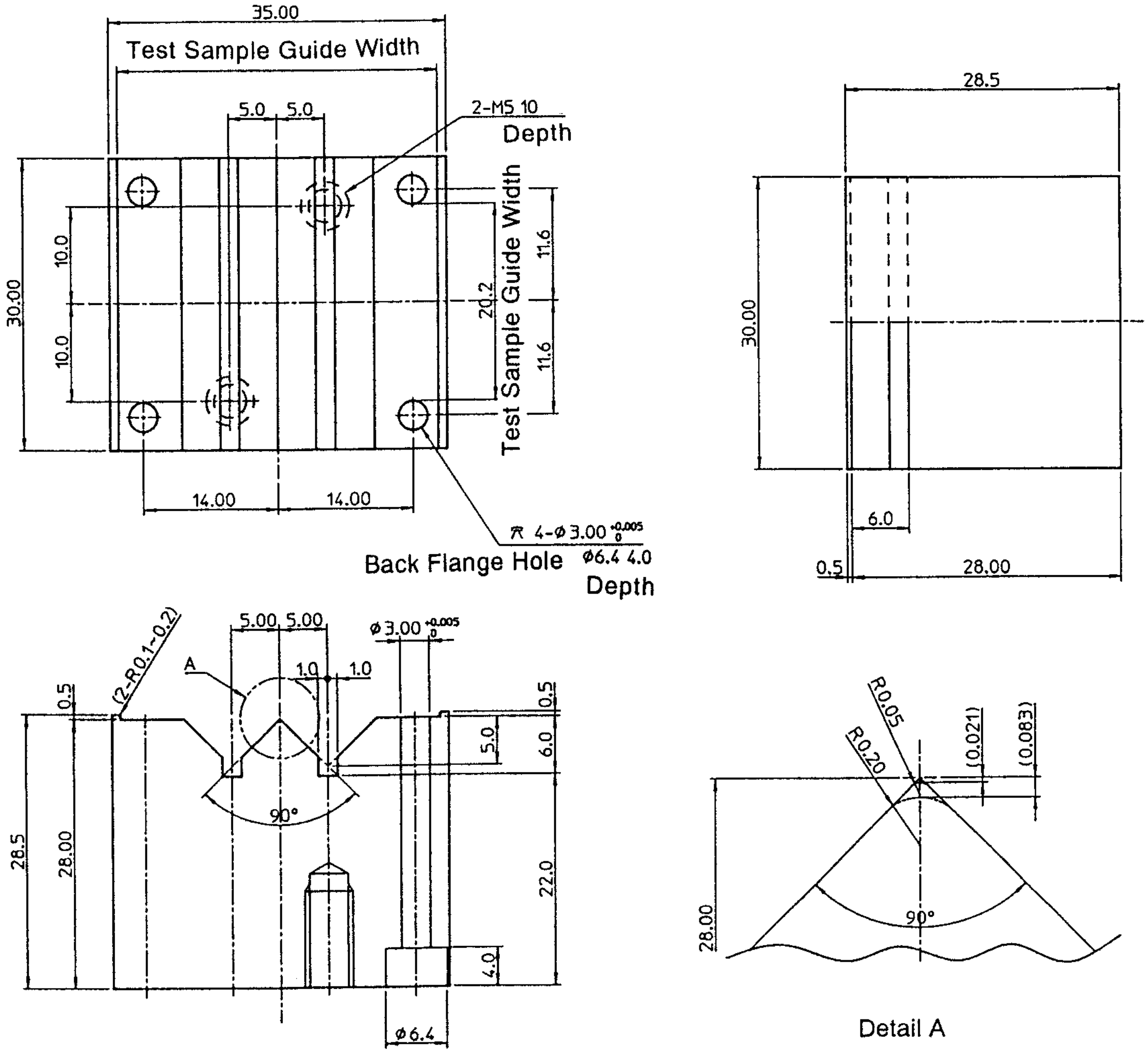



**Figure 7**
**Die Core Detail**

8.3 *Micrometer*

8.4 *Microscope* — 75× used to inspect lead surface characteristics.

8.5 *Protractor* — 10× and accuracy 0.1° used to measure the leadform spring back.

8.6 *Projector* — 10×.

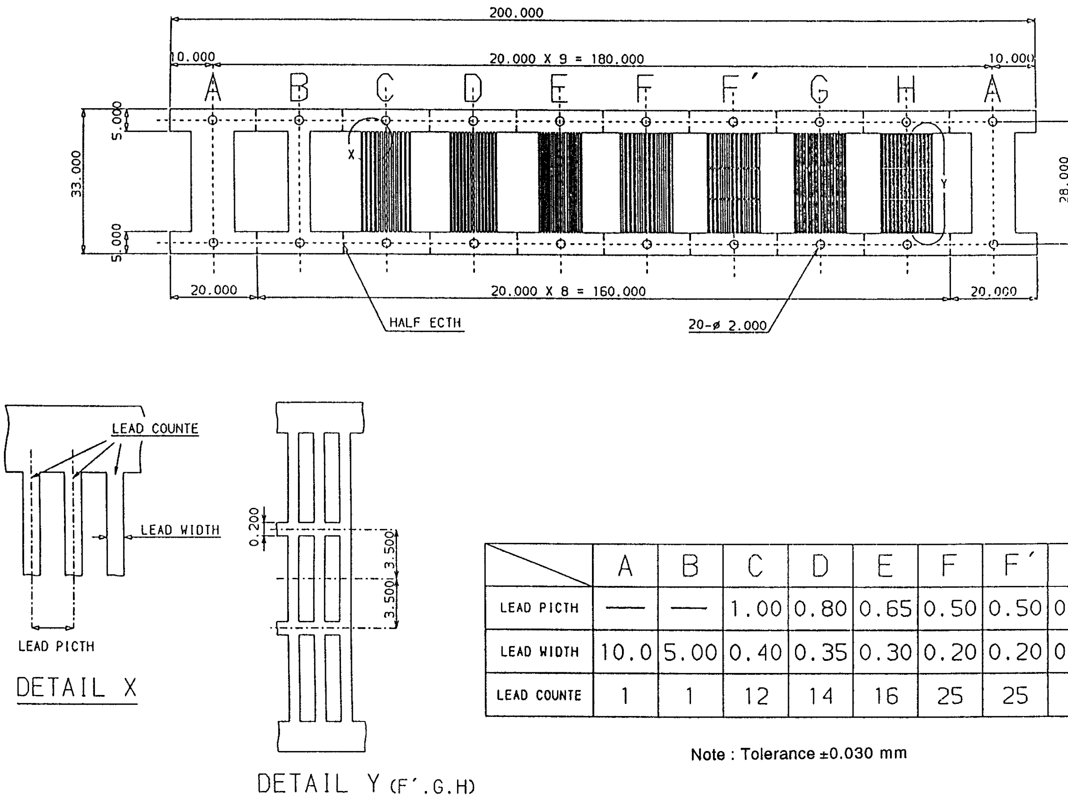
## 9 Sampling Plan

9.1 The sampling plan shall be agreed between user and supplier. It is suggested that a minimum of five (5) samples (2 leads per sample) of 0.3 mm width on 0.65 mm pitch, be used for these tests.

NOTE 3: If the leadframe is four-sided, take samples from both orthogonal directions.

## 10 Sample Preparation

10.1 The samples are prepared by etching a leadframe pattern into a blank piece of the leadframe material using a standard mask. An example of the recommended configuration is shown in Figure 8.




| | A | B | C | D | E | F | F′ | G | H |
|---|---|---|---|---|---|---|---|---|---|
| LEAD PICTH | — | — | 1.00 | 0.80 | 0.65 | 0.50 | 0.50 | 0.40 | 0.30 |
| LEAD WIDTH | 10.0 | 5.00 | 0.40 | 0.35 | 0.30 | 0.20 | 0.20 | 0.16 | 0.12 |
| LEAD COUNTE | 1 | 1 | 12 | 14 | 16 | 25 | 25 | 31 | 42 |

Note : Tolerance ±0.030 mm

**Figure 8**
**Standard Sample Configuration**

10.2 Measure the sample thickness at three (3) points on the siderail using micrometer.

## 11 Setup and Procedure

11.1 *Setup*

11.1.1 Warm up and calibrate the tensile tester according to the operation manual.

11.1.2 Set the “W” forming tool in the tensile tester.

11.1.3 Set the tensile tester in the push mode and adjust the force to 9800N.

11.2 *Procedure*

11.2.1 Place the sample on the lower section of the “W” forming tool.

11.2.2 Lower the upper section of the “W” forming tool at the speed of 1 to 5 mm/min.

11.2.3 Raise up the upper section of the “W” forming tool and remove the sample carefully.

11.2.4 Repeat the test for the other samples.

11.3 *Measurement*

11.3.1 Remove the leads from the bent sample by cutting at the cutting position.

NOTE 4: Perform this operation carefully to avoid reforming the leads.

11.3.2 Select two (2) leads from one sample.

11.3.3 Observe the outside surface of the lead and take a photograph with a microscope set at 75× magnification.

11.3.4 Set the lead sample in a projector.

11.3.5 Project the picture of the sample on the screen.

11.3.6 Adjust the protractor to the picture and read the form angle.

## 12 Calculation

12.1 Calculate the spring back value as follows:

12.1.1 Spring back = actual angle of sample - designed form angle

12.2 Calculate the average spring back value.

12.3 Round the result to one significant figure.

## 13 Report

13.1 The report shall contain the following information:

13.1.1 Leadframe material name, lot number, and vendor

13.1.2 Average thickness (per Section 10.2)

13.1.3 Photograph taken using 75× magnification (per 11.3.3)

13.1.4 List of observations (per Section 11.3.3)

NOTE 5: Classify observation results as crack, orange peel, and good according to their definition in Section 4. If required, further classification should be agreed between customer and vendor.

13.1.5 Spring Back Value (per Sections 11.3.4 to 11.3.6) — Average, minimum, maximum

13.1.6 Rejection — The limit shall be agreed between user and supplier.

## 14 Related Documents

14.1 *SEMI Specification*

SEMI G4 — Specification for Integrated Circuit Leadframe Materials Used in the Production of Stamped Leadframes

14.2 *JIS Specifications*

JIS-Z-2248 — Method of Bend Test for Metallic Materials

JIS-H-3130 — Copper Beryllium Alloy, Phosphor Bronze and Nickel Silver Sheets, Plates, and Strips for Springs

14.3 *CES Specification*

M0002-6 — Test Method of W Bend for Metallic Materials

SEMI G66-96 (Reapproved 1104)
# TEST METHOD FOR THE MEASUREMENT OF WATER ABSORPTION CHARACTERISTICS FOR SEMICONDUCTOR PLASTIC MOLDING COMPOUNDS

This test method was technically approved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on July 23, 2004. Initially available at www.semi.org September 2004; to be published November 2004. Originally published in 1996.

## 1 Purpose

1.1 This method describes a procedure for measuring the water absorption rate for plastic molding compounds and provides a method to calculate the diffusion and solubility coefficients, which are required to simulate the water absorption characteristics.

## 2 Scope

2.1 This method may be applied to all semiconductor plastic molding compounds.

2.2 This method may be used to characterize molding compounds in development.

2.3 Packaging engineers may simulate the water absorption characteristics and their significance in relation to package cracks at soldering by using calculated diffusion and solubility coefficients.

**NOTICE:** This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

## 3 Referenced Standards

3.1 None.

## 4 Terminology

4.1 *Definitions*

4.1.1 *diffusion coefficient, D* — the diffusion rate of water into a molding compound (see Appendix 1 and Figure 1).

4.1.2 *solubility coefficients, S* — ratio of saturated moisture concentration in molding compounds to partial pressure of moisture in environment (see Appendix 1 and Figure 1).

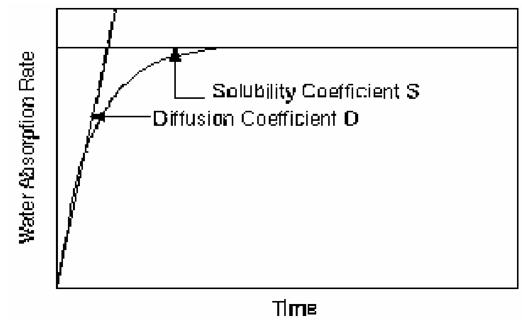



**Figure 1**
**Concept of Diffusion and Solubility Coefficients**

## 5 Summary of Method

5.1 This method is based on the measurement of the increase in weight, due to water absorption, after exposing the molding compound to a high-temperature, high-humidity environment.

## 6 Equipment

6.1 *Balance* — An analytical balance capable of reading 0.0001g.

6.2 *High-Temperature Chamber* — Capable of maintaining a uniform temperature of 125 ± 3°C.

6.3 *Temperature/Humidity Chamber* — Capable of maintaining a uniform temperature of 85 ± 2°C and 85 ± 5% relative humidity.

6.4 *Desiccator (1)* — To hold specimens during cool-down from high-temperature conditioning.

6.5 *Desiccator (2)* — This desiccator, with water in the bottom rather than drying compound, is to hold the specimens after exposure to heat and humidity.

6.6 Mold for specimen preparation.

## 7 Reagents and Materials

7.1 *Deionized Water* — Resistivity ≥ 15M ohm-cm at 25°C

## 8 Sampling Plan

8.1 At least three samples shall be chosen for each molding type for each test.

## 9 Test Specimens

9.1 Test specimens are required as follows:

9.1.1 Specimens for diffusion area.

9.1.1.1 *Diameter* — 50 ± 1 mm

9.1.1.2 *Thickness* — 3 ± 0.2 mm

9.1.2 Specimens for saturated area.

9.1.2.1 *Diameter* — 50 ± 1 mm

9.1.2.2 *Thickness* — 1 ± 0.2 mm

## 10 Equipment Set-Up

10.1 Refer to manufacturer's operation manuals.

## 11 Procedure

11.1 *Specimen Preparation*

11.1.1 Prepare the specimens by molding samples using the specimen mold and conditions recommended by the molding compound manufacturer.

11.1.2 Post-mold cure the specimens to recommended conditions using the high-temperature chamber.

11.2 *Specimen Conditioning*

11.2.1 Dry the specimens at 125°C in the high-temperature chamber for 24 hours minimum.

NOTE 1: If the samples are already dry (e.g., samples directly from post-mold cure), additional conditioning is not required.

11.2.2 Place the specimens in the desiccator (1) and allow to cool to room temperature.

11.2.3 Weigh the specimens to the nearest 0.0001g.

11.3 Water Absorption Exposure and Reconditioning

11.3.1 *Diffusion Area*

11.3.1.1 Place the conditioned specimens (3 mm thickness) in the high-temperature/humidity chamber set at 85°C and 85% relative humidity for 24 ± 1 hours.

NOTE 2: The specimens should be placed to avoid any contact with each other and with the walls of the chamber, e.g. to use a holder or to place on a wire net.

11.3.1.2 Remove the specimens from the chamber and wipe off any excess water from the surfaces with a clean cloth or absorbant paper.

11.3.1.3 Place the specimens in desiccator (2) and allow to cool to room temperature.

NOTE 3: The specimens should be placed to avoid any contact with each other and with the walls of the chamber (e.g., to use a holder or to place on a wire net).

11.3.1.4 Re-weigh the specimens to the nearest 0.0001 g.

11.3.2 *Saturated Area*

11.3.2.1 Place the conditioned specimens (1 mm thickness) in the high-temperature/humidity chamber set at 85°C and 85% relative humidity for 168 ± 4 hours.

NOTE 4: The specimens should be placed to avoid any contact with each other and with the walls of the chamber (e.g., to use a holder or to place on a wire net).

11.3.2.2 Remove the specimens from the chamber and wipe off any excess water from the surfaces with a clean cloth or absorbant paper.

11.3.2.3 Place the specimens in desiccator (2) and allow to cool to room temperature.

NOTE 5: The specimens should be placed to avoid any contact with each other and with the walls of the chamber, e.g. to use a holder or to place on a wire net.

11.3.2.4 Re-weigh the specimens to the nearest 0.0001g.

## 12 Calculations

12.1 *Water Absorption Rate* — The rate is calculated as follows:

12.1.1 Water absorption rate (wt%) = ( (M2 M1) /M1) × 100 (1)

Where:

M1 is the initial conditioned weight, and

M2 is the reconditioned weight after exposure to

temperature/humidity

12.2 *Diffusion and Solubility Coefficients*

12.2.1 There are various methods to calculate diffusion and solubility coefficients. See Appendix 1 for one of these methods.

## 13 Report

13.1 The following information shall be reported:

13.1.1 Manufacturer and identification of molding compound

13.1.2 Specimen sizes

13.1.3 Test conditions

13.1.4 Water absorption rate

13.1.5 Date of test

## 14 Related Documents

14.1 *ASTM Specification*[1]

ASTM D 570 — Standard Test Method for Water Absorption of Plastic

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, Pennsylvania 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555, Website: www.astm.org

# APPENDIX 1
# APPLICATION NOTES — METHOD OF CALCULATION FOR DIFFUSION AND SOLUBILITY COEFFICIENT

**NOTICE**: The material in this appendix is an official part of SEMI G66 and was approved by full letter ballot procedures.

## A1-1 Purpose

A1-1.1 This application note describes a method for calculating diffusion and solubility coefficients.

## A1-2 Solubility Coefficient, S

A1-1.2 The solubility coefficient is given from the data of saturated area as follows:

A1-1.2.1 $S = M_s \times d / P \times 1000$ (2)

Where:

S = Solubility coefficient ((mg/cm$^3$ / (kg/mm$^2$))

M = Saturated moisture absorption rate (wt%) (data from saturated area test)

D = Density of specimen (g/cm$^3$)

P = Partial pressure of moisture in environment (Pa) (value at 85 C in this test)

## A1-3 Diffusion Coefficient, D

A1-1.3 The moisture absorption rate in resin exposed for relatively short term is calculated using the following equation based on Fick's formula:

$M_t / M_s = 4\times\{ (D\times t) / (1\times\pi) \}^{1/2}$ (3)

Then:

$D = 1^2\times M_t^2 \times\pi / (t \times 4^2 \times M_s^2)$ (4)

Where:

D = Diffusion coefficient (cm$^2$ / h)

t = Time of moisture absorption (h) (data from diffusion area test — 24 hours)

$M_t$ = Moisture absorption rate at the time "t" (wt%) (data from diffusion area test)

1 = Thickness of the specimen (cm) (data from diffusion area test = 0.3 cm)

$M_5$= Saturated moisture absorption rate (wt%) (data of saturated area test)

# SEMI G67-0996 (Reapproved 1104)
# TEST METHOD FOR THE MEASUREMENT OF PARTICLE GENERATION FROM SHEET MATERIALS

This test method was technically reapproved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on July 23, 2004. Initially available at www.semi.org September 2004; to be published November 2004. Originally published September 1996.

## 1 Purpose

1.1 This test method describes a procedure to measure particles on sheet materials.

## 2 Scope

2.1 The method described may be used for the measurement of particles on items such as:

- Leadframe Interleaves,
- Cleanroom Paper, and
- Packing Material.

2.2 The procedures may be used by the material manufacturer for quality control or by a customer at incoming inspection.

**NOTICE:** This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

## 3 Referenced Standards

3.1 None.

**NOTICE:** Unless otherwise indicated, all documents cited shall be the latest published versions.

## 4 Terminology

4.1 None.

## 5 Summary of Method

5.1 The method is based on measuring a background particle count in a clean enclosure and then measuring the increased particle count when items under test are submitted to handling operations likely to generate particles.

## 6 Interference

6.1 Care must be taken to avoid contaminating the clean bench when sheet materials are placed inside. All external packaging material shall be removed and the internal packaging shall be cleaned by appropriate means prior to placing inside the bench.

6.2 A method of cutting the specimens to size, if performed, must not add to, or detract from, the contamination levels on the sheet materials.

6.3 Care must be taken to avoid contaminating the specimens from the human body and clothes when the sheet materials are prepared for the test method.

## 7 Equipment

7.1 *Particle Counter and Recorder*

7.2 *Clean Bench with Full Gloves and a Dust Particle Measurement Port* — See Figure 1.

7.2.1 Air flow speed in the clean bench should be 0.6 m/sec.

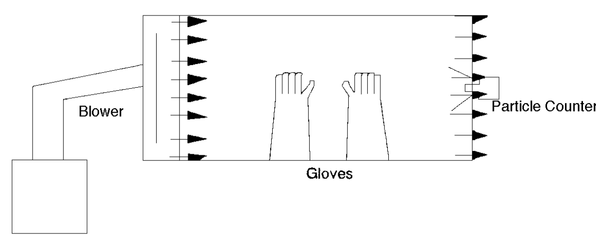



**Figure 1**
**Clean Bench Configuration**

## 8 Sampling

8.1 Sampling plans shall be agreed between user and supplier.

## 9 Test Specimen

9.1 Specimen size shall be agreed between user and supplier. It is recommended that a 152.4 mm × 203.2 mm (6 × 8 inches) test piece be used.

## 10 Equipment Set-Up

10.1 The particle counter shall be set up with the probe in the clean bench. Calibrate the counter in accordance with the equipment manufacturer's instructions.

10.2 Allow the clean bench to come to equilibrium and perform a background particle count.

NOTE 1: Between each test, allow the clean bench to return to a stable background particle count before proceeding with the next test.

NOTE 2: After several thousand particles have been measured, the clean bench must be cleaned before making the next measurement.

## 11 Test Procedure

11.1 Place the items to be tested in the clean bench and allow the clean bench to return to a stable background level for particle count.

11.2 *Crumpling Test*

11.2.1 Crumple a test specimen in gloved hands at the rate of one (1) crumple every fifteen (15) seconds and record the maximum particle count.

11.2.2 Record the maximum particle count and the initial background count.

11.3 *Friction Test*

11.3.1 Place two sheets of the material to be tested face to face and rub together three (3) times in ten (10) seconds.

11.3.2 Record the maximum particle count and the initial background count.

11.4 *Tearing and Crumpling Test*

11.4.1 Tear a sheet into five (5) pieces at the rate of one (1) tear every five (5) seconds. Crumple the pieces in gloved hands at the rate of one (1) crumple every fifteen (15) seconds.

11.4.2 Record the maximum particle count and the initial background count.

## 12 Calculations and Reporting Results

12.1 For each measurement and test method type, calculate the particle count on the material under test as follows:

- Particle Count (no./$m^3$) = (Measured Count from each test) - (Background Count)

12.2 Average the results for each test type.

## 13 Report

The test report shall include the following items:

- Material Designation under Test,
- Manufacturer,
- Shipping Lot Number,
- Test Date,
- Test Conditions — temperature, humidity in the clean bench,
- Particle Counter Sensitivity,
- Test Time, and
- Results for Each Test Type in particles/$m^3$.

NOTE 3: If the test is performed by the manufacturer, some of these items may be replaced by in-house requirements such as manufacturer lot number.

# SEMI G68-0996 (Reapproved 1104)
# TEST METHOD FOR JUNCTION-TO-CASE THERMAL RESISTANCE MEASUREMENTS IN AIR ENVIRONMENT FOR SEMICONDUCTOR PACKAGES

This test method was technically approved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on July 23, 2004. Initially available at www.semi.org September 2004; to be published November 2004. Originally published in 1996.

## 1 Purpose

1.1 The purpose of this test is to determine the thermal resistance of semiconductor packages using thermal test chips. This test method deals with junction-to-case measurements of thermal resistance in air environment.

## 2 Scope

2.1 The results of this test method are used to obtain the junction temperature.

2.2 The measurement results are usually different from the results obtained by testing in the fluid bath environment described in SEMI G30 and SEMI G43.

2.3 This test method uses SI units.

**NOTICE:** This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

## 3 Limitation

3.1 This method applies only to packages whose surface is wide enough to place a thermocouple.

## 4 Referenced Standards

4.1 *SEMI Standards*

SEMI G30 — Test Method for Junction-to-Case Thermal Resistance Measurements of Ceramic Packages

SEMI G32 — Guideline for Unencapsulated Thermal Test Chip

SEMI G38 — Test Method for Still- and Forced-Air Junction-to-Ambient Thermal Resistance Measurements of Integrated Circuit Packages

SEMI G42 — Specification for Thermal Test Board Standardization for Measuring Junction-to-Ambient Thermal Resistance of Semiconductor Packages

SEMI G43 — Test Method for Junction-to-Case Thermal Resistance Measurements of Molded Plastic Packages

**NOTICE:** Unless otherwise indicated, all documents cited shall be the latest published versions.

## 5 Terminology

5.1 *Definitions*

5.1.1 The following definitions and symbols shall apply to this test:

5.1.2 *case top temperature measured in air environment, $T_t$* — in °C, is the temperature at the specified accessible reference point on the package in measured in air environment.

NOTE 1: $T_C$ defined in SEMI G43 is different from $T_t$.

5.1.3 *junction temperature, $T_j$* — in °C, is the temperature of the semiconductor junction on the microcircuit in which the major part of the heat is generated.

5.1.4 *power dissipation $P_H$* — in watt, is the heating power applied to the device causing a junction-to reference point temperature difference.

5.1.5 *thermal resistance measured in air environment, junction to package surface, $\Psi_{jt}$* — in °C/watt, is the temperature difference from the junction to the center point on the package divided by the power dissipation $P_H$.

## 6 Summary of Method

6.1 A thermocouple is attached on the surface of the package on the test board.

6.2 After the chip is heated, the junction temperature is measured by the diode in the test chip. The surface temperature is measured in an air environment by the thermocouple.

6.3 The junction-to-case thermal resistance is calculated using the case temperature, junction temperature and power dissipation.

## 7 Interference

7.1 It is recommended that an operator who is familiar with the measuring system and test method conduct the actual measurement in order to obtain the best result.

7.2 The procedure for attaching the thermocouple described in Section 12.3 on the test package should be followed in order to obtain the accurate measurement result.

## 8 Apparatus

8.1 *Thermocouple*

8.1.1 *Material* — Copper-constantan or equivalent.

8.1.2 *Temperature Range* — -100 to +300°C.

8.1.3 *Wire Size* — No larger than AWG size 36.

8.1.4 *The Junction* — Shall be welded to form a bead rather than soldered or twisted.

8.1.5 *Accuracy* — ± 0.5%.

8.2 *Suitable Electrical Equipment* — As required to provide controlled levels of conditioning power and to make the specified measurements.

8.2.1 *Resolution* — 50 µV and 5 µA.

8.3 *Wind Tunnel (as necessary)* — See SEMI G38 or equivalent.

## 9 Materials

9.1 *Test Chip* — Referred to in SEMI G32, or equivalent.

9.2 *Test Board* — Referred to in SEMI G42, or equivalent.

9.3 *Adhesive* — Alpha Cyano-Acrylate.

9.4 *Aluminum Foil* — 4 mm × 4 mm.

## 10 Setup

10.1 Warm up the test equipment before measurements.

## 11 Calibration

11.1 Calibrate the equipment in accordance with the operation manual as necessary.

## 12 Procedure

12.1 *Preparation of Test Package*

12.1.1 Prepare the semiconductor package in which the test chip is mounted.

12.2 Assemble the package on the test board using solder.

12.3 *Attach the Thermocouple*

12.3.1 Apply adhesive on the center point of the package.

12.3.2 Place the thermocouple and aluminum foil on the adhesive and press the aluminum foil using a finger in order to attach the thermocouple on the package surface as close as possible.

12.4 Measure the thermal characteristic of the diode of the test chip.

NOTE 2: It is recommended that the ambient temperature $T_a$ is measured using the thermocouple.

12.5 Mount the test board in a test socket in a still-air enclosure or wind tunnel as necessary.

12.6 *Heating Chip*

12.6.1 Supply power to the chip.

12.6.2 Adjust the measurement equipment to the measured case temperature $T_t$ or the measured power $P_{H\ (package)}$.

NOTE 3: The thermal resistance usually depends on the power dissipation (see Figure 1). The thermal resistance is variable within a power and stable beyond the power.

12.7 Wait until the thermal characteristic of the diode is stable.

12.8 Calculate the junction temperature $T_j$ by the diode thermal characteristics.

12.9 Measure the case temperature $T_t$ using the thermocouple and record the case temperature.

12.10 Record the voltage and the current in order to obtain the $P_{H\ (package)}$.

## 13 Calculation

13.1 The thermal resistance of the package can be calculated as follows:

$\Psi_{jt}$ (°C/watt) =

$(T_j — T_t) / P_{H\ (package)}$

## 14 Report

14.1 The following details shall be reported:

a. Description of package.

b. Description of test board.

c. Power dissipation of test chip.

d. Thermal resistance $R_{\Psi jt}$ for test condition.

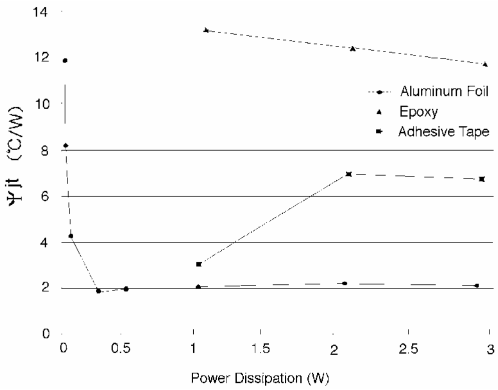



**Figure 1**
**Dependence of $R_{\Psi jt}$ on Power Dissipation**

**NOTICE:** SEMI makes no warranties or representations as to the suitability of the standard set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials or equipment mentioned herein. These standards are subject to change without notice.

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# SEMI G69-0996 (Reapproved 1104)
# TEST METHOD FOR MEASUREMENT OF ADHESIVE STRENGTH BETWEEN LEADFRAMES AND MOLDING COMPOUNDS

This test method was technically approved by the Global Assembly & Packaging Committee and is the direct responsibility of the Japanese Packaging Committee. Current edition approved by the Japanese Regional Standards Committee on July 23, 2004. Initially available at www.semi.org September 2004; to be published November 2004. Originally published in 1996.

## 1 Purpose

1.1 This document describes procedures for measuring adhesive strength between leadframes and molding compounds for semiconductor packages.

1.2 The procedures include shear test, pull test, and three-point bending techniques.

## 2 Scope

2.1 This document may be used on all types of semiconductor leadframe and molding compound.

2.2 The methods help leadframe manufacturers, molding compound manufacturers and their customers in evaluating leadframes, and molding compounds as a guideline.

2.3 The methods in this document use SI units.

**NOTICE:** This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

## 3 Terminology

3.1 None.

## 4 Summary of Method

4.1 *Shear Method* — A frustum-shaped button of molding compound on the surface of a leadframe sample is sheared off the leadframe surface using a tensile tester (see Figure 1).

4.2 *Pull Method* — A sample of leadframe material molded into the side of a block of a molding compound is pulled out using a tensile tester (see Figure 2).

4.3 *Three-Point Bending Method*[1] — Molding compound is molded onto the surface of a leadframe sample such that part of the leadframe is free of molding compound adherence to the surface. Using a bending technique, the adherent molding compound is cracked away from the surface. This process is repeated from both sides of the sample in order to calculate the true adhesive strength (see Figure 3).

## 5 Equipment

5.1 *Tensile Tester*

5.1.1 *Measurement Range* — Maximum 980 N (100 kgf)

5.1.2 Accuracy — ± 1%

5.1.3 *Crosshead Speed* — 2–10 mm/min (recommended), constant speed.

5.1.4 Fixtures suitable for holding the samples, shearing the molding compound, pulling the leadframe, and applying bending load.

5.2 *Chart Recorder*

5.3 Transfer molding machine or suitable replacement that can encapsulate individual samples with required pressure and temperature.

5.4 *Pre-Heater* — High frequency heater for molding compounds.

5.5 *Molds* — Suitable to mold the samples as shown in Figures 1, 2, and 3.

5.6 *Recirculating Air Oven* — With controller in range of 170–180°C.

5.7 Equipment to pre-treat the leadframe sample, as required.

5.8 Ultrasonic inspection apparatus for three-point bending method.

## 6 Configuration and Dimension of Sample

6.1 The sample configuration and dimensions for measurement are shown in Figures 1, 2, and 3.

1 A. Nishimura, I. Hirose and N. Tanaka, "A New Method for Measuring Adhesion Strength of IC Molding Compounds", ASME Journal of Electronic Packaging, Vol. 114, pp 407-412, 1992

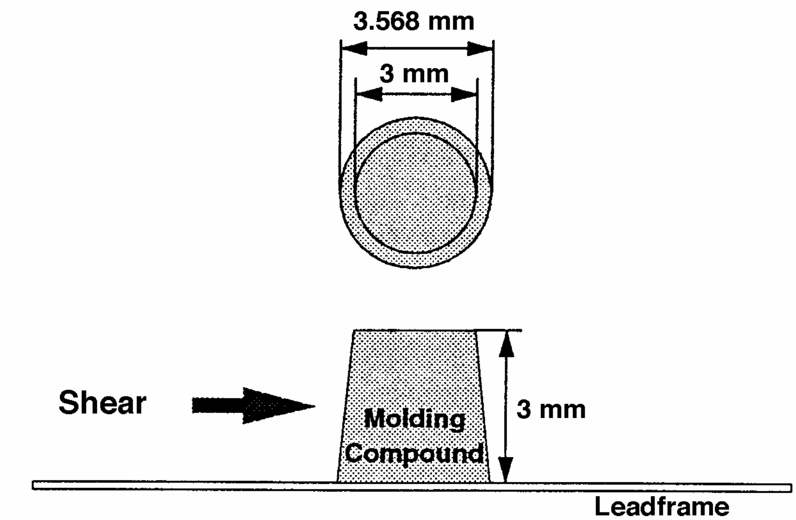


**Figure 1**
**Sample for Shear Method**

| *Adhesive Area* | *Leadframe Thickness* | *Height of Molding Compound* |
|---|---|---|
| $10 \pm 0.5$ mm$^2$ | 0.254–0.125 mm<br>(0.15 mm is recommended) | $3 \pm 0.15$ mm |

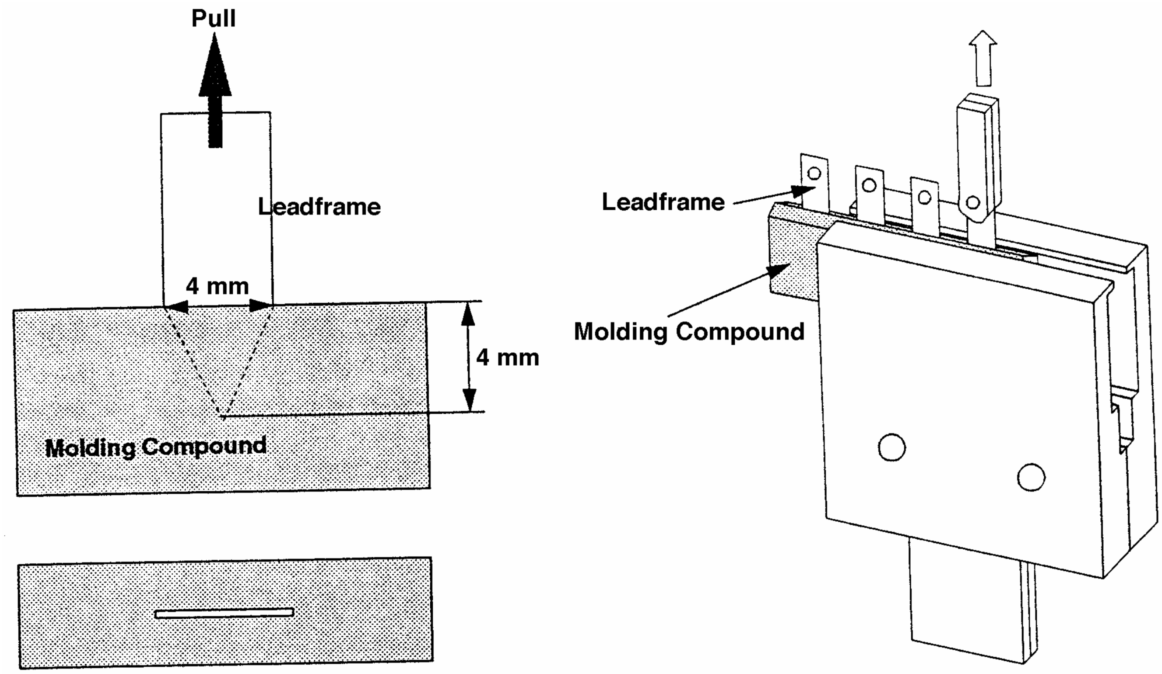


**Figure 2**
**Sample for Pull Method**

| *Adhesive Area* | *Molding Compound Sample Thickness* |
|---|---|
| 16 ± 0.8 mm$^2$ (both sides) | 3.5–4.0 mm (equivalent to DIP 16 300 mil) |

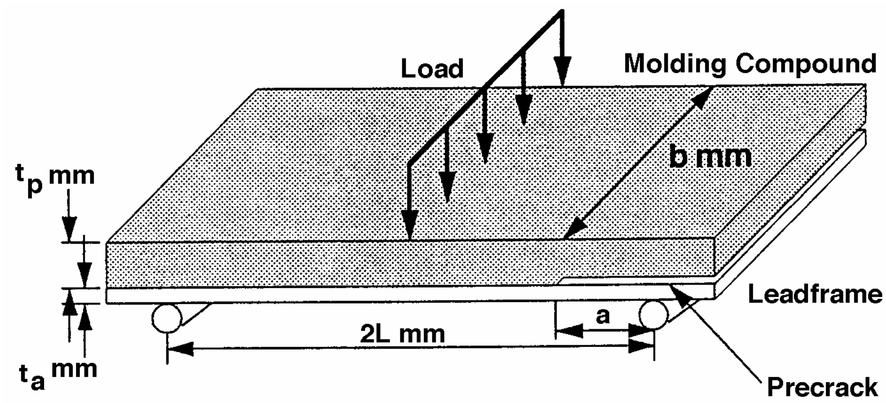


**Figure 3**
**Sample for Three-Point Bending Method**

| | *Molding Compound Thickness $t_p$ (mm)* | *Leadframe Thickness $t_a$ (mm)* | *Span 2L (mm)* | *Pre-Crack Length a (mm)* | *Sample Width b (mm)* |
|---|---|---|---|---|---|
| Standard | 1.5 | 0.25 | 45 | 10–15 | 6 |
| Type A (for low adhesive strength) | 0.8 | 0.2 | 35 | 8–10 | 4 |
| Type B (for high temperature measurement) | 4 | 0.5 | 50 | 10–15 | 6 |
| Other Sample Types | The following equations should be satisfied $2L \geq 8\ (t_p + t_a)$ and $L - a \geq 2\ (t_p + t_a)$ | | | | |

## 7 Sampling Plan

7.1 The sampling plan shall be in agreement between customer and vendor. It is recommended that the following minimum sample sizes are used:

- *Shear Method* — Four (4) samples
- *Pull Method* — Four (4) samples
- *Three-Point Bending Method* — Three (3) samples in each direction

NOTE 1: Three-point bending method needs at least 2 samples to obtain adhesive strength.

## 8 Materials

8.1 Leadframe or appropriated sample from strip meeting dimensions for test.

8.2 Molding compound

## 9 Sample Preparation

9.1 *Leadframe Sample Preparation*

9.1.1 Process the leadframe samples through the various cleaning and heat cycles that would be normal for the leadframe under consideration as required.

NOTE 2: When this method is applied to copper leadframes, copper oxide on the surface shall be considered when results are interpreted.

9.2 Clean and condition the molds to provide well formed samples as required.

9.3 Set the molds to the specified temperature and record the temperature.

9.4 Set the transfer molding pressure, transfer time and cure time to the following recommended molding conditions. If the condition is not suitable for the material, the condition should be agreed between customer and vendor.

| *Molding condition* | |
|---|---|
| Cure temperature | 170–180°C |
| Cure time | 120 sec. |
| Molding pressure | 6.8–7.8 MPa (70–80 kgf/cm$^2$) |

9.5 Mold all the required samples.

9.6 Remove the samples from the molds.

NOTE 3: After removing the samples from the molds, natural cooling of the samples is recommended.

9.7 Post mold cure the samples at the following recommended conditions.

| *Post-cure condition* | |
|---|---|
| Temperature | 175 ± 5°C |
| Time | 4–8 hours |

9.8 Store the samples and record the storage conditions.

9.9 *Three-Point Bending Samples*

9.9.1 In addition to the treatment mentioned in Section 10.1.1, and to facilitate cracking during the three point bending method, apply a thin layer of mold release to on end of the leadframe sample in order to form a "pre-crack" condition (i.e., the molding compound will not adhere to this section of the sample, see Figure 3).

NOTE 4: It is recommended that toluen-based thermosetting silicone be used as a mold release agent to prevent molding process contamination.

## 10 Calibration

10.1 *Tensile Tester Calibration*

10.1.1 Calibrate the tensile tester in accordance with the manufacturer's instructions.

## 11 Test Procedure

11.1 *Shear Method*

11.1.1 Attach the sample to the tensile test such that shear may be applied.

11.1.2 Place the shear tool against the molding compound formation and initiate a load at a constant speed between 2–10 mm/min while recording the load and displacement.

11.1.3 Record the peak load before the sudden drop in applied load as the sample shears off the leadframe or the molding compound breaks.

NOTE 5: Disregard any results which have the appearance of sample slipping or shear tool riding over the molding compound.

11.2 *Pull Method*

11.2.1 Attach the sample to the tensile tester such that the leadframe may be pulled out of the molding compound with a vertical pull action.

11.2.2 Attach the pulling grips to the leadframe and initiate a load at a constant speed between 2–10 mm/min. while recording the load and displacement.

11.2.3 Record the peak load before the sudden drop in applied load as the sample is pulled from the molding compound samples.

NOTE 6: Disregard any results which have the appearance of slippage of the sample or pulling grips.

11.3 *Three-Point Bending Method*

11.3.1 Measurement of the pre-crack length

11.3.1.1 Measure the pre-crack length using an ultrasonic inspection technique (see Figure 4).

NOTE 7: The sample, in this case, is placed in the vessel with the leadframe side up, and then secured with an adhesive tape so that the water cannot penetrate into the interface area created by the mold release.

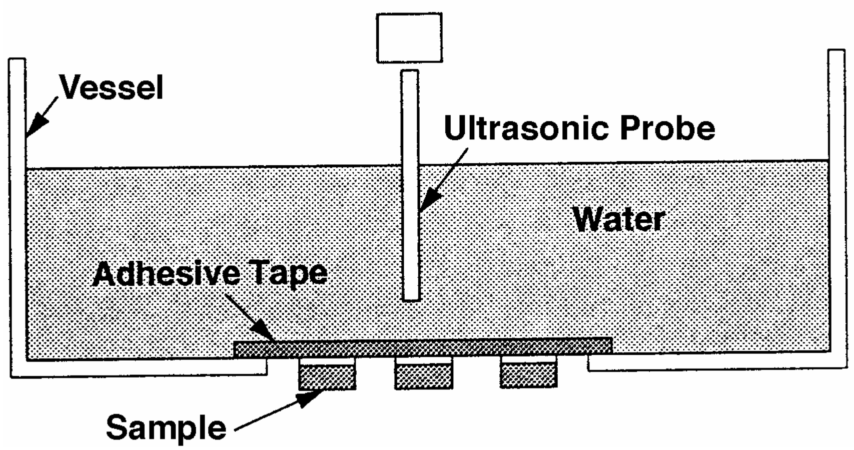


Figure 4
**Measurement of Pre-Crack Length**

11.3.2 *Test Procedure*

11.3.2.1 Attach support fixture and load wedge to the tensile tester.

11.3.2.2 Place the sample on the support fixture with the molded side up (see Figure 5).

NOTE 8: The support fixture tool should be located at a constant distance from the tip of pre-crack for every measurement.

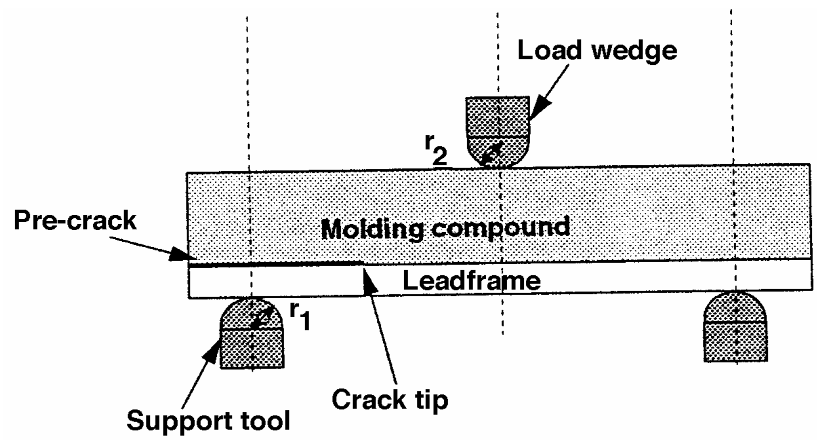


**Figure 5**
**Sample Setup**

| | |
|---|---|
| Radius of support tool $r_1$ | 5–8 mm |
| Radius of load wedge $r_2$ | 2–5 mm |

11.3.2.3 Place the load wedge in contact with the molded surface and initiate the loading at a constant speed between 2–10 mm/min while recording the load and displacement.

11.3.2.4 Record the peak load before the sudden drop in applied load.

11.3.2.5 Repeat the test with another sample which has the leadframe side up.

## 12 Calculation

12.1 *Shear and Pull Method*

12.1.1 The adhesive strength is calculated as follows:

12.1.1.1 Adhesive Strength (N/mm$^2$) = Peak Load (N)/Nominal Adhesive Area (mm$^2$)

12.2 *Three-Point Bending Method*

12.2.1 *Apparent Adhesive Strength* — Apparent adhesive strength including residual stress, is calculated using the stress intensity factor $K_i$ as follows:

$$K_i = 4 \times 10^{-6} \cosh(\varepsilon\pi) \sqrt{\frac{G}{\frac{\kappa_p + 1}{\mu_p} + \frac{\kappa_a + 1}{\mu_a}}}$$

where

$$G = 3\left\{\frac{1}{t_p^3E_p + t_p^3E_a} - \frac{t_pE_p + t_aE_a}{k}\right\}\frac{P^2a^2}{2b^2}$$

$$k = 4t_pt_aE_pE_a\left(t_p + t_a\right)^2 + \left(t_p^2E_p + t_a^2E_a\right)^2$$

$$\varepsilon = \frac{1}{2\pi}\ln\left\{\frac{\frac{\kappa_p}{\mu_p} + \frac{1}{\mu_a}}{\frac{\kappa_a}{\mu_a} + \frac{1}{\mu_p}}\right\}$$

$$\kappa_j = 3 - 4\nu_j \qquad \text{(j = p or a)}$$

$P$ : Peak load (N)

$a$ : Pre - crack length (m)

$b$ : Sample width (m)

$t_p$ : Thickness of molding compound (m)

$t_a$ : Thickness of leadframe (m)

$E_p$ : Young' s modulus of molding compound (Pa)

$E_a$ : Young' s modulus of leadframe (Pa)

$\mu_p$ : Shear modulus of molding compound (Pa)

$\mu_a$ : Shear modulus of leadframe (Pa)

$\nu_p$ : Poisson' s ratio of molding compound

$\nu_a$ : Poisson' s ratio of leadframe