Table 6 Dimensional Characteristics of 150 mm Polished Monocrystalline Silicon Wafers with Secondary Flat[#1]

Previous SEMI Reference:		*SEMI M1.8*	
Wafer Category:		*1.8.1*	*1.8.2*
Property		*150 mm Wafers*[#2]	
2-6.1	Diameter	150.00 ± 0.20 mm	
2-6.2	Primary Flat Length	57.5 ± 2.5 mm	
2-6.3	Primary Flat Orientation[#3]	{110} ± 1°	
2-6.4	Secondary Flat Length	37.5 ± 2.5 mm	
2-6.5	Secondary Flat Location (See Figure 4) {111} *p*-type {100} *p*-type {111} *n*-type {100} *n*-type	 No secondary flat 90° ± 5° clockwise from primary flat (θ = 180° ± 5°) 45° ± 5° clockwise from primary flat (θ = 225° ± 5°) 135° ± 5° clockwise from primary flat (θ = 135° ± 5°)	
2-6.6	Edge Profile Coordinate, C_y	T/3 Template (See Table 3) 225 µm	T/4 Template (See Table 3) 169 µm
2-6.7	Thickness, Center Point	675 ± 20 µm	
2-6.8	Total Thickness Variation, Max.	10 µm	
2-6.9	Bow, Max.	60 µm	
2-6.10	Warp, Max.	60 µm	
2-5.7	Edge Surface Condition	Supplier-customer agreement[#4]	

[#1] Note that these specifications were originated in the United States. Care should be taken in applying this configuration to specific applications (see ¶6.6.3).

[#2] For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. CAUTION: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

[#3] For (111) wafers, the $(1\bar{1}0)$, $(01\bar{1})$, , and $(\bar{1}01)$ planes are the equivalent, allowable (110) planes. For (100) wafers, the allowable equivalent (110) planes are $(01\bar{1})$, (011), $(0\bar{1}1)$, and $(0\bar{1}\bar{1})$.

[#4] If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

Table 7 Dimensional Characteristics of 100 mm and 125 mm Polished Monocrystalline Silicon Wafers without Secondary Flat[#1]

	Previous SEMI Reference:	*SEMI M1.11*	*SEMI M1.12*
	Wafer Category:	*1.11*	*1.12*
	Property	*100 mm Wafers without secondary flat (t=525μm)*[#2]	*125 mm Wafers without secondary flat (t=625μm)*[#2]
2-6.1	Diameter	100.00 ± 0.20 mm.	125.00 ± 0.20 mm
2-6.2	Primary Flat Length	32.5 ± 2.5 mm	42.5 ± 2.5 mm
2-6.3	Primary Flat Orientation[#3]	{110} ± 1°	
2-6.5	Secondary Flat Location	No secondary flat	
2-6.6	Edge Profile Coordinate, C_y (T/3 Template, see Table 3)	175 μm	208 μm
2-6.7	Thickness, Center Point	525 ± 15 μm.	625 ± 15 μm
2-6.8	Total Thickness Variation, Max.	10 μm	
2-6.9	Bow, Max.	40 μm	
2-6.10	Warp, Max.	40 μm	

[#1] Note that these specifications were originated in Japan. They are equivalent to the specifications for wafers of the same nominal diameter in JEITA EM-3602. Care should be taken in applying this configuration to specific applications (see ¶6.6.3).

[#2] For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. CAUTION: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

[#3] For (111) wafers, the $(1\bar{1}0)$, $(01\bar{1})$, and $(\bar{1}01)$ planes are the equivalent, allowable (110) planes. For (100) wafers, the allowable equivalent (110) planes are $(01\bar{1})$, (011), $(0\bar{1}1)$, and $(0\bar{1}\bar{1})$.

Table 8 Dimensional Characteristics of 150 mm and 200 mm Polished Monocrystalline Silicon Wafers without Secondary Flat[#1]

	Previous SEMI Reference:	*SEMI M1.13*		*SEMI M1.10*	
	Wafer Category:	*1.13.1*	*1.13.2*	*1.10.1*	*1.10.2*
	Property	*150 mm Wafers without secondary flat (t=625 μm)[#2]*		*200 mm Wafers flatted, without secondary flat[#2]*	
2-6.1	Diameter	150.00 ± 0.20 mm		200.00 ± 0.20 mm	
2-6.2	Primary Flat Length	47.5 ± 2.5 mm		Not applicable	
	Flat Diameter	Not applicable		195.50 ± 0.20 mm	
2-6.3	Primary Flat Orientation[#3]	{110} ± 1°			
2-6.5	Secondary Flat Location	No secondary flat			
2-6.6	Edge Profile Coordinate, C_y (see Table 3)	T/3 Template 208 μm	T/4 Template 156 μm	T/3 Template 242 μm	T/4 Template 181 μm
2-6.7	Thickness, Center Point	625 ± 15 μm		675 ± 15 μm	
2-6.8	Total Thickness Variation, Max.	10 μm			
2-6.9	Bow, Max.	60 μm		65 μm	
2-6.10	Warp, Max.	60 μm		75 μm	
2-5.7	Edge Surface Condition	Not specified		Supplier-customer agreement[#4]	

[#1] Note that these specifications were originated in Japan. They are equivalent to the specifications for wafers of the same nominal diameter in JEITA EM-3602. Care should be taken in applying this configuration to specific applications (see ¶6.6.3).

[#2] For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. CAUTION: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

[#3] For (111) wafers, the $(1\bar{1}0)$, $(01\bar{1})$, and $(\bar{1}01)$ planes are the equivalent, allowable (110) planes. For (100) wafers, the allowable equivalent (110) planes are $(01\bar{1})$, (011), $(0\bar{1}1)$, and $(0\bar{1}\bar{1})$.

[#4] If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

Table 9 Dimensional Characteristics and Wafer ID Marking Requirements for Notched 200 mm and 300 mm Polished Monocrystalline Silicon Wafers[#1]

	Previous SEMI Reference:	*SEMI M1.9*		*SEMI M1.15*
	Wafer Category:	*1.9.1*	*1.9.2*	*1.15*
	Property	*200 mm Wafers (Notched)*[#2]		*300 mm Wafers (Notched)*[#2]
2-6.1	Diameter	200.00 ± 0.20 mm.		300.00 ± 0.20 mm
2-6.2	Notch Dimensions (See Figure 5) Depth Angle	1.00 mm +0.25 mm –0.00 mm 90° +5° –1°		
2-6.3	Orientation of Notch Axis[#3]	<110> ± 1°		
2-6.5	Secondary Fiducial Location	No secondary fiducial		
2-6.6	Edge Profile Coordinate, C_y (see Table 3)	T/3 Template 242 µm	T/4 Template 181 µm	T/4 Template 194 µm
2-6.7	Thickness, Center Point	725 ± 20 µm.		775 ± 20 µm
2-6.8	Total Thickness Variation, Max.	10 µm		10 µm[#4]
2-6.9	Bow, Max.	65 µm		Not specified
2-6.10	Warp, Max.	75 µm		100 µm[#5]
2-5.1	Wafer ID Marking	Supplier-customer agreement		SEMI T7 mark with optional A/N mark (See ¶6.5.1.4)
2-5.7	Edge Surface Condition	Supplier-customer agreement[#6]		Polished[#6]
2-9.8	Back Surface Brightness (Gloss)	Not specified		0.80[#6,#7]

[#1] Note that these specifications were originated in the United States. Care should be taken in applying this configuration to specific applications (see ¶6.6.3). The specification for 300 mm wafers is essentially equivalent to the specification for wafers of this diameter in JEITA EM-3602.

[#2] For referee purposes, metric (SI) units apply. To ensure that product shipped is within specification, any conversion to U.S. Customary equivalents should be done following the maximum-minimum convention in which the minimum values are rounded-up and the maximum values are rounded-down to ensure that the equivalent range is always inside the referee range. If U.S. Customary equivalents are used for incoming inspection, minimum values should be rounded-down and maximum values rounded-up to avoid rejection of material that is within the specification when measured by the referee system of units. CAUTION: The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data which can be used to construct appropriate guard bands.

[#3] For 200 mm (111) wafers, the $[1\bar{1}0]$, $[01\bar{1}]$, , and $[\bar{1}01]$ axes are the equivalent, allowable <110> axees. For (100) wafers, the allowable equivalent <110> axes are $[01\bar{1}]$, $[011]$, $[0\bar{1}1]$, and $[0\bar{1}\bar{1}]$.

[#4] Full wafer scan as described in SEMI MF1530.

[#5] Warp corrected for gravitational effects. However, warp is not an adequate wafer shape specification for all applications.

[#6] If specified as polished, this term is meant to imply a surface condition and not a particular processing technique. If desired, a quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures, including sampling plan and detrending procedures, shall be agreed upon between supplier and customer.

[#7] Gloss as measured in accordance with ASTM Test Method D 523 or JIS Z 8741 with visible illumination at a 60° angle of incidence referenced to a mirror polished silicon wafer front surface. This metric may not describe the back surface finish adequately to establish detectability of small localized light scatterers (LLSs). If it is necessary to detect LLSs smaller than 0.25 µm LSE, another quantitative measure of surface finish may optionally be indicated by specifying the rms microroughness over a specified spatial frequency (or wavelength) range. Because a standardized test method has not yet been developed for this metric, both values and test procedures shall be agreed upon between supplier and customer.

6.6.3 *Shape* — The shape decision tree in Appendix 2 fully describes the various shape parameters that can be specified.

6.6.3.1 Warp is generally the most often specified shape parameter. Only wafers of category 1.1 (2 in. diameter) do not have a warp specification. Note that there are two forms of warp, one corrected for gravitational sag and the other not so corrected.

6.6.3.2 If bow is specified, a sign may be included in the specification to denote convex (positive) or concave (negative) curvature of the median surface of the wafer with the front surface up. If no sign is included in the specification, bow may vary between -*a* and +*a*, where "*a*" is the specified maximum magnitude of bow.

6.6.3.3 Sori is an attribute that may be specified with agreement between the supplier and customer in lieu of or in addition to bow and/or warp.

6.6.4 *Standard Wafer Categories* — The standardized dimensions, dimensional tolerances, and fiducial (flat or notch) characteristics for various standard wafer categories are summarized in Tables 4 through 9. These categories of wafers shall meet all requirements listed in the appropriate table, unless an exception is negotiated between supplier and customer and is shown on the purchase order.

6.6.4.1 Wafers of the same nominal diameter may typically have different dimensional configurations in different regions of the world. Many of these configurations are represented in these tables. In selecting the appropriate standard polished wafer category, consideration should be given to compatibility with processes and equipment generally available in the region of use.

6.6.5 *Flatness* — The wafers shall meet global and site flatness requirements as specified in the purchase order. Details of different flatness parameters are given in Appendix 1.

6.6.6 *Nanotopography* — The wafers shall meet nanotopography requirements specified in the purchase order.

6.7 *Front Surface Chemistry*

6.7.1 If surface metal contamination levels are specified on the purchase order, the maximum area densities shall be designated in units of atoms/cm^2 for specific individual elements together with the measurement method by which the densities are to be determined. The wafers shall not contain more than the specified density of each metal.

NOTE 3: An example of such a specification applicable to 1 μm geometries is given in Related Information 1.

6.7.2 If surface organic contamination levels are specified on the purchase order, the maximum area densities shall be designated in units of ng/cm^2 for total surface organics density together with the method by which the density is to be determined. The wafers shall not contain more than the specified density of total surface organics.

6.8 *Front and Back Surface Inspection Characteristics*

6.8.1 The wafers shall conform to the limits on observable (visually or otherwise) front and back surface characteristics as specified on the purchase order.

6.8.2 For wafers of diameter 150 mm or smaller for which visual inspection of surface defects is acceptable, the defect limits in Table 10 may be used as a guide for determining acceptable defect levels. Under these circumstances, minimal conditions or dimensions for surface features to be considered as defects are stated below. These limits shall be used for determining wafer acceptability; anomalies smaller than these limits shall not be considered defects.

6.8.2.1 *Item 2-8.1, scratches, macro* — Any anomaly conforming to the definition that has a length-to-width ratio greater than 5:1 and is visible under diffuse illumination as well as under high intensity illumination.

6.8.2.2 *Item 2-8.2, scratches, micro* — Any anomaly conforming to the definition that has a length-to-width ratio greater than 5:1 and is visible only under high intensity illumination.

6.8.2.3 *Item 2-8.3, pits* — Any individually distinguishable nonremovable surface anomaly conforming to the definition that is visible when viewed under intense illumination.

6.8.2.4 *Item 2-8.4, haze* — Haze is indicated when the image of a narrow beam tungsten lamp filament is detectable on the polished wafer surface. Under some conditions, contamination may appear as haze.

Table 10 Polished Wafer Defect Limits

Item	*Characteristics*	*Maximum Defect Limit*	*AQL*[#1]	*Illumination Conditions*[#2]
FRONT SURFACE				
2-8.1	Scratches – Macro[#3]	None		Diffuse
2-8.2	Scratches – Micro[#3]	None		High Intensity
2-8.3	Pits[#3]	None	1.0% Cum.	High Intensity
2-8.4	Haze[#3]	None	1.0%	High Intensity
2-8.5	Localized Light Scatterers (LLS) (Contamination, Particulate) [#3] Maximum Number 2 in. Diameter Wafer 3 in. Diameter Wafer 100 mm Diameter Wafer 125 mm Diameter Wafer 150 mm Diameter Wafer	 4 6 10 10 15	1.0%	High Intensity
2-8.6	Contamination, Area[#3]	None	1.0%	High Intensity or Diffuse
2-8.7	Edge Chips and Indents[#4]	None	1.0% Cum. with item 15[#5]	Diffuse
2-8.9	Cracks, Crow's Feet	None		Diffuse
2-8.10	Craters[#3]	None		Diffuse
2-8.11	Dimples[#3]	None		Diffuse
2-8.12	Grooves[#3]	None	1.0% Cum.	Diffuse
2-8.13	Mounds[#3]	None		Diffuse
2-8.14	Orange Peel[#3]	None		Diffuse
2-8.15	Saw Marks[#3]	None	1.0% Cum.	Diffuse
2-8.16	Resistivity Striations (Dopant Striation Rings)	None, except on low resistivity wafers[#6].		Diffuse
BACK SURFACE				
2-9.1	Edge Chips[#4]	None	1.0% Cum. with item 6[#5]	Diffuse
2-9.3	Cracks, Crow's Feet	None		Diffuse
2-9.4	Contamination, Area	None	1.0% Cum.	Diffuse
2-9.5	Saw Marks[#7]	None	1.0% Cum.	Diffuse
ALL LISTED CHARACTERISTICS			Total 2.5%	

[#1] Single, Normal, Level II Sampling Plan as defined in ANSI/ASQC Z1.4.

[#2] See SEMI MF523 for definition of Illumination Conditions.

[#3] The outer 0.062 inch (1.57 mm) annulus is excluded from these criteria.

[#4] For wafers that are not mechanically edge-rounded, accept/reject criterion shall be agreed upon between supplier and customer.

[#5] The cumulative AQL for both front surface and back surface of wafer is 1.0%.

[#6] Striations may be visible on low resistivity wafers (<0.020 Ω·cm).

[#7] For non-lapped wafers accept/reject criterion shall be agreed upon between supplier and customer.

6.8.2.5 *Item 2-8.5, localized light scatterers (particulate contamination)* — Distinct particles or other surface anomalies resting on the surface that are revealed under collimated light as bright points.

6.8.2.6 *Items 2-8.6 and 2-9.4, area contamination* — Any foreign matter on the surface in localized areas that is revealed under the inspection lighting conditions as discolored, mottled, or cloudy appearance resulting from smudges, stains, water spots, etc.

6.8.2.7 *Items 2-8.7 and 2-9.1, edge chips and indents* — Any edge anomaly including saw exit marks conforming to the definition that is greater than 0.010 in. (0.25 mm) in radial depth and peripheral length.

6.8.2.8 *Items 2-8.9a and 2-9.3a, cracks* — Any anomaly conforming to the definition that is greater than 0.25 mm (0.010 in. for 2 and 3 in. diameter wafers) in total length.

6.8.2.9 *Items 2-8.9b and 2-9.3b, crow's feet*—Any anomaly conforming to the definition that is greater than 0.25 mm (0.010 in. for 2 and 3 in. diameter wafers) in total length.

6.8.2.10 *Item 2-8.10, craters*—Any individually distinguishable surface anomaly conforming to the definition that is visible when viewed under diffused illumination.

6.8.2.11 *Item 2-8.11, dimples*—Any smooth surface depression greater than 3 mm in diameter.

6.8.2.12 *Item 2-8.12, grooves*—Any anomaly conforming to the definition that is greater than 0.13 mm (0.0005 in. for 2 in. and 3 in. diameter wafers) wide or 0.76 mm (0.030 in. for 2 in. and 3 in. diameter wafers) in length.

6.8.2.13 *Item 2-8.13, mounds* — Any anomaly conforming to the definition that is greater than 0.25 mm (0.010 in. for 2 in. and 3 in. diameter wafers) in maximum dimension.

6.8.2.14 *Item 2-8.14, orange peel* — Any visually detectable roughened surface conforming to the definition that is observable under diffused illumination.

6.8.2.15 *Items 2-8.15 and 2-9.5, saw marks* — Any anomaly conforming to the definition that is visible under diffuse illumination.

6.8.2.16 *Item 2-8.16, resistivity striations* (*dopant striation rings*) — Any feature conforming to the definition that is detectable under diffused lighting conditions.

6.8.3 For other cases, acceptable surface defect levels shall be defined based on the use of surface scanning inspections systems (SSIS) for automated surface inspection. In this case, definitions of what surface anomalies constitute surface defects shall be agreed upon between supplier and customer.

7 Basic Specification Requirements

7.1 A basic silicon wafer specification is one that describes a commercially appropriate prime silicon wafer product having stable quality and parametric control. Wafers procured to this specification for 300 mm diameter, double side polished silicon wafers shall meet all of the requirements of Table 11 without any change or additional options. Listed specification values represent generally accepted silicon wafer process capability that is consistent with many advanced integrated circuit applications at the 130 nm technology level.

Table 11 Basic Specification for 300 mm Polished Prime Silicon Wafers for the 130 nm Technology Node

	Item	*Specification*
2-1. GENERAL CHARACTERISTICS		
2-1.1	Growth Method	Supplier Option of Cz or MCz
2-1.2	Use of Refined Polysilicon	Permitted
2-1.4	Conductivity Type	*p*
2-1.5	Dopant	Boron
2-1.6	Nominal Edge Exclusion	3 mm
2-1.8	Wafer Surface Orientation	(100) ± 0.5°
2-2. ELECTRICAL CHARACTERISTICS		
2-2.1	Resistivity	Center Point (Target): 1.5 Ω·cm, 10 Ω·cm, or 21 Ω·cm Resistivity Tolerance: ±33%
2-2.2	Radial Resistivity Variation	±10% at 6 mm from edge as in SEMI MF81, Sampling Plan B
2-3. CHEMICAL CHARACTERISTICS		
2-3.1	Oxygen Concentration	Center Point (target): 15 or 18 ppma (IOC-88) Tolerance: ±1.5 ppma (IOC-88)
2-3.2	Radial Oxygen Variation	≤10% at 10 mm from edge as in SEMI MF951, Sampling Plan A1
2-3.3	Carbon Concentration	≤0.5 ppma (SEMI MF1391)
2-4. STRUCTURAL CHARACTERISTICS		
2-4.1	Dislocation Etch Pit Density	None
2-4.2	Slip	None
2-4.7	Oxidation Induced Stacking Faults	≤100 cm^{-2}

	Item	*Specification*
2-5. WAFER PREPARATION CHARACTERISTICS		
2-5.1	Wafer ID Marking	SEMI T7 plus optional Alphanumeric Mark per Wafer Category 1.15 (see Figure 3)
2-5.7	Edge Surface Condition	Polished
2-5.8	Back Surface Condition	Polished
2-6. DIMENSIONAL CHARACTERISTICS		
2-6.1	Diameter	300.00 ± 0.20 mm
2-6.2	Notch Dimensions	In accordance with requirements of Wafer Category 1.15 (see Figure 5)
2-6.3	Notch Orientation	<110> ± 1°
2-6.6	Edge Profile	T/4 Template (see Figure 6)
2-6.7	Thickness	775 ± 20 μm
2-6.8	Total Thickness Variation (GBIR)	≤10 μm
2-6.10	Warp	≤100 μm
2-6.13	Site Flatness [SFQR][#1]	>99.9% of all full sites ≤200 nm; Site size: 26 mm × 8 mm Include partial sites: No Offset: None
2-7. FRONT SURFACE CHEMISTRY		
2-7.1	Surface Metal Contamination[#2]	$\leq 1 \times 10^{10}$ cm^{-2}
2-8. FRONT SURFACE INSPECTION CHARACTERISTICS		
2-8.1	Scratches – macro	None
2-8.2	Scratches – micro	None
2-8.5	Localized Light Scatterers (LLS)	≤1200/wafer, ≥0.12μm (LSE) and ≤10/wafer, ≥0.25μm (LSE)
2-8.7	Edge Chips	None
2-8.8	Edge Cracks	None
2-9. BACK SURFACE INSPECTION CHARACTERISTICS		
2-9.1	Edge Chips and Indents	None
2-9.2	Edge Cracks	None
2-9.4	Area Contamination	None
2-9.9	Scratches – macro	<0.25 × Diameter
2-9.10	Scratches – micro	Not Specified

[#1] This site flatness process capability allows approximately one full site to have SFQR >200 nm for every four wafers shipped.

[#2] Individual process median capability for each of the following metal contaminants: Al, Ca, Cr, Cu, Fe, K, Na, Ni, and Zn. Due to high measurement variability, data are recorded for process capability and not for individual shipment quality reports.

7.2 Effective implementation of the basic specification concept requires the standardization of many wafer characteristics that have not historically been specified in a SEMI standard, as well as some characteristics that have historically been specified in SEMI standards, but have been routinely modified as a customer preference. The resulting variety of customer specifications causes silicon suppliers to install additional processes and metrics, or different processes and technologies for satisfying individual specifications. To realize the full benefits of a basic specification, it is essential that all parameters be accepted without additional options.

7.3 Wafers produced to this specification shall be qualified through routine process checks, demonstrating the process is in state of control. Verification of the process and quality control shall be provided on a shipment basis through a certification that does not require the inclusion of data specifically from that shipment.

8 Sampling

8.1 Unless otherwise specified, ASTM Practice E 122 shall be used to define the sampling plan. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

9 Test Methods

9.1 Measurements shall be made or certifiable to one of the SEMI, ASTM, JEITA, JIS, or DIN standard test methods for the item as selected from Table 1 and specified in the purchase order.

9.2 If several different standard test methods for an item are commonly used within a region, it is particularly important that the applicable method of test be identified in the purchase order.

9.3 If no method of test is specified in the purchase order and if standard test methods from different geographic regions are available, the default method shall be a method in common usage for the region of the purchaser of the wafer.

9.4 If no standard test method for an item is available, the test procedure to be used must be agreed upon between supplier and customer.

9.5 Information about the various test methods listed in Table 1 is provided in Related Information 2 together with information about some additional test methods no longer in wide use throughout the industry.

10 Certification

10.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

10.2 In the interest of controlling inspection costs, the supplier and the customer may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in §9. However, if the customer performs the test and the material fails to meet the requirement, the material may be subject to rejection.

11 Product Labeling

11.1 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductivity type, dopant, orientation, resistivity range, and lot number. The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one month after that particular lot has been accepted by the customer.

11.2 Alternatively, if agreed upon between supplier and customer, one of the box labeling schemes in SEMI T3 shall be used and the information listed in ¶11.1 that is not included on the label shall be retained in the supplier's data base for at least one month after that particular lot has been accepted by the customer.

11.3 Wafers of Category 1.15 (300 mm in diameter) shall be shipped in packages labeled in accordance with SEMI M45.

12 Packing and Shipping Container Labeling

12.1 Special packing requirements shall be subject to agreement between the supplier and customer. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination and in accordance with the best industry practices to provide ample protection against damage during shipment.

12.2 Wafers of Category 1.15 (300 mm in diameter) shall be shipped in accordance with SEMI M45.

12.3 Unless otherwise indicated in the purchase order, all outside wafer shipping containers shall be labeled in accordance with ANSI/EIA 556-B.

APPENDIX 1
FLATNESS DECISION TREE

NOTICE: The material in this appendix is an official part of M1. Approval was by full letter ballot procedures with publication authorized by the NA Regional Standards Committee on October 21, 1999.

A1-1 Scope

A1-1.1 The increasing complexity of integrated circuits and the reduction in design rule dimensions place new demands on the characterization of wafer surface geometry. Various high resolution optical lithographic systems have very limited depth of field and use a variety of methods to hold the wafer, to establish the focal plane, and to position the wafer relative to the focal plane during exposure. These varying focusing and location methods differ enough to make a single, simple flatness criterion (such as global TIR) ineffective in predicting successful or unsuccessful lithography in all cases.

A1-1.2 To clarify the requirements for wafer flatness characterization for the various classes of lithographic equipment, the decision tree depicted in Figure A1-1 has been developed. This tree gives an orderly procedure for selecting the various parameters that must be specified if wafer flatness is specified.

A1-1.3 In this tree, it is assumed that the focal point is the site center for all parameters, except for SFQD, SFQR, SFSD, and SFSR, where the focal plane is identical to the reference plane. Most flatness characterization systems employ this convention. However, a number of photolithographic aligners use slightly different conventions for determining the focal plane. Currently, the difference between the centerpoint and other focusing conventions has not been quantified, but it is presumed to be insignificant for material characterization purposes.

A1-1.4 For sites to be included in the measurement, the site center must lie within the Flatness Quality Area (FQA). For subsites (se Figure A1-2) to be included in the measurement, the subsite center must lie within a site whose center is within the FQA and some of the subsite must lie within the FQA (see Figure A1-3).

A1-2 Use of the Flatness Decision Tree

A1-2.1 In the decision tree, there are decision blocks, shown as diamonds, whose use requires some knowledge of the lithographic tool to be used. The rectangular blocks require information to be furnished; this information is dependent on the device layout and the manufacturing procedures to be employed (such as dedicated or mixed aligner use).

A1-2.2 *Step 1* — Select the Fixed Quality Area (FQA): Decide on and specify the nominal edge exclusion, *EE*, which defines the FQA. (See Figure 1.)

A1-2.3 *Step 2* — Choose the Measurement Method: Choose global flatness (G) if the lithographic tool uses a single, global exposure of the wafer, or choose site flatness (S) if the lithographic tool steps across the wafer, exposing only a portion of the wafer at a time.

A1-2.3.1 If global flatness is chosen, proceed to Step 3. If site flatness is chosen, it is also necessary to specify site size (related to exposure area dimensions) and site array (including (a) number of sites, (b) location of sites relative to the center of the FQA and to each other, as in an offset or bricklaying pattern, and (c) whether or not partial sites are to be excluded).

A1-2.4 *Step 3* — Choose the Reference Surface: Choose front surface (F) or back surface (B), depending on whether the lithographic tool is referenced to the front or back surface.

A1-2.5 *Step 4* — Choose the Reference Plane and Area:

A1-2.5.1 For global flatness measurements, a global reference plane is appropriate. If the lithographic tool is referenced to the back surface, an ideal plane (I) defined by the chuck which holds the wafer is appropriate. If the lithographic tool is referenced to the front surface, either a 3-point plane (3) defined by three points equally spaced about the edge of the front surface of the wafer or a plane defined by the least squares fit to the front surface (L) may be appropriate. The 3-point plane is appropriate if the lithographic tool holds the wafer in this fashion and does not allow interactive gimbaling of the wafer, while the least squares plane is appropriate if the lithographic tool allows interactive gimbaling of the wafer.

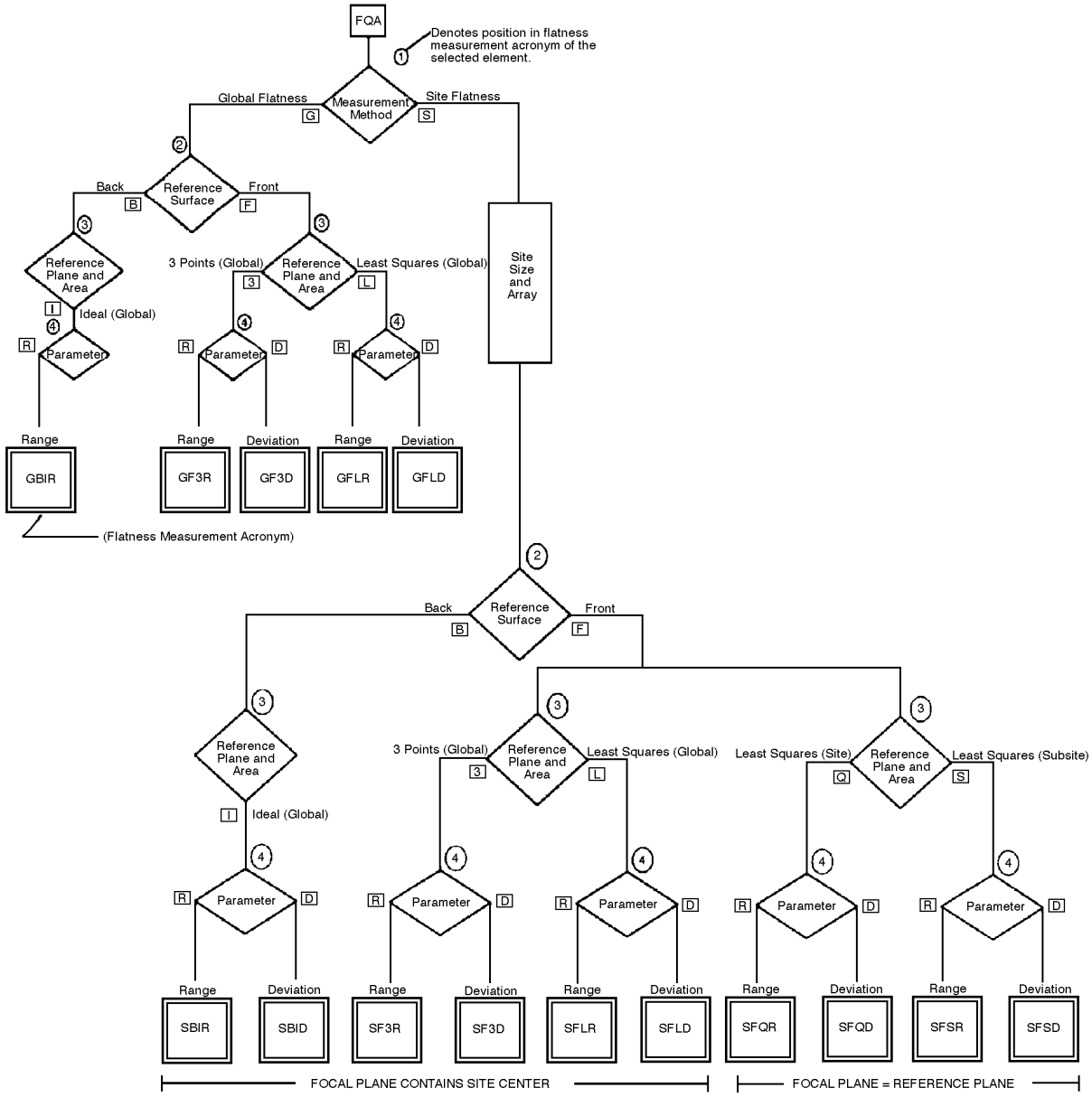


Figure A1-1
Flatness Decision Tree

A1-2.5.2 For site flatness measurements, any of the above three planes [(1), (3), or (L)] may be suitable or, if the wafer is regimballed once at each site, a site least squares reference plane (Q) may be appropriate or, if the wafer is regimballed more than once at each site, a subsite least squares reference plane (S) may be appropriate.

A1-2.6 *Step 5* — Choose the Measurement Parameter: Choose either TIR, also known as range (R), or FPD, also known as deviation (D). In the case of site measurements, it is possible to specify the maximum value of (R) or (D) or the percentage of the sites (or FQA) which have an (R) or (D) less than some specified value.

A1-2.7 The codes in parentheses in Steps 2 through 5 may be used to form a code which uniquely defines the measurement technique as follows:

- Position 1: Measurement Method (G) or (S),
- Position 2: Reference Surface (F) or (B),

- Position 3: Reference Plane and Area (I), (3), (L), (Q), or (S), and
- Position 4: Measurement Parameter (R) or (D).

A1-2.7.1 Stating this code, the numerical values for the FQA parameters (and, if required, information on site size and array), and the numerical limit for the measurement parameter provides enough information to describe the measurement and provide numerical limits.

A1-3 Future Developments

A1-3.1 As noted above, there may be specific systems which are not exactly described by one of the branch ends on this decision tree. This tree is an approximation of the more complete one which would describe all existing and possible lithographic technologies.

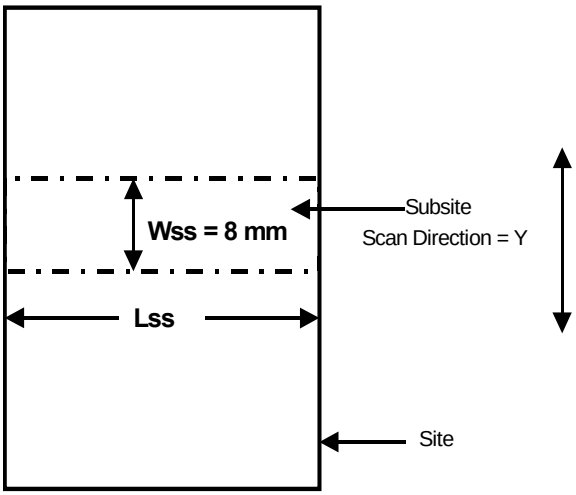


Figure A1-2
Scanner Site and Subsite Flatness Elements

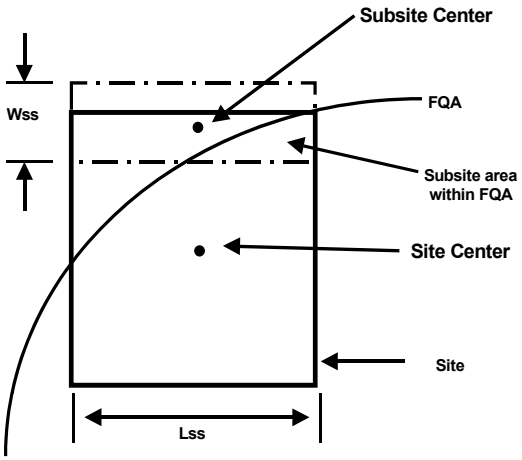


Figure A1-3
Subsite Center near Boundaries of Site and FQA

APPENDIX 2
SHAPE DECISION TREE

NOTICE: The material in this appendix is an official part of M1. Approval was by full letter ballot procedures with publication authorized by the NA Regional Standards Committee on October 21, 1999.

A2-1 Scope

A2-1.1 In modern wafer fabrication processes, wafer surface geometry in the unclamped state can be a sensitive indicator of process effects. Larger wafer diameters and increasing complexity of processes and circuits have increased the need for accurate, standardized measurement of unclamped wafer geometry. The quantities that have historically been used, Bow and Back Surface Referenced Warp, may be inadequate to describe and quantify the geometries of interest in advanced processes. Additional surface geometry quantities, such as Sori and Median Surface Referenced Warp, have been introduced into standards.

A2-1.2 In addition, there is considerable confusion as to the precise meaning of these quantities, even though they are defined in the applicable SEMI test methods.

A2-1.3 The Shape Decision Tree was developed to provide an orderly method of identifying each of the variables involved in the quantities used to quantify unclamped wafer surface geometry. As such, the tree provides a concise and precise description of each shape quantity. A branch of the tree consists of a selection of one of the choices for each variable. The variables and the choices for each are listed in Table A1-1.

A2-1.4 Four branches of the tree, representing quantities for which measurement methods have been standardized by SEMI, are depicted in Figure A1-1. There are many other branches of the tree, not all of which may represent practical combinations of variables.

A2-2 Use of the Shape Decision Tree

A2-2.1 Step 1. Select the Fixed Quality Area (FQA): Decide on and specify the nominal edge exclusion, *EE*, which defines the FQA. (See Figure 1.)

A2-2.2 Step 2. Select the measurement method: global (over the entire fixed quality area) or local (over a site).

NOTE 1: At present, all shape quantities in common use are global measurements. The significance and use of local shape quantities have yet to be defined.

A2-2.3 Step 3. Select the reference surface: front, median, or back, to be used to establish the reference plane.

A2-2.4 Step 4. Select the kind of reference plane: least-squares or 3-point.

NOTE 2: A measurement made with a least-squares reference plane is less affected by small changes in wafer position within the measurement apparatus than is a measurement made with a 3-point reference plane.

A2-2.5 Step 5. Determine whether the effects of gravitational sag on the wafer are accounted for (yes) or not (no).

NOTE 3: Gravitational effects may be accounted for by inverting the wafer during the measurement, by placing the wafer in a vertical or nearly vertical position during the measurement, or mathematically.

A2-2.6 Step 6. Select the measurement surface: front, median, or back, for which the deviations are to be measured.

A2-2.7 Step 7. Select the measurement pattern: full scan (a regular array of measurement points over the entire measurement area), partial scan (a specified pattern of measurement points covering only a portion of the measurement area), or centerpoint (measurement at the center of the wafer only).

A2-2.8 Step 8. Select the parameter to be determined: range (TIR) or maximum RPD.

A2-2.9 Step 9. Compare the branch thus obtained with the branches in Figure A2-1. If the branch obtained matches one of the branches illustrated in Figure A1-1, the resulting quantity is given by the code shown in the box at the bottom of the branch. Standard test methods have been adopted for measurement of each of these quantities. If the branch obtained does not match any of the branches illustrated in Figure A2-1, the quantity obtained has not been given a standardized term, nor has a standard test method been adopted for its measurement.

A2-2.9.1 These codes, which uniquely describe the various branches, are formed from the codes in Table A2-1. Stating this code together with the numerical value for the FQA nominal edge exclusion provides enough information to describe the shape parameter and to establish numerical limits for it.

A2-2.9.2 Table A2-2 summarizes the shape parameters for which SEMI has standardized test methods. This table lists the code, the term in common use for the parameter, the SEMI test method, and the expanded form of the code.

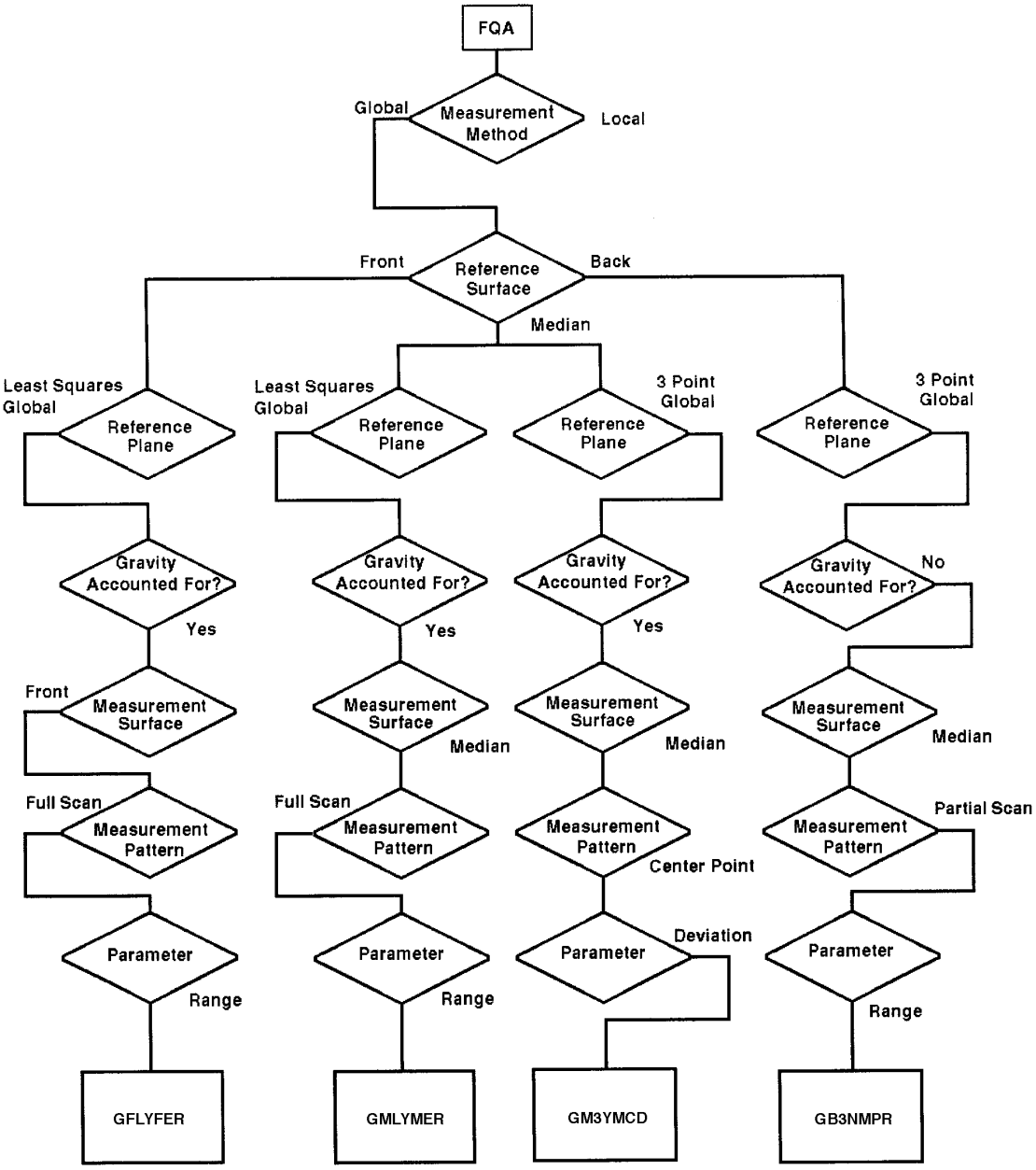


Figure A2-1
Four Branches of the Shape Decision Tree

Table A2-1 Variables in Shape Quantities

Variable	*Options*	*Code*
Measurement Method	Global	G
	Local (Site)	S
Reference Surface	Front	F
	Median	M
	Back	B
Reference Plane	Least-Square	L
	3-Point	3
Corrected for Gravitational Sag	Yes	Y
	No	N
Measurement Surface	Front	F
	Median	M
	Back	B
Measurement Pattern	Full Scan (Entire)	E
	Partial Scan	P
	Centerpoint	C
Parameter	Range (TIR)	R
	Maximum RPD	D

Table A2-2 Shape Code Summary

Code	*Term*	*Test Method*	*Expanded Form of Code*
GFLYFER	sori	SEMI MF1451	Global, Front-surface Least-squares reference plane, Yes (corrected for gravitational sag), Front-surface measurement, Entire surface scanned, Range
GMLYMER	warp	SEMI MF1390	Global, Median-surface Least-squares reference plane, Yes (corrected for gravitational sag), Median-surface measurement, Entire surface scanned, Range
GM3YMCD	bow	SEMI MF534	Global, Median-surface 3-point plane, Yes (corrected for gravitational sag), Median-surface measurement at Center point, Deviation
GB3NMPR	warp	SEMI MF657	Global, Back-surface 3-point reference plane, No (not corrected for gravitational sag), Median-surface measurement, Partial surface scanned, Range

RELATED INFORMATION 1
SURFACE METAL CONTAMINATION

NOTICE: This related information is not an official part of SEMI M1 and is not intended to modify or supersede the official standard. Approval was by full letter ballot procedures with publication authorized by the NA Regional Standards Committee beginning with the 1995 edition of the standard. Determination of the suitability of the material is solely the responsibility of the user.

R1-1 Scope

R1-1.1 Maximum allowable surface metal contamination levels for wafers to be used in integrated circuit (IC) fabrication generally depend upon the IC device density and upon the IC process design. In general, as the device density increases, the allowable surface metal contamination levels become lower.

R1-1.2 This related information is intended to provide guidance regarding allowable surface concentrations of metal contaminants that have been reported to be deleterious to circuit and device performance.

R1-2 Suggested Allowable Surface Metal Contamination Levels for 1 µm Geometries

R1-2.1 Table R1-1 lists suggested surface metal limits for circuits and devices with a minimum linewidth in the range of 0.8 µm to 1.2 µm for two alkali metals (Na, K), a light metal (Al), and five heavy metals (Cr, Fe, Ni, Cu, Zn). These are same elements as are listed in the items under Section 2-7 of Table 1, Part 2, and they are listed in the same order as they appear in that table.

Contaminant levels in Table R1-1 are significantly higher than would be allowed for leading edge technologies at the time of approval of this standard.

Table R1-1 Suggested Polished Wafer Surface Metal Contamination Limits Appropriate to Circuits and Devices with a Minimum Linewidth in the Range 0.8 µm to 1.2 µm

Element	*Contaminant Level*
Sodium (Na)	Not greater than 1×10^{11} atoms/cm^2
Aluminum (Al)	Not greater than 1×10^{11} atoms/cm^2
Potassium (K)	Not greater than 1×10^{11} atoms/cm^2
Chromium (Cr)	Not greater than 1×10^{11} atoms/cm^2
Iron (Fe)	Not greater than 1×10^{11} atoms/cm^2
Nickel (Ni)	Not greater than 1×10^{11} atoms/cm^2
Copper (Cu)	Not greater than 1×10^{11} atoms/cm^2
Zinc (Zn)	Not greater than 1×10^{12} atoms/cm^2

R1-3 Test Methods

R1-3.1 The test methods suitable for use in determining the levels of each surface metal contaminant are listed in the items under Section 2-7 of Table 1, Part 2. This list and the related discussion of these test methods in Related Information 2 should be referenced in selecting methods appropriate for testing the individual surface metals.

RELATED INFORMATION 2
TEST METHODS

NOTICE: This related information is not an official part of SEMI M1 and is not intended to modify or supersede the official standard. This information was developed during the revision of this standard in 2004. It is based in part on information previously published as part of SEMI M28, withdrawn in October 2000. Approval was by full letter ballot procedures with publication authorized by the NA Regional Standards Committee on November 4, 2004. Determination of the suitability of the material is solely the responsibility of the user.

R2-1 Scope

R2-1.1 This Related Information Section discusses aspects of the various test methods listed in Table 1 together with additional information about other test methods that are not listed in Table 1 but either have been or still are used in the industry.

R2-1.2 The next section contains references to the test methods that are not cited in the main body of SEMI M1 but that are discussed here. The various test methods are discussed in order that the items they cover are listed in Table 1.

R2-1.3 Note that silicon wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must, therefore, be used in the selection and execution of measurement methods.

NOTICE: This section does not purport to address safety issues, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

R2-2 Referenced Standards

R2-2.1 The standards listed in this section are referenced only in this related information. See Section 4 for other standards that are referenced in this related information.

R2-2.2 *SEMI Standards*

SEMI M49 — Guide for Specifying Geometry Measurement Equipment for Silicon Wafers for the 130 nm Technology Generation

SEMI M50 — Test Method for Determining Capture Rate and False Count Rate for Surface Scanning Inspection Systems by the Overlay Method

SEMI M52 — Guide for Specifying Scanning Surface Inspection Systems for Silicon Wafers for the 130 nm Technology Generation

SEMI MF43 — Test Methods for Resistivity of Semiconductor Materials

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wavenumber or Wavelength of the Plasma Resonance Minimum

SEMI MF723 — Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped, Phosphorus-Doped, and Arsenic-Doped Silicon.

SEMI MF1527 — Guide for Application of Silicon Certified Reference Materials and Reference Wafers for Calibration and Control of Instruments for Measuring Resistivity of Silicon

SEMI MF1529 — Test Method for Sheet Resistance Uniformity Evaluation by In-Line Four-Point Probe with the Dual-Configuration Procedure

SEMI MF1618 — Practice for Determination of Uniformity of Thin Films on Silicon Wafers

SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Structural Defects on Silicon Wafers

R2-2.3 *JEITA* (*formerly JEIDA*) *Standard*[2]

EM-3505 — Height Calibration in 1 nm Order for AFM

R2-2.4 *DIN Standards*[4]

50430 — Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals in Bars by Means of the Two-point-probe Direct Current Method

50444 — Conversion Between Resistivity and Dopant Density; Silicon

R2-2.5 *ANSI Standard*[5]

ANSI/ASME B46.1 — Surface Texture (Surface Roughness, Waviness, and Lay)

R2-2.6 *ISO Standards*[6]

ISO 4287/1 — Surface Roughness – Terminology – Part 1: Surface and its Parameters

ISO 14644/1 — Clean Room and Associated Controlled Environments — Classification of Air Cleanliness

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

R2-3 General Characteristics

R2-3.1 *Crystal Orientation*—The crystallographic orientation of the source crystal can be determined by the x-ray methods of SEMI MF26, JEITA EM-3501, or DIN 50433/1, the optical method of SEMI MF26 or DIN 50433/2, or the Laue method of DIN 50433/3. X-ray methods are most commonly used by wafer suppliers. {Need some discussion here about differences between MF26 and EM-3501}}

R2-3.2 *Conductivity Type*—One of the five methods of SEMI MF42, one of the methods of JIS H 0607, or one of the four methods of DIN 50432 should be used to determine conductivity type. This quantity is generally well controlled by silicon wafer suppliers and is not usually verified on incoming.

R2-3.3 Many of these tests need to be carried out in cleanroom environments of ISO Class 4, 5, or 6 depending on the cleanliness requirements. These classes are defined in ISO 14664-1.

R2-4 Electrical Characteristics

R2-4.1 *Resistivity* of wafers is most appropriately determined for referee purposes by SEMI MF84 or DIN 50431. Under some circumstances these tests may be considered destructive, and an alternative means may be required. One nondestructive test is SEMI MF673, having a range from 0.0001 to 100 Ω·cm. Another nondestructive test is SEMI MF398, which is limited to carrier concentrations in the ranges from 1.5×10^{18} to 1.5×10^{21} cm^{-3} for *n*-type silicon and from 3×10^{18} to 5×10^{20} cm^{-3} for *p*-type silicon, and has only moderate inter-laboratory precision. Other older methods that require a bar-shaped test specimen include SEMI MF43 and DIN 50430; these methods are no longer in general use. It is also possible to establish the dopant density from room temperature measurements in silicon using SEMI MF723 (for boron, phosphorus, or arsenic doped silicon) or DIN 50444 (for boron and phosphorus doped silicon only). SEMI MF1527 is a useful standard in describing ways of ensuring that resistivity measuring instruments are performing correctly.

R2-4.2 *Radial Resistivity Variation* is generally determined by SEMI MF81 or DIN 50435. These test methods use several different measurement positions so the desired position must be specified. It is also possible to measure the resistivity in one of the circular patterns specified in SEMI MF1618 using SEMI MF1529 as the resistivity measurement method.

R2-4.3 *Resistivity Striations* can generally be viewed visually using one of the techniques discussed in Section R2-9. For an electrical measurement, spreading resistance (SEMI MF525) is generally employed but this is strictly an off-line measurement.

R2-4.4 *Minority Carrier Lifetime* can be measured by a number of methods. The photoconductive decay methods (SEMI MF28, JIS H 0604, and DIN 50440/1 all require the use of special test specimens; Microwave reflectivity measurements (SEMI MF1535 and JEITA EM-3502) are applicable to measurements on wafers, but special surface passivation procedures may be required to obtain meaningful results. Minority carrier lifetime may also be inferred from measurements made in accordance with SEMI MF1388, which yields generation lifetime if the measurements

are made at room temperature and recombination lifetime if they are made at elevated temperature (50° to 75°C). The test specimens required for this test method can be made by procedures compatible with typical wafer processing.

R2-5 Chemical Characteristics

R2-5.1 *Oxygen Concentration* in relatively high resistivity specimens (ρ > 1 to 3 Ω·cm at room temperature) should be measured by infrared techniques. SEMI MF1188, JEITA EM-3504, and DIN 50438 all utilize approximately normal incidence illumination and the IOC-88 calibration factor to determine the interstitial oxygen content. See SEMI M44 for a discussion of other calibration factors and their relationship to IOC-88. SEMI MF1619 uses *p*-polarized radiation, incident at the Brewster angle to reduce the multiple reflections from polished wafers. For more heavily doped wafers, secondary ion mass spectrometry (SIMS, SEMI MF1366) and gas fusion analysis (GFA) can be used to determine total oxygen content. There is no standardized method for performing GFA, and the repeatability of this technique is generally poorer than SIMS.

R2-5.2 *Radial Oxygen Variation* should be determined by measuring the oxygen content by one of the above methods at selected locations on the wafer defined in SEMI MF951. Usually measurements are made at the center and at a single point on the primary flat or notch bisector 10 mm from the edge of the wafer opposite the fiducial; this is known as test plan A-1.

R2-5.3 *Carbon Concentration* should be measured by SEMI MF1391, JEITA 56, and DIN 50438/2. The most modern calibration coefficients are used in SEMI MF1391 and JEITA 56. For these methods, the test specimen cannot be too heavily doped, and special thick test specimens may be necessary.

R2-5.4 *Boron Contamination* in heavily doped *n*-type silicon can be determined by SEMI MF1528.

R2-6 Structural Characteristics

R2-6.1 *Dislocation Etch Pit Density, Slip, Lineage, Twins, and Swirl* are usually displayed by etching and visual or microscopic observation. JIS H 0609 is a comprehensive test method for carrying out this procedure with the use of non-chromic etchants. SEMI MF1809 also recommends non-chromic etchants for this test. For the full procedure, SEMI MF1809 must be used with other standards including SEMI MF1726 and SEMI MF1810. DIN 50434 is an older, but comprehensive test procedure to observe these and other structural defects based on chrome-containing etchants. It is also possible to observe these defects by x-ray topography using DIN 50443/1.

R2-6.2 *Shallow Pits* can be exposed by the relatively low temperature heating cycle and procedures in SEMI MF1049 if they are present in sufficient density, but testing for shallow pits in production environments is usually carried out using the temperature cycle in SEMI MF1727 followed by etching with etchants discussed in SEMI MF1809, examination by SEMI MF1726, and counting by SEMI MF1810. They can also be observed by using JIS H 0609.

R2-6.3 *Oxidation Induced Stacking Faults* (*OISF*) can be observed by using JIS H 0609, or by using the temperature cycle in SEMI MF1727 followed by etching with etchants discussed in SEMI MF1809, examination by SEMI MF1726, and counting by SEMI MF1810. OISF can also be observed by x-ray topography using DIN 50443/1 following thermal treatment according to JIS H 0609 or SEMI MF1727.

R2-6.4 *Oxide Precipitates* (*Bulk Micro Defects*, *BMD*) are generated with the use of a temperature cycle such as those in SEMI MF1239. The amount of precipitation can be measured by the oxygen reduction method of SEMI MF1239 or by direct observation by infrared that has not yet been standardized.

R2-6.5 *Bulk Defects* can be detected by x-ray topography in accordance with DIN 50443/1.

R2.7 Dimensional Characteristics

R2-7.1 *Diameter* is presently very well controlled in silicon wafers that have been edge profiled with cam follower equipment. For three-point measurements at locations defined by SEMI MF2074 and, except for positions on 150 mm diameter, *n*-type (100) wafers, by DIN 50441/4. The latter utilizes a measuring or projection microscope to make the diameter measurements, but the former allows a dial gauge or any other equally accurate method of dimensional measurement.

R2-7.2 *Flat Length* should be determined by SEMI MF671. If flat diameter is specified instead of flat length, it can be determined by ¶6.2.1 of DIN 50441/4 or by a dial gauge method as agreed upon between the supplier and customer. Both SEMI MF671 and DIN 50441/4 take account of the possibility that the ends of the flat might be rounded.

R2-7.3 *Notch Dimensions* should be determined by SEMI MF1152 (see Figure 5).

R2-7.4 *Flat Orientation* can be confirmed by SEMI MF847. There is no standardized method for determining the crystallographic orientation of the diameter that bisects the notch.

R2-7.5 *Edge Profile* is usually determined by using one of the two templates (see Figure 6) with Method B of SEMI MF928 or Procedure 2 of DIN 50441/2, both of which are nondestructive. The other two procedures in these methods are destructive and not so widely used.

R2-7.6 *Thickness* is usually determined at the center point of the wafer with the use of SEMI MF1530, an automated technique. Manual techniques originally used in the industry include SEMI MF533, JIS H 0611, and DIN 50441/1.

NOTE 2: Test methods SEMI MF1530 (for thickness, thickness variation, and flatness), SEMI MF1451 (for sori), and SEMI MF1390 (for warp) may not be suitable for use on large diameter wafers with polished back surfaces. New standardized test methods for measuring these parameters on such wafers are under development.

R2-7.7 *Total Thickness Variation* (*TTV*) was originally determined with the use of manual 5-point techniques covered in SEMI MF533, JIS H 0611, and DIN 50441/1. JIS H 0611 differs from SEMI MF533 and DIN 50441/1, in that the measurements in JIS H 0611 are taken at the center and at 5 mm from the edge on diameters parallel and perpendicular to the primary flat or notch bisector, while the measurements in SEMI MF533 and DIN 50441/1 are taken at the center and at 6 mm from the edge on diameters 30 degrees and 120 degrees counterclockwise from the bisector to the primary flat or notch (with the wafer facing front surface up). TTV can also be determined with the use of SEMI MF657, which involves a continuous scan pattern over a portion of the wafer surface. Currently, however, it is most frequently determined using SEMI MF1530, which involves an automated continuous scan pattern over the entire wafer surface. In this case, the quantity determined is equal to the global flatness GBIR (see Appendix 1 and Note 1, above).

R2-7.8 *Surface Orientation* can be determined by the x-ray methods of SEMI MF26, JEITA EM-3501, or DIN 50433/1, the optical method of SEMI MF26 or DIN 50433/2, or the Laue method of DIN 50433/3.

R2-7.9 For off-orientation {111} wafers, the orthogonal misorientation is specified for each of the wafer categories in Tables 4 through 9. There is no standardized measurement method for this property so it should be determined by a method agreed upon between supplier and customer.

R2-7.10 *Bow* can be determined with the manual methods SEMI MF534 and JIS H 0611. Currently, bow is not as widely used a parameter as warp.

R2-7.11 *Warp* is currently most often measured with the use of SEMI MF1390, which is an automated method with full surface scan and correction for gravitational sag. It can also be measured with the use of the contactless manual method SEMI MF657, in which the prescribed scan pattern covers only a portion of the wafer surface in which there is no correction for gravitational sag. As noted in Appendix 2, different reference planes are used for the two methods. Because SEMI MF657 employs a back surface reference plane, the measured warp may include contributions from thickness variation of the wafer. SEMI MF1390 employs a median surface reference plane and is not susceptible to interferences from thickness variations. In general, the latter is preferred, especially for wafers 150 mm in diameter and larger (see Note 1, above).

R2-7.12 *Sori* , which is sometimes specified in lieu of bow or warp or both, can be determined by SEMI MF1451 (see Note 1, above).

R2-7.13 *Global Flatness* can be determined by either capacitance measurements, as in SEMI MF1530, or by multiple beam interference, as in DIN 50441/3. Generally, the former is considered to be more reliable, especially as the need increases for measuring smaller flatness deviation (see Note 1, above). As noted in ¶R2-7.7, GBIR is the same as TTV; other global flatness parameters are discussed in Appendix 1.

R2-7.14 *Site Flatness* is generally determined by SEMI MF1530 (see Note 1, above). The most commonly used site flatness parameter is SFQR; other site flatness parameters are discussed in Appendix 1. Although it is not widely used, the scanning site flatness parameter SFSR was recently introduced. For this parameter, use a subsite width, Wss, equal to 8 mm and orient the wafer so the effective scan direction is along the wafer's *y*-axis as defined in SEMI M20.

R2-7.14.1 SEMI M49 is a guide for specifying test equipment for use in determining thickness, shape, and flatness parameters on wafers intended to be used to fabricate advanced integrated circuits.

R2-7.15 *Nanotopography* should be determined by SEMI M43. This guide gives a variety of options that can be used, so it is essential to specify the various conditions that are desired in any given case. The conditions chosen should be agreed upon between supplier and customer.

R2-8 Front Surface Chemistry

R2-8.1 *Surface Metal Contaminants*

R2-8.1.1 Sodium, aluminum, potassium, and iron can be measured by secondary ion mass spectrometry (SIMS), inductively coupled plasma mass spectrometry (ICP/MS), or atomic absorption spectroscopy (AAS). SIMS has been standardized as SEMI MF1617. The latter two methods are frequently combined with vapor phase decomposition (VPD), but they have not yet been standardized.

R2-8.1.2 Potassium, chromium, iron, nickel, copper, and zinc can be measured by Total Reflection X-Ray Fluorescence Spectroscopy (TXRF), ICP/MS, and AAS. TXRF has been standardized both with (SEMI M33 and ISO 17706) and without (ISO 14706) use of VPD to preconcentrate the surface metal contaminants.

R2-8.1.2.1 VPD is chemical preconcentration of the surface metals using vapor phase HF to decompose the surface native oxide and a water (or acid-spiked water) droplet to scan across the wafer dissolving the surface metals. The recovery rate of this preconcentration method is dependent upon the chemistry of the surface metals and upon the chemistry used for the preconcentration. An alternative preconcentration method to VPD is to scan an acid droplet across the wafer surface.

R2-8.1.2.2 VPD/AAS is a single-element technique which is widely used in Japan. It is element-specific and very sensitive. VPD/ICP-MS is a rapid multi-element technique which is a more recent development. It is also very sensitive, but its reproducibility is dependent upon the injection process into the ICP-MS. VPD/TXRF is an even more recently developed multi-element technique. It is also very sensitive, but its reproducibility is dependent on the residue-drying process.

R2-8.2 *Surface Organics* can be measured by SEMI MF1982. This standard describes two methods; the method to be utilized should be agreed upon between supplier and customer.

R2-9 Surface Inspection Characteristics

R2-9.1 *Visual Inspection* of either the front or back surface of wafers can be carried out in accordance with SEMI MF523 or JIS H 0614. The following conditions should be used for examination under high intensity illumination:

- Background light intensity: 8 ± 2 fc (86 ± 22 lux),
- Angle (alpha): 45° ± 10°, and
- Angle (beta): 90° ± 10°.

See ¶6.8 for a discussion of which artifacts on the surface should be considered as defects. SEMI MF154 is a useful guide for identifying structures and contaminants seen on silicon surfaces.

R2-9.1.1 *Scratches*—In inspecting for scratches, it is important to note that while macro-scratches can be seen under both high intensity and diffuse illumination, micro-scratches can be seen only under high intensity illumination. Therefore, to separate the two kinds of scratches, it is necessary to count the scratches observed under both kinds of illumination. The count of scratches seen under diffuse illumination is the number of macro-scratches while the difference of the counts seen under high intensity illumination and diffuse illumination is the number of micro-scratches. Of course, if the total requirement is for no scratches of either kind, then examination under high intensity illumination only is adequate.

R2-9.2 *X-ray Topography* (DIN 50443/1) can also be used to test for defects in silicon wafers. This method may see defects that do not intersect the surface, and can also be used to examine for bulk defects in the wafer (see Section 2.4.10 of Table 1).

R2-9.3 *Automated Surface Inspection by Light Scattering* can also be used to detect many surface defects, especially on polished surfaces. These techniques have not been fully standardized but there is a group of standards that assist in making certain that the instruments are performing correctly. These include SEMI M52 for determining if surface scanning inspection systems (SSIS) have suitable characteristics for the desired use, SEMI M53 for calibrating SSISs, SEMI M58 for assuring that the calibration artifacts meet the desired requirements, SEMI M50 for determining capture rate characteristics of SSISs and SEMI M35 for discriminating among various surface features with an SSIS. Because of the lack of complete standardization, the testing conditions for use of SSISs should be agreed upon between supplier and customer.

R2-9.3.1 *Localized Light Scatterers* — SSISs are particularly appropriate for inspecting polished surfaces for the presence of particles and other localized light scatterers (LLS). In this case, it is essential to define the size ranges (in units of latex sphere equivalents, LSE) as well as the maximum permissible counts, usually in terms of counts per wafer, but occasionally in terms of counts per unit area.

R2-9.4 *Surface Roughness* affects the size of particle or other LLS that can be detected on a surface. SEMI M40 provides guidance on how to measure and report surface roughness on planar surfaces. Surface microroughness can be determined with SSISs, through the use of the power spectral density as described in SEMI MF1811, or with an atomic force microscope, which can be calibrated with the use of JEITA EM-3505. Other documents useful in connection with surface microroughness measurements include ISO 4287/1 and ANSI/ASME B46.1. Because of the lack of standardization, the testing conditions for surface microroughness measurements should be agreed upon between supplier and customer.

R2-9.5 *Back Surface Finish* of 300 mm diameter wafers is specified as “polished.” The standard quantitative test for the polish finish, which is not a smooth as the mirror polished front surface, is gloss. The general techniques for determining gloss are given in ASTM Test Method D 523 and JIS Z 8741. However, for measuring gloss of silicon surfaces, visible illumination at a 60° angle of incidence is referenced to a mirror polished silicon front surface. Surface microroughness measurements (see ¶R2-9.4) can also be used as a quantitative test for back surface finish, especially when it is necessary to observe particles or other LLSs smaller than 0.25 μm LSE on the surface.

REVISION RECORD

NOTICE: The Revision Record is an official part of the standard. It is optional and placed at the end of the standard. Negative votes may not be based on the Revision Record.

<table>
<tr><th>Cycle</th><th>Ballot</th><th>Section</th><th>Description</th><th>Committee Approval</th></tr>
<tr><td>0305</td><td>3907</td><td>Entire Document</td><td>This revision combines most of SEMI M1 with parts of SEMI M18 to form a new set of specifications that includes:
Purpose, a new scope, referenced standards, ordering information (consolidated with some of SEMI M18), requirements (assembled from several existing sections in SEMI M1), sampling, test methods, certification, and packing and shipping container labeling sections;
Basic polished wafer specifications (developed by the Basic Wafer Specification TF);
The two appendices and one related information section included in previous editions of SEMI M1; and
A new related information section on detailed discussion of test methods, based largely on material previously in SEMI M28.
A new table of contents has been added to make it easier to locate specific information in the standard, and the terminology section of SEMI M1 was combined with SEMI MF1241 and issued as SEMI M59. The EDI codes from SEMI M18 remain in that standard.
The material in all of the substandards previously included at the end of SEMI M1 is now included in the body of the document with no change of the technical content. In addition, polished wafers and substrates have been assigned category numbers based on the previous substandard designation number. In some cases there are two categories, based on differences in the edge rounding template used. All of the specification requirements previously in the substandards have been moved to tables as follows:
<table>
<tr><th>Substandard</th><th>Nominal Diameter</th><th>Located in Table</th><th>Wafer Category(s)</th></tr>
<tr><td>SEMI M1.1</td><td>2 inch</td><td>4</td><td>1.1</td></tr>
<tr><td>SEMI M1.2</td><td>3 inch</td><td>4</td><td>1.2</td></tr>
<tr><td>SEMI M1.5</td><td>100 mm</td><td>5</td><td>1.5</td></tr>
<tr><td>SEMI M1.6</td><td>100 mm</td><td>5</td><td>1.6</td></tr>
<tr><td>SEMI M1.7</td><td>125 mm</td><td>5</td><td>1.7</td></tr>
<tr><td>SEMI M1.8</td><td>150 mm</td><td>6</td><td>1.8.1 and 1.8.2</td></tr>
<tr><td>SEMI M1.9</td><td>200 mm</td><td>9</td><td>1.9.1 and 1.9.2</td></tr>
<tr><td>SEMI M1.10</td><td>200 mm</td><td>8</td><td>1.10.1 and 1.10.2</td></tr>
<tr><td>SEMI M1.11</td><td>100 mm</td><td>7</td><td>1.11</td></tr>
<tr><td>SEMI M1.12</td><td>125 mm</td><td>7</td><td>1.12</td></tr>
<tr><td>SEMI M1.13</td><td>150 mm</td><td>8</td><td>1.13.1 and 1.13.2</td></tr>
<tr><td>SEMI M1.15</td><td>300 mm</td><td>9</td><td>1.15</td></tr>
</table>
Additional material related to 300 mm wafers is given elsewhere in SEMI M1, most notably in ¶6.5.1.4, which describes the wafer marking requirements. Also it should be noted that (1) the information on surface orientation, for which the substandards allowed any of a number of options, has been moved to Item 2-1.8 of Table 1, Silicon Wafer Specification Format for Order Entry, Parts 1 and 2, and (2) the information on orthogonal misorientation, which is the same for all (111) silicon wafers has been moved to Item 2-1.9 of the same table.</td><td></td></tr>
</table>

SEMI M2-1103
SPECIFICATION FOR SILICON EPITAXIAL WAFERS FOR DISCRETE DEVICE APPLICATIONS

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on July 12, 2003. Initially available at www.semi.org October 2003; to be published November 2003. Originally published in 1985; previously published September 1997.

1 Purpose

1.1 This specification defines silicon epitaxial wafer requirements for discrete semiconductor device manufacture. It is restricted to wafers with device feature sizes in excess of 1 µm or wafers with epi layers thicker than 25 µm. By defining inspection procedures and acceptance criteria, suppliers and consumers may uniformly define product characteristics and quality requirements.

2 Scope

2.1 This specification covers characteristics of both the substrate (through reference to SEMI M1) and the epitaxial layer including handling and packaging.

2.2 This specification is specifically directed to silicon homoepitaxial deposits thicker than 25 µm on homogeneous silicon substrates or similar epitaxial wafers that are to be used to make discrete devices. Specifications for silicon epitaxial wafers with greater uniformity and more stringent surface defect criteria are given in SEMI M11.

2.3 The primary standardized properties set forth in this specification relate to physical, electrical, and surface defect parameters.

2.4 A complete purchase specification requires that additional physical properties be specified along with suitable test methods for their measurement. SEMI M18 may be used for this purpose.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI M11 — Specifications for Silicon Epitaxial Wafers for Integrated Circuit (IC) Applications

SEMI M17 — Specification for a Universal Wafer Grid

SEMI M18 — Format for Silicon Wafer Specification Form for Order Entry

SEMI MF95 — Test Method for Thickness of Epitaxial Layers of Silicon on Substrates of the Same Type by Infrared Reflectance

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, and Ion-Implanted Layers Using an Inline Four-Point Probe with the Single Configuration

SEMI MF398 — Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wavelength of the Plasma Resonance Minimum

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Slices

SEMI MF525 — Test Method for Measuring Resistivity of Silicon Wafers Using a Spreading Resistance Probe

SEMI MF672 — Test Method for Measuring Resistivity Profiles Perpendicular to the Surface of a Silicon Wafer Using a Spreading Resistance Probe

SEMI MF723 — Practice for Conversion between Resistivity and Dopant Density for Boron-Doped and Phosphorus-Doped Silicon

SEMI MF1241 — Terminology of Silicon Technology

SEMI MF1392 — Test Method for Determining Net Carrier Density Profiles in Silicon Wafer by Capacitance-Voltage Measurements with a Mercury Probe

SEMI MF1393 — Test Method for Determining Net Carrier Density in Silicon Wafers by Miller Feedback Profiler Measurements with a Mercury Probe

SEMI MF1726 — Guide for Analysis of Crystallographic Perfection of Silicon Wafers

3.2 *Other Standards*[1]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 Many terms relating to silicon technology are defined in SEMI MF1241.

4.2 Descriptions of other epitaxial wafer defects covered in Table 1 are given in SEMI MF154.

4.3 Other terms are defined as follows:

4.3.1 *autodoping, of an epitaxial layer* — incorporation of dopant originating from the substrate into the epitaxial layer. Also called *self-doping*.

NOTE 1: Sources of autodoping can be the back and front surfaces and edges of the substrate, other substrates in the reactor, the susceptor, or other parts of the deposition assembly.

4.3.2 *chemical vapor deposition, in semiconductor technology* — a process in which a controlled chemical reaction produces a thin surface film.

NOTE 2: Epitaxial growth is an example of a special case of chemical vapor deposition (CVD).

4.3.3 *edge crown* — the difference between the surface elevation 1/8 inch (3.2 mm) from the edge of the wafer and the elevation at the wafer edge.

4.3.4 *effective layer thickness, of an epitaxial layer* — the depth from the front surface in which the net carrier density is within the specified limits.

4.3.5 *epi profile slope, of an epitaxial layer* — the difference between the net carrier density at 0.75 of the layer thickness and the net carrier density at 0.25 of the layer thickness divided by one-half the layer thickness:

$$\text{epi profile slope} = \frac{N_{0.75t} - N_{0.25t}}{0.5t} \quad (1)$$

where:
N = net carrier density, cm^{-3}, and
t = layer thickness, μm.

4.3.6 *epitaxial layer* — a layer of single crystal semiconductor material grown on a host substrate that determines its orientation.

4.3.7 *epitaxy* — The growth of a single crystal layer on a substrate of the same material, homoepitaxy; or on a substrate of different material with a compatible crystal structure, heteroepitaxy.

4.3.8 *flat zone, of an epitaxial layer* — The depth from the front surface to the point where the net carrier density is 20% greater than or less than the average net carrier density (see Section 8.3.2) of the region between 0.25 and 0.75 of the layer thickness.

4.3.9 *thickness, of an epitaxial layer* — The distance from the surface of the wafer to the layer-substrate interface.

4.3.10 *transition width, of an epitaxial layer deposited on a more heavily doped substrate of the same conductivity type* — The difference between the layer thickness as determined by infrared reflectance (see Section 8.3.1) and the flat zone based on the same thickness measurement.

5 Ordering Information

5.1 Purchase orders for the epitaxial layer on substrates furnished to this specification shall include the following items:

5.1.1 Substrate characteristics,

5.1.2 Silicon source (if required) (see Note 3),

5.1.3 Conductivity type and doping source (see Note 3),

5.1.4 Etch removal (if required),

5.1.5 Center-point thickness and thickness tolerances,

5.1.6 Radial thickness variation range,

5.1.7 Center-point net carrier density and net carrier density tolerances (or resistivity and resistivity tolerances) (see Note 4),

5.1.8 Radial net carrier density (or resistivity) variation range (see Note 4),

5.1.9 Epitaxial wafer defect limits,

5.1.10 Methods of test and measurements (see Section 8),

5.1.11 Lot acceptance procedures (see Section 7),

5.1.12 Certification (if required) (see Section 9), and

5.1.13 Packing and marking (see Section 10).

NOTE 3: The dopant, doping method, and growth method are difficult to ascertain in the finished wafers. Verification test procedures or certification of these characteristics shall be agreed upon between the supplier and the purchaser (see Section 9).

1 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

NOTE 4: Care should be taken in converting between carrier density and resistivity using SEMI MF723. Multiple conversions may introduce differences in values. For example, converting from carrier density (C_i) to resistivity and back to carrier density (C_f), may result in C_i not equaling C_f.

6 Requirements

6.1 The substrate shall conform to SEMI M1 and to the appropriate polished silicon wafer standard.

6.2 Epitaxial wafer defects shall not exceed the limits as given in Table 1.

NOTE 5: When an unetched wafer is observed for slip, it is impossible to differentiate between slip and linear misfit lines.

6.3 *Layer Thickness Variation* — Unless otherwise specified, the radial thickness variation shall be determined from values measured at the center and half radius (R/2) locations, on diameters both parallel and perpendicular to the primary flat, and shall be ≤ 6% defined as follows:

$$\text{Variation}\,(\%) = \frac{\left(\frac{R}{2} - C\right)_{\max}}{C} \times 100 \qquad (2)$$

where R/2 denotes one of the layer thickness values measured at half radius and C denotes the value at the center point.

6.4 *Net Carrier Density Variation* — The radial net carrier density variation shall be determined from values measured at the center and half radius (R/2) locations, on diameters both parallel and perpendicular to the primary flat, and shall be ≤10% for net carrier density $\geq 1 \times 10^{15}$ cm^{-3} and ≤15% for net carrier density $< 1 \times 10^{15}$ cm^{-3} defined as follows:

$$\text{Variation}\,(\%) = \frac{\left(\frac{R}{2} - C\right)_{\max}}{C} \times 100 \qquad (3)$$

where R/2 denotes one of the net carrier density values measured at half radius and C denotes the value at the center point.

7 Sampling

7.1 Unless otherwise specified, appropriate sample sizes shall be selected from each lot according to ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) in accordance with ANSI/ASQC Z1.4. Inspection levels shall be agreed upon between supplier and purchaser.

7.2 Unless otherwise specified, the following AQL's shall be assigned:

7.2.1 Epitaxial layer thickness, 6.5%,

7.2.2 Epitaxial layer net carrier density, 6.5%,

7.2.3 Epitaxial wafer defects, cumulative, 4.0%.

8 Test Methods

8.1 Measurements shall be carried out in conformance with the specified SEMI methods. Where no methods are specified or where choices are given, the supplier and purchaser shall agree in advance on the means for making the measurement.

8.2 *Substrate* — Determine in accordance with methods defined in SEMI M1.

8.3 *Epitaxial Layer*

8.3.1 *Thickness* — Determine in accordance with SEMI MF95 or SEMI MF110.

NOTE 6: There is a possibility that various types of infrared reflectance instrumentation may result in different values of epitaxial layer thickness. Therefore, the instrumentation used shall be agreed upon between supplier and purchaser.

8.3.2 *Net Carrier Density* — Determine by method(s) agreed upon between supplier and purchaser.

NOTE 7: SEMI MF1392 and SEMI MF1393 are methods for measuring net carrier density using a mercury probe contact. If resistivity is measured, as by SEMI MF374 or SEMI MF525, conversion to dopant density shall be made using SEMI MF723. Net carrier density of very heavily doped layers (or substrates) may be found using SEMI MF398. Net carrier density profiles may be determined directly in accordance with SEMI MF1392 or SEMI MF1393 or indirectly in accordance with SEMI MF672, with conversion from resistivity to net carrier density in accordance with SEMI MF723. If the method used for determining the net carrier density profile is not the same as that used to determine the center point net carrier density, correlation between the two methods used shall be established.

8.3.3 *Epitaxial Wafer Defects* — Determine in accordance with the methods given in Table 1.

8.3.3.1 Surface inspection shall be performed before any other testing. Wafers may be cleaned prior to inspection to minimize difficulty in the visual inspection of defects other than foreign matter.

8.3.3.2 Inspection for slip shall be done using grid elements constructed in accordance with SEMI M17. An element is defective if it contains one or more slip lines. The total number of defective elements shall be less than or equal to *n*, where *n* is listed in Table 1.

8.4 If substrates of different type and net carrier density than the product substrates are to be used for deposition control, their type, net carrier density, and quantity per run or lot shall be agreed upon between supplier and purchaser.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 The user and supplier may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 8; however, if the user performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Packing and Package Labeling

10.1 Special packing requirements shall be subject to agreement between the supplier and the purchaser. Otherwise, all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices to provide protection against damage during shipment.

10.2 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or container, and each subdivision thereof, in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include supplier's name and reference number, purchaser's P.O. number, quantity, dopant, orientation, conductivity type of substrates and epitaxial layers, carrier density (or resistivity, if so specified in the purchase order or contract), and thickness of the epitaxial layer. The reference number assigned by the supplier shall provide ready access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one year after the particular lot has been shipped.

Table 1 Discrete Epitaxial Wafer Defect Limits

Item	*Characteristics*	*Maximum Limit*				*Test Method*	*Notes*
1	Stacking Faults	15 per cm^2				SEMI MF1726	1
2	Slip	n = 36 grid elements				SEMI M17 and SEMI MF1726	1, 2, 3
3	Haze	NONE				SEMI MF523 Section 12.2	1, 4, 5
4	Scratches	NONE				SEMI MF523 Section 12.2	1, 5, 6
5	Edge Chips	NONE				SEMI MF523 Section 12.2	7
6	Edge Crown	Projection above wafer surface not to exceed 1/3 of epi layer thickness				To be defined	2, 8
7	Foreign Matter	NONE				SEMI MF523 Section 12.3	1, 4
8	Back Surface Contamination	NONE				SEMI MF 523 Section 12.4	1, 4
Front Surface Characteristics Dependent on Layer Thickness		Epitaxial Layer Thickness					
		< 25 µm	25–50 µm	50–100 µm	> 100 µm		
9	Large Point Defects (Density per m^2)	700	900	1200	1500	SEMI MF523 or, with automated surface inspection equipment ≥ 20 µm LSE, based on calibration of surface scanning inspection systems with polystyrene latex spheres, 90% capture rate	1, 2, 5
10	Total Localized Light Scatterers (Density per m^2)	2000	2400	2700	3000	SEMI MF523 or with automated surface inspection equipment ≥ 0.5 µm LSE, based on calibration of surface scanning inspection systems with polystyrene latex spheres, 90% capture rate	1, 2, 5

Notes:

1. Defect limits shall apply to quality area, which is defined as the entire wafer surface except a defined outer annulus: 2 inch and 3 inch = 2 mm; 100 mm and 125 mm = 3 mm; 150 mm and 200 mm = 4 mm and any are included in a window where there is a laser indentification mark.

2. Test method(s) to be agreed upon between supplier and purchaser.

3. For observation of gross slip, examine the epi layer under illumination conditions specified in Section 12.2 of SEMI MF523. For more demanding applications, it may be desirable to etch the surface in accordance with SEMI MF1726 prior to the visual inspection.

4. Any adherent contaminants, such as stains, glovemarks, dirt, smudges, and solvent residues. This characteristic does not include point defects. Any nonadherent contaminant or particulate matter easily removed by industry accepted cleaning techniques shall not constitute foreign matter or haze.

5. In today's technology, it may be possible to do this inspection using automated laser scanning systems; however, a standard test procedure has yet to be developed. Application of automated inspection must be agreed upon between supplier and user.

6. The cumulative AQL for both front surface and back surface of wafer is 2.5%.

7. The cumulative AQL for both front surface and back surface of wafer is 1.0%. Maximum radial penetration, 1.0 mm; maximum single chip peripheral length, 6.3 mm; maximum cumulative peripheral length, 6.3 mm.

8. Edge crowning may be reduced by pre-epitaxy edge rounding, or removed by post-epitaxy edge rounding.

NOTICE: SEMI makes no warranties or representations as to the suitability of the standards set forth herein for any particular application. The determination of the suitability of the standard is solely the responsibility of the user. Users are cautioned to refer to manufacturer's instructions, product labels, product data sheets, and other relevant literature respecting any materials mentioned herein. These standards are subject to change without notice.

The user's attention is called to the possibility that compliance with this standard may require use of copyrighted material or of an invention covered by patent rights. By publication of this standard, SEMI takes no position respecting the validity of any patent rights or copyrights asserted in connection with any item mentioned in this standard. Users of this standard are expressly advised that determination of any such patent rights or copyrights, and the risk of infringement of such rights, are entirely their own responsibility.

SEMI M3-0304
SPECIFICATIONS FOR POLISHED MONOCRYSTALLINE SAPPHIRE SUBSTRATES

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on December 4, 2003. Initially available at www.semi.org February 2004; to be published March 2004. Originally published in 1978; last published November 2003.

1 Purpose

1.1 Sapphire substrates are utilized for heteroepitaxial growth of silicon films for certain types of device structures. The properties of the films depend in part on the properties of the substrate used. These specifications are intended to provide specifications for the criteria necessary for growth of films suitable for device production.

2 Scope

2.1 These specifications cover requirements for five sizes (from 2 inch to 150 mm) of monocrystalline high-purity polished sapphire substrates. Dimensional and crystallographic orientation characteristics are the only standardized properties set forth herein. A purchase specification may require that additional physical properties be defined. Many of these properties are listed, together with test methods suitable for determining their magnitude. Additional information and recommended specification levels for several of these properties are provided in Related Information sections.

2.2 These specifications are directed specifically to sapphire substrates with one polished surface. Substrates polished on both sides, or unpolished, or with epitaxial deposits, are not covered; however, purchasers of such substrates may find these specifications to be a useful guide in defining their requirements.

2.3 Appendix 1 covers dimensional requirements for reclaimed 3 inch sapphire substrates.

2.4 For referee purposes, U.S. customary units shall be used for substrates of 2.0 and 3.0 in. nominal diameters, and SI (System International, commonly called metric) units for 100 mm and larger diameter substrates.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standards*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces

SEMI MF533 — Test Method for Thickness and Thickness Variation of Silicon Wafers

SEMI MF534 — Test Method for Bow of Silicon Wafers

SEMI MF671 — Test Method for Measuring Flat Length on Wafers of Silicon and Other Electronic Materials

SEMI MF847 — Test Methods for Measuring Crystallographic Orientation of Flats on Single Crystal Silicon Wafers by X-Ray Techniques

SEMI MF928 — Test Methods for Edge Contour of Circular Semiconductor Wafers and Rigid Disk Substrates

SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers

SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers

3.2 *ASTM Standard*[1]

E 122 — Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

1 Volume 14.02 of the *Annual Book of ASTM Standards,* ASTM International, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959, USA. Telephone: 610.832.9585, Fax: 610.832.9555, Website: www.astm.org.

3.3 *Other Standard*[2]

ANSI/ASQC Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall be the latest published versions.

4 Terminology

4.1 *Definitions*

4.1.1 *lot* — for the purposes of these specifications, (a) all of the substrates of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of substrates as (a) above which have been identified by the supplier as constituting a lot.

4.1.2 *sapphire* (*in silicon-on-sapphire technology*) — single crystal aluminum oxide (Al_2O_3) having a definite orientation that allows epitaxial silicon deposition.

4.1.3 *substrate* — the polished sapphire slice upon which the epitaxial layer of silicon is grown.

5 Ordering Information

5.1 Purchase orders for sapphire substrates furnished to these specifications shall include the following items:

5.1.1 Nominal diameter (see Table 1),

5.1.2 Crystal growth method (see Note 1),

5.1.3 Surface orientation (see Table 1 and Figures 1 and 2),

5.1.4 Lot acceptance procedures (see Section 9),

5.1.5 Certification (if required) (see Section 12), and

5.1.6 Packing and marking (see Section 13).

5.2 The following items may be specified optionally in addition to those listed in Section 5.1:

5.2.1 Crystal perfection,

5.2.2 Surface defect and contaminant levels,

5.2.3 Impurities,

5.2.4 Front surface finish quality level (see Figures R2-1 through R2-4),

5.2.5 Back surface finish,

5.2.6 Secondary flat (see Figure 3),

5.2.7 Flatness (see Table 2), and

5.2.8 Edge Profile.

NOTE 1: The crystal growth method (for example, Czochralski or EFG ribbon) is difficult to ascertain in the finished substrates. Verification test procedures or certification of these characteristics (see Section 12) shall be agreed upon between the supplier and the purchaser.

NOTE 2: Items in Section 5.2 are less commonly specified than the others but are included for completeness as parameters for which methods of evaluation have been developed.

6 Dimensions and Permissible Variations

6.1 The material shall conform to the dimensions and dimensional tolerances as specified in Table 1 for the following parameters.

6.1.1 *Diameter*,

6.1.2 *Center Point Thickness*,

6.1.3 *Total Thickness Variation*,

6.1.4 *Primary Flat Length*,

6.1.5 *Secondary Flat Length*,

6.1.6 *Flat Locations*, and

6.1.7 *Bow*.

6.2 The orientation of the substrate material shall be identified by a flat system as defined in Section 11.

6.3 If specified in the purchase order or contract the front surface flatness shall be identified in accordance with the classification system in Table 2.

6.4 If specified in the purchase order or contract, the edge shall be rounded and beveled.

7 Materials and Manufacture

7.1 The material shall consist of slices from sapphire grown by the process specified in the purchase order or contract.

8 Physical Requirements

8.1 The material shall conform to the crystallographic orientation details listed in Table 1 (see Figure 1).

8.2 The following items, if included, shall conform to the requirements specified in the purchase order or contract:

8.2.1 Crystal perfection,

8.2.2 Surface defect and contaminant levels (See Related Information 1 for surface defect definitions and Table R1-1 for suggested allowable levels of surface defects.),

8.2.3 Amount of impurities,

2 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202. Website: www.asqc.org.

8.2.4 Front surface finish quality level (see Related Information 2 and Figures R2-1 through R2-4 for information on recommended front surface finish quality levels), and

8.2.5 Back surface finish (see Related Information 2 for recommended back surface finish level).

9 Sampling

9.1 Unless otherwise specified, ASTM Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4-1993. Each quality characteristic shall be assigned an acceptable quality level (AQL) and lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4-1993 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL and LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

10 Test Methods

10.1 *Dimensions* — Measure as follows:

10.1.1 *Diameter* — Determine by a method agreed upon between the supplier and the purchaser at locations specified in Configuration 1 of SEMI MF2074.

NOTE 3: Sapphire substrates are highly susceptible to surface damage. While the mechanical dimensions of a slice can be measured by use of tools such as micrometer calipers and other conventional techniques, the substrate may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement methods.

10.1.2 *Thickness, Center Point* — Determine at the center of the substrate (Point 2 in Figure 4) in accordance with SEMI MF533.

10.1.3 *Total Thickness Variation (5 point)* — Determine in accordance with SEMI MF533, except that thickness measurements shall be made at the five locations in Figure 4 instead of the locations specified in SEMI MF533. Points 1, 3, 4, and 5 in Figure 4, which define the locations of the edge measurements, are located 6 mm in from the wafer periphery.

10.1.4 *Flat Length* — Determine in accordance with SEMI MF671.

10.1.5 *Bow* — Determine in accordance with SEMI MF534.

10.2 *Flat Orientation* — Determine in accordance with SEMI MF847.

10.3 *Surface Orientation* — Determine in accordance with the x-ray method of SEMI MF26.

10.4 *Crystal Perfection* — Unless otherwise specified, determine in accordance with SEMI MF1810.

10.5 *Surface Defects and Contamination* — Determine defects in accordance with SEMI MF523.

10.6 *Other Impurities* — Determine by methods agreed upon between the supplier and the purchaser.

10.7 *Front Surface Finish* — Determine by methods agreed upon between the supplier and the purchaser.

10.8 *Back Surface Finish* — Determine by methods agreed upon between the supplier and the purchaser.

10.9 *Flatness* — Determine by a method agreed upon between the supplier and the purchaser.

10.10 *Edge Profile* — Determine by a method agreed upon between the supplier and the purchaser. Method B of SEMI MF928 is a non-destructive way of evaluating the shape of the edge profile; if this method is used, the template to be used shall be agreed upon between the supplier and the purchaser.

11 Flat System

11.1 Figures 2 and 3 describe the primary and secondary flat system.

11.1.1 *Primary Flat:* 45° ± 2° in the counter-clockwise direction from the projection of the c-axis along an r-plane.

11.1.2 *Secondary Flat (Optional):* 90° ± 2° in the counter-clockwise direction from the primary flat, along an r-plane.

11.2 The a-axis lies between the two flats bisecting the 90° angle. Projection of the c-axis lies 45° in the clockwise direction from the primary flat and 90° in the clockwise direction from the a-axis.

12 Certification

12.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

12.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 11. However, if the purchaser performs the test and the material fails to

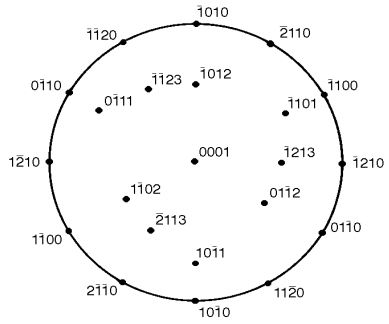
meet the requirements, the material may be subject to rejection.

13 Packing and Marking

13.1 Special packing requirements shall be subject to agreement between the supplier and the purchaser. Otherwise all slices shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices to provide ample protection against damage during shipment.

13.2 The substrates supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container, and each subdivision thereof, in which it may reasonably be expected that the substrates will be stored prior to further processing. Identification shall include, as a minimum, the nominal diameter, orientation, and lot number. The lot number, either (1) assigned by the original manufacturer of the substrates, or (2) assigned subsequent to substrate's manufacture, but providing reference to the original lot number, shall provide ready access to information concerning the fabrication history of the particular substrates in that lot. Such information shall be retained on file at the manufacturer's facility for at least one month after that particular lot has been accepted by the purchaser.

Structural Indices	Mineralogical Symbols
$1\bar{1}02$	r
$01\bar{1}2$	r
$\bar{1}012$	r
0001	c
1010	m
$11\bar{2}0$	a
$10\bar{1}1$	s
$2\bar{1}\bar{1}3$	n



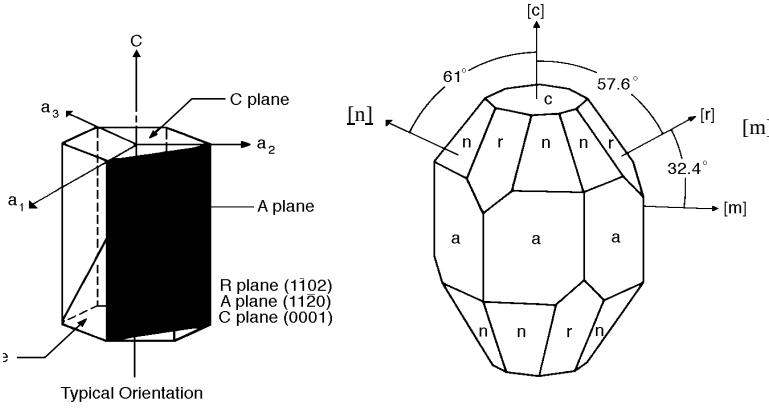


Figure 1
Sapphire Crystallographic Diagrams

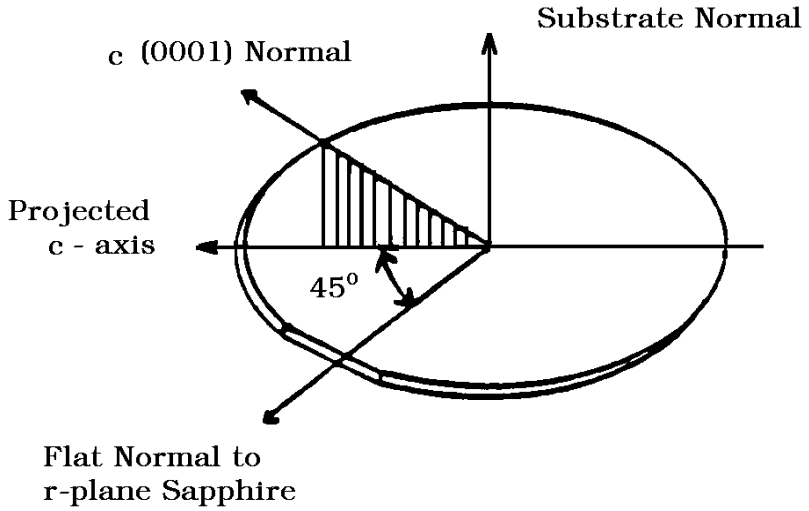


Figure 2
Sapphire Surface Orientation

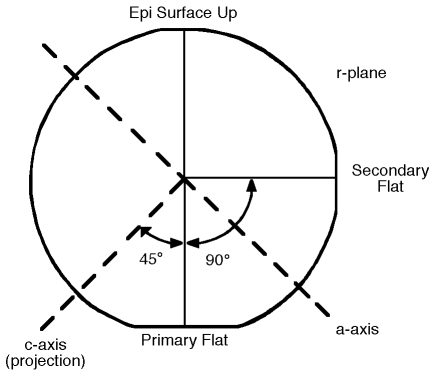


Figure 3
Primary and Secondary Flat Locations

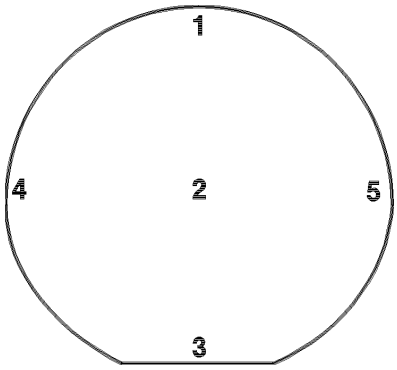


Figure 4
Measurement Points for Determination of Layer Thickness Variation

Table 1 Dimensional Specification for Sapphire Substrates

Nominal Diameter		*2 inch*		*3 inch*		*100 mm*		*125 mm*		*150 mm*	
Previous Standard		*SEMI M3.2-91*		*SEMI M3.4-91*		*SEMI M3.5-92*		*SEMI M3.7-91*		*SEMI M3.8-91*	
Property	*Units*	*Min*	*Max*	*Min*	*Max*	*Min*	*Max*	*Min*	*Max*	*Min*	*Max*
DIAMETER	mm in.	50.55 1.990	51.05 2.010	76.95 2.990	76.45 3.010	99.0 3.90	101.0 3.97	124.0	126.0	149.0	151.0
THICKNESS, CENTER POINT	µm in.	280 0.011	380 0.015	380 0.15	480 0.19	500 0.0197	550 0.0216	600	650	650	700
PRIMARY FLAT LENGTH	mm in.	14.23 0.56	17.52 0.69	19 0.75	25 1.00	30.0 1.182	35.0 1.377	40.0	45.0	55.0	60.0
SECONDARY FLAT LENGTH	mm. in.	6.35 0.25	9.65 0.38	9.6 0.38	12.7 0.50	16.0 0.630	20 0.787	18.0	22.0	35.0	40.0
BOW, max	µm in.		38 0.0015		51 0.002		40		60		60
WARP, max	µm in.	Not Specified		Not Specified			40		60		60
TOTAL THICKNESS VARIATION, max	µm in.		51 0.002		76 0.0030		56 0.0019		50		60
SURFACE ORIENTATION		$\{1\bar{1}02\} \pm 2.0°$ (NOTE 3)									
NOTES		1		1		2		2		2	

NOTE 1: For referee purposes, the U.S. Customary units apply. Conversion to metric (SI) equivalents was done following the maximum-minimum convention in which the minimum values are rounded up and the maximum values are rounded down to ensure that the equivalent range is always inside the referee range. If the metric equivalents are used for incoming inspection measurements, the rightmost digit of minimum values should be reduced by 1 and the rightmost digit of maximum values should be increased by 1 to avoid rejection of material that is within the specification when measured by the referee system of units. CAUTION — The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data that can be used to construct appropriate guard bands.

NOTE 2: For referee purposes, the metric (SI) units apply. Conversion to U.S. Customary equivalents was done following the maximum-minimum convention in which the minimum values are rounded up and the maximum values are rounded down to ensure that the equivalent range is always inside the referee range. If the metric equivalents are used for incoming inspection measurements, the rightmost digit of minimum values should be reduced by 1 and the rightmost digit of maximum values should be increased by 1 to avoid rejection of material that is within the specification when measured by the referee system of units. CAUTION — The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data that can be used to construct appropriate guard bands.

NOTE 3: Equivalent $\{1\bar{1}02\}$ r planes are $(1\bar{1}02)$, $(01\bar{1}2)$, and $(10\bar{1}2)$, see Figure 1.

Table 2 Flatness Classes for Sapphire Substrates

Class	*Flatness (TIR), µm*
I	25 max
II	14 max
III	10 max
IV	8 max
V	6 max

APPENDIX 1
SPECIFICATION FOR 3 INCH RECLAIMED SAPPHIRE SUBSTRATES

NOTICE: The material in this appendix is an official part of SEMI M3 and was approved by full letter ballot procedures on September 3, 2003**.** The material in this appendix was originally included in SEMI M3.6-88, Standard for 3 inch Reclaimed Sapphire Substrates.

A1-1.1 Dimensional specifications for 3 inch reclaimed sapphire substrates are given in Table A1-1.

A1-1.2 Surface orientation shall be as received for reclamation.

A1-1.3 Flat location(s) shall be as received for reclamation.

A1-1.4 Flatness shall be classified in accordance with Table 2. The amount of surface damage and flatness of the as-received substrate determines final flatness.

A1-1.5 Front surface finish shall be in accordance with the purchase order or contract. See Related Information 2 for recommendations on acceptable front surface finish level.

A1-1.6 Back surface finish shall be as received for reclamation.

A1-1.7 Other characteristics, including sampling, test methods, surface defect limits, certification, and packing and marking, shall be as specified in SEMI M3.

Table A1-1 Dimensional Specification

Property	*Min*	*Max*	*Units (see NOTE 1)*
DIAMETER	As received for reclamation.		
THICKNESS, CENTER POINT (see NOTE 2)	0.014 360	0.019 480	in. μm
FLAT LENGTH	As received for reclamation.		
BOW, max		0.002 51	in. μm

NOTE 1: For referee purposes, the U.S. Customary units apply. Conversion to metric (SI) equivalents was done following the maximum-minimum convention in which the minimum values are rounded up and the maximum values are rounded down to ensure that the equivalent range is always inside the referee range. If the metric equivalents are used for incoming inspection measurements, the rightmost digit of minimum values should be reduced by 1 and the rightmost digit of maximum values should be increased by 1 to avoid rejection of material that is within the specification when measured by the referee system of units. CAUTION — The significance of the rightmost digit may vary, depending on the quantity being measured and the precision of the test procedure. Refer to the relevant test method for precision data that can be used to construct appropriate guard bands.

NOTE 2: Amount of surface damage and flatness of as-received substrate determines final substrate thickness.

RELATED INFORMATION 1
RECOMMENDED SAPPHIRE SUBSTRATE FRONT SURFACE DEFECT LIMITS

NOTICE: This related information is not an official part of SEMI M3 and was derived from the original edition of the specifications which erroneously included this optional material as a part of the text of the specification. This related information was approved for publication by full letter ballot procedure on September 3, 2003.

R1-1 Definitions for surface defects are found in SEMI MF523, where defects commonly found on silicon slices are defined. Some of these terms do not apply to sapphire substrates, but are present in Table R-1, which lists recommended limits for front surface defect levels, to provide a convenient reference point to the silicon wafer standards, such as SEMI M1.

R1-1.1 *Minimal Conditions and/or Dimensions* — Minimal conditions or dimensions for defects are stated below and shall be used for determining substrate acceptability unless other minimal limiters are agreed upon by the interested parties. Anomalies less than these limits shall not be considered defects.

R1-1.2 *Area Contamination* — Foreign matter on the surface in localized areas which is revealed as discolored, mottled, or cloudy appearance resulting from smudges, stains, water spots, etc.

R1-1.3 *Contamination* — Any foreign matter detectable under the inspection lighting conditions.

R1-1.4 *Edge Chips and Indents* — Any edge or surface anomaly conforming to the accepted definition greater than 0.010 inch in radial depth and peripheral length.

R1-1.5 *Cracks* — Any anomaly conforming to the accepted definition greater than 0.010 inch (0.25 mm) in total length.

R1-1.6 *Craters* — Any individually distinguishable surface anomaly conforming to the accepted definition visible when viewed under diffuse illumination.

R1-1.7 *Crow's Feet* — N.A.

R1-1.8 *Grooves* — N.A.

R1-1.9 *Haze* — Haze is indicated when the image of a narrow beam tungsten lamp filament is detectable on the epi silicon surface. (Under some conditions, contamination may appear as haze.)

R1-1.10 *Mounds* — N.A.

R1-1.11 *Orange Peel* — Any visually detectable roughened surface conforming to the accepted definition observable under diffuse illumination.

R1-1.12 *Pits* — Any individually distinguishable nonremovable surface anomaly conforming to the accepted definition visible when viewed under intense illumination.

R1-1.13 *Saw Exit Mark* — N.A.

R1-1.14 *Scratch* — Any anomaly conforming to the definition with a length-to-width ratio greater than 5:1.

R1-1.15 *Striation* — Any feature conforming to the accepted definition detectable under background lighting conditions.

Table R1-1 Recommended Sapphire Substrate Defect Limits

Item	*Characteristics*	*Max Defect Limit*	*AQL (see NOTE 6)*	*Illumination*	*Notes*
1	SCRATCHES Maximum Number Maximum Length	3 R/2		High Intensity	1
2	PITS Maximum Number 2" Diameter Substrate 3" Diameter Substrate 100 mm Diameter Substrate 125 mm Diameter Substrate 150 mm Diameter Substrate	 4 9 15 20 25	4% Cum.		1, 2
3	HAZE	None — see NOTE 4	4% Cum.		4
4	CONTAMINATION/PARTICULATE Maximum Number 2" Diameter Substrate 3" Diameter Substrate 100 mm Diameter Substrate 125 mm Diameter Substrate 150 mm Diameter Substrate	 4 9 15 20 25	4% Cum.	Diffuse	1, 2
5	CONTAMINATION/AREA	None			
6	EDGE CHIPS Maximum Number Maximum Radial Penetration Maximum Single Chip Peripheral Length Maximum Cumulative Peripheral Length	see NOTE 3 2 0.12" (3 mm) 0.250" (6.35 mm) 0.250" (6.35 mm)	4% Cum.	Diffuse	3
7	CRACKS, CROW' S FEET		see NOTE 6		6
8	CRATERS	None			1, 5
9	DIMPLES	None			1
10	GROOVES	None	4% Cum.		1, 5
11	MOUNDS	None			1, 5
12	ORANGE PEEL	None		Diffuse	1
13	SAW MARKS	None			1, 5
14	STRIATIONS				
SLICE BACK SURFACE					
15	CHIPS	see NOTE 3	see NOTE 3	Diffuse	3
16	CRACKS, CROW' S FEET	None	see Note 6		6
17	CONTAMINATION/AREA	None			
18	SAW MARKS Incidence Maximum Depth	N.A.	see Note 5		5

NOTE 1: The outer 4 mm annulus is excluded from these criteria.

NOTE 2: Ninety percent of substrate shall be free of contaminants after pre-inspection treatment. Balance of substrate may have light-reflecting particles up to the limit established for Item 2 — Pits.

NOTE 3: All chips shall be beveled. Chips less than 0.4 mm should not be counted.

NOTE 4: Haze refers to epitaxial silicon appearance only, not to condition of polished sapphire substrate.

NOTE 5: These defects are not observed in SOS wafers. Terms remain for convenient reference to silicon specification.

NOTE 6: Cracks are observed in sapphire substrates as fractures or as surface separations along cleavage planes. The cumulative AQL for both front surface and back surface of substrate is 4% for both. Crow's feet see Note 5.

RELATED INFORMATION 2
RECOMMENDED SURFACE FINISH CHARACTERISTICS FOR SAPPHIRE SUBSTRATES

NOTICE: This related information is not an official part of SEMI M3 and was derived from the original edition of the specifications which erroneously included this optional material as a part of the text of the specification. This related information was approved for publication by full letter ballot procedure on September 3, 2003.

R2-1 Front Surface Finish

R2-1.1 The substrate should be polished on one side suitable for the epitaxial growth of silicon.

R2-1.2 The quality of this surface may be determined by optical examination at 70× using Nomarski interference contrast microscopy after etching the substrate in potassium hydroxide at 310°C for one to three minutes.

R2-1.3 The photomicrographs in Figures R2-1 through R2-4 may be used as a surface quality guide.

R2-1.3.1 Figure R2-1 shows an acceptable surface.

R2-1.3.2 Figures R2-2 and R2-3 show questionable surfaces that are subject to individual evaluation.

R2-1.3.3 Figure R2-4 shows an unacceptable surface.

R2-2 Back Surface Finish

R2-2.1 The recommended back surface finish is approximately 32 μin, rms, as determined by stylus or optical profilometer.

Figure R2-1
Acceptable Surface

Figure R2-2
Questionable Surface

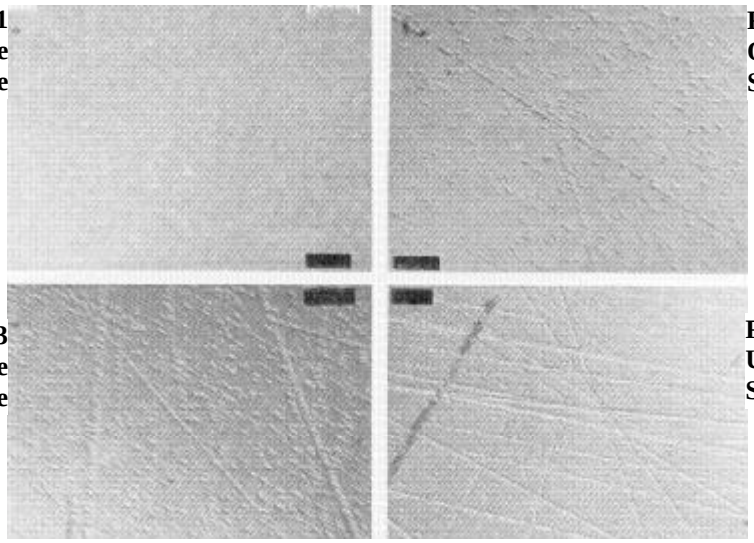


Figure R2-3
Questionable Surface

Figure R2-4
Unacceptable Surface

Figures R2-1 through R2-4
Illustrations of Acceptable, Unacceptable, and Questionable Sapphire Substrate Front Surface Finishes.

SEMI M4-1103
SPECIFICATIONS FOR SOS EPITAXIAL WAFERS

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the North American Silicon Wafer Committee. Current edition approved by the North American Regional Standards Committee on July 27, 2003. Initially available on www.semi.org October 2003; to be published November 2003. Originally published in 1978; previously published July 2003.

1 Purpose

1.1 These specifications cover requirements for monocrystalline silicon epitaxial layers on sapphire substrates, used for semiconductor device manufacture. The combination of a silicon epitaxial layer on a sapphire substrate is known as a silicon on sapphire (SOS) epitaxial wafer. By outlining an inspection process and defining various reject criteria, both suppliers and purchasers can uniformly define epitaxial layer quality.

1.2 The defects discussed originate from two sources: those which are caused by imperfection in the sapphire substrate and those related to the epitaxial layer, including handling and packaging.

2 Scope

2.1 The primary standardized properties set forth in this specification relate to physical, dimensional, and electrical characteristics of SOS epitaxial wafers.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards

3.1 *SEMI Standard*

SEMI M3 — Specifications for Polished Monocrystalline Sapphire Substrates

SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers

SEMI MF95 — Test Method for Thickness of Epitaxial Layers of Silicon on Substrates of the Same Type by Infrared Reflectance

NOTE 1: Modifications to this procedure are required for use on SOS wafers.

SEMI MF110 — Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique

SEMI MF154 — Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces

SEMI MF374 — Test Method for Sheet Resistance of Silicon Epitaxial, Diffused, Polysilicon, and Ion-implanted Layers Using an In-Line Four-Point Probe with the Single-Configuration Procedure

SEMI MF523 — Practice for Unaided Visual Inspection of Polished Silicon Wafers

SEMI MF673 — Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

3.2 *ASTM Standards*[1]

E 122 — Practice for Choice of Sample Size to Estimate the Average Quality of a Lot or Process

3.3 *Other Standard*[2]

ANSI/ASQC Z1.4-1993 — Sampling Procedures and Tables for Inspection by Attributes

NOTICE: Unless otherwise indicated, all documents cited shall the the latest published versions.

4 Terminology

4.1 *Definitions*

4.1.1 *deposition* — the technique involved in the vapor deposition of single-crystal silicon on oriented sapphire substrates.

4.1.2 *dopant* — a chemical element, usually from the third or fifth columns of the periodic table (typically phosphorous, arsenic, or boron), incorporated in trace amounts in the epitaxial layer to establish its conductivity type and resistivity.

4.1.3 *doping* — the process of incorporation of a dopant into the epitaxial layer while the film is growing.

4.1.4 *epitaxial layer* — the layer of semiconductor material that is grown on the substrate.

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1 ASTM International, 100 Barr Harbor Drive, West Conshohoken, PA 19428-2959, USA, Website: www.astm.org, (PracticeE 122 may be found in Volume 14.02 of the Annual Book of ASTM Standards.)
2 American National Standards Institute, Headquarters: 1819 L Street, NW, Washington, DC 20036, USA. Telephone: 202.293.8020; Fax: 202.293.9287, New York Office: 11 West 42nd Street, New York, NY 10036, USA. Telephone: 212.642.4900; Fax: 212.398.0023, Website: www.ansi.org

4.1.5 *lot* — for the purpose of this document, (a) all of the wafers of nominally identical specification and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of epitaxial wafers as above which have been identified by the supplier as constituting a lot.

4.1.6 *pre-epitaxial treatment* — the process of etching an amount of material from the sapphire substrate in situ prior to deposition.

NOTE 2: Hydrogen (H_2) gas is commonly used for this purpose.

4.1.7 *resistivity (*Ω·cm*)* — for the purpose of this method, the volume resistivity, the ratio of the potential gradient parallel to the current in the material to the current density.

4.1.8 *silicon source* — volatile or gaseous silicon compound.

NOTE 3: Silane (SiH_4) gas is commonly used for this purpose.

4.1.9 *substrate* — the polished sapphire slice upon which the epitaxial layer is deposited.

4.1.10 *surface defects* — refers to mechanical imperfections, SiO_2 residual dust, and other imperfections visible on the wafer surface. Some examples of surface defects are: dimples, pits, particulates, spots, scratches, smears, hillocks, and polycrystalline regions. Definitions given in SEMI MF154 shall be used.

4.1.11 *wafer, SOS epitaxial* — the combined sapphire substrate with the deposited epitaxial layer.

5 Ordering Information

5.1 Purchase orders for sapphire substrates furnished to this specification shall refer to SEMI M3.

5.2 Purchase orders for the epitaxial layer on sapphire substrates furnished to this specification shall include specifications for the following items:

5.2.1 Silicon source (if required),

5.2.2 Conductivity type and doping source,

5.2.3 Pre-epitaxial treatment (if required),

5.2.4 Thickness and thickness variation,

5.2.5 Resistivity and resistivity variation,

5.2.6 Film crystallinity,

5.2.7 Microparticulate density,

5.2.8 Surface defects and contamination,

5.2.9 Methods of test and measurements (see Section 7),

5.2.10 Lot acceptance procedures (see Section 8),

5.2.11 Certification (if required) (see Section 9), and

5.2.12 Packing and marking (see Section 10).

6 Requirements

6.1 The substrate shall conform to the requirements of SEMI M3.

6.2 The epitaxial layer shall meet the specification requirements for the following characteristics as specified in the purchase order or contract (see Section 5.2).

6.2.1 Pre-epitaxial treatment (if required),

6.2.2 Thickness and thickness variation,

6.2.3 Resistivity and resistivity,

6.2.4 Film crystallinity,

6.2.5 Microparticulate density, and

6.2.6 Surface defects.

6.2.7 Correlation of these characteristics and verification test procedures or certification of these characteristics shall be agreed upon between the supplier and purchaser.

7 Methods of Test and Measurement

7.1 *Substrate* — Determine by methods agreed upon between the user and supplier. For measurement methods, see SEMI M3.

7.2 *Epitaxial Layer (See Note 4)*

7.2.1 *Layer Thickness* — Determine by a method agreed upon between supplier and purchaser. The film thickness at Point 2, at the wafer center as shown in Figure 1, is the nominal film thickness for the wafer. Recommended: SEMI MF95, suitably modified for use with SOS structures.

7.2.2 *Layer Thickness Variation* — Unless otherwise specified, the radial thickness variation shall be determined from values measured at the center and edge locations, as shown in Figure 1. Points 1, 3, 4, and 5 are located 6 mm in from the wafer periphery and define the location of the edge measurements. All thickness values must be within the specified range. For example, for a film specified at 0.50 µm ± 10%, all readings at points 1–5 must be within the range from 0.45 to 0.55 µm.

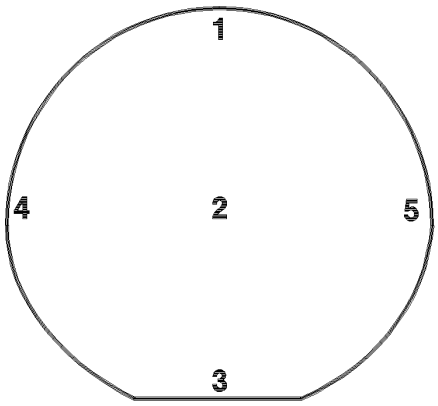

Figure 1
Measurement Points for Determination of Layer Thickness Variation

7.2.3 *Resistivity* — Determine by a method agreed upon between supplier and purchaser. Contacting method: SEMI MF374; Non-contacting method: SEMI MF673.

7.2.4 *Radial Resistivity Variation* — Determine in accordance with sampling plan A of SEMI MF81.

7.2.5 *Film Crystallinity* — Determine by the following or an alternative method as agreed between supplier and purchaser.

7.2.5.1 SOS films can display varying degrees of haze due to polycrystalline silicon deposits in the film. These polycrystalline deposits can result from improper deposition temperatures, substrate surface contaminants, or contaminants in the reactor or reactor gases.

7.2.5.2 Haze can be seen visually and can be quantitatively measured by ultraviolet light reflectance spectroscopy or by x-ray diffraction (pole figure) measurements.[3] The ultraviolet light reflectance (UVR) value is commonly measured to determine the film crystalline quality. In this technique, measure the relative reflectance at two wavelengths, 280 and 440 nm, using a clean, polished (100) silicon substrate as the reference as in the following example:

$$\Delta R_{280} = \frac{|R_{ref} - R_{SOS}|}{R_{ref}}$$

7.2.5.3 Record the difference between the two reflectance values, R_{280}–R_{440}, as the UVR value. For films in the thickness range 0.5 to 0.8 µm, the R_{280}–R_{440} value shall be less than 15 units. This value is an average of 5 points measured in the wafer as shown in Figure 1. The edge measurements are located at 12.5 mm in from the wafer periphery.

7.2.5.4 For thinner films from 0.2 to 0.6 µm, the reflectance value at the single wavelength of 280 nm can be used.

7.2.5.5 X-ray pole figure analysis measures the volume concentration of microtwins, as % (111), in the silicon film.

7.2.5.6 The ultraviolet reflectance values and pole figure values are dependent on film thickness, so specified limits are listed for each film thickness in Table 1.

7.2.6 *Microparticulate Density* — SOS films can display varying degrees of surface cleanliness as viewed with a microscope. Small particles trapped in the film can cause yield losses in some devices. Determine the density of small particles by counting the particles observed during an *X-Y* scan across the wafer using Normarski interference contrast microscopy at 100×. For particles greater than 2 µm in diameter, the particle density shall be less than 2 defects per square centimeter, excluding the outer 6 mm of the wafer periphery.

Table 1 Ultraviolet Reflection and X-Ray Pole Figure Values

Film Thickness	*Average Value, (MAX)*		*1 Peripheral Value, (MAX)*	
µm	ΔR_{280}	*%(111)*	ΔR_{280}	*%(111)*
0.20	15	7.0	23	11.5
0.30	17	5.5	28	9.5
0.40	21	5.0	33	8.0
0.50	27	4.5	42	7.0
0.60	32	4.0	51	6.5

3 Currently, there is no standardized method for this procedure. The procedure is described in: M.T. Duffy, *et al*, *Semiconductor Measurement Technology*: Method to Determine the Quality of Sapphire, National Institute of Standards and Technology Report No. NBS SP400-62,August 1980. Available from the National Technical Information Service, Springfield, VA, as PB80-212830. See also: M.T. Duffy, *et al, J. Crystal Growth* **58** (1982) 10.

7.2.7 *Surface Defects and Contamination* — Determine by methods agreed upon between user and supplier. SEMI MF154 is a useful guide for defining a variety of surface features and establishing commonly understood terms for describing surface defects and contamination. SEMI MF523 is also recommended (see Note 5). Recommended maximum levels of surface defects and contamination are listed in Table 2.

NOTE 4: SOS wafers are susceptible to surface damage. The thin film on the hard sapphire substrate may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement procedures.

NOTE 5: In SEMI MF523, defects commonly found in silicon wafers are defined. Some of these terms do not apply to SOS wafers, but are included in Table 2 to provide a convenient reference point to the silicon wafer and epitaxial wafer standards. In this case, the recommended maximum acceptable limit is shown as N.A. (not applicable).

8 Sampling

8.1 Unless otherwise specified, ASTM Practice E 122 shall be used. When so specified, appropriate sample sizes shall be selected from each lot according to ANSI/ASQC Z1.4-1993. Each quality characteristic shall be assigned an acceptable quality level (AQL) and lot total percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4-1993 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL and LTPD values. Inspection levels shall be agreed upon between user and supplier.

Table 2 Recommended Maximum Surface Defects Levels by Non-Destructive Means

ITEM	*CHARACTERISTICS*	*MAX ACCEPTABLE LIMIT*	*TEST METHOD*	*DEFECT DEFINITION PER*	*NOTES*
1	STACKING FAULTS	N.A.			2
2	SLIP	N.A.			2
3	PROTRUDING DEFECTS (Including spikes, hillocks, pyramids, and inclusions)	N.A.			2
4	PITS	Diameter No. 2" 4 3" 9 100 mm 15 125 mm 20 150 mm 25	SEMI MF523	SEMI MF154	1, 3
5	SCRATCHES	Cumulative L 1/2 wafer radius	SEMI MF523	SEMI MF154	1, 3
6	CRACKS, FRACTURES	None	SEMI MF523	SEMI MF154	5
7	ORANGE PEEL	N.A.			2
8	EDGE CHIPS	Max No. 2	SEMI MF523	SEMI MF154	2
9	EDGE CROWN	N.A.			2
10	HAZE	None	SEMI MF523	SEMI MF154	1, 6
11	FOREIGN MATTER FINGER PRINTS	None	SEMI MF523	SEMI MF154	1, 7

NOTE 1: The outer 4 mm annulus is excluded from these criteria.

NOTE 2: These defects are not observed in SOS wafers. Terms remain for convenient reference to epitaxial silicon wafer specification.

NOTE 3: Ninety percent of the wafers shall be free of these defects. Balance of wafer may have defects at these limits.

NOTE 4: All chips shall be beveled. Maximum penetration 3 mm. Pointed apex chips none. Chips less than 0.4 mm (0.015 in.) shall not be counted. See SEMI M3, Table R1-1.

NOTE 5: Cracks are observed in sapphire as fractures or as surface separations along cleavage planes.

NOTE 6: Haze refers to the presence of polycrystalline silicon deposits in the film, as described in Section 7.2.5. Haze shall not be visible under lighting conditions of ASTM F 523.

NOTE 7: Particulate matter easily removed by industry-accepted cleaning techniques shall not constitute foreign matter.

9 Certification

9.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 In the interest of controlling inspection costs, the supplier and purchaser may agree that the material shall be certified as "capable of meeting" certain requirements. In this context, "capable of meeting" shall signify that the supplier is not required to perform the appropriate tests in Section 7; however, if the purchaser performs the test and the material fails to meet the requirements, the material may be subject to rejection.

10 Packing and Marking

10.1 Special packing requirements shall be subject to agreement between the user and supplier. Otherwise all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices to provide protection against damage during shipment.

10.2 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or container, and each subdivision thereof, in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include supplier's name and reference number, purchaser's part number, purchaser order number, quantity, dopant, conductivity type of epitaxial layers, resistivity and thickness of the epitaxial layer; the reference number assigned by the supplier shall provide ready access to information concerning the fabrication history of the particular substrates in that lot. Such information shall be retained on file at the manufacturer's facility for at least one month after that particular lot has been accepted by the purchaser.

SEMI M6-1000
SPECIFICATION FOR SILICON WAFERS FOR USE AS PHOTOVOLTAIC SOLAR CELLS

This specification was technically approved by the Global Silicon Wafer Committee and is the direct responsibility of the European Materials Committee. Current edition approved by the European Regional Standards Committee on July 28, 2000. Initially available at www.semi.org September 2000; to be published October 2000. Originally published in 1981; previously published in 1985.

NOTE: This document replaces the previous version of SEMI M6 and M6.1, M6.2, M6.3, M6.4, and M6.5 in their entirety.

1 Purpose

1.1 This specification covers the requirements for silicon wafers for use in photovoltaic (PV) solar cell manufacture.

2 Scope

2.1 The dimensional characteristics, crystalline defects and commonly used wafer electronic properties are described. Two classes of crystalline silicon materials are recognized: monocrystalline and multicrystalline.

2.2 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

2.3 SI (System International) units are used throughout.

3 Referenced Standards

NOTE 1: The specification recognizes only two discrete material forms monocrystalline and multicrystalline. In the monocrystalline form one crystallographic orientation describes the whole wafer and in the multicrystalline case there is more than one crystallographic orientation present.

3.1 *SEMI Standard*

SEMI M1 — Specifications for Polished Monocrystalline Silicon Wafers

3.2 *ASTM Standards*[1]

E 122 — Standard Practice for Choice of Sample Size to Estimate the Average for a Characteristic of a Lot or Process

F 26 — Standard Test Methods for Determining the Orientation of a Semiconductive Single Crystal

F 28 — Standard Test Methods for Minority-Carrier Lifetime in Bulk Germanium and Silicon by Measurement of Photoconductivity Decay

F 42 — Standard Test Methods for Conductivity Type of Extrinsic Semiconducting Materials

F 43 — Standard Test Methods for Resistivity of Semiconductor Materials

F 84 — Standard Test Method for Measuring Resistivity of Silicon Wafers with an In-Line Four-Point Probe

F 391 — Standard Test Methods for Minority Carrier Diffusion Length in Extrinsic Semiconductors by Measurement of Steady-State Surface Photovoltage

F 398 — Standard Test Method for Majority Carrier Concentration in Semiconductors by Measurement of Wavenumber or Wavelength of the Plasma Resonance Minimum

F 533 — Standard Test method for Thickness and Thickness Variation of Silicon Wafers

F 613 — Standard Test Method for Measuring Diameter of Semiconductor Wafers

F 657 — Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning

F 673 — Standard Test Methods for Measuring Resistivity of Semiconductor Slices or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage

F 1188 — Standard Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

F 1391 — Standard Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

F 1535 — Standard Test Method for Carrier Recombination Lifetime in Silicon Wafers by Noncontact Measurement of Photoconductivity Decay by Microwave Reflectance

F 1619 — Standard Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle

1 American Society for Testing and Materials, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959

3.3 *DIN Standards*[2]

50430 — Messung des spezifischen elektrischen Widerstandes von stabformigen Einkristallen aus Silicium oder Germanium mit dem Zwei-Sonden-Gleichstrom-Verfahren (Measurement of the Electrical Resistivity of Silicon or Germanium single Crystals in Bars by means of the Two-Point-Probe Direct Current Method)

50431 — Messung des spezifischen elektrischen Widerstandes von Einkristallen aus Silicium oder Germanium mit dem Vier-Sonden-Gleichstrom-Verfahren bei linearer Anordnung der Sonden (Measurement of the Electrical Resistivity of Silicon or Germanium Single Crystals by Means of the Four-Point-Probe Direct Current method with collinear Four Probe Array)

50432 — Bestimmung des Leitungstyps von Silicium oder Germanium mittels Richttest oder Thermosonde (Determination of the Conductivity Type of Silicon or Germanium by Means of Rectification Test or Hot-Probe)

50433-1 — Bestimmung der Orientierung von Einkristallen mit einem Roentgengoniometer (Determining the orientation of Single Crystals by Means of X-Ray Diffraction)

50433-2 — Bestimmung der Orientierung von Einkristallen nach der Lichtfigurenmethode (Determining the orientation of Single crystals by Means of Optical Reflection Figure)

50433-3 — Bestimmung der Orientierung von Einkristallen mittels Laue-Rueckstrahl-Verfahren (Determination of the Orientation of Single Crystals by Means of Laue Back Scattering)

50438-1 — Bestimmung des Verunreinigungsgehaltes in Silicium mittels lnfrarot-Absorption - Teil 1: Sauerstoff (Determination of impurity Content in silicon by Infrared Absorption - Part 1: oxygen)

50438-2 — Bestimmung des Verunreinigungsgehaltes in Silicium mittels Infrarot-Absorption; Kohlenstoff (Determination of Impurity Content in Silicon by infrared Absorption; Carbon)

50441-1 — Messung der geometrischen Dimensionen von Halbleiterscheiben - Teil 1: Dicke und Dickenvariation (Determination of the Geometric Dimensions of Semiconductor Wafers; Part 1: Measurement of Thickness)

2 Deutches Institut für Normung e.V., Beuth Verlag GmbH, Burggrafenstrasse 4-10, D-10787 Berlin, Germany

3.4 *ASQC standard*[3]

ANSI/ASQC Z1.4 — Sampling Procedures and Tables for Inspection by Attributes

3.5 *JEIDA standard*[4]

JEIDA-53 — Test Method for Carrier Recombination Lifetime in Silicon Wafers by Measurement of Photoconductivity Decay by Microwave Reflectance

NOTE 2: As listed or revised, all documents shall be the latest publications of adopted standards.

4 Terminology

4.1 *dopant* — A chemical element, usually from the third or fifth columns of the periodic table, incorporated in trace amounts in a semiconductor crystal to establish its conductivity type and resistivity. Common doping elements are boron and phosphorous.

4.2 *lot* — For the purposes of this document, (a) all of the wafers of nominally identical size and characteristics contained in a single shipment, or (b) subdivisions of large shipments consisting of wafers as listed above which have been identified by the supplier as constituting a lot.

4.3 *monocrystalline* — (synonym: single crystal) A body of crystalline material that contains no large-angle boundaries or twin boundaries.

4.4 *multicrystalline* — A body of crystalline material that contains large-angle boundaries or twin boundaries. Most crystals of this body have dimensions in the millimeter up to centimeter range.

5 Ordering Information

5.1 Purchase orders for silicon wafers furnished to this specification shall include the following items:

5.1.1 Nominal dimensions,

5.1.2 Either monocrystalline or multicrystalline,

5.1.3 Crystal growth method,

5.1.4 Surface orientation, crystal planes for monocrystalline wafers

5.1.5 Conductivity type and dopant,

NOTE 3: The dopant is difficult to ascertain in the finished wafers. Verification test procedures or certification (see Section 9) shall be agreed upon between the supplier and the purchaser.

5.1.6 Resistivity or resistivity range,

3 American Society for Quality Control, 611 East Wisconsin Avenue, Milwaukee, WI 53202

4 Japan Electronic Industry Development Association, 3-5-8 Shibakoen, Minato-ku, Tokyo 105, Japan

5.1.7 Lot acceptance procedures (see Section 6.4),

5.1.8 Certification (if required) (see Section 8),

5.1.9 Packing and marking (see Section 9),

5.1.10 Selection of test method to be used in evaluating those items for which alternate tests exist (see Section 7), and

5.1.11 Carbon and oxygen content.

5.2 Optional criteria. The following items may be specified optionally in addition to those listed above:

NOTE 4: Items in Paragraph 5.2 are less commonly specified than the others, but are included for completeness as parameters for which methods of evaluation have been developed.

5.2.1 Impurities other than common doping elements,

5.2.2 Diffusion length, and

5.2.3 Minority carrier lifetime.

NOTE 5: Up to now diffusion length and minority carrier lifetime cannot be measured with sufficient inter-laboratory accuracy. Subsequent recommendations, following lifetime round robin experiments, will be available in the future and will be presented in an addendum to this standard.

Even in the case of comparable and reproducible lifetime and diffusion length measurements, the measured characteristics must be regarded as an indication for solar cell efficiency. There is no general relation between initial minority carrier lifetime and solar cell efficiency as other parameters such as carbon or oxygen content will also influence the wafer in the solar cell process. However, in practical cases a dependence between minority carrier lifetime and solar cell efficiency can be found for a fixed solar cell process and a certain silicon wafer material. If one of them is changed the relation between them is suspect to change too.

6 Requirements

6.1 *Dimensions and Permissible Variations*

6.1.1 *Wafer Thickness and Variation*

6.1.1.1 Wafer thickness is typically 330 micrometer in 1999. In the future wafers should be specified in 50 micrometer intervals in the range between 150 and 400 micrometers.

6.1.1.2 The variation of wafer thickness in a lot as measured according to 7.2 at the center point of each wafer will be less than 15% of the specified wafer thickness.

6.1.2 *Rectangular Mainly Square Wafer Dimensions* — Depending upon the wafer type, one of the sections 6.1.2.1, 6.1.2.2 or 6.1.2.3 applies.

6.1.2.1 *Square Crystalline Silicon Wafer Dimensions*

6.1.2.1.1 *Physical dimensions* — See Figure 1, Table 2

Rectangular cells are permitted as long as the measures of A and B are according to the nominal size measures in Table 2.

Example: A = 100 mm, B = 150 mm.

Dimension D (identical for all sizes) min = 0.5 mm, max = 2.0 mm. By bilateral agreement, one corner can be of different angle and size to indicate the orientation of the wafer.

Squareness: The wafer will fit inside a square of the maximum dimension A and contain a square of the minimum dimension A.

6.1.2.1.2 TTV: 50 micrometer.

6.1.2.2 *Circular Monocrystalline Photovoltaic Solar Cell Silicon Wafers*

6.1.2.2.1 Diameters (mm): 100, 125, 150, 175, 200: Variation in diameter: ± 1 mm all sizes

6.1.2.2.2 TTV: 30 micrometer.

6.1.2.2.3 Warp: 75 micrometer.

6.1.2.3 *Pseudo-Square Monocrystalline Photovoltaic Solar Cell Silicon Wafers*

6.1.2.3.1 Physical dimensions: See Figure 2, Table 3

6.1.2.3.2 TTV: 30 micrometer.

6.1.2.3.3 Warp: 75 micrometer.

6.2 *Materials and Manufacture*

6.2.1 The material shall consist of wafers conforming to the structural class specified in the purchase order or contract.

6.3 *Physical Parameters*

6.3.1 The material shall conform to the crystallographic orientation details as specified in the purchase order or contract.

6.3.2 The material shall conform to the details specified in the purchase order or contract, as follows:

6.3.2.1 Conductivity type and dopant (see Note 3),

6.3.2.2 Resistivity,

6.3.2.3 Amounts of impurities other than common dopants (such as phosphorous, boron), especially oxygen and carbon content (optional),

6.3.2.4 Diffusion length (optional), and

6.3.2.5 Minority-carrier lifetime (optional).

6.4 *Wafer defect limits* — See Table 1.

Table 1 Wafer Defect Limits

Item	*Characteristics**	*Max Defect Limits*	*Notes*
1	Saw Marks	20 µm TIR	1
2	Area Contamination	To be determined	
3	Edge Chips/Indents	2 per wafer max up to l mm wide and l mm deep	2
4	Cracks/crow's feet	None	

* Characteristics are defined in SEMI M1, Section 10.

NOTE 1: The outer l mm (0.040") is excluded from these criteria.

NOTE 2: Excluding conchoidal chips.

6.5 *Sampling*

6.5.1 Unless otherwise specified, Practice E 122 shall be used.

6.5.1.1 When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) and lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL and LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

7 Test Methods

NOTE 6: Silicon wafers are extremely fragile. While the mechanical dimensions of a wafer can be measured by use of tools such as micrometer calipers and other conventional techniques, the wafer may be damaged physically in ways that are not immediately evident. Special care must therefore be used in the selection and execution of measurement methods.

7.1 *Length, Width, or Diameter* — Determine the diameter of circular wafers in accordance with ASTM Test Method F 613. Determine the side length of square wafers by a method agreed upon between the supplier and the purchaser.

7.2 *Thickness, Center Point* — Determine in accordance with ASTM Test Methods F 533 or DIN 50441-1.

7.3 *Thickness Variation* — Determine in accordance with ASTM Test Methods F 533 or F 657.

7.4 *Structural Class* — Determine the structural class by a method agreed upon between the supplier and the purchaser.

7.5 *Surface Orientation* — Determine in accordance with ASTM Test Methods F 26 or DIN 50433-1, DIN 50433-2 and DIN 50433-3.

7.6 *Conductivity Type* — Determine in accordance with ASTM Test Methods F 42 or DIN 50432.

7.7 *Resistivity* — Determine by methods agreed upon between the supplier and the purchaser.

NOTE 7: Resistivity of wafers is most appropriately determined for referee purposes by ASTM Method F 84 or DIN 50431. Reliable measurements with these methods can only be made in regions of a wafer which contain no grain boundaries; these methods are therefore not appropriate for multicrystalline material. Under some circumstances these tests may be considered destructive, and an alternative means may be required. One non-destructive test is ASTM Test method F 673, having a range from 0.001 to 100 Ω-cm. This method is relatively insensitive to the presence of grain boundaries and is recommended for all material types. Another nondestructive test is ASTM Test Method F 398. This method is limited to carrier concentrations in the ranges from 1.5×10^{18} cm^{-3} to 1.5×10^{21} cm^{-3} for n-type silicon and from 3×10^{18} cm^{-3} to 5×10^{20} cm^{-3} for p-type, and has only moderate inter-laboratory precision. Other available methods include ASTM Test methods F 43 or DIN 50430 (referee methods requiring a bar-shaped sample).

7.8 *Other Impurities* — Determine by methods agreed upon between the supplier and the purchaser.

NOTE 8: ASTM Test Methods F 1188, F 1619 and DIN 50438-1 are specific tests for oxygen. ASTM F 1391 and DIN 50438-2 are specific tests for carbon; special thick test specimens are necessary.

7.9 *Minority Carrier Diffusion Length* — Determine by methods agreed upon between the supplier and the purchaser.

NOTE 9: Methods for minority carrier diffusion length are listed in ASTM F 391.

7.10 *Minority Carrier Lifetime* — Determine by methods agreed upon between the supplier and the purchaser.

NOTE 10: Methods for minority carrier lifetime measurements are given in ASTM F 28 (bulk material), ASTM F 1535 (wafers) and JEIDA-53 (wafers). As the wafer methods measure an effective lifetime, the sample preparation (surface passivation) and measurement conditions will influence the results and must be considered.

8 Certification

8.1 Upon request of the purchaser in the contract or order, a manufacturer's or supplier's certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

8.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material shall be certified as 'capable of meeting' certain requirements. In this context, 'capable of meeting' shall signify that the supplier is not required to perform the appropriate tests in Section 7. However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

9 Packing and Package Labeling

9.1 Special packing requirements shall be subject to agreement between the supplier and the purchaser. Otherwise all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination, and in accordance with the best industry practices to provide ample protection against damage during shipment.

9.2 The wafers supplied under these specifications shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Identification shall include as a minimum the nominal diameter, conductivity type, dopant, orientation, resistivity range, and lot number. The lot number, either (1) assigned by the original manufacturer of the wafers, or (2) assigned subsequent to wafer manufacture but providing reference to the original lot number, shall provide easy access to information concerning the fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer's facility for at least one year after that particular lot has been accepted by the purchaser.