实验报告

计算机科学与技术

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1、新增指令

1.1 R型指令

R-type = op(6) + rs(5) + rt(5) + rd(5) + shamt(5) + funct(6)

- mfhi : GPR[rd] = HI
- mflo : GPR[rd] = LO
- mthi : HI = GPR[rs]
- mtlo : LO = GPR[rs]
- mult : (HI, LO) = GPR[rs] * GPR[rt] (signed)
- multu : (HI, LO) = GPR[rs] * GPR[rt] (unsigned)
- div : (HI, LO) = GPR[rs] / GPR[rt] (signed)
- divu : (HI, LO) = GPR[rs] / GPR[rt] (unsigned)
- sllv : GPR[rd] = GPR[rt] << GPR[rs][4:0] (logical)
- srav : GPR[rd] = GPR[rt] >> GPR[rs][4:0] (arithmetic)
- srlv : GPR[rd] = GPR[rt] >> GPR[rs][4:0] (logical)
- jalr: GPR[rd] = pc + 8, pc = GPR[rs]

1.2 I型指令

I-type = op(6) + rs(5) + rt(5) + imm(16)

- bgtz : if(GPR[rs] > 0) pc += 4 + imm << 2
- blez : if(GPR[rs] <= 0) pc += 4 + imm << 2
- bgez : if(GPR[rs] >= 0) pc += 4 + imm << 2
- bgezal : if(GPR[rs] >= 0) GPR[31] = pc + 8, pc += 4 + imm << 2
- bltz : if(GPR[rs] < 0) pc += 4 + imm << 2
- bltzal : if(GPR[rs] < 0) GPR[31] = pc + 8, pc += 4 + imm << 2
- lb : GPR[rt] = sign_ext((byte)mem[GPR[rs] + offset])

- lbu : GPR[rt] = zero_ext((byte)mem[GPR[rs] + offset])
- lh : GPR[rt] = sign_ext((halfword)mem[GPR[rs] + offset])
- lhu: GPR[rt] = zero_ext((halfword)mem[GPR[rs] + offset])
- sb : mem[GPR[rs] + offset] = (byte)GPR[rt]
- sh : mem[GPR[rs] + offset] = (halfword)GPR[rt]

2、修改记录

1. icode.svh：增加了新增指令的编码。
2. fetch阶段： 增加了对新跳转指令的支持。
3. decode阶段：将控制信号增加2位记录内存读写粒度，增加1位记录读内存符号扩展，增加4位记录HILO读写。增加对新增分支指令的判断。处理寄存器值作为shamt的情况。
4. execute阶段：增加mult单周期乘除法器。
5. memory阶段：增加mem_input、mem_extension模块，分别处理不同粒度的内存读写。
6. writeback阶段：增加hi、lo以及由hilo到寄存器的写逻辑。
7. hazard：增加内存延迟的阻塞。增加对hi、lo的转发。
8. VTop：加入地址翻译。
9. Mycore：针对上述修改增加数据通路。增加hilo用于读写hi、lo寄存器。

3、测试照片

3.1 verilator test1

```
srs@srs-virtual-machine:~/桌面/ICS-2021Spring-FDU$ make vsim TARGET=mycpu/VTop TEST=test1 -j
./build/gcc/mycpu/VTop/vmain  -m misc/nscscc/test1.coe -r misc/nscscc/test1.txt
(info) #1 completed.
(info) #2 completed.
(info) #3 completed.
(info) #4 completed.
(info) #5 completed.
(info) #6 completed.
(info) #7 completed.
(info) #8 completed.
(info) #9 completed.
(info) #10 completed.
(info) #11 completed.
(info) #12 completed.
(info) #13 completed.
(info) #14 completed.
(info) #15 completed.
(info) #16 completed.
(info) #17 completed.
(info) #18 completed.
(info) #19 completed.
(info) #20 completed.
(info) #21 completed.
(info) #22 completed.
(info) #23 completed.
(info) #24 completed.
(info) #25 completed.
(info) #26 completed.
(info) #27 completed.
(info) testbench finished in 173625 cycles (781.098 KHz).
```

3.2 verilator test1 延时

```
srs@srs-virtual-machine:~/桌面/ICS-2021Spring-FDU$ make vsim TARGET=mycpu/VTop TEST=test1 VSIM_ARGS='-p 0.99'
./build/gcc/mycpu/VTop/vmain -p 0.99 -m misc/nscscc/test1.coe -r misc/nscscc/test1.txt
(info) #1 completed.
(info) #2 completed.
(info) #3 completed.
(info) #4 completed.
(info) #5 completed.
(info) #6 completed.
(info) #7 completed.
(info) #8 completed.
(info) #9 completed.
(info) #10 completed.
(info) #11 completed.
(info) #12 completed.
(info) #13 completed.
(info) #14 completed.
(info) #15 completed.
(info) #16 completed.
(info) #17 completed.
(info) #18 completed.
(info) #19 completed.
(info) #20 completed.
(info) #21 completed.
(info) #22 completed.
(info) #23 completed.
(info) #24 completed.
(info) #25 completed.
(info) #26 completed.
(info) #27 completed.
(info) testbench finished in 11655357 cycles (1.328 MHz).
```

3.3 verilator test2

```
srs@srs-virtual-machine:~/桌面/ICS-2021Spring-FDU$ make vsim TARGET=mycpu/VTop TEST=test2
./build/gcc/mycpu/VTop/vmain  -m misc/nscscc/test2.coe -r misc/nscscc/test2.txt
(info) #1 completed.
(info) #2 completed.
(info) #3 completed.
(info) #4 completed.
(info) #5 completed.
(info) #6 completed.
(info) #7 completed.
(info) #8 completed.
(info) #9 completed.
(info) #10 completed.
(info) #11 completed.
(info) #12 completed.
(info) #13 completed.
(info) #14 completed.
(info) #15 completed.
(info) #16 completed.
(info) #17 completed.
(info) testbench finished in 179919 cycles (770.337 KHz).
```

3.4 verilator test2 延时

```
srs@srs-virtual-machine:~/桌面/ICS-2021Spring-FDU$ make vsim TARGET=mycpu/VTop TEST=test2 VSIM_ARGS='-p 0.99'
./build/gcc/mycpu/VTop/vmain -p 0.99 -m misc/nscscc/test2.coe -r misc/nscscc/test2.txt
(info) #1 completed.
(info) #2 completed.
(info) #3 completed.
(info) #4 completed.
(info) #5 completed.
(info) #6 completed.
(info) #7 completed.
(info) #8 completed.
(info) #9 completed.
(info) #10 completed.
(info) #11 completed.
(info) #12 completed.
(info) #13 completed.
(info) #14 completed.
(info) #15 completed.
(info) #16 completed.
(info) #17 completed.
(info) testbench finished in 12073878 cycles (1.320 MHz).
```

3.5 verilator test3

```
srs@srs-virtual-machine:~/桌面/ICS-2021Spring-FDU$ make vsim TARGET=mycpu/VTop TEST=test3
./build/gcc/mycpu/VTop/vmain  -m misc/nscscc/test3.coe -r misc/nscscc/test3.txt
(info) #1 completed.
(info) #2 completed.
(info) #3 completed.
(info) #4 completed.
(info) #5 completed.
(info) #6 completed.
(info) #7 completed.
(info) #8 completed.
(info) #9 completed.
(info) testbench finished in 40059 cycles (662.094 KHz).
```

3.6 verilator test3 延时

```
srs@srs-virtual-machine:~/桌面/ICS-2021Spring-FDU$ make vsim TARGET=mycpu/VTop TEST=test3 VSIM_ARGS='-p 0.99'
./build/gcc/mycpu/VTop/vmain -p 0.99 -m misc/nscscc/test3.coe -r misc/nscscc/test3.txt
(info) #1 completed.
(info) #2 completed.
(info) #3 completed.
(info) #4 completed.
(info) #5 completed.
(info) #6 completed.
(info) #7 completed.
(info) #8 completed.
(info) #9 completed.
(info) testbench finished in 2684291 cycles (1.319 MHz).
```

3.7 vivado test1 仿真

```
        [13982000 ns] Test is running, debug_wb_pc = 0xbfc06b28
        [13992000 ns] Test is running, debug_wb_pc = 0xbfc06bcc
 ----[13995565 ns] Number 8'd27 Functional Test Point PASS!!!
        [14002000 ns] Test is running, debug_wb_pc = 0xbfc009ac
        [14012000 ns] Test is running, debug_wb_pc = 0xbfc00964
 ================================================================
 Test end!
 ----PASS!!!
 $finish called at time : 14012296500 ps : File "C:/Users/Dell/Desktop/ICS-2021Spring-FDU/vivado/test1/soc_axi_func/testbench/mycpu_tb.v" Line 269
) run: Time (s): cpu = 00:02:22 ; elapsed = 00:03:20 . Memory (MB): peak = 4876.746 ; gain = 0.000
```

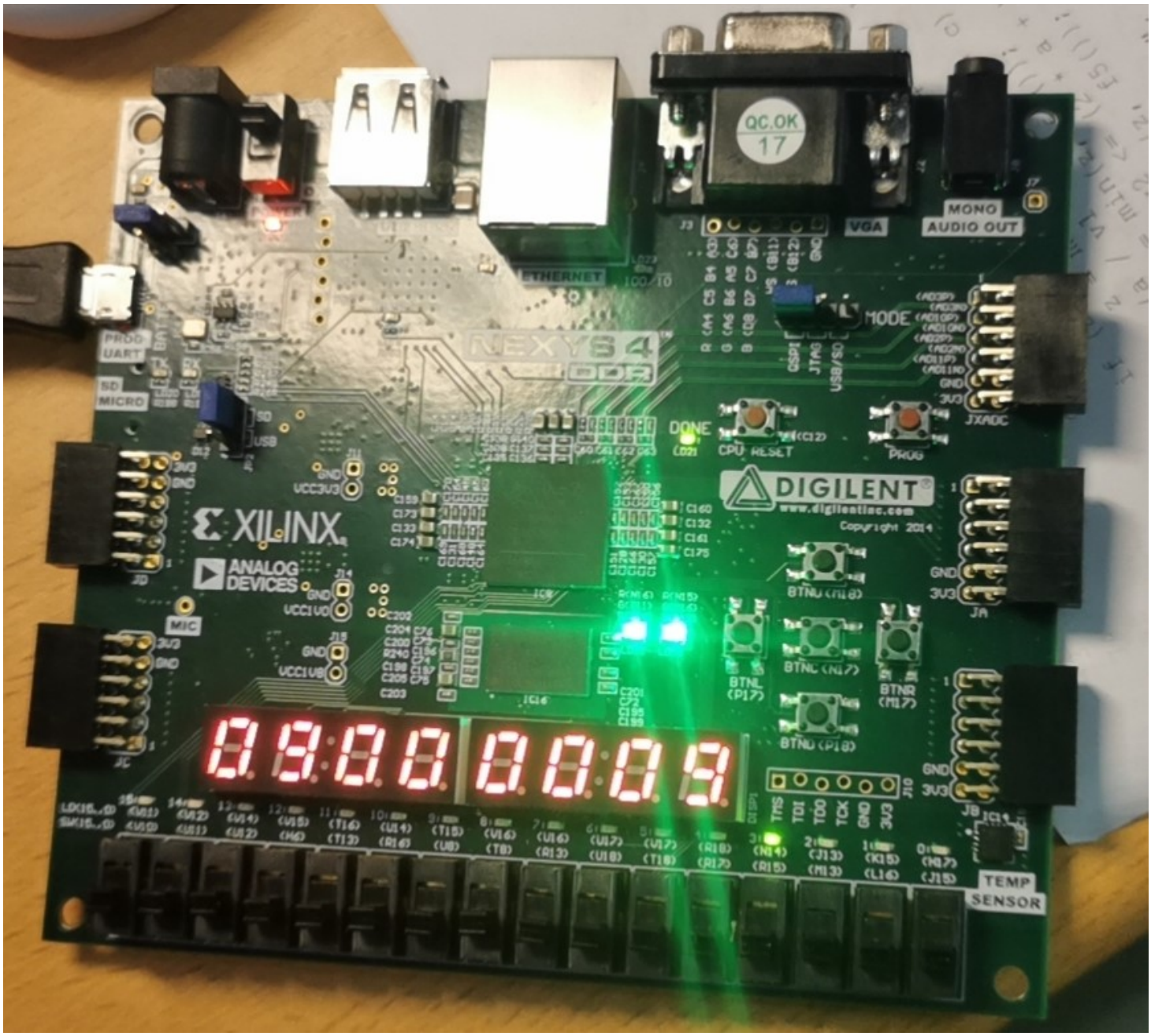
3.8 vivado test2 仿真

```
        [14512000 ns] Test is running, debug_wb_pc = 0xbfc39ca0
 ----[14517215 ns] Number 8'd17 Functional Test Point PASS!!!
        [14522000 ns] Test is running, debug_wb_pc = 0xbfc008f4
        [14532000 ns] Test is running, debug_wb_pc = 0xbfc008b8
 ================================================================
 Test end!
 ----PASS!!!
 $finish called at time : 14533949500 ps : File "C:/Users/Dell/Desktop/ICS-2021Spring-FDU/vivado/test2/soc_axi_func/testbench/mycpu_tb.v" Line 269
) run: Time (s): cpu = 00:02:15 ; elapsed = 00:03:25 . Memory (MB): peak = 4349.777 ; gain = 0.000
```

3.9 vivado test3 仿真

```
        [3182000 ns] Test is running, debug_wb_pc = 0xbfc00df4
        [3192000 ns] Test is running, debug_wb_pc = 0xbfc00e98
        [3202000 ns] Test is running, debug_wb_pc = 0xbfc00f40
        [3212000 ns] Test is running, debug_wb_pc = 0xbfc00fe4
 ----[3217075 ns] Number 8'd09 Functional Test Point PASS!!!
        [3222000 ns] Test is running, debug_wb_pc = 0xbfc00874
        [3232000 ns] Test is running, debug_wb_pc = 0xbfc00838
 ================================================================
 Test end!
 ----PASS!!!
 $finish called at time : 3233803500 ps : File "C:/Users/Dell/Desktop/ICS-2021Spring-FDU/vivado/test3/soc_axi_func/testbench/mycpu_tb.v" Line 269
) run: Time (s): cpu = 00:00:35 ; elapsed = 00:00:49 . Memory (MB): peak = 4876.746 ; gain = 0.000
```

3.10 上板



4、ToDo

1. 多周期乘除法器
2. 修改数据通路，用结构体规整数据传递格式
3. 仲裁器
4. 在CPU上运行程序