

1. Description

1.1. Project

Project Name	ped_box
Board Name	custom
Generated with:	STM32CubeMX 6.12.1
Date	11/17/2024

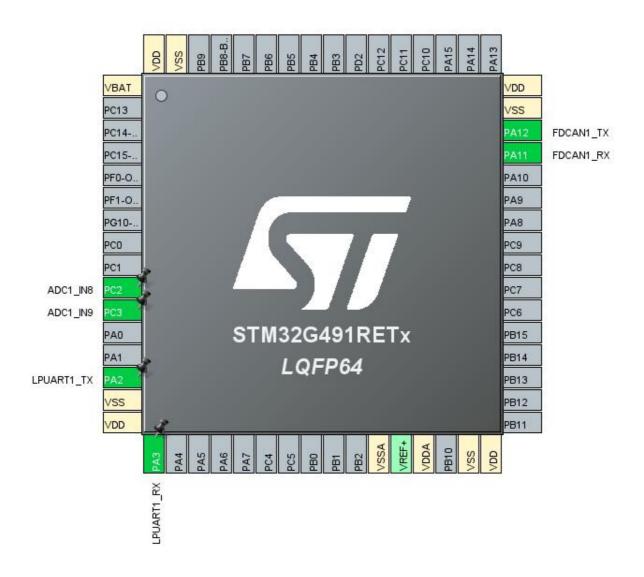
1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G491RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M4

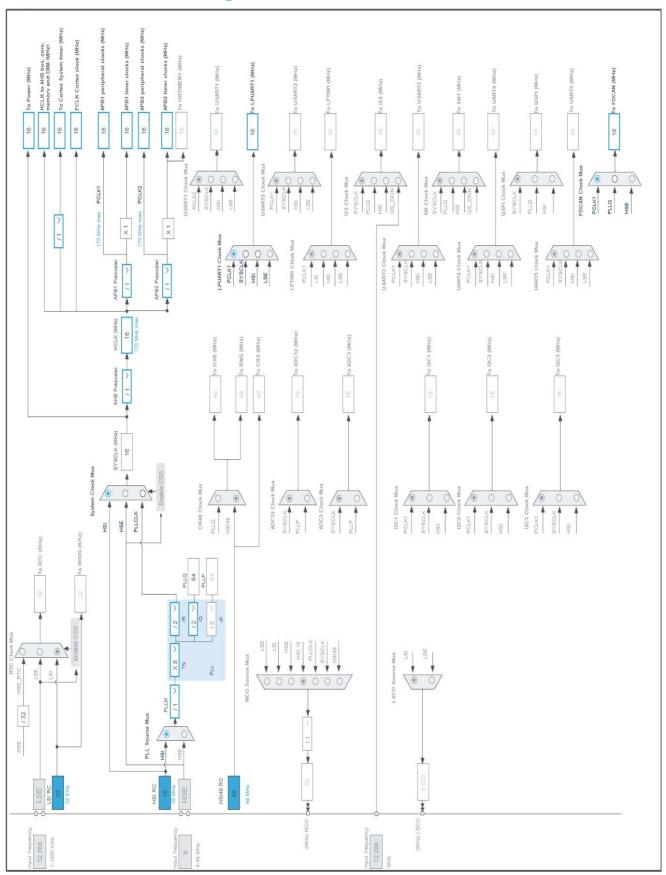
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
10	PC2	I/O	ADC1_IN8	
11	PC3	I/O	ADC1_IN9	
14	PA2	I/O	LPUART1_TX	
15	VSS	Power		
16	VDD	Power		
17	PA3	I/O	LPUART1_RX	
27	VSSA	Power		
29	VDDA	Power		
31	VSS	Power		
32	VDD	Power		
45	PA11	I/O	FDCAN1_RX	
46	PA12	I/O	FDCAN1_TX	
47	VSS	Power		
48	VDD	Power		
63	VSS	Power		
64	VDD	Power		

4. Clock Tree Configuration



Page 4

1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
мси	STM32G491RETx
Datasheet	DS13122_Rev1

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

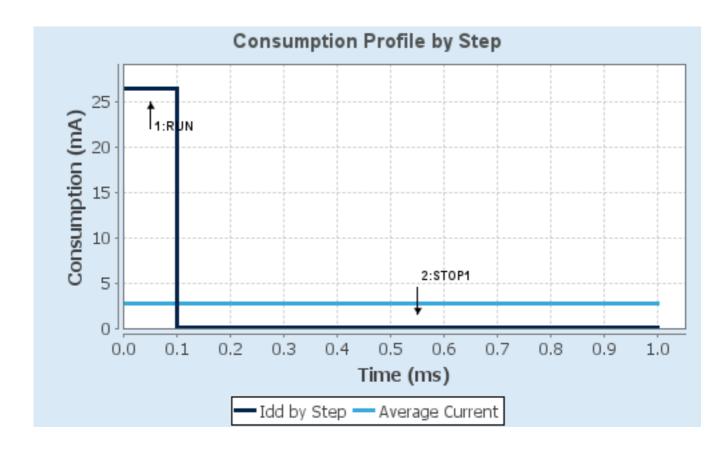
1.4. Sequence

_		
Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	LSE LowDrive RTC
Clock Source Frequency	4 MHz	32.768 kHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	26.4 mA	57.3 μA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	146.08	149.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.69 mA
Battery Life	1 month, 22 days,	Average DMIPS	212.5 DMIPS
	3 hours		

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	ped_box
Project Folder	C:\Users\kehrenj\STM32CubeIDE\workspace_1.16.1\ped_box
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.6.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	Yes
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_FDCAN1_Init	FDCAN1
5	MX_LPUART1_UART_Init	LPUART1

3. Peripherals and Middlewares Configuration

3.1. ADC1

IN8: IN8 Single-ended IN9: IN9 Single-ended

mode: Temperature Sensor Channel

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler Synchronous clock mode divided by 2

Resolution ADC 12-bit resolution

Data Alignment Right alignment

Gain Compensation 0

Scan Conversion Mode Disabled

Low Power Auto Wait Disabled

Continuous Conversion Mode Enabled *

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

Overrun behaviour Overrun data preserved

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable
Enable Regular Oversampling Disable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel 8
Sampling Time 2.5 Cycles
Offset Number No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

3.2. FDCAN1

mode: Activated

3.2.1. Parameter Settings:

Basic Parameters:

Clock Divider Divide kernel clock by 1

Frame Format Classic mode Mode Normal mode Auto Retransmission Disable Transmit Pause Disable Disable Protocol Exception Nominal Sync Jump Width 1 Data Prescaler 1 Data Sync Jump Width Data Time Seg1 Data Time Seg2

0

Tx Fifo Queue Mode FIFO mode

Bit Timings Parameters:

Std Filters Nbr

Ext Filters Nbr

Nominal Prescaler 1 *

Nominal Time Quantum 62.5 *
Nominal Time Seg1 13 *
Nominal Time Seg2 2
Nominal Time for one Bit 1000

Nominal Baud Rate 1000000 *

3.3. LPUART1

Mode: Asynchronous

3.3.1. Parameter Settings:

Basic Parameters:

Baud Rate 115200 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Single Sample Disable

ClockPrescaler 1

Fifo Mode FIFO mode disable

Txfifo Threshold 1 eighth full configuration

Rxfifo Threshold 1 eighth full configuration

Advanced Features:

TX Pin Active Level Inversion Disable
RX Pin Active Level Inversion Disable
Data Inversion Disable
TX and RX pins Swapping Disable
Overrun Enable
DMA on RX Error Enable
MSB First Disable

3.4. RCC

3.4.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 64
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration TRUE

3.5. SYS

Timebase Source: SysTick

mode: save power of non-active UCPD - deactive Dead Battery pull-up

ped_	box	Pro	ject
Configura	ation	Re	port

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
ADC1	PC2	ADC1_IN8	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
FDCAN1	PA11	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
FDCAN1 interrupt 0	true	0	0
FDCAN1 interrupt 1	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupt	unused		
FPU global interrupt	unused		
LPUART1 global interrupt	unused		

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
FDCAN1 interrupt 0	false	true	true
FDCAN1 interrupt 1	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

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BSDL files https://www.st.com/resource/en/bsdl_model/stm32g4_bsdl.zip

IBIS models https://www.st.com/resource/en/ibis_model/stm32g4_ibis.zip

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