Package Model RLCK Extraction

Prerequisites

Before you can start you must enable the Package Model Extraction tool through the ADS App Manager under the ADS Main Window Tools menu. In the Application and Add-on manager enable the Package RLCK Extraction entry.

When you restart ADS this will add the Package Model Extraction capability under the Add-Ons menu in both Layout and Schematic windows.

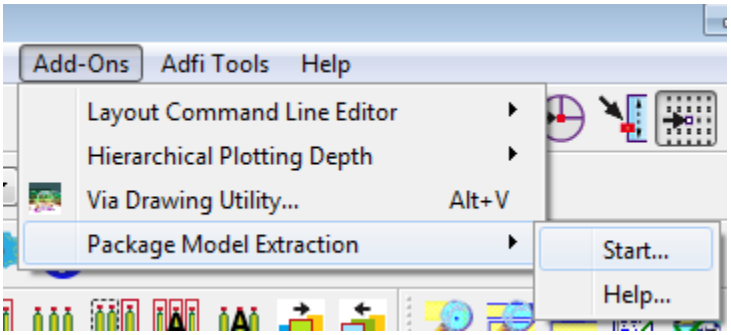

Figure 1 Add-Ons menu with Package Model Extraction sub menu

Before you can use the tool in ADS in RFIC Interoperability mode you need to make sure that you have the Cadence Virtuoso libraries analogLib and basic library available in your ADS workspace. These two libraries can be found on any unix installation of Cadence Virtuoso:

- <Cadence Virtuoso IC tools install directory>/tools/dfII/etc/cdslib/basic
- <Cadence Virtuoso IC tools install directory>/tools/dfII/etc/cdslib/artist/analogLib

The analogLib library needs to be updated for ADS usage through the Build ADS analogLib… command under the ADS Main Window Tools menu. Once this is done you can add these two libraries in read only mode to your ADS workspace using the DesignKits → Manage Libraries… menu as shown in figure 2.

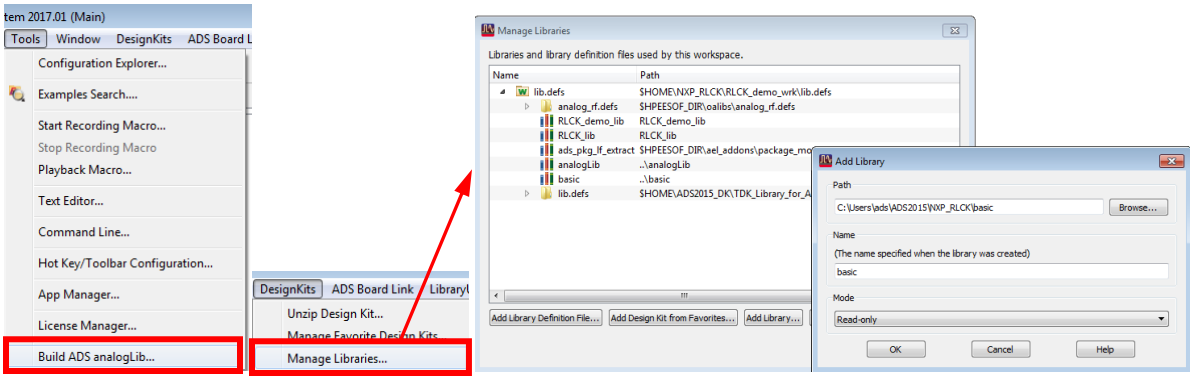

Figure 2 Build analogLib and analogLib and basic lib to your workspace libraries through ADS library management

In addition interoperable operation requires an RFIC Interoperable License in ADS.

Using the extraction tool

The Package Model RLCK Extraction tool allows to create a low frequency RLCK model from S-parameter data representing the package interconnect. It models the structure as a series RL block followed by a parallel GC block to ground. In between the RL and GC block the interconnect block W models the fan out from in to outputs. Mutual coupling between the different branches is taken into account.

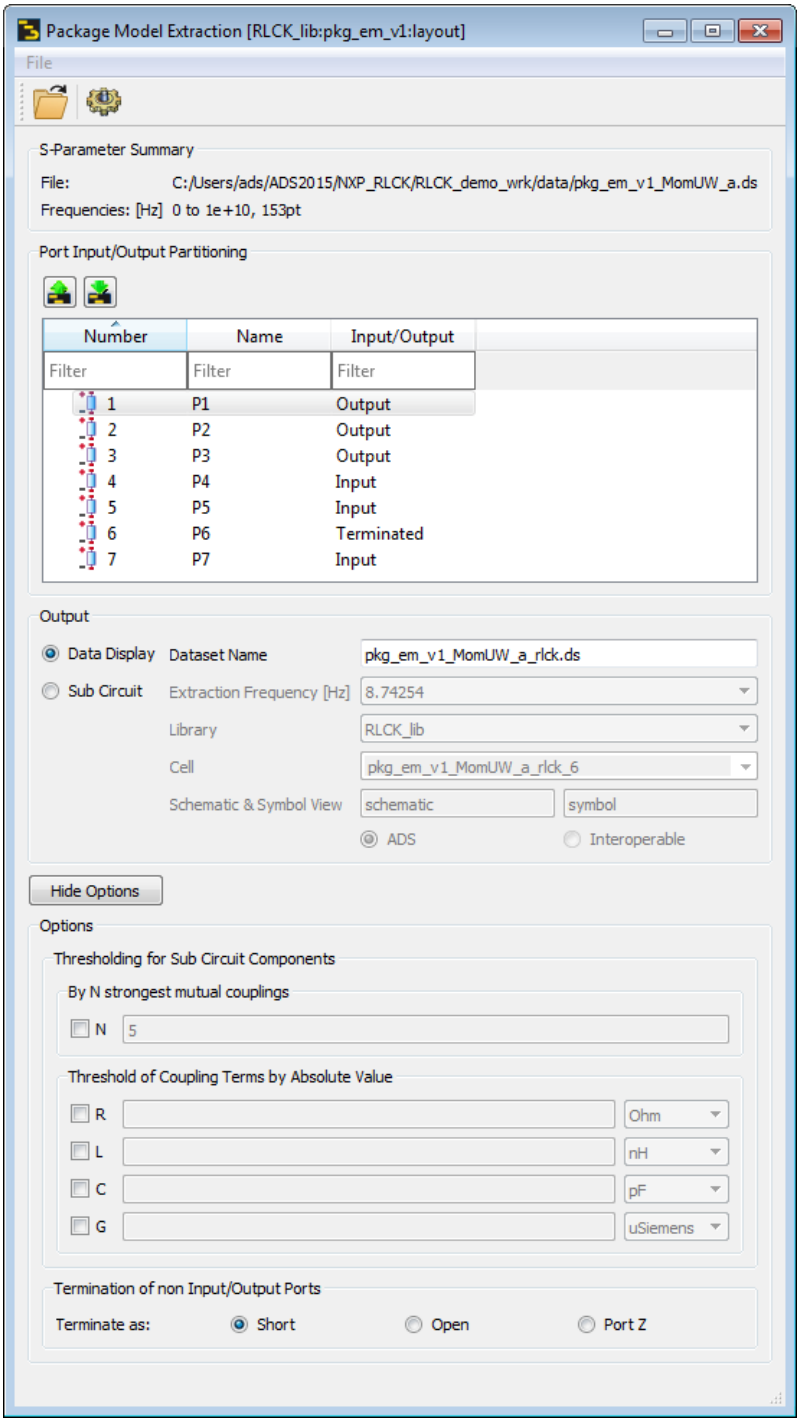

Figure 3 Package extraction user interface

The File->Open menu or File icon opens a file browser to select an S parameter model of your package in dataset, touchstone or citi file format. Once an S-parameter file is selected the interface is populated with the initial data.

The summary shows basic info about the selected dataset such as name and number of available frequency points.

The Port Input/Output Partitioning portions allows you to specify the input output of the target package. Input/Ouput can be specified by the available ports in the S-parameter and will be used in modeling process.

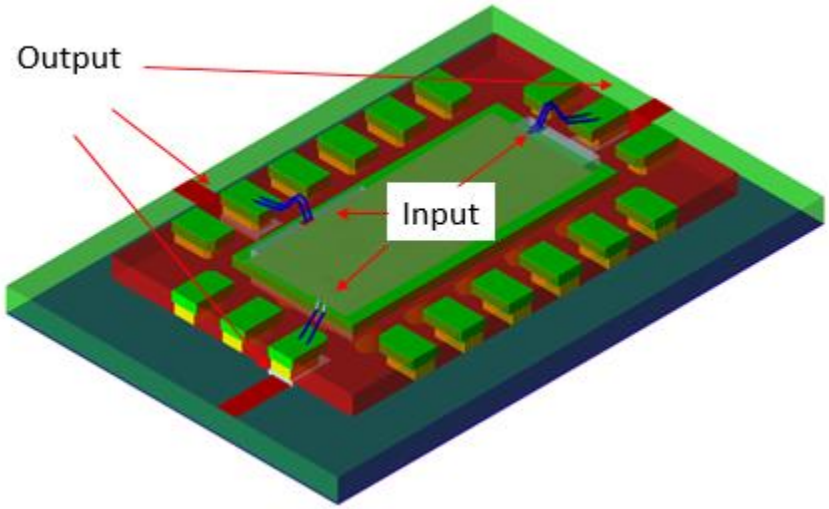

Figure 4 Example package: die ports are usually specified as input, package pin ports are typically outputs.

When port names are available the names are picked from the S-parameter file. When no port names exist, P1 up to Pn is used with n the number of ports in the file.

The third column shows the I/O behavior you have for the design. This can be defined by the layout you used to start the tool when the port specification matches your dataset. When no match exist the third column will initially only show Terminated. For a valid setup you need to have at least 1 Input and 1 Output port. Normally all ports need to be correctly defined. This can be done by picking up the info from a layout's port configuration through the left arrow icon. The right icon allows you to update the layout's configuration from the RLCK extraction UI.

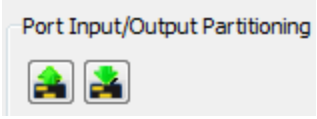

Figure 5 Load or save a port Input/Ouput configuration from or to the parent layout window

The drop down on each Input/Ouput cell, or the context menu on a set of selected ports allows you to update the Input/Ouput configurations for one or more pins. Terminated pins will not be maintained in

the extracted output. These non Input/Output ports will be terminated with either shorted, left open or terminated with the reference impedance of the terminated ports. The options below allow to choose that.

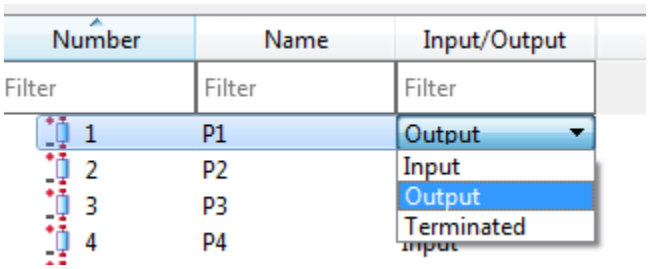

Figure 6 Individual port configuration through drop down selection

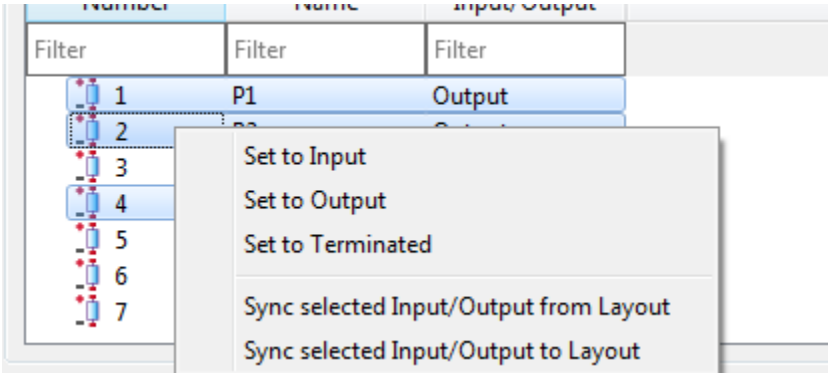

Figure 7 Multiple port configuration through context menu on right mouse click

The Output section allows you to specify the output of the RLCK extraction tool when hitting the Run icon. You have the choice between a Data Display with the RLCK fit for all frequencies of the original dataset or a schematic created for a specific extraction frequency available in the S-parameter data.

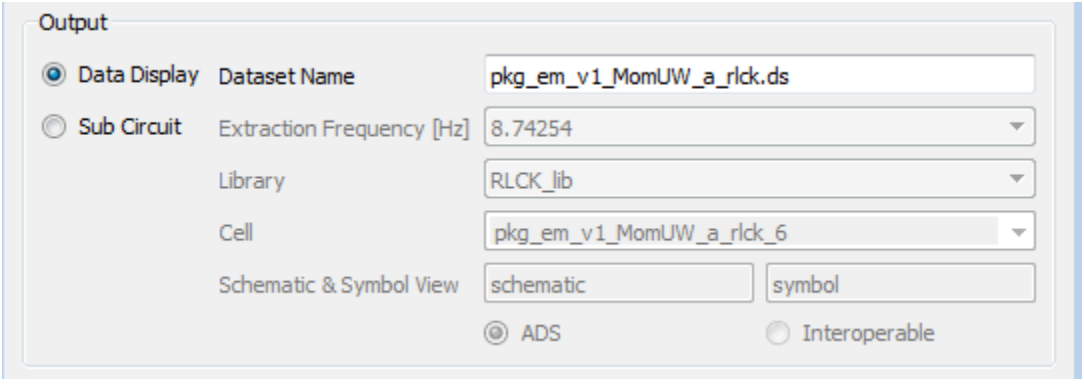

Figure 8 Output section of the extraction tool

When a Data Display is selected the Run action first creates a dataset that is shown directly in a Data Display with a specific template matching the output data. Page 1 allows to browse through the values at different frequencies. Only results for the specified Input/Output ports are retained. The terminated ports are eliminated using the specified termination. The Export to .csv file tab will dump the RLCK data at the selected frequency to 4 CSV files in the ADS workspace directory.

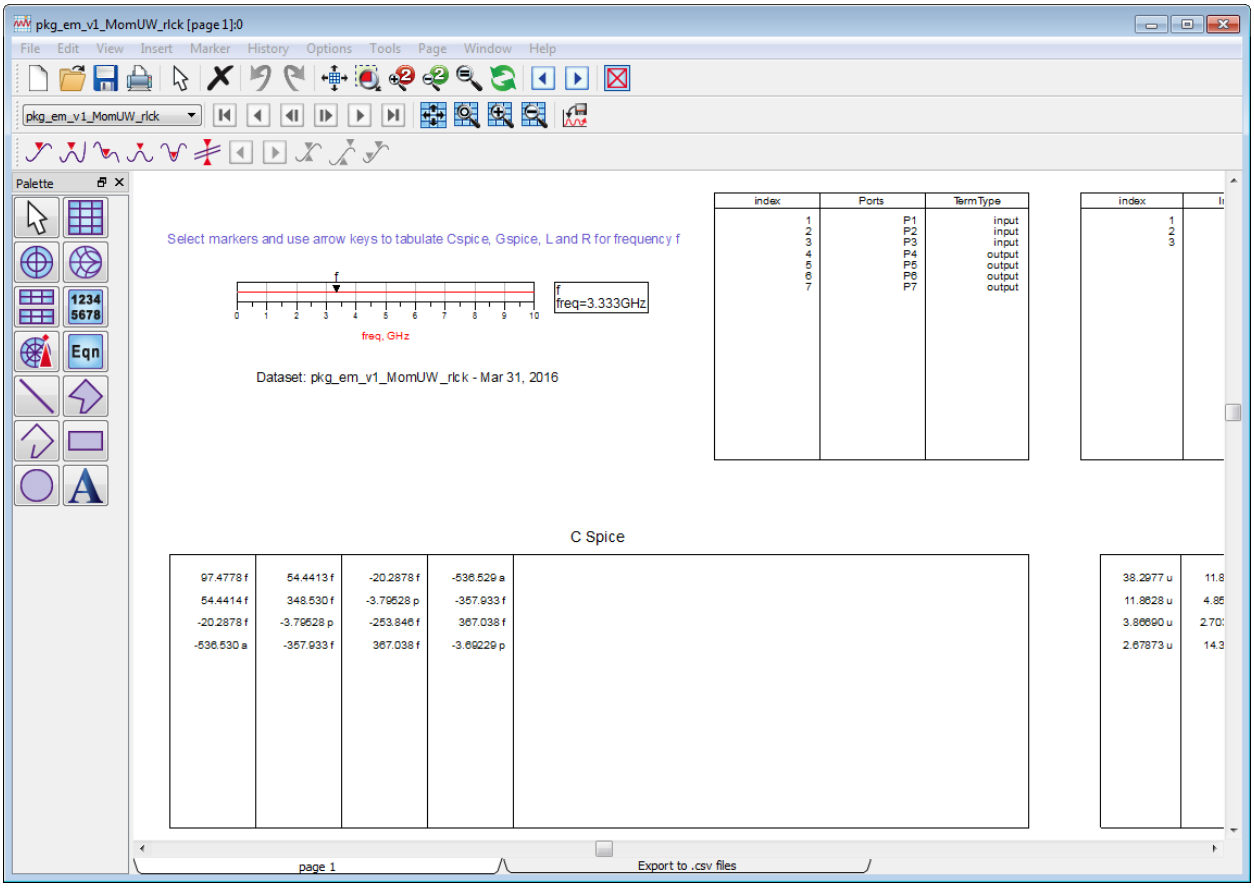

Figure 9 Data Display page using RLCK extraction template with extracted ... _rlck dataset

When Sub Circuit is selected the output of the tool is a schematic and symbol generated at the extraction frequency. You specify the library, cell, schematic view and symbol view for the output and the schematic format that needs to be used. By default the schematic uses components from the ads_rflib for simulation within ADS only. When the Interoperable option is selected the generation builds a schematic using components from Cadence Virtuoso analog and basic libraries that can be used immediately in the Virtuoso schematic environment. When you select design views that already exists the tool asks if it ok to overwrite them.

The Input ports of the schematic are placed on the left of the design. They are followed by the RL block consisting of the series R, L and mutual inductances and mutual resistances between the branches. When connections have fan out from input to output a W interconnect structure is place after the RL block. On the right side the Ouput ports are places connected with the GC block providing the parasitic capacitances and admittances to the ground (Ref) and parasitic capacitance and admittance between the Ouput ports.

When the number of ports on the design is large this densely coupled circuit with fully populated matrices becomes very large. This makes it slow to create. But much more importantly circuit simulations with this complex circuit can take up a lot of simulation resources. In general however most of the mutual couplings elements are very small and have little effect on the simulation results. They can be neglected without ill effects on the simulation results. The Options section allows to control the

dropping of the smallest elements by keeping only the largest n mutual couplings and/or ignoring off-diagonal elements below the certain absolute threshold values for the mutual resistance, mutual inductance, admittance and capacitance.

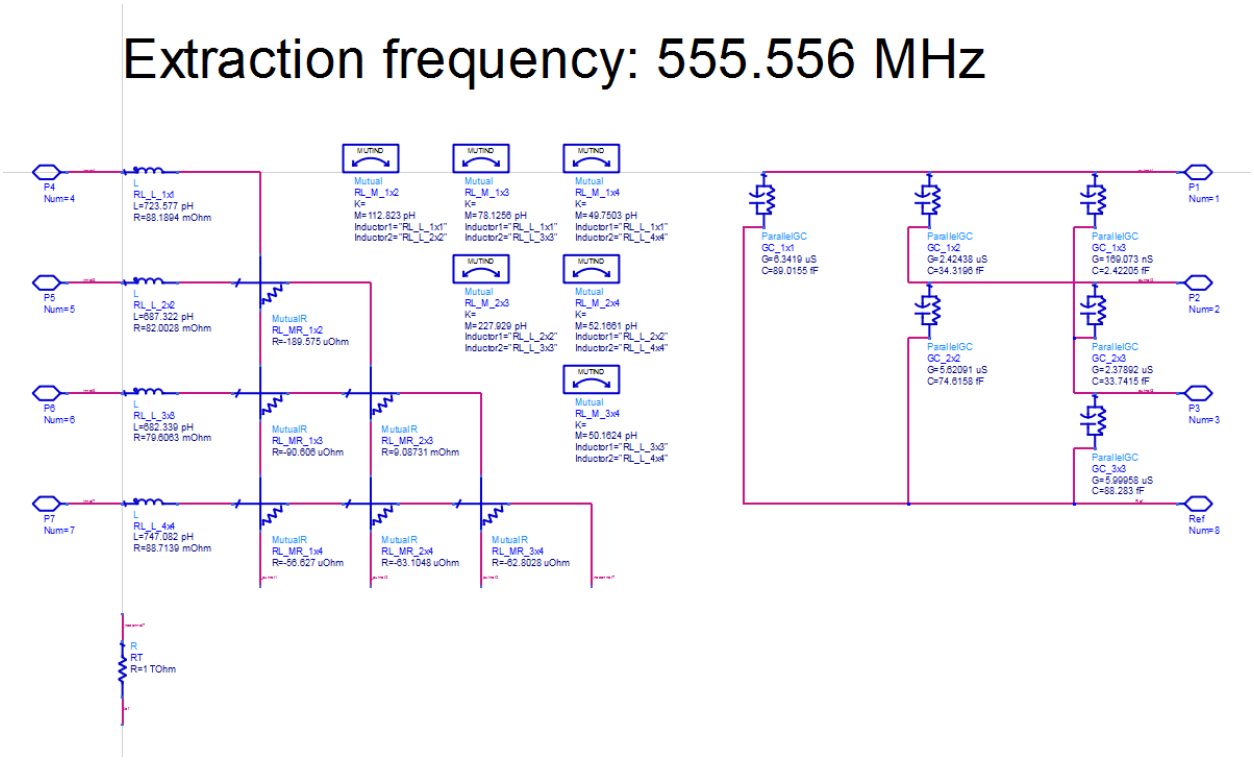

Figure 10 Example extracted schematic

A thresholding is only applied when enabled in the UI. The N setting is applied on individual R, L, G and C elements. When the absolute value threshold is also active the smallest number elements is kept. When the N value is set to 0 all off diagonal elements of the RL and GC matrices are ignored.

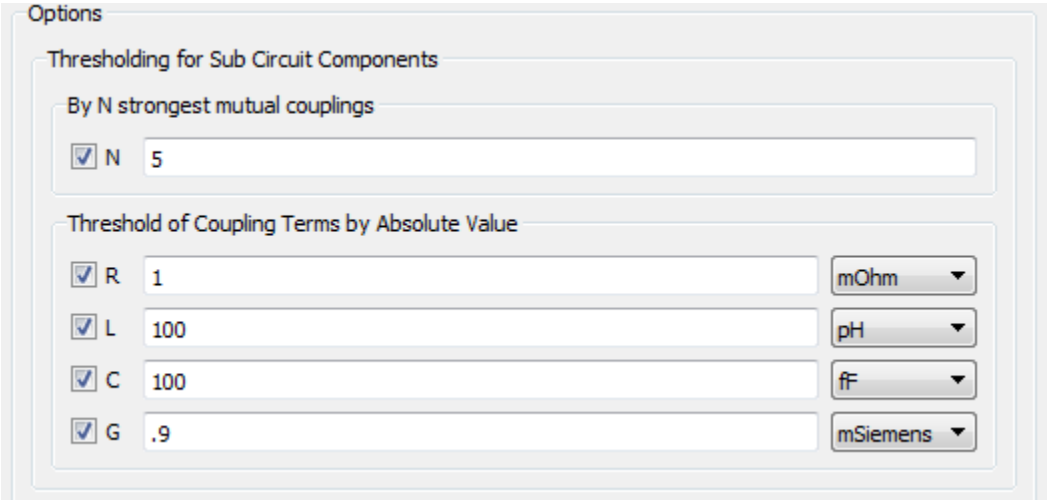

Figure 11 Sub Circuit thresholding settings to sparsify the generated schematic circuits

The series (self) R and L value of each input branch is always maintained but the G and C to ground (Ref) on the outputs nodes can be dropped when below the threshold.

The Options sections also allows to specify the termination of ports that are not of interest for the extraction. Three possibilities can be selected. The terminated ports are shorted, left open or terminated with the reference impedance Port Z as specified in the loaded S-parameter data. The Short setting is the default.

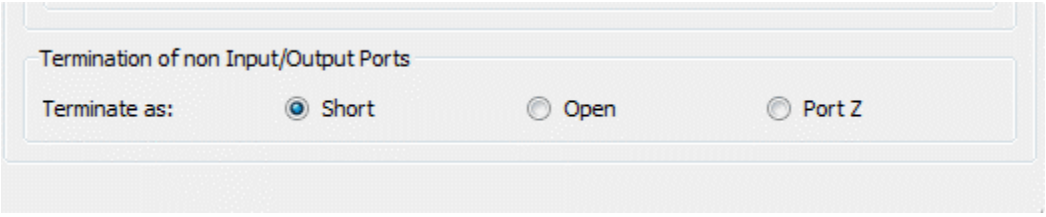

Figure 12 Termination for non Input/Output Ports with default selection to Short.