MINESH PATEL

Citizenship: USA
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RESEARCH INTERESTS

Computer Systems; Computer Architecture; Memory; Performance Modeling; Performance Analysis; Statistical Analysis; Runtime and Operating Systems; Binary Analysis and Compilation; Computer Graphics

EDUCATION

2016-Present **ETH Zürich, Zürich, Switzerland**
Ph.D. in Electrical and Computer Engineering (adviser: Onur Mutlu)
Field: Computer Architecture
Expected Graduation: **Oct. 2021**

2015-2016 **Carnegie Mellon University, Pittsburgh, PA**
Ph.D. in Electrical and Computer Engineering (transferred to ETH with adviser Onur Mutlu)

2011-2015 **University of Texas at Austin, Austin, TX** (GPA: 3.97 / 4.00)
B.S. (Honors) Electrical and Computer Engineering
B.S. (Honors) Physics

PROFESSIONAL EXPERIENCE

Mar–Aug 2019 **Apple Inc:** Graduate Research Intern, SEG DRAM (Cupertino, CA, USA)

Jun–Sep 2018 **Microsoft Research:** Research Intern, Mobility and Networking Group (Seattle, WA, USA)

May–Dec 2016, Jun–Dec 2017 **Apple Inc:** Graduate Research Intern, Platform Architecture (Cupertino, CA, USA)
Explored memory subsystem performance and power opportunities using a combination of performance modeling and post-silicon main memory testing

May–Aug 2015 **Microsoft:** Silicon Implementation Intern, HoloLens (Fort Collins, CO, USA)
Designed image processing hardware using high-level synthesis and Verilog

Jan–Aug 2014 **Apple Inc:** Silicon Engineering Intern, SEG Graphics/GPU (Austin, TX, USA)
Functional model bring-up in C++ with multiple GPU driver APIs, including OpenGL

May–Aug 2013 **National Instruments R&D:** HW Engineering (Digital Design) Intern (Austin, TX, USA)
Designed a CPLD-based CAT-II ch-ch isolated voltage module, verified prototype PCB

May–Aug 2012 **General Electric:** ITLP Intern, UNIX/Linux Engineering Team (Cincinnati, OH, USA)
Evaluated Solaris-/SPARC-based virtualization technologies

PUBLICATIONS

1. Minesh Patel, G. F. de Oliveira Jr., O. Mutlu. **"HARP: Practically and Effectively Identifying Uncorrectable Errors in Main Memory Chips That Use On-Die ECC."**
To appear in *International Symposium on Microarchitecture (MICRO-54)*, Oct. 2021.

2. L. Orosa, G. Yaglikci, H. Luo, A. Olgun, J. Park, H. Hassan, Minesh Patel, J. S. Kim, O. Mutlu. **"A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses."**
To appear in *International Symposium on Microarchitecture (MICRO-54)*, Oct. 2021.

3. Ataberk Olgun, Minesh Patel l, A. Giray Yaglikci, Haocong Luo, Jeremie S. Kim, F. Nisa Bostanci, Nandita Vijaykumar, Oguz Ergin, and Onur Mutlu. **"QUAC-TRNG: High-Throughput True Random Number Generation Using Quadruple Row Activation in Commodity DRAM Chips."**
International Symposium on Computer Architecture (ISCA-48), Jun. 2021.

4. Lois Orosa, Yaohua Wang, Mohammad Sadrosadati, Jeremie S. Kim, Minesh Patel, Ivan Puddu, Haocong Luo, Kaveh Razavi, Juan Gomez-Luna, Hasan Hassan, Nika Mansouri-Ghiasi, Saugata Ghose, and Onur Mutlu. **"CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations."**
International Symposium on Computer Architecture (ISCA-48), Jun. 2021.

5. Nastaran Hajinazar, Geraldo F. Oliveira, Sven Gregorio, Joao Dinis Ferreira, Nika Mansouri Ghiasi, Minesh Patel, Mohammed Alser, Saugata Ghose, Juan Gomez-Luna, and Onur Mutlu. "**SIMDRAM: An End-to-End Framework for Bit-Serial SIMD Computing in DRAM.**"
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-26), Mar.-Apr. 2021.

6. A. G. Yaglikci, Minesh Patel, J. S. Kim, R. Azizi, A. Olgun, L. Orosa, H. Hassan, J. Park, K. Kanellopoulos, T. Shahroodi, S. Ghose, and O. Mutlu. "**BlockHammer: Preventing RowHammer at Low Cost by Blacklisting Rapidly-Accessed DRAM Rows.**"
International Symposium on High-Performance Computer Architecture (HPCA-27), Feb. 2021.

7. Minesh Patel, J. S. Kim, T. Shahroodi, H. Hassan, and O. Mutlu. "**Bit-Exact ECC Recovery (BEER): Determining DRAM On-Die ECC Functions by Exploiting DRAM Data Retention Characteristics**."
International Symposium on Microarchitecture (MICRO-53), Oct. 2020.
Best Paper Award.

8. Y. Wang, L. Orosa, X. Peng, Y. Guo, S. Ghose, Minesh Patel, J. S. Kim, J. G. Luna, M. Sadrosadati, N. M. Ghiasi, and O. Mutlu. **"FIGARO: Improving System Performance via Fine-Grained In-DRAM Data Relocation and Caching."**
International Symposium on Microarchitecture (MICRO-53), Oct. 2020.

9. J. S. Kim, Minesh Patel, A. G. Yaglikci, H. Hassan, R. Azizi, L. Orosa, and O. Mutlu. **"Revisiting RowHammer: An Experimental Analysis of Modern Devices and Mitigation Techniques."**
International Symposium on Computer Architecture (ISCA-47), Jun. 2020.

10. H. Luo, T. Shahroodi, H. Hassan, Minesh Patel, A. G. Yaglikci, L. Orosa, J. Park, and O. Mutlu. **"CLR-DRAM: A Low-Cost DRAM Architecture Enabling Dynamic Capacity-Latency Trade-Off."**
International Symposium on Computer Architecture (ISCA-47), Jun. 2020.

11. N. Hajinazar, P. Patel, Minesh Patel, K. Kanellopoulos, S. Ghose, R. Ausavarungnirun, G. F. de Oliveira Jr., J. Appavoo, V. Seshadri, and O. Mutlu. **"The Virtual Block Interface: A Flexible Alternative to the Conventional Virtual Memory Framework."**
International Symposium on Computer Architecture (ISCA-47), Jun. 2020.

12. L. Cojocar, J. S. Kim, Minesh Patel, L. Tsai, S. Saroiu, A. Wolman, and O. Mutlu. **"Are We Susceptible to Rowhammer? An End-to-End Methodology for Cloud Providers."**
IEEE Symposium on Security and Privacy (S&P-41), May 2020.

13. H. Hassan, Minesh Patel, J. S. Kim, A. G. Yaglikci, N. Vijaykumar, N. M. Ghiasi, S. Ghose, and O. Mutlu. **"CROW: A Low-Cost Substrate for Improving DRAM Performance, Energy Efficiency, and Reliability."**
International Symposium on Computer Architecture (ISCA-46), Jun. 2019.

14. A. Boroumand, S. Ghose, Minesh Patel, H. Hassan, B. Lucia, R. Ausavarungnirun, K. Hsieh, N. Hajinazar, K. T. Malladi, H. Zheng, and O. Mutlu. **"CoNDA: Efficient Cache Coherence Support for Near-Data Accelerators."**
International Symposium on Computer Architecture (ISCA-46), Jun. 2019.

15. Minesh Patel, J. S. Kim, H. Hassan, and O. Mutlu. **"Understanding and Modeling On-Die Error Correction in Modern DRAM: An Experimental Study Using Real Devices."**
IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-49), Jun. 2019.
Best Paper Award.

16. J. S. Kim, Minesh Patel, H. Hassan, L. Orosa, and O. Mutlu. **"D-RaNGe: Using Commodity DRAM Devices to Generate True Random Numbers with Low Latency and High Throughput."**
International Symposium on High-Performance Computer Architecture (HPCA-25), Feb. 2019.
IEEE Micro Top Picks Honorable Mention

17. Y. Wang, A. Tavakkol, L. Orosa, S. Ghose, N. M. Ghiasi, Minesh Patel, J. S. Kim, H. Hassan, M. Sadrosadati, and O. Mutlu. **"Reducing DRAM Latency via Charge-Level-Aware Look-Ahead Partial Restoration."**
International Symposium on Microarchitecture (MICRO-51), Oct. 2018.

18. J. S. Kim, Minesh Patel, H. Hassan, and O. Mutlu. **"Solar-DRAM: Reducing DRAM Access Latency by Exploiting the Variation in Local Bitlines**."
IEEE International Conference on Computer Design (ICCD-36), Oct. 2018.

19. J. S. Kim, Minesh Patel, H. Hassan, and O. Mutlu. **"The DRAM Latency PUF: Quickly Evaluating Physical Unclonable Functions by Exploiting the Latency-Reliability Tradeoff in Modern DRAM Devices."**
International Symposium on High-Performance Computer Architecture (HPCA-24), Feb. 2018.

20. Minesh Patel, J. S. Kim, and O. Mutlu. **"The Reach Profiler (REAPER): Enabling the Mitigation of DRAM Retention Failures via Profiling at Aggressive Conditions."**
International Symposium on Computer Architecture (ISCA-44), Jun. 2017.

21. A. Boroumand, S. Ghose, Minesh Patel, H. Hassan, B. Lucia, K. Hsieh, K. T. Malladi, H. Zheng, and O. Mutlu. **"LazyPIM: An Efficient Cache Coherence Mechanism for Processing-in-Memory."**
IEEE Computer Architecture Letters (CAL), Jun. 2017.

HONORS AND AWARDS

- ISCA Hall of Fame
- Best Paper Award, MICRO 2020
- IEEE Micro Top Picks Honorable Mention 2020
- Best Paper Award, DSN 2019
- Eagle Scout Award
- UT Endowed Pres. Scholarship in ECE, Physics
- UT Engineering Honors Scholarship

PATENTS

J. S. Kim, Minesh Patel, S. Meier, T. Huberty, O. Mutlu. **"Security Techniques Based on Memory Timing Characteristics."** *U.S. Patent US10776521B2*. Sep. 2020.

TEACHING EXPERIENCE

2017-Present	**Computer Architecture**, ETH Zurich, *Teaching Assistant*
2017-Present	**Digital Design and Circuits**, ETH Zurich, *Teaching Assistant*
2017-Present	**Seminar in Computer Architecture**, ETH Zurich, *Teaching Assistant*
2011-2013	**PHY303K, PS303, PHY355** (UT Mechanics, Intro to Modern Physics), *Teaching Assistant*

OPEN-SOURCE TOOLS/INFRASTRUCTURE

BEER: C++/Python/SMT tool for analyzing and reverse-engineering DRAM error-correcting codes (ECCs)
https://github.com/CMU-SAFARI/BEER

EINSIM: C++ Monte-Carlo simulator for exploring how error-correcting codes (ECCs) impact DRAM errors
https://github.com/CMU-SAFARI/EINSim

CONFERENCE TALKS

1. **"Bit-Exact ECC Recovery (BEER): Determining DRAM On-Die ECC Functions by Exploiting DRAM Data Retention Characteristics**," *International Symposium on Microarchitecture (MICRO-53)*, Virtual, Oct. 2020.

2. **"Understanding and Modeling On-Die Error Correction in Modern DRAM: An Experimental Study Using Real Devices"**, *International Conference on Dependable Systems and Networks (DSN-49)*, Portland, OR, Jun. 2019

3. **"The Reach Profiler (REAPER): Enabling the Mitigation of DRAM Retention Failures via Profiling at Aggressive Conditions"**, *International Symposium on Computer Architecture (ISCA-44)*, Toronto, Canada, Jun. 2017.

RELEVANT COURSEWORK

Computational Intelligence Lab (ETH, 2017), Probabilistic AI (ETH, 2019)
Overview of common statistical and machine learning techniques for image and data analysis

Advanced Systems Lab (ETH, 2017)
Implementation and performance evaluation of middleware in a Java-based distributed client-server system

Operating System Design and Implementation (CMU 15-410, 2016)
From-scratch x86 UNIX-like kernel with preemption, memory management, synchronization, NUMA multiproc.

Advanced Digital Integrated Circuit Design (CMU 18-622, 2016)
Hand-optimized 16x16-bit SRAM + integer ALU + datapath VLSI design and layout with timing/area constraints

Team Senior Design Project (UT EE464H, 2014-2015) under Prof. Yale Patt
From-scratch scalar in-order and OoO ARMv4 microarchitecture design in both SystemC/C++ and Verilog

Real Time Embedded Systems (UT EE345M, 2014)
Won 1st place in autonomous robot racing using an ARM embedded system with a home-grown real time OS

TECHNICAL PROFICIENCIES

Python, Bash, TCL for scripting, data analysis, and general-purpose programming
C, C++, Assembly for high-performance and/or low-level programming
Pintool, Gem5 for workload analysis and processor simulation
OpenGL, Vulkan for computer graphics programming