Michael R. Paulson

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Security Clearance - TS/SCI Full Scope with Poly

Knowledgeable computer science student with a strong work ethic and customer service background. Works well independently, but also enjoys roles in a group setting. Provides an innovative perspective on issues and has a strong ability to troubleshoot in high stress environments. Skilled in analyzing problems, designing efficient solutions, and taking on leadership roles to see them through.

Work History

Science and Technology Intern

05/2021 - 08/2021

- National Security Agency (NSA) Fort Meade, MD
 - Utilized the Riverbed Tool Suite to update functional network models
- Completed CompTIA Network+ (2014) trainings
- Applied knowledge of the OSI model and TCP/IP to create network simulations

Computer Science Grader

-Texas State University - San Marcos, TX

01/2021 - 05/2021

• Debugged and tested assignments as well as provided constructive feedback on assignments to each student to help them better understand the content.

Technical Intern

- Edwards Aquifer Authority - San Antonio, TX

08/2020 - 12/2020

- Performed systems testing of newly developed software.
- Efficiently communicated with team members, requesting they execute testing while logging their resulting issues/successes, this cleared lines of communication and allowed for an increase in ticket resolution.

Branch Manager

- Square Cow Moovers - Austin, TX

10/2012 - 05/2016

- Lead team in building new branch of the company which surpassed the success of all previous branches throughout Texas within the year.
- Highest performing salesperson booking \$1.2 million/year.

Education

Computer Science (BS) minor focus in business admin

Texas State University - San Marcos, TX | 3.89 GPA

Graduation 05/2022

Languages/Skills/Tools

• C++ | Java | JavaScript | Python | HTML | CSS | Riverbed Suite | OSI Model | TCP/IP | Linux

Projects

-Disassembler + Emulator- (C++)

Implemented the decoding method of a disassembler that reads MIPS machine instructions from a (simplified) binary executable file and prints each assembly language instruction to the screen. The emulator reads MIPS machine instructions from the provided binary executable files and emulates a MIPS CPU that executes the program.

-Data Cache- (C++)

We further enhanced the simulator to model pipeline stalls due to memory latency and simulated a data cache to study the performance impact of caching.

-Discrete Time Simulator- (C++)

This simulator was designed to assess the speedup when using multiple CPUs in a first-come-first-served queuing system. The simulation runs in two different scenarios: Single Queue | Multi-CPU or Multi-Queue | Multi-CPU.