Digital IC Design Final Project Report

J Manoj Vikram, EE10B018
M Pavankumar Reddy, EE10B020
Siva Teja M G V,EE10B039
Somani Abhishek,EE10B040

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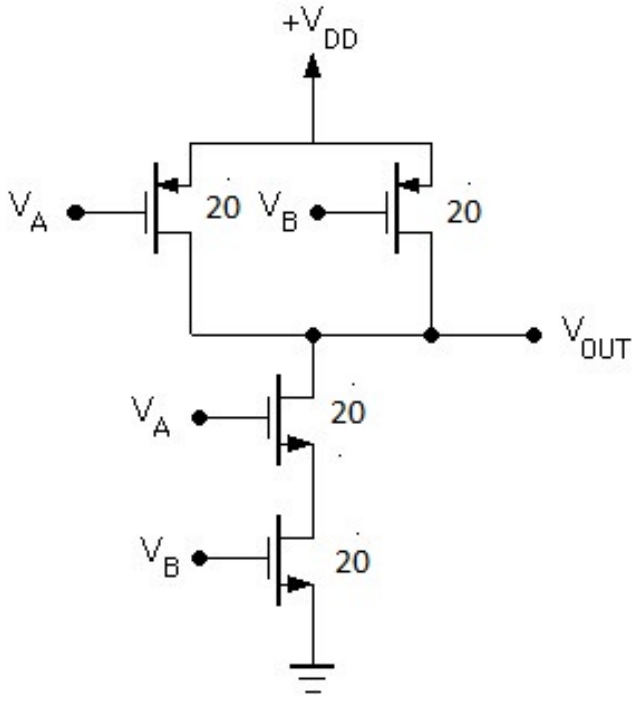
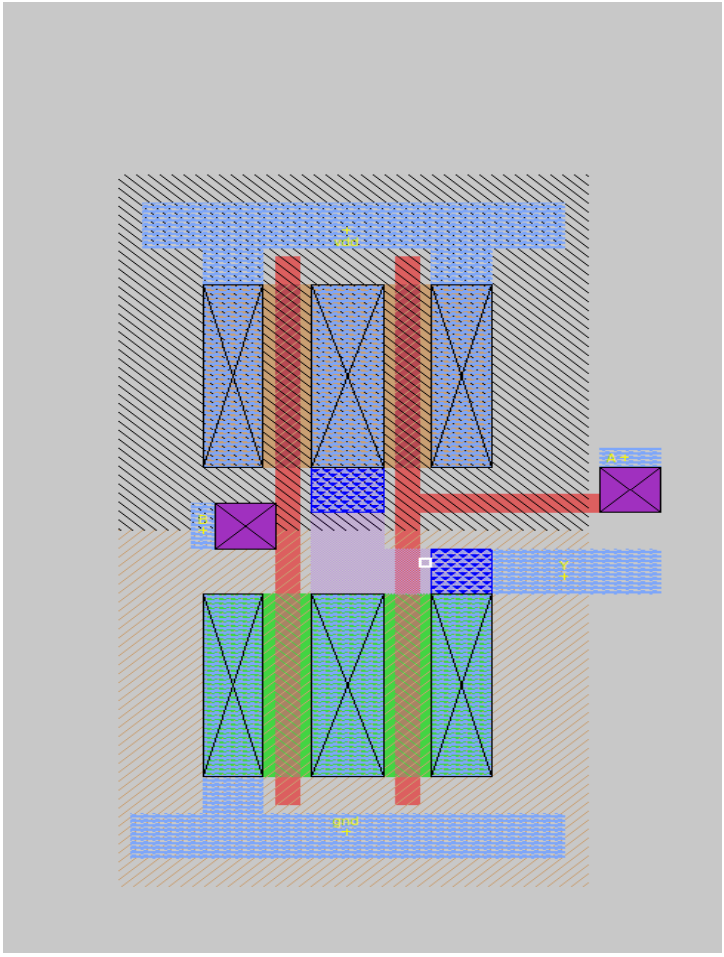
Introduction

We have chosen to implement the standard cells NAND2x1, NOR2X1 and DFFNEGX1. The inverter given is taken as a unit reference. The approximate sizes and schematics for each cell are given below.

NAND2X1



Circuit Diagram for NAND2X1 A



Magic Layout for NAND2X1 1

Analysis:

Layout and sizes:

To make the width a multiple of 6λ, we increased the size of the center pdcontact to 6λ,thus the overall width being 18λ. Height of the layout is 72λ.

To ensure that the drive of this cell will be approximately the same as that of the inverter,

1. We used pmos of size 20λ to make the pull up resistance approximately equal to pull up resistance of the given standard inverter.

2. We used nmos of size 20λ (as they are in series) to make the pull down resistance approximately equal to pull down resistance of the given standard inverter.

Computation of Parameters:

1. **Delay:** We have added the capacitance to the output and gave the input pulse to one of the inputs while keeping the other one at Vdd. The rising and falling delays were obtained using the cursor function for both inputs and all the cases in this manner.

2. **Power:** We have used the average current to measure the power in the circuit. The average current out of the supply was multiplied with supply voltage to give the power. One of the inputs was given as a pulse while the other was kept at vdd. This multiplied with time period gives power in pico joules

3. **Static Power:** The average current was measured while keeping both the inputs constant. This was multiplied with supply voltage to get average static power.

4. **Driving strength:** This is given by delay/capacitance. We took the minimum value of all the measured ratios.

Inference:

1. The average delay was around the same value (+/- 10ps) as the reference standard inverter. There was a steady increase in the delay values as the load capacitance increased. This is because larger capacitances take more time to charge/discharge.

2. The power values in general increased with increasing load capacitance. This is because more energy is required to charge a larger capacitor.

3. The power also increases as rise/fall times are increased. This could be because the longer rise/fall time implies that the cmos circuit is in transition state (non-static state) for a longer period thus increasing the power consumed.

Results:

NAND2X1

Function

Y= $\overline{\mathbf{AB}}$

Static Power:

When	Static Power [nW]
-	0.0312

Port:

Name	Direction
A	INPUT
B	INPUT
Y	OUTPUT

Output Driving Strength

Name	Rise		Fall	
	Strength (sec/F)	Limit (pF)	Strength (sec/F)	Limit (pF)
Y	2.34e+03	0.5	1.54e+03	0.5

(01A=>10Y)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.03133	0.05978	0.23165
0.42	0.039149	0.092931	0.28669
1.2	0.01957	0.10178	0.344

(10A=>01Y)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.04381	0.08654	0.3404
0.42	0.09795	0.15925	0.41533
1.2	0.1799	0.2669	0.5924

(01B=>10Y)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.03614	0.0645	0.2361
0.42	0.0366	0.08385	0.2700
1.2	0.001955	0.07658	0.3303

(10B=>01Y)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.05691	0.09898	0.3515
0.42	0.1225	0.17655	0.4282
1.2	0.2223	0.2971	0.607

(A=1, B changing periodically)

POWER [pJ]

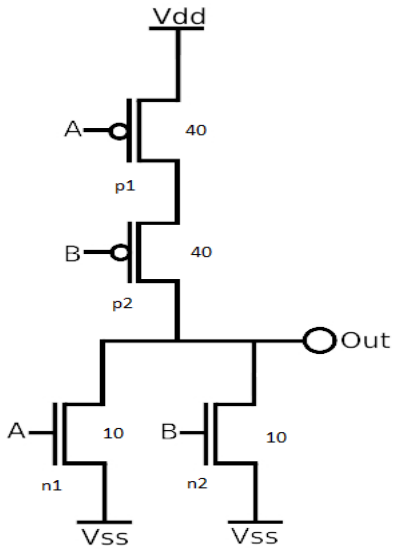
cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.036768	0.08194	0.3529
0.42	0.0453	0.0853	0.351
1.2	0.0978	0.129	0.375

(B=1, A changing periodically)

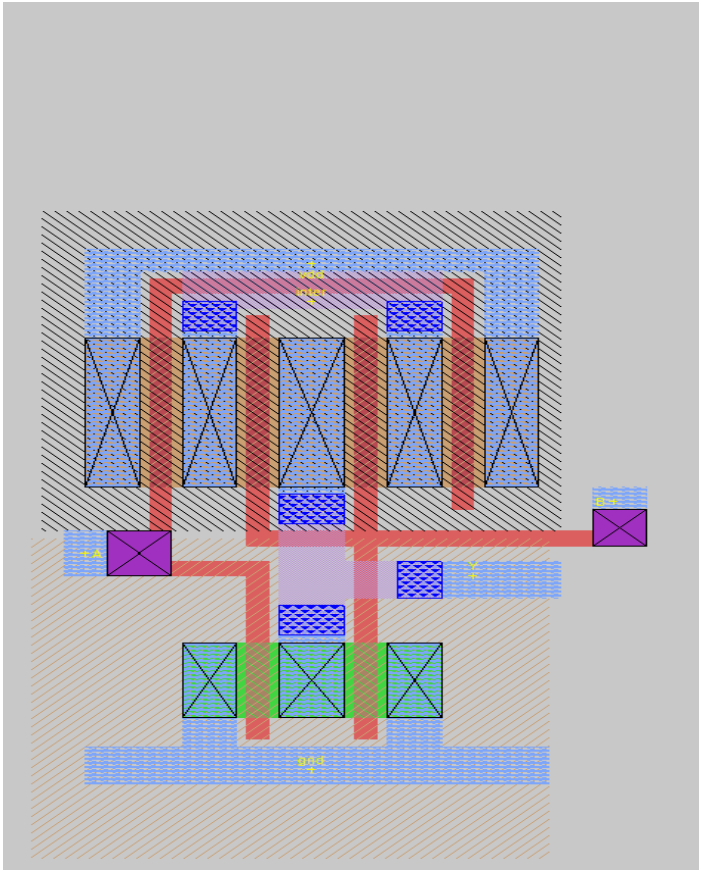
POWER [pJ]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.0238	0.070	0.343
0.42	0.0377	0.076	0.342
1.2	0.0907	0.120	0.366

NOR2X1



Circuit Diagram for NOR2X1 1



Maigic Layout for NOR2X1 1

Analysis:

Layout and sizes:

To make the width a multiple of 6λ, we increased the size of the center pdcontact to 6λ,thus the overall width being 42λ. Height of the layout is 72λ.

To ensure that the drive of this cell will be approximately the same as that of the inverter,

1. We used pmos of size 40λ(as they are in series) to make the pull up resistance approximately equal to pull up resistance of the given standard inverter.

2. nmos of size 10λ to make the pull down resistance approximately equal to pull down resistance of the given standard inverter.

Computation of Parameters:

1. Delay: We have added the capacitance to the output and gave the input pulse to one of the inputs while keeping the other one at GND. The rising and falling delays were obtained using the cursor function for both inputs and all the cases in this manner.

2. Power: We have used the average current to measure the power in the circuit. The average current out of the supply was multiplied with supply voltage to give the power. One of the input was given as a pulse while the other was kept at vdd.

3. Static Power: The average current was measured while keeping both the inputs constant. This was multiplied with supply voltage to get average static power.

4. Driving strength: This is given by delay/capacitance . We took the minimum value of all the measured ratios.

Inference:

1. The average delay was around the same value (+-10ps) as the reference standard inverter. There was a steady increase in the delay values as the load capacitance increased. This is because larger capacitances take more time to charge/discharge.

2. The power values in general increased with increasing load capacitance. This is because more energy is required to charge larger capacitor.

3. The power also increases as rise/fall times are increased. This could be because the longer rise/fall time implies that the cmos circuit is in transition state (non-static state) for a longer period thus increasing the power consumed.

Results:

NOR2X1(data type: typ)

Function

Y= $\overline{\mathbf{A+B}}$

Static Power:

When	Static Power [nW]
-	0.028561

Port:

Name	Direction
A	INPUT
B	INPUT
Y	OUTPUT

Output Driving Strength

Name	Rise		Fall	
	Strength (sec/F)	Limit (pF)	Strength (sec/F)	Limit (pF)
Y	1.95e+03	0.5	1.74e+03	0.5

(01B=>10Y)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.0359	0.0741	0.291
0.42	0.0564	0.116	0.347
1.2	0.0689	0.158	0.472

(10B=>01Y)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.0384	0.0734	0.320
0.42	0.0732	0.135	0.385
1.2	0.1192	0.210	0.535

(01A=>10Y)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.04655	0.0788	0.300
0.42	0.0818	0.1344	0.358
1.2	0.1194	0.192	0.488

(10A=>01Y)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.0445	0.0838	0.324
0.42	0.0649	0.119	0.368
1.2	0.08900	0.169	0.465

(A=0, B changing periodically)

POWER [pJ]

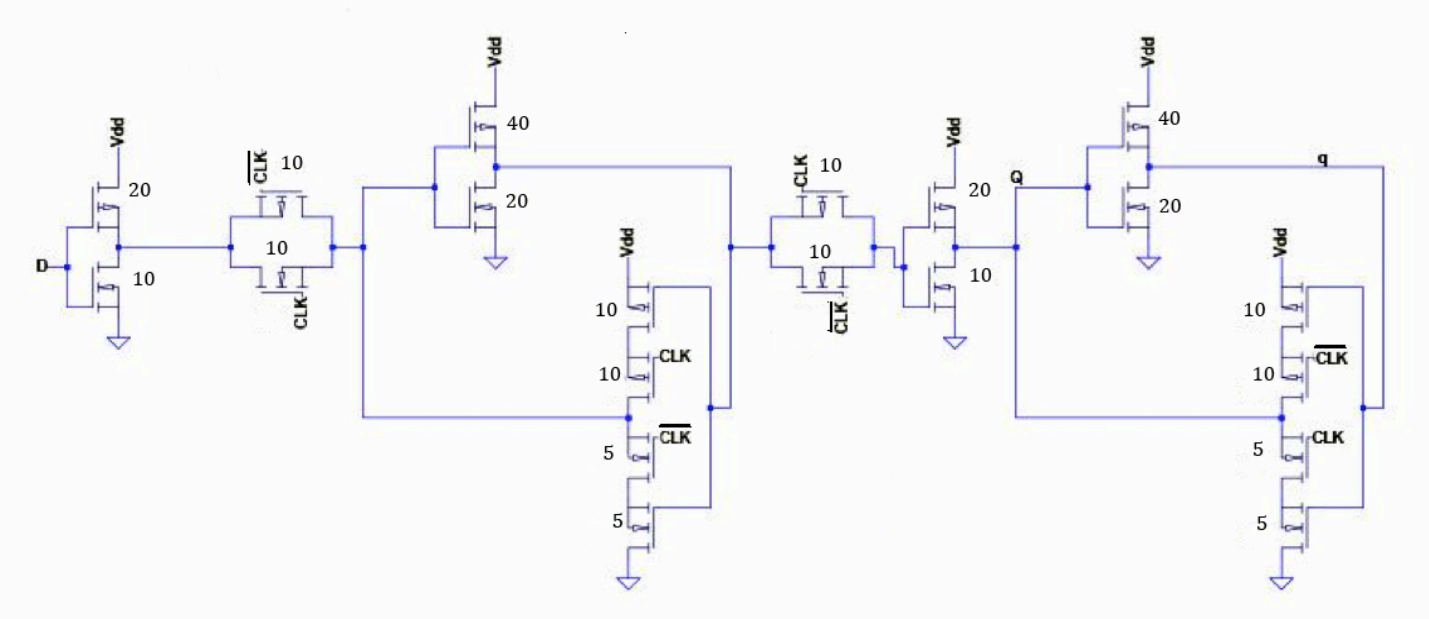
cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.044	0.131	0.621
0.42	0.065	0.136	0.616
1.2	0.126	0.158	0.377

(B=0, A changing periodically)

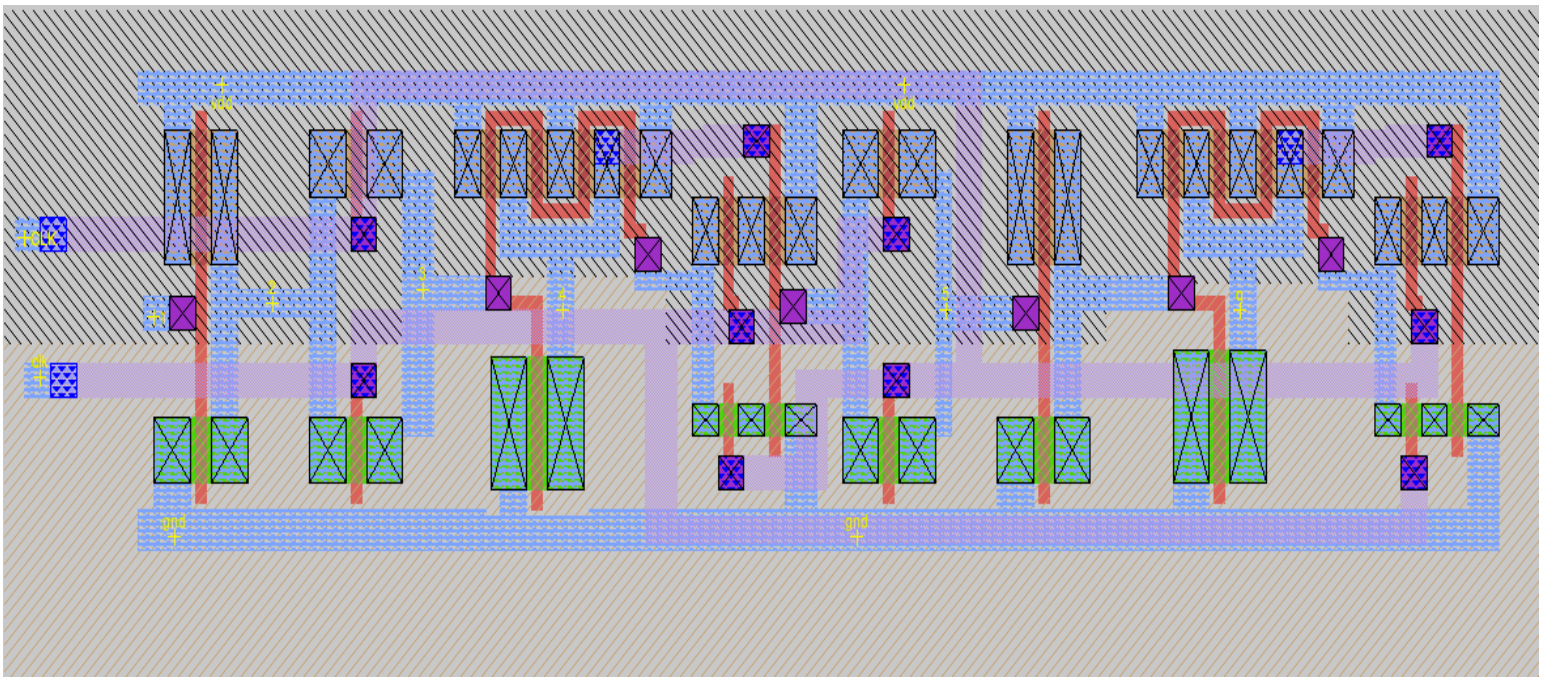
POWER [pJ]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.070	0.149	0.634
0.42	0.082	0.155	0.633
1.2	0.150	0.188	0.404

DFFNEGX1



Circuit Diagram for DFFNEGX1 1



Magic Layout for DFFNEGX1 1

Analysis

Layout and sizes:

Total height is 72λ and total width is 264λ. There are three types of CMOS circuits namely inverters, pass transistors and loop inverters.

1. The sizes of inverters are the same as the standard reference.
2. The sizes of the pass transistors are taken in the ratio 1:1 and thus both PMOS and NMOS have 10λ width. 2.
3. For the loop inverters, the forward strength should be more than the feedback inverter strength. Thus, we chose 10λ width for the forward loop and 5λ width for the feedback loop.

Computation of Parameters:

1. Delay: We have added the capacitance to the output and gave the required input pulse. The rising and falling Clock to output Q delays were obtained using the cursor function for both inputs and all the cases in this manner.
2. Power: We have used the average current to measure the power in the circuit. The average current out of the supply was multiplied with supply voltage to give the power. One of the input was given as a pulse while the other was kept at vdd.
3. Static Power: The average current was measured while keeping both the inputs constant. This was multiplied with supply voltage to get average static power.
4. Driving strength: This is given by delay/capacitance . We took the minimum value of all the measured ratios.

Inference:

1. The average delay was around the same value (+-10ps) as the reference standard inverter. There was a steady increase in the delay

values as the load capacitance increased. This is because larger capacitances take more time to charge/discharge.

2. Thepowervaluesingeneralincreasedwithincreasingloadcapacitance.This is because more energy is required to charge larger capacitor.
4. The power also increases as rise/fall times are increased. This could be because the longer rise/fall times implies that the cmos circuit is in transition state (non-static state) for a longer period thus increasing the power consumed.

Results

DFFNEGX1(data type: typ)

Function
FLIPFLOP{
DATA=D
CLOCK=!CLK
Q=DS0000
QN=P0002
}
Q=DS0000

Static Power:

When	Static Power [nW]
-	2.3

Port:

Pin	Direction	Signaltype	Polarity
CLK	INPUT	CLOCK	FALLING_EDGE
D	INPU	DATA	-
Q	OUTPUT	-	-

Output Driving Strength

Name	Rise		Fall	
	Strength (sec/F)	Limit (pF)	Strength (sec/F)	Limit (pF)
Q	2.15e+3	0.992	2.15e+3	0.992

(10CLK=>01Q)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.126	0.173	0.313
0.48	0.140	0.188	0.329
1.2	0.162	0.197	0.409

POWER [pJ]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.374	0.437	0.893
0.48	0.392	0.454	0.911
1.2	0.497	0.558	1.015

(10CLK=>10Q)

DELAY [ns]

cl[pF] / ts[ns]	0.005	0.025	0.15
0.06	0.123	0.173	0.313
0.48	0.148	0.189	0.339
1.2	0.170	0.198	0.403

POWER [pJ]

cl[pF] ts[ns]	0.005	0.025	0.15
0.06	0.374	0.437	0.893
0.48	0.392	0.454	0.911
1.2	0.497	0.558	1.015