M Pavankumar Reddy

Indian Institute of Technology Madras

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Objective

Pursue funded graduate research in the areas of computer engineering, digital design and testing in a reputed university under an eminent professor.

Education

Indian Institute of Technology, Madras (B.Tech) - 9.09/10 **Aug 2010 - Present**

- Major: Electrical Engineering. CGPA: 9.10/10
- Minor: Operations Research. GPA: 9/10
- Enrolled to the honours program which requires twelve extra credits and a minimum CGPA of 8.5/10.

Vijayaratna Junior College, Hyderabad - 96.4% **March 2010**

Bharatiya Vidya Bhavan's Public School, Hyderabad - 92% **March 2008**

Scholastic Achievements

- All India Rank (AIR) of 305 in IIT-Joint Entrance Examination 2010.
- State rank of 27 and All India Rank of 83 in All India Engineering Entrance Examination 2010.
- A GPA of 9.5 in Mathematics.
- Among the top 10% in a class of 127.
- Recipient of the Central Board of Secondary Education Merit Scholarship.
- Recipient of the Pratibha Scholarship for extraordinary performance in high school.
- Recipient of the IIT Madras Merit Certificate.
- Top 1% in National Standard Examination in Astronomy 2009.
- Rank 9 in National Mathematics Talent Competitions organized by Association of Mathematics Teachers in India.
- High distinction in International Assessment of Indian Schools in Mathematics by University of New South Wales. Placed 2nd in the region with a score of 39/40.
- High distinction in Royal Australian Chemistry Quiz 2009.
- Represented school in 58th International Astronautical Congress, Hyderabad 2007.
- City rank 1 and state rank 3 in 10th National Science Olympiad (National Percentile of 99.63).

Projects

High Level Synthesis and Mapping of Digital Circuits (Senior Thesis) **September 2013 - Present**

- Guide: *Prof. V. Kamakoti, IITM*
- My current research involves mapping of hardware description (in Chisel[1]) into structures called Assignment Decision Diagrams(ADDs) that is capable of representing circuit in its most parallel form independent of the language constructs. Introducing this new level of abstraction ensures that the resulting hardware synthesized from the ADD would be consistent and optimized for input descriptions with different groupings and orderings.

Design of a Technology Library in 180nm Technology **August 2013 - Present**

- Advisor: *Prof. Nitin Chandrachoodan, IITM*
- *Objective:* Design and Characterize a standard cell library in 180nm Technology.

Fully differential operational amplifier design **January 2013 - April 2013**

- Advisor: *Prof. Sankaran Aniruddhan, IITM*
- Designed and implemented a fully differential two stage opamp with specified gain, bandwidth and phase margin.

Class D Audio Amplifier **January 2013 - April 2013**

- Advisor: *Nagendra Krishnapura, IITM*
- Made a class D audio amplifier with a pulse width modulator (using LM311) followed by a switch (NPN and PNP transistor pair driven by a CMOS inverter buffers) that will drive the speakers.

[1] Chisel is an open-source hardware description language based on Scala developed at UC Berkeley

Networks Project **August 2012-November 2012**

- Advisor: *Andrew Thangaraj, IITM* and *Krishna Jagannathan*
- *Objective:* Visualize the emergence of technologies in a field to identify trends.
- *Result:* Used author keywords from the papers of a target technology field and clustered them to create a semantic network of keywords. This categorization (using clustering) is used to present the technology evolution on a timeline for visualization.

Online Scientific Editor, Chennai **November 2011 - January 2012**

- *TNQ Books and Publishers, Chennai*
- *Objective:* Editor for editing academic documents online.
- *Result:* Designed and developed a online editor for editing academic documents (including latex, word and other formats) online in collaboration with *TNQ Books and Publishers*.

Internships

Texas Instruments, High Performance Analog Team, Bangalore **May 2013 - July 2013**

- Designed and developed a high frequency mixer for frequencies around 25GHz and a bandwidth of 1GHz.
- Employed a Gilbert Cell Core followed by a transimpedance amplifier for the above mixer.

General Electric - Intelligent Platforms, Bangalore **May 2012 - July 2012**

- Ported a 9030C software stack to existing GE Fanuc platform.
- Optimized library modules to run 50 times faster using the C software stack.

Relevant Courses and Labs

- Electric and Magnetic Circuits
- Digital Systems
- Networks and Systems
- Computer Organization and Microprocessors
- Analog and Digital Signal Processing
- Solid State Devices
- Analog Circuits
- Control Systems
- Analog IC Design
- Data Structures and Algorithms
- Digital IC Design[2]
- Digital Communication Systems[2]
- Communication Networks[2]
- Heterogeneous Parallel Programming[3]
- Computer Architecture[3]
- Linear Algebra and Numerical Analysis
- Probability and Random Processes
- Computer Aided Design Laboratory
- Digital Circuits Laboratory
- Microprocessor Laboratory
- Analog Circuits Laboratory

Skills

- **Languages and tools:** C, Python, VHDL, Verilog, CudaC, OpenCL, Chisel(Scala), Assembly(8051, ARM), Java, Javascript
- **Platforms and tools:** Magic VLSI, ModelSim, Xilinx ISE, Keil μVision, Spice OPUS, Virtuoso Analog Environment, LT Spice, GE Fanuc PLC Platform, Adobe Dreamweaver, Adobe Photoshop, AutoCAD
- **Operating Systems:** Mac OSX, Ubuntu, Microsoft Windows

Positions of Responsibility

IEEE Student Member **Present**

Head Coordinator for the Web and Mobile Development team in Saarang **April 2012 - January 2013**

Coordinator for the Web and Mobile Development team in Saarang **October 2011 - January 2012**

- Chief coordinator for web and mobile development teams of Saarang 2013 which is responsible for the website (www.saarang.org) and mobile applications.
- As a coordinator, responsible for developing the front-end of the website.

Coordinator for Electronics Workshop **October 2011 - January 2012**

- Planned and organized a bio-medical electronics workshop attended by more than 300 students. This included a lecture followed by a hands-on session on making an electronics stethoscope.

[2]Courses in the current semester
[3]Courses pursued on Coursera

– Coordinated a lecture on the topic bio-medical instrumentation with the engineering manager (Virendra Rode) at GE Healthcare, India.

Events Organizer, Entrepreneurship Cell (C-TIDES), IIT-Madras **August 2010 - April 2011**

– Member of organizing committee of Genesis-2011, a social business plan competition which invites entries from across the globe and involves seed funding worth 0.3 million INR.

Co-Curricular Activities

- Won the online games contest at Shaastra 2011.
- Active volunteer for HelpAge India.
- Finalist in the Verizon Ideation Challenge 2012.
- Member of National Cadet Corps, Air Squadron. Flight Cadet under the unit *4(TN) Air Squadron (Tech)* and a 'B' Certificate holder.
- Part of startup (Desto) which focused on design and web consultation.