Analog IC Design - Assignment 6

M Pavankumar Reddy
EE10B020

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Abstract

This document contains the design of a fully differential two stage operational amplifier with specifications of closed loop gain of 2, closed loop 3-db bandwidth of 5MHz and a phase margin of 60^0 in all loops. This is followed by the design of a bandgap reference with an output voltage of 1.2V and with $\frac{dv_{bg}}{dT} = 0$ where T is temperature at $T = 27^0$

1 Introduction

We are going to see the design of a two stage fully differential amplifier. Like its single ended counterpart the fully differential amplifier helps in reducing common mode gain and additionally it rejects noise and other residual signals from the source, ground and therefore provides a superior alternative to the former.

2 Design of the Operational Amplifier

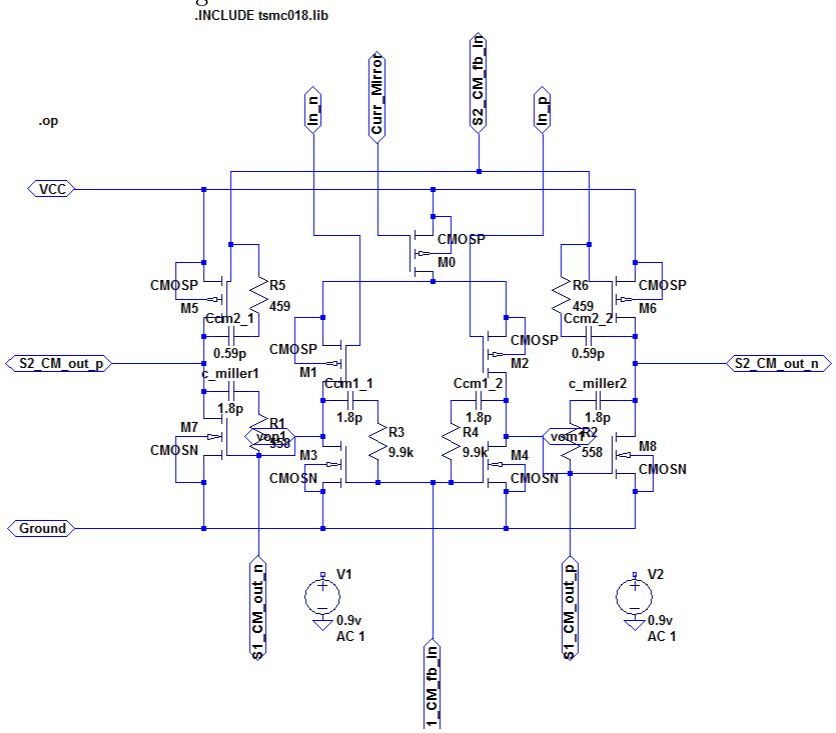
2.1 Design of the differential stage of the amplifier

The two stage fully differential amplifier is similar to the single ended amplifier in the design except that the diode connection in one of the n-mos'(which form the load to the p-mos input pair) is removed to get a differential output signal. The common mode output of the first stage is then set by common mode feedback loop. The output at the second stage is then set to a common mode value in a similar fashion. Various parameters of the first stage are tabulated below.

Device name	W	L	g_m	g_{ds}	$V_{gs} - V_T$	I_D
M_0	$30\mu m$	$0.72\mu m$	$4.29 \times 10^{-4} A/V$	$7.93 \times 10^{-6} \Omega^{-1}$	$0.15V$	$41.4\mu A$
M_1, M_2	$15\mu m$	$0.72\mu m$	$2.19 \times 10^{-4} A/V$	1.78×10^{-6}	$0.147V$	$20.7\mu m$
M_3, M_4	$1.565\mu m$	$0.72\mu m$	$1.42 \times 10^{-4} A/V$	1.43×10^{-6}	$0.203V$	$20.7\mu m$
M_5, M_6	$60\mu m$	$0.72\mu m$	$1.49 \times 10^{-3} A/V$	1.56×10^{-5}	$0.251V$	$258\mu m$
M_7, M_8	$20\mu m$	$0.72\mu m$	$1.79 \times 10^{-3} A/V$	1.47×10^{-5}	$0.203V$	$258\mu m$

The schematic of the fully differential amplifier is shown below.

Figure 1: Main schematic



The following table tabulates some of the main results derived in class for a two stage amplifier

Parameter	Formula
Transfer function	$\frac{g_{m1}(g_{m7}-sC_{miller})}{\{g_{o1}g_{o2}+s(C_{miller}(g_{m7}+g_{o1}+g_{o2})+g_{o1}C_2+g_{o2}C_1)+s^2(C_{miller}C_1+C_1C_2+C_{miller}C_2)\}}$
DC Gain	$\frac{g_{m1}g_{m7}}{(g_{ds1}+g_{ds3})}$
Unity gain frequency,ω_u	$\frac{g_{m1}}{C_{miller}}$
Phase Margin, ϕ_{ugf}	$-90^0 - tan^{-1}(\frac{\omega_u}{\omega_{p2}}) - tan^{-1}(\frac{\omega_u}{\omega_{z1}})$

where $g_{01} = g_{ds1}+g_{ds3}$ is the output impedance at the first stage and $C_1$and C_2 are the output capacitances at the first stage and the second stage respectively. The load capacitance C_L is given to be 10pF. Therefore, if we can design other capacitors to be smaller compared to this one we can make the following assumptions,

$$C_2 = C_L$$

$$g_{o2} = 1/R_L$$

$$\omega_{p2} = \frac{g_{m7}}{C_L}$$

By fixing all the transistor lengths to $0.72\mu m$ we calculate the values of λ_n and λ_p to be around 0.045 and 0.048 respectively using plots of $\frac{dI_D}{dV_{DS}}$ of the n-mos and p-mos models available. By fixing $V_{ov} = 0.2V$, we get the gain of the first stage to be,

$$Gain1 = \frac{g_{m1}}{(g_{ds1}+g_{ds3})} = \frac{2}{V_{ov1}} \times \frac{1}{(\lambda_n+\lambda_p)} = 107$$

We need a closed loop bandwidth of 5MHz. So, we should have $\omega_u = 20\Pi Mrad/s$ and using the formula for phase margin (for 60^0) mentioned earlier, we can calculate, $\omega_{p2} = \sqrt{3} \times \omega_u$, (ignoring the contribution from the zero). Hence, we get $g_{m7} = 1.088mS$. I_{D1} is set set to $20\mu A$ and we get value of $g_{m1} = 0.2mS$. As we can see from the above table the values of g_m for transistors M_1 and M_2 were almost same after tweaking

the values in the simulator for getting appropriate gain although values of M_3 and M_4 did deviate a little away. The calculated value of DC gain is 292.47 which is pretty close to the actual gain of 277.

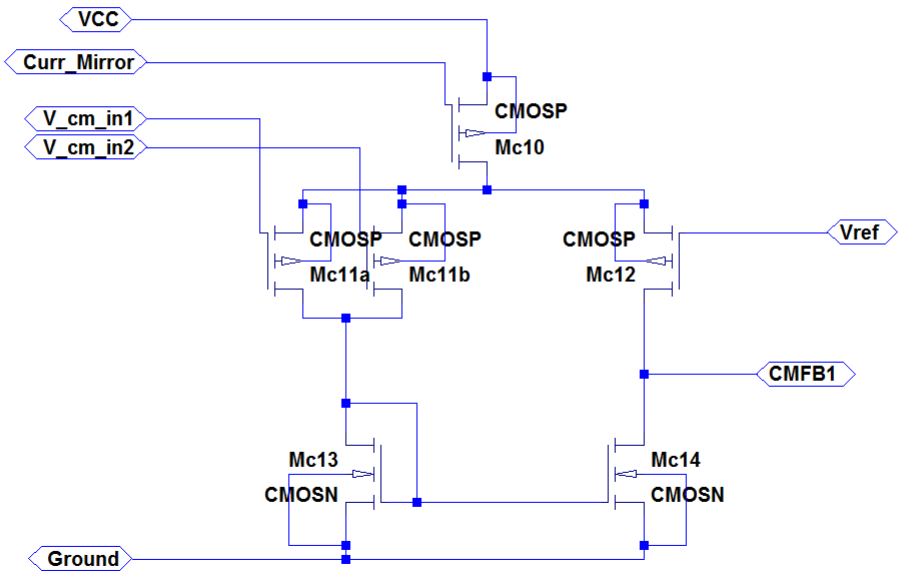
Finally, we get the following values for various parameters for the first stage.

Parameter	Value
DC gain	48.8dB (277)
ω_u	10.5MHz
C_{miller}	1.8pF
Phase Margin	64^0
ω_{p1}	45.5KHz

2.2 Design of common mode feedback loop 1

For the design of the common mode feedback loop of the amplifier we use a sigle-ended differential amplifier. As we have considerable gain at the end of first stage, we donot need that much gain for this op-amp. We try to establish replica bias here with the first stage to ensure 0 error in the output voltage and the reference voltage. As we are designing a 2-stage differential amplifier, we will not have much swing at the end of first stage and hence, we can use a p-mos common mode detector shown here.

Figure 2: Common mode detector 1 amplifier



The amplifier in the common mode has been designed for a current of $20\mu A$ in $Mc10$ and $10\mu A$ current in the two branches and usual assumption of $L = 0.72\mu m$ and $V_{ov} = 0.2V$. The reference voltage used was 0.7V as calculated for the main opamp for maximum swing at the first stage. After tweaking through the values for the stabilization and for a phase margin of 60^0 we get the following values for parmeters in the common mode loop for the first stage output.

The closed loop DC gain achieved in this block is 37dB(66).

The compensation capacitor used for this is,

$$C_{cm1} = 1.8pF$$

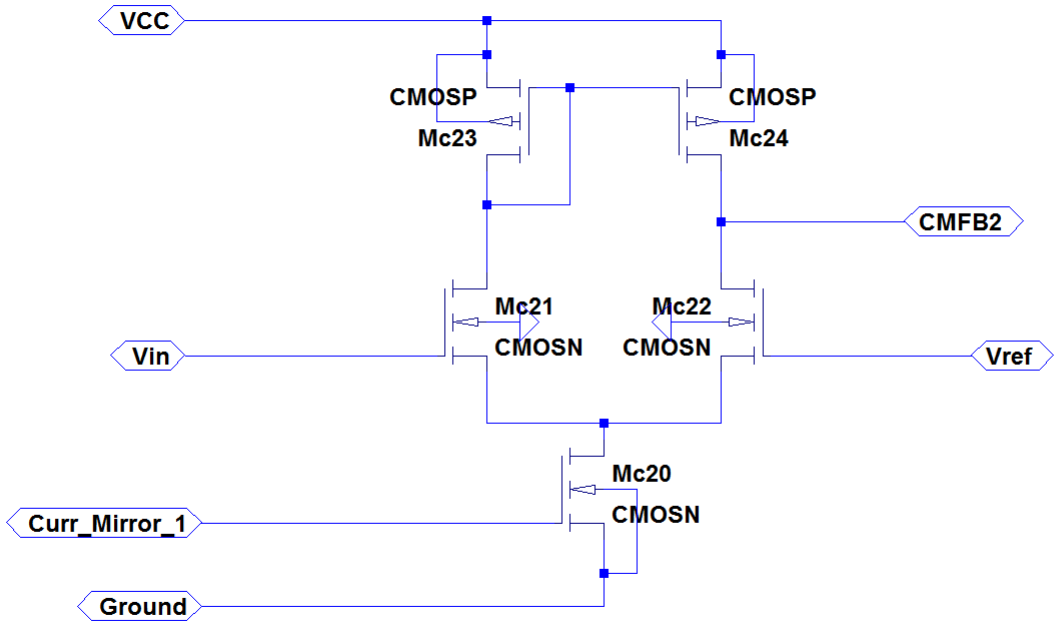
Device name	W	L	g_m	$g_{ds}(\Omega^{-1})$	$V_{gs} - V_T$	I_D
M_{c10}	$18\mu m$	$0.72\mu m$	$2.63 \times 10^{-4} A/V$	3.13×10^{-6}	$0.15V$	$25.3\mu A$
M_{c11a}, M_{c11b}	$2.4\mu m$	$0.72\mu m$	$4.81 \times 10^{-5} A/V$	0.493×10^{-6}	$0.197V$	$6.25\mu A$
M_{c12}	$4.8\mu m$	$0.72\mu m$	$9.58 \times 10^{-5} A/V$	1.01×10^{-6}	$0.198V$	$12.6\mu A$
M_{c13}, M_{c14}	$1.2\mu m$	$0.72\mu m$	$9.9 \times 10^{-5} A/V$	0.926×10^{-5}	$0.183V$	$12.6\mu A$

For these values, we get a phase margin of 75^0 which was well above the required phase margin.

2.3 Design of common mode feedback loop 2

The second common mode detector is designed on similar lines to the first one (with replica bias) but instead of using a p-mos common mode detector, we use a resistive divider to detect the common mode voltage. The resistive divider along with the amplifier used are shown below.

Figure 3: Common detector 2 amplifier



The capacitors which are parallel to the common detector resisitors, C_2 have been set to a value of 5pF so that they act as load capacitor to the output stage and helps in decreasing the phase margin of the total system (it was 75^0 before the addition of these capacitors and is now 64^0). Helps make the system go from overdamped to underdamped and hence helps in settling faster.

The DC gain acheived here was 37.4dB(74) and phase margin is 74^0.

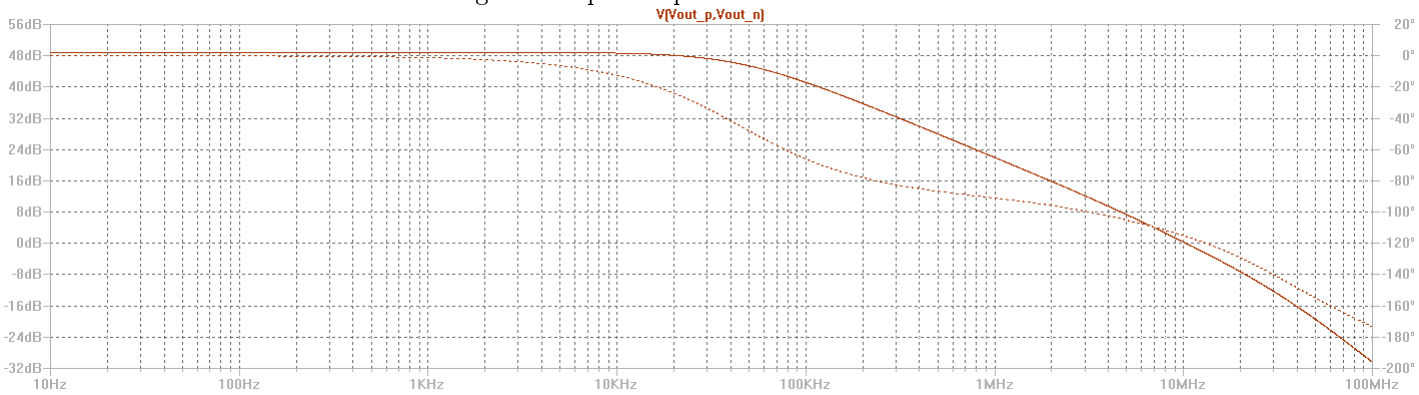
The compensation capacitor used here is

$$C_{cm2} = 0.59pF$$

Device name	W	L	g_m	$g_{ds}(\Omega^{-1})$	$V_{gs} - V_T$	I_D
M_{c20}	$18\mu m$	$0.72\mu m$	$1.67 \times 10^{-4} A/V$	6.21×10^{-5}	$0.202V$	$28.2\mu A$
M_{c21}, M_{c22}	$2.4\mu m$	$0.72\mu m$	$1.05 \times 10^{-4} A/V$	8.6×10^{-7}	$0.194V$	$14.1\mu A$
M_{c23}, M_{c24}	$1.2\mu m$	$0.72\mu m$	$1.02 \times 10^{-4} A/V$	1.05×10^{-6}	$0.205V$	$14.1\mu A$

2.4 Open loop analysis

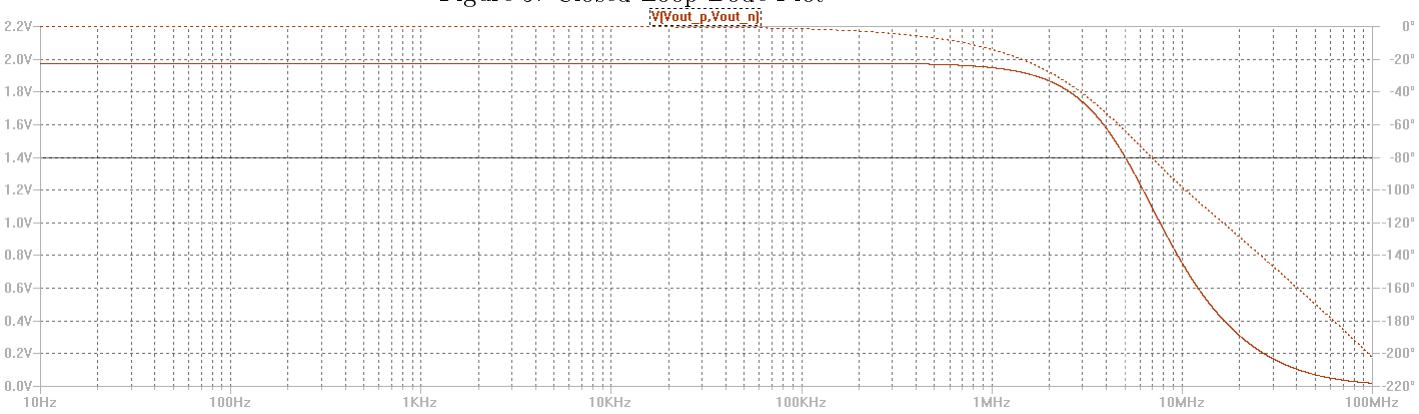
Figure 4: Open loop Bode Plot



The open loop Bode plot is shown above. We can clearly see that the 0 dB point is around 10MHz in the plot (the exact value is 10.3MHz) and the phase at the 0 dB point can be seen to be -116^0 and hence the phase margin is 64^0. It can also be seen from the above plot that ω_d is at 45KHz.

2.5 Closed loop analysis

Figure 5: Closed Loop Bode Plot

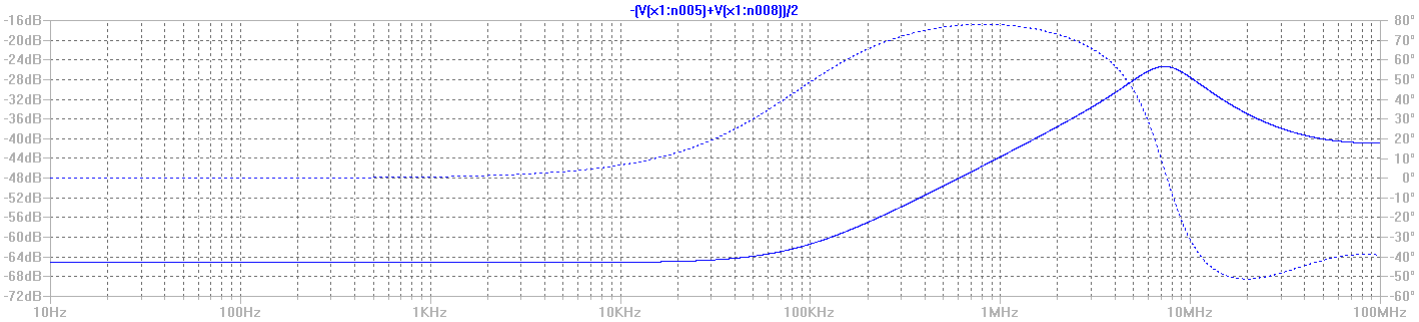


The closed loop gain of the amplifier is 1.976 and hence the 3-dB bandwidth correnspoding to a gain of 1.393 ($1.976/\sqrt{2}$) from the graph (the thick horizontal line) is 5.03MHz which is expected ($\omega_u/\sqrt{2}$).

2.6 First stage common mode response

The plot below shows the reponse to a common mode input (normalised i.e gain is shown below) at the first stage output. As expected the common mode of the first stage is low.

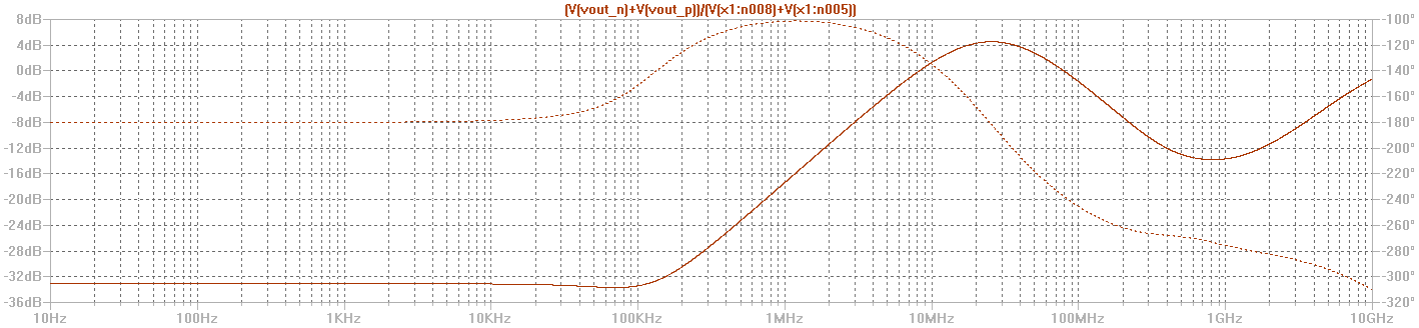
Figure 6: First stage common mode bode plot ((vop1+vom1)/2)



2.7 Second stage common mode gain

The plot below shows the second stage common mode loop gain magnitude.

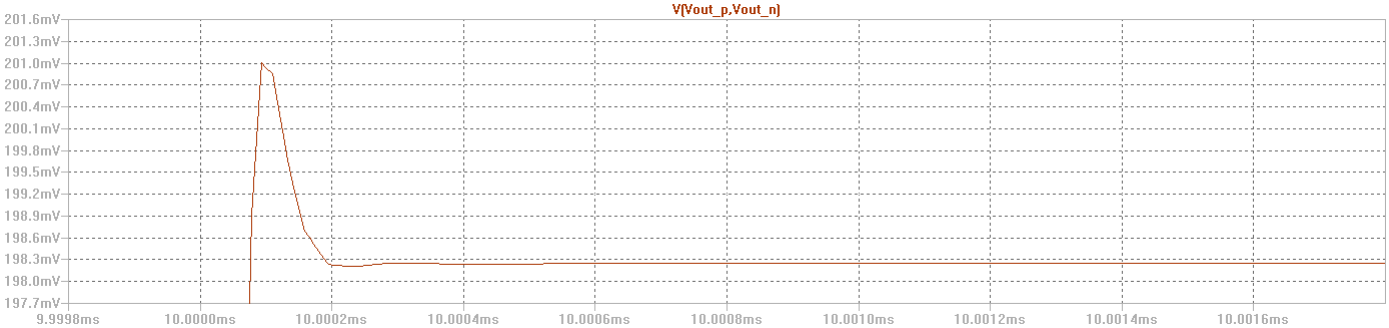
Figure 7: Second stage common mode loop gain bode plot (vop+vom)/(vop1+vom1)



2.8 Transient response with differential step

The following is the plot of the response for a 0.2V step differential input when the op-amp is in unity gain inverting mode. We expect a 200mV output as the opamp is in unity gain mode.

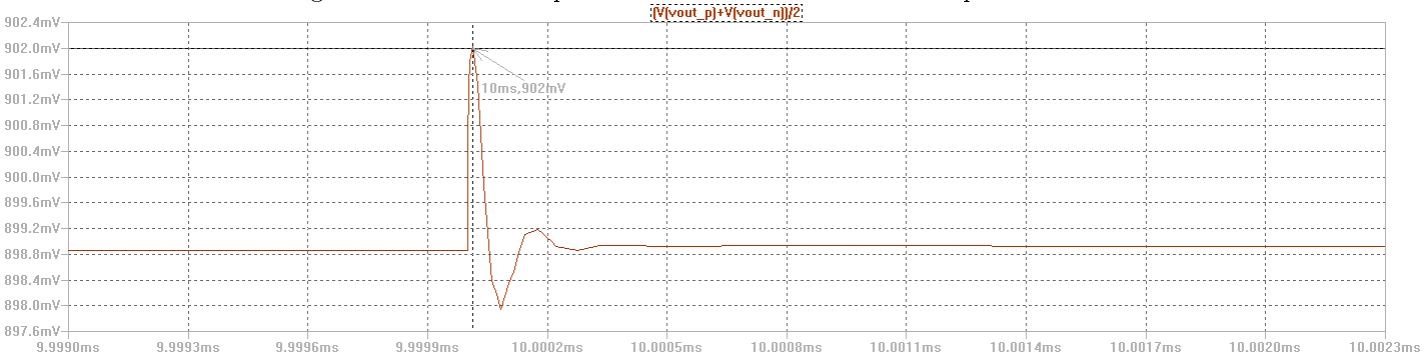
Figure 8: Transient response for a 0.2V differential step



2.9 Transient response with common mode step

The following is the plot of the response for a 0.1V common mode step input.

Figure 9: Transient response for a 0.1V common mode step



2.10 Input referred noise spectral density

The following are the plots of noise spectral density in open loop and closed loop conditions. And in the plot we shall plot the $1/f$ noise corner.

Figure 10: Open loop noise spectral density with $1/f(60.3Hz)$ marked

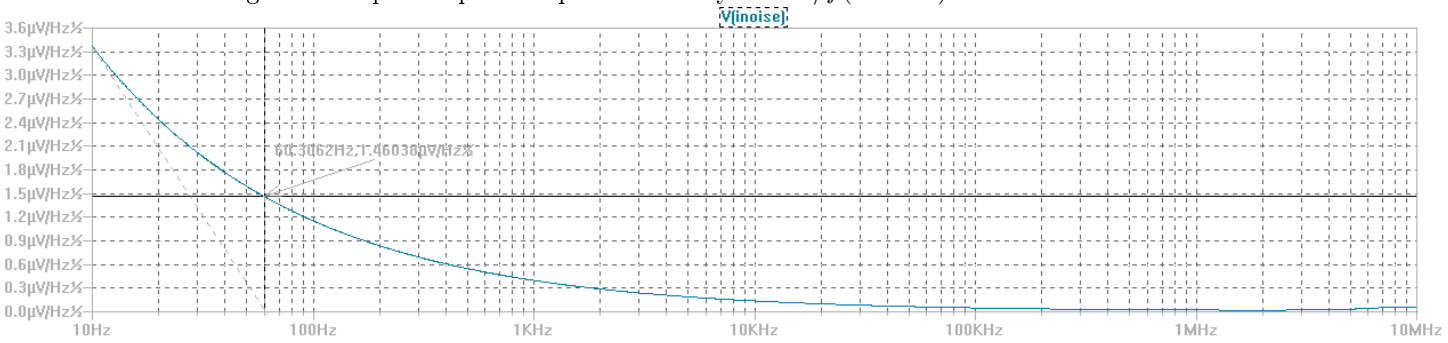
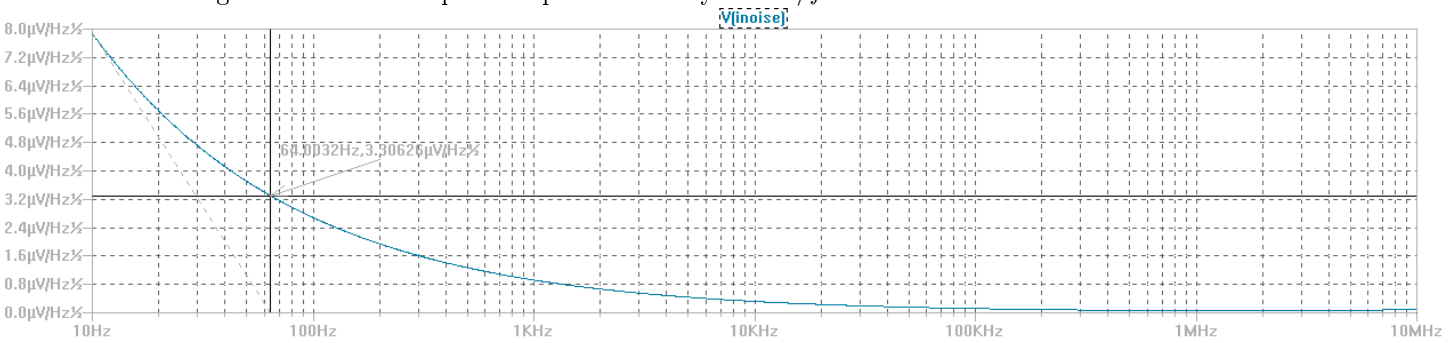


Figure 11: Closed loop noise spectral density with $1/f$ noise corner at 64Hz



2.11 Input referred offset voltage

By analysis we get the input referred offset to be by considering it as input voltage to get the difference (offset to 0) can be calculated to be,

$\sigma_{in} = \sqrt{(\sigma_{12}^2 + (\sigma_3 \frac{g_{m3}}{g_{m1}})^2 + (\sigma_{56} \times \frac{g_{o1}+g_{o3}}{g_{m1}})^2 + (\sigma_{78} \times \frac{g_{o1}+g_{o3}}{g_{m1}} \times \frac{g_{m7}}{g_{m5}})^2)}$,

Here, $\sigma = \frac{A_{vT}}{\sqrt{WL}}$

By substituting the values of various parmeters from the above tables we get offset voltage to be approximately, $2.34mV$

2.12 Other values asked in the question

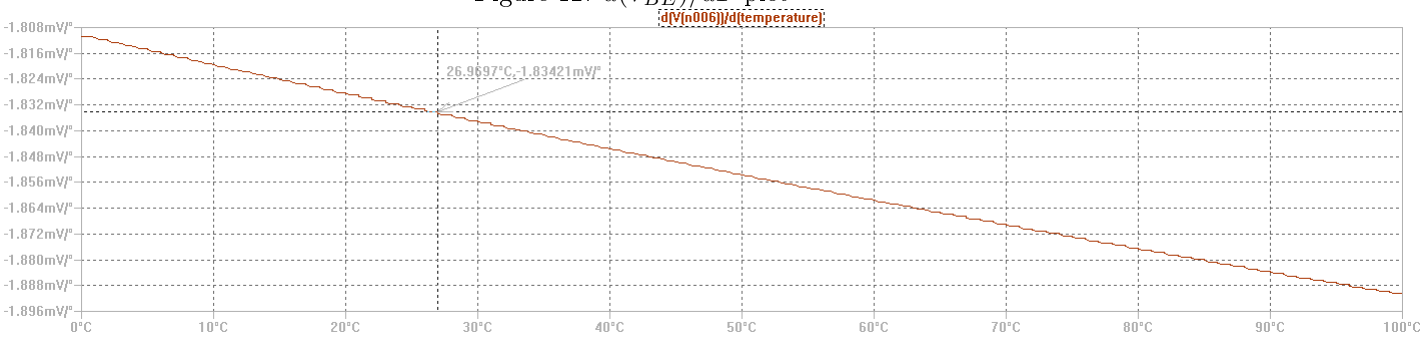
Total power consumed = 1.15mW

3 Bandgap Reference

3.1 Analysis

First we calculate the value of $\frac{dV_{BE}}{dT}$ by plotting in and taking the value at 27^0C (room temperature) as shown below. For the pnp model given, the value turns out to be -1.834mv/K at room temperature.

Figure 12: $d(V_{BE})/dT$ plot



Now, take a current of $5\mu A$ in each of the branches, and try to make V_{bg} constant at room temperature. From the circuit, we get

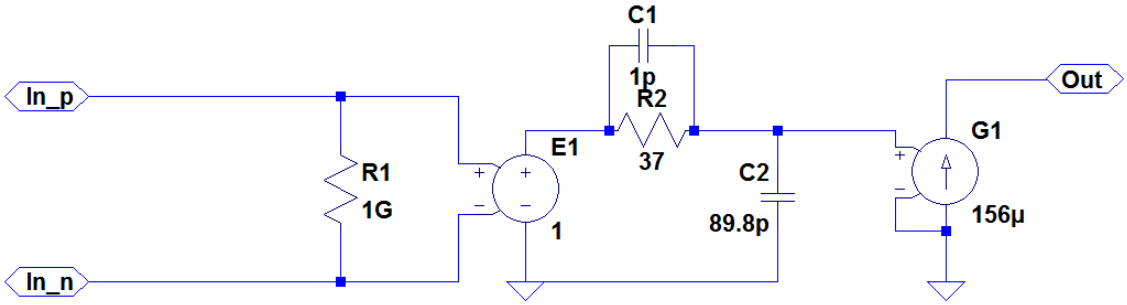
$$V_{bg} = V_{BE} + I_1 R_2$$

Differentiating on both sides we get,

$$\frac{dV_{bg}}{dT} = \frac{dV_{BE}}{dT} + \frac{dI_1}{dT} R_2$$

To drive the LHS of the equation to 0 at room temperature, we need to have RHS at 0 at room temperature.
We also have,
$I = \frac{V_2 - V_3}{R_1} = \frac{V_T ln(8)}{R_1} = 5\mu A$
From the above equation we get $R_1 = 10.77K\Omega$
Using the previous equation we get $R_2 = 110.100K\Omega$
We now try to model the first stage of the op-amp designed earlier.
By plotting it, we see that it has a pole at 47.89MHz and zero at 4.3GHz
Now, we try to model these values and put it into an ideal amplifier given in the question. The schematic of the amplifier has been shown below.

Figure 13: Schematic of the ideal amplifier given



Now we get the transfer function for this circuit to be,

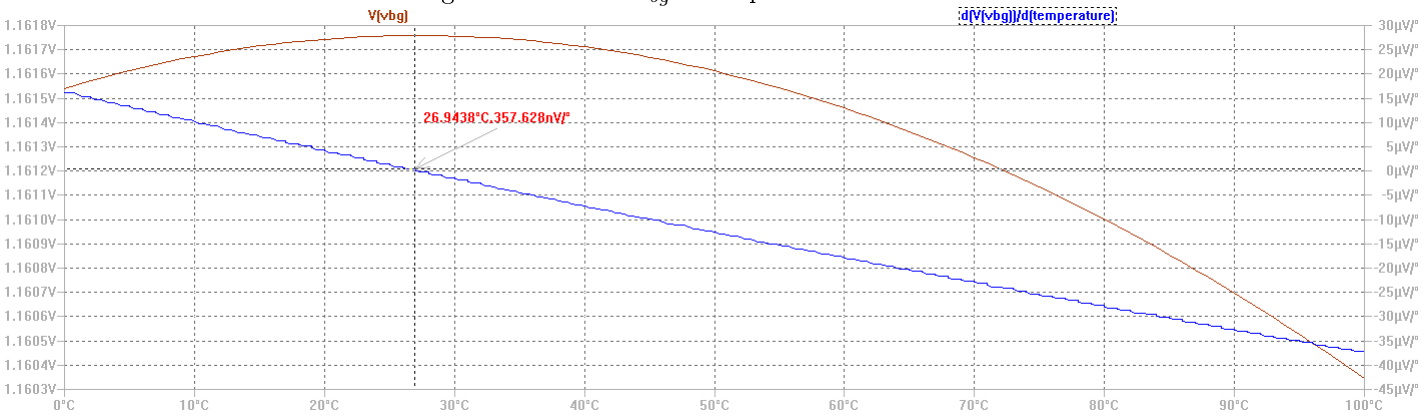
$$\frac{V(out)}{V(in)} = \frac{1 + sC_1R_1}{1 + s(C_1 + C_2)R_1}$$

So, we this also has one zero and one pole at $1/C_1R_1$ and $1/(C_1 + C_2)R_1$
By taking C_1 to be 1pF, we get the other values to,
$R_1 = 37\Omega$ and $C_2 = 89.8pF$ and $G_m = 156\mu S$

3.2 Simulations with the ideal model

We keep the ideal model of the amplifier mentioned above and simulate. The V_{bg} plot for a temperature sweep is shown below.

Figure 14: Plot of V_{bg}vs temperature



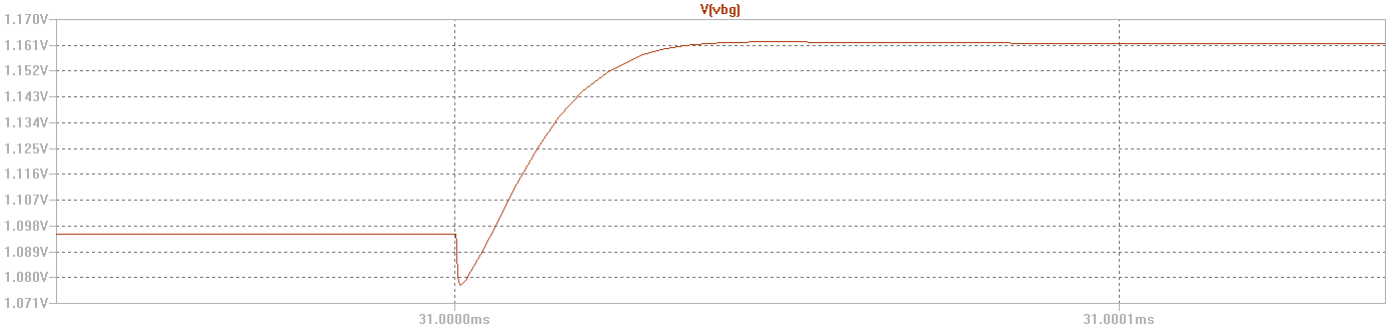
We can see from the plot that variation of V_{bg}vs temperature at room temperature is very low $357.628nV/^0$which is nearly 0. For this the values of resistances and the capacitances were slightly tweaked and the new values are,

$R_2 = R_3 = 115K\Omega$ and $R_1 = 11.735K\Omega$

and to get less than 10% overshoot the emperical value of the capacitance used is $0.05pF$ (even no capacitor achieved similar results).

The transient response of the $1\mu A$ impulse at the output of the opamp is shown below.

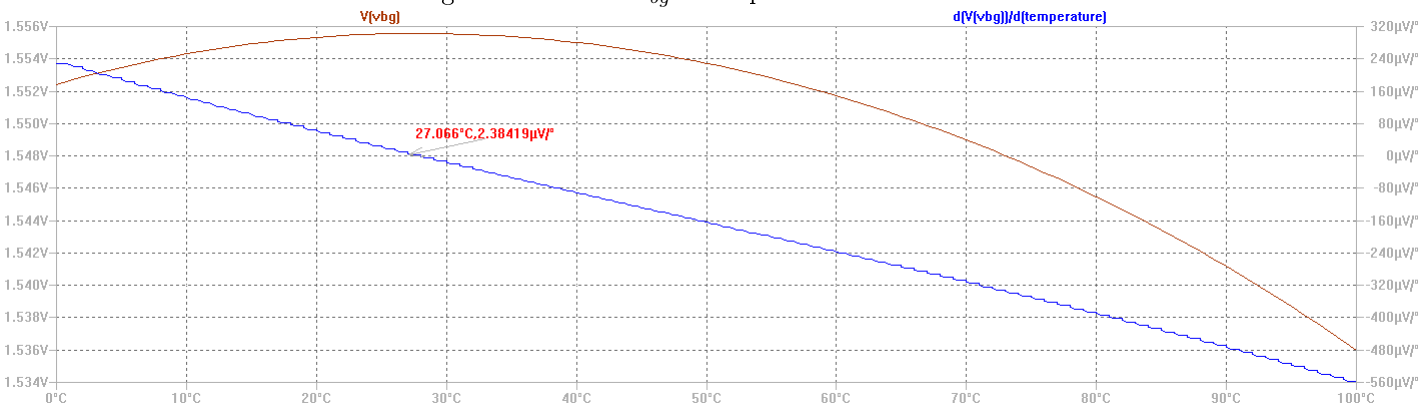
Figure 15: Transient response for current step



3.3 Simulations with actual one stage op-amp

By replacing the idela model in the previous part with the real opamp the V_{bg} plot for a temperature sweep is shown below.

Figure 16: Plot of V_{bg}vs temperature



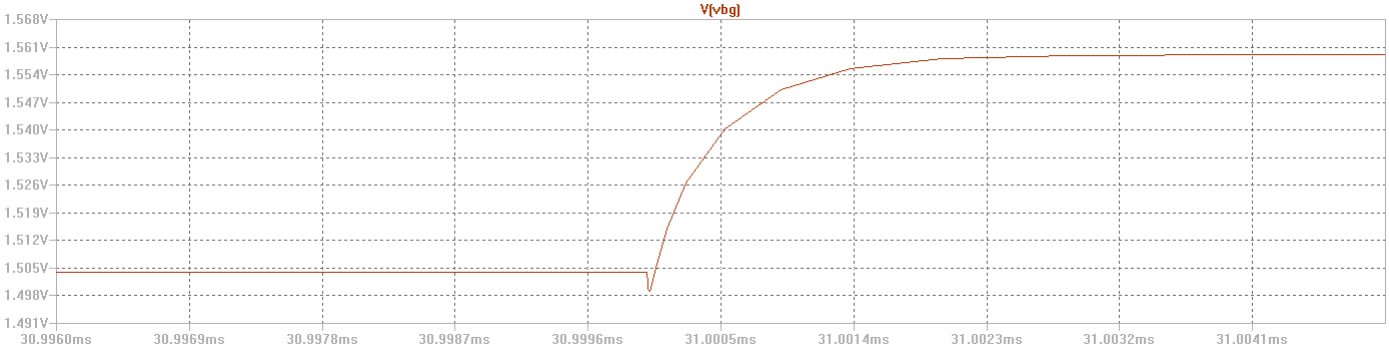
Here too we got a very small gradient for the output voltage at room temperature. For this circuit, the new values (after sweeping various resistances) are

$R_2 = R_3 = 120K\Omega$ and $R_1 = 7.15K\Omega$

and to get less than 10% overshoot the emperical value of the capacitance used is $1.2pF$.

The transient response of the $1\mu A$ impulse at the output of the opamp is shown below.

Figure 17: Transient response for current step



3.4 Loop gain of bandgap reference

We get the following plots for loop gain of the bandgap reference circuit

Figure 18: Loop Gain (with real amplifier)

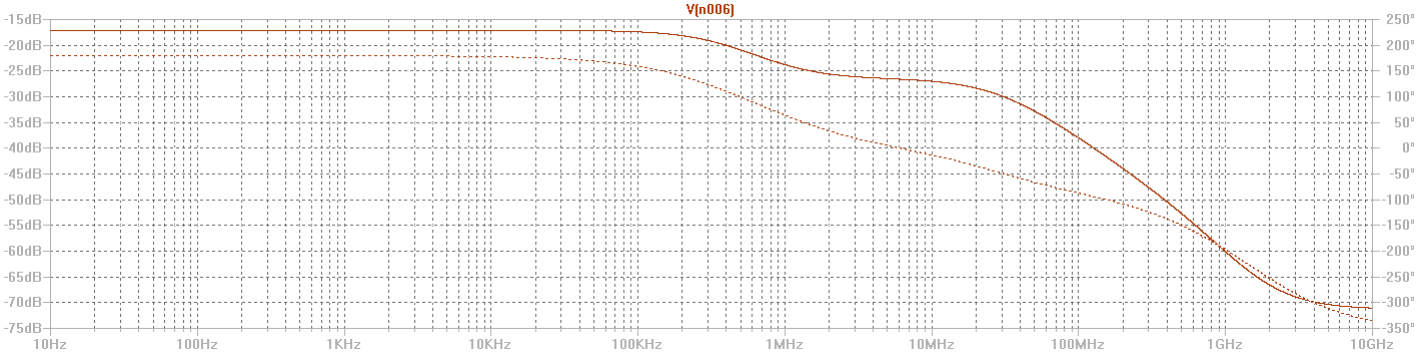


Figure 19: Loop Gain (with ideal amplifier)