

Fundamentals and Applications of Modern Single-Photon Detector Circuits and Processing Systems

Part 2: Applications

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Part 2: Outline

- Silicon Photomultipliers
 - Modelling
 - Readout architectures
 - Applications

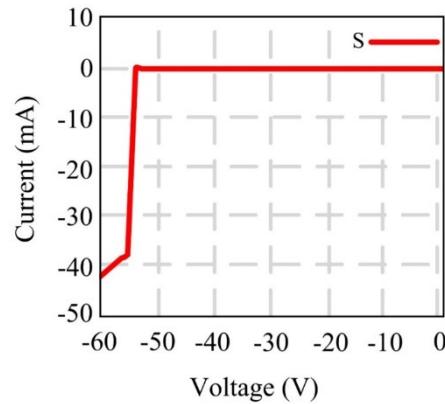
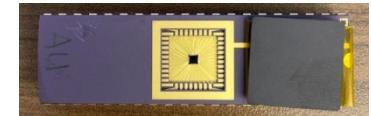
Learning Outcomes

1. Models for SPADs and SiPMs
2. SiPM configurations
3. Example Implementations

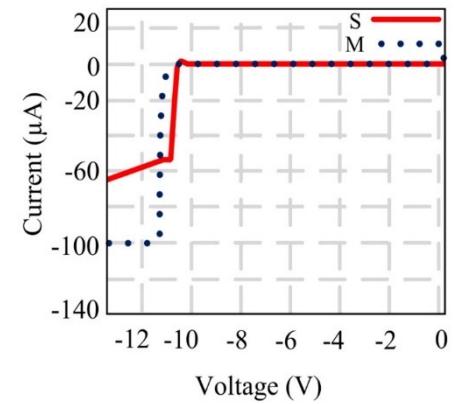
SiPM Configurations and Models

Commercial vs CMOS SiPM

- Simulation in Cadence using a SPAD SPICE model
- The custom CMOS SiPM active area is 2×2 mm and microcell dimensions are $20 \mu\text{m}$.
- The Hamamatsu S13360 is 6×6 mm and microcell dimensions are $50 \mu\text{m}$.



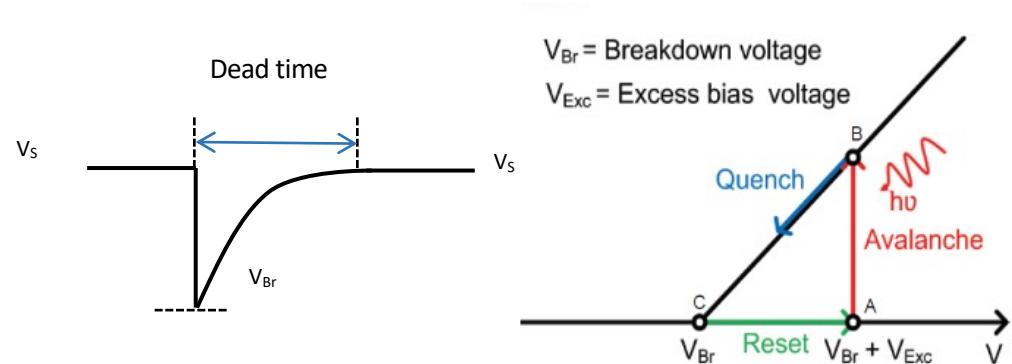
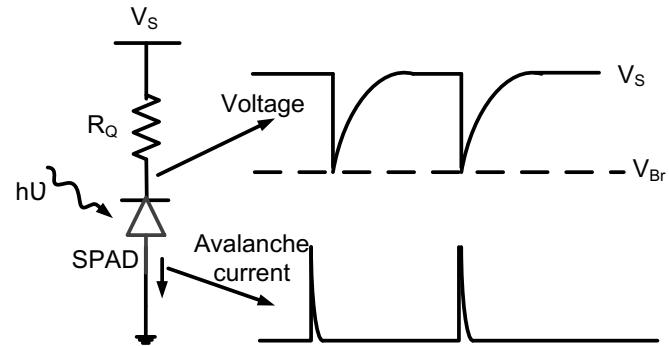
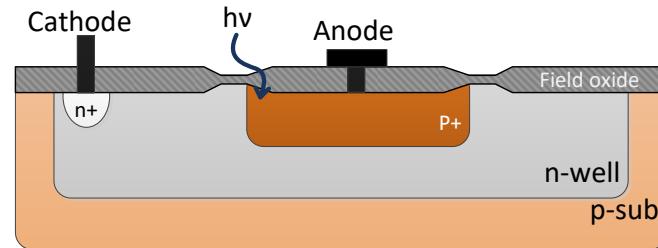
HAMAMATSU



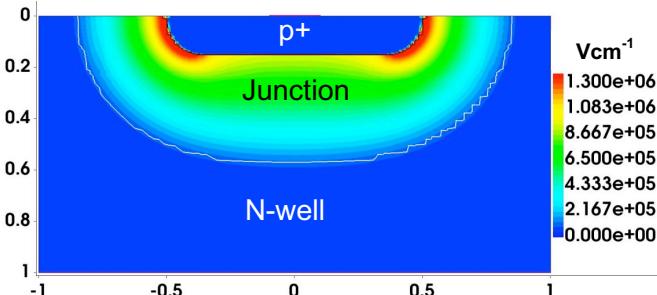
Custom CMOS SPAD

Single Photon Avalanche Diode

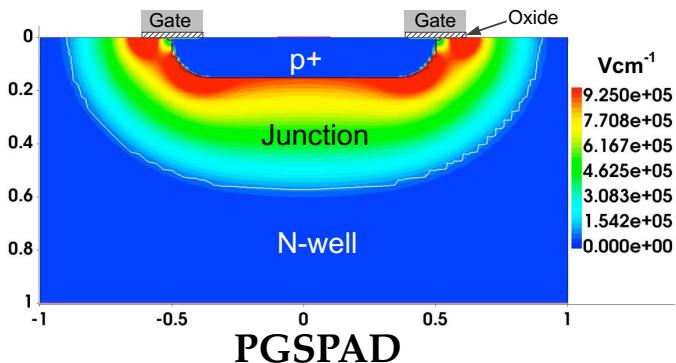
- SPAD is a pn junction biased just above breakdown voltage
- Photon initiates impact ionization in depletion region
- After absorbing energy from the photon, frees carrier drift with the electric field, causing ionization and triggering an avalanche
- Local current density increases rapidly until quenched



Perimeter Gated SPAD (PGSPAD)

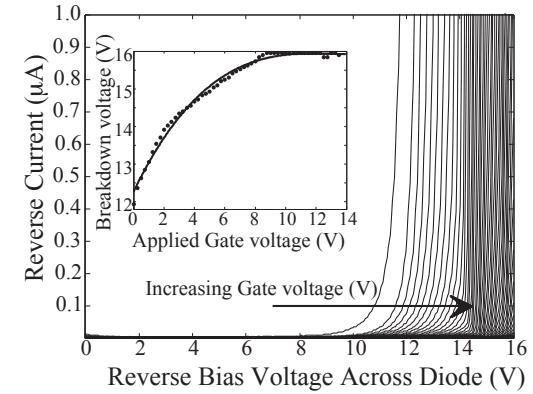
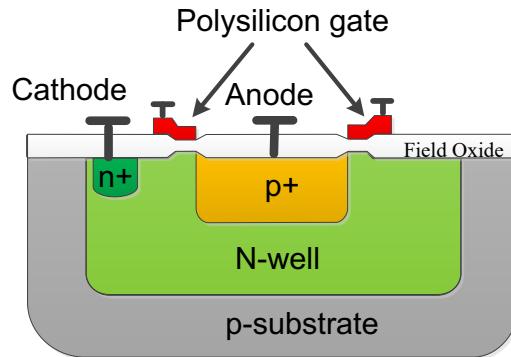


SPAD



PGSPAD

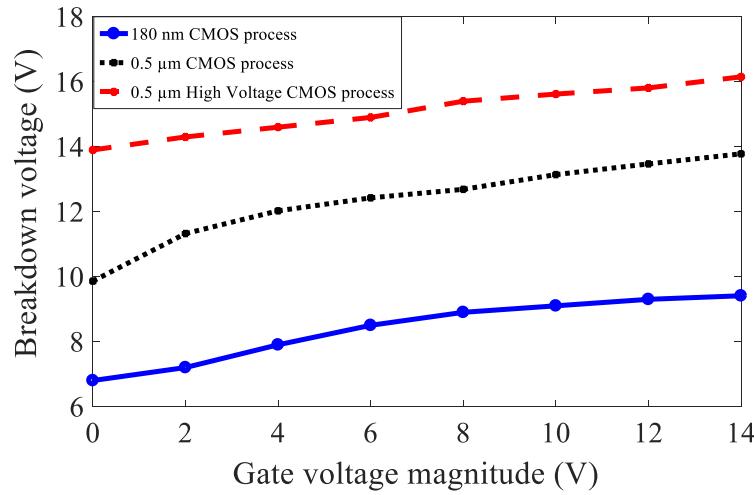
(x-axis and y-axis are in μm)



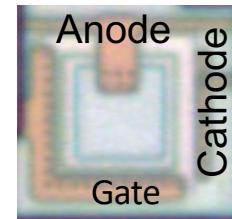
Advantages of PGSPAD:

- Uniform electric field distribution
- Prevents premature edge breakdown
- Within fabrication design rules
- Control breakdown voltage
- Tune noise floor

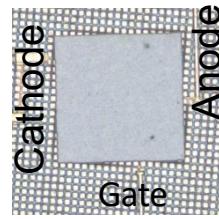
Breakdown Voltage vs Gate Voltage For PGSPAD



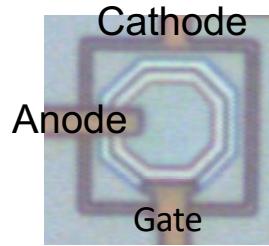
Breakdown voltage increases with gate voltage



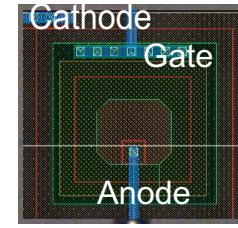
0.5 μm CMOS



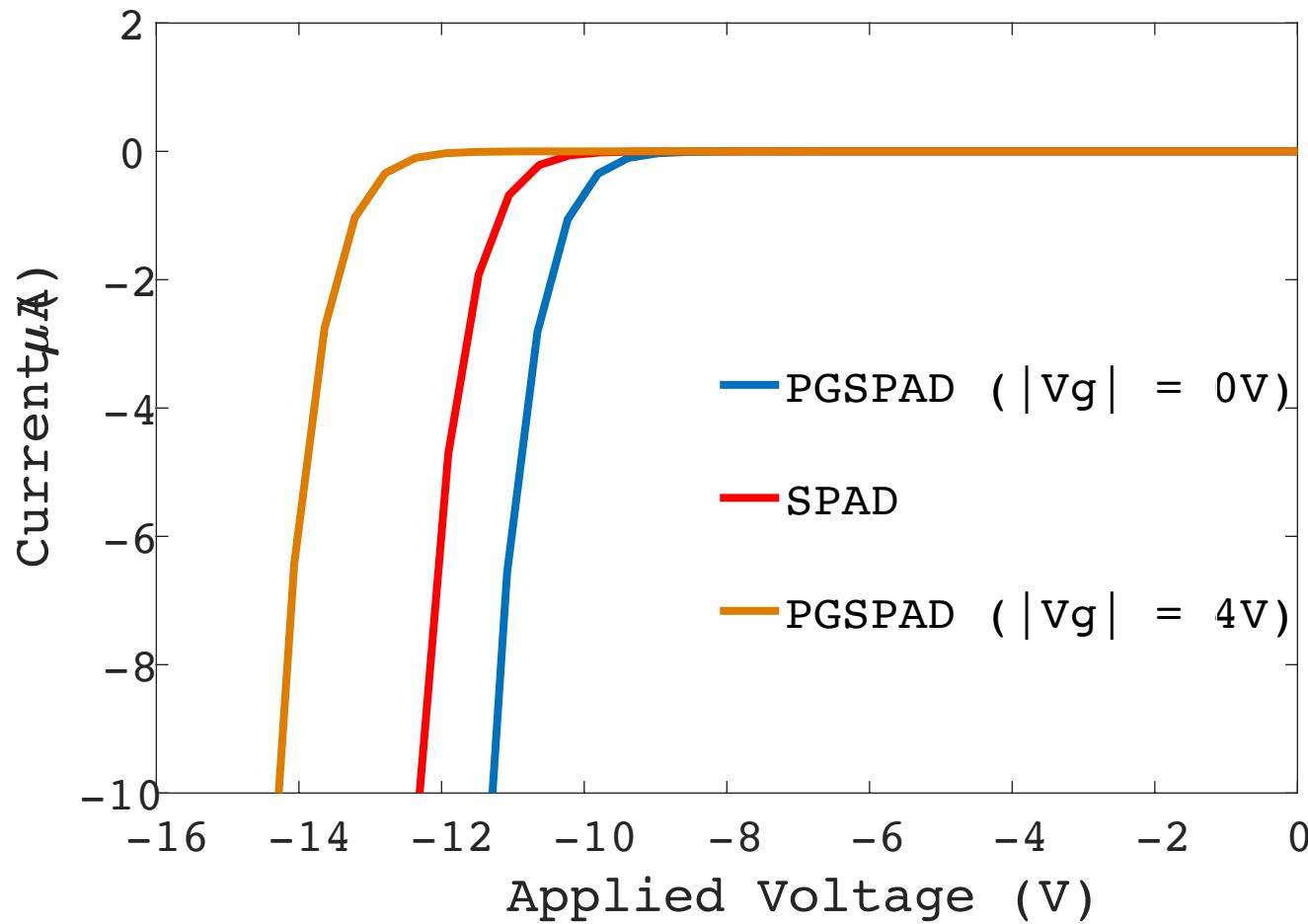
0.5 μm HV CMOS



180nm CMOS



PGSPAD vs SPAD with single implant



Models

Class 1

Semiconductor level
Semi-classical
Quantum mechanics

Breakdown voltage avalanche gain

Class 2

Equivalent circuit representation
DC I-V characteristics
Geiger mode temporal
characteristics

Class 3

Equivalent circuit representation
Stochastic nature

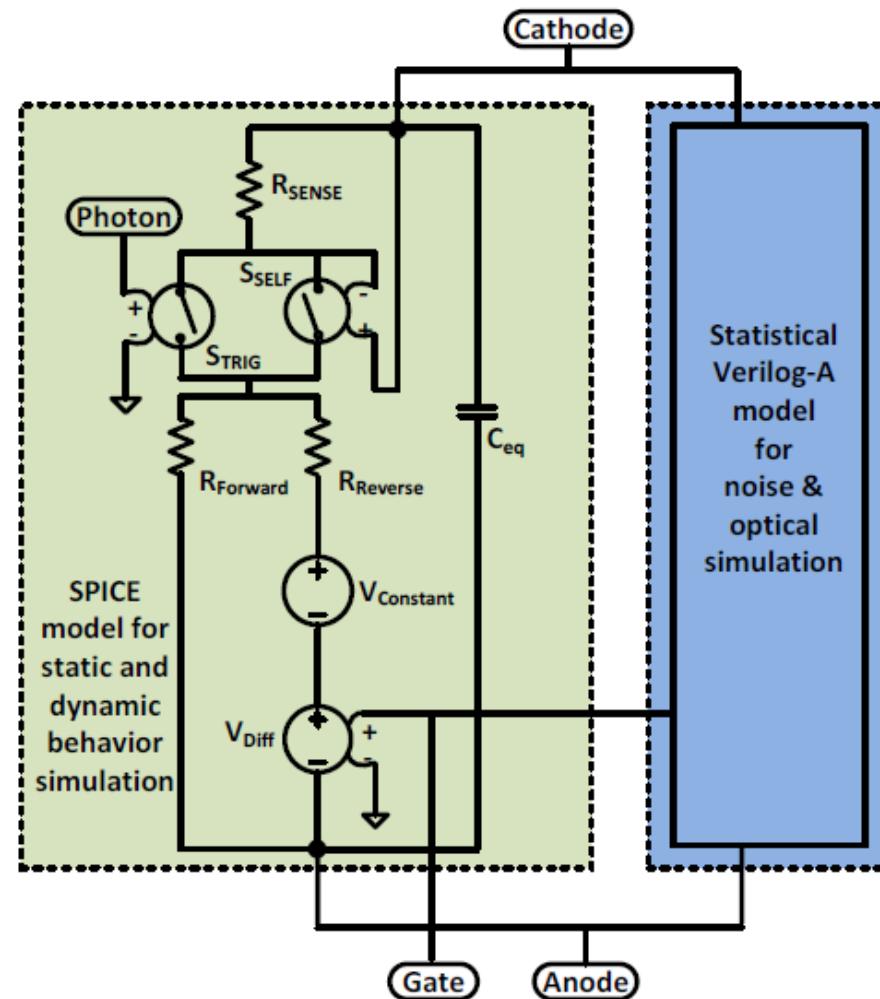
Dark count rate
Afterpulsing
Breakdown probability

Class 4

System level model
Array behavior
Pixel cross talk
Non-uniformity

Modeling

- IV simulation
- Timing simulation
- Noise simulation
- Optical simulation



SPICE Model

- $R_{Reverse} = Ae^{-B(V_{CA} + \alpha V_G^2 + \beta V_G)}$
- $R_{Forward} = Ce^{-D(V_{CA})}$
- $V_{BV} = V_{Constant} + V_{Diff}$
- $V_{Diff} = \alpha V_G^2 + \beta V_G$

$A, B, C, D, \alpha, \beta$ are constants

V_{CA} = Voltage between cathode and anode

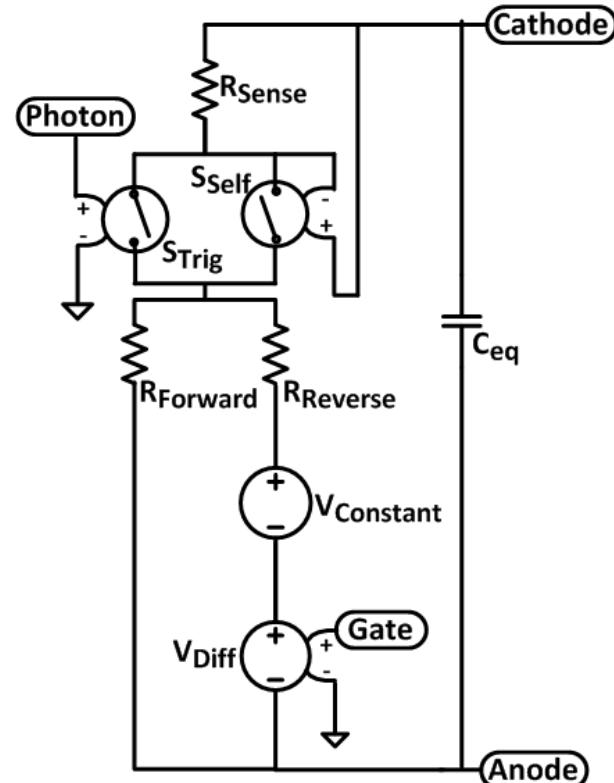
V_{BV} = Breakdown voltage

V_G = Gate voltage

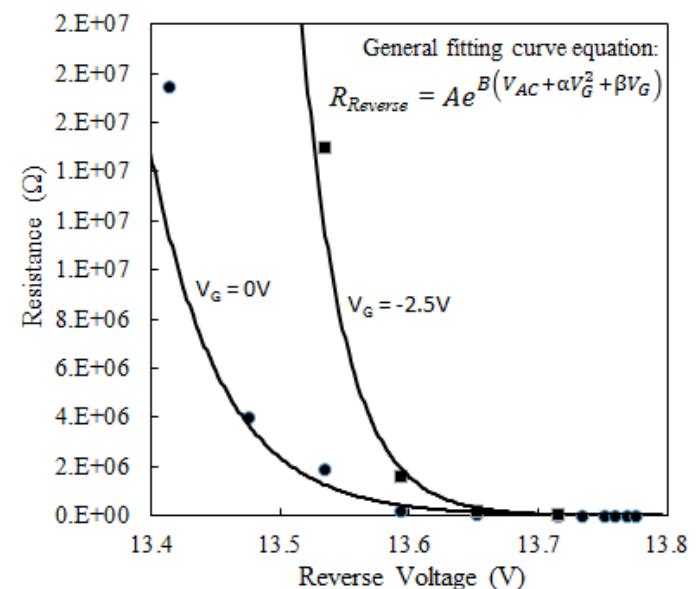
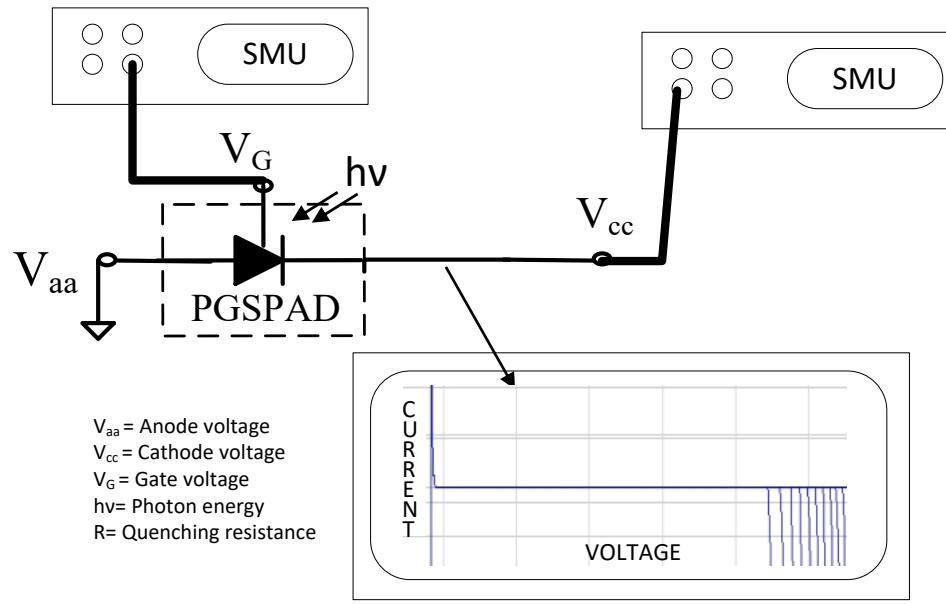
$R_{Forward}$ = Resistance acting in forward bias

$R_{Reverse}$ = Resistance acting in reverse bias

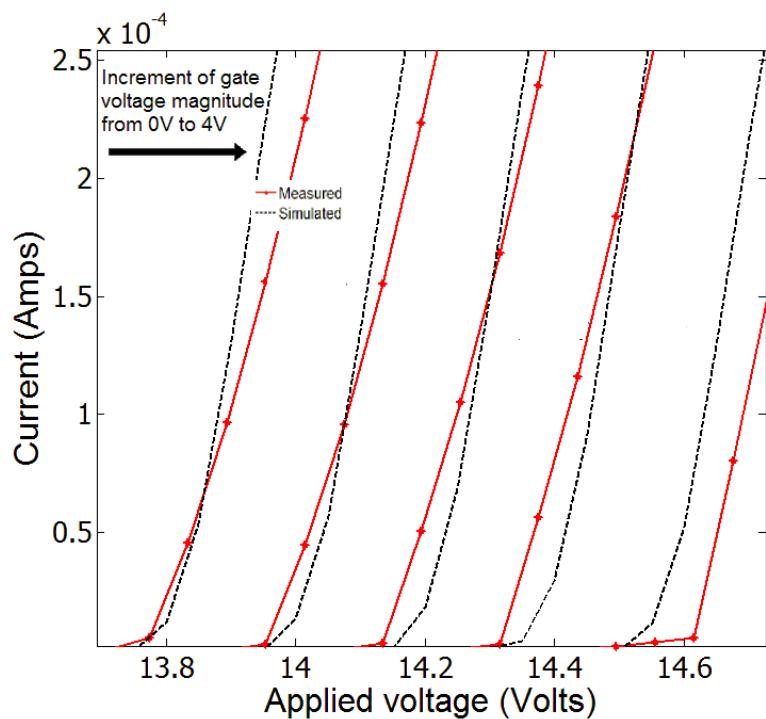
V_{Diff} = Gate voltage dependent voltage source to model the variation in breakdown voltage



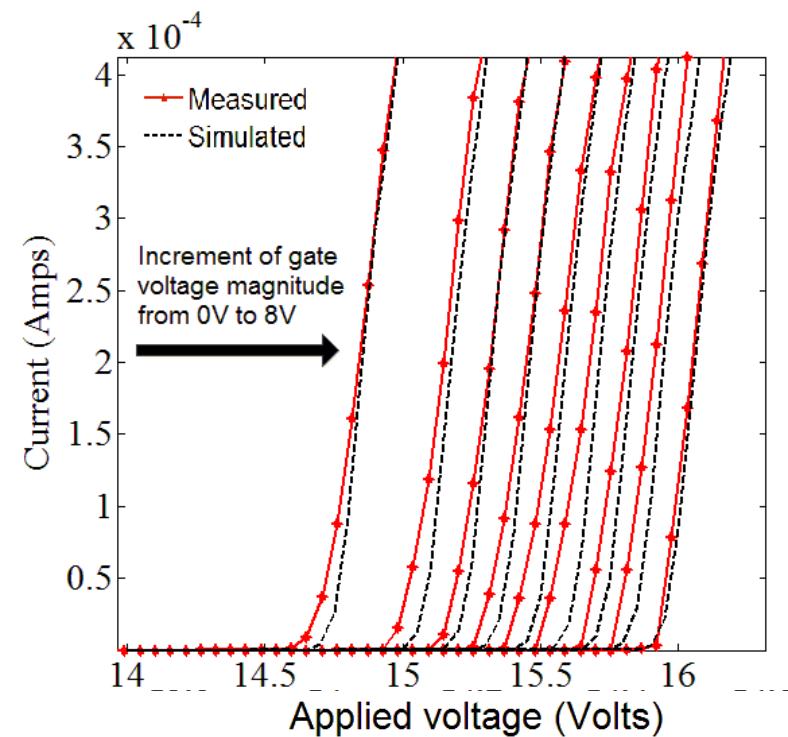
Parameter Extraction



Reverse IV Characteristics

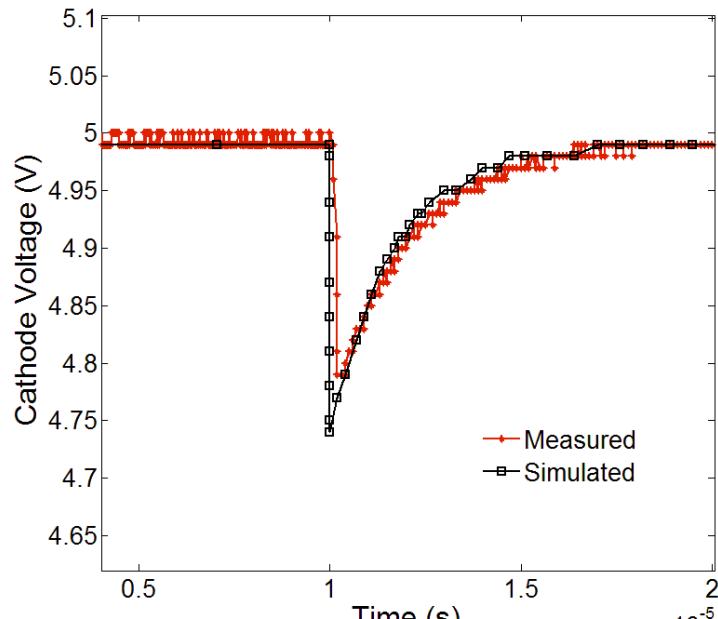


Device # 1

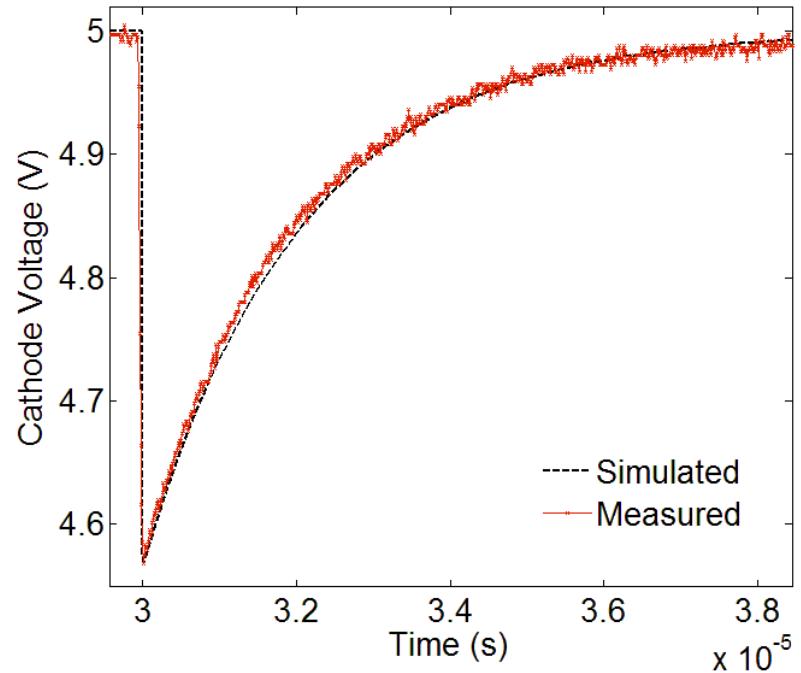


Device # 2

Dynamic Characteristic

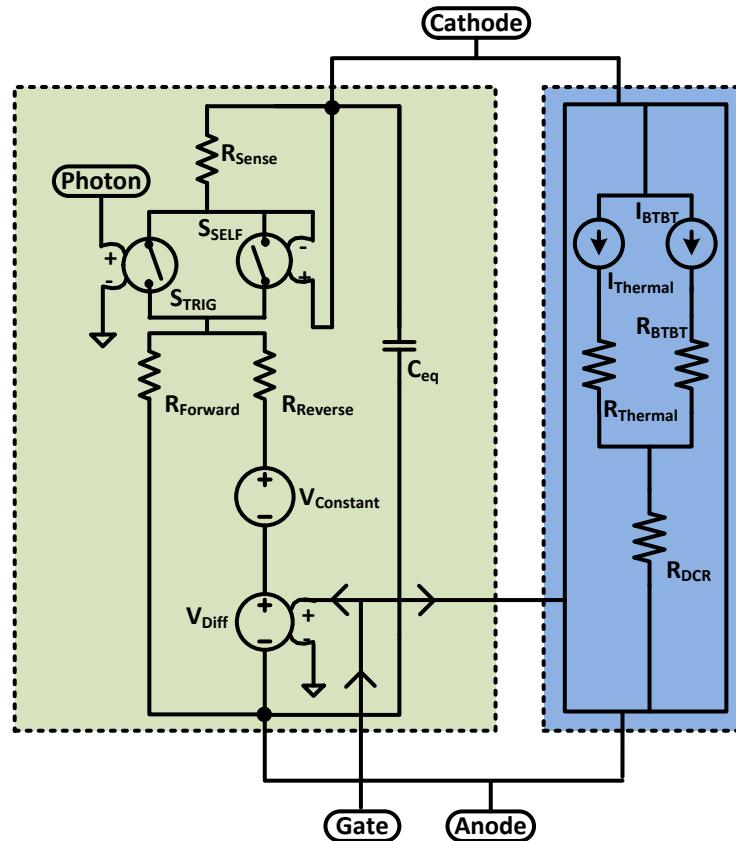


Device # 1



Device # 2

SPICE Model



Noise Modeling

$$CGR_{Thermal} \approx \frac{n_i v_{th} \sigma_0 N_t}{2} \times A_{Active} W_D$$

$$CGR_{BTTB} = \frac{\sqrt{2m^*} q^2 F V_R}{h^2 \sqrt{E_g}} \exp\left(-\frac{8\pi\sqrt{2m^*} E_g^{3/2}}{3qFh}\right) A_{Active}$$

$$P_{Av} = \begin{cases} 0, & V_{Exc} < 0 \\ 1 - e^{-\frac{V_{Exc}}{\eta_T V_{Br}}}, & V_{Exc} \geq 0 \end{cases}$$

$$DCR = P_{Av} \times CGR$$

A_{Active} = Active area

W_D = Depeltion width

N_t = density of generation centers

v_{th} = Thermal velocity

σ_0 = Carrier capture crosssection

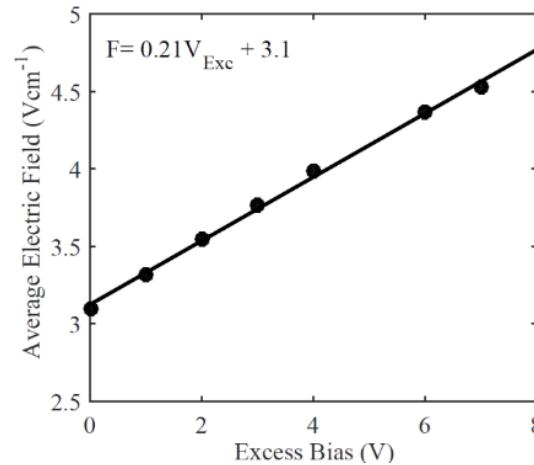
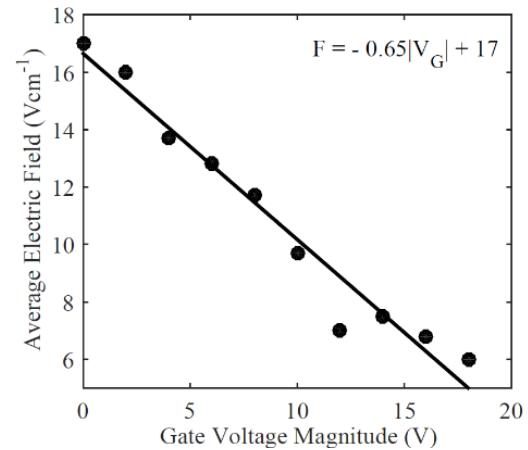
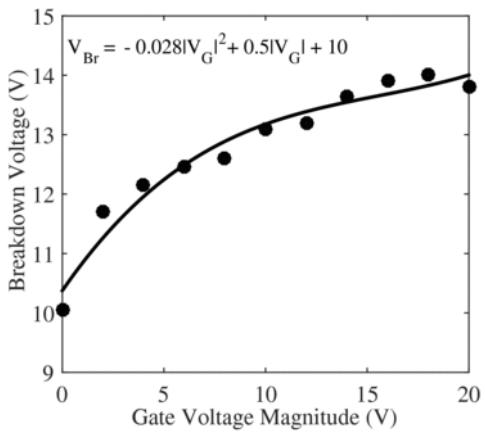
P_{Av} = Avalanche probability

Parameters affecting noise:

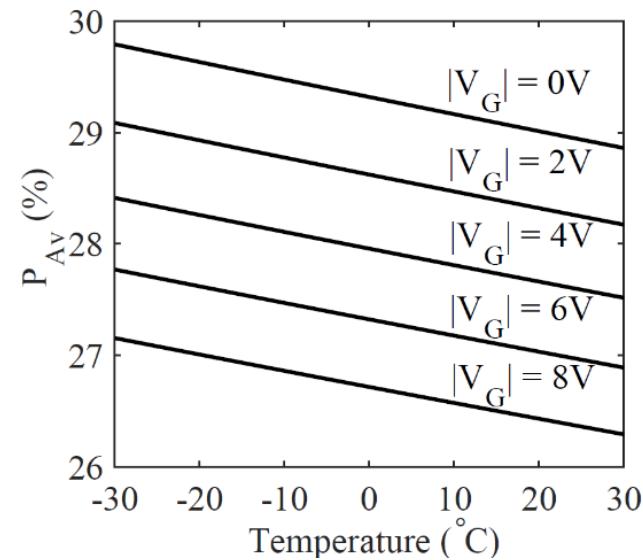
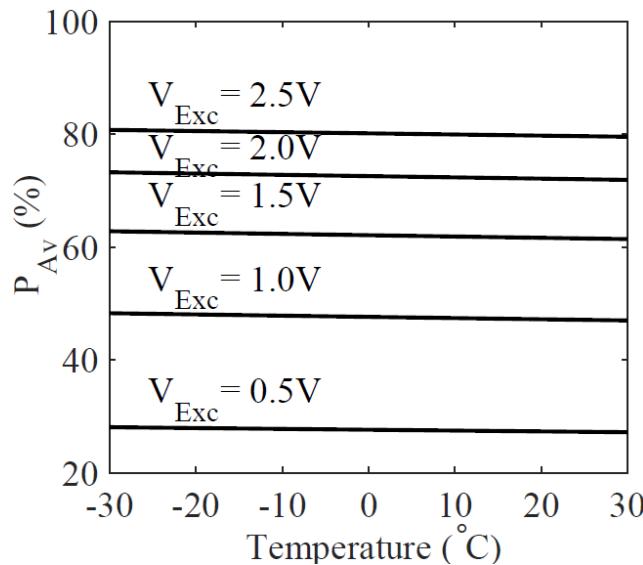
- Average electric field (F),
- Applied reverse voltage (V_R),
- Breakdown voltage (V_{Br}),
- Excess bias voltage (V_{Exc})

Noise Modeling

- Breakdown voltage (V_{Br}) \uparrow , $V_G \uparrow$
- Average Electric field (F) \uparrow , $V_G \downarrow$
- Average Electric field (F) \uparrow , $V_{Exc} \uparrow$

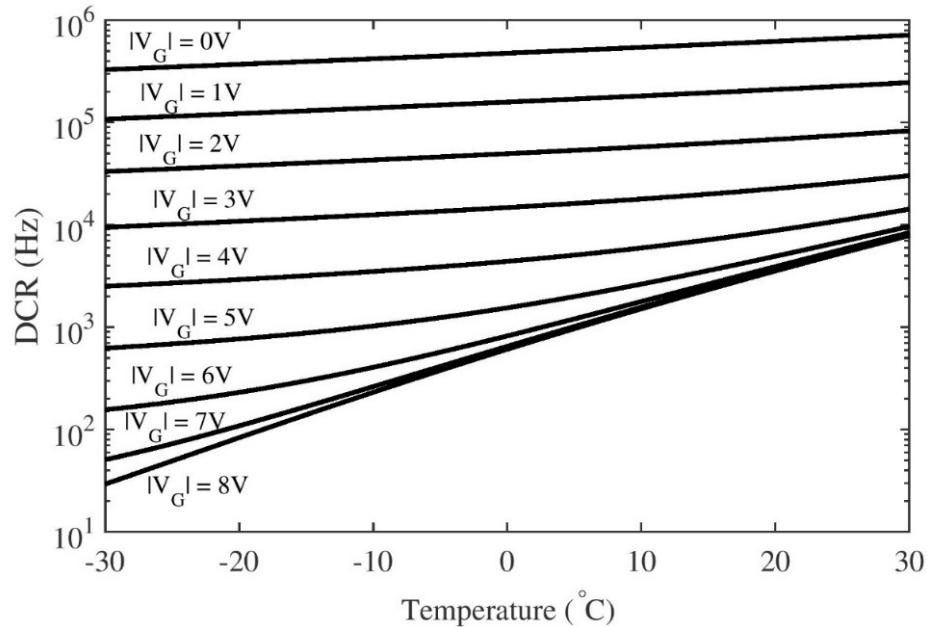
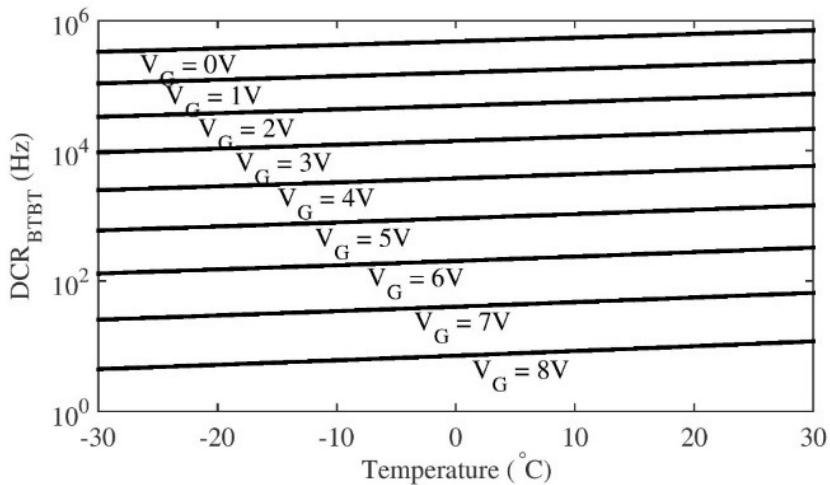
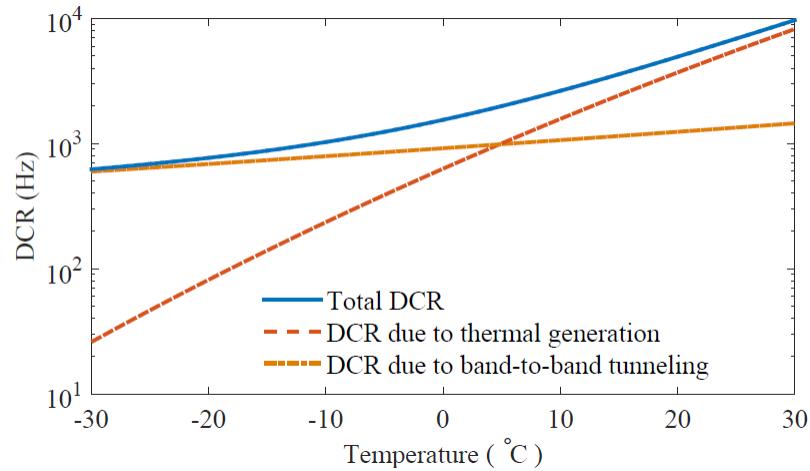


Noise Modeling – Avalanche Probability

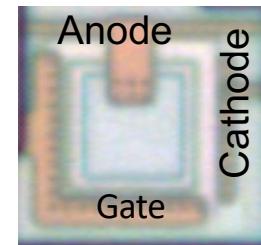
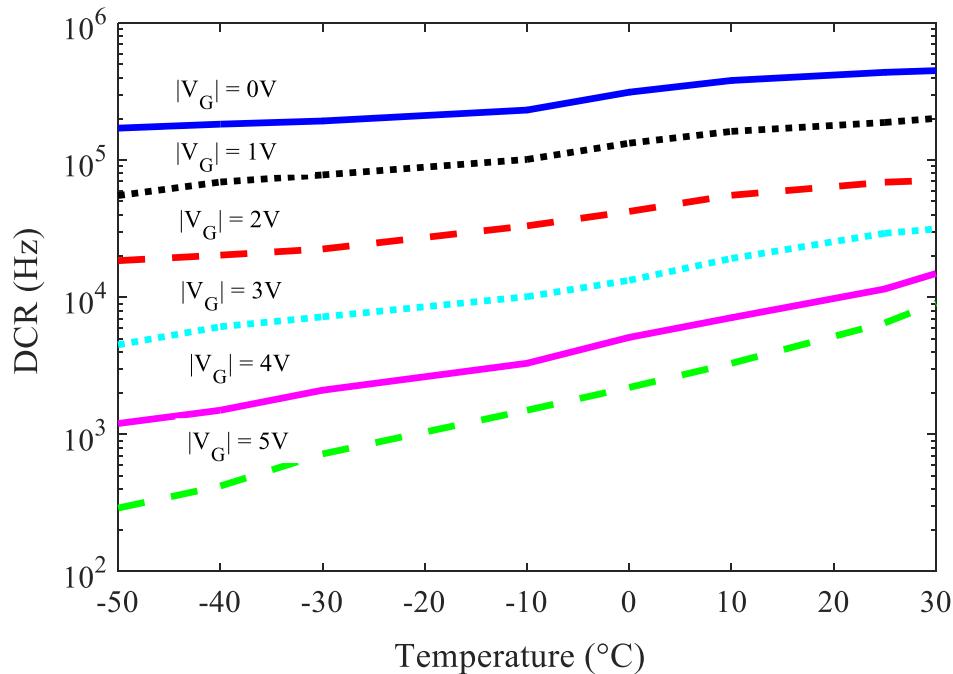


$$P_{Av} = \begin{cases} 0, & V_{Exc} < 0 \\ 1 - e^{-\frac{V_{Exc}}{\eta_T V_{Br}}}, & V_{Exc} \geq 0 \end{cases}$$

Noise Modeling – DCR



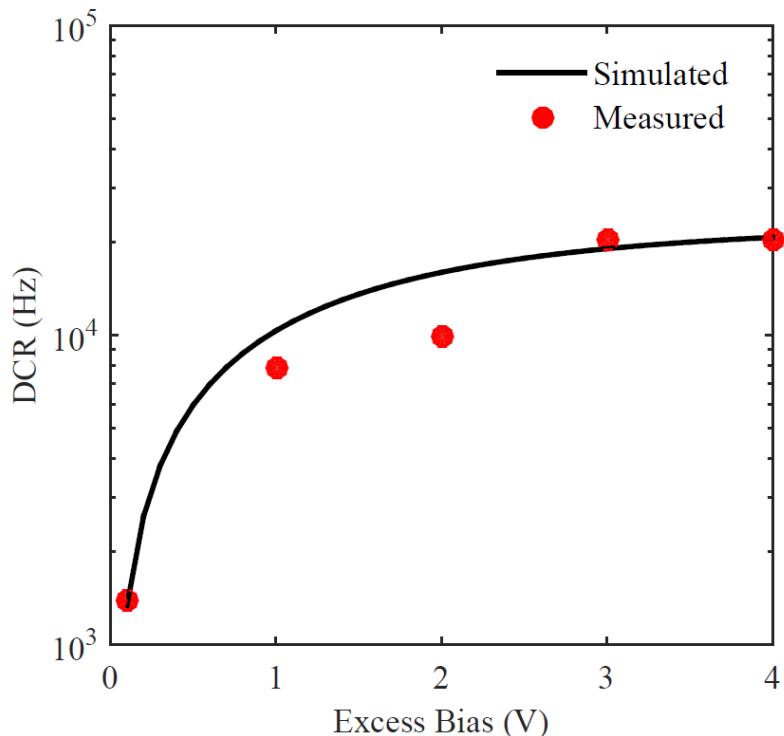
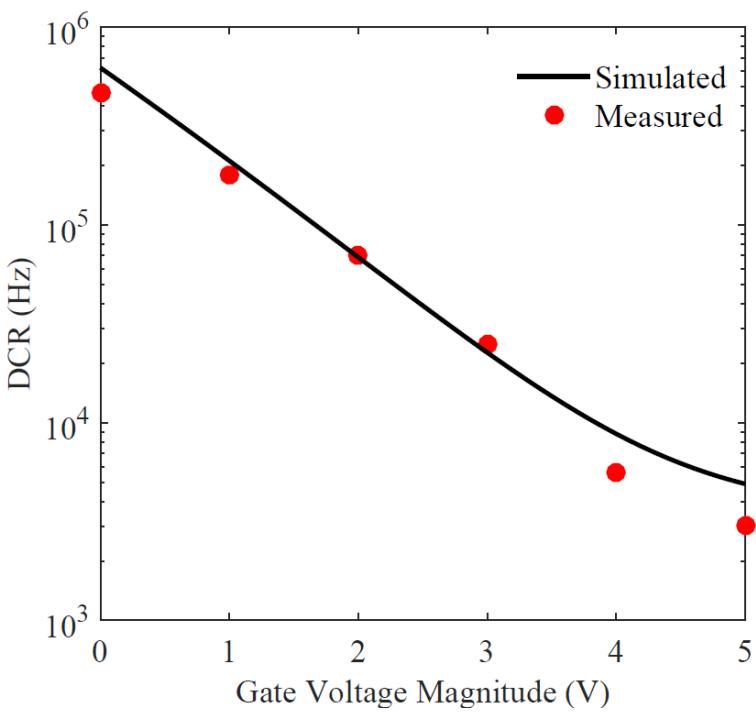
Noise Reduction



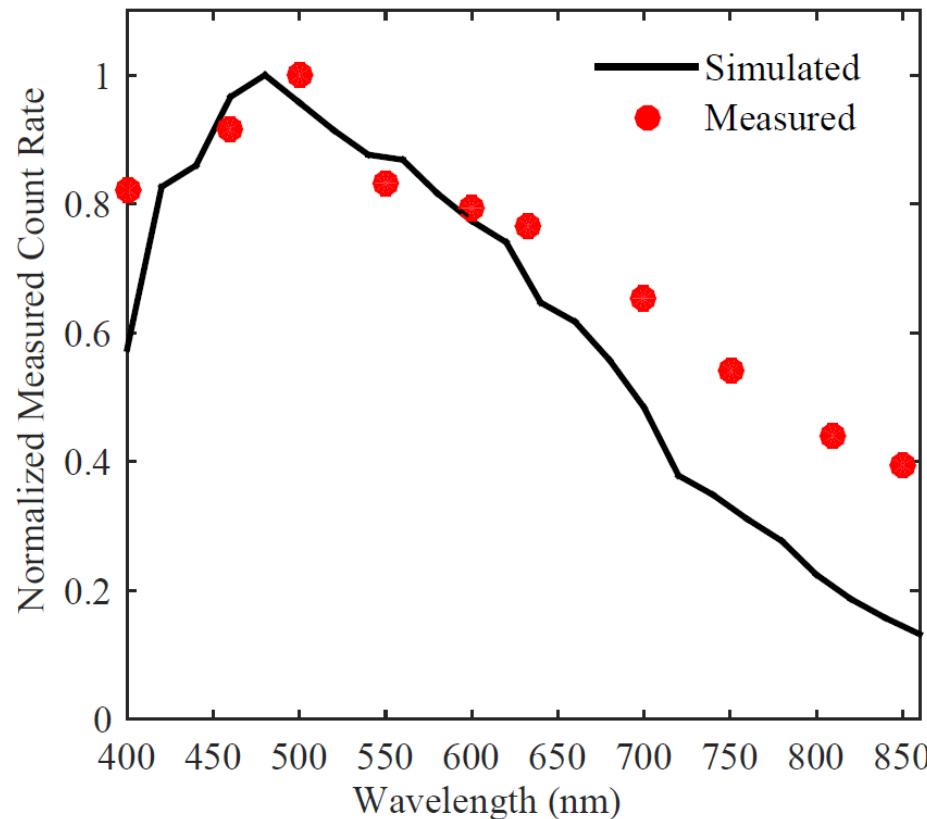
Experimental measurement

- Applied gate voltage reduces dark count rate (noise)
- Reduction of noise is primarily caused by reduction of band-to-band noise

Noise Modeling



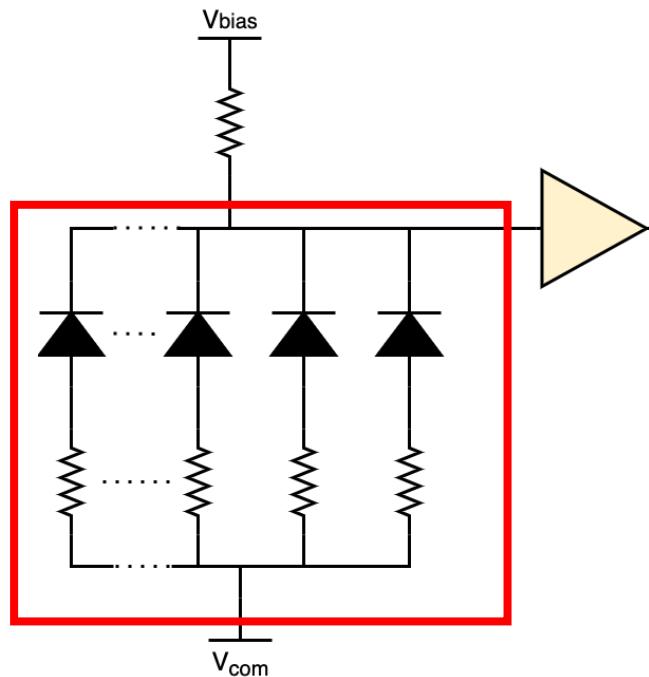
Optical Simulation



$$PDP(\lambda) = QE^*(\lambda) \times P_{Av}$$

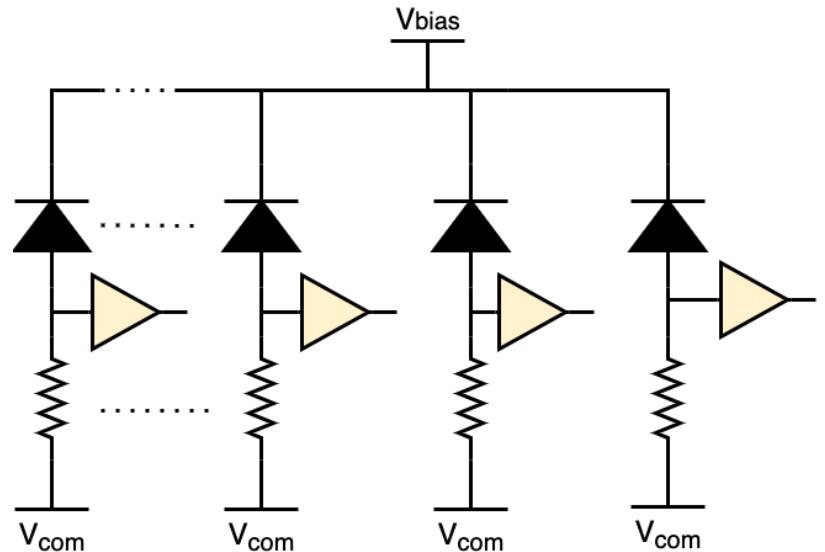
SiPM Types

Analog SiPM



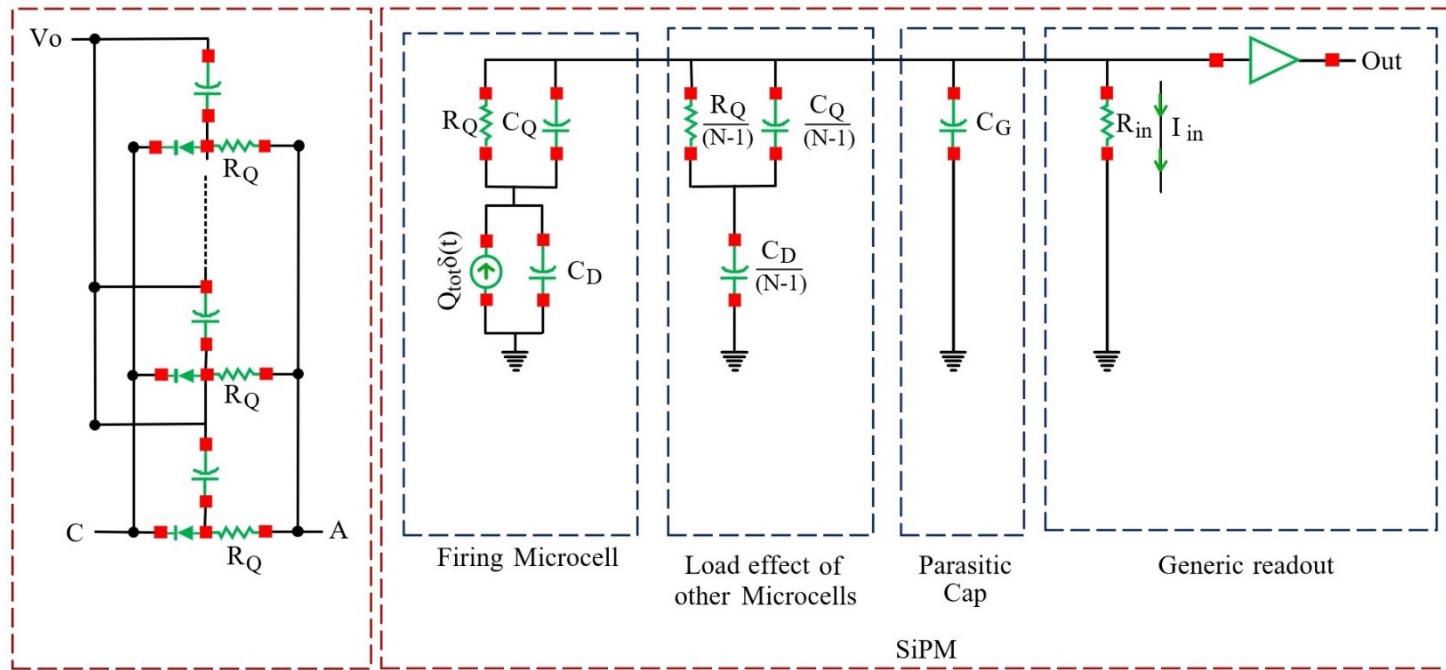
Total current is measured as output

Digital SiPM

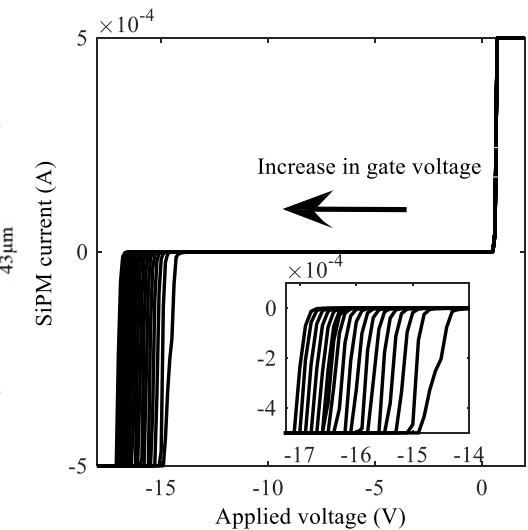
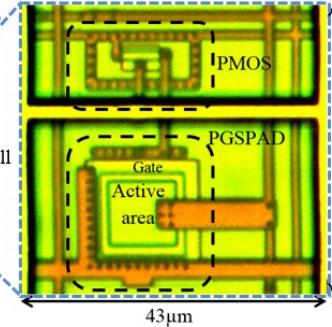
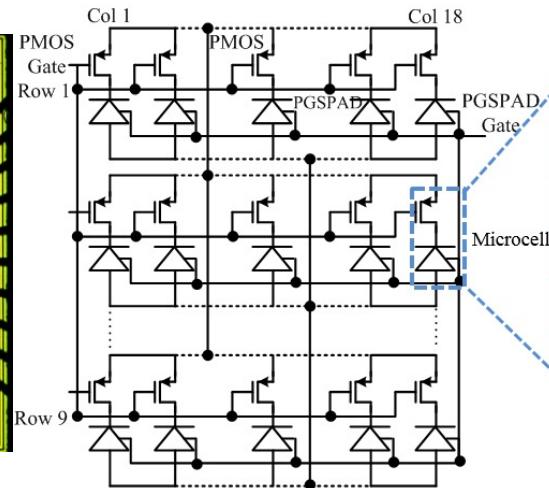
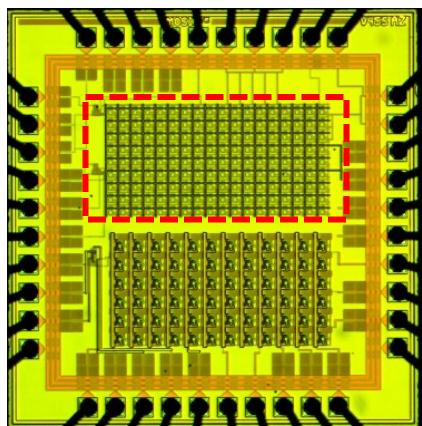


Total count rate is measured as output

SiPM Model

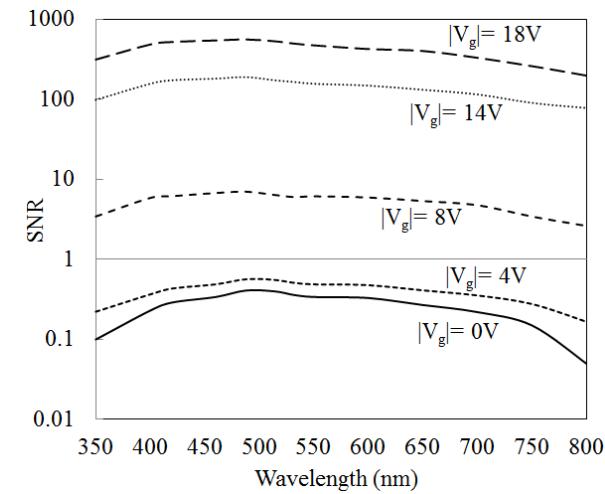
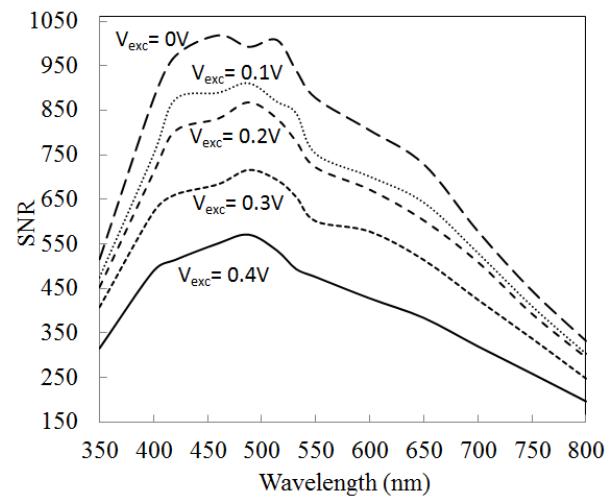
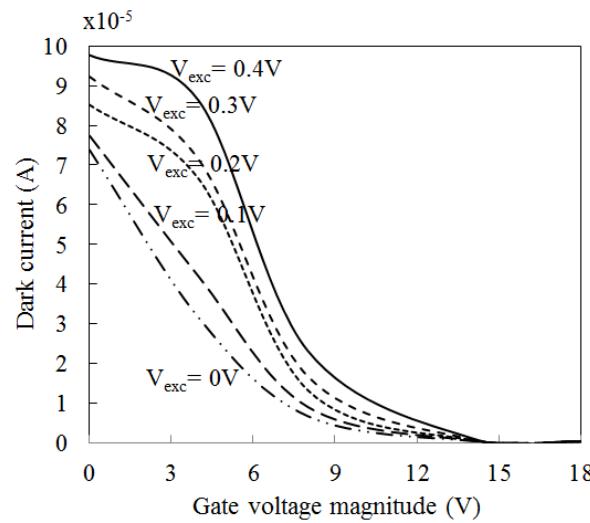


Analog SiPM



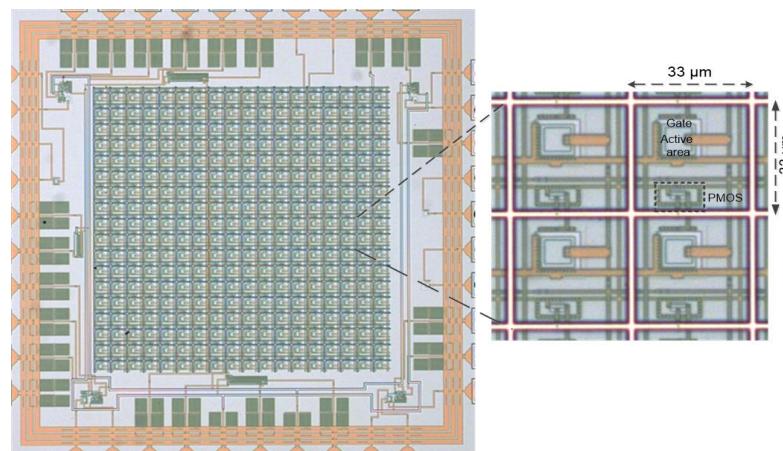
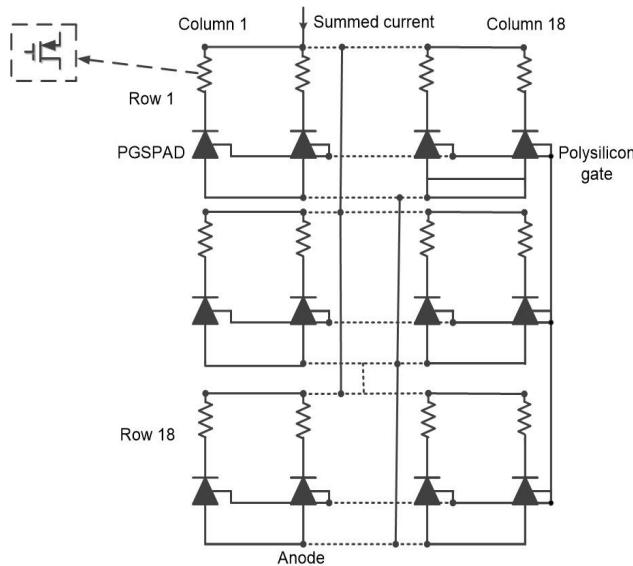
- SiPM has 162 microcells in 18 columns and 9 rows
- Each microcell has a perimeter gated SPAD
- PMOS is used for quenching

Analog SiPM



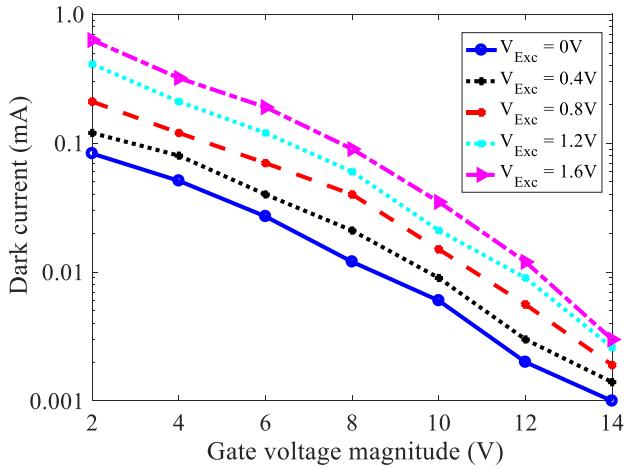
$$SNR = \frac{\text{Measured current} - \text{Dark current}}{\text{Dark current}}$$

Analog SiPM using PGSPAD

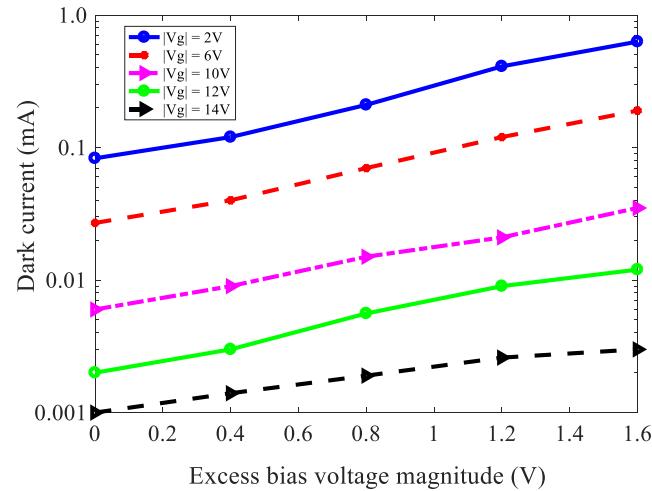


- SiPM has 324 microcells in 18 columns and 18 rows
 - Each microcell has a perimeter gated SPAD
 - PMOS is used to implement the quenching resistor

Dark Current



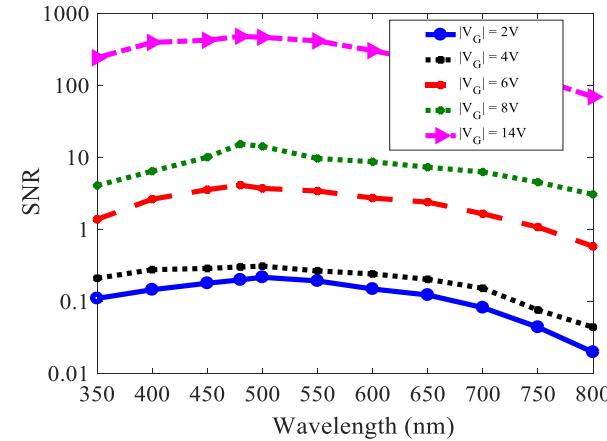
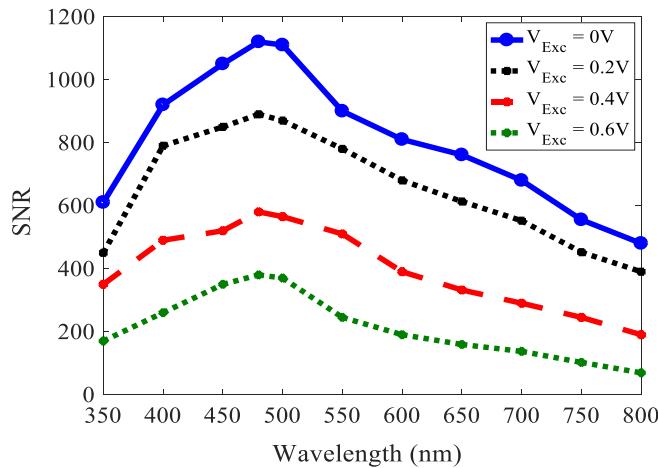
Dark current decreases with Gate Voltage



Dark current increases with Excess Bias voltage

Average values of three tested chips are reported for each dataset

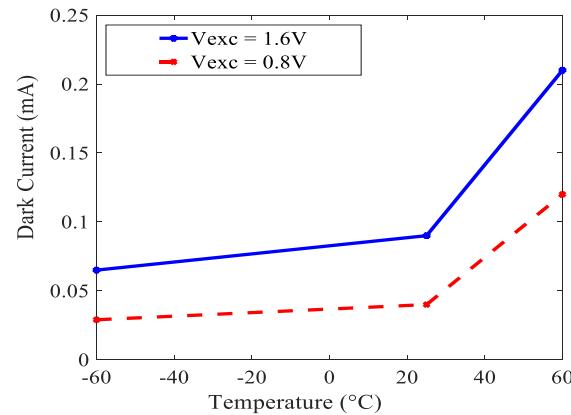
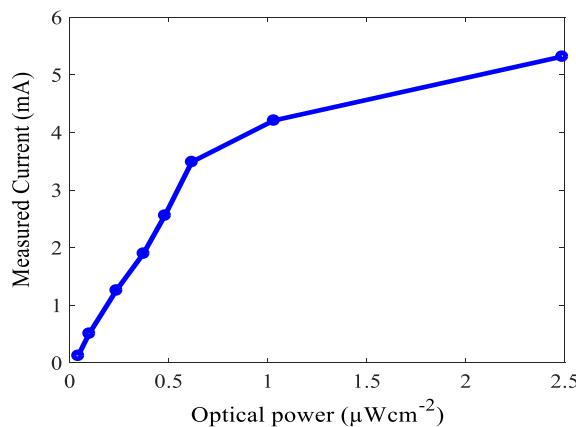
Optical Response



$$SNR = \frac{\text{Measured current} - \text{Dark current}}{\text{Dark current}}$$

- SNR increases with Gate Voltage
- SNR can be tuned over a range of 1 to 1150 using the applied gate voltage

Sensitivity and Temperature



- Output current increases with input optical power with sensitivity of $1.06 \times 10^3 \text{ A/Wcm}^2$
- Dark current increases with temperature and changes more prominently at higher temperature
- PGSPAD SiPM is expected to have a more significant change in dark current at lower temperatures based on PGSPAD experiment

PGSPAD SiPM Model

- Equivalent capacitance, capacitance of all passive microcells and all coupling capacitance

$$C_{eqv} = (N - T) \frac{C_{quench} C_{diode}}{C_{quench} + C_{diode}} + N C_{coupl}$$

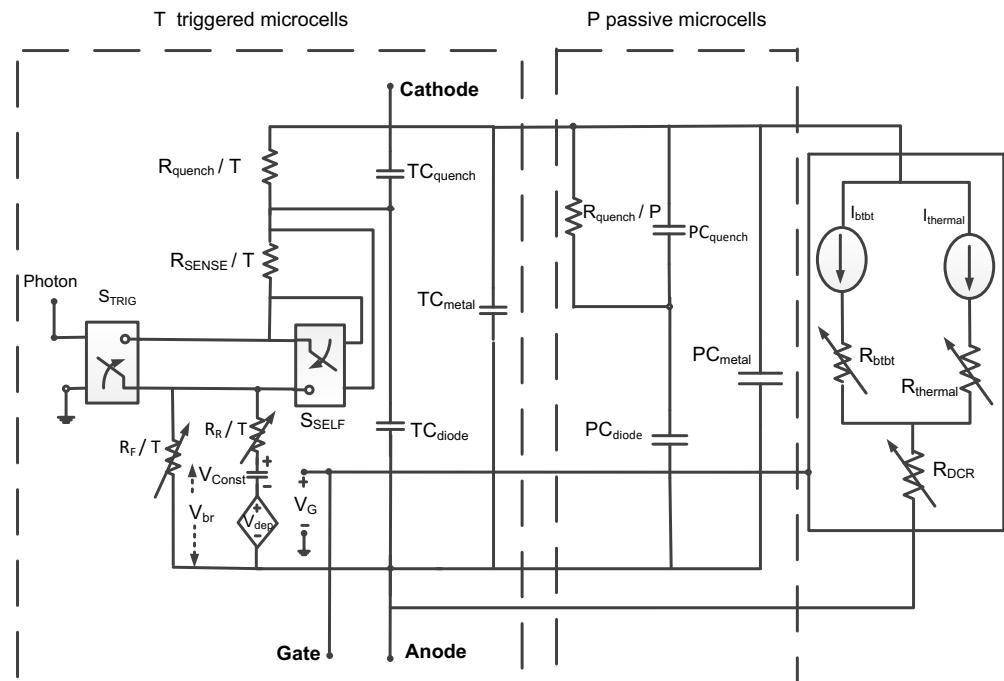
N = Number of total microcells

T = Number of triggered microcells

$P = N - T$ = Number of passive microcells

C_{quench} = Stray capacitance associated with quenching resistance, R_{quench}

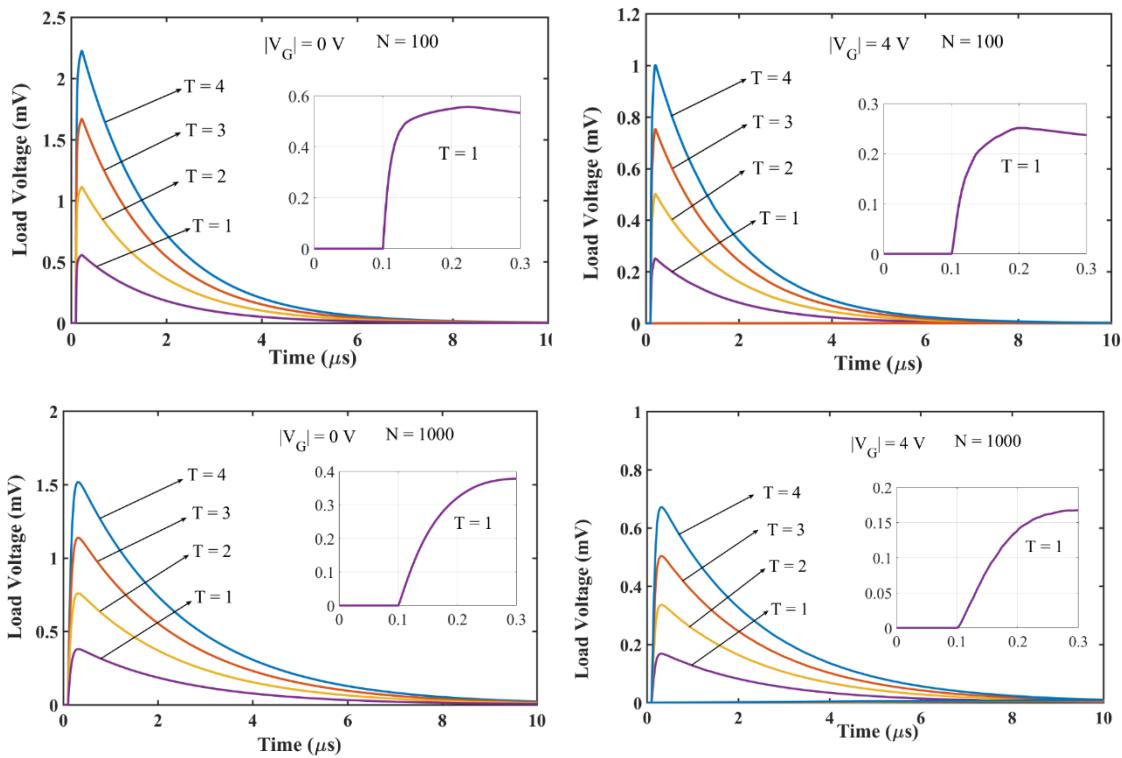
C_{diode} = Total capacitance of PGSPAD device



Overall PGSPAD SiPM with T triggered microcells and P passive microcells

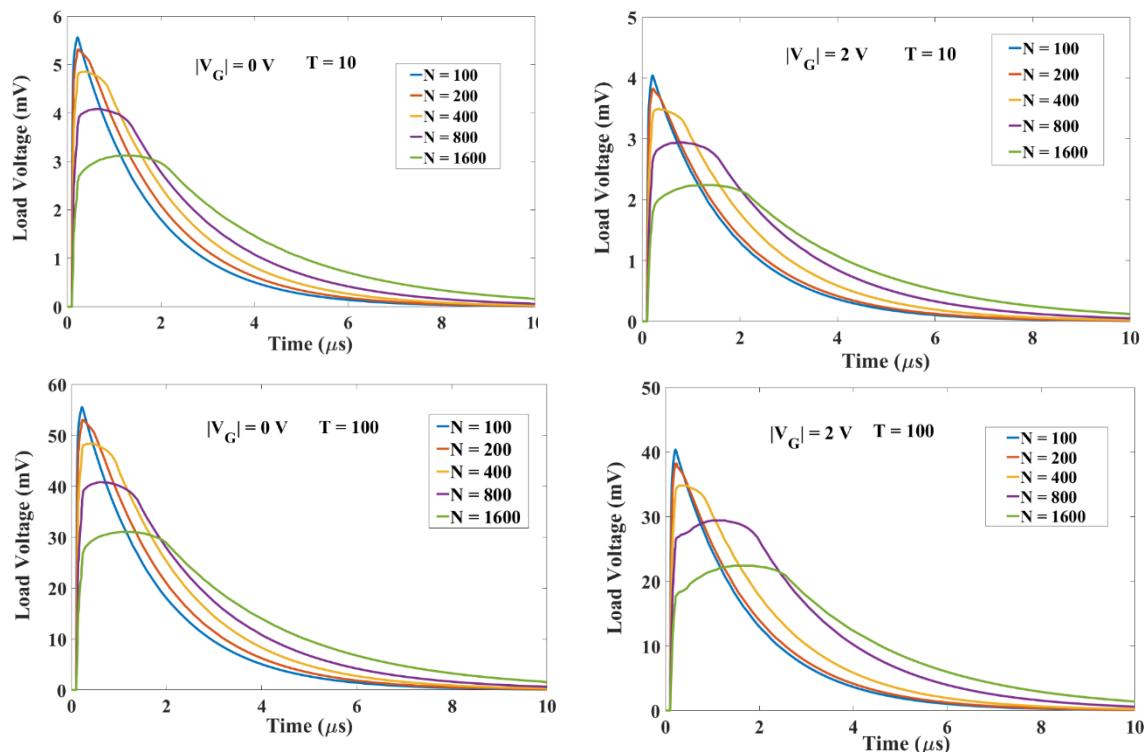
Transient Response

- No. of triggered microcells (T) \uparrow , Peak amplitude \uparrow for a SiPM
- No. of total microcells (N) \uparrow , Peak amplitude \downarrow , Rising edge is slower
- Gate voltage (V_G) \uparrow , Peak amplitude \downarrow for a SiPM

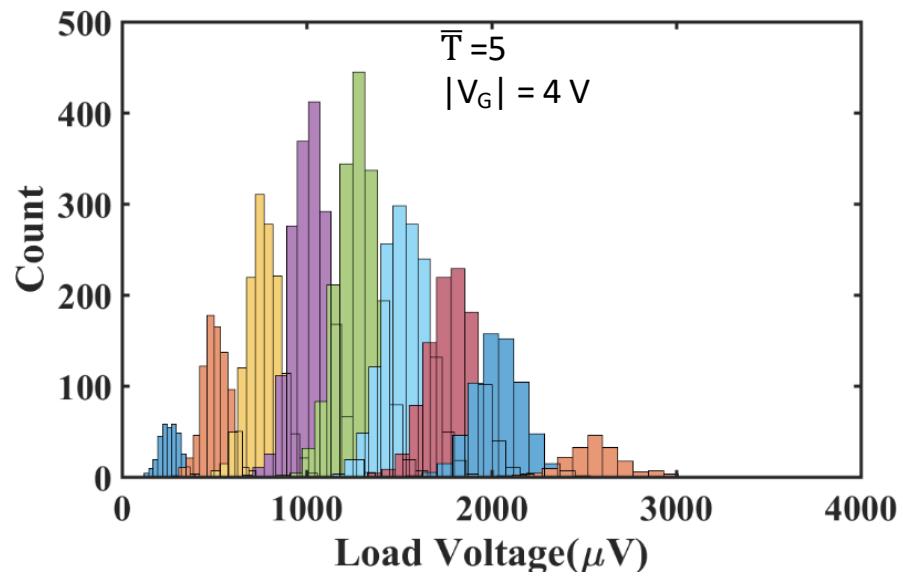
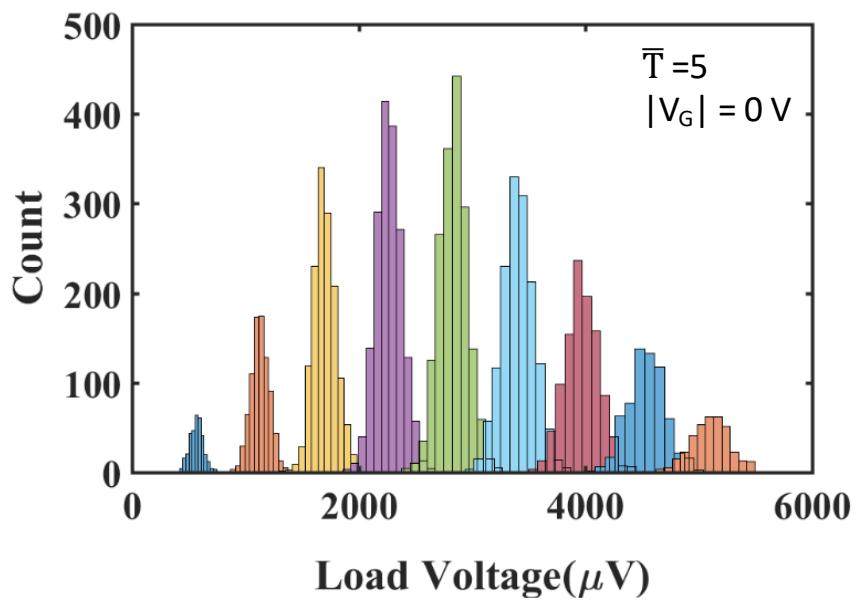


Transient Response of PGSPAD SiPM

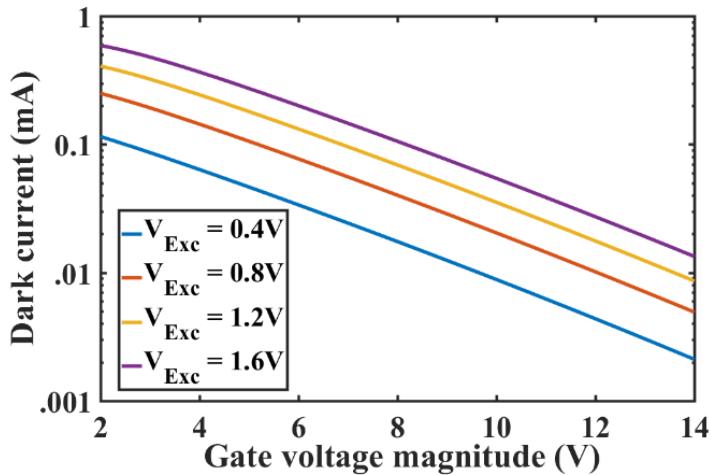
- No. of triggered microcells (T) ↑, Peak amplitude ↑ for a SiPM
- No. of total microcells (N) ↑, Peak amplitude ↓, Rising edge is slower
- Gate voltage (V_G) ↑, Peak amplitude ↓ for a SiPM



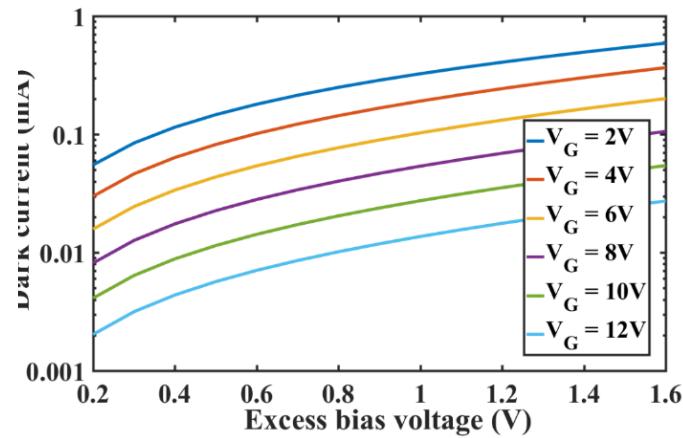
Photoelectron Spectrum



Simulated Noise of PGSPAD SiPM



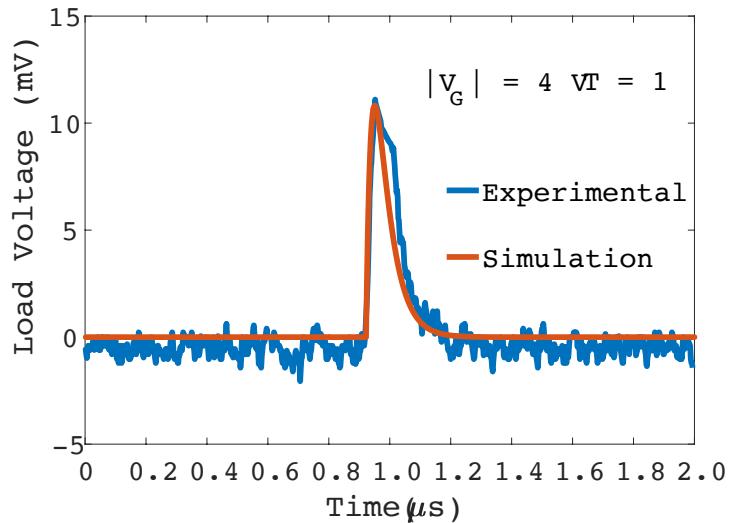
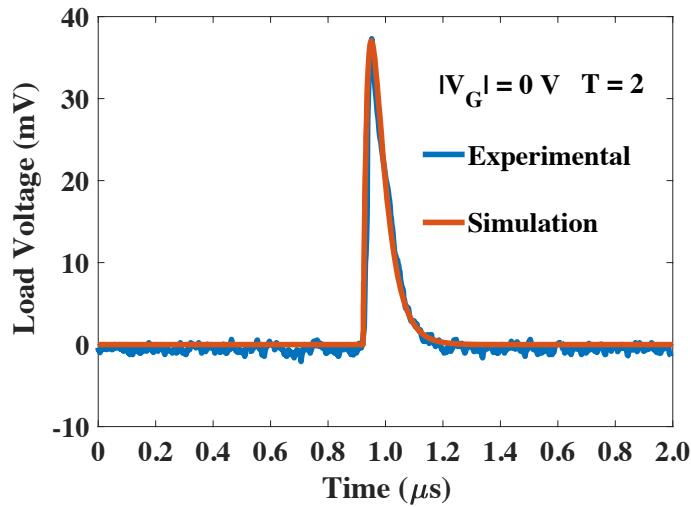
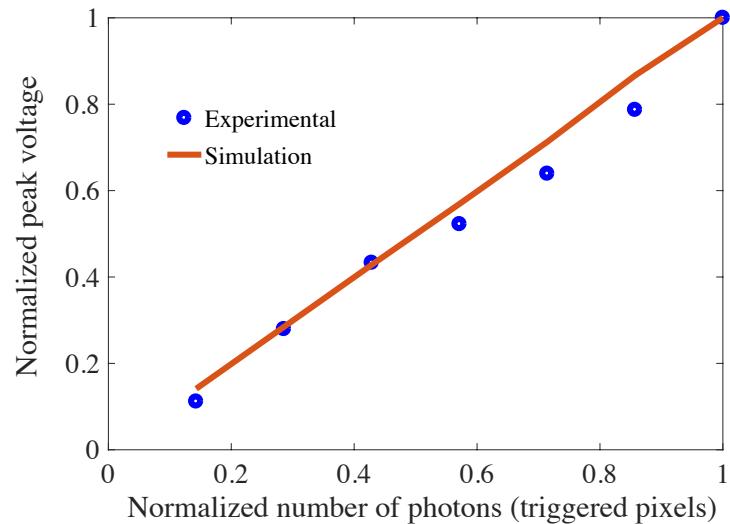
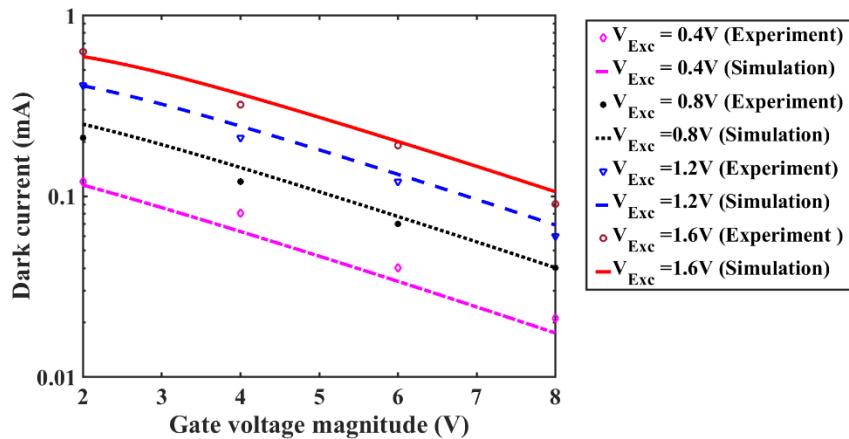
Dark current noise as a function of applied gate voltage with two different excess bias voltages, V_{Exc}



Dark current noise as a function of excess bias voltage with two different applied gate voltages, $|V_G|$

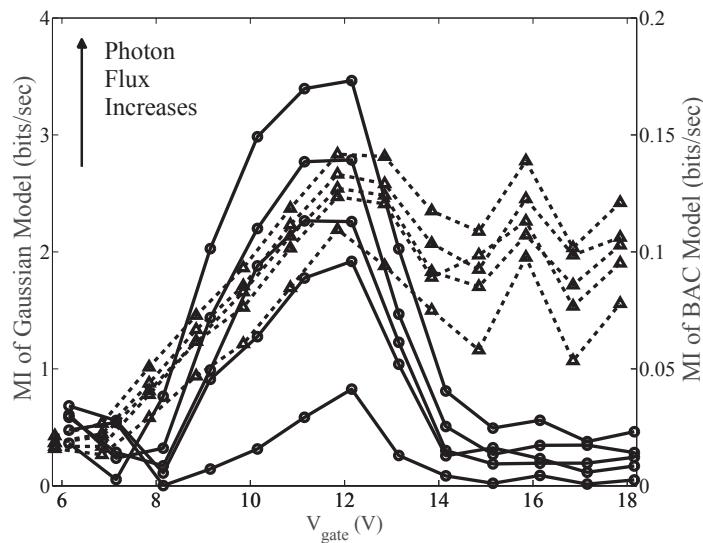
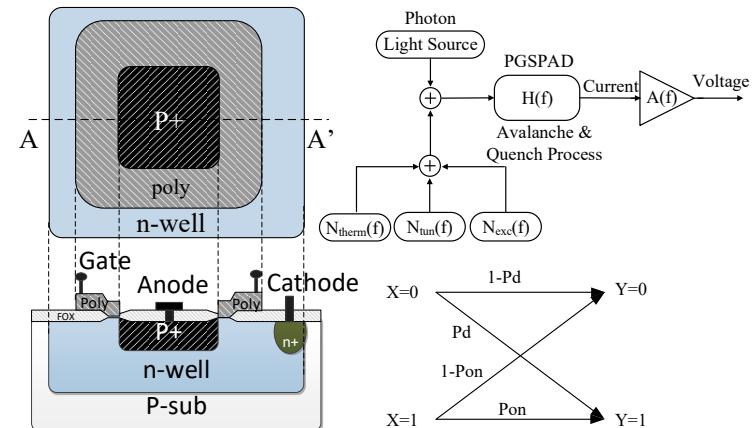
- Dark current reduces with the increase of applied gate voltage
- Dark current increases with the increase of excess bias voltage
- Measured results are obtained from testing of a PGSPAD SiPM (18×18 array) fabricated in 0.5 μ m CMOS process
- Simulation results show very good matching with experimental measurements

Model Validation



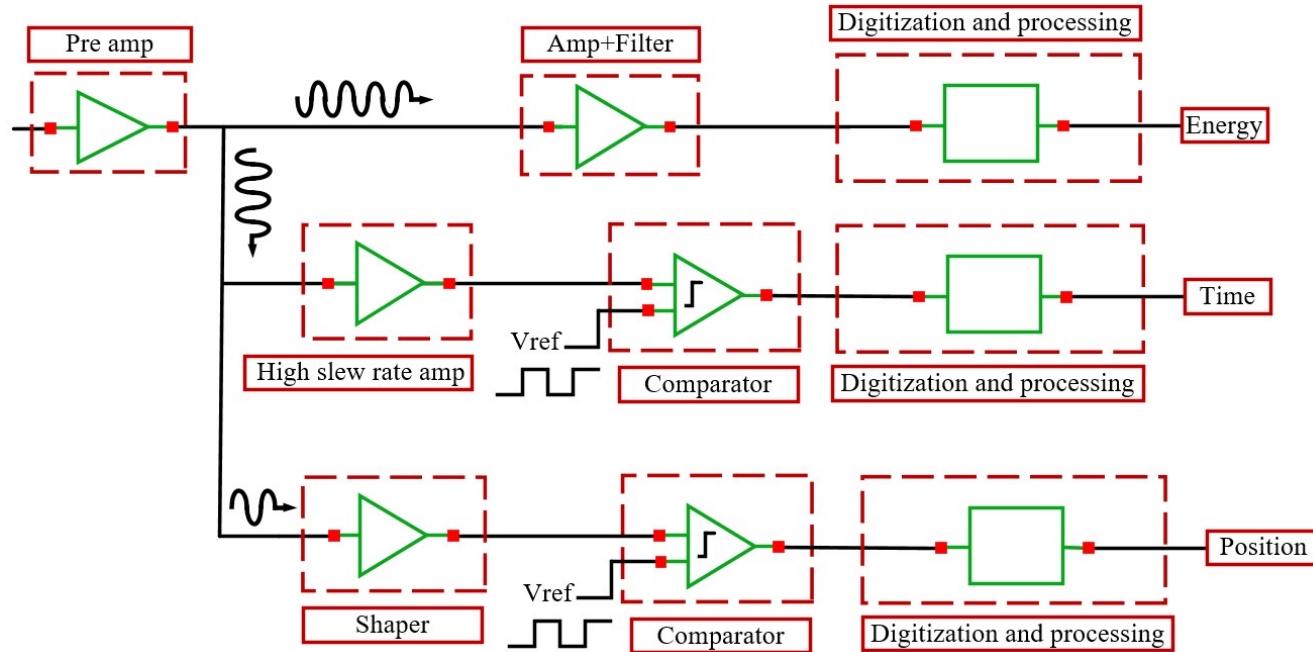
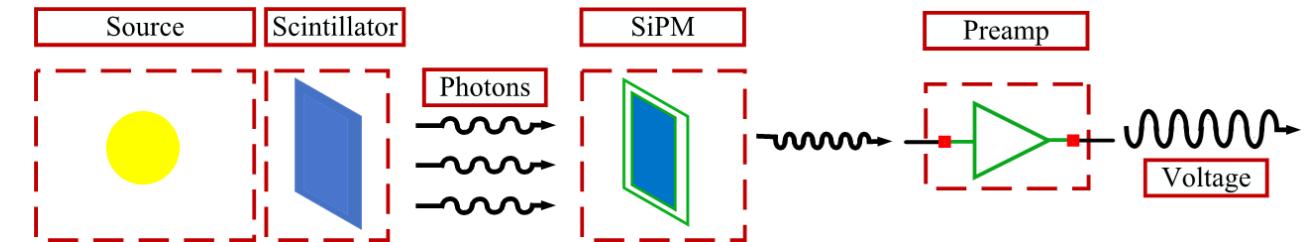
Information Theoretic Model

- Model as a binary asymmetric channel: X = incident photon, Y =avalanche event
- PDP and DCR experimentally derived
- Maximizing information rate requires moderately excess bias voltage, gate voltage, and photon flux
- Can inform adoption of readout topologies

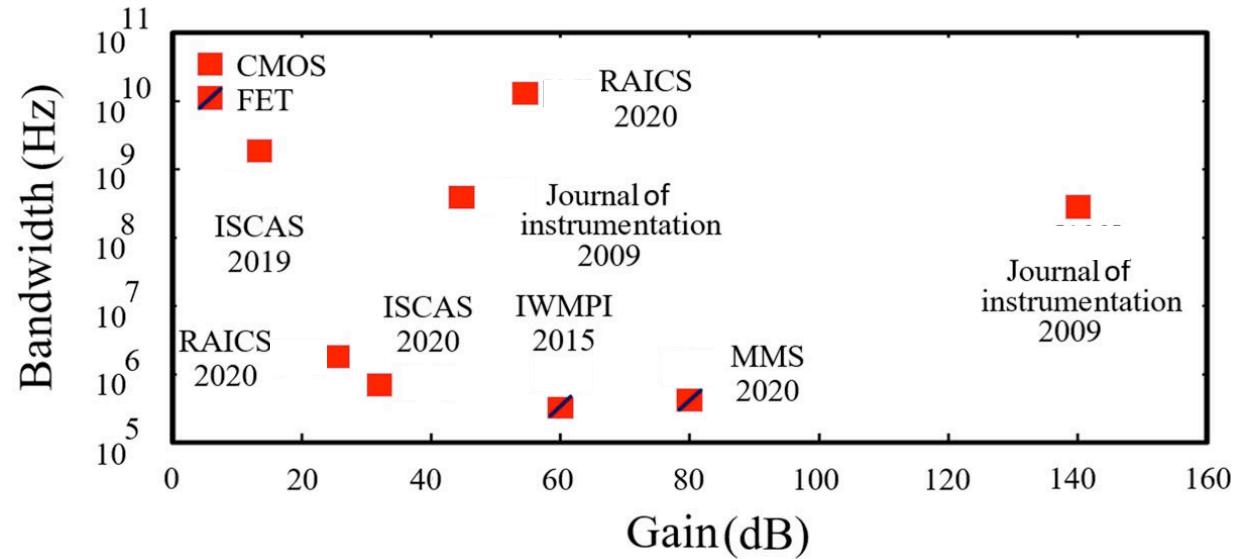
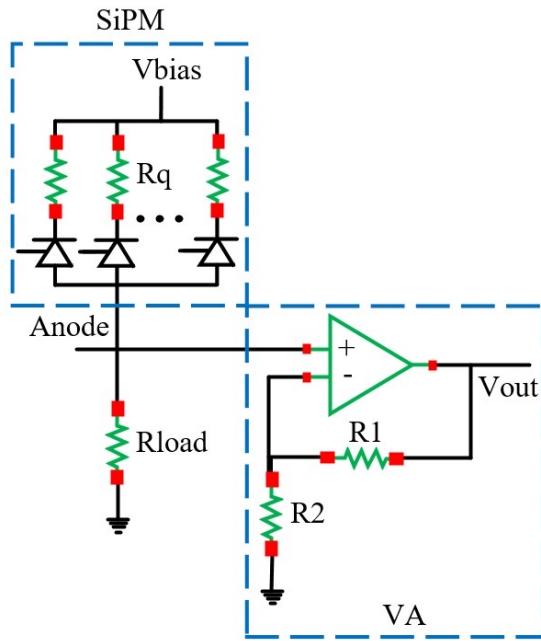


Readout Topologies

Nuclear Imaging Readout

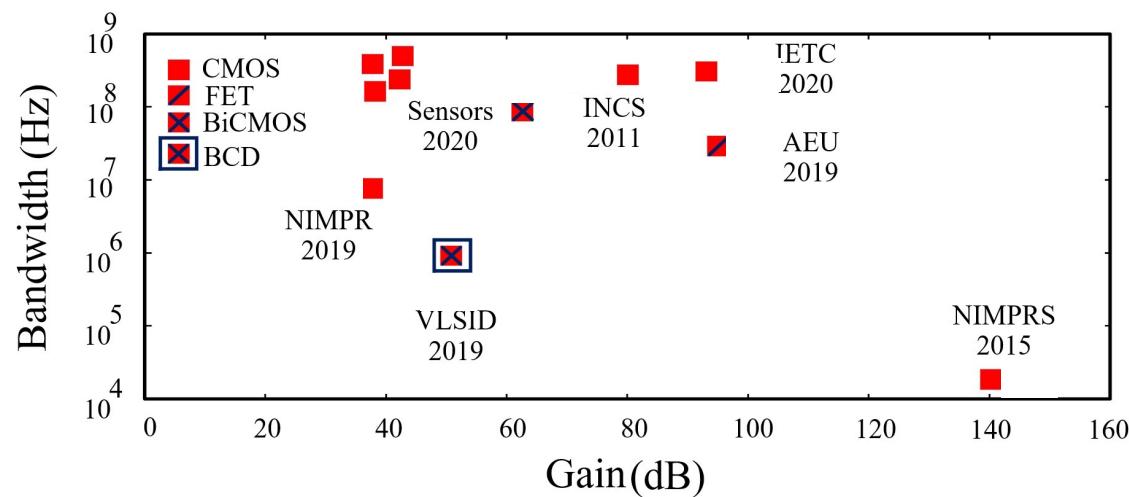
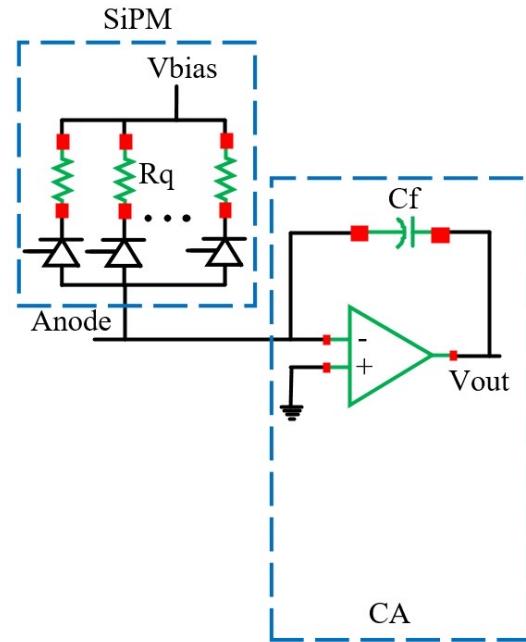


Voltage amplifiers



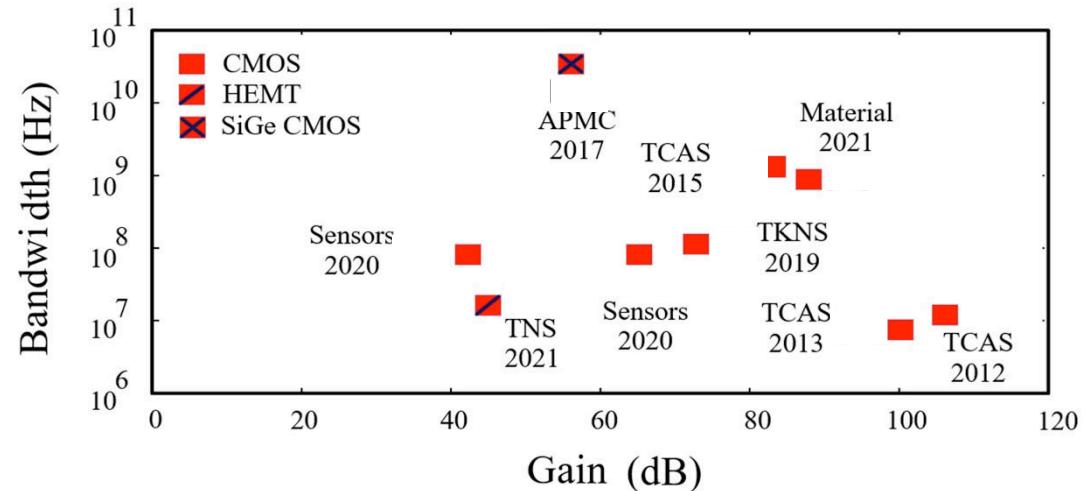
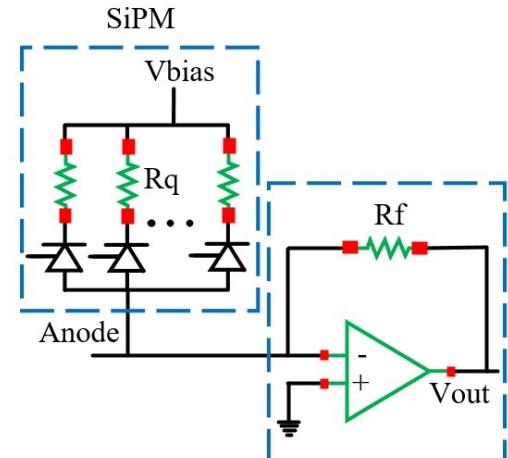
Charge Amplifiers

- Large capacitor is in parallel with device parasitics due to Miller effect
- Require a feedback resistor
- Large area due to passive devices
- Slew rate may be too slow
- Low noise
- Difficulty with large SiPM signals

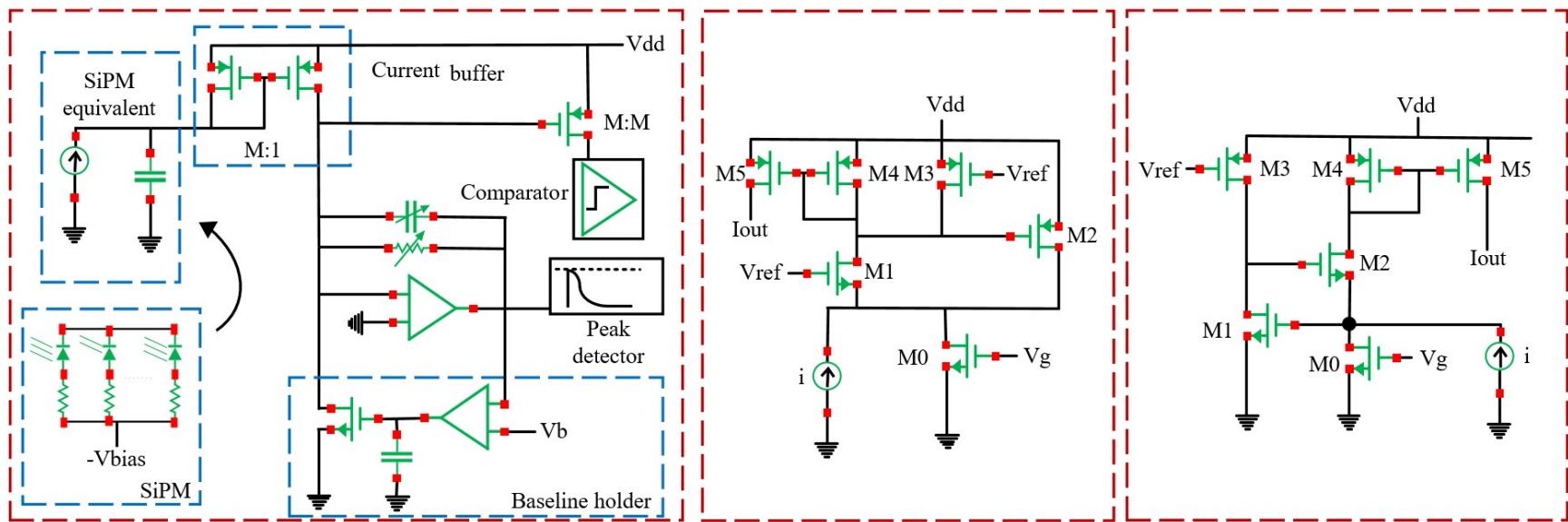


Transimpedance

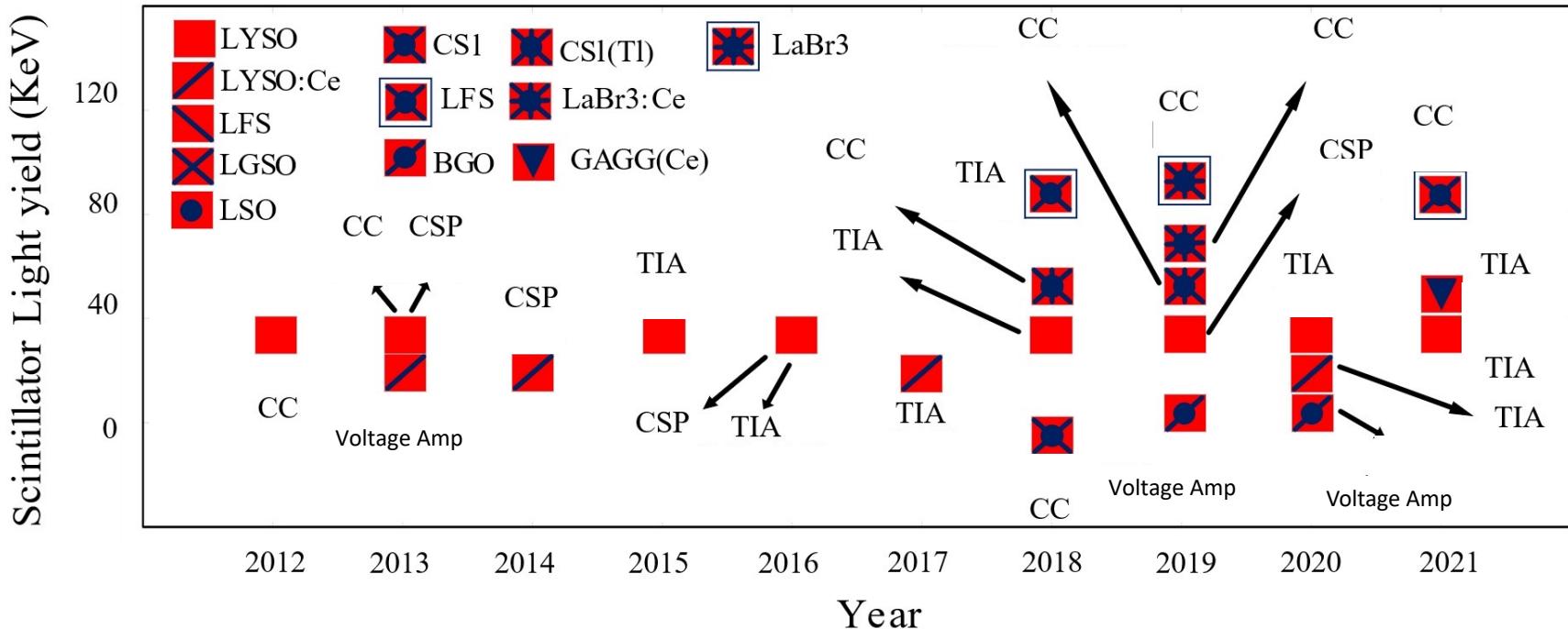
- Input resistance minimized with large gain
- Feedback R with parasitic capacitance → oscillations – requires C in feedback path
- Can use CG, CB topologies
- Input impedance affects sensitivity to



Current mode readouts

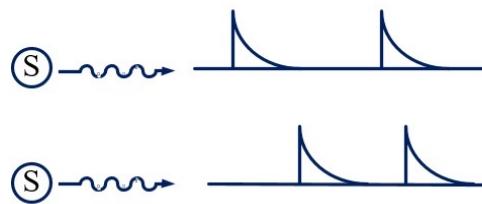


Scintillators

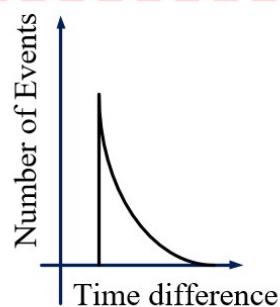
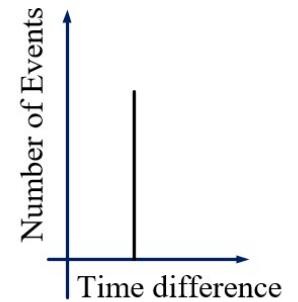
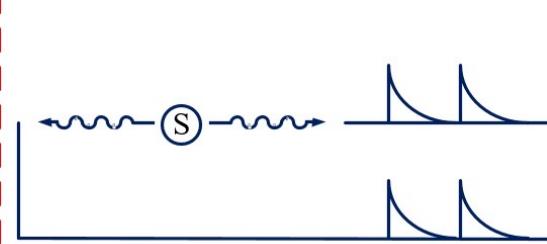


Timing

Uncorrelated Events



Prompt Coincidence

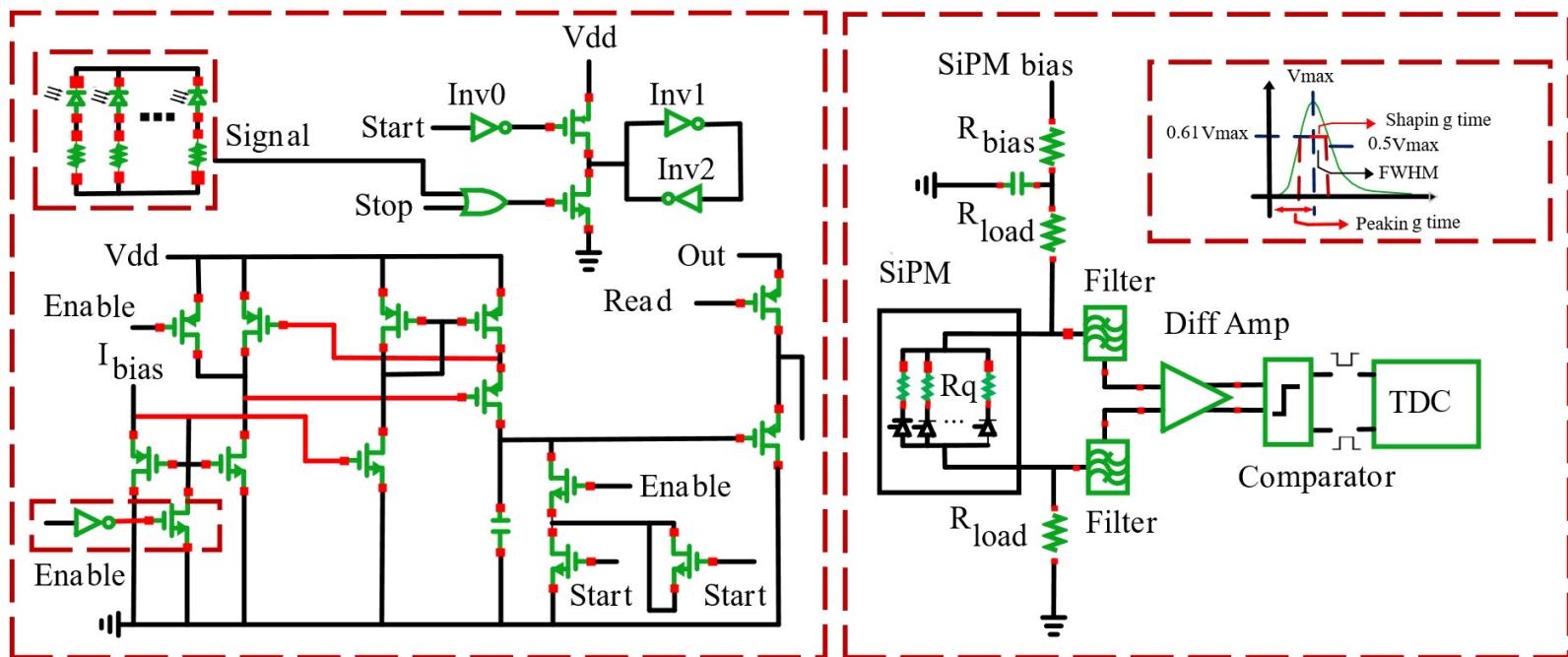


Delayed Coincidence

Charged Particle

Time of Flight

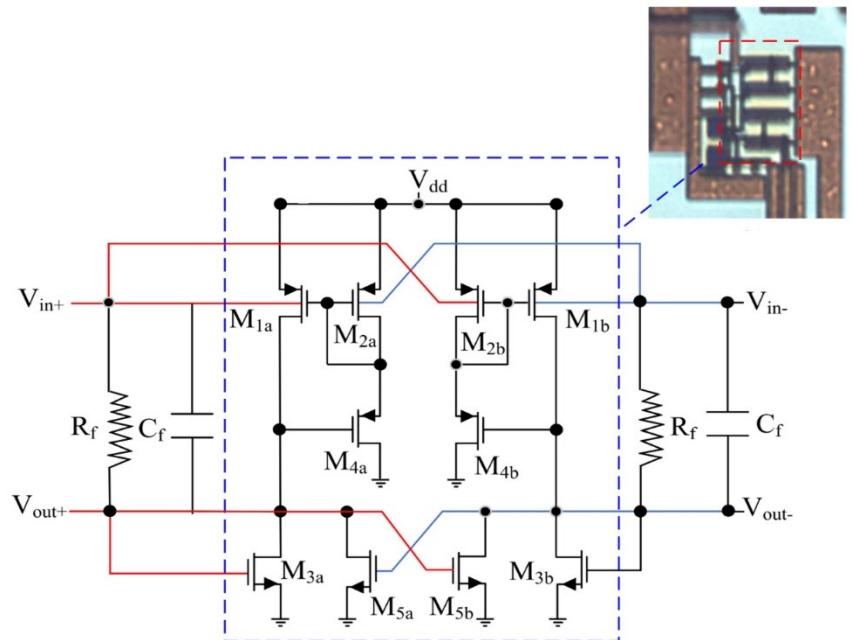
Timing



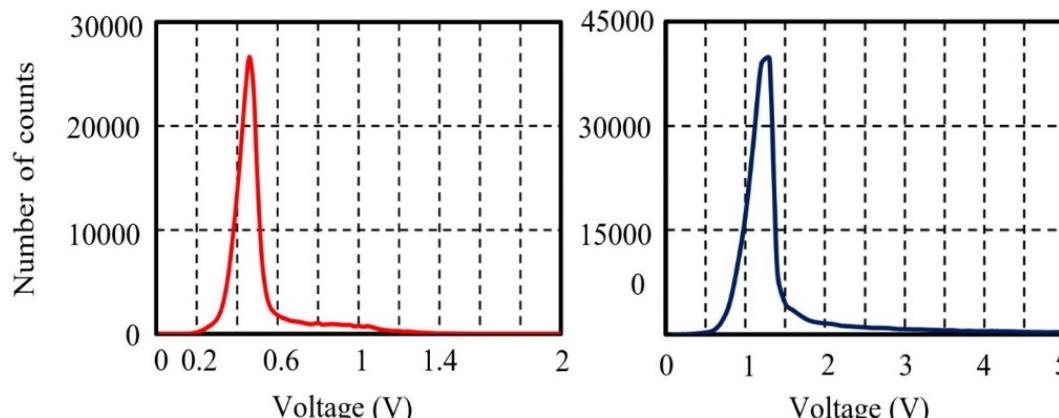
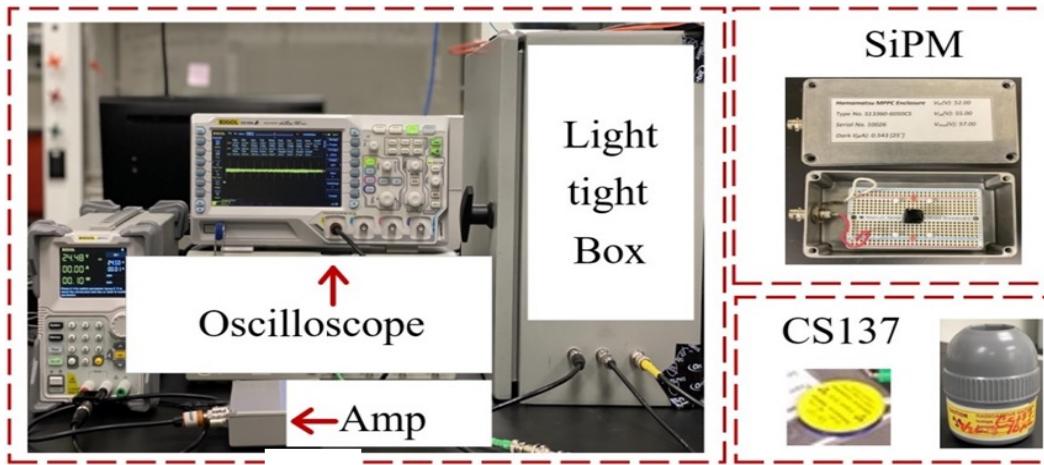
Implementations

TIA readout for SiPMs

- Bulk driven amplifier
- First stage amplification is performed through M4A and M4B
- M3A, M3B, M5A, and M5B increase the gain

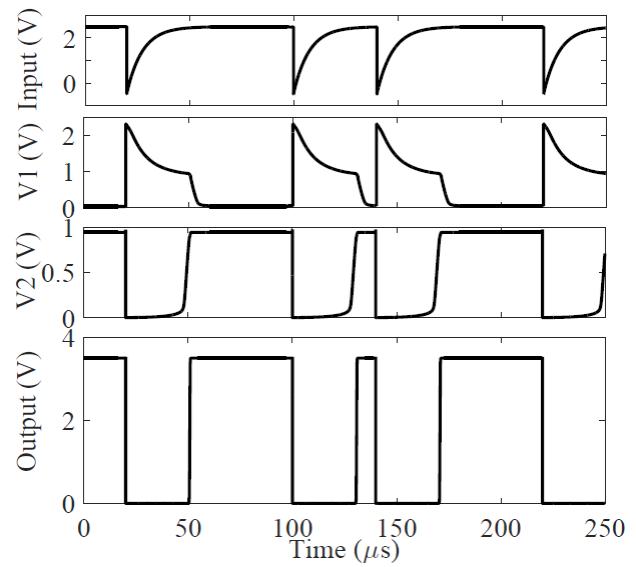
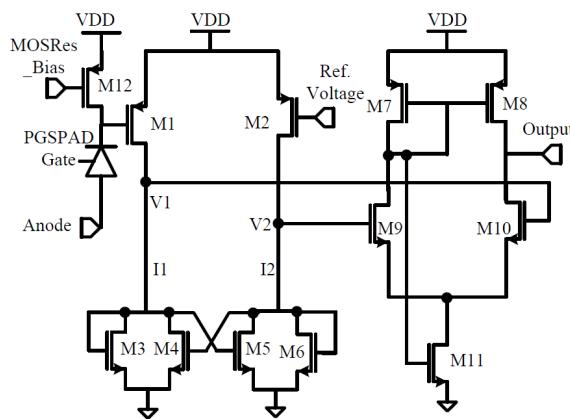
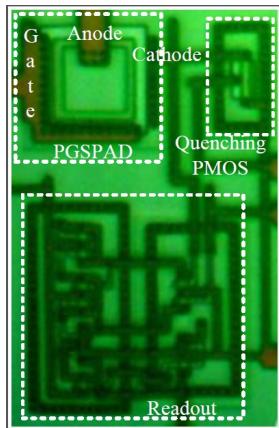


TIA readout for SiPMs



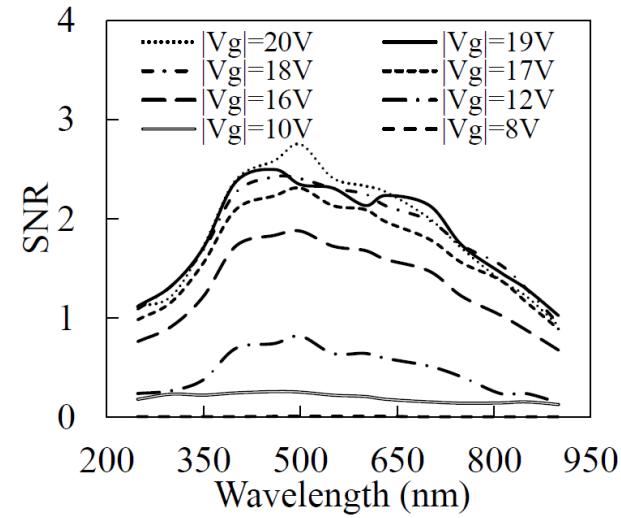
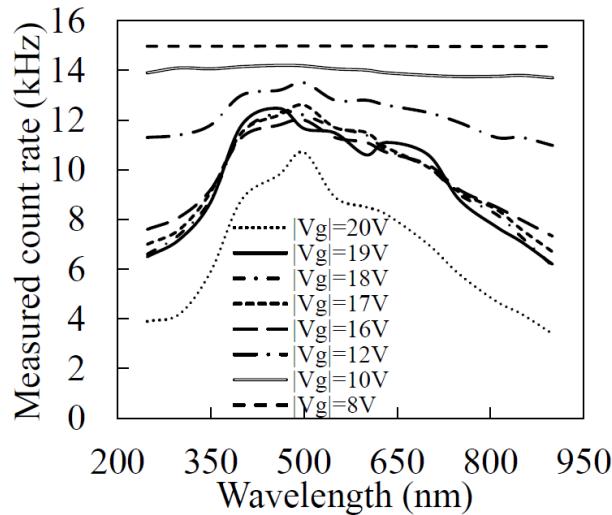
Commercial TIA vs Custom TIA

Digital Readout



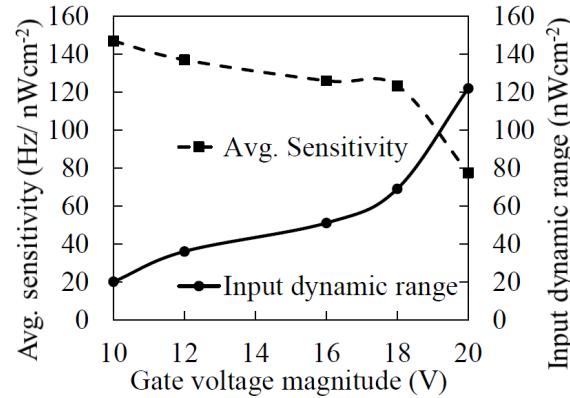
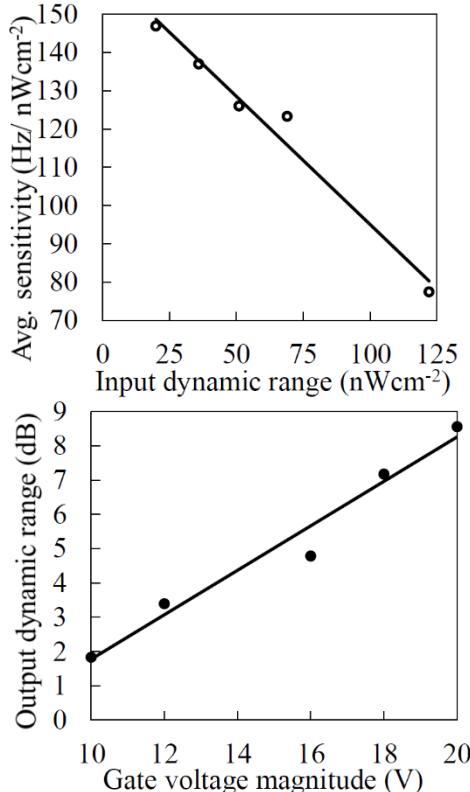
Simulated timing diagram

Digital PGPSAD



$$SNR = \frac{Measured\ count\ rate - Dark\ count\ rate}{Dark\ count\ rate}$$

Sensitivity-Dynamic Range Trade-Off



- $MCR = \text{Measured count rate}$

$$\text{Sensitivity} = \frac{\Delta MCR}{\Delta \text{Optical power}}$$

$$\text{Output dynamic range} = 20 \log_{10} \frac{MCR_{max}}{MCR_{min}}$$

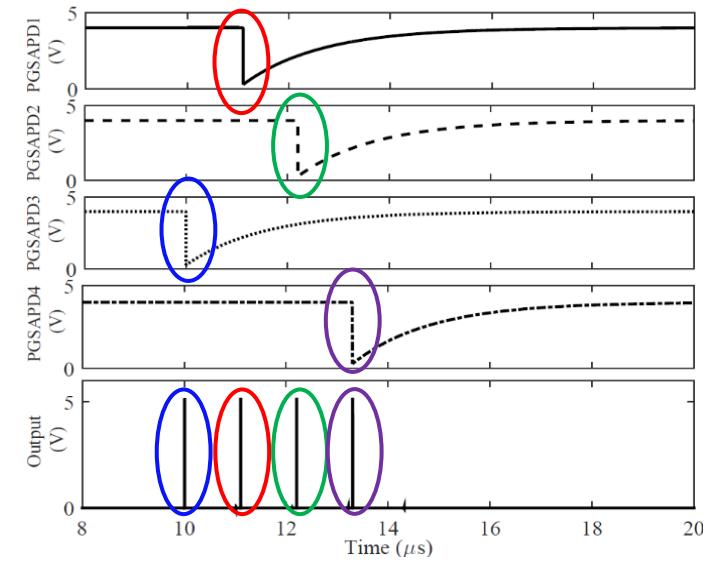
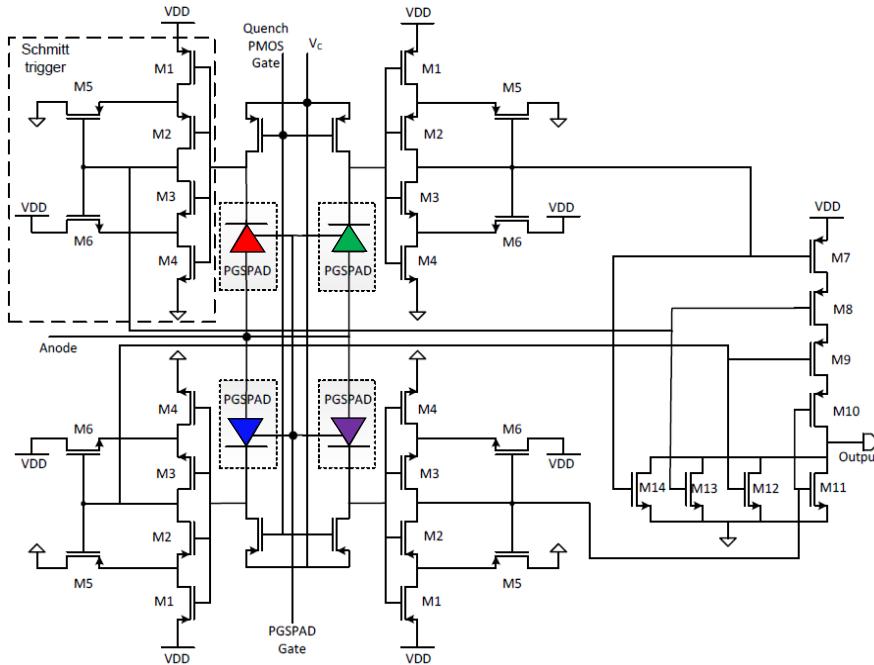
Input dynamic range = largest nonsaturating signal – smallest detectable input signal

Digital Pixel Performance Summary

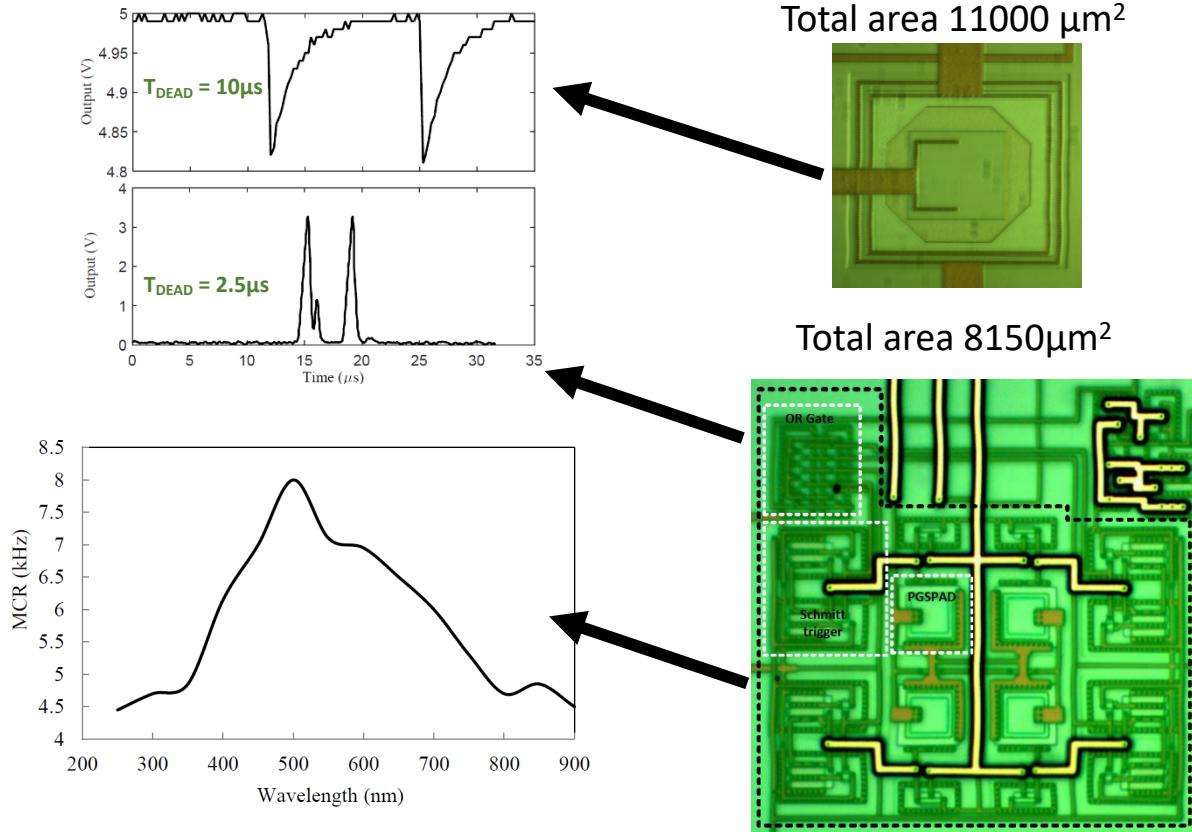
GATE VOLTAGE AFFECTING BREAKDOWN VOLTAGE, SENSITIVITY,
DYNAMIC RANGE, SNR

Gate Voltage Magnitude (V)	Break- down Voltage (V)	Average Sensitivity ($Hz / nW cm^{-2}$)	Input Dynamic Range ($nW cm^{-2}$)	Output Dynamic Range (dB)	Peak SNR ($nW cm^{-2}$)
10	-15.12	147	20	1.1	0.26
12	-15.32	137	36	3.1	0.82
16	-15.52	125	51	8.7	1.87
18	-15.66	123	69	12.4	2.42
20	-15.83	77	122	18.9	2.75

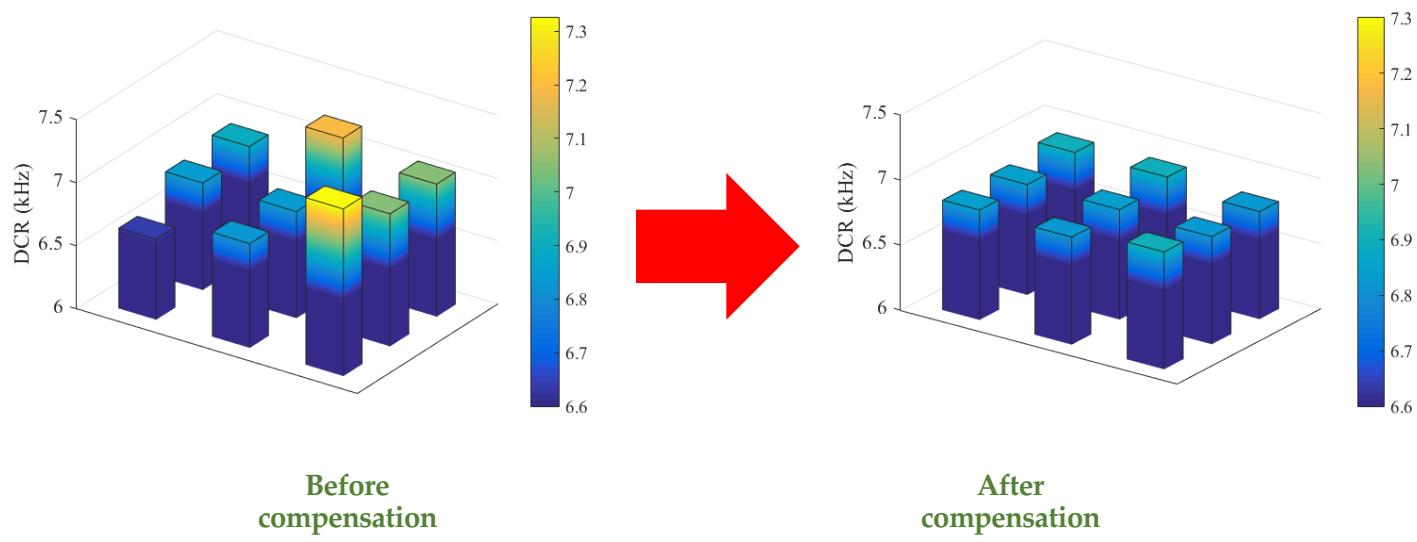
Pixel for Digital SiPM



Dead time Minimization



Noise Variation Compensation



Noise variation compensation by controlling individual gate voltages

Limitation of Synchronous Readout

Sequential architecture

- Best fill factor
- Worst bandwidth and detection efficiency

In-Column architecture

- Improves bandwidth
- Degrades fill-factor.

Fully Parallel In-pixel

- Best detection bandwidth
- Worst fill-factor

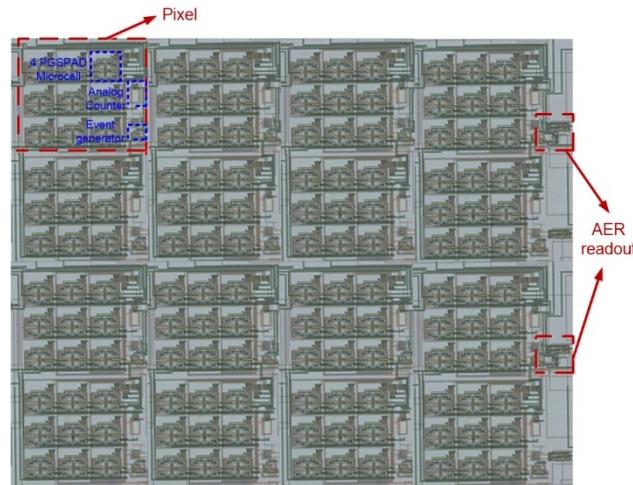
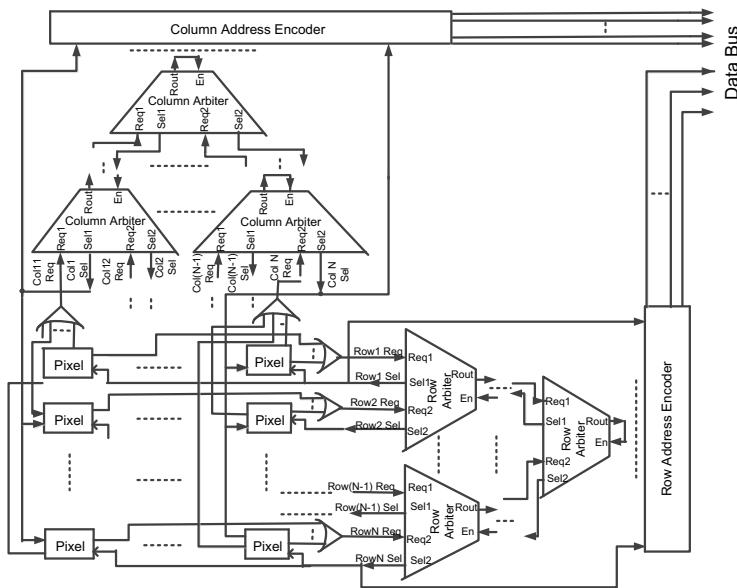


Asynchronous Readout

- Best serves asynchronously arriving photons
- Provides high bandwidth communication
- Improves system Signal to Noise Ratio

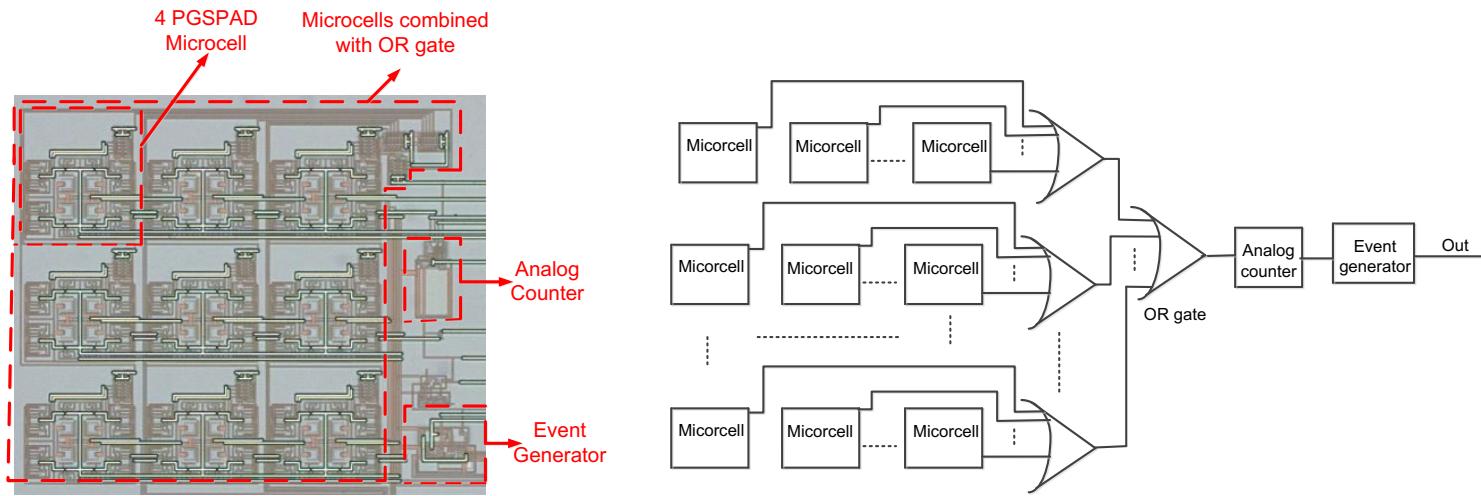
Digital SiPM with Asynchronous AER Readout

- High-bandwidth communication
 - Data driven
 - Minimizes temporal aliasing
 - No sampling



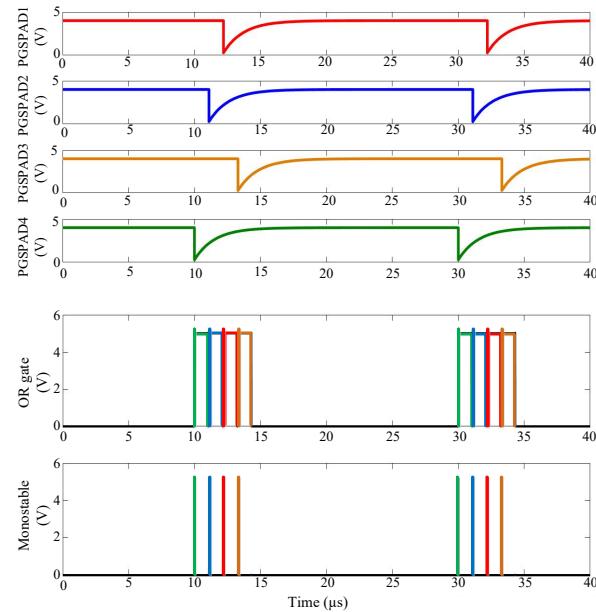
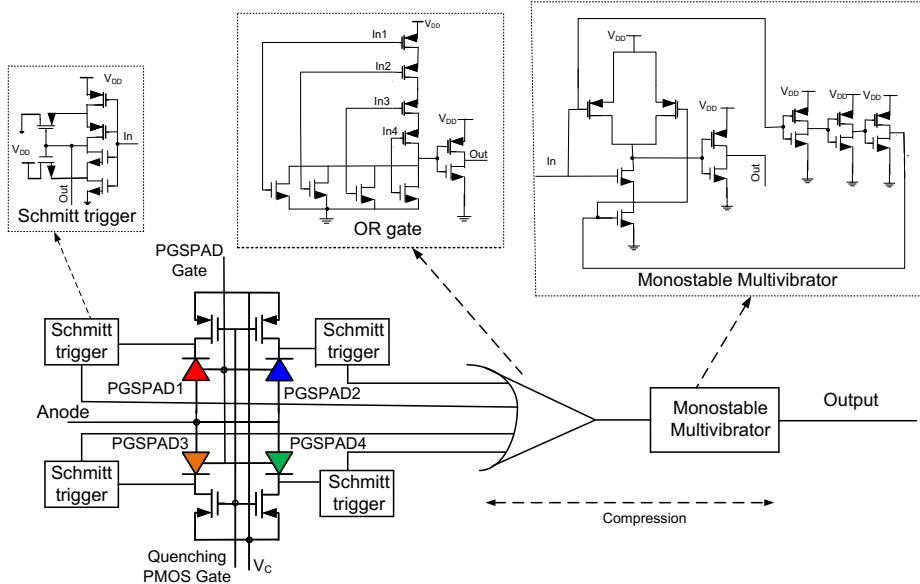
A 4×4 pixel array based on PGSPAD with AER readout

Pixel of Digital SiPM



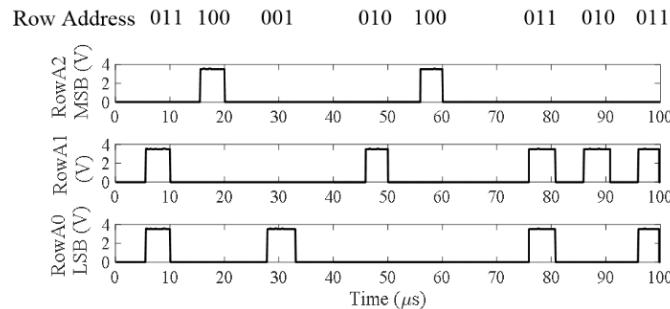
- Pixel includes 9 microcells, an analog counter, and an event generator
- Each microcell uses PGSPADs to provide tunability of noise.
- Analog counter provides a more compact implementation with lower power consumption than digital counters improving the fill factor
- Event generator is included to realize the AER readout at the top level of digital SiPM

Microcell of pixel

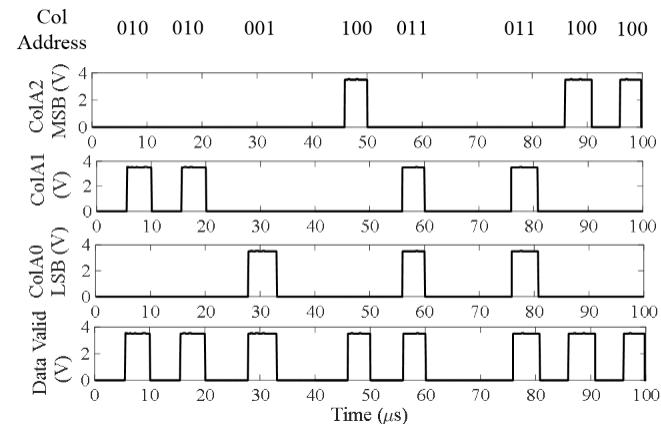


- Includes both spatial and temporal compression schemes to improve DCR versus fill factor compromise with reduced electronics and dead time
- Improved temporal compression by a factor of 10
- Improved dead time is less than 0.25 of the dead time of a single larger PGSPAD of same area

4×4 PGSPAD Digital SiPM with Asynchronous AER Readout



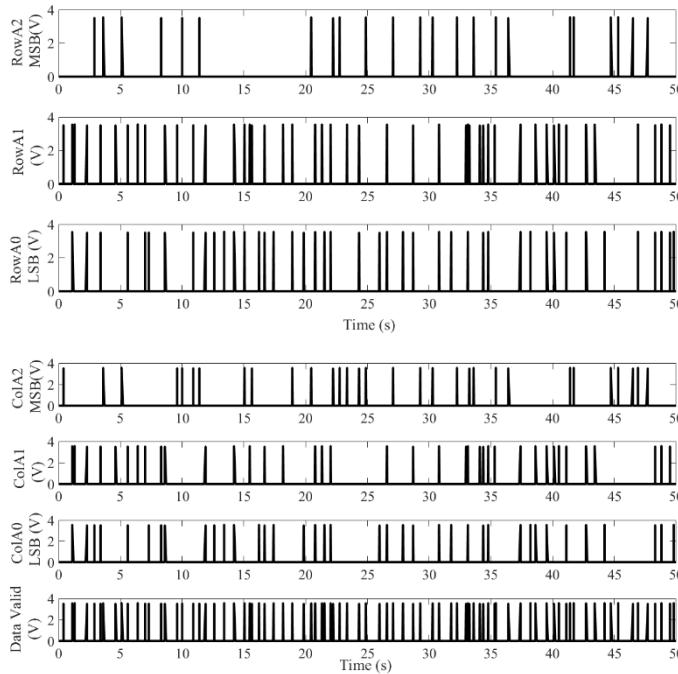
Output Row Address with optical power of 100 nWcm^{-2}



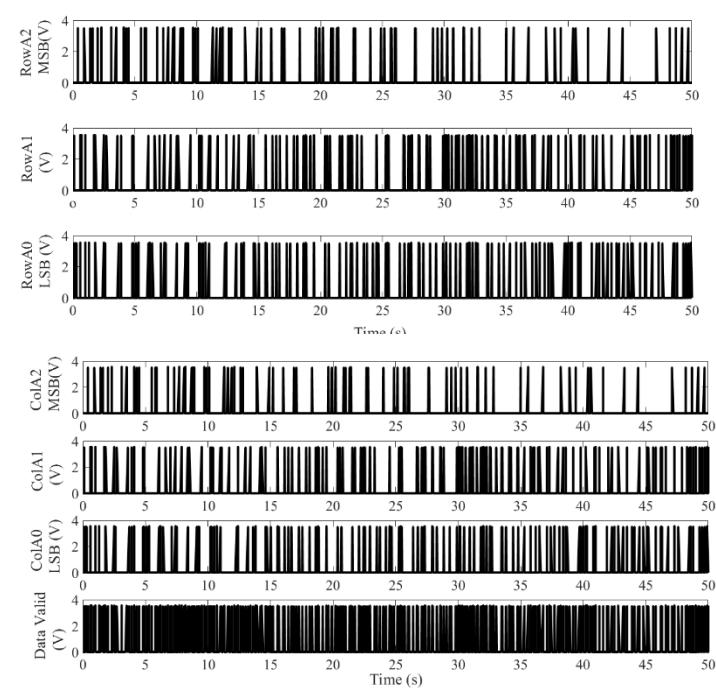
Column address with data valid bit at optical power of 100 nWcm^{-2}

- Measured 7-bit address (3-bit row address, 3-bit column address, and 1-bit data valid bit) represents the address of triggered pixel
- Triggered pixels are P10 (011, 010), P14 (100, 010), P1 (001, 001), P8 (010, 100), P15 (100, 011), P11 (011, 011), P8 (010, 100), and P12 (011, 100).

Measured Outputs of PGSPAD Digital SiPM with Asynchronous AER Readout

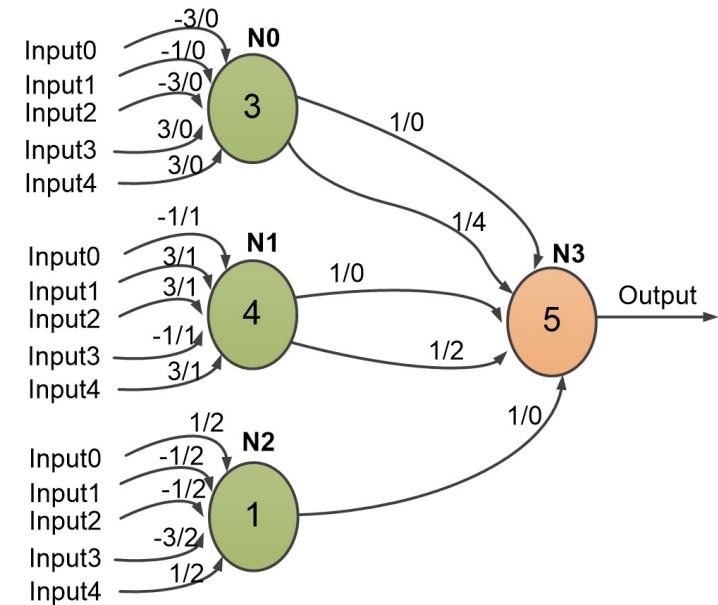
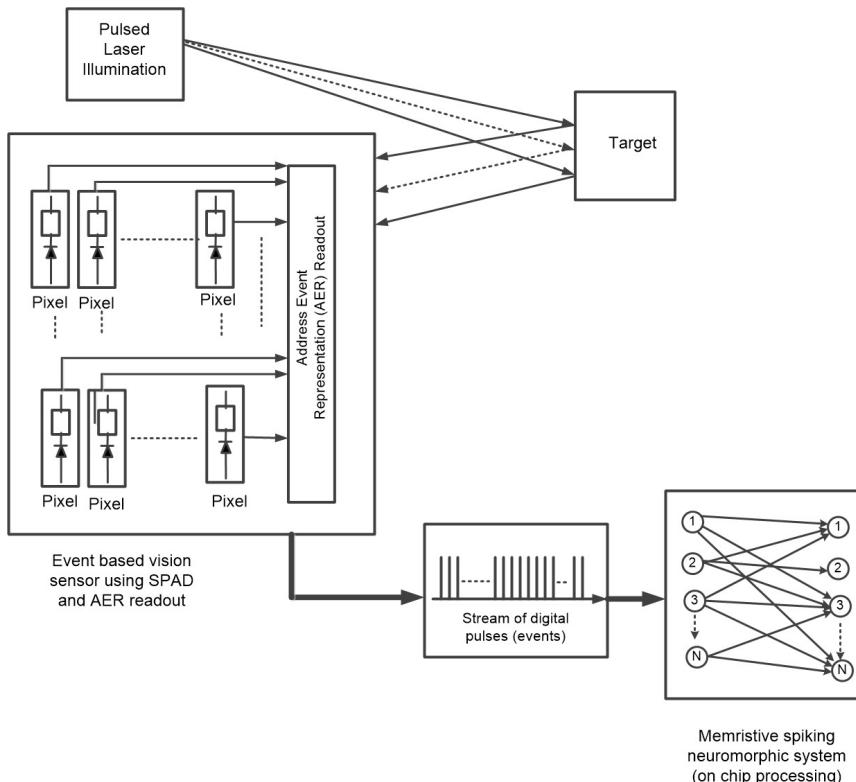


Output Addresses with optical power
of 26 nWcm^{-2}



Output Addresses with optical power
of 130 nWcm^{-2}

SPAD Based Vision Sensor with Memristive Spiking Neuromorphic System



Basic shape recognition
DR: 152 dB, Power: 2.1mW

0.48 pJ per synaptic spike
12.5 pJ per neuron per spike

Acknowledgements

