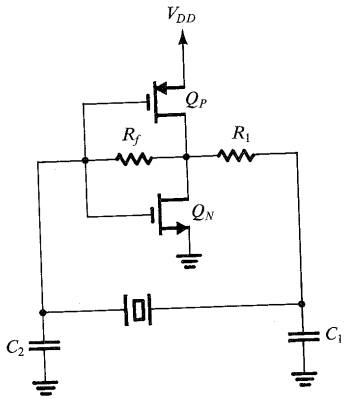


FIGURE 13.16 A Pierce crystal oscillator utilizing a CMOS inverter as an amplifier.

have the shape shown in Fig. 13.15(c). We observe that the crystal reactance is inductive over the very narrow frequency band between ω_s and ω_p. For a given crystal, this frequency band is well defined. Thus we may use the crystal to replace the inductor of the Colpitts oscillator (Fig. 13.12a). The resulting circuit will oscillate at the resonance frequency of the crystal inductance L with the series equivalent of C_s and $(C_p + C_1C_2/(C_1 + C_2))$. Since C_s is much smaller than the three other capacitances, it will be dominant and

$$\omega_0 \simeq 1/\sqrt{LC_s} = \omega_s \tag{13.27}$$

In addition to the basic Colpitts oscillator, a variety of configurations exist for crystal oscillators. Figure 13.16 shows a popular configuration (called the **Pierce oscillator**) utilizing a CMOS inverter (see Section 4.10) as amplifier. Resistor R_f determines a dc operating point in the high-gain region of the CMOS inverter. Resistor R_1 together with capacitor C_1 provides a low-pass filter that discourages the circuit from oscillating at a higher harmonic of the crystal frequency. Note that this circuit also is based on the Colpitts configuration.

The extremely stable resonance characteristics and the very high Q factors of quartz crystals result in oscillators with very accurate and stable frequencies. Crystals are available with resonance frequencies in the range of few kilohertz to hundreds of megahertz. Temperature coefficients of ω_0 of 1 or 2 parts per million (ppm) per degree Celsius are achievable. Unfortunately, however, crystal oscillators, being mechanical resonators, are fixed-frequency circuits.

EXERCISE

13.10 A 2-MHz quartz crystal is specified to have $L = 0.52$ H, $C_s = 0.012$ pF, $C_p = 4$ pF, and $r = 120\ \Omega$. Find f_s, f_p, and Q.

Ans. 2.015 MHz; 2.018 MHz; 55,000

13.4 BISTABLE MULTIVIBRATORS

In this section we begin the study of waveform-generating circuits of the other type—nonlinear oscillators or function generators. These devices make use of a special class of circuits known as **multivibrators.** As mentioned earlier, there are three types of multivibrator: bistable, monostable, and astable. This section is concerned with the first, the bistable multivibrator.[5]

As its name indicates, the **bistable multivibrator** has *two stable states*. The circuit can remain in either stable state indefinitely and moves to the other stable state only when appropriately *triggered.*

13.4.1 The Feedback Loop

Bistability can be obtained by connecting a dc amplifier in a positive-feedback loop having a loop gain greater than unity. Such a feedback loop is shown in Fig. 13.17; it consists of an op amp and a resistive voltage divider in the positive-feedback path. To see how bistability is obtained, consider operation with the positive input terminal of the op amp near ground potential. This is a reasonable starting point, since the circuit has no external excitation. Assume that the electrical noise that is inevitably present in every electronic circuit causes a small positive increment in the voltage v_+. This incremental signal will be amplified by the large open-loop gain A of the op amp, with the result that a much greater signal will appear in the op amp's output voltage v_O. The voltage divider (R_1, R_2) will feed a fraction $\beta \equiv R_1/(R_1 + R_2)$ of the output signal back to the positive input terminal of the op amp. If $A\beta$ is greater than unity, as is usually the case, the fed-back signal will be greater than the original increment in v_+. This *regenerative* process continues until eventually the op amp saturates with its output voltage at the positive saturation level, L_+. When this happens, the voltage at the positive input terminal, v_+, becomes $L_+R_1/(R_1 + R_2)$, which is positive and thus keeps the op amp in positive saturation. This is one of the two stable states of the circuit.

In the description above we assumed that when v_+ was near zero volts, a positive increment occurred in v_+. Had we assumed the equally probable situation of a negative increment, the op amp would have ended up saturated in the negative direction with $v_O = L_-$ and $v_+ = L_-R_1/(R_1 + R_2)$. This is the other stable state.

We thus conclude that the circuit of Fig. 13.17 has two stable states, one with the op amp in positive saturation and the other with the op amp in negative saturation. The circuit can exist in either of these two states indefinitely. We also note that the circuit cannot exist in the state for which $v_+ = 0$ and $v_O = 0$ for any length of time. This is a state of *unstable equilibrium* (also known as a **metastable state**); any disturbance, such as that caused by electrical noise,

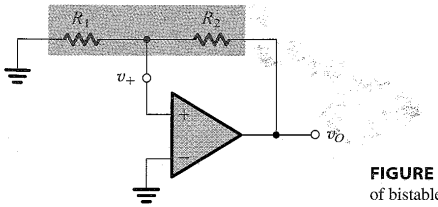


FIGURE 13.17 A positive-feedback loop capable of bistable operation.

[5] Digital implementations of multivibrators were presented in Chapter 11. Here, we are interested in implementations utilizing op amps.

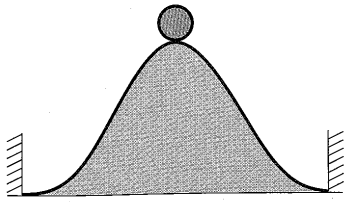


FIGURE 13.18 A physical analogy for the operation of the bistable circuit. The ball cannot remain at the top of the hill for any length of time (a state of unstable equilibrium or metastability); the inevitably present disturbance will cause the ball to fall to one side or the other, where it can remain indefinitely (the two stable states).

causes the bistable circuit to switch to one of its two stable states. This is in sharp contrast to the case when the feedback is negative, causing a virtual short circuit to appear between the op amp's input terminals and maintaining this virtual short circuit in the face of disturbances. A physical analogy for the operation of the bistable circuit is depicted in Fig. 13.18.

13.4.2 Transfer Characteristics of the Bistable Circuit

The question naturally arises as to how we can make the bistable circuit of Fig. 13.17 change state. To help answer this crucial question, we derive the transfer characteristics of the bistable. Reference to Fig. 13.17 indicates that either of the two circuit nodes that are connected to ground can serve as an input terminal. We investigate both possibilities.

Figure 13.19(a) shows the bistable circuit with a voltage v_I applied to the inverting input terminal of the op amp. To derive the transfer characteristic v_O–v_I, assume that v_O is at one of its two possible levels, say L_+, and thus $v_+ = \beta L_+$. Now as v_I is increased from 0 V we can see from the circuit that nothing happens until v_I reaches a value equal to v_+ (i.e., βL_+). As v_I begins to exceed this value, a net negative voltage develops between the input terminals of the op amp. This voltage is amplified by the open-loop gain of the op amp, and thus v_O goes negative. The voltage divider in turn causes v_+ to go negative, thus increasing the net negative input to the op amp and keeping the regenerative process going. This process culminates in the op amp saturating in the negative direction: that is, with $v_O = L_-$ and, correspondingly, $v_+ = \beta L_-$. It is easy to see that increasing v_I further has no effect on the acquired state of the bistable circuit. Figure 13.19(b) shows the transfer characteristic for increasing v_I. Observe that the characteristic is that of a comparator with a threshold voltage denoted V_{TH}, where $V_{TH} = \beta L_+$.

Next consider what happens as v_I is decreased. Since now $v_+ = \beta L_-$, we see that the circuit remains in the negative-saturation state until v_I goes negative to the point that it equals βL_-. As v_I goes below this value, a net positive voltage appears between the op amp's input terminals. This voltage is amplified by the op-amp gain and thus gives rise to a positive voltage at the op amp's output. The regenerative action of the positive-feedback loop then sets in and causes the circuit eventually to go to its positive-saturation state, in which $v_O = L_+$ and $v_+ = \beta L_+$. The transfer characteristic for decreasing v_I is shown in Fig. 13.19(c). Here again we observe that the characteristic is that of a comparator, but with a threshold voltage $V_{TL} = \beta L_-$.

The complete transfer characteristics, v_O–v_I, of the circuit in Fig. 13.19(a) can be obtained by combining the characteristics in Fig. 13.19(b) and (c), as shown in Fig. 13.19(d). As indicated, the circuit changes state at different values of v_I, depending on whether v_I is increasing or decreasing. Thus the circuit is said to exhibit *hysteresis;* the width of the hysteresis is the difference between the high threshold V_{TH} and the low threshold V_{TL}. Also note that the bistable circuit is in effect a comparator with hysteresis. As will be shown shortly, adding hysteresis to a comparator's characteristics can be very beneficial in certain applications. Finally, observe that because the bistable circuit of Fig. 13.19 switches from the positive state ($v_O = L_+$) to the negative state ($v_O = L_-$) as v_I is increased past the positive threshold V_{TH}, the circuit is said to be *inverting*. A bistable circuit with a *noninverting* transfer characteristic will be presented shortly.

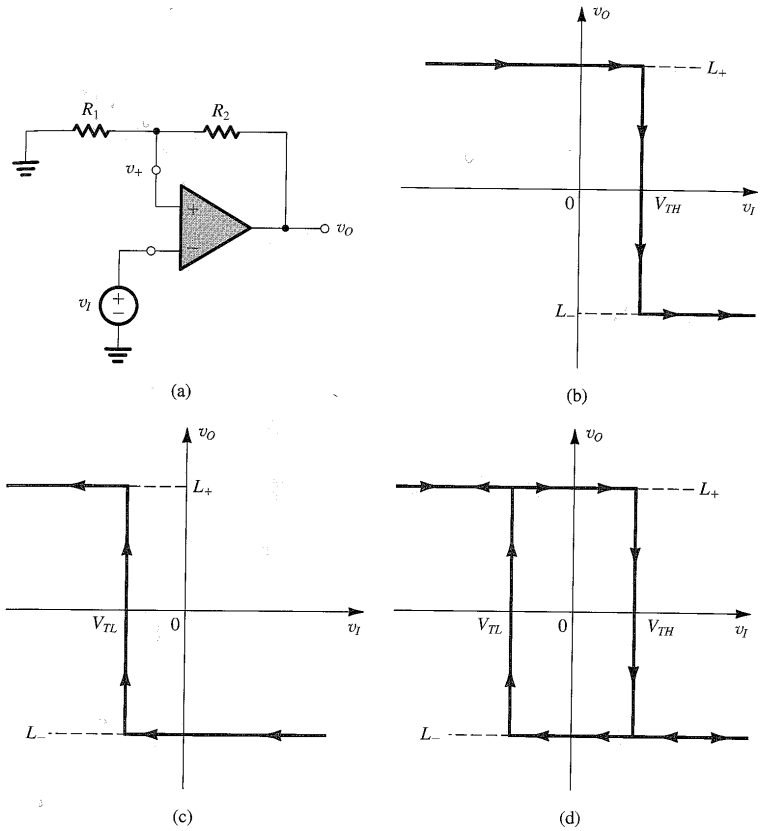


FIGURE 13.19 **(a)** The bistable circuit of Fig. 13.17 with the negative input terminal of the op amp disconnected from ground and connected to an input signal v_I. **(b)** The transfer characteristic of the circuit in (a) for increasing v_I. **(c)** The transfer characteristic for decreasing v_I. **(d)** The complete transfer characteristics.

13.4.3 Triggering the Bistable Circuit

Returning now to the question of how to make the bistable circuit change state, we observe from the transfer characteristics of Fig. 13.19(d) that if the circuit is in the L_+ state it can be switched to the L_- state by applying an input v_I of value greater than $V_{TH} \equiv \beta L_+$. Such an input causes a net negative voltage to appear between the input terminals of the op amp, which initiates the regenerative cycle that culminates in the circuit switching to the L_- stable state. Here it is important to note that the input v_I merely initiates or *triggers* regeneration. Thus we can remove v_I with no effect on the regeneration process. In other words, v_I can be simply a pulse of short duration. The input signal v_I is thus referred to as a **trigger signal,** or simply a **trigger.**

The characteristics of Fig. 13.19(d) indicate also that the bistable circuit can be switched to the positive state ($v_O = L_+$) by applying a negative trigger signal v_I of magnitude greater than that of the negative threshold V_{TL}.

13.4.4 The Bistable Circuit as a Memory Element

We observe from Fig. 13.19(d) that for input voltages in the range $V_{TL} < v_I < V_{TH}$, the output can be either L_+ or L_-, *depending on the state that the circuit is already in.* Thus, for this input range, the output is determined by the *previous* value of the trigger signal (the trigger signal that caused the circuit to be in its current state). Thus the circuit exhibits *memory.* Indeed, the bistable multivibrator is the basic memory element of digital systems, as we have seen in Chapter 11. Finally, note that in analog circuit applications, such as the ones of concern to us in this chapter, the bistable circuit is also known as a **Schmitt trigger.**

13.4.5 A Bistable Circuit with Noninverting Transfer Characteristics

The basic bistable feedback loop of Fig. 13.17 can be used to derive a circuit with noninverting transfer characteristics by applying the input signal v_I (the trigger signal) to the terminal of R_1 that is connected to ground. The resulting circuit is shown in Fig. 13.20(a). To obtain the transfer characteristics we first employ superposition to the linear circuit formed by R_1 and R_2, thus expressing v_+ in terms of v_I and v_O as

$$v_+ = v_I \frac{R_2}{R_1 + R_2} + v_O \frac{R_1}{R_1 + R_2} \tag{13.28}$$

From this equation we see that if the circuit is in the positive stable state with $v_O = L_+$, positive values for v_I will have no effect. To trigger the circuit into the L_- state, v_I must be made negative and of such a value as to make v_+ decrease below zero. Thus the low threshold V_{TL} can be found by substituting in Eq. (13.28) $v_O = L_+$, $v_+ = 0$, and $v_I = V_{TL}$. The result is

$$V_{TL} = -L_+(R_1/R_2) \tag{13.29}$$

Similarly, Eq. (13.28) indicates that when the circuit is in the negative-output state ($v_O = L_-$), negative values of v_I will make v_+ more negative with no effect on operation. To initiate the regeneration process that causes the circuit to switch to the positive state, v_+ must be made

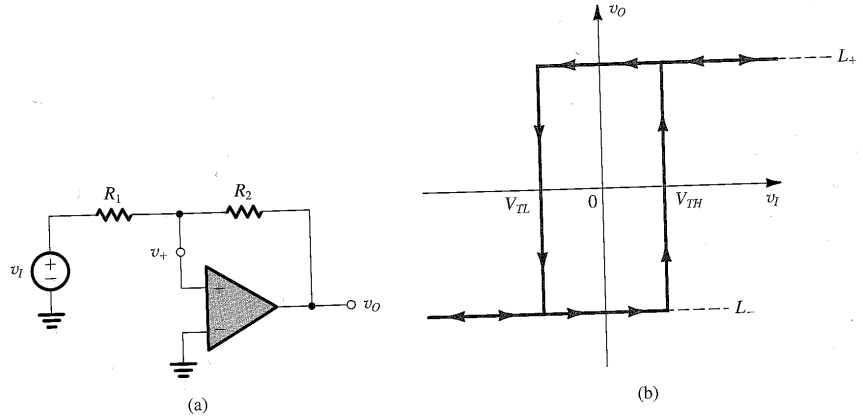


FIGURE 13.20 **(a)** A bistable circuit derived from the positive-feedback loop of Fig. 13.17 by applying v_I through R_1. **(b)** The transfer characteristic of the circuit in (a) is noninverting. (Compare it to the inverting characteristic in Fig. 13.19d.)

to go slightly positive. The value of v_I that causes this to happen is the high threshold voltage V_{TH}, which can be found by substituting in Eq. (13.28) $v_O = L_-$ and $v_+ = 0$. The result is

$$V_{TH} = -L_-(R_1/R_2) \tag{13.30}$$

The complete transfer characteristic of the circuit of Fig. 13.20(a) is displayed in Fig. 13.20(b). Observe that a positive triggering signal v_I (of value greater than V_{TH}) causes the circuit to switch to the positive state (v_O goes from L_- to L_+). Thus the transfer characteristic of this circuit is noninverting.

13.4.6 Application of the Bistable Circuit as a Comparator

The comparator is an analog-circuit building block that is used in a variety of applications ranging from detecting the level of an input signal relative to a preset threshold value, to the design of analog-to-digital (A/D) converters (see Section 9.1). Although one normally thinks of the comparator as having a single threshold value (see Fig. 13.21a), it is useful in many applications to add hysteresis to the comparator characteristics. If this is done, the comparator exhibits two threshold values, V_{TL} and V_{TH}, symmetrically placed about the

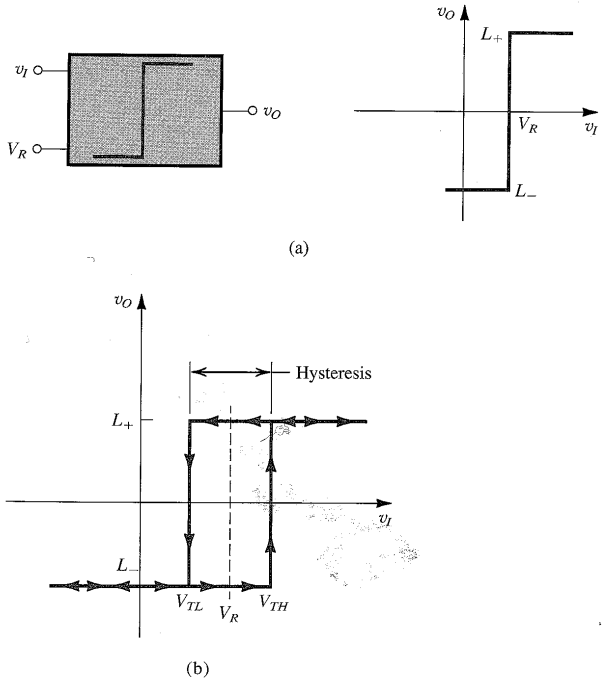


FIGURE 13.21 **(a)** Block diagram representation and transfer characteristic for a comparator having a reference, or threshold, voltage V_R. **(b)** Comparator characteristic with hysteresis.

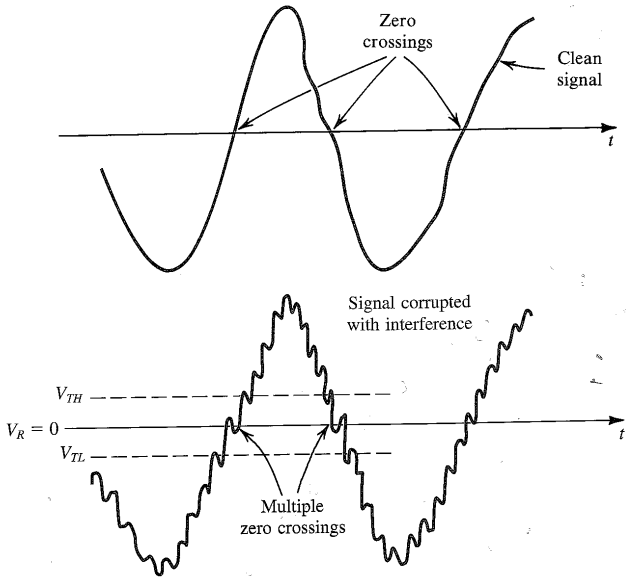


FIGURE 13.22 Illustrating the use of hysteresis in the comparator characteristics as a means of rejecting interference.

desired reference level, as indicated in Fig. 13.21(b). Usually V_{TH} and V_{TL} are separated by a small amount, say 100 mV.

To demonstrate the need for hysteresis we consider a common application of comparators. It is required to design a circuit that detects and counts the zero crossings of an arbitrary waveform. Such a function can be implemented using a comparator whose threshold is set to 0 V. The comparator provides a step change at its output every time a zero crossing occurs. Each step change can be used to generate a pulse, and the pulses are fed to a counter circuit.

Imagine now what happens if the signal being processed has—as it usually does have—interference superimposed on it, say of a frequency much higher than that of the signal. It follows that the signal might cross the zero axis a number of times around each of the zero-crossing points we are trying to detect, as shown in Fig. 13.22. The comparator would thus change state a number of times at each of the zero crossings, and our count would obviously be in error. However, if we have an idea of the expected peak-to-peak amplitude of the interference, the problem can be solved by introducing hysteresis of appropriate width in the comparator characteristics. Then, if the input signal is increasing in magnitude, the comparator with hysteresis will remain in the low state until the input level exceeds the high threshold V_{TH}. Subsequently the comparator will remain in the high state even if, owing to interference, the signal decreases below V_{TH}. The comparator will switch to the low state only if the input signal is decreased below the low threshold V_{TL}. The situation is illustrated in Fig. 13.22, from which we see that including hysteresis in the comparator characteristics provides an effective means for rejecting interference (thus providing another form of filtering).

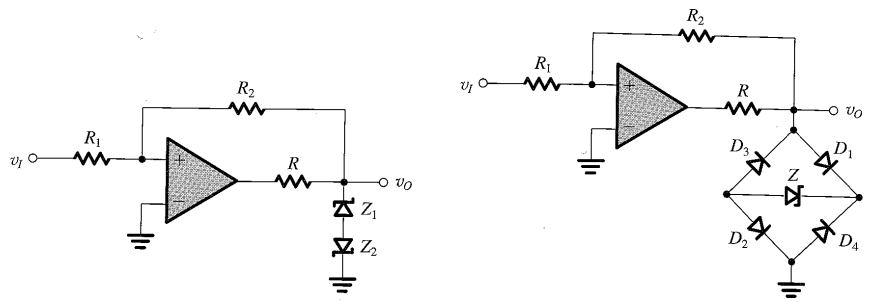


FIGURE 13.23 Limiter circuits are used to obtain more precise output levels for the bistable circuit. In both circuits the value of R should be chosen to yield the current required for the proper operation of the zener diodes. **(a)** For this circuit $L_+ = V_{Z_1} + V_D$ and $L_- = -(V_{Z_2} + V_D)$, where V_D is the forward diode drop. **(b)** For this circuit $L_+ = V_Z + V_{D_1} + V_{D_2}$ and $L_- = -(V_Z + V_{D_3} + V_{D_4})$.

13.4.7 Making the Output Levels More Precise

The output levels of the bistable circuit can be made more precise than the saturation voltages of the op amp are by cascading the op amp with a limiter circuit (see Section 3.6 for a discussion of limiter circuits). Two such arrangements are shown in Fig. 13.23.

EXERCISES

D13.11 The op amp in the bistable circuit of Fig. 13.19(a) has output saturation voltages of ±13 V. Design the circuit to obtain threshold voltages of ±5 V. For $R_1 = 10$ kΩ, find the value required for R_2.

Ans. 16 kΩ

D13.12 If the op amp in the circuit of Fig. 13.20(a) has ±10-V output saturation levels, design the circuit to obtain ±5-V thresholds. Give suitable component values.

Ans. Possible choice: $R_1 = 10$ kΩ and $R_2 = 20$ kΩ

13.13 Consider a bistable circuit with a noninverting transfer characteristic, and let $L_+ = -L_- = 10$ V and $V_{TH} = -V_{TL} = 5$ V. If v_I is a triangular wave with a 0-V average, a 10-V peak amplitude, and a 1-ms period, sketch the waveform of v_O. Find the time interval between the zero crossings of v_I and v_O.

Ans. v_O is a square wave with 0-V average, 10-V amplitude, and 1-ms period and is delayed by 125 μs relative to v_I.

13.14 Consider an op amp having saturation levels of ±12 V used without feedback, with the inverting input terminal connected to +3 V and the noninverting input terminal connected to v_I. Characterize its operation as a comparator. What are L_+, L_-, and V_R, as defined in Fig. 13.21(a)?

Ans. +12 V; −12 V; +3 V

13.15 In the circuit of Fig. 13.20(a) let $L_+ = -L_- = 10$ V and $R_1 = 1$ kΩ. Find a value for R_2 that gives a hysteresis of 100-mV width.

Ans. 200 kΩ

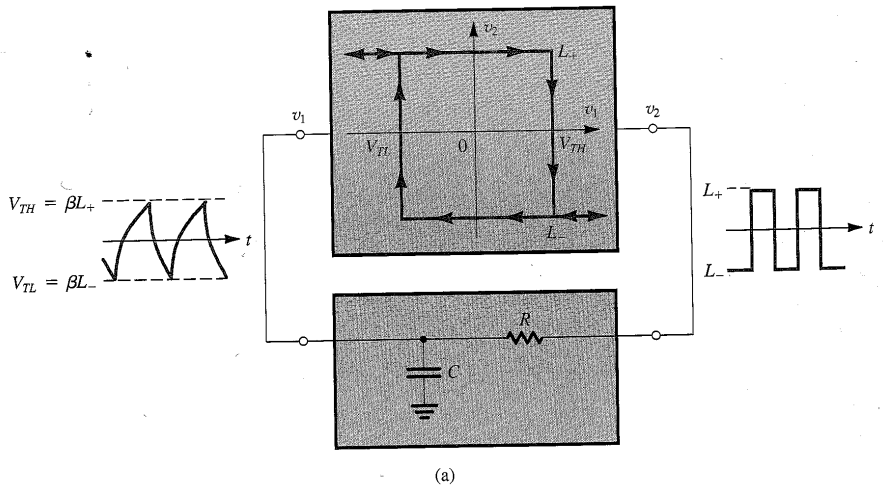
13.5 GENERATION OF SQUARE AND TRIANGULAR WAVEFORMS USING ASTABLE MULTIVIBRATORS

A square waveform can be generated by arranging for a bistable multivibrator to switch states periodically. This can be done by connecting the bistable multivibrator with an RC circuit in a feedback loop, as shown in Fig. 13.24(a). Observe that the bistable multivibrator has an inverting transfer characteristic and can thus be realized using the circuit of Fig. 13.19(a). This results in the circuit of Fig. 13.24(b). We shall show shortly that this circuit has no stable states and thus is appropriately named an **astable multivibrator.**

13.5.1 Operation of the Astable Multivibrator

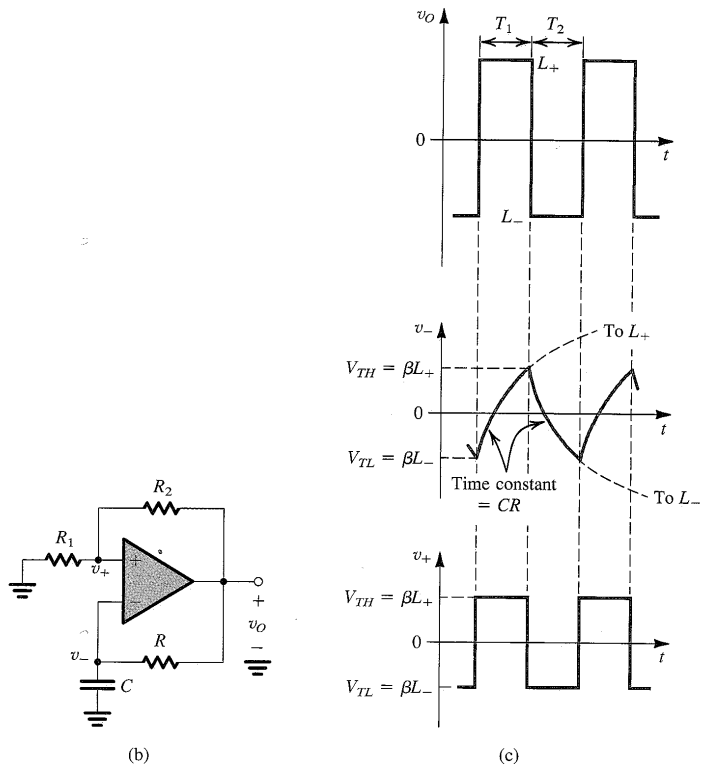
To see how the astable multivibrator operates, refer to Fig. 13.24(b) and let the output of the bistable multivibrator be at one of its two possible levels, say L_+. Capacitor C will charge toward this level through resistor R. Thus the voltage across C, which is applied to the negative input terminal of the op amp and thus is denoted v_-, will rise exponentially toward L_+ with a time constant $\tau = CR$. Meanwhile, the voltage at the positive input terminal of the op amp is $v_+ = \beta L_+$. This situation will continue until the capacitor voltage reaches the positive threshold $V_{TH} = \beta L_+$ at which point the bistable multivibrator will switch to the other stable state in which $v_O = L_-$ and $v_+ = \beta L_-$. The capacitor will then start discharging, and its voltage, v_-, will decrease exponentially toward L_-. This new state will prevail until v_- reaches the negative threshold $V_{TL} = \beta L_-$, at which time the bistable multivibrator switches to the positive-output state, the capacitor begins to charge, and the cycle repeats itself.

From the preceding description we see that the astable circuit oscillates and produces a square waveform at the output of the op amp. This waveform, and the waveforms at the two input terminals of the op amp, are displayed in Fig. 13.24(c). The period T of the square



(a)

FIGURE 13.24 **(a)** Connecting a bistable multivibrator with inverting transfer characteristics in a feedback loop with an RC circuit results in a square-wave generator.



(b) (c)

FIGURE 13.24 *(Continued)* **(b)** The circuit obtained when the bistable multivibrator is implemented with the circuit of Fig. 13.19(a). **(c)** Waveforms at various nodes of the circuit in (b). This circuit is called an astable multivibrator.

wave can be found as follows: During the charging interval T_1 the voltage v_- across the capacitor at any time t, with $t = 0$ at the beginning of T_1, is given by (see Appendix D)

$$v_- = L_+ - (L_+ - \beta L_-)e^{-t/\tau}$$

where $\tau = CR$. Substituting $v_- = \beta L_+$ at $t = T_1$ gives

$$T_1 = \tau \ln \frac{1 - \beta(L_-/L_+)}{1 - \beta} \tag{13.31}$$

Similarly, during the discharge interval T_2 the voltage v_- at any time t, with $t = 0$ at the beginning of T_2, is given by

$$v_- = L_- - (L_- - \beta L_+)e^{-t/\tau}$$

Substituting $v_- = \beta L_-$ at $t = T_2$ gives

$$T_2 = \tau \ln \frac{1 - \beta(L_+/L_-)}{1 - \beta} \tag{13.32}$$

Equations (13.31) and (13.32) can be combined to obtain the period $T = T_1 + T_2$. Normally, $L_+ = -L_-$, resulting in symmetrical square waves of period T given by

$$T = 2\tau \ln \frac{1+\beta}{1-\beta} \tag{13.33}$$

Note that this square-wave generator can be made to have variable frequency by switching different capacitors C (usually in decades) and by continuously adjusting R (to obtain continuous frequency control within each decade of frequency). Also, the waveform across C can be made almost triangular by using a small value for the parameter β. However, triangular waveforms of superior linearity can be easily generated using the scheme discussed next.

Before leaving this section, however, note that although the astable circuit has no stable states, it has two *quasi-stable* states and remains in each for a time interval determined by the time constant of the RC network and the thresholds of the bistable multivibrator.

EXERCISES

13.16 For the circuit in Fig. 13.24(b), let the op-amp saturation voltages be ±10 V, $R_1 = 100\ \text{k}\Omega$, $R_2 = R = 1\ \text{M}\Omega$, and $C = 0.01\ \mu\text{F}$. Find the frequency of oscillation.

Ans. 274 Hz

13.17 Consider a modification of the circuit of Fig. 13.24(b) in which R_1 is replaced by a pair of diodes connected in parallel in opposite directions. For $L_+ = -L_- = 12$ V, $R_2 = R = 10\ \text{k}\Omega$, $C = 0.1\ \mu\text{F}$, and the diode voltage a constant denoted V_D, find an expression for frequency as a function of V_D. If $V_D = 0.70$ V at 25°C with a TC of −2 mV/°C, find the frequency at 0°C, 25°C, 50°C, and 100°C. Note that the output of this circuit can be sent to a remotely connected frequency meter to provide a digital readout of temperature.

Ans. $f = 500/\ln[(12 + V_D)/(12 - V_D)]$ Hz; 3995 Hz, 4281 Hz, 4611 Hz, 5451 Hz

13.5.2 Generation of Triangular Waveforms

The exponential waveforms generated in the astable circuit of Fig. 13.24 can be changed to triangular by replacing the low-pass RC circuit with an integrator. (The integrator is, after all, a low-pass circuit with a corner frequency at dc.) The integrator causes linear charging and discharging of the capacitor, thus providing a triangular waveform. The resulting circuit is shown in Fig. 13.25(a). Observe that because the integrator is inverting, it is necessary to invert the characteristics of the bistable circuit. Thus the bistable circuit required here is of the noninverting type and can be implemented using the circuit of Fig. 13.2.

We now proceed to show how the feedback loop of Fig. 13.25(a) oscillates and generates a triangular waveform v_1 at the output of the integrator and a square waveform v_2 at the output of the bistable circuit: Let the output of the bistable circuit be at L_+. A current equal to L_+/R will flow into the resistor R and through capacitor C, causing the output of the integrator to *linearly* decrease with a slope of $-L_+/CR$, as shown in Fig. 13.25(c). This will continue until the integrator output reaches the lower threshold V_{TL} of the bistable circuit, at which point the bistable circuit will switch states, its output becoming negative and equal to

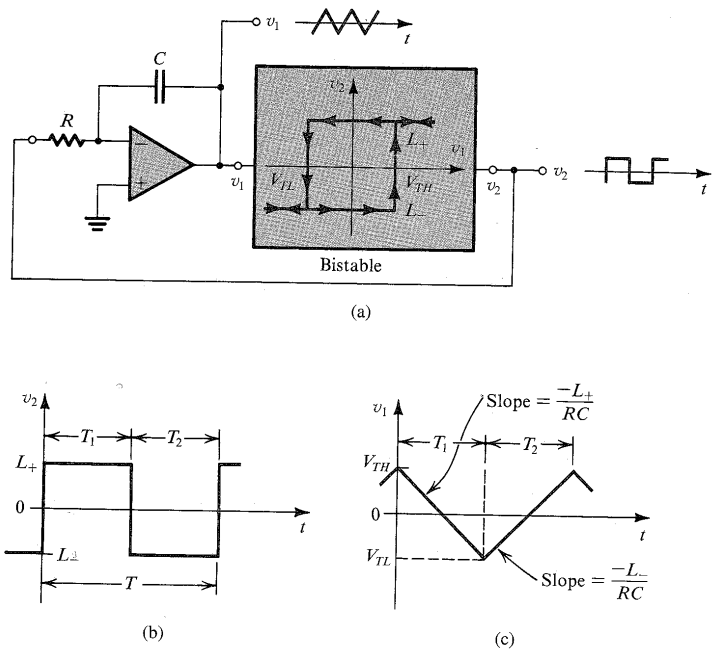


FIGURE 13.25 A general scheme for generating triangular and square waveforms.

L_-. At this moment the current through R and C will reverse direction, and its value will become equal to $|L_-|/R$. It follows that the integrator output will start to increase linearly with a positive slope equal to $|L_-|/CR$. This will continue until the integrator output voltage reaches the positive threshold of the bistable circuit, V_{TH}. At this point the bistable circuit switches, its output becomes positive (L_+), the current into the integrator reverses direction, and the output of the integrator starts to decrease linearly, beginning a new cycle.

From the discussion above it is relatively easy to derive an expression for the period T of the square and triangular waveforms. During the interval T_1 we have, from Fig. 13.25(c),

$$\frac{V_{TH} - V_{TL}}{T_1} = \frac{L_+}{CR}$$

from which we obtain

$$T_1 = CR\frac{V_{TH} - V_{TL}}{L_+} \tag{13.34}$$

Similarly, during T_2 we have

$$\frac{V_{TH} - V_{TL}}{T_2} = \frac{-L_-}{CR}$$

from which we obtain

$$T_2 = CR\frac{V_{TH} - V_{TL}}{-L_-} \tag{13.35}$$

Thus to obtain symmetrical square waves we design the bistable circuit to have $L_+ = -L_-$.

EXERCISE

D13.18 Consider the circuit of Fig. 13.25(a) with the bistable circuit realized by the circuit in Fig. 13.20(a). If the op amps have saturation voltages of ±10 V and if a capacitor $C = 0.01\ \mu$F and a resistor $R_1 = 10$ kΩ are used, find the values of R and R_2 (note that R_1 and R_2 are associated with the bistable circuit of Fig. 13.20a) such that the frequency of oscillation is 1 kHz and the triangular waveform has a 10-V peak-to-peak amplitude.

Ans. 50 kΩ; 20 kΩ

13.6 GENERATION OF A STANDARDIZED PULSE—THE MONOSTABLE MULTIVIBRATOR

In some applications the need arises for a pulse of known height and width generated in response to a trigger signal. Because the width of the pulse is predictable, its trailing edge can be used for timing purposes—that is, to initiate a particular task at a specified time. Such a standardized pulse can be generated by the third type of multivibrator, the **monostable multivibrator.**

The monostable multivibrator has one stable state in which it can remain indefinitely. It also has a quasi-stable state to which it can be triggered and in which it stays for a predetermined interval equal to the desired width of the output pulse. When this interval expires, the monostable multivibrator returns to its stable state and remains there, awaiting another triggering signal. The action of the monostable multivibrator has given rise to its alternative name, the *one shot*.

Figure 13.26(a) shows an op-amp monostable circuit. We observe that this circuit is an augmented form of the astable circuit of Fig. 13.24(b). Specifically, a clamping diode D_1 is added across the capacitor C_1, and a trigger circuit composed of capacitor C_2, resistor R_4, and diode D_2 is connected to the noninverting input terminal of the op amp. The circuit operates as follows: In the stable state, which prevails in the absence of the triggering signal, the output of the op amp is at L_+ and diode D_1 is conducting through R_3 and thus clamping the voltage v_B to one diode drop above ground. We select R_4 much larger than R_1, so that diode D_2 will be conducting a very small current and the voltage v_C will be very closely determined by the voltage divider R_1, R_2. Thus $v_C = \beta L_+$, where $\beta = R_1/(R_1 + R_2)$. The stable state is maintained because βL_+ is greater than V_{D1}.

Now consider the application of a negative-going step at the trigger input and refer to the signal waveforms shown in Fig. 13.26(b). The negative triggering edge will be coupled to the cathode of diode D_2 via capacitor C_2, and thus D_2 conducts heavily and pulls node C down. If the trigger signal is of sufficient height to cause v_C to go below v_B, the op amp will see a net negative input voltage and its output will switch to L_-. This in turn will cause v_C to go negative to βL_-, keeping the op amp in its newly acquired state. Note that D_2 will then cut off, thus isolating the circuit from any further changes at the trigger input terminal.

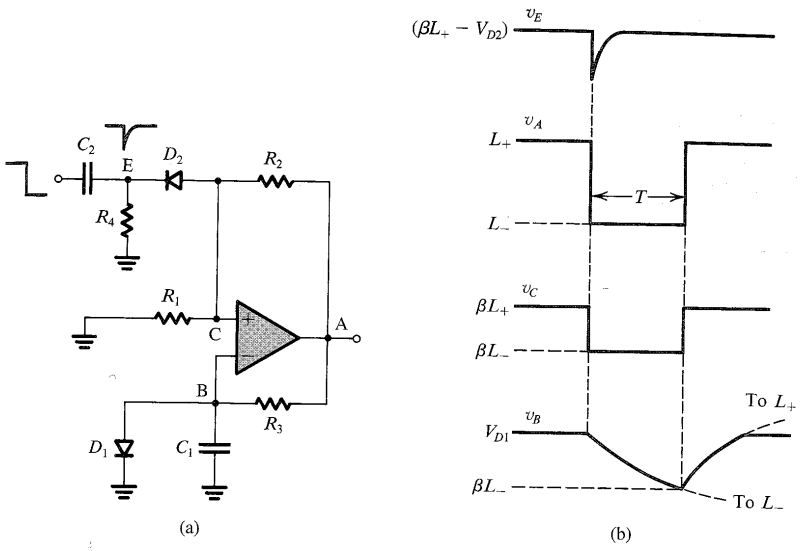


FIGURE 13.26 **(a)** An op-amp monostable circuit. **(b)** Signal waveforms in the circuit of (a).

The negative voltage at A causes D_1 to cut off, and C_1 begins to discharge exponentially toward L_- with a time constant C_1R_3. The monostable multivibrator is now in its *quasi-stable state,* which will prevail until the declining v_B goes below the voltage at node C, which is βL_-. At this instant the op-amp output switches back to L_+ and the voltage at node C goes back to βL_+. Capacitor C_1 then charges toward L_+ until diode D_1 turns on and the circuit returns to its stable state.

From Fig. 13.26(b), we observe that a negative pulse is generated at the output during the quasi-stable state. The duration T of the output pulse is determined from the exponential waveform of v_B,

$$v_B(t) = L_- - (L_- - V_{D1})e^{-t/C_1R_3}$$

by substituting $v_B(T) = \beta L_-$,

$$\beta L_- = L_- - (L_- - V_{D1})e^{-T/C_1R_3}$$

which yields

$$T = C_1R_3 \ln\left(\frac{V_{D1} - L_-}{\beta L_- - L_-}\right) \tag{13.36}$$

For $V_{D1} \ll |L_-|$, this equation can be approximated by

$$T \simeq C_1R_3 \ln\left(\frac{1}{1-\beta}\right) \tag{13.37}$$

Finally, note that the monostable circuit should not be triggered again until capacitor C_1 has been recharged to V_{D1}; otherwise the resulting output pulse will be shorter than normal. This recharging time is known as the **recovery period.** Circuit techniques exist for shortening the recovery period.

EXERCISE

13.19 For the monostable circuit of Fig. 13.26(a) find the value of R_3 that will result in a 100-μs output pulse for $C_1 = 0.1\ \mu$F, $\beta = 0.1$, $V_D = 0.7$ V, and $L_+ = -L_- = 12$ V.

Ans. 6171 Ω

13.7 INTEGRATED-CIRCUIT TIMERS

Commercially available integrated-circuit packages exist that contain the bulk of the circuitry needed to implement monostable and astable multivibrators with precise characteristics. In this section we discuss the most popular of such ICs, the **555 timer.** Introduced in 1972 by the Signetics Corporation as a bipolar integrated circuit, the 555 is also available in CMOS technology and from a number of manufacturers.

13.7.1 The 555 Circuit

Figure 13.27 shows a block-diagram representation of the 555 timer circuit [for the actual circuit, refer to Grebene (1984)]. The circuit consists of two comparators, an SR flip-flop,

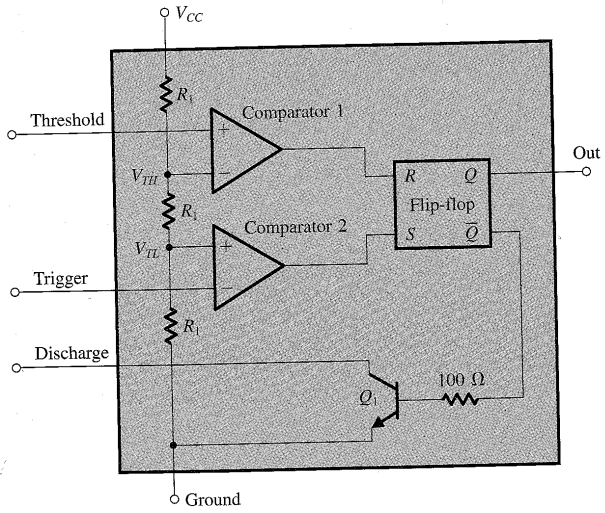


FIGURE 13.27 A block diagram representation of the internal circuit of the 555 integrated-circuit timer.

and a transistor Q_1 that operates as a switch. One power supply (V_{CC}) is required for operation, with the supply voltage typically 5 V. A resistive voltage divider, consisting of the three equal-valued resistors labeled R_1, is connected across V_{CC} and establishes the reference (threshold) voltages for the two comparators. These are $V_{TH} = \frac{2}{3}V_{CC}$ for comparator 1 and $V_{TL} = \frac{1}{3}V_{CC}$ for comparator 2.

We studied SR flip-flops in Chapter 11. For our purposes here we note that an SR flip-flop (also called a latch) is a bistable circuit having complementary outputs, denoted Q and $\overline{Q}$. In the *set* state, the output at Q is "high" (approximately equal to V_{CC}) and that at $\overline{Q}$ is "low" (approximately equal to 0 V). In the other stable state, termed the *reset* state, the output at Q is low and that at $\overline{Q}$ is high. The flip-flop is set by applying a high level (V_{CC}) to its set input terminal, labeled S. To reset the flip-flop, a high level is applied to the reset input terminal, labeled R. Note that the reset and set input terminals of the flip-flop in the 555 circuit are connected to the outputs of comparator 1 and comparator 2, respectively.

The positive-input terminal of comparator 1 is brought out to an external terminal of the 555 package, labeled Threshold. Similarly, the negative-input terminal of comparator 2 is connected to an external terminal labeled Trigger, and the collector of transistor Q_1 is connected to a terminal labeled Discharge. Finally, the Q output of the flip-flop is connected to the output terminal of the timer package, labeled Out.

13.7.2 Implementing a Monostable Multivibrator Using the 555 IC

Figure 13.28(a) shows a monostable multivibrator implemented using the 555 IC together with an external resistor R and an external capacitor C. In the stable state the flip-flop will be in the reset state, and thus its $\overline{Q}$ output will be high, turning on transistor Q_1. Transistor Q_1 will be saturated, and thus v_C will be close to 0 V, resulting in a low level at the output of comparator 1. The voltage at the trigger input terminal, labeled v_{trigger}, is kept high (greater than V_{TL}), and thus the output of comparator 2 also will be low. Finally, note that since the flip-flop is in the reset state, Q will be low and thus v_O will be close to 0 V.

To trigger the monostable multivibrator, a negative input pulse is applied to the trigger input terminal. As v_{trigger} goes below V_{TL}, the output of comparator 2 goes to the high level, thus setting the flip-flop. Output Q of the flip-flop goes high, and thus v_O goes high, and output $\overline{Q}$ goes low, turning off transistor Q_1. Capacitor C now begins to charge up through resistor R, and its voltage v_C rises exponentially toward V_{CC}, as shown in Fig. 13.28(b). The monostable multivibrator is now in its quasi-stable state. This state prevails until v_C reaches, and begins to exceed, the threshold of comparator 1, V_{TH}, at which time the output of comparator 1 goes high, resetting the flip-flop. Output $\overline{Q}$ of the flip-flop now goes high and turns on transistor Q_1. In turn, transistor Q_1 rapidly discharges capacitor C, causing v_C to go to 0 V. Also, when the flip-flop is reset its Q output goes low, and thus v_O goes back to 0 V. The monostable multivibrator is now back in its stable state and is ready to receive a new triggering pulse.

From the description above we see that the monostable multivibrator produces an output pulse v_O as indicated in Fig. 13.28(b). The width of the pulse, T, is the time interval that the monostable multivibrator spends in the quasi-stable state; it can be determined by reference to the waveforms in Fig. 13.28(b) as follows: Denoting the instant at which the trigger pulse is applied as $t = 0$, the exponential waveform of v_C can be expressed as

$$v_C = V_{CC}(1 - e^{-t/CR}) \tag{13.38}$$