High Frequency Performance of CASCODE Amplifier

Objective:

Measure the small-signal frequency response of a CASCODE amplifier and compare the bandwidth improvement versus the single stage CE amplifier.

Introduction:

The CASCODE amplifier is comprised of two cascade stages of a CE and CB amplifiers. The CE makes up the input stage with a very low voltage gain of $A_{v1} \approx - 1$ and the second (the output) is a wideband CB amplifier with a voltage gain of $A_{v2} = g_m R_C$. The input impedance of C_B, R_{in2}, viewed at the emitter, is very low equal to, $R_{in2} \approx 1/gm$. And it is this low impedance that causes the CE to have a low voltage gain. Generally the common CE amplifier due to its high voltage gain has a much larger input capacitance due to the enhanced Miller effect. Since the voltage gain of CE is reduced to nearly unity, in CASCODE configuration, the input capacitance will be reduced significantly and hence the overall bandwidth will increase considerably. Note that $A_{v1} = - g_m R_{in2}$ where $R_{in2} \approx 1/g_m$, is the collector resistance of the stage one, and hence $A_{v1} \approx - 1$.

Design:

1) Design of the CASCODE amplifier:
   $I_{C1q} \approx I_{C2q} = 10$ mA and the output AC resistance, R_o, is 470 Ω.
2) DC currents for good DC stability:
   $I_{R1} = 11 \times I_{B2q}$
   $I_{R2} = 10 \times I_{B1q}$
   $I_{R3} = 9 \times I_{B1q}$
   $V_E = 2.7$ V
   $V_{B2} = 8.0$ V the terminal voltage of both transistors will be identical to the transistor used in the previous CE analysis. This measure will ensure the junction capacitances in both circuits will remain unchanged.
   Assumptions: $\beta \approx 100$ and $V_T = 25$ mV, where V_T is the thermal voltage of the semiconductor.

   a) $I_{B2} = \frac{I_C}{\beta} = 100\ \mu A = I_{B1}$

      $I_{B2} = I_{B1}$

   b) $R_1 = \frac{V_{CC} - V_{B2}}{11 \times I_{B2}} = 7.82\ k\Omega = 7.5\ k\Omega$

      $R_o = R_C = 470\ \Omega$

      $V_{B1} = V_E + V_{BE} = 3.4\ V$

$$R_2 = \frac{V_{B2} - V_{B1}}{10 \times I_B} = 4.6\ k\Omega = 4.7\ k\Omega$$

$$R_3 = \frac{V_{B1}}{9 \times I_B} = 3.78\ k\Omega = 3.9\ k\Omega$$

$$R_E = \frac{V_E}{I_C} = 270\ \Omega$$

3) Small signal equivalent circuit of the CASCODE stage using hybrid-π models, mid-band frequency voltage gain of the CE stage defined as $A_{v1} = v_{o1}/v_i$. Including Calculation of the gain of the CB stage, $A_{v2} = v_o/v_{i2}$.

a) $g_m = \frac{I_C}{V_T} = \frac{10\ mA}{25\ mV} = 0.4\ S,$

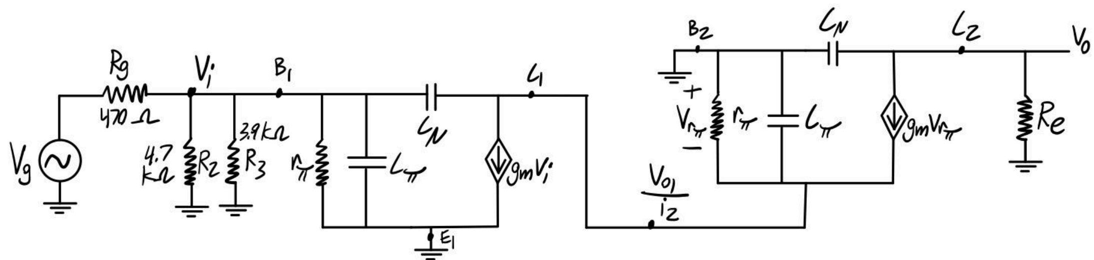
$$R_{in2} = \frac{1}{g_m} = \frac{1}{0.4\ S} = 2.5\ \Omega$$

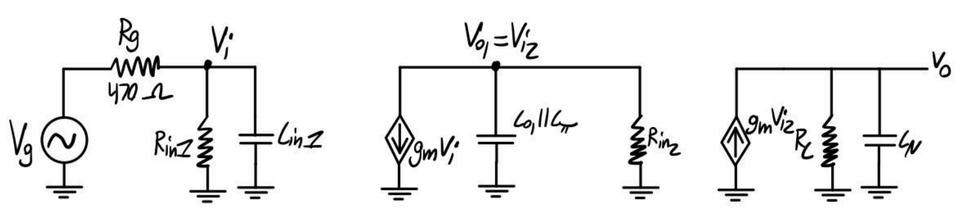
$$r_\pi = \frac{\beta}{g_m} = \frac{100}{0.4} = 250\ \Omega$$

$$R_{in1} = R_2 || R_3 || r_\pi = 224\ \Omega$$

$$A_{v1} = \frac{v_{o1}}{v_i} = -g_m R_{in2} = -(0.4\ S)(2.5\ \Omega) = -1,$$

$$A_{v2} = \frac{v_o}{v_{i2}} = g_m R_C = (0.4\ S)(470\ \Omega) = 188$$





4) Input and output capacitances of the amplifiers using the Miller effect partitioning technique. C_μ (C_{cb}) is approximately 8 pF from the datasheet and the base-to-emitter capacitance, C_π (AKA C_{be}) may be determined from the equation, $C_\pi = g_m/2\pi f_T - C_\mu$, where $g_m = I_{Cq}/ V_T$. Here f_T is the unity current-gain frequency of the 2N2222A transistor. For 2N2222A, f_T is assumed to be 300 MHz (Datasheet).

a) $C_\mu = 8\,pF$

$$C_\pi = \frac{g_m}{2\pi f_T} - C_\mu = \frac{0.4\,S}{2\pi(300\,MHz)} - 8\,pF = 204\,pF,$$

$$C_{in1} = (1 + |A_{v1}|)C_\mu + C_\pi = (1 + 1) \times 8\,pF + 204\,pF = 220\,pF$$

$$C_{o1} = (\frac{1+1}{1})C_\mu = 2 \times 8\,pF = 16\,pF$$

$$C_{in2} = C_\pi = 204\,pF$$

$$C_{o2} = C_\mu = 8\,pF$$

$$C_{o1}||C_\pi = 220\,pF$$

Measurement Results:

1. DC measurements for constructed circuit:

$V_{E1} = 2.97$ V $\quad V_{B1} = 3.7$ V $\quad V_{C2} = 11.65$ V $\quad V_{B2} = 8.48$ V

$I_{C2} = (V_{CC} - V_{C2})/R_C = (16.6\text{ V} - 11.6\text{ V})/470\ \Omega = 10.6$ mA

2. For $v_g = 15\ mV_{PP}$ adjusting the signal generator amplitude to about 1.5 V_{PP}; the 1000/10 resistive attenuator will reduce the generator output by approximately 100 times so that the desired 15 mV_{pp} signal can be obtained.
3. mid-band frequency (at 5-10 kHz range) voltage gains, A_V, A_g, A_{v1}, A_{v2}, the input impedance R_{in1} and the output resistance R_o:

$A_v = v_o/v_i = 132 \quad A_{v1} = v_{o1}/v_i = 0.75 \quad A_{v2} = v_o/v_{i2} = 176$

$A_g = v_o/v_g = 71.8 \quad R_{in1} = v_i/i_{in} = 560\ \Omega \quad R_o = 470\ \Omega$

where i_{in} is determined from, $i_{in} = (v_g - v_i)/R_g$.

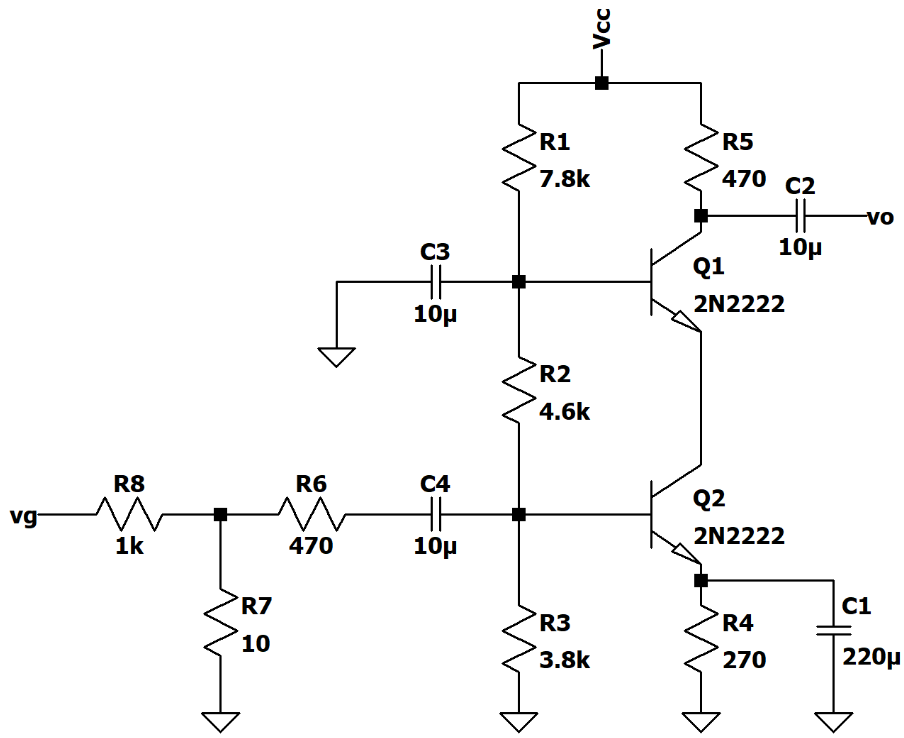
4. Vg frequency varied from 10 kHz to 10 MHz and **graph** the **“stage” overall** voltage gain, defined as $\mathbf{A_g = v_o/v_g}$, versus the applied frequency.

f (Hz)	10 k	100 k	300 k	1 M	1.2 M	2 M	3 M	4 M	10 M
v_o (mV)	912	910	901	858	643	416	275	204	83
v_g (mV_{PP})	15	15	15	15	15	15	15	15	15
$A_g = v_o/v_g$	60.80	60.66	60.07	57.20	42.87	27.73	18.33	13.60	5.53
$20\log A_g$ (dB)	35.68	35.65	35.57	35.14	32.64	28.86	25.26	22.67	14.85

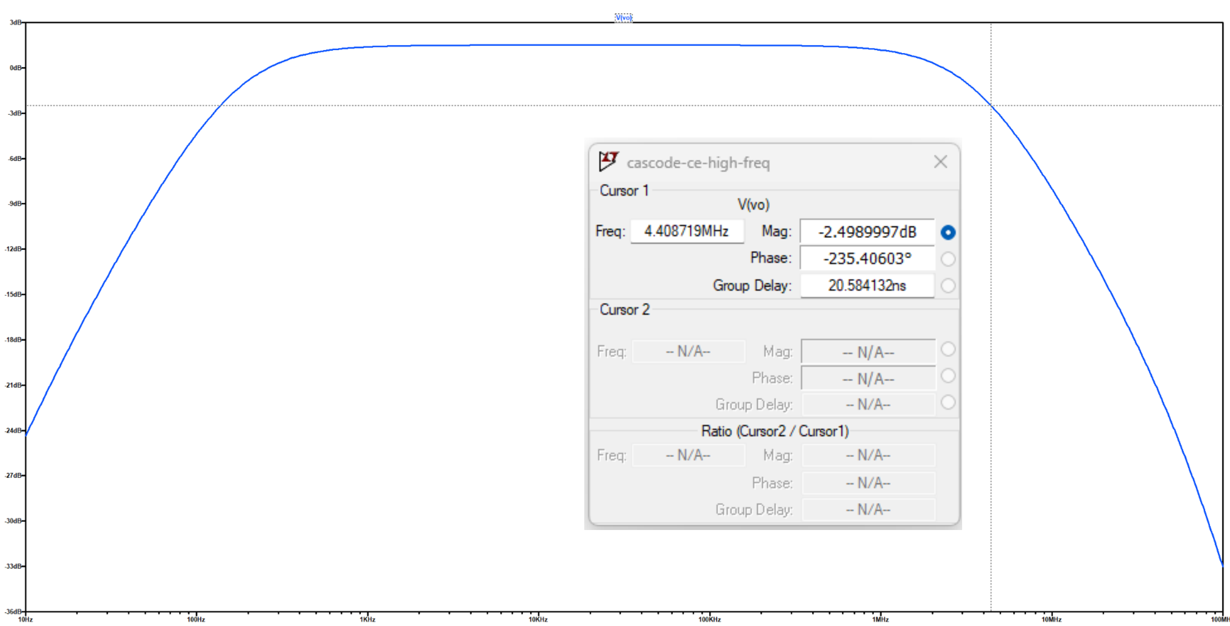
f_{ch} = 1.2 MHz

The previous measured common-emitter dominant pole frequency was 740 kHz. This cascode stage has a higher bandwidth of 1.2 Mhz by measurement than the single stage CE is due to reduced the Miller effect by providing isolation, lower the input capacitance, and lower feedback.

Simulation:



Bode Plot:



Theoretical Cutoff Frequency:

$T_1 = C_{in1}(R_g || R_{in1}) T_1 = (220\ pF)(470\ \Omega || 224\ \Omega)$

$T_1 = 33.37\ ns$

$w_{ch} = \frac{1}{T_1}, f_{ch} = \frac{1}{2\pi T_1}$

$f_{ch} = \frac{1}{2\pi(33.37\ ns)} = 4.8\ MHz$

Comparison:

From the simulation, the upper cutoff frequency resulted in 4.4 MHz. The measured value came out to 1.2 MHz. This large discrepancy can likely be attributed to parasitic capacitances, transistor variations in transition frequency, and any factor that is not accounted for in ideal simulations; however, the cascode bandwidth performance is clear.