Icarus Verilog

I. Setting up directories and folders

Create a folder for your programs in your Documents folder or on your C: drive (Window system). Let's use C:\verilog\homework5, for example. Save your Verilog files to that folder. You can use notepad or any other plain text editor to write your Verilog programs.

Here's two example Verilog files, simple.v and simple_tb.v, that you can copy into your directory to test things out.

simple.v:

```
module simple(A, B);
input [3:0] A;
output [3:0] B;

// mix up the input bits
assign B = { A[0], A[2], A[1], A[3] };
endmodule
```

simple tb.v:

```
module simple_tb;

reg [3:0] A = 4'b1010;

wire [3:0] B;

initial
  begin
     $\dumpfile(\"simple.vcd\");
     $\dumpvars(0, s);
     $\smonitor(\"A is \%b, B is \%b.\", A, B);
     #50 A = 4'b1100;
     #50 \$finish;
  end

simple s(A, B);

endmodule
```

II. Compiling your Verilog program

You need to *compile* your Verilog program before you can simulate it. Open up a DOS prompt (run cmd.exe from the Start menu) and type the following, hitting enter after each line:

```
K:
  cd verilog\homework5
  iverilog -o simple.vvp simple_tb.v
```

If the compilation went OK, you won't see any output. What this does is creating a file called simple.vvp that we can feed to the simulator.

III. Running the simulation

To run the simulation, type

```
vvp simple.vvp
```

and hit Enter. You should see output something like:

```
VCD info: dumpfile simple.vcd opened for output.
A is 1010, B is 0011.
A is 1100, B is 0101.
```

IV. Viewing the output

You can use the GTKWave program to view the output. From the DOS prompt, type

```
gtkwave simple.vcd
```

to view the results of your simulation.

V. Troubleshooting

VI. I get the error "Unknown module type: foo" when I run iverilog!

You might have run iverilog without all of the sources needed to define all of the modules. A common cause is compilingfoo_tb.v without also compiling foo.v.

VII. I get the error "foo.vvp: Unable to open input file." when I run vvp!

You might have forgotten to specify -o foo.vvp when you ran iverilog.

VIII. The vvp program never stops running!

Is there a \$finish statement anywhere in your code? Are you sure it is getting run? You should be able to type Ctrl + C at the DOS prompt to kill the simulator.

IX. There is no data file produced!

Make sure your test bench includes a \$dumpfile statement and a \$dumpvars statement.