MAX 10 General Purpose I/O User Guide

UG-M10GPIO
2015.06.10

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Contents

MAX 10 I/O Overview

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The MAX® 10 general purpose I/O (GPIO) system consists of the I/O elements (IOE) and the Altera GPIO Lite IP core.

- The IOEs contain bidirectional I/O buffers and I/O registers located in I/O banks around the periphery of the device.
- The Altera GPIO Lite IP core supports the GPIO components and features, including double data rate I/O (DDIO), delay chains, I/O buffers, control signals, and clocking.

Related Information

- **MAX 10 I/O Architecture and Features** on page 2-1
  Provides information about the architecture and features of the I/Os in MAX 10 devices.
- **MAX 10 I/O Design Considerations** on page 3-1
  Provides I/O design guidelines for MAX 10 Devices.
- **MAX 10 I/O Implementation Guides** on page 4-1
  Provides guides to implement I/Os in MAX 10 Devices.
- **Altera GPIO Lite IP Core References** on page 5-1
  Lists the parameters and signals of Altera GPIO Lite IP core for MAX 10 Devices.

MAX 10 Devices I/O Resources Per Package

Table 1-1: Package Plan for MAX 10 Single Power Supply Devices—Preliminary

Device	Package			
	Type	M153 153-pin MBGA	U169 169-pin UBGA	E144 144-pin EQFP
	Size	8 mm × 8 mm	11 mm × 11 mm	22 mm × 22 mm
	Ball Pitch	0.5 mm	0.8 mm	0.5 mm
10M02		112	130	101
10M04		112	130	101
10M08		112	130	101
10M16		—	130	101

Device	Package			
	Type	M153 153-pin MBGA	U169 169-pin UBGA	E144 144-pin EQFP
	Size	8 mm × 8 mm	11 mm × 11 mm	22 mm × 22 mm
	Ball Pitch	0.5 mm	0.8 mm	0.5 mm
10M25		—	—	101
10M40		—	—	101
10M50		—	—	101

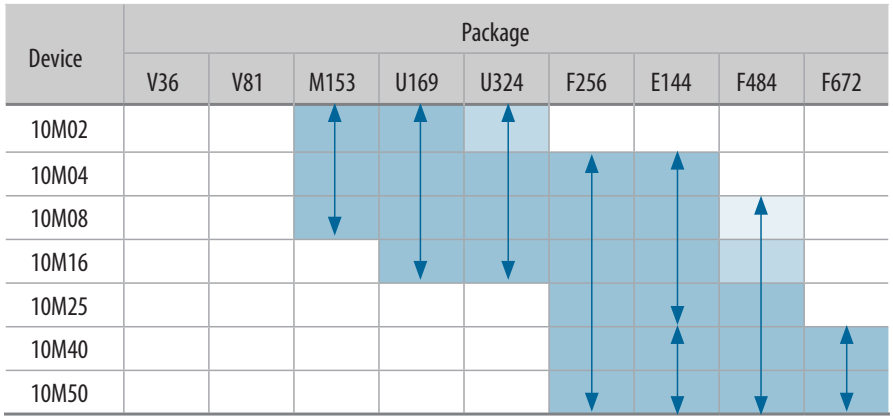
Table 1-2: Package Plan for MAX 10 Dual Power Supply Devices—Preliminary

Device	Package						
	Type	V36 36-pin WLCSP	V81 81-pin WLCSP	U324 324-pin UBGA	F256 256-pin FBGA	F484 484-pin FBGA	F672 672-pin FBGA
	Size	3 mm × 3 mm	4 mm × 4 mm	15 mm × 15 mm	17 mm × 17 mm	23 mm × 23 mm	27 mm × 27 mm
	Ball Pitch	0.4 mm	0.4 mm	0.8 mm	1.0 mm	1.0 mm	1.0 mm
10M02		27	—	160	—	—	—
10M04		—	—	246	178	—	—
10M08		—	56	246	178	250	—
10M16		—	—	246	178	320	—
10M25		—	—	—	178	360	—
10M40		—	—	—	178	360	500
10M50		—	—	—	178	360	500

MAX 10 I/O Vertical Migration Support

Figure 1-1: Migration Capability Across MAX 10 Devices—Preliminary

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Some packages have several migration paths. Devices with lesser I/O resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os usage to match the product line with the lowest I/O count.



Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus® II software Pin Planner.

Related Information

Verifying Pin Migration Compatibility on page 4-8

MAX 10 I/O Architecture and Features

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The I/O system of MAX 10 devices support various I/O standards. In the MAX 10 devices, the I/O pins are located in I/O banks at the periphery of the devices. The I/O pins and I/O buffers have several programmble features.

Related Information

MAX 10 I/O Overview on page 1-1

MAX 10 I/O Standards Support

MAX 10 devices support a wide range of I/O standards, including single-ended, voltage-referenced single-ended, and differential I/O standards.

Table 2-1: Supported I/O Standards in MAX 10 Devices

The voltage-referenced I/O standards are not supported in the following I/O banks of these device packages:

- All I/O banks of V36 package of 10M02.
- All I/O banks of V81 package of 10M08.
- Bank 1A and 1B of E144 package of 10M50.

I/O Standard	Type	Direction		Application	Standard Support
		Input	Output		
3.3 V LVTTL/3.3 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-B
3.0 V LVTTL/3.0 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-B
2.5 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-5
1.8 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-7
1.5 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-11

I/O Standard	Type	Direction		Application	Standard Support
		Input	Output		
1.2 V LVCMOS	Single-ended	Yes	Yes	General purpose	JESD8-12
3.0 V PCI	Single-ended	Yes	Yes	General purpose	PCI Rev. 2.2
3.3 V Schmitt Trigger	Single-ended	Yes	—	General purpose	—
2.5 V Schmitt Trigger	Single-ended	Yes	—	General purpose	—
1.8 V Schmitt Trigger	Single-ended	Yes	—	General purpose	—
1.5 V Schmitt Trigger	Single-ended	Yes	—	General purpose	—
SSTL-2 Class I	Voltage-referenced	Yes	Yes	DDR1	JESD8-9B
SSTL-2 Class II	Voltage-referenced	Yes	Yes	DDR1	JESD8-9B
SSTL-18 Class I	Voltage-referenced	Yes	Yes	DDR2	JESD8-15
SSTL-18 Class II	Voltage-referenced	Yes	Yes	DDR2	JESD8-15
SSTL-15 Class I	Voltage-referenced	Yes	Yes	DDR3	—
SSTL-15 Class II	Voltage-referenced	Yes	Yes	DDR3	—
SSTL-15(1)	Voltage-referenced	Yes	Yes	DDR3	JESD79-3D
SSTL-135(1)	Voltage-referenced	Yes	Yes	DDR3L	—
1.8 V HSTL Class I	Voltage-referenced	Yes	Yes	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
1.8 V HSTL Class II	Voltage-referenced	Yes	Yes	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
1.5 V HSTL Class I	Voltage-referenced	Yes	Yes	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6

(1) Available in MAX 10 16, 25, 40, and 50 devices only.

I/O Standard	Type	Direction		Application	Standard Support
		Input	Output		
1.5 V HSTL Class II	Voltage-referenced	Yes	Yes	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
1.2 V HSTL Class I	Voltage-referenced	Yes	Yes	General purpose	JESD8-16A
1.2 V HSTL Class II	Voltage-referenced	Yes	Yes	General purpose	JESD8-16A
HSUL-12(1)	Voltage-referenced	Yes	Yes	LPDDR2	—
Differential SSTL-2 Class I and II	Differential	Yes(2)	Yes(3)	DDR1	JESD8-9B
Differential SSTL-18 Class I and Class II	Differential	Yes(2)	Yes(3)	DDR2	JESD8-15
Differential SSTL-15 Class I and Class II	Differential	Yes(2)	Yes(3)	DDR3	—
Differential SSTL-15	Differential	Yes(2)	Yes(3)	DDR3	JESD79-3D
Differential SSTL-135	Differential	Yes(2)	Yes(3)	DDR3L	—
Differential 1.8 V HSTL Class I and Class II	Differential	Yes(2)	Yes(3)	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
Differential 1.5 V HSTL Class I and Class II	Differential	Yes(2)	Yes(3)	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
Differential 1.2 V HSTL Class I and Class II	Differential	Yes(2)	Yes(3)	General purpose	JESD8-16A
Differential HSUL-12	Differential	Yes(2)	Yes(3)	LPDDR2	—
LVDS (dedicated)(4)	Differential	Yes	Yes	—	ANSI/TIA/EIA-644
LVDS (external resistor)	Differential	—	Yes	—	ANSI/TIA/EIA-644
Mini-LVDS (dedicated)(4)	Differential	—	Yes	—	—

(2) The inputs treat differential inputs as two single-ended inputs and decode only one of them.
(3) The outputs use two single-ended output buffers with the second output buffer programmed as inverted.
(4) You can use dedicated LVDS transmitters only on the bottom I/O banks. You can use LVDS receivers on all I/O banks.

I/O Standard	Type	Direction		Application	Standard Support
		Input	Output		
Mini-LVDS (external resistor)	Differential	—	Yes	—	—
RSDS (dedicated)(4)	Differential	—	Yes	—	—
RSDS (external resistor, 1R)	Differential	—	Yes	—	—
RSDS (external resistor, 3R)	Differential	—	Yes	—	—
PPDS (dedicated)(4)	Differential	—	Yes	—	—
PPDS (external resistor)	Differential	—	Yes	—	—
LVPECL	Differential	Yes	—	—	—
Bus LVDS	Differential	Yes	Yes(5)	—	—
TMDS	Differential	Yes	—	—	—
Sub-LVDS	Differential	Yes	Yes(6)	—	—
SLVS	Differential	Yes	Yes(7)	—	—
HiSpi	Differential	Yes	—	—	—

Related Information

- **MAX 10 I/O Buffers** on page 2-11
  Provides more information about available I/O buffer types and supported I/O standards.
- **LVDS Transmitter I/O Termination Schemes, MAX 10 High-Speed LVDS I/O User Guide**

MAX 10 I/O Standards Voltage and Pin Support

Table 2-2: MAX 10 I/O Standards Voltage Levels and Pin Support

I/O Standard	V_{CCIO} (V)		V_{REF} (V)	Pin Type Support				
	Input	Output		PLL_CLKOUT	MEM_CLK	CLK	DQS	User I/O
3.3 V LVTTL/ 3.3 V LVCMOS	3.3/3.0/ 2.5	3.3	—	Yes	Yes	Yes	Yes	Yes

(5) The outputs use two single-ended output buffers with the second output buffer programmed as inverted. A single series resistor is required.
(6) Requires external termination resistors.
(7) The outputs uses two single-ended output buffers as emulated differential outputs. Requires external termination resistors.

I/O Standard	V_{CCIO} (V)		V_{REF} (V)	Pin Type Support				
	Input	Output		PLL_CLKOUT	MEM_CLK	CLK	DQS	User I/O
3.0 V LVTTL/ 3.0 V LVCMOS	3.0/2.5	3.0	—	Yes	Yes	Yes	Yes	Yes
2.5 V LVCMOS	3.0/2.5	2.5	—	Yes	Yes	Yes	Yes	Yes
1.8 V LVCMOS	1.8/1.5	1.8	—	Yes	Yes	Yes	Yes	Yes
1.5 V LVCMOS	1.8/1.5	1.5	—	Yes	Yes	Yes	Yes	Yes
1.2 V LVCMOS	1.2	1.2	—	Yes	Yes	Yes	Yes	Yes
3.0 V PCI	3.0	3.0	—	Yes	Yes	Yes	Yes	Yes
3.3 V Schmitt Trigger	3.3	—	—	—	—	Yes	Yes[8]	Yes
2.5 V Schmitt Trigger	2.5	—	—	—	—	Yes	Yes[8]	Yes
1.8 V Schmitt Trigger	1.8	—	—	—	—	Yes	Yes[8]	Yes
1.5 V Schmitt Trigger	1.5	—	—	—	—	Yes	Yes[8]	Yes
SSTL-2 Class I	2.5	2.5	1.25	Yes	Yes	Yes	Yes	Yes
SSTL-2 Class II	2.5	2.5	1.25	Yes	Yes	Yes	Yes	Yes
SSTL-18 Class I	1.8	1.8	0.9	Yes	Yes	Yes	Yes	Yes
SSTL-18 Class II	1.8	1.8	0.9	Yes	Yes	Yes	Yes	Yes
SSTL-15 Class I	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
SSTL-15 Class II	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
SSTL-15	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
SSTL-135	1.35	1.35	0.675	Yes	Yes	Yes	Yes	Yes
1.8 V HSTL Class I	1.8	1.8	0.9	Yes	Yes	Yes	Yes	Yes
1.8 V HSTL Class II	1.8	1.8	0.9	Yes	Yes	Yes	Yes	Yes
1.5 V HSTL Class I	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
1.5 V HSTL Class II	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes

(8) Bidirectional— use Schmitt Trigger input with LVTTL output.

I/O Standard	V_{CCIO} (V)		V_{REF} (V)	Pin Type Support				
	Input	Output		PLL_CLKOUT	MEM_CLK	CLK	DQS	User I/O
1.2 V HSTL Class I	1.2	1.2	0.6	Yes	Yes	Yes	Yes	Yes
1.2 V HSTL Class II	1.2	1.2	0.6	Yes	Yes	Yes	Yes	Yes
HSUL-12	1.2	1.2	0.6	Yes	Yes	Yes	Yes	Yes
Differential SSTL-2 Class I and II	—	2.5	—	Yes	Yes	—	Yes	—
	2.5	—	1.25	—	—	Yes	Yes	—
Differential SSTL-18 Class I and Class II	—	1.8	—	Yes	Yes	—	Yes	—
	1.8	—	0.9	—	—	Yes	Yes	—
Differential SSTL-15 Class I and Class II	—	1.5	—	Yes	Yes	—	Yes	—
	1.5	—	0.75	—	—	Yes	Yes	—
Differential SSTL-15	—	1.5	—	Yes	Yes	—	Yes	—
	1.5	—	0.75	—	—	Yes	Yes	—
Differential SSTL-135	—	1.35	—	Yes	Yes	—	Yes	—
	1.35	—	0.675	—	—	Yes	Yes	—
Differential 1.8 V HSTL Class I and Class II	—	1.8	—	Yes	Yes	—	Yes	—
	1.8	—	0.9	—	—	Yes	Yes	—
Differential 1.5 V HSTL Class I and Class II	—	1.5	—	Yes	Yes	—	Yes	—
	1.5	—	0.75	—	—	Yes	Yes	—
Differential 1.2 V HSTL Class I and Class II	—	1.2	—	Yes	Yes	—	Yes	—
	1.2	—	0.6	—	—	Yes	Yes	—
Differential HSUL-12	—	1.2	—	Yes	Yes	—	Yes	—
	1.2	—	0.6	—	—	Yes	Yes	—
LVDS (dedicated)	2.5	2.5	—	Yes	Yes	Yes	—	Yes
LVDS (external resistor)	—	2.5	—	Yes	Yes	—	—	Yes
Mini-LVDS (dedicated)	—	2.5	—	Yes	Yes	—	—	Yes
Mini-LVDS (external resistor)	—	2.5	—	Yes	Yes	—	—	Yes

I/O Standard	V_{CCIO} (V)		V_{REF} (V)	Pin Type Support				
	Input	Output		PLL_CLKOUT	MEM_CLK	CLK	DQS	User I/O
RSDS (dedicated)	—	2.5	—	Yes	Yes	—	—	Yes
RSDS (external resistor, 1R)	—	2.5	—	Yes	Yes	—	—	Yes
RSDS (external resistor, 3R)	—	2.5	—	Yes	Yes	—	—	Yes
PPDS (dedicated)	—	2.5	—	Yes	Yes	—	—	Yes
PPDS (external resistor)	—	2.5	—	Yes	Yes	—	—	Yes
LVPECL	2.5	—	—	—	—	Yes	—	—
Bus LVDS	2.5	2.5	—	—	—	—	—	Yes
TMDS	2.5	—	—	—	—	Yes	—	Yes
Sub-LVDS	2.5	1.8	—	Yes	Yes	Yes	—	Yes
SLVS	2.5	2.5	—	Yes	Yes	Yes	—	Yes
HiSpi	2.5	—	—	—	—	Yes	—	Yes

MAX 10 I/O Elements

The MAX 10 I/O elements (IOEs) contain a bidirectional I/O buffer and five registers for registering input, output, output-enable signals, and complete embedded bidirectional single data rate (SDR) and double data rate (DDR) transfer.

The I/O buffers are grouped into groups of four I/O modules per I/O bank:

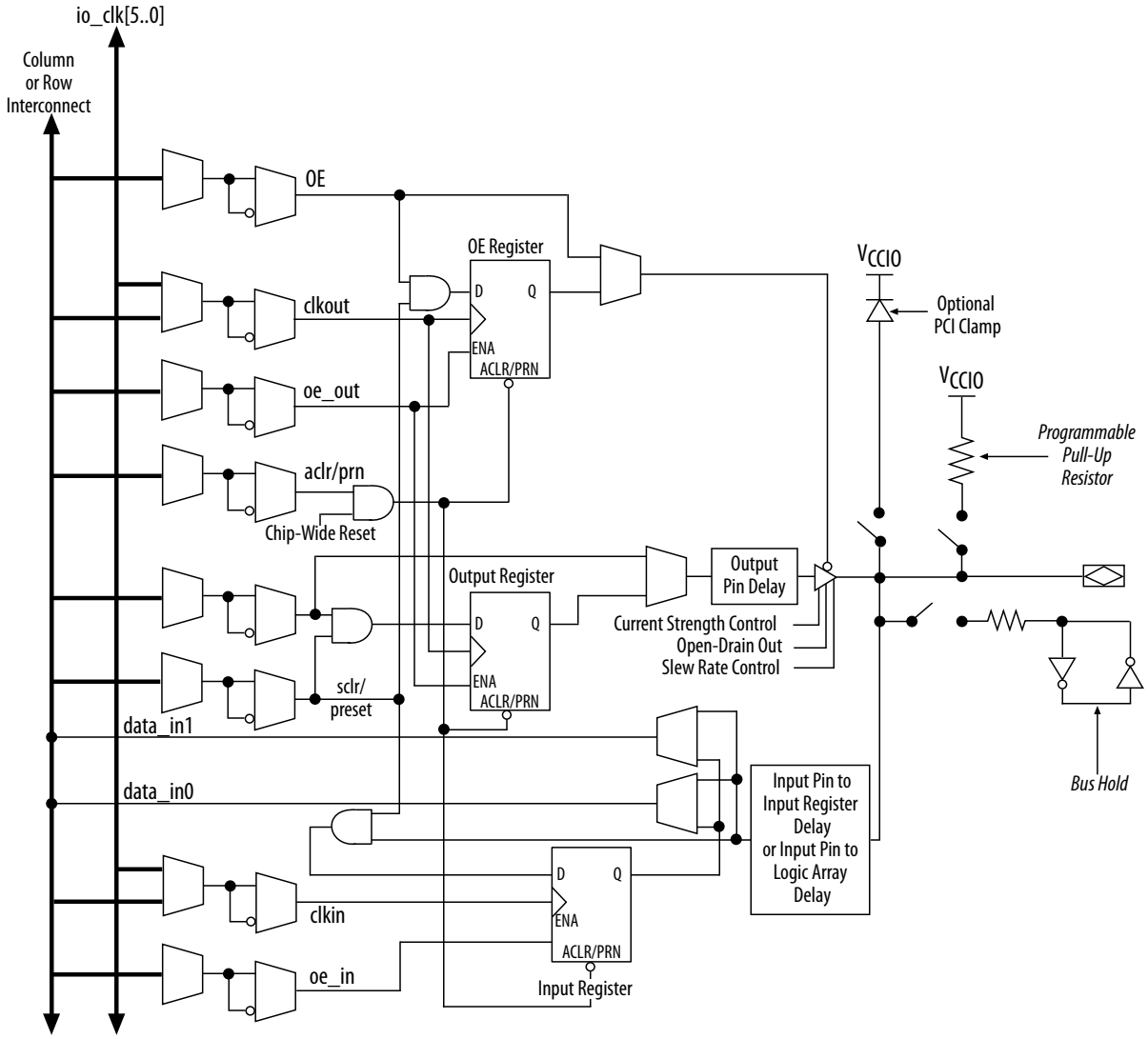
- The MAX 10 devices share the user I/O pins with the VREF, RUP, RDN, CLKPIN, PLLCLKOUT, configuration, and test pins.
- Schmitt Trigger input buffer is available in all I/O buffers.

Each IOE contains one input register, two output registers, and two output-enable (OE) registers:

- The two output registers and two OE registers are used for DDR applications.
- You can use the input registers for fast setup times and output registers for fast clock-to-output times.
- You can use the OE registers for fast clock-to-output enable times.

You can use the IOEs for input, output, or bidirectional data paths. The I/O pins support various single-ended and differential I/O standards.

Figure 2-1: IOE Structure in Bidirectional Configuration



Related Information

MAX 10 Power Management User Guide

Provides more information about the I/O buffers in different power cycles and hot socketing.

MAX 10 I/O Banks Architecture

The I/O elements are located in a group of four modules per I/O bank:

- High speed DDR3 I/O banks—supports various I/O standards and protocols including DDR3. These I/O banks are available only on the right side of the device.
- High speed I/O banks—supports various I/O standards and protocols except DDR3. These I/O banks are available on the top, left, and bottom sides of the device.
- Low speed I/O banks—lower speeds I/O banks that are located at the top left side of the device.

For more information about I/O pins support, refer to the pinout files for your device.

Related Information

MAX 10 Device Pin-Out Files

MAX 10 I/O Banks Locations

The I/O banks are located at the periphery of the device.

For more details about the modular I/O banks available in each device package, refer to the relevant device pin-out file.

Figure 2-2: I/O Banks for MAX 10 02 Devices—Preliminary

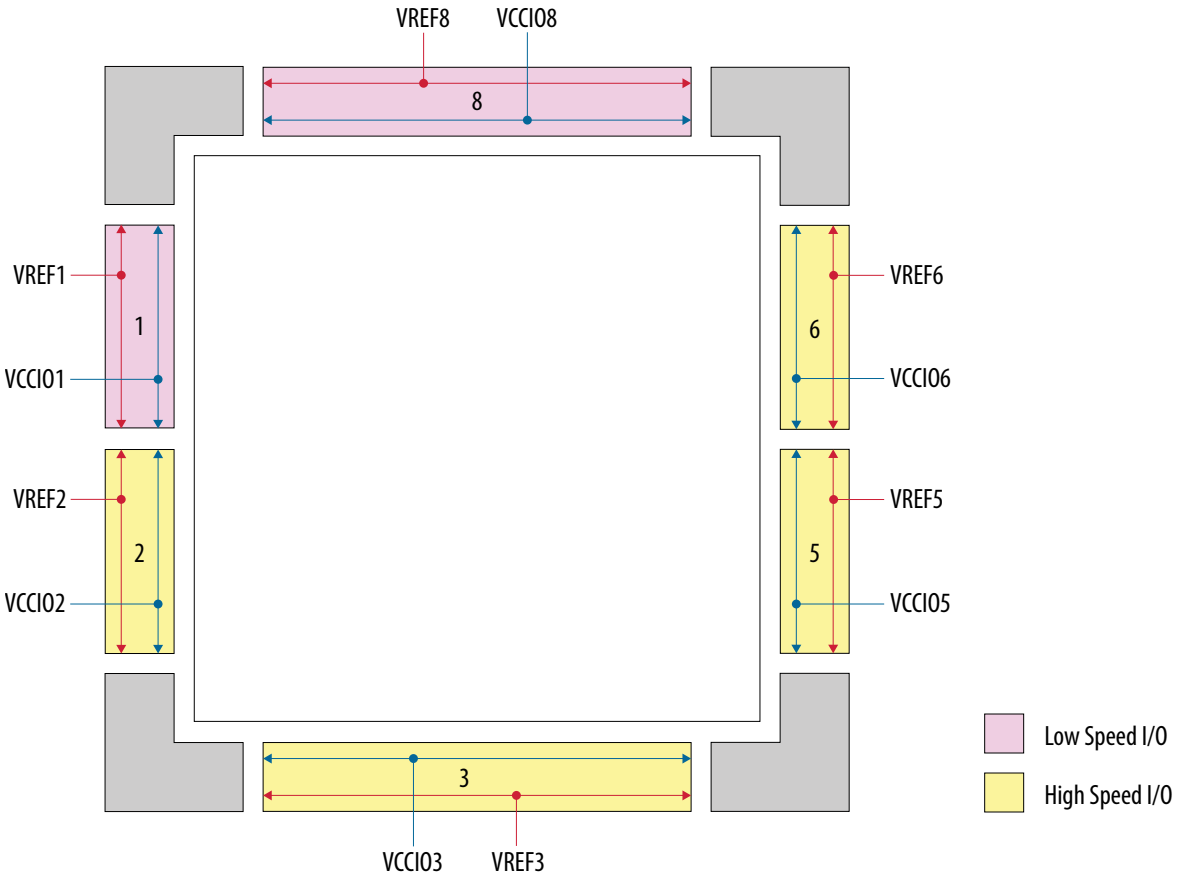


Figure 2-3: I/O Banks for MAX 10 04 and 08 Devices—Preliminary

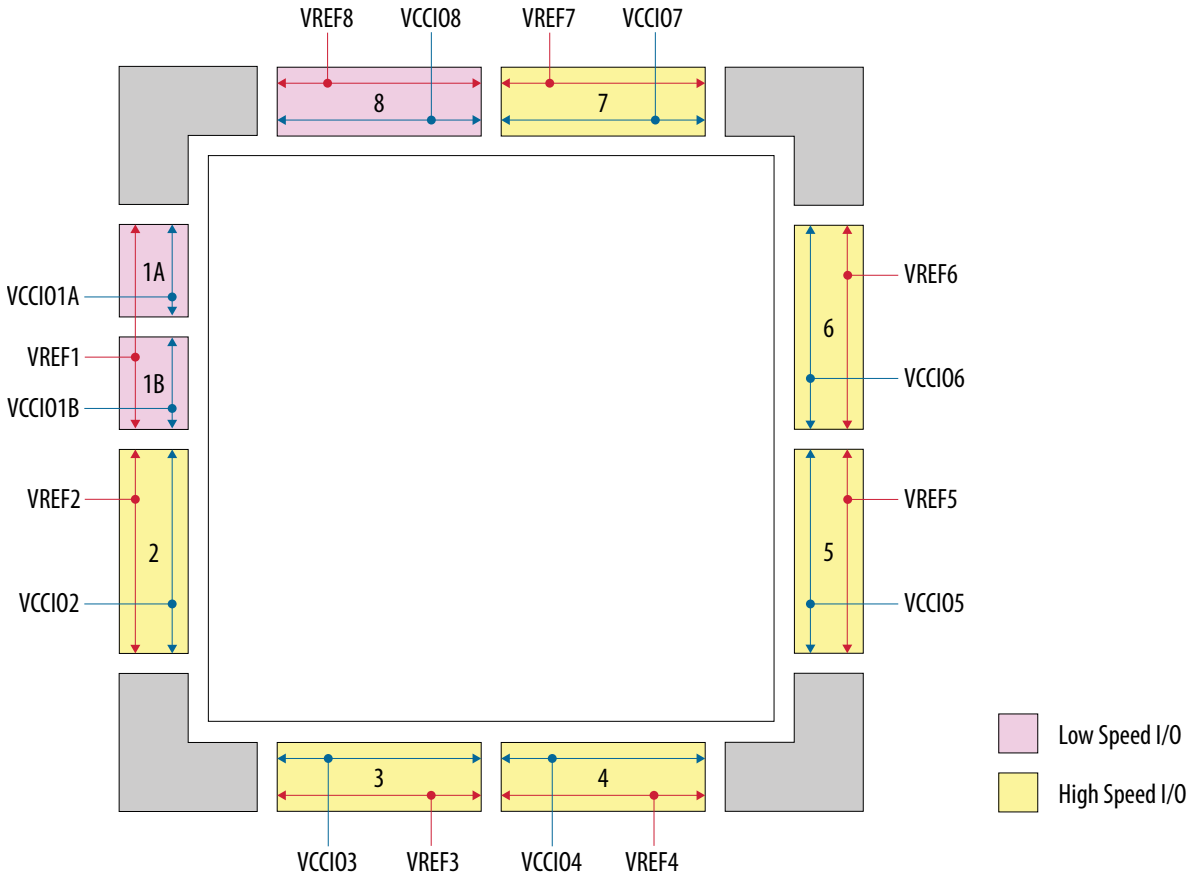
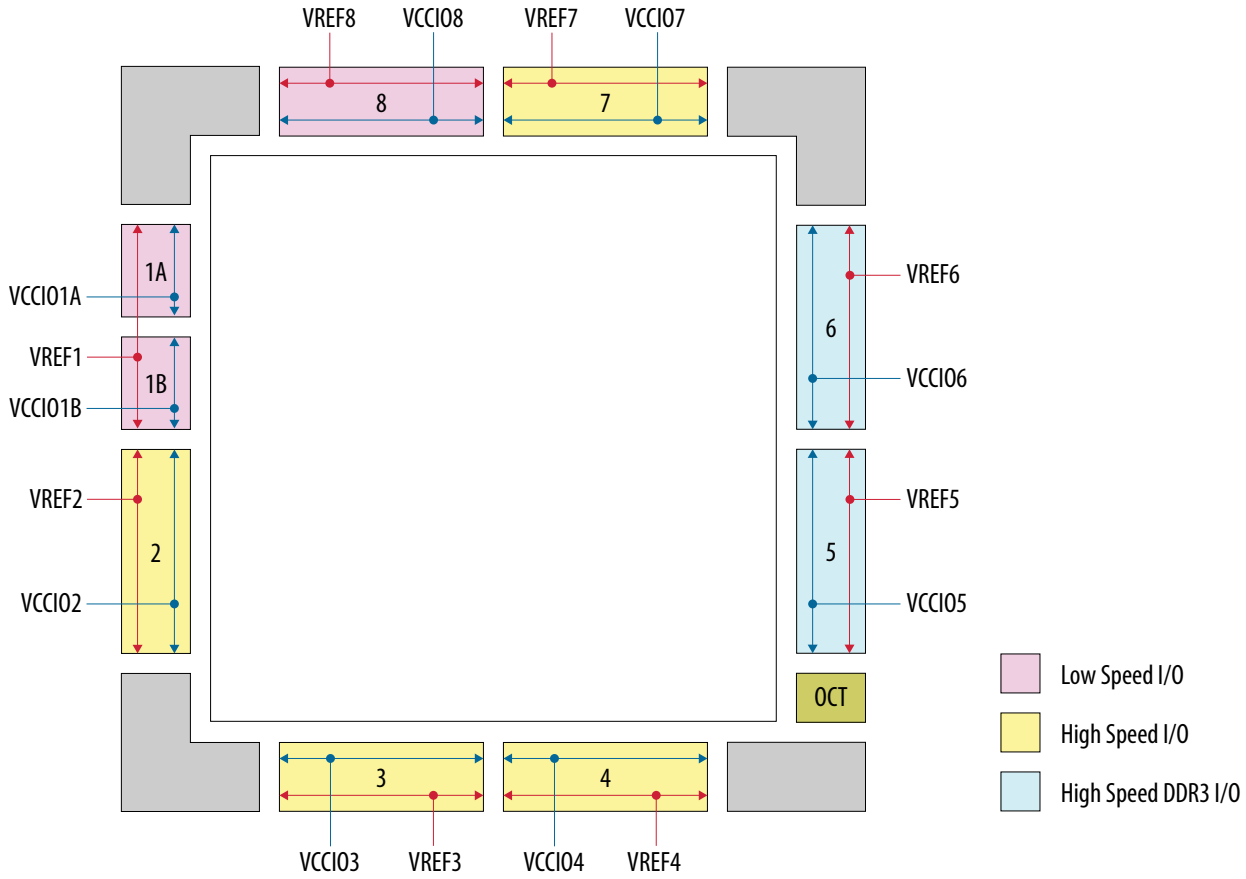


Figure 2-4: I/O Banks for MAX 10 16, 25, 40, and 50 Devices—Preliminary



Related Information

MAX 10 Device Pin-Out Files

MAX 10 I/O Buffers

The general purpose I/Os (GPIOs) in MAX 10 devices consist of LVDS I/O and DDR I/O buffers.

Table 2-3: Types of GPIO Buffers in MAX 10 Devices

LVDS I/O Buffers	DDR I/O Buffers
• Support differential and single-ended I/O standards. • Available only on I/O banks at the bottom side of the device. • For LVDS, the bottom I/O banks support LVDS transmitter, emulated LVDS transmitter, and LVDS receiver buffers.	• Support differential and single-ended I/O standards. • Available on I/O banks at the left, right, and top sides of the device. • For LVDS, the DDR I/O buffers support only LVDS receiver and emulated LVDS transmitter buffers. • For DDR, only the DDR I/O buffers on the right side of the device supports DDR3 external memory interfaces. DDR3 support is only available for MAX 10 16, 25, 40, and 50 devices.

Related Information

- **MAX 10 I/O Standards Support** on page 2-1
- **LVDS Transmitter I/O Termination Schemes, MAX 10 High-Speed LVDS I/O User Guide**

Schmitt-Trigger Input Buffer

The MAX 10 devices feature selectable Schmitt trigger input buffer on all I/O banks.

The Schmitt trigger input buffer has similar V_{IL} and V_{IH} as the LVTTL I/O standard but with better noise immunity. The Schmitt trigger input buffers are the used as default input buffers during configuration mode.

Related Information

MAX 10 Device Datasheet

Programmable I/O Buffer Features

The MAX 10 I/O buffers support a range of programmable features. These features increase the flexibility of I/O utilization and provide an alternative to reduce the usage of external discrete components such as a pull-up resistor and a diode.

Programmable Open Drain

The optional open-drain output for each I/O pin is equivalent to an open collector output. If it is configured as an open drain, the logic value of the output is either high-Z or logic low.

Use an external resistor to pull the signal to a logic high.

Programmable Bus Hold

Each I/O pin provides an optional bus-hold feature that is active only after configuration. When the device enters user mode, the bus-hold circuit captures the value that is present on the pin by the end of the configuration.

The bus-hold circuitry holds this pin state until the next input signal is present. Because of this, you do not require an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

For each I/O pin, you can individually specify that the bus-hold circuitry pulls non-driven pins away from the input threshold voltage—where noise can cause unintended high-frequency switching. To prevent over-driving signals, the bus-hold circuitry drives the voltage level of the I/O pin lower than the V_{CCIO} level.

If you enable the bus-hold feature, you cannot use the programmable pull-up option. To configure the I/O pin for differential signals, disable the bus-hold feature.

Programmable Pull-Up Resistor

Each I/O pin provides an optional programmable pull-up resistor during user mode. The pull-up resistor, typically 25 kΩ, weakly holds the I/O to the V_{CCIO} level.

If you enable the weak pull-up resistor, you cannot use the bus-hold feature.

Programmable Current Strength

You can use the programmable current strength to mitigate the effects of high signal attenuation that is caused by a long transmission line or a legacy backplane.

Table 2-4: Programmable Current Strength Settings for MAX 10 Devices

The output buffer for each MAX 10 device I/O pin has a programmable current strength control for the I/O standards listed in this table.

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) (Default setting in bold)
3.3 V LVCMOS	**2**
3.3 V LVTTL	**8**, 4
3.0 V LVTTL/3.0 V LVCMOS	16, **12**, 8, 4
2.5 V LVTTL/2.5 V LVCMOS	16, **12**, 8, 4
1.8 V LVTTL/1.8 V LVCMOS	16, **12**, 10, 8, 6, 4, 2
1.5 V LVCMOS	16, **12**, 10, 8, 6, 4, 2
1.2 V LVCMOS	12, 10, **8**, 6, 4, 2
SSTL-2 Class I	12, **8**
SSTL-2 Class II	**16**
SSTL-18 Class I	12, 10, **8**
SSTL-18 Class II	**16**, 12
SSTL-15 Class I	12, 10, **8**
SSTL-15 Class II	**16**
1.8 V HSTL Class I	12, 10, **8**
1.8 V HSTL Class II	**16**
1.5 V HSTL Class I	12, 10, **8**
1.5 V HSTL Class II	**16**
1.2 V HSTL Class I	12, 10, **8**

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) (Default setting in bold)
1.2 V HSTL Class II	**14**
BLVDS	**16**, 12, 8
SLVS	**16**, 12, 8
Sub-LVDS	**12**, 8, 4

Note: Altera recommends that you perform IBIS or SPICE simulations to determine the best current strength setting for your specific application.

Programmable Output Slew Rate Control

You have the option of three settings for programmable slew rate control—0, 1, and 2 with 2 as the default setting. Setting 0 is the slow slew rate and 2 is the fast slew rate.

- Fast slew rate—provides high-speed transitions for high-performance systems.
- Slow slew rate—reduces system noise and crosstalk but adds a nominal delay to the rising and falling edges.

Table 2-5: Programmable Output Slew Rate Control for MAX 10 Devices

This table lists the single-ended I/O standards and current strength settings that support programmable output slew rate control. For I/O standards and current strength settings that do not support programmable slew rate control, the default slew rate setting is 2 (fast slew rate).

I/O Standard	I_{OH} / I_{OL} Current Strength Supporting Slew Rate Control
3.0 V LVTTL/3.0 V LVCMOS	16, 12, 8
2.5 V LVTTL/2.5 V LVCMOS	16, 12, 8
1.8 V LVTTL/1.8 V LVCMOS	16, 12, 8
1.5 V LVCMOS	16, 12, 10, 8
1.2 V LVCMOS	12, 10, 8
SSTL-2 Class I	12, 8
SSTL-2 Class II	16
SSTL-18 Class I	12, 10, 8
SSTL-18 Class II	16, 12
SSTL-15 Class I	12, 10, 8
SSTL-15 Class II	16
1.8 V HSTL Class I	12, 10, 8
1.8 V HSTL Class II	16
1.5 V HSTL Class I	12, 10, 8
1.5 V HSTL Class II	16

I/O Standard	I_{OH} / I_{OL} Current Strength Supporting Slew Rate Control
1.2 V HSTL Class I	12, 10, 8
1.2 V HSTL Class II	14

You can specify the slew rate on a pin-by-pin basis because each I/O pin contains a slew rate control. The slew rate control affects both the rising and falling edges.

Note: Altera recommends that you perform IBIS or SPICE simulations to determine the best slew rate setting for your specific application.

Programmable IOE Delay

You can activate the programmable IOE delays to ensure zero hold times, minimize setup times, increase clock-to-output times, or delay the clock input signal. This feature helps read and write timing margins because it minimizes the uncertainties between signals in the bus.

Each pin can have a different input delay from pin-to-input register or a delay from output register-to-output pin values to ensure that the signals within a bus have the same delay going into or out of the device.

Table 2-6: Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin-to-logic array delay	Input delay from pin to internal cells
Input pin-to-input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Dual-purpose clock input pin delay	Input delay from dual-purpose clock pin to fan-out destinations

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to the internal logic element (LE) registers that reside in two different areas of the device. You must set the two combinational input delays with the input delay from pin to internal cells logic option in the Quartus II software for each path. If the pin uses the input register, one of the delays is disregarded and the delay is set with the input delay from pin to input register logic option in the Quartus II software.

The IOE registers in each I/O block share the same source for the preset or clear features. You can program preset or clear for each individual IOE, but you cannot use both features simultaneously. You can also program the registers to power-up high or low after configuration is complete. If programmed to power-up low, an asynchronous clear can control the registers. If programmed to power-up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of the active-low input of another device upon power up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Related Information

- **MAX 10 Device Datasheet**

- **Timing Closure and Optimization chapter, Volume 2: Design Implementation and Optimization, Quartus II Handbook**
  Provides more information about the input and output pin delay settings.

PCI Clamp Diode

The MAX 10 devices are equipped with optional PCI clamp diode that you can enable for the input and output of each I/O pin.

The PCI clamp diode is available and enabled by default in the Quartus II software for the following I/O standards:

- 3.3 V LVTTL/3.3 V LVCMOS
- 3.0 V LVTTL/3.0 V LVCMOS
- 3.0 V PCI

Programmable Pre-Emphasis

The differential output voltage (V_{OD}) setting and the output impedance of the driver set the output current limit of a high-speed transmission signal. At a high frequency, the slew rate may not be fast enough to reach the full V_{OD} level before the next edge, producing pattern-dependent jitter. Pre-emphasis momentarily boosts the output current during switching to increase the output slew rate.

Pre-emphasis increases the amplitude of the high-frequency component of the output signal. This increase compensates for the frequency-dependent attenuation along the transmission line.

The overshoot introduced by the extra current occurs only during change of state switching. This overshoot increases the output slew rate but does not ring, unlike the overshoot caused by signal reflection. The amount of pre-emphasis required depends on the attenuation of the high-frequency component along the transmission line.

Figure 2-5: LVDS Output with Programmable Pre-Emphasis

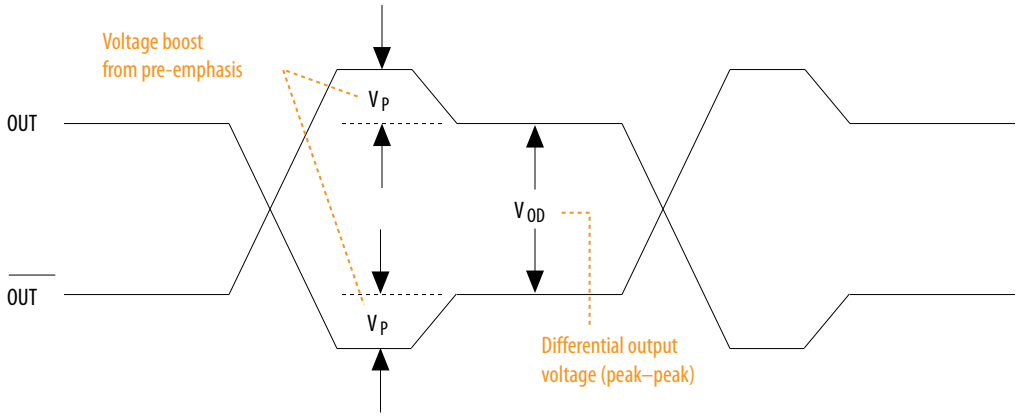


Table 2-7: Quartus II Software Assignment for Programmable Pre-Emphasis

Field	Assignment
To	tx_out
Assignment name	Programmable Pre-emphasis

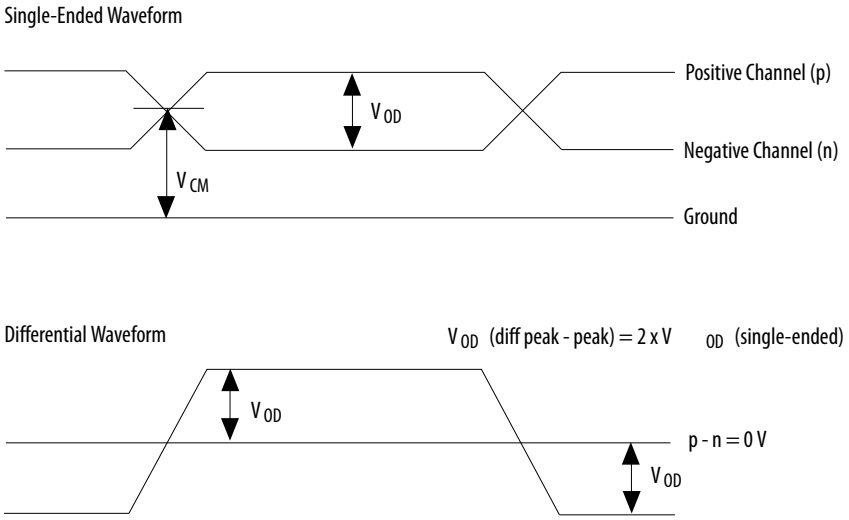
Field	Assignment
Allowed values	0 (disabled), 1 (enabled). Default is 1.

Programmable Differential Output Voltage

The programmable V_{OD} settings allow you to adjust the output eye opening to optimize the trace length and power consumption. A higher V_{OD} swing improves voltage margins at the receiver end, and a smaller V_{OD} swing reduces power consumption.

Figure 2-6: Differential V_{OD}

This figure shows the V_{OD} of the differential LVDS output.



You can statically adjust the V_{OD} of the differential signal by changing the V_{OD} settings in the Quartus II software Assignment Editor.

Table 2-8: Quartus II Software Assignment Editor—Programmable V_{OD}

Field	Assignment
To	`tx_out`
Assignment name	Programmable Differential Output Voltage (V_{OD})
Allowed values	0 (low), 1 (medium), 2 (high). Default is 2.

Programmable Emulated Differential Output

The MAX 10 devices support emulated differential output where a pair of IOEs drives bidirectional I/O pins.

The emulated differential output feature is supported for the following I/O standards:

- Differential SSTL-2 Class I and II
- Differential SSTL-18 Class I and II
- Differential SSTL-15 Class I and II
- Differential SSTL-15

- Differential SSTL-135
- Differential 1.8 V HSTL Class I and II
- Differential 1.5 V HSTL Class I and II
- Differential 1.2 V HSTL Class I and II
- Differential HSUL-12
- LVDS 3R
- Mini-LVDS 3R
- PPDS 3R
- RSDS 1R and 3R
- BLVDS
- SLVS
- Sub-LVDS

Programmable Dynamic Power Down

The MAX 10 16, 25, 40, and 50 devices feature programmable dynamic power down for several I/O standards to reduce the static power consumption.

In these devices, you can apply the programmable dynamic power down feature to the I/O buffers for the following I/O standards:

- Input buffer—SSTL, HSTL, HSUL, LVDS
- Output buffer—LVDS

Related Information

MAX 10 Power Management User Guide
Provides more information about using the programmable dynamic power down feature.Provides more information about the programmable output delay specifications.

I/O Standards Termination

Voltage-referenced and differential I/O standards requires different termination schemes.

The 3.3-V LVTTL, 3.0-V LVTTL and LVCMOS, 2.5-V LVTTL and LVCMOS, 1.8-V LVTTL and LVCMOS, 1.5-V LVCMOS, 1.2-V LVCMOS, and 3.0-V PCI I/O standards do not specify a recommended termination scheme per the JEDEC standard.

Voltage-Referenced I/O Standards Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

Figure 2-7: HSTL I/O Standard Termination

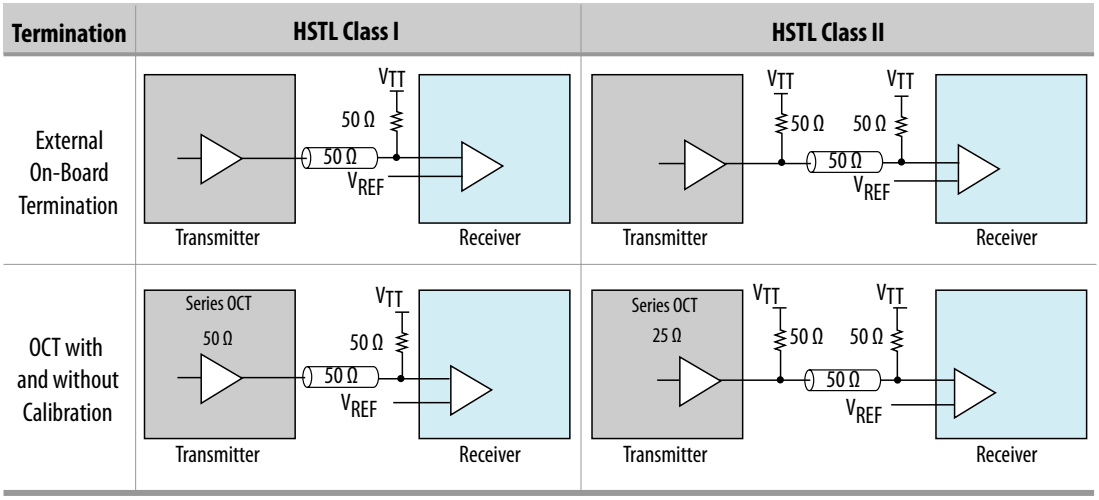
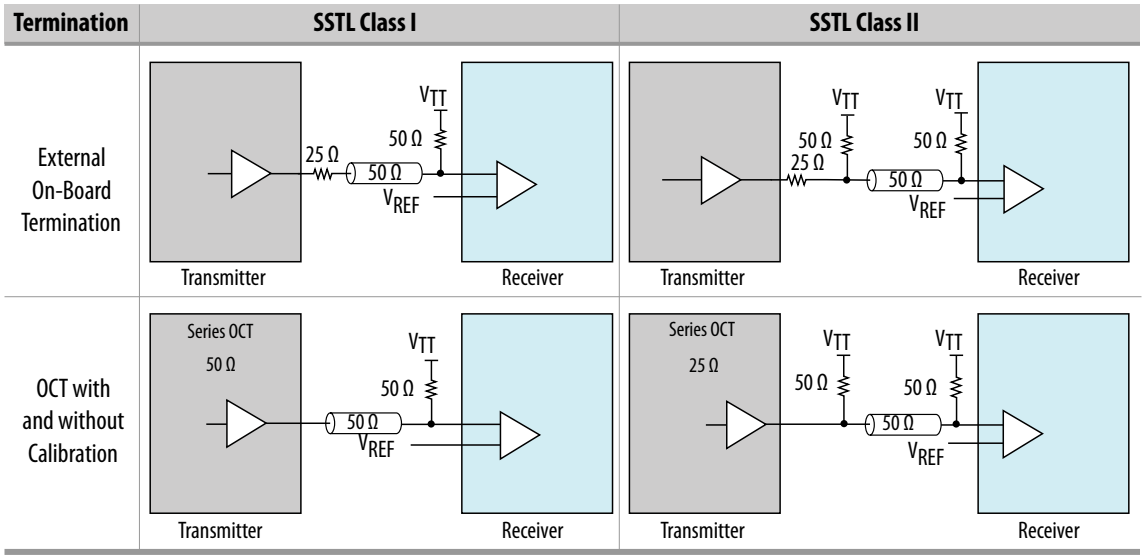


Figure 2-8: SSTL I/O Standard Termination



Differential I/O Standards Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus.

Figure 2-9: Differential HSTL I/O Standard Termination

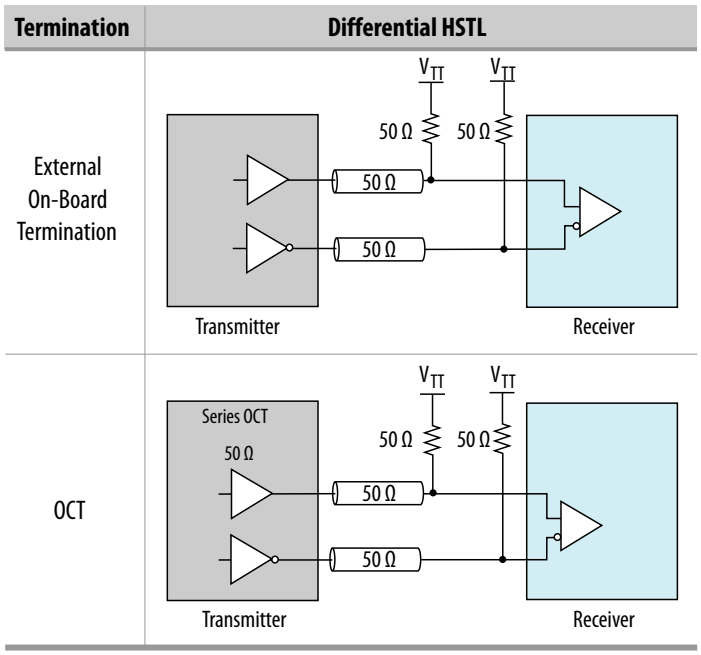
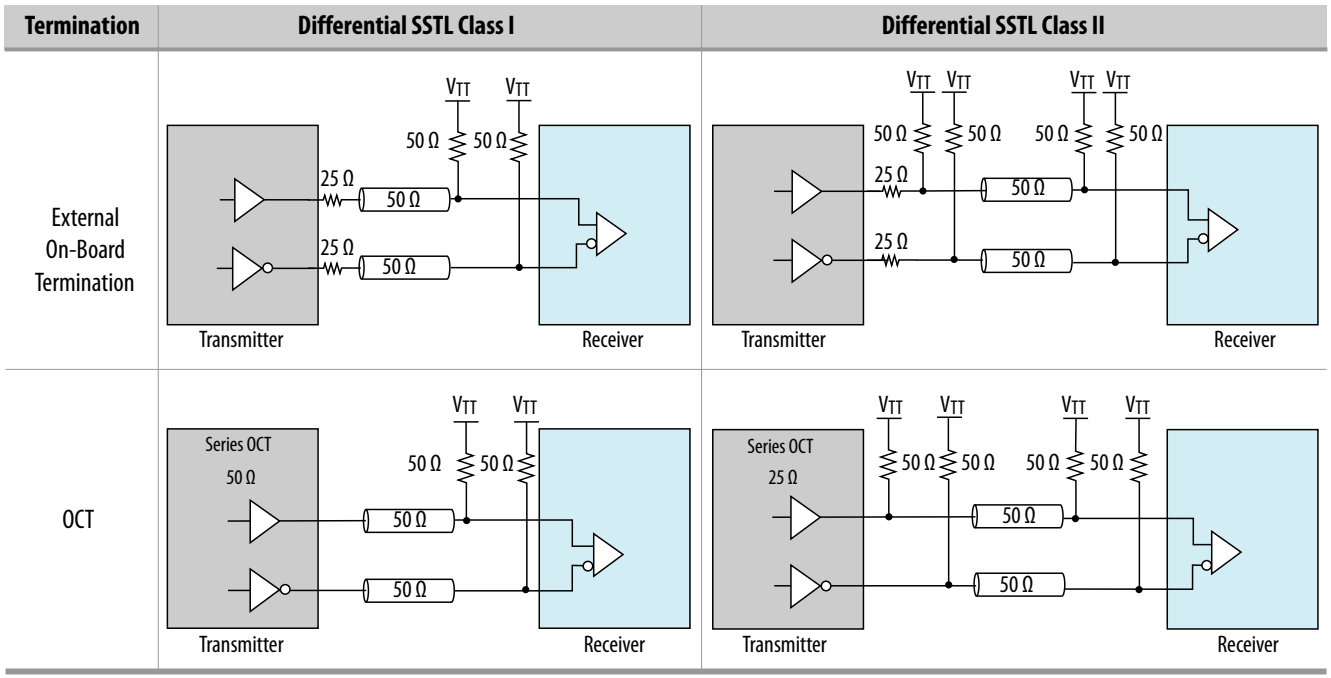


Figure 2-10: Differential SSTL I/O Standard Termination



Related Information

MAX 10 High-Speed LVDS I/O User Guide

Provides more information about differential I/O external termination.

MAX 10 On-Chip I/O Termination

The on-chip termination (OCT) block in MAX 10 devices provides I/O impedance matching and termination capabilities. OCT maintains signal quality, saves board space, and reduces external component costs.

The MAX 10 devices support serial (R_S) OCT for single-ended output pins and bidirectional pins. For bidirectional pins, OCT is active for output only.

Figure 2-11: Single-ended I/O Termination (R_S)

This figure shows the single-ended termination scheme supported in MAX 10 device.

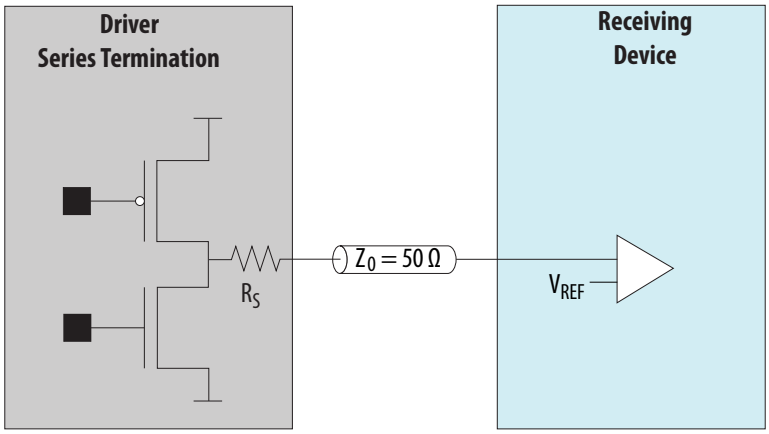


Table 2-9: OCT Schemes Supported in MAX 10 Devices

Direction	OCT Schemes	Device Support	I/O Bank Support
Output	R_S OCT with calibration	MAX 10 16, 25, 40, and 50 devices	Right bank only
	R_S OCT without calibration	All MAX 10 devices	All I/O banks

OCT Calibration

The OCT calibration circuit compares the total impedance of the output buffer to the external resistors connected to the RUP and RDN pins. The circuit dynamically adjusts the output buffer impedance until it matches the external resisters.

Each calibration block comes with a pair of RUP and RDN pins.

During calibration, the RUP and RDN pins are each connected through an external 25 Ω, 34 Ω, 40 Ω, 48 Ω, or 50 Ω resistor for respective on-chip series termination value of 25 Ω, 34 Ω, 40 Ω, 48 Ω, and 50 Ω:

- RUP—connected to VCCIO.
- RDN—connected to GND.

The OCT calibration circuit compares the external resistors to the internal resistance using comparators. The OCT calibration block uses the comparators' output to dynamically adjust buffer impedance.

During calibration, the resistance of the RUP and RDN pins varies. To estimate of the maximum possible current through the external calibration resistors, assume a minimum resistance of 0 Ω on the RUP and RDN pins.

R_S OCT in MAX 10 Devices

Table 2-10: Selectable I/O Standards for R_S OCT

This table lists the output termination settings for R_S OCT with and without calibration on different I/O standards.

- R_S OCT with calibration—supported only on the right side I/O banks of the MAX 10 16, 25, 40, and 50 devices.
- R_S OCT without calibration—supported on all I/O banks of all MAX 10 devices.

I/O Standard	Calibrated OCT (Output)	Uncalibrated OCT (Output)
	R_S (Ω)	R_S (Ω)
3.0 V LVTTL/3.0V LVCMOS	25, 50	25, 50
2.5 V LVTTL/2.5 V LVCMOS	25, 50	25, 50
1.8 V LVTTL/1.8 V LVCMOS	25, 50	25, 50
1.5 V LVCMOS	25, 50	25, 50
1.2 V LVCMOS	25, 50	25, 50
SSTL-2 Class I	50	50
SSTL-2 Class II	25	25
SSTL-18 Class I	50	50
SSTL-18 Class II	25	25
SSTL-15 Class I	50	50
SSTL-15 Class II	25	25
SSTL-15	34, 40	34, 40
SSTL-135	34, 40	34, 40
1.8 V HSTL Class I	50	50
1.8 V HSTL Class II	25	25
1.5 V HSTL Class I	50	50
1.5 V HSTL Class II	25	25
1.2 V HSTL Class I	50	50
1.2 V HSTL Class II	25	25
HSUL-12	34, 40, 48	34, 40, 48
Differential SSTL-2 Class I	50	50
Differential SSTL-2 Class I	25	25

I/O Standard	Calibrated OCT (Output)	Uncalibrated OCT (Output)
	R_S (Ω)	R_S (Ω)
Differential SSTL-18 Class I	50	50
Differential SSTL-18 Class II	25	25
Differential SSTL-15 Class I	50	50
Differential SSTL-15 Class II	25	25
Differential SSTL-15	34, 40	34, 40
Differential SSTL-135	34, 40	34, 40
Differential 1.8 V HSTL Class I	50	50
Differential 1.8 V HSTL Class II	25	25
Differential 1.5 V HSTL Class I	50	50
Differential 1.5 V HSTL Class II	25	25
Differential 1.2 V HSTL Class I	50	50
Differential 1.2 V HSTL Class II	25	25
Differential HSUL-12	34, 40, 48	34, 40, 48

MAX 10 I/O Design Considerations

3

2015.06.10

UG-M10GPIO

There are several considerations that require your attention to ensure the success of your designs. Unless noted otherwise, these design guidelines apply to all variants of this device family.

Related Information

MAX 10 I/O Overview on page 1-1

Guidelines: V_{CCIO} Range Considerations

There are several V_{CCIO} range considerations because of I/O pin configuration function and I/O bank location.

- The shared I/O pins can only support a V_{CCIO} range of 1.5 V to 3.3 V when you access the configuration function in user mode.The configuration function of the I/O pins can only support 1.5 V to 3.3 V. If you need to access, for example, JTAG pins during user mode, the bank where the pin resides will be constrained by this V_{CCIO} range. If you want to use I/O standards within the 1.2 V to 1.35 V range, you must not use the configuration function of any of the I/O pins during user mode. This only affects bank 1 (including bank 1A and bank 1B in applicable devices) and bank 8 because only these banks have I/O pins with configuration function.
- If you plan to migrate from devices that has banks 1A and 1B to devices that has only bank 1, ensure that the V_{CCIO} of bank 1A and 1B are the same.
- For the V36 package of the 10M02 device, the V_{CCIO} of these groups of I/O banks must be the same:
  - Group 1—banks 1, 2 and 8
  - Group 2—banks 3, 5, and 6
- For the V81 package of the 10M08 device, the V_{CCIO} of these groups of I/O banks must be the same:
  - Group 1—banks 1A, 1B, and 2
  - Group 2—banks 5 and 6

Guidelines: Voltage-Referenced I/O Standards Restriction

These restrictions apply if you use the V_{REF} pin.

- If you use a shared VREF pin as an I/O, all voltage-reference input buffers (SSTL, HSTL, and HSUL) are disabled.
- If you use a shared VREF pin as a voltage reference, you must enable the input buffer of specific I/O pin to use the voltage-reference I/O standards.
- The voltage-referenced I/O standards are not supported in the following I/O banks of these device packages:
  - All I/O banks of V36 package of 10M02.
  - All I/O banks of V81 package of 10M08.
  - Bank 1A and 1B of E144 package of 10M50.
- Maximum number of voltage-referenced inputs for each VREF pin is 75% of total number of I/O pads. The Quartus II software will provide a warning if you exceed the maximum number.
- Except for I/O pins that you used for static signals, all non-voltage-referenced output must be placed two pads away from a VREF pin. The Quartus II software will output an error message if this rule is violated.

Related Information

MAX 10 I/O Standards Support on page 2-1

Guidelines: Enable Clamp Diode for LVTTL/LVCMOS Input Buffers

If the V_{CCIO} of the I/O bank is lower than the voltage of the LVTTL/LVCMOS input buffers, Altera recommends that you enable the clamp diode.

- 3.3 V LVCMOS/LVTTL input buffers—enable clamp diode if V_{CCIO} of the I/O bank is 3.0 V.
- 3.3 V or 3.0 V LVCMOS/LVTTL input buffers—enable clamp diode if V_{CCIO} of the I/O bank is 2.5 V.

By enabling the clamp diode under these conditions, you will be able to limit overshoot or undershoot. However, this does not comply with hot socket current specification.

If you do not enable the clamp diode under these conditions, the signal integrity for the I/O pin will be impacted and there will be overshoot or undershoot problem. In this situation, you must ensure that your board design conforms to the overshoot/undershoot specifications.

Table 3-1: Voltage Tolerance Maximum Ratings for 3.3 V or 3.0 V

This table lists the voltage tolerance specifications. Ensure that your board design conforms to these specifications if you do not want to follow the clamp diode recommendation.

Voltage	Minimum (V)	Maximum (V)
V_{CCIO} = 3.3 V	3.135	3.45
V_{CCIO} = 3.0 V	2.85	3.15
V_{IH} (AC)	—	4.1
V_{IH} (DC)	—	3.6
V_{IL} (DC)	–0.3	0.8

Guidelines: Adhere to the LVDS I/O Restrictions Rules

For LVDS applications, adhere to the I/O restriction pin connection guidelines to avoid excessive jitter on the LVDS transmitter output pins. The Quartus II software generates a critical warning if these rules are violated.

Related Information

MAX 10 FPGA Device Family Pin Connection Guidelines

Guidelines: I/O Restriction Rules

For different I/O standards and conditions, you must limit the number of I/O pins. This I/O restriction rule is applicable if you use LVDS transmitters or receivers.

Table 3-2: Maximum Percentage of I/O Pins Allowed for Specific I/O Standards in an I/O Bank

This table lists the maximum number of general purpose output pins allowed in a bank in terms of percentage to the total number of I/O pins available in an I/O bank if you use these combinations of I/O standards and conditions.

I/O Standard	Condition	Max Pins Per Bank (%)
2.5 V LVTTL/ LVCMOS	16 mA current strength and 25 Ω OCT (fast and slow slew rate)	25
	12 mA current strength (fast and slow slew rate)	30
	8 mA current strength (fast and slow slew rate) and 50 Ω OCT (fast slew rate)	45
	4 mA current strength (fast and slow slew rate)	65
2.5 V SSTL	—	100

Guidelines: Analog-to-Digital Converter I/O Restriction

These restrictions are applicable if you use the analog-to-digital converter (ADC) block.

The Quartus II software uses physics-based rules to define the number of I/Os allowed in a particular bank. These rules are based on noise calculation to analyze accurately the impact of I/O placement on the ADC performance.

Implementation of the physics-based rules will be in stages, starting from Quartus II software version 14.1 for 10M04, 10M08, 10M40, and 10M50 devices. The physics-based rules for other MAX 10 devices will be implemented in future versions of the software.

Altera highly recommends that you adhere to these guidelines to ensure ADC performance. Furthermore, following these guidelines prevents additional critical warning from future versions of the Quartus II software when the physics-based rules are implemented.

Table 3-3: I/O Restrictions Related to ADC Usage—Preliminary

This table lists the I/O restrictions by MAX 10 device package if you use the dedicated analog input (ANAIN1 or ANAIN2) or any dual function ADC I/O pins as ADC channel inputs.

Package	Restriction/Guideline
All	Disable all JTAG operation during ADC sampling. The ADC signal-to-noise and distortion ratio (SINAD) is not guaranteed during JTAG operation.

M153
U169
U324
F256
F484
F672
	• Banks 1A and 1B—You cannot use GPIO pins in these banks.
	• Banks 2, 3, 4, 5, 6, and 7—You can use GPIO pins located in these banks.
	• Bank 8—You can use a percentage of the GPIO pins in this bank based on drive strength:
	  • For the percentage of GPIO pins allowed, refer to Table 3-4(9).
	  • Use low drive strength (8 mA and below) and differential I/O standards.
	  • Do not place transmitter pins in this bank. Use banks 2, 3, 4, 5, 6, or 7 instead.
	  • You can use static pins such as RESET or CONTROL.
	  • GPIO pins in this bank are governed by physics-based rules. The Quartus II software will issue a critical warning I/O settings violates any of the I/O physic-based rule.

E144	• Bank 1A, 1B, 2, and 8—You cannot use GPIO pins in these banks.
	• Banks 4 and 6—You can use GPIO pins located in these banks.
	• Banks 3, 5, and 7—You can use a percentage of the GPIO pins in this bank based on drive strength:
	  • For the percentage of GPIO pins allowed, refer to Table 3-5.
	  • Use low drive strength (8 mA and below) and differential I/O standards.
	  • GPIO pins in these banks are governed by physics-based rules. The Quartus II software will issue a critical warning I/O settings violates any of the I/O physic-based rule.

Table 3-4: I/O Usage Restriction for Bank 8 in MAX 10 F484 Package

This table lists the percentage of I/O pins available in I/O bank 8 if you use the dedicated analog input (ANAIN1 or ANAIN2) or any dual function ADC I/O pins as ADC channel. Refer to Table 3-6 for the list of I/O standards in each group.

I/O Standards	TX	RX	Total	Availability (%)
Group 1	18	18	36	100
Group 2	16	16	32	89
Group 3	7	11	18	50
Group 4	5	7	12	33
Group 5	4	6	10	28

(9) Percentage of GPIO pins allowed in bank 8 for other packages will be made available in the future.

I/O Standards	TX	RX	Total	Availability (%)
Group 6	4	4	8	22
Group 7	0	8	8	22

Table 3-5: I/O Usage Restriction for Banks 3, 5, and 7 in MAX 10 E144 Package

This table lists the percentage of I/O pins available in banks 3, 5, and 7 if you use the dedicated analog input (`ANAIN1` or `ANAIN2`) or any dual function ADC I/O pins as ADC channel inputs. Refer to **Table 3-6** for the list of I/O standards in each group.

I/O Standards	Bank 3			Bank 5			Bank 7			Device I/O Availability (%)
	TX	RX	Availability (%)	TX	RX	Availability (%)	TX	RX	Availability (%)	
Group 1	7	8	88	6	6	100	4	3	100	54
Group 2	7	8	88	6	6	100	4	3	100	54
Group 3	4	5	50	6	6	100	2	0	29	45
Group 4	3	4	39	5	5	83	0	0	0	39
Group 5	2	3	28	5	5	83	0	0	0	37
Group 6	1	2	17	5	5	83	0	0	0	35
Group 7	0	0	0	5	5	83	0	0	0	32

Table 3-6: I/O Standards Groups Categorized According to Drive Strengths

I/O Standard Group	I/O Standards Name and Drive Strength
Group 1	• 2.5 V LVDS • 2.5 V RSDS • BLVDS at 4 mA • SLVS at 4 mA

I/O Standard Group	I/O Standards Name and Drive Strength
Group 2	• BLVDS at 8 mA • SLVS at 8 mA • Sub-LVDS at 8 mA • 1.8 V, 1.5 V, and 1.2 V HSTL Class I at 8 mA • SSTL-15 at 34 Ω or 40 Ω • SSTL-135 at 34 Ω or 40 Ω • HSUL-12 at 34 Ω or 40 Ω • SSTL-2 Class I at 8 mA • SSTL-18 Class I at 8 mA • SSTL-15 Class I at 8 mA • 2.5 V and 1.8 V LVTTL at 4 mA • 2.5 V, 1.8 V, 1.5 V, and 1.2 V LVCMOS at 4 mA • 1.8 V LVTTL at 2 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 2 mA
Group 3	• BLVDS at 12 mA • SLVS at 12 mA • Sub-LVDS at 12 mA • SSTL-2 Class I at 10 mA or 12 mA • SSTL-18 Class I at 10 mA or 12 mA • SSTL-15 Class I at 10 mA or 12 mA • 1.8 V, 1.5 V, and 1.2 V HSTL Class I at 10 mA or 12 mA • SSTL-2 at 50 Ω • SSTL-18 at 50 Ω • SSTL-15 at 50 Ω • 1.8 V, 1.5 V and 1.2 V HSTL at 50 Ω • HSUL-12 at 48 Ω • 2.5 V and 1.8 V LVTTL at 50 Ω • 2.5 V, 1.8 V, 1.5 V, and 1.2 V LVCMOS at 50 Ω • 1.8 V LVTTL at 6 mA or 8 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 6 mA or 8 mA • 3.0 V LVTTL at 4 mA • 3.0 V LVCMOS at 4 mA
Group 4	• SSTL-18 Class II at 12 mA • 3.0 V LVTTL at 50 Ω • 3.0 V LVCMOS at 50 Ω • 2.5 V LVTTL at 8 mA • 2.5 V LVCMOS at 8 mA • 1.8 V LVTTL at 10 mA or 12 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 10 mA or 12 mA • 3.3 V LVCMOS at 2 mA

I/O Standard Group	I/O Standards Name and Drive Strength
Group 5	• SSTL-2 Class II at 16 mA • SSTL-18 Class II at 16 mA • SSTL-15 Class II at 16 mA • 1.8 V and 1.5 V HSTL Class II at 16 mA • 1.2 V HSTL Class II at 14 mA • SSTL-18 at 25 Ω • SSTL-15 at 25 Ω • SSTL-2 at 25 Ω • 1.8 V, 1.5 V, and 1.2 V HSTL at 25 Ω • 2.5 V and 1.8 V LVTTL at 25 Ω • 2.5 V, 1.8 V, 1.5 V, and 1.2 LVCMOS at 25 Ω • 1.8 V LVTTL at 16 mA • 1.8 V and 1.5 V LVCMOS at 16 mA • 2.5 V LVCMOS at 12 mA • 2.5 V LVTTL at 12 mA • 3.0 V LVCMOS at 8 mA • 3.0 V LVTTL at 8 mA • 3.3 V LVTTL at 4 mA or 8 mA
Group 6	• 2.5 V LVTTL at 16 mA • 2.5 V LVCMOS at 16 mA • 3.0 V LVTTL at 12 mA • 3.0 V LVCMOS at 12 mA • 3.0 V LVTTL at 25 Ω • 3.0 V LVCMOS at 25 Ω
Group 7	• 3.0 V LVTTL at 16 mA • 3.0 V LVCMOS at 16 mA

Guidelines: External Memory Interface I/O Restrictions

These I/O rules are applicable if you use external memory interfaces in your design.

Two GPIOs Adjacent to DQ Pin Is Disabled

This limitation is applicable to MAX 10 10M16, 10M25, 10M40, and 10M50 devices, and only if you use DDR3 and LPDDR2 SDRAM memory standards.

Table 3-7: DDR3 and LPDDR2 Memory Interface Widths and Device Packages Where Two GPIOs Adjacent to DQ Pins Are Disabled

This table lists the combination of MAX 10 10M16, 10M25, 10M40, and 10M50 device packages, and DDR3 and LPDDR2 memory interface widths where you cannot use two GPIO pins that are adjacent to the DQ pins.

Device Package	Memory Interface Width (DDR3 and LPPDR2 only)
U324	x8
F484	x8, x16, x24
F672	x8, x16, x24

Total I/O Utilization In Bank Must Be 75 Percent or Less In Some Devices

If you use DDR3 or LPDDR2 SDRAM memory interface standards, you can generally use a maximum of 75 percent of the total number of I/O pins available in a bank. This restrictions differ from device to device. In some devices packages you can use all 100 percent of the I/Os. The Quartus II software will output an error message if the I/O usage per bank of that device is affected by this rule.

If you use DDR2 memory interface standards, you can assign 25 percents of the I/O pins as input pins only.

Guidelines: Dual-Purpose Configuration Pin

To use configuration pins as user I/O pins in user mode, you have to adhere to the following guidelines.

Table 3-8: Dual-Purpose Configuration Pin Guidelines for MAX 10 Devices

Pins	Guidelines
nCONFIG nSTATUS CONF_DONE	During initialization: • tri-state the external I/O driver and drive an external pull-up resistor(10) or • use the external I/O driver to drive the pins to the state same as the external weak pull-up resistor
nSTATUS CONF_DONE TDO	Tri-state the external driver of the configuration pins before the t_{WAIT} (minimum) wait time is reached. You can use these pins for configuration purpose after t_{WAIT} (maximum).
nCONFIG	You can only use the nCONFIG pin as a single-ended input pin in user mode. If the nCONFIG is set as user I/O, you can trigger the reconfiguration by: • asserting RU_nCONFIG of the remote system upgrade circuitry • issuing PULSE_NCONFIG JTAG instruction

(10) If you intend to remove the external weak pull-up resistor, Altera recommends that you remove it after the device enters user mode.

Pins	Guidelines
TDO TMS TCK TDI	• If you intend to switch back and forth between user I/O pins and JTAG pin functions using the JTAGEN pin, all JTAG pins must be assigned as single-ended I/O pins or voltage-referenced I/O pins. Schmitt trigger input is the recommended input buffer. • JTAG pins cannot perform as JTAG pins in user mode if you assign any of the JTAG pin as a differential I/O pin. • You must use the JTAG pins as dedicated pins and not as user I/O pins during JTAG programming. • Do not toggle JTAG pin during the initialization stage. • Put the test access port (TAP) controller in reset state and drive the TDI and TMS pins high and TCK pin low before the initialization.

Related Information

MAX 10 FPGA Configuration User Guide

Provides more information about the dual-purpose I/O pins in configuration and user modes.

MAX 10 I/O Implementation Guides

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You can implement your I/O design in the Quartus II software. The software contains tools for you to create and compile your design, and configure your device.

The Quartus II software allows you to prepare for device migration, set pin assignments, define placement restrictions, setup timing constraints, and customize IP cores. For more information about using the Quartus II software, refer to the related information.

Related Information

MAX 10 I/O Overview on page 1-1

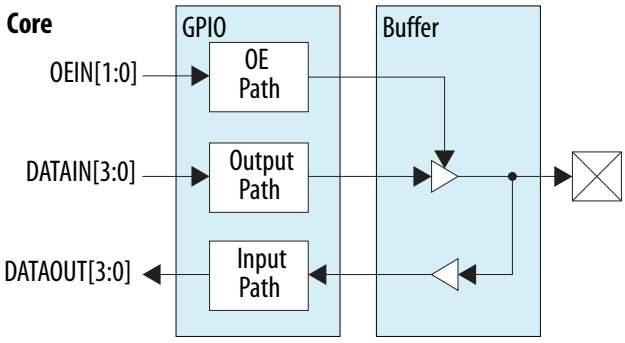
Altera GPIO Lite IP Core

The Altera GPIO Lite IP core supports the MAX 10 GPIO components. To implement the GPIOs in your design, you can customize the Altera GPIO Lite IP core to suit your requirements and instantiate it in your design.

GPIOs are I/Os used in general applications not specific to transceivers, memory-like interfaces or LVDS. The Altera GPIO Lite IP core features the following components:

- Double data rate input/output (DDIO)—A digital component that doubles the data-rate of a communication channel.
- I/O buffers—connect the pads to the FPGA.

Figure 4-1: High Level View of Single-Ended GPIO



Related Information

- **Altera GPIO Lite IP Core References** on page 5-1
- **Introduction to Altera IP Cores**
- **Specifying IP Core Parameters and Options** on page 4-6
- **Files Generated for Altera IP Cores (Legacy Parameter Editor)**
- **Simulating Altera IP Cores in other EDA Tools**
- **Upgrading Outdated IP Cores**

Altera GPIO Lite IP Core Data Paths

Table 4-1: Altera GPIO Lite Data Path Modes

Data Path	Mode		
	Bypass	Single Register	DDR
Input	Data goes from the delay element to the core, bypassing all double data rate I/Os (DDIOs).	The full-rate DDIO operates as a single register.	The full-rate DDIO operates as a regular DDIO.
Output	Data goes from the core straight to the delay element, bypassing all DDIOs.	The full-rate DDIO operates as a single register.	The full-rate DDIO operates as a regular DDIO.
Bidirectional	The output buffer drives both an output pin and an input buffer.	The full-rate DDIO operates as a single register. The output buffer drives both an output pin and an input buffer.	The full-rate DDIO operates as a regular DDIO. The output buffer drives both an output pin and an input buffer. The input buffer drives a set of three flip-flops.

If you use asynchronous clear and preset signals, all DDIOs share these same signals.

DDR Input Path

The pad sends data to the input buffer and the input buffer feeds the delay element. From the delay element, the data is fed to the DDIO stage, which consists of three registers:

- `RegAi` samples the data from `pad_in` at the positive clock edge.
- `RegBi` samples the data from `pad_in` at the negative clock edge.
- `RegCi` samples the data from `RegAi` at the negative clock edge.

Figure 4-2: Simplified View of Altera GPIO Lite DDR Input Path

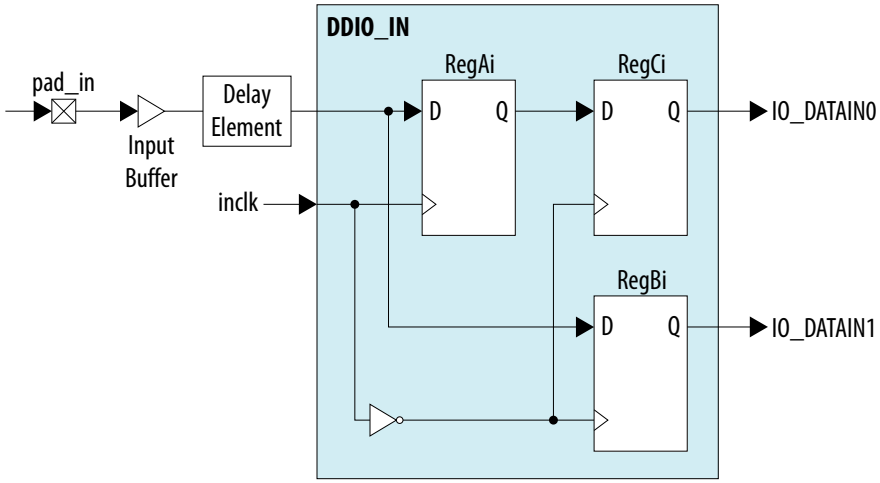
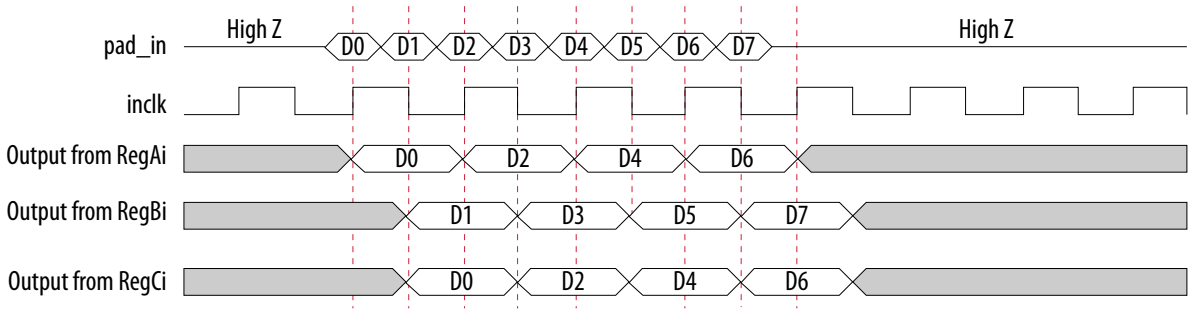


Figure 4-3: Altera GPIO Lite Input Path Timing Diagram



DDR Output Path with Output Enable

- `RegCo` samples the data from `IO_DATAOUT0` at the positive clock edge.
- `RegDo` samples the data from `IO_DATAOUT1` when `outclock` value is 0.
- `Output DDR` samples the data from `RegCo` at the positive clock edge, and from `RegDo` at the negative clock edge.

Figure 4-4: Simplified View of Altera GPIO Lite DDR Output Path with Output Enable

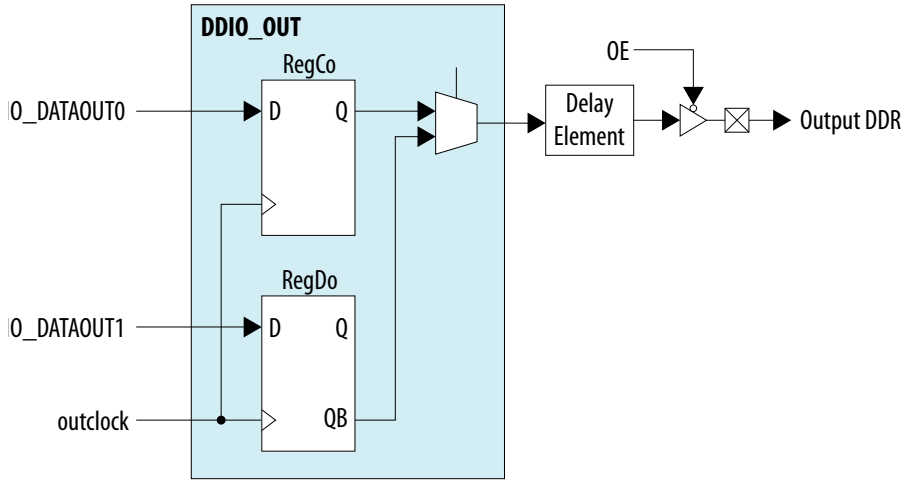
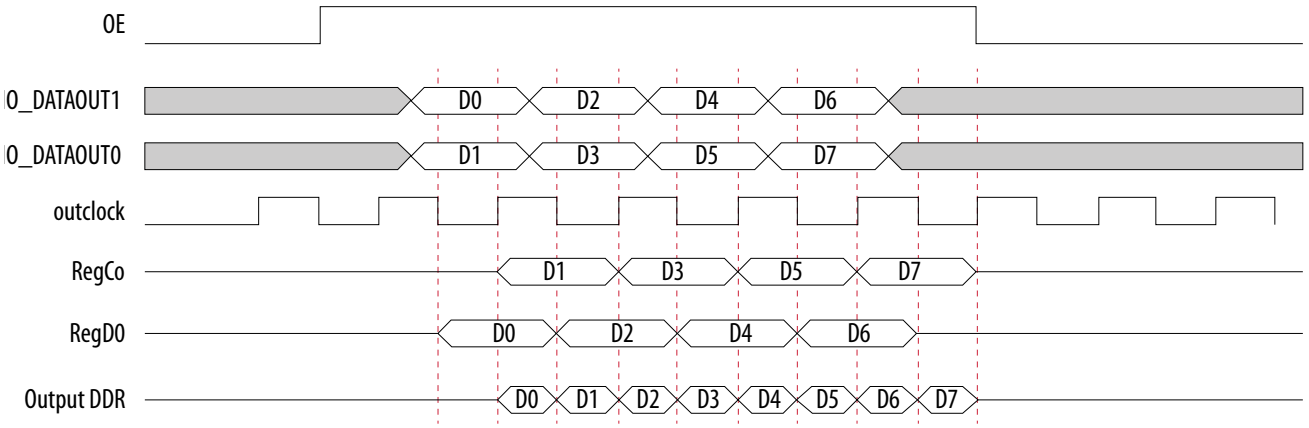


Figure 4-5: Altera GPIO Lite Output Path Timing Diagram



IP Catalog and Parameter Editor

The Quartus II IP Catalog (**Tools** > **IP Catalog**) and parameter editor help you easily customize and integrate IP cores into your project. You can use the IP Catalog and parameter editor to select, customize, and generate files representing your custom IP variation.

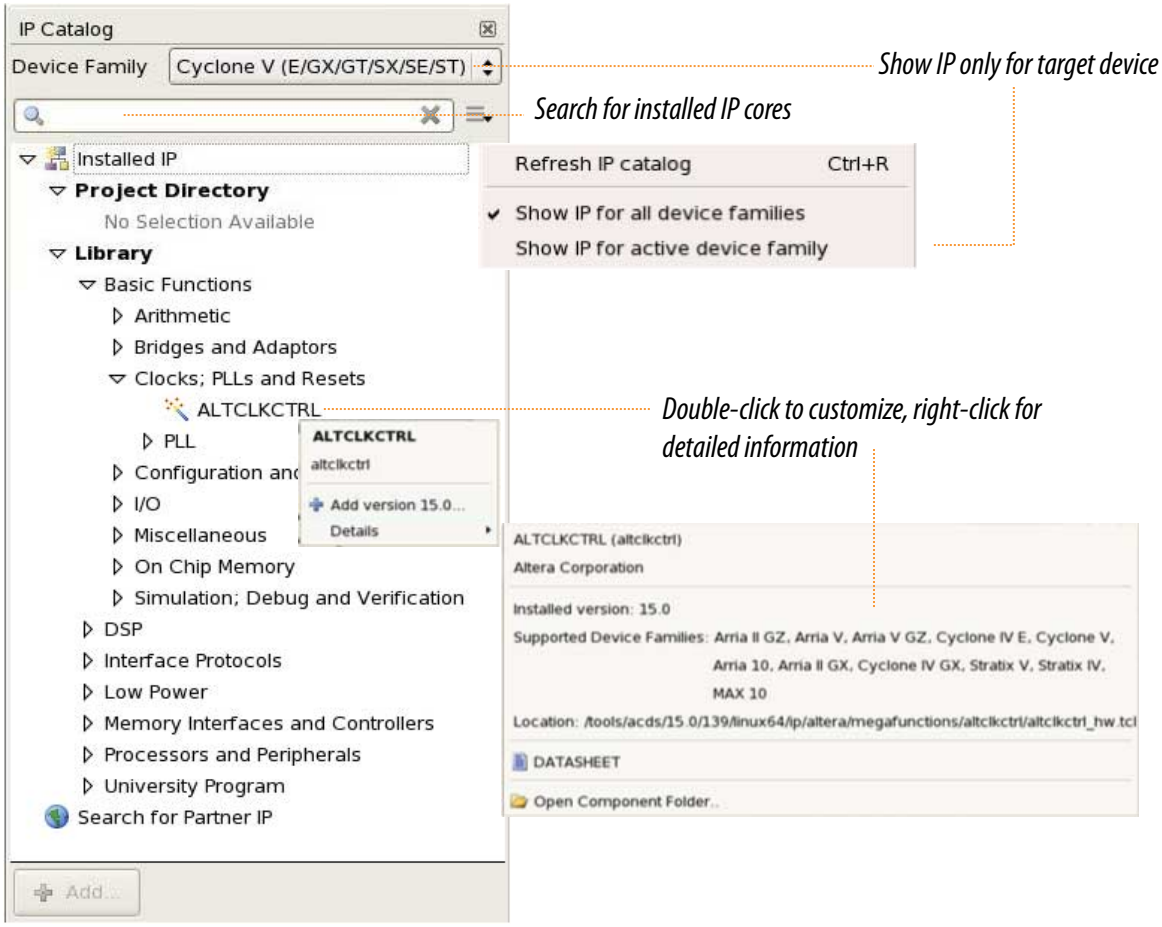
Note: The IP Catalog (**Tools** > **IP Catalog**) and parameter editor replace the MegaWizard™ Plug-In Manager for IP selection and parameterization, beginning in Quartus II software version 14.0. Use the IP Catalog and parameter editor to locate and paramaterize Altera IP cores.

The IP Catalog lists installed IP cores available for your design. Double-click any IP core to launch the parameter editor and generate files representing your IP variation. The parameter editor prompts you to specify an IP variation name, optional ports, and output file generation options. The parameter editor generates a top-level Qsys system file (**.qsys**) or Quartus II IP file (**.qip**) representing the IP core in your project. You can also parameterize an IP variation without an open project.

Use the following features to help you quickly locate and select an IP core:

- Filter IP Catalog to **Show IP for active device family** or **Show IP for all device families**. If you have no project open, select the **Device Family** in IP Catalog.
- Type in the Search field to locate any full or partial IP core name in IP Catalog.
- Right-click an IP core name in IP Catalog to display details about supported devices, open the IP core's installation folder, and view links to documentation.
- Click **Search for Partner IP**, to access partner IP information on the Altera website.

Figure 4-6: Quartus II IP Catalog



Note: The IP Catalog is also available in Qsys (**View** > **IP Catalog**). The Qsys IP Catalog includes exclusive system interconnect, video and image processing, and other system-level IP that are not available in the Quartus II IP Catalog. For more information about using the Qsys IP Catalog, refer to *Creating a System with Qsys* in the *Quartus II Handbook*.

Related Information

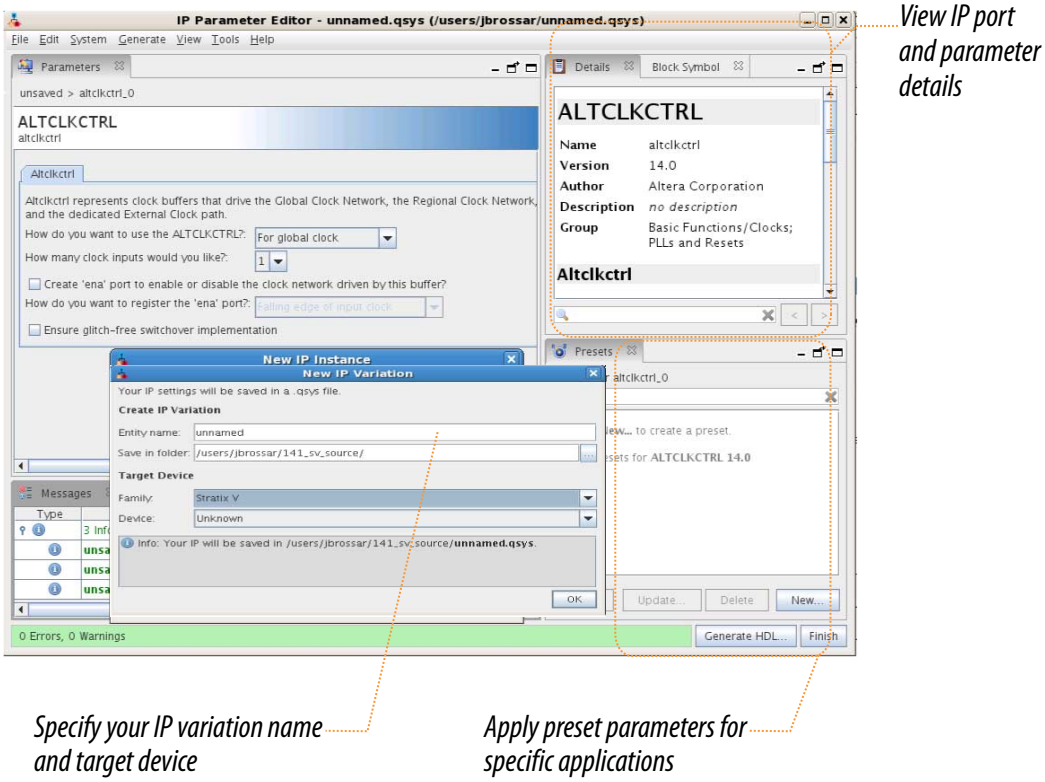
Provides more information about the programmableCreating a System With Qsys, Volume 1: Design and Synthesis, Quartus II Handbook

Specifying IP Core Parameters and Options

You can quickly configure a custom IP variation in the parameter editor. Use the following steps to specify IP core options and parameters in the parameter editor. Refer to *Specifying IP Core Parameters and Options (Legacy Parameter Editors)* for configuration of IP cores using the legacy parameter editor.

1. In the IP Catalog (**Tools** > **IP Catalog**), locate and double-click the name of the IP core to customize. The parameter editor appears.
2. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named <*your_ip*>**.qsys**. Click **OK**.
3. Specify the parameters and options for your IP variation in the parameter editor, including one or more of the following. Refer to your IP core user guide for information about specific IP core parameters.
   - Optionally select preset parameter values if provided for your IP core. Presets specify initial parameter values for specific applications.
   - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
   - Specify options for processing the IP core files in other EDA tools.
4. Click **Generate HDL**, the **Generation** dialog box appears.
5. Specify output file generation options, and then click **Generate**. The IP variation files generate according to your specifications.
6. To generate a simulation testbench, click **Generate** > **Generate Testbench System**.
7. To generate an HDL instantiation template that you can copy and paste into your text editor, click **Generate** > **HDL Example**.
8. Click **Finish**. The parameter editor adds the top-level **.qsys** file to the current project automatically. If you are prompted to manually add the **.qsys** file to the project, click **Project** > **Add/Remove Files in Project** to add the file.
9. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

Figure 4-7: IP Parameter Editor



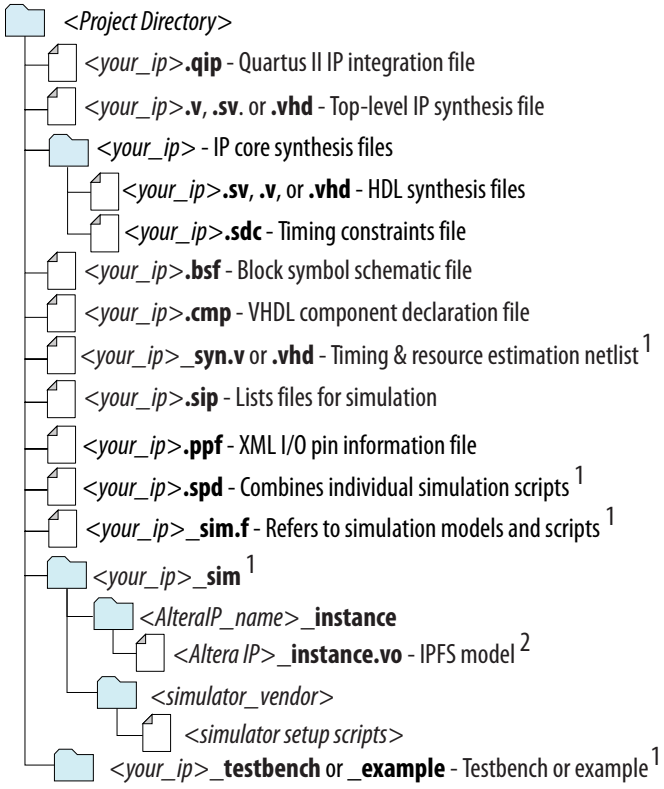
Related Information

- **Altera GPIO Lite IP Core** on page 4-1
- **Quartus II Handbook, Volume 1: Design and Synthesis**
  Provides more information about using IP cores in the Quartus II software.

Files Generated for Altera IP Cores (Legacy Parameter Editor)

The Quartus II software version 14.0 and previous generates the following output for IP cores that use the legacy MegaWizard parameter editor.

Figure 4-8: IP Core Generated Files



Notes:
1. If supported and enabled for your IP variation
2. If functional simulation models are generated

Verifying Pin Migration Compatibility

You can use the **Pin Migration View** window in the Quartus II software Pin Planner to assist you in verifying whether your pin assignments migrate to a different device successfully.

You can vertically migrate to a device with a different density while using the same device package, or migrate between packages with different densities and ball counts.

1. Open **Assignments** > **Pin Planner** and create pin assignments.
2. If necessary, perform one of the following options to populate the Pin Planner with the node names in the design:
   - Analysis & Elaboration
   - Analysis & Synthesis
   - Fully compile the design
3. Then, on the menu, click **View** > **Pin Migration View**.
4. To select or change migration devices:

a. Click **Device** to open the **Device** dialog box.
b. Under **Migration compatibility** click **Migration Devices**.

5. To show more information about the pins:
   a. Right-click anywhere in the **Pin Migration View** window and select **Show Columns**.
   b. Then, click the pin feature you want to display.
6. If you want to view only the pins, in at least one migration device, that have a different feature than the corresponding pin in the migration result, turn on **Show migration differences**.
7. Click **Pin Finder** to open the **Pin Finder** dialog box and find and highlight pins with specific functionality.

   If you want to view only the pins found and highlighted by the most recent query in the **Pin Finder** dialog box, turn on **Show only highlighted pins**.
8. To export the pin migration information to a Comma-Separated Value File (**.csv**), click **Export**.

Related Information

MAX 10 I/O Vertical Migration Support on page 1-3

Altera GPIO Lite IP Core References

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You can set various parameter settings for the Altera GPIO Lite IP core to customize its behaviors, ports, and signals.

The Quartus II software generates your customized Altera GPIO Lite IP core according to the parameter options that you set in the parameter editor.

Related Information

- **MAX 10 I/O Overview** on page 1-1
- **Altera GPIO Lite IP Core** on page 4-1

Altera GPIO Lite Parameter Settings

You can set the parameter settings for the Altera GPIO Lite IP core in the Quartus II software. There are three groups of options: **General**, **Buffer**, and **Registers**.

Table 5-1: Altera GPIO Lite Parameters - General

Parameter	Condition	Allowed Values	Description
Data direction	—	• input • output • bidir	Specifies the data direction for the GPIO.
Data width	—	1 to 128	Specifies the data width.

Table 5-2: Altera GPIO Lite Parameters - Buffer

Parameter	Condition	Allowed Values	Description
Use true differential buffer	Data direction = input or output	• On • Off	If turned on, enables true differential I/O buffers and disables pseudo differential I/O buffers.

Parameter	Condition	Allowed Values	Description
Use pseudo differential buffer	Data direction = output or bidir	• On • Off	• If turned on in output mode—enables pseudo differential output buffers and disables true differential I/O buffers. • If turned on in bidir mode—enables true differential input buffer and pseudo differential output buffer.
Use bus-hold circuitry	Data direction = input or output	• On • Off	If turned on, the bus hold circuitry can weakly hold the signal on an I/O pin at its last-driven state where the output buffer state will be 1 or 0 but not high-impedance.
Use open drain output	Data direction = output or bidir	• On • Off	If turned on, the open drain output enables the device to provide system-level control signals such as interrupt and write enable signals that can be asserted by multiple devices in your system.
Enable oe port	Data direction = output	• On • Off	If turned on, enables user input to the OE port. This option is automatically turned on for bidirectional mode.

Table 5-3: Altera GPIO Lite Parameters - Registers

Parameter	Condition	Allowed Values	Description
Register mode	—	• bypass • single-register • ddr	Specifies the register mode for the Altera GPIO Lite IP core: • **bypass**—specifies a simple wire connection from/to the buffer. • **single-register**—specifies that the DDIO is used as a simple register in single data-rate mode (SDR). The Fitter may pack this register in the I/O. • **ddr**— specifies that the IP core uses the DDIO.
Enable aclr port	• Register mode = ddr	• On • Off	If turned on, enables the ACLR port for asynchronous clears.
Enable aset port	• Data direction = output or bidir • Register mode = ddr • Set registers to power up high (when aclr and aset ports are not used) = off	• On • Off	If turned on, enables the ASET port for asynchronous preset.
Set registers to power up high (when aclr and aset ports are not used)	• Register mode = ddr • Enable aclr port = off • Enable aset port = off • Enable sclr port = off	• On • Off	If you are not using the ACLR and ASET ports: • **On**—specifies that registers power up HIGH. • **Off**—specifies that registers power up LOW.

Parameter	Condition	Allowed Values	Description
Enable inclocken/outclocken ports	Register mode = ddr	• On • Off	• **On**—exposes the clock enable port to allow you to control when data is clocked in or out. This signal prevents data from being passed through without your control. • **Off**—clock enable port is not exposed and data always pass through the register automatically.
Invert din	• Data direction = output • Register mode = ddr	• On • Off	If turned on, inverts the data out output port.
Invert DDIO inclock	• Data direction = input or bidir • Register mode = ddr	• On • Off	• **On**—captures the first data bit on the falling edge of the input clock. • **Off**—captures the first data bit on the rising edge of the input clock.
Use a single register to drive the output enable (oe) signal at the I/O buffer	• Data direction = output or bidir • Register mode = single-register or ddr • Use DDIO registers to drive the output enable (oe) signal at the I/O buffer = off	• On • Off	If turned on, specifies that a single register drives the `OE` signal at the output buffer.
Use DDIO registers to drive the output enable (oe) signal at the I/O buffer	• Data direction = output or bidir • Register mode = ddr • Use a single register to drive the output enable (oe) signal at the I/O buffer = off	• On • Off	If turned on, specifies that the DDR I/O registers drive the `OE` signal at the output buffer. The output pin is held at high impedance for an extra half clock cycle after the `OE` port goes high.

Parameter	Condition	Allowed Values	Description
Implement DDIO input registers in hard implementation (Only available in certain devices)	• Data direction = input or bidir • Register mode = ddr	• On • Off	• **On**—implements the DDIO input registers using hard block at the I/O edge. • **Off**—implements the DDIO input registers as soft implementation using registers in the FPGA core fabric. This option is applicable only for MAX 10 16, 25, 40, and 50 devices because the DDIO input registers hard block is available only in these devices. To avoid Fitter error, turn this option off for other MAX 10 devices.

Altera GPIO Lite Interface Signals

Depending on parameter settings you specify, different interface signals are available for the Altera GPIO Lite IP core.

Table 5-4: Pad Interface Signals

The pad interface connects the Altera GPIO Lite IP core to the pads.

Signal Name	Direction	Description
`pad_in`	Input	Input pad port if you use the input path.
`pad_in_b`	Input	Input negative pad port if you use the input path and enable the true or pseudo differential buffers.
`pad_out`	Output	Output pad port if you use the output path.
`pad_out_b`	Output	Output negative pad port if you use the output path and enable the true of pseudo differential buffers.
`pad_io`	Bidirectional	Bidirectional pad port if you use bidirectional paths.
`pad_io_b`	Bidirectional	Bidirectional negative pad port if you use bidirectional paths and enable true or pseudo differential buffers.

Table 5-5: Data Interface Signals

The data interface is an input or output interface from the Altera GPIO Lite IP core to the FPGA core.

Signal Name	Direction	Description
din	Input	Data received from the input pin. Signal width for each input pin: • DDR mode—2 • Other modes—1
dout	Output	Data to send out through the output pin. Signal width for each output pin: • DDR mode—2 • Other modes—1
oe	Input	Control signal that enables the output buffer. This signal is active HIGH.
nsleep	Input	Control signal that enables the input buffer. This signal is active LOW. This signal is available for the 10M16, 10M25, 10M40, and 10M50 devices.

Table 5-6: Clock Interface Signals

The clock interface is an input clock interface. It consists of different signals, depending on the configuration. The Altera GPIO Lite IP core can have zero, one, two, or four clock inputs. Clock ports appear differently in different configurations to reflect the actual function performed by the clock signal.

Signal Name	Direction	Description
inclock	Input	Input clock that clocks the registers in the input path.
inclocken	Input	Control signal that controls when data is clocked in. This signal is active HIGH.
outclock	Input	Input clock that clocks the registers in the output path.
ouctlocken	Input	Control signal that controls when data is clocked out. This signal is active HIGH.

Table 5-7: Reset Interface Signals

The reset interface connects the Altera GPIO Lite IP core to the DDIOs.

Signal Name	Direction	Description
aclr	Input	Control signal for asynchronous clear that sets the register output state to 0. This signal is active HIGH.
aset	Input	Control signal for asynchronous preset that sets the register output state to 1. This signal is active HIGH.
sclr	Input	Control signal for synchronous clear that sets the register output to 0. This signal is active HIGH.

Additional Information for MAX 10 General Purpose I/O User Guide

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Document Revision History for MAX 10 General Purpose I/O User Guide

Date	Version	Changes
June 2015	2015.06.10	• Added related link to the MAX 10 device pin-outs in topic about I/O banks locations. The device pin-out files provide more information about available I/O pins in each I/O bank. • Updated the ADC I/O restriction guidelines topic.
May 2015	2015.05.04	• Removed the F672 package of the MAX 10 10M25 device. • Updated footnote for LVDS (dedicated) in the table listing the supported I/O standards to clarify that you can use LVDS receivers on all I/O banks. • Added missing footnote number for the DQS column of the 3.3 V Schmitt Trigger row in the table that lists the I/O standards voltage levels and pin support. • Added a table listing the I/O standards and current strength settings that support programmable output slew rate control. • Updated the topic about external memory interface I/O restrictions to add x24 memory interface width to the F484 package. • Added topic about the programmable differential output voltage. • Updated the guidelines for voltage-referenced I/O standards to add a list of device packages that do not support voltage-referenced I/O standards. • Updated the topic about the I/O restriction rules to remove statements about the differential pad placement rules. • Renamed the `input_ena` signal name to `nsleep` and updated the relevant description. • Updated the description for the **Invert DDIO inclock** parameter of the Altera GPIO Lite IP core.

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Date	Version	Changes
December 2014	2014.12.15	Updated the topic about the ADC I/O restriction: • Added information about implementation of physics-based rules in the Quartus II software. • Updated the list of I/O standards groups for the ADC I/O restriction.
September 2014	2014.09.22	Initial release.