

Notified Access Implementation Discussion

James Dinan

MPI Forum

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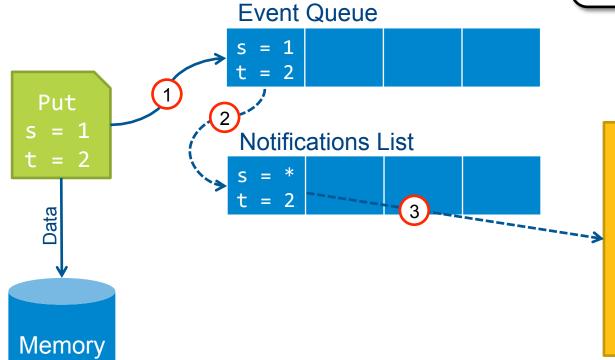
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Implementation Sketch





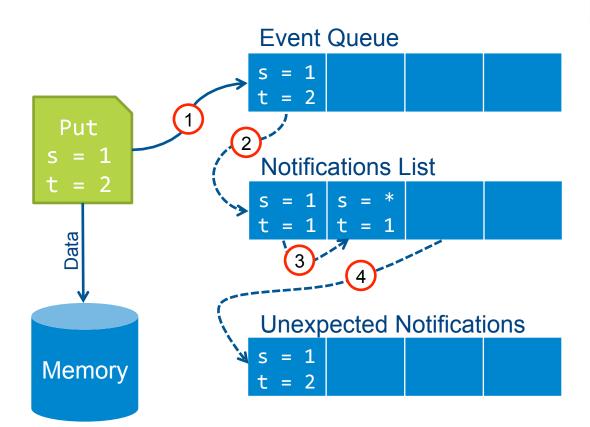


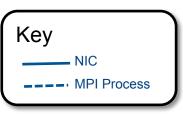
Notification Request

```
s = *
t = 2
count = 5
max = 10
last_src = 1
last_tag = 2
```

Implementation Sketch

Unexpected Case





Implementation Gotchas

Event queue and unexpected notification space exhaustion at target

- Requires flow control
- Need to preserve RMA ordering

RMA would need to perform ordered tag matching

Adds overhead, could impact performance for small messages

Things that could make this proposal better

- Eliminate returning last source/tag in MPI_Status
- Eliminate unexpected notifications
- Eliminate matching ordering



