```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.all;
library work;
use work.costanti.all;
use work.myfunc.all;

entity Sim_Circ is

end Sim_Circ;

architecture Behavioral of Sim_Circ is
component Complementer is
    Port ( A : in STD_LOGIC_VECTOR (nb-1 downto 0);
           B : in STD_LOGIC_VECTOR (nb-1 downto 0);
           C : in STD_LOGIC;
           Ris : out STD_LOGIC_VECTOR (nb+1 downto 0));
end component;
signal IA, IB:  STD_LOGIC_VECTOR (nb-1 downto 0);
signal IC: STD_LOGIC;
signal ORis, TestRIS: STD_LOGIC_VECTOR (nb+1 downto 0);
begin
  CUT: Complementer port map (IA,IB,IC,ORis);
  process
  begin
    --t=0
    --wait for 110ns; -- attesa per il global reset
    for i in -pow2(nb-1) to pow2(nb-1)-1 loop
        for j in -pow2(nb-1) to pow2(nb-1)-1 loop
            IA<=conv_std_logic_vector(i,nb);
            IB<=conv_std_logic_vector(j,nb);
            IC<='0';
            TestRIS<=conv_std_logic_vector(2*i+2*j,nb+2); -- per debug
            wait for 10ns;
            IC<='1';
            TestRIS<=conv_std_logic_vector(2*i-2*j,nb+2); -- per debug
            wait for 10ns;
        end loop;
    end loop;
  end process;
end Behavioral;
```