```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_SIGNED.ALL;

entity Adder is
    generic (nb: integer);
    Port ( A : in STD_LOGIC_VECTOR (nb-1 downto 0);
           B : in STD_LOGIC_VECTOR (nb-1 downto 0);
           Sum : out STD_LOGIC_VECTOR (nb downto 0));
end Adder;

architecture Behavioral of Adder is

begin
  Sum<=(A(nb-1)&A)+(B(nb-1)&B);
end Behavioral;
```