ME 333 Quiz 3: Chapter 3

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January 27, 2022

Quiz 3

1) **The PIC32 has four types of memory: data RAM, program flash, SFRs, and boot flash. Which is cacheable, which is not? Why?**

   Data RAM, program flash, and boot flash can all be cacheable. However, the PIC32 is configured to access program flash via cache, since flash memory is slow, and RAM without the cache, since RAM is fast. SFRs are not cacheable, since they correspond to physical devices — if they were cacheable, the CPU could read outdated values.

2) **For the following SFR, how many implemented bitfields are there? After reset, which bitfields are initially set?**

   There are **8 implemented bitfields**. 0-3 and 12-15 are initially set after reset (although bit 0 technically doesn't exist). This means the fields that are set include: TRISC1, TRISC2, TRISC3, TRISC12, TRISC13, TRISC14, and TRISC15.

3) **What is the function of the processor.o file?**

   The processor.o file is a model specific mapping of virtual memory addresses to PIC32 SFRs.

4) **The prefetch module has a 128 bit wide path to Flash memory, but the rest of the bus matrix inside the PIC32 is only 32 bits wide. Why?**

   The prefecth module has a 128 bit wide path to flash memory to store sets of instructions prior to the CPU requesting them. This increases performance by allowing the prefetch cache to run ahead of execution despite the slow flash load times. The 128 bit path allows for four sets of instructions to be stored in advance of being requested by the CPU.