

ENERGETIC ELECTRON-INDUCED SINGLE EVENT UPSETS
IN STATIC RANDOM ACCESS MEMORY

By

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For my grandfather, Edward Gray, who was my greatest teacher.

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Chapter 1

Introduction

The ability to store and read information is critical for reliable system operations in modern electronics. Information is stored in densely packed arrays of devices and circuits whose purpose is to maintain mission critical instructions, record data, and return that information for further computation or analysis. Circuit- and device-level memories exist in the form of volatile and non-volatile elements; the static random access memory (SRAM) being a circuit element volatile memory, which is widely used in many applications.

SRAMs, and related memories, are renown for fast read and write times, small areal density, exhibit a non-destructive read operation, and do not require periodic refreshing of data since information persists while the memory is powered. The SRAM represents a stable memory that has become an essential circuit-level cell because it has the ability to rapidly access and store information, making it ideal for low-power and mobile applications as well as microprocessor and system level cache. Radiation sensitivity of circuit-level memory is an important consideration when evaluating reliability concerns of modern technology in a variety of hazardous environments including military, space, nuclear, and the terrestrial level. Single-event upset (SEU) is an example of the sensitivity of modern microelectronics to ionizing radiation. SEUs

are defined as the erroneous change of state of a semiconductor memory, such as an SRAM, resulting from the interaction between ionizing radiation and the sensitive region of the microelectronic element.

The semiconductor industry continues to scale complementary metal-oxide-semiconductor (CMOS) technologies to smaller feature sizes with reduced operating voltages in pursuit of performance and density goals. Continuing decreases in device dimension and operating voltage reduce the critical charge required to produce a SEU, significantly affecting the reliability of modern technologies in space and terrestrial environments. Decreasing critical charge has led to the emergence of SEUs induced by lightly ionizing particles, such as low-energy protons and muons [1, 2]. Traditionally, the primary radiation effects caused by energetic electrons in the trapped radiation environments of Earth and Jupiter were considered to be total-ionizing dose (TID), displacement damage, and spacecraft charging [3, 4]. However, in recent years interest has emerged regarding effects related to the spatial distribution of charge produced by lightly ionizing particles, including high-energy secondary electrons [5–11]. These secondary electrons, also called δ -rays, lose their kinetic energy through ionization, producing electron-hole ($e-h$) pairs that may cause SEUs. Various studies [5–11] have obtained conflicting results in attempts to quantify, primarily via modeling and simulation, the contributions of energetic electrons to the overall upset rate in memories fabricated at advanced technology nodes. Despite extensive efforts, lack of experimental data has left the role of energetic electrons in the SEU response of modern SRAMs an open question.

In this dissertation, a low-energy X -ray source is used to generate energetic, nearly ballistic electrons to evaluate the susceptibility of CMOS SRAMs fabricated in the 28 nm and 45 nm technology nodes to electron-induced SEUs. Throughout this dissertation, “electron-induced SEUs” refer to events in which the initiating particle

is a high-energy electron (δ -ray); the eventual upsets are produced by thermalized electron-hole pairs generated as the δ -rays lose their energy through ionization. Upsets are observed within 10% of nominal supply voltage for the 28 nm technology node. That these memory upsets are indeed electron-induced SEUs is supported by Monte Carlo radiation transport simulations, which show that single energetic electrons deposit sufficient ionizing energy to generate charge in the sensitive volume of the device that is well in excess of estimated critical charge values. The relative importance of electron-induced SEUs is compared to other physical processes, such as direct ionization from low-energy protons [1, 12–14] and muon-induced upsets [2, 15] in determining error rates in 28 nm and 45 nm technology generations. The impact of electron-induced SEU on scaling of feature size and voltage in modern CMOS processes, ultra-low power applications, and error rates in the space radiation environment is discussed in detail.

The organization of this dissertation is as follows. Chapter 2 presents relevant background material including SRAM topology, operation, and stability, radiation effects in SRAMs, and the physics of secondary electron generation and energy deposition. Chapter 3 will show and discuss experimental results of SEUs observed during X -ray irradiation of 28 nm and 45 nm bulk silicon SRAMs. Chapter 4 presents supporting simulation results for the X -ray that show good agreement with experimental results. Error rates are estimated using simulation techniques, the consequences and importance of these results are discussed for the space radiation environment. Analysis of the contribution of δ -rays generated in heavy-ion irradiation to single- and multiple-bit upset rates is also discussed. Finally, Chapter 5 presents conclusions and discusses the significance of these results for modern technology nodes.

Chapter 2

Background

The reliable operation of microelectronic memories is a primary concern for the semiconductor industry. The space radiation environment is complicated by high cost of entry and increased hazards when compared to the terrestrial level, including additional risk of fault or failures in electronics due to the presence of ionizing radiation. The interaction of ionizing radiation with microelectronics in the space environment, and at the terrestrial level, has been observed to cause both temporary and permanent damage to semiconductor devices, circuits, and systems.

This chapter presents relevant background information, including SRAM topology, operation, and stability, radiation effects in SRAMs, the physics of photon–matter interactions, and heavy-ion track structure. A large segment of this chapter focuses on single-event effects (SEEs), specifically SEU, which is the erroneous change of state of an electronic memory due to ionizing radiation depositing energy within the circuit element. In the context of an SRAM cell this corresponds to the change in state of the memory, either from a *0* to *1* state or *1* to a *0* state. The change of information state is due to energy deposited within a sensitive node of an SRAM cell and corresponding device response latching in the erroneous state. For applications in space, SEUs have been attributed to heavy ions from the galactic cosmic ray

(GCR) environment and energetic protons, which can be found in the trapped radiation environments of the Van Allen belts or in the Jovian environment. Traditionally, SEUs in the terrestrial environment are dominated by neutrons and alpha particles emitted by packaging contaminants. The particle species present in the space and terrestrial radiation environment have inherently different interactions with semiconductor devices and consequently differing implications for the reliable operation of memories. The increased cost of entry associated with space applications introduces additional, stringent reliability requirements due to the high risk of mission failure. Higher reliability expectations in the space radiation environment have often required the use of electronic components that are “radiation-hardened” or at best “radiation-tolerant” devices that have increased resistance to the effects of ionizing radiation. Commercial-off-the-shelf parts are appealing to designers as a venue to reduce cost of production and power consumption, however, these trade-offs come with an increase sensitivity to ionizing radiation and consequently mission risk. Conversely in the terrestrial environment, commercial enterprise relies heavily on cloud computing, routers, and servers for computation, transactions, and communications. Faults in these types of systems represent unacceptable losses of time, financial transactions, and connectivity. Understanding the threat and source of reliability concerns is essential for effective mitigation strategies and maintaining stable operation of critical electronic systems.

The following sections address a broad range of topics related to SRAM operation and the effects of ionizing radiation on SRAM cells. Relevant background discussion includes the topology, stability, and operation of the six-transistor SRAM, a basic description of SEUs in SRAMs, including the observation of upsets due to low-energy protons and muons, TID effects on SRAMs, and dose-rate effects on SRAMs. Further discussion will then briefly introduce the physics of photon-matter interactions and

an overview of recent studies regarding the effects of δ -rays on microelectronics.

2.1 Basic SRAM Topology and Operation

As CMOS feature sizes have decreased, a corresponding reduction in areal density of individual memory cells has resulted in lowering of the cost per bit. This has enabled access to low-cost, high-speed memory for many applications. These attributes have made SRAMs ideal for use in microprocessor cache memory, general use registers, FPGAs, and other applications.

While SRAM implementations can be expensive, in terms of area, they are typically more desirable than conventional dynamic random access memory (DRAM) in terms of speed and power consumption. Since an SRAM cell takes up more area than DRAM cell in the same technology node, these benefits come at the expense of increased area and cost. Since SRAM cells do not require the refreshing of data, SRAM implementations offer significant advantages over DRAM in terms of power consumption. SRAMs are ideal where bandwidth, power, or both are a primary design consideration.

The basic topology of a standard six transistor (6T) SRAM can be seen in Fig. 2.1. While other SRAM implementations are possible, including non-volatile topologies, this dissertation only considers the standard 6T SRAM cell. The basic SRAM cell stores information on two cross-coupled inverters, consisting of four transistors (M1–M4), that form a basic latch, enabling the stable states of either 0 or 1. Two additional access transistors (M5 and M6) allow access operations, primarily read and write, to the SRAM cell. An SRAM cell has three standard modes of operation, write, read, and standby. A write operation occurs by applying a voltage to the bit line and its complement (BL and \overline{BL}) and asserting the word line. The voltage applied to the bit lines should have a large potential difference such that the state is quickly reinforced

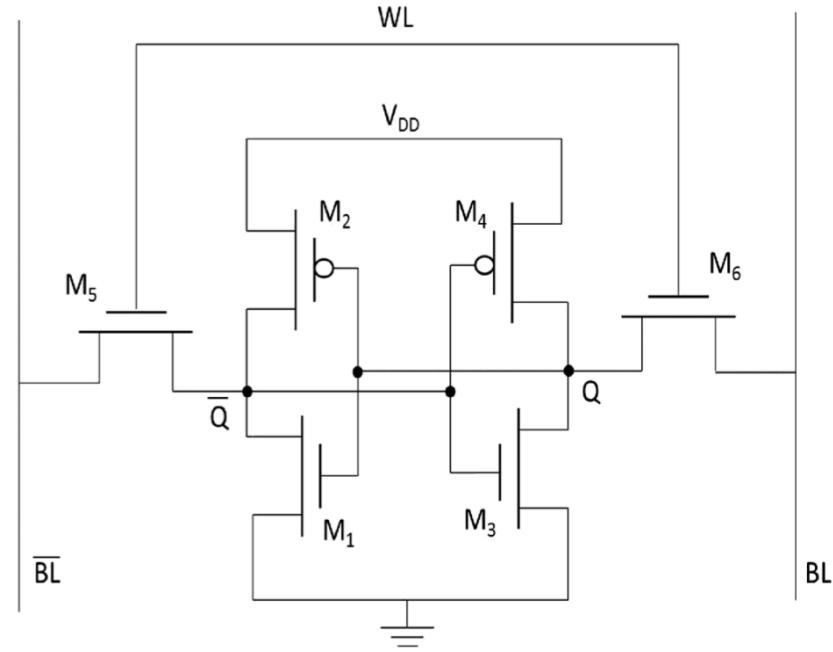


Figure 2.1 Basic SRAM circuit topology consists of two cross coupled inverters and two access transistors.

by the two inverters. A potential difference close to the supply voltage (V_{DD}) is quite common in standard technology implementations. A read operation occurs when the bit lines are left floating while the word line is asserted. Using peripheral circuitry (not shown), a high-speed sense amplifier compares the voltage difference between the bit line and its complement and outputs the state of the cell to subsequent buffers and is then passed to the output bus. Standby mode occurs when the word line is left floating, during which time the access transistors are “off” and the inverters continually reinforce the present state of the SRAM cell. Standby mode is the “idle state” of any SRAM cell and results in the lowest power consumption of all stable SRAM operating modes. A common practice to lower power consumption while operating in standby mode is to reduce the supply voltage to the SRAM below the nominal supply voltage. This is a method known as dynamic voltage, frequency scaling at the systems level and is used to reduce power consumption when operating frequency is

a secondary priority [16, 17]. The trade-off is typically made in applications where low-power is a primary operating parameter such as medical implant devices, mobile communications, and mobile computing. For these applications SRAMs are designed to remain stable and completely functional at 70–80% of the nominal supply voltage while maintaining valid information.

While both bit lines are not required for proper SRAM cell operation, utilizing both the bit line and its complement increases the circuit's noise margin and results in increased read and write speed. Fig. 2.2 shows the transfer characteristics for

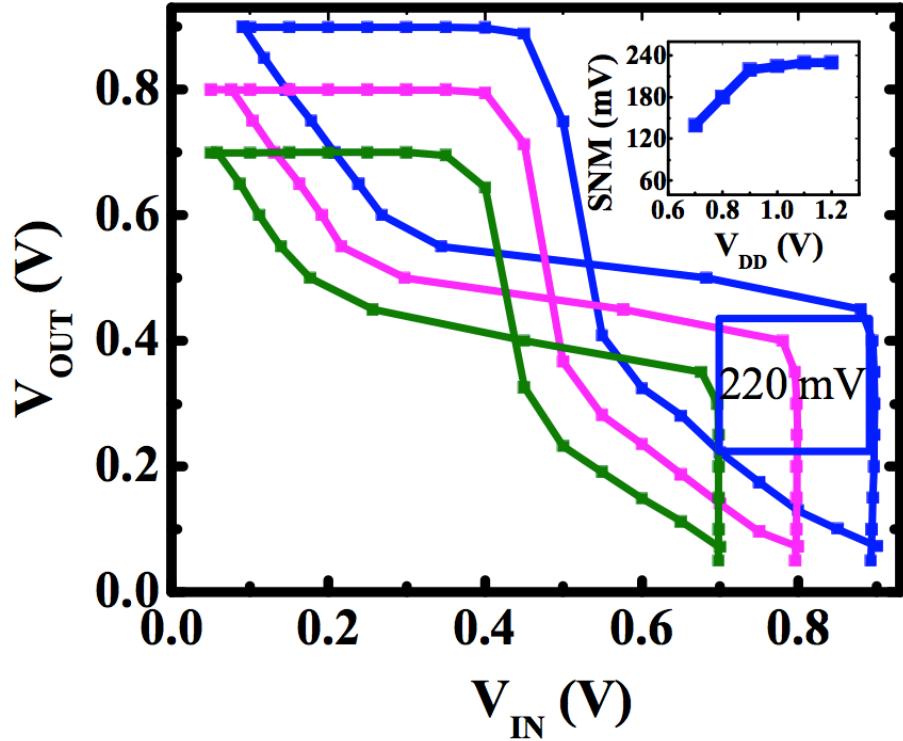


Figure 2.2 Butterfly curves for $0.1 \mu\text{m}^2$ 6T-SRAM cell showing SNM of 220 mV, 180 mV and 148 mV at $V_{dd}=0.9$, 0.8 and 0.7 V respectively [18].

a functional 22 nm SOI SRAM from [18]. The static noise margin (SNM) of an SRAM cell is the side-length distance, given in millivolts, of the difference in transfer characteristics for the high and low state of the cross-coupled inverters. The stability

of an SRAM cell is generally described in terms of the SNM, which is the *DC* noise an SRAM cell can tolerate while maintaining its intended state. Exceeding the SNM for an SRAM cell results in a change of state and results in an error. Fig. 2.2 shows the SNM of the cell depends on the supply voltage, with lower V_{DD} corresponding to a smaller SNM. Similarly, the switching voltage, the input voltage where the state of the SRAM cell changes from a 1 to 0, or vice versa, also depends on the supply voltage. The decrease in switching voltage and SNM under reduced supply voltage conditions effectively increases the sensitivity of SRAM cells to errors from dynamic disturbances caused by ionizing radiation, crosstalk, voltage supply ripple, and thermal noise.

2.2 Radiation Effects on SRAM

This section deals with the broad topic of radiation effects in SRAMs. Initially, an introduction to SEUs is made, focusing on historical methods of understanding, modeling, and analyzing SEU data. The concept of critical charge is defined for the purpose of understanding the analysis and methods in Chapters 3 and 4. Recent studies detailing the observation of low-energy proton- and muon-induced upsets will be discussed, emphasizing the trend towards increased sensitivity in modern devices. The effects of TID on SRAMs will be introduced with the primary example being the “memory pattern imprinting” effect. Relevant issues related to transient radiation environments, so-called dose-rate effects, will also be introduced.

2.2.1 Single-Event Upset in SRAMs

Energetic particles passing through material lose energy to the target medium through electronic and nuclear processes. The electronic component consists of energy loss due to interaction with the electron gas, comprised of valance band electrons, in the target medium. Energy loss by the incident ion results in generation of mobile carriers in

the conduction band and valance band, known as *e-h* pairs. Electron-hole pairs in the presence of an electric field contribute to a current transient whose magnitude and duration is determined by the amount of charge generated in the depletion region by the incident ion. In the context of an SRAM, the largest electric fields are located in the reverse biased *pn* junctions present in each of the cross coupled inverters. To first order, the sensitive region of a CMOS SRAM may be considered the two reverse biased junctions of the *off*-state transistors shown in Fig. 2.1. The amount of charge generated by the passage of a incident ion through an sensitive region of a semiconductor memory is related to the average energy required to generate a single *e-h* pair, in silicon this energy is 3.6 eV. In this sense, the energy lost by an incident particle is correlated with the amount of charge generated within the semiconductor device material. The rate of energy lost per unit path length by an incident ionizing particle is described by its linear energy transfer (LET), which is represented in units of MeV-cm²/mg. SEU cross-sections have typically been analyzed as a function of incident ion LET based on the assumption that knowledge of the average interaction is sufficient to predict the event response, and subsequently, the error rate in the environment of interest.

As an example, Fig. 2.3 demonstrates the concept of critical charge, or the magnitude of charge collection required to induce an upset in an SRAM. Two transients are shown in Fig. 2.3 with different amounts of total charge being collected and the resulting transient on the output of the off-state transistor in an SRAM cell. The top image shows a transient corresponding to 0.23 pC of charge collection within the SRAM cell. The state of the cell is temporarily perturbed, however, the resulting transient is insufficient to cause the SRAM cell to latch into an erroneous state.

In the bottom image, the transient shown corresponds to 0.25 pC of charge collected in the SRAM cell. While the magnitude of charge collection differs by only

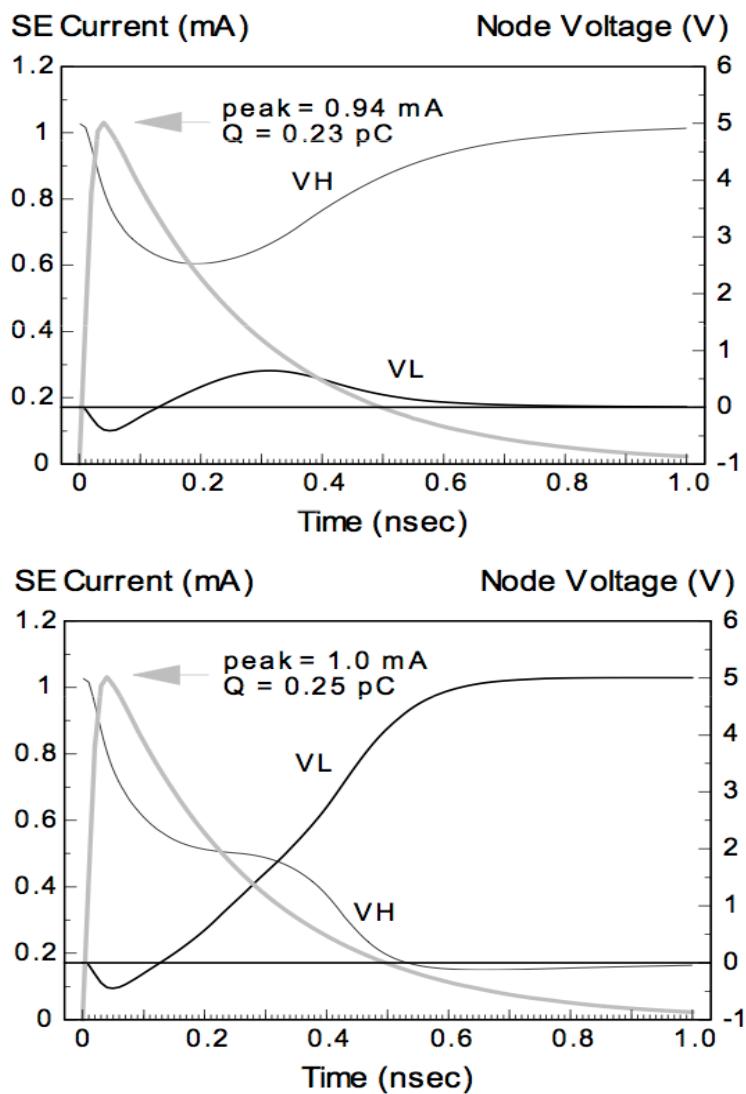


Figure 2.3 Current transients in an SRAM cell demonstrate the concept of critical charge. The transient corresponding to 0.23 pC of charge collection is insufficient to cause the SRAM cell to latch into an erroneous state. However, when the amount of collected charge is increased to 0.25 pC the resulting transient is latched into the SRAM cell, resulting in an error.

0.02 pC, the resulting circuit response is dramatically different. The resulting transient is of sufficient magnitude and duration to latch an erroneous state into the SRAM cell, resulting in an error. The critical charge of this SRAM cell would therefore be defined to be 0.25 pC since a typical SRAM cell response for the corresponding technology node would result in an error. There are many nuances and specific details that may impact the error margins for determining critical charge such as corner to corner variations, magnitude and duration of the transient pulse, and charge collection efficiency of carriers in depletion regions. However, Fig. 2.3 is intended solely to convey the concept of critical charge, which is defined in this dissertation as a single valued metric for determining the energy deposition threshold for the onset of errors in an SRAM cell. We will see that the magnitude of charge collection shown in Fig. 2.3 is extremely large when compared to the critical charge for sub-65 nm technology nodes.

In [19], Sierawski attempted to estimate the critical charge for several current- and next-generation technology nodes, the resulting calculations can be seen in Fig. 2.4. Using SPICE simulations and injecting current pulses of varying magnitude and duration Sierawski was able to obtain an upper bound for critical charge. The lower bounds were obtained by extracting process details from the ITRS road map [20] and applying the following relation,

$$Q_{crit} = \frac{V_{DD}}{2} \frac{\epsilon_{SiO_2} \epsilon_0 A_{cell}}{t_{ox}} \quad (2.1)$$

where V_{DD} is the supply voltage for the technology node, ϵ_0 is the permittivity of free space, ϵ_{SiO_2} is the relative permittivity of SiO_2 , A_{cell} is the cell area, and t_{ox} is the equivalent SiO_2 oxide thickness for the technology node. Fig. 2.4 shows an overall decrease in critical charge with decreasing technology node feature size. These conclusions are consistent with publications that indicate the critical charge of 65 nm

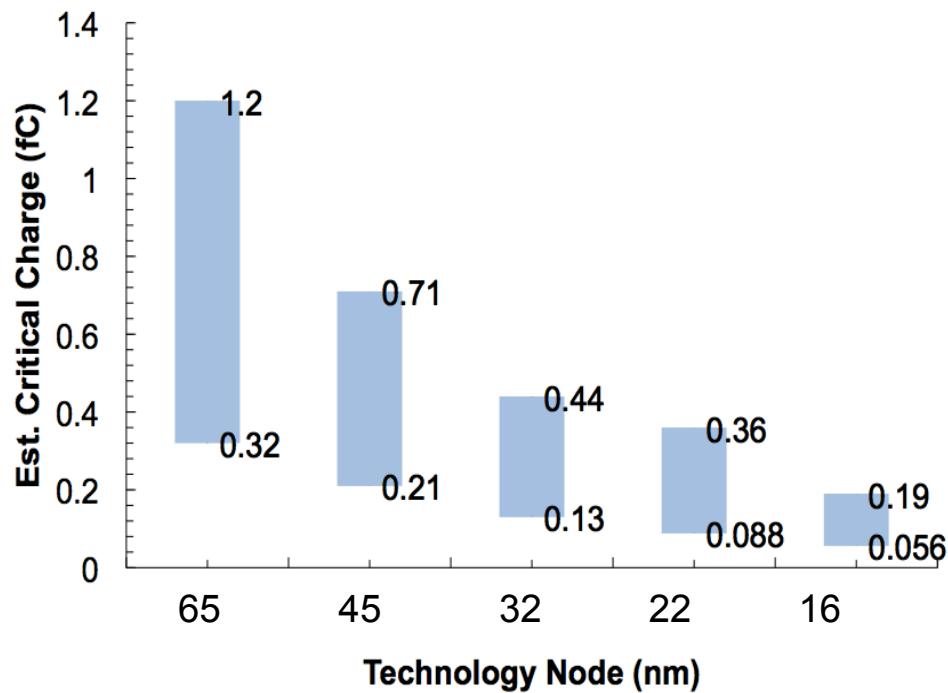


Figure 2.4 Estimation of critical charge as a function of technology node feature size [19].

silicon-on-insulator SRAMs is between 0.21 and 0.27 fC [1].

While much of the energy lost by the incident ion results in the generation of $e\text{-}h$ pairs by direct ionization, secondary particles also deposit energy in regions surrounding the incident ion path and have been predicted to contribute to the SEU response. The secondary particles of concern are generated by incident particles through either nuclear or Coulomb interactions. Several of the more common secondary particles are referred to in literature as δ -rays, which are energetic secondary electrons, Coulomb scatters, which are displaced atoms from the crystal lattice, and nuclear interactions including spallation, elastic, and inelastic events. The generation of δ -rays will be discussed thoroughly in Section 2.4.

In 1988, Stapor *et al.* illustrated the potential for differences in the response of microelectronics for two incident ions with similar LET due to differences in the resulting energy deposition profiles [21]. These conclusions were supported by analyzing the transient response of devices to ions having the same LET but different energies in [22]. Similar conclusions were reached by Weller and Kobayashi in previous work that illustrated the importance of energy deposition profiles for proton and alphas in determining the device response to ionizing radiation [5, 23].

The LET metric has been robust and effective for understanding and modeling the SEU response of SRAMs for many years and continues to serve as the basis for the majority of SEE analysis [24–26]. The application of LET to SEU/SEE analysis relies on the assumption that knowledge about the average energy deposition event is sufficient to predict the event response. In recent years however, additional physical mechanisms have been required to explain SEU cross sections where LET alone has been insufficient [27–31]. With the observation of low-energy proton- and muon-induced SEUs the trend towards increased device SEU sensitivity to ionizing radiation is indeed following the trends shown in Fig. 2.4 and does not appear to be slowing.

2.2.2 Low-Energy Proton-Induced SEUs

The primary effects due to incident protons on microelectronics in the space radiation environment have *historically* been displacement damage and TID. In addition, nuclear spallation reactions were observed to contribute to measured SEU cross-sections [12]. The contribution of protons to upset cross-sections due to direct ionization has traditionally been ignored since the electronic stopping power of protons is quite small. However, a series of papers demonstrated protons near their end of range were capable of generating sufficient charge to upset SRAMs and latches fabricated in a 65 nm node [1, 12–14, 32].

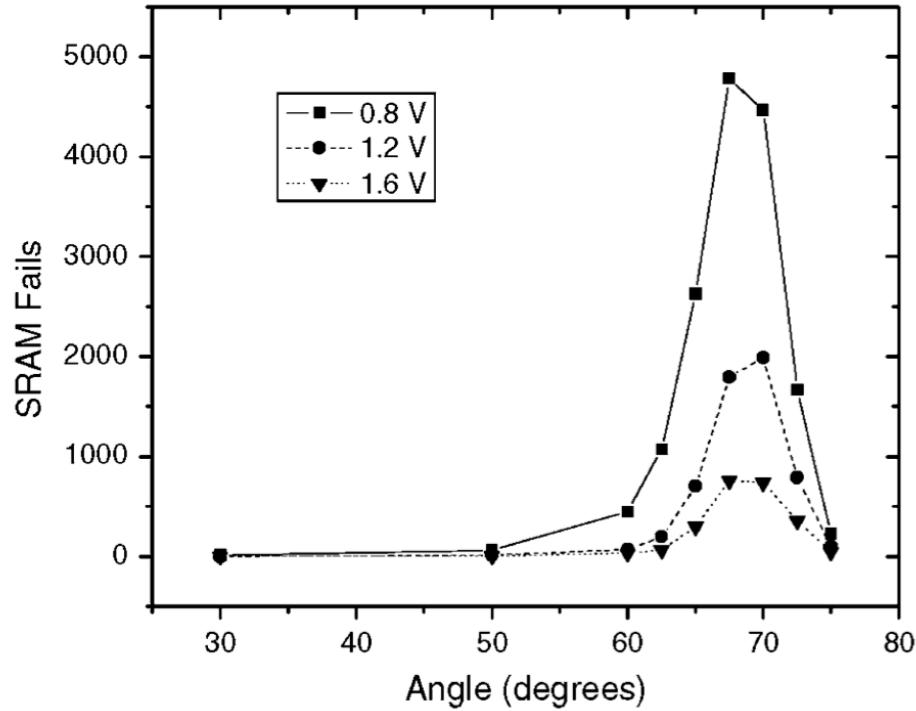


Figure 2.5 SRAM fails (an average of write 1 and write 0) as a function of the incident angle for an SRAM array at 0.8 V, 1.2 V and 1.6 V using 1.5 MeV protons [1].

The Bragg peak for protons occurs near their end of range, implying that protons

near stopping have a maximum LET. By exposing SRAM and latches to a source of low-energy protons, in the energy range of 1-2 MeV, Heidel and Rodbell were able to show that proton-induced direct ionization can cause upsets in SRAMs fabricated in 45 nm and 65 nm technology nodes [1, 13, 32]. Because SOI technology has a large angular dependence [27], proton direct ionization effects were confirmed by performing experiments at large angle of incidence. Rotating parts using a goniometer in order to test parts at large angle of incidence, where a beam normally incident on the device under test is considered to be 0° , resulted in an increased upset rate. This is due to an increased path length for incident protons through the active region of the test chip, corresponding to more energy deposited within the sensitive region of the SRAM [32].

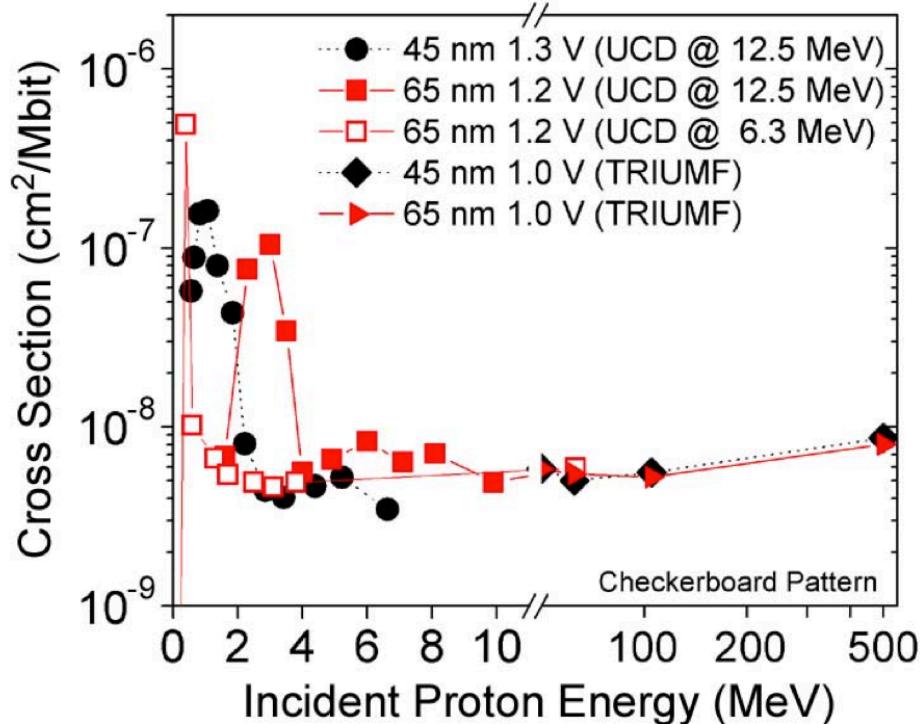


Figure 2.6 The SBU cross section versus proton energy for both 45 nm and 65 nm SOI SRAMs [13].

Fig. 2.6 shows the proton SEU cross-section as a function of incident proton energy for 45 nm and 65 nm SRAMs. For very energetic incident protons (>10 MeV) upsets can be attributed to nuclear reaction events. In this energy range, the SEU cross-section remains fairly constant. As the incident proton energy is reduced (<5 MeV) the measured upset cross-section begins to increase, corresponding to the protons with sufficient LET to upset the device under test. Incident proton energies between 1-4 MeV correspond to a “plateau” in the measured upset cross-section. In this region, the upset cross-section is two orders of magnitude higher than the high-energy proton cross-section and corresponds to a region where most of the incident protons are near their end of range. Decreasing the incident proton energy further results in a reduced SEU cross section. This is due to a corresponding reduction in the range of incident protons and prevents protons from transporting into the sensitive region of the device with sufficient energy to impact the SRAM cells nominal operation.

Closer study of Fig. 2.6 shows that multiple supply voltage conditions were used while performing the initial low-energy proton experiments. The sensitivity of SRAMs to low-energy protons was initially observed under reduced bias conditions at high angle of incidence [32]. Further study showed sensitivity of 45 nm SRAMs at normal incidence and under nominal bias conditions [1, 13]. A plot showing the SEU cross-section dependence on applied bias, in arbitrary units, can be seen in Fig. 2.7 for 1 MeV and 1.5 MeV protons (also more energetic alpha particles are shown). A gentle gradient can be observed in the SEU cross-section for low-energy protons (the curve corresponding to 1 MeV protons) as a function of applied bias. Recalling the discussion regarding Eq. (2.1), the critical charge of elementary 6T-SRAM cell should depend on the supply voltage. Here the bias dependence manifests as a linear slope (although significantly less than unity) in the measured SEU cross-section. Heidel and Rodbell both reported the critical charge for SRAMs fabricated in the 65 nm SOI

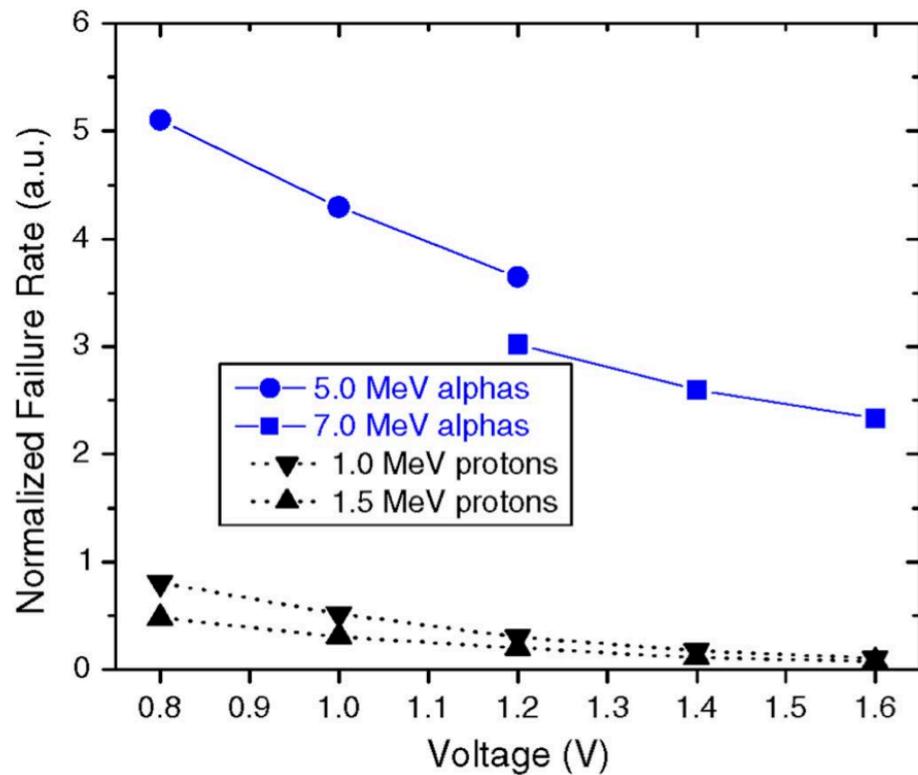


Figure 2.7 Plot of the SRAM SEU cross-section (in arbitrary units) as a function of voltage for 5.0 MeV and 7.0 MeV alpha particles and for 1.0 MeV and 1.5 MeV protons [1].

technology node to have a critical charge between 0.21 fC and 0.27 fC [1, 32]. The values of critical charge from [1, 32] are consistent with the estimations for SRAMs in the 65 nm technology node made by Sierawski and shown in Fig. 2.4. Interestingly, the reported values of critical charge correspond to 1300-1700 collected electrons. The observation of effects from low-energy protons signifies a noteworthy shift in the sensitivity of modern (here modern is taken to be sub-65 nm technology nodes) SRAMs.

These results primarily impact the space radiation environment, where energy loss through spacecraft shielding can shift the differential flux spectrum of protons towards lower energies, where direct ionization effects begin to contribute to the SEU cross-section and error rates [14]. Nuclear reactions involving more energetic protons and/or the heavy ions from the galactic cosmic ray environment also result in the generation of large numbers of protons [1]. The contribution of low-energy protons also extends to the terrestrial environment where neutron-induced spallation reactions produce a substantial number of low energy protons [1].

2.2.3 Muon-Induced SEUs

Wallmark and Marcus performed a preliminary analysis of the fundamental limitations of microelectronics and highlighted ionizing radiation particles, chiefly amongst these were terrestrial muons and electrons, as the principal factors that would impact the continued reliable scaling of semiconductor devices and technology [33]. Additional analysis regarding error rates and the sensitivity of SRAMs was performed by Ziegler *et al.* The results of that work suggested that the continued scaling of CMOS memory would result in a substantial increase in the sensitivity of SRAMs to ionizing radiation with continued device scaling and result in a large soft-error rate for the space and terrestrial radiation environments [34].

Research has shown commercial SRAMs are vulnerable to low-energy proton induced SEUs due to the relatively small critical charge required to cause an error in modern SRAMs. This revelation has changed the way the radiation effects and reliability community view lightly ionizing radiation. Contributions of low-energy protons to upset cross-sections, as discussed previously, were traditionally ignored, they are now being considered as a real and significant reliability concern. For many years, the presence of atmospheric neutrons and alpha particles (largely the result of packaging impurities) presented the only feasible source of soft errors at the terrestrial level. Muons, the most abundant species at the terrestrial level, have recently been shown to induce SEU in sub-65 nm SRAMs [2, 15, 19].

Like protons, muons are singly charged particles with a mass roughly 200 times that of the electron mass. Fig. 2.8 shows the stopping power, or mass stopping

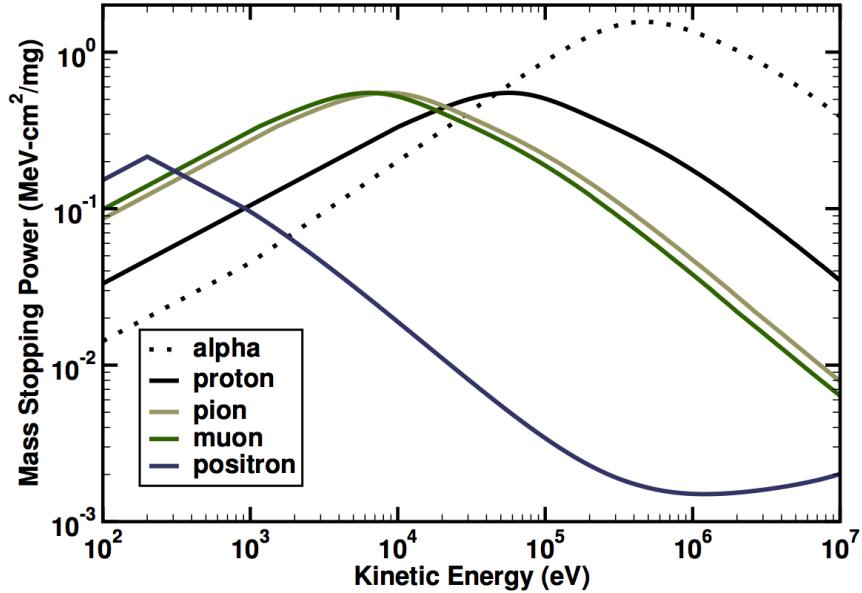


Figure 2.8 Mass stopping power extracted from Geant4 for protons, pions, muons, and positrons in silicon. Alpha particle stopping power shown for reference [15].

power, the rate of energy loss per unit path length, for a variety of particle species.

The curves for protons and muons are similar having a comparable magnitude. The difference in the stopping power curves is due to the lower mass of the muon when compared to that of protons. This parallel indicates that the energy deposition from stopping muons would be comparable to that of low-energy protons. By induction, muons could therefore contribute to the soft error rate, particularly in the terrestrial environment, of SRAMs that exhibit sensitivity to low-energy protons.

Sierawski *et al.* demonstrated that stopping muons were indeed capable of upsetting SRAMs fabricated in the 65 nm technology under reduced bias conditions [2]. Fig. 2.9 plots the muon-induced upset cross-section as a function of incident muon energy. The characteristics of Fig. 2.9 are quite similar to low-energy proton SEU cross-sections. There is a flat region corresponding to the most energetic muons and as the incident muon energy is reduced there is an abrupt increase in the SEU cross-section. Further reductions in incident muon energy result in particles with insufficient range to reach the sensitive region of the SRAM. Consequently, the lowest energy muons do not contribute to the upset cross-section.

Fig. 2.10 shows the SEU response of a 65 nm SRAM as a function of supply voltage for incident muons with average energy of approximately 400 keV. For a nominal supply voltage of 1.2 V, few errors are observed. As the applied bias is reduced, there is a corresponding increase in the number of muon-induced upsets. As discussed regarding Eq. (2.1) and the bias dependence of low-energy protons in Section 2.2.2, reduction in supply voltage results in a corresponding reduction in critical charge. Consequently, reduction in critical charge with decreasing supply voltage makes the SRAM test chip vulnerable to a wider range of incident muon energies, which explains the bias dependence shown in Fig. 2.10.

The impact of muon-induced SEUs parallels that of effects due to low-energy protons. The contribution of each has traditionally been considered negligible to the

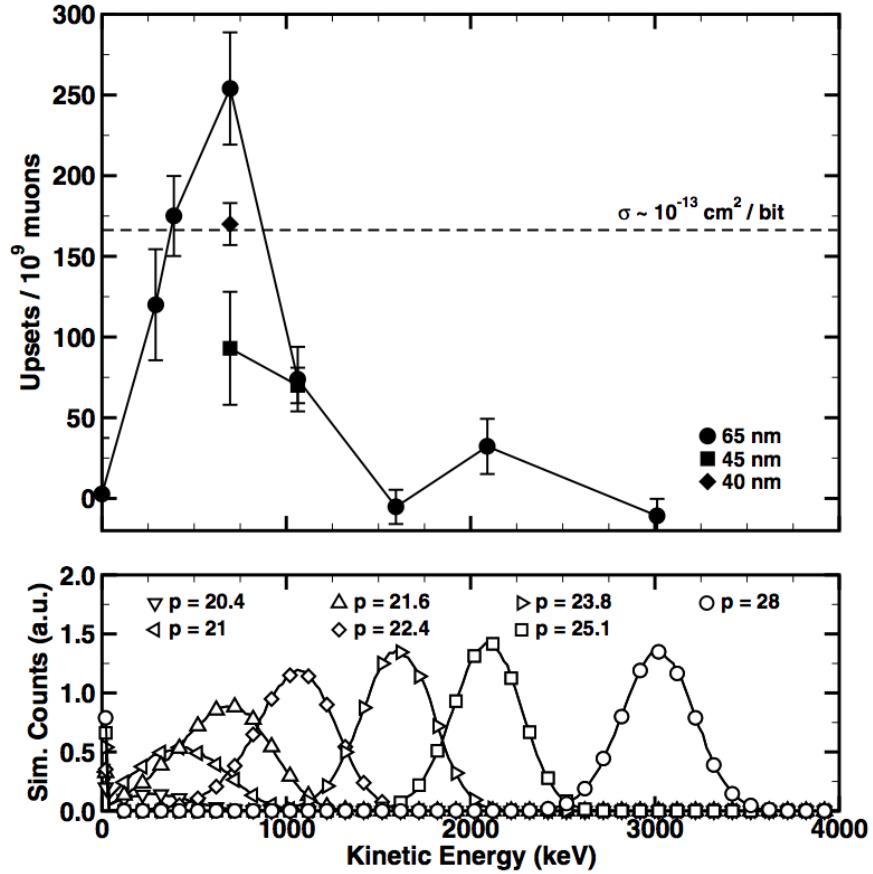


Figure 2.9 Simulated muon kinetic energy distributions, as seen at the front of the part, corresponding to experimental momenta including upstream energy losses and straggling (bottom). Error counts for 65 nm, 45 nm, and 40 nm SRAMs versus estimated muon kinetic energy at 1.0 V bias (top). Dashed horizontal line represents an approximate muon-induced SEU cross section for reference [2].

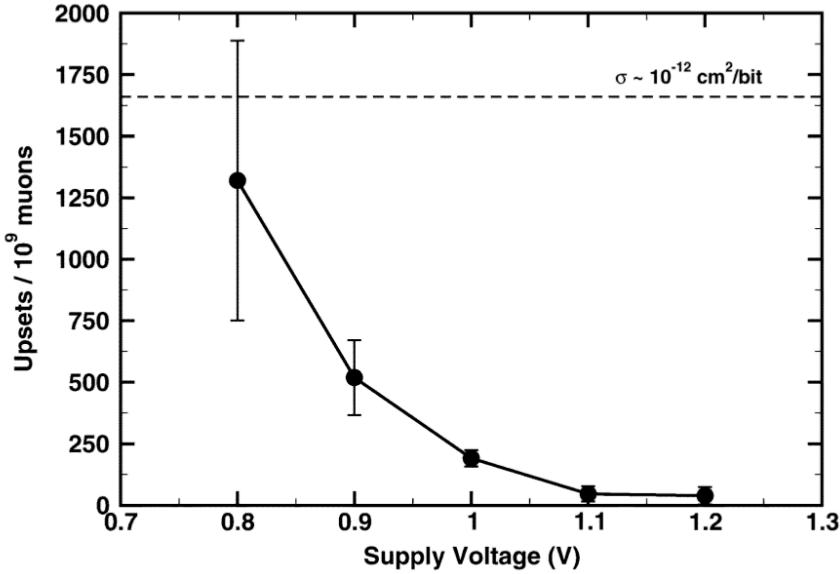


Figure 2.10 Error counts for 65 nm SRAM versus supply voltage for approximately 400 keV muons produced by 21 MeV/c momentum selection. Dashed horizontal line represents an approximate muon-induced SEU cross section for reference [2].

overall SEU cross-section and/or SER of modern SRAMs and has only recently been observed to contribute to error rates. Ultimately, the observation of upsets due to low-energy protons and muons signal that commercial SRAM components are becoming increasingly sensitive to effects from a wider range of ionizing particle species.

2.2.4 SRAM Cell Imprinting

CMOS devices exposed to ionizing radiation can experience threshold voltage shifts and decreased carrier mobility as a result of accumulated dose in oxides and the formation of interface traps [35–38]. The severity of radiation induced degradation in devices is a complicated interaction dependent on the bias conditions during and after exposure. Because the drive strength of *n*-channel MOSFETs is much higher than *p*-channel devices, the total-ionizing dose (TID) response of CMOS SRAMs depends strongly on parametric shifts in the *n*MOSFET device elements [39, 40].

While process hardening efforts may improve the circuits tolerance to TID, designs may still experience functional failure due to speed and timing degradation [40, 41].

Radiation induced threshold voltage shifts in the *n*MOSFET elements of CMOS SRAMs were initially reported to cause an imbalance in device turn-on voltages [42]. The data state of an SRAM establishes bias conditions for the transistor elements of the cross-coupled inverter when exposed to a source of ionizing radiation. The resulting cell imbalance of *n*MOSFET threshold voltages causes an asymmetry in switching voltage and SNM that is dependent on the stored data state of the cell. Fleetwood *et al.* published a study seeking to quantify the “worst-case” SRAM radiation response by evaluating each possible bias condition. In [40], the bias conditions

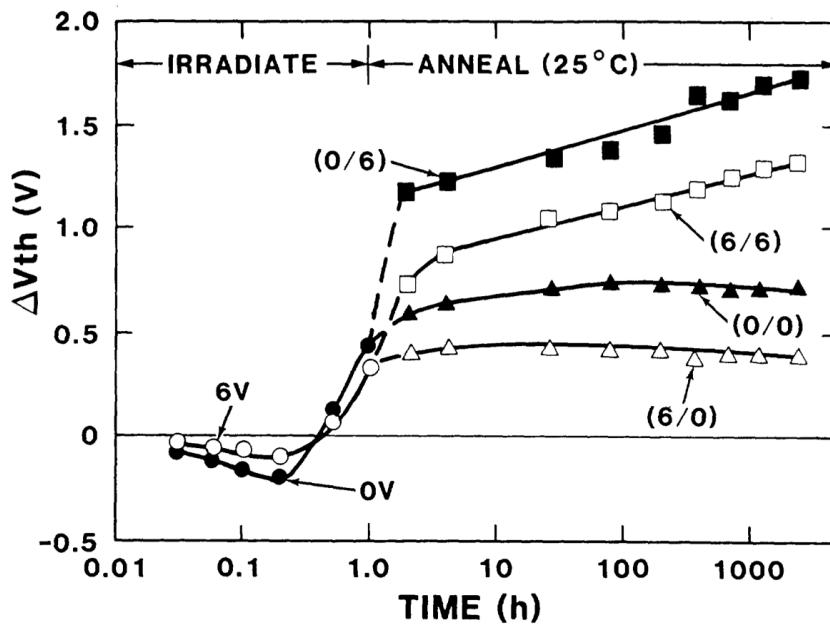


Figure 2.11 ΔV_{th} versus time, for *n*-channel transistors irradiated to 1.0 Mrad and annealed at 25°C [40].

are evaluated to a total dose of 1 Mrad(Si) and the results can be seen in Fig. 2.11. During irradiation the initial threshold voltage shift, for both the “on” and “off” conditions, is negative, consistent with the build-up of charge in the gate oxide region

[35,36]. For consistency, the *1* state of the SRAM cell is defined to be when Q is low, that is when the transistor M3 of Fig. 2.1 is “on”. Fig. 2.11 indicates that the devices irradiated in the “off” state experience a larger threshold voltage shift than those irradiated in the “on” state. Additional exposure of the *n*-channel devices shows a rebound effect, which is attributed to the accumulation of interface traps that very quickly begin to dominate the device response [36,37]. Fig. 2.11 shows that the accumulation of interface traps continues even after irradiation, resulting in large, positive threshold voltage shifts for each bias condition.

The threshold voltage imbalance, V_{imb} , induced by bias conditions during irradiation can be quantified as

$$V_{imb} = V_{TM1} - V_{TM3} \quad (2.2)$$

where V_{TM1} is the *n*MOSFET transistor with the largest threshold voltage after irradiation and V_{TM3} has the less positive threshold voltage. As defined in Eq. (2.2), a positive value of V_{imb} implies a preferred *1* state for the SRAM cell. Conversely, a negative value of V_{imb} implies a preferred *0* state for the cell.

A plot of threshold voltage imbalance versus irradiation and annealing time from [40] can be seen in Fig. 2.12 for conditions where the cell is initially in a *1* state during irradiation and the cell state is either retained, rewritten, or power is removed from the cell during annealing. Initial reports indicated that the SRAM cell was “imprinted” and the preferred state exclusively became that which it was irradiated under, however, Fig. 2.12 shows an initial preference for the *0* state when the programmed pattern was the *1* state. The preferred state of the SRAM therefore depends on bias conditions during irradiation and total dose accumulated [40]. Cells irradiated in the *1* state and annealed in the *0* state show the strongest preference for the *1* device state. These bias conditions correspond to the largest positive threshold voltage shift in M1 and the least positive threshold voltage shift in M3, as shown in

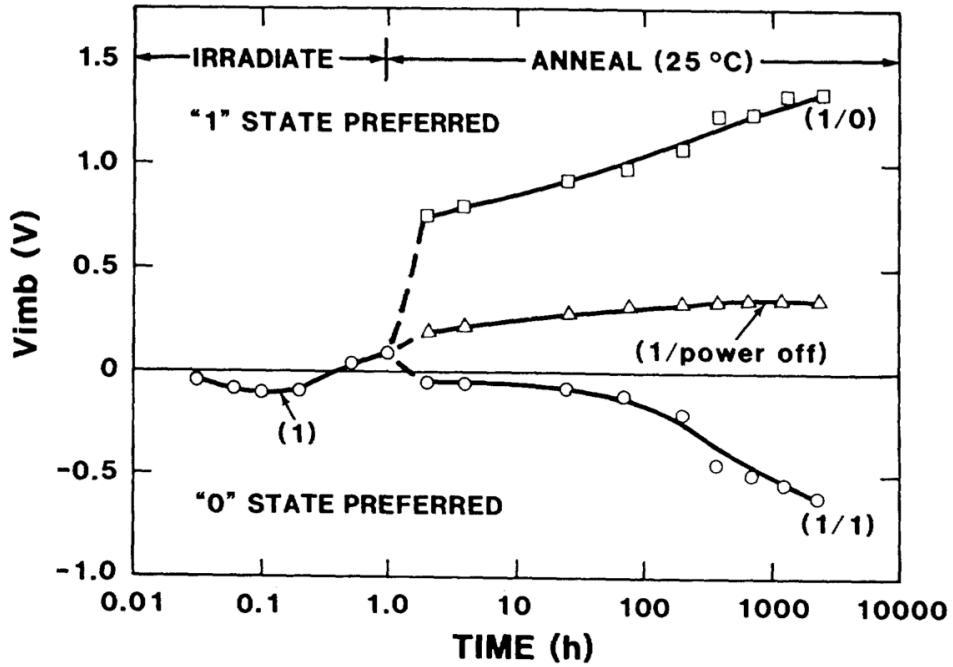


Figure 2.12 SRAM cell imbalance versus radiation and anneal time, based on the data of Fig. 2.11.

Fig. 2.11. These conditions result in the largest speed and timing penalty, as well as the largest SRAM cell imbalance and are considered the “worst-case” conditions for TID in SRAMs.

The speed, timing degradation, and SRAM cell imbalances described above contribute to increased leakage current and functional failure of the SRAM cell. Aggressive scaling of CMOS features size has resulted in a decrease in gate oxide thickness. The magnitude of threshold voltage shifts observed in more modern technology nodes has reduced relative to nominal supply voltage. For a highly optimized process, even small changes in operating points can be a significant issue, in this case however, scaling has improved commercial CMOS tolerance to TID [41, 43]. Investigations by Felix and Yao have studied TID effects on more recent commercial CMOS SRAMs and conclude that below 90 nm SRAMs are highly resistant to “pattern imprinting”

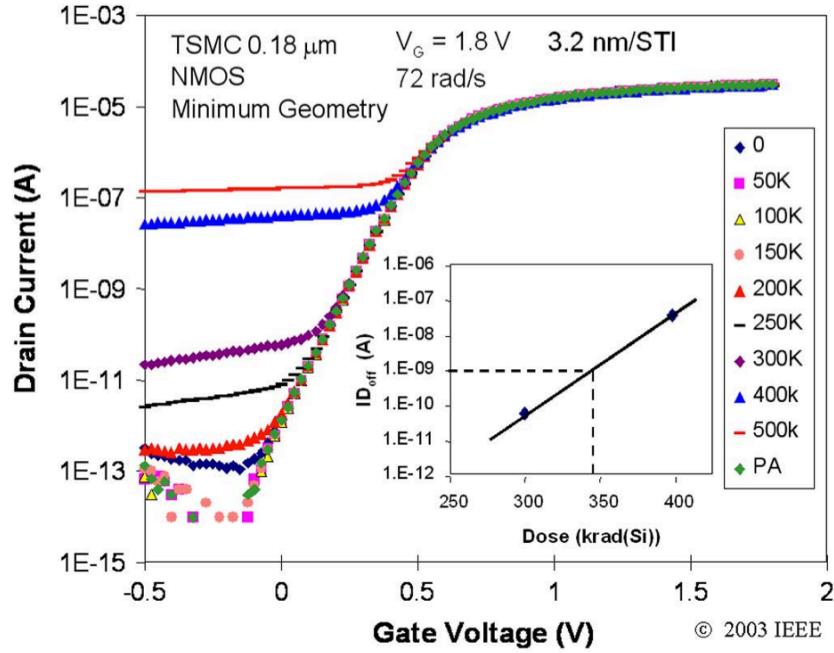


Figure 2.13 Impact of STI radiation damage on the current-voltage characteristics of n MOSFET fabricated in TSMC 0.18 μ m CMOS [43]

effects [41, 44, 45]. Along those lines, functional device failure at the 130 nm node did not typically occur until 200-400 krad(SiO_2) of dose accumulated within the device. The failure mechanism was no longer reported to be threshold voltage shifts and mobility degradation, but increased sidewall leakage at the shallow trench isolation (STI)-silicon interface, an issue that has become increasingly problematic for current-generation technology nodes [41, 43]. Accumulation of charge in the STI activates a parasitic sidewall transistor along the edge of the device acting as a constant bias condition that may deplete or, given sufficient dose, invert nearby active silicon resulting in a static increase in leakage current. The impact of charge build up in STI on transistor I - V characteristics is shown in Fig. 2.13. It is important to note the lack of threshold voltage shift in Fig. 2.13, instead a semi-static leakage increase is seen in the “off” region of the n -channel device, effectively swamping the device response at sufficiently high dose and reducing the on/off current ratio by many orders of magni-

tude. This is problematic for present-generation technology nodes because increased leakage currents can interfere with proper pre-charging and small signal development on bit-lines [44].

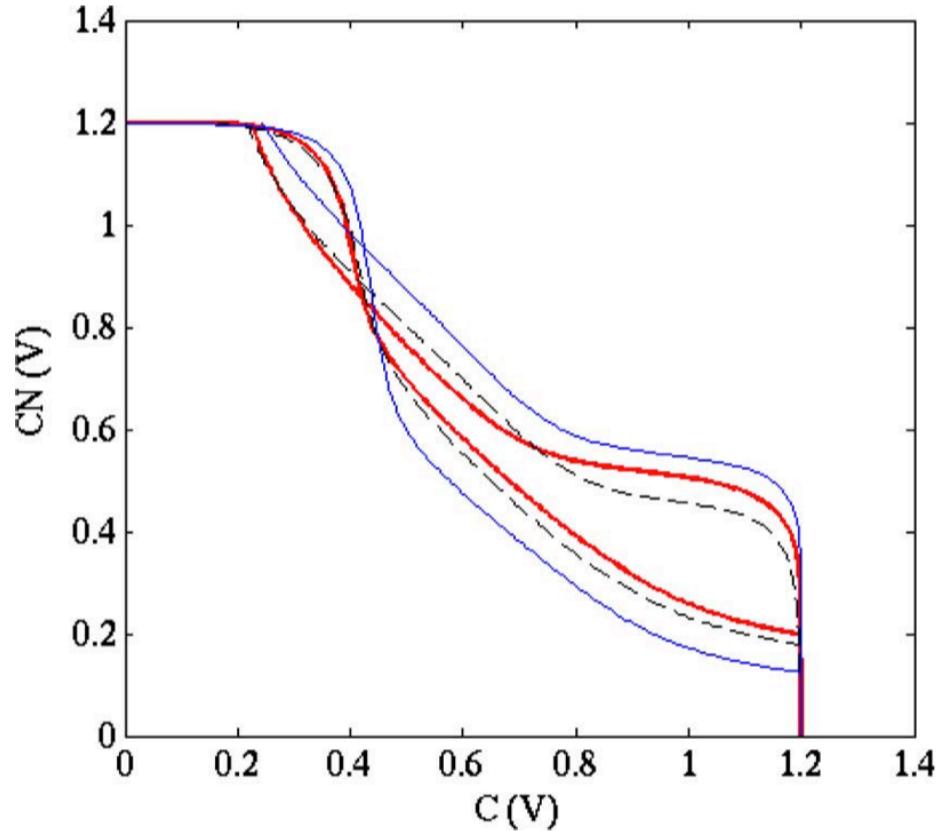


Figure 2.14 Worst-case Monte Carlo derived read SNM pre- and post-irradiation. The thin blue and dashed green lines show the post-irradiation SNM, while the thick red lines show the pre-irradiation response. The worst-case, i.e., the smallest box that fits within the “eyes” is improved after irradiation [44].

As a consequence of degraded speed, timing, threshold voltage imbalances, and increased leakage, irradiated SRAMs exhibit reduced SNMs and have been reported to have increased sensitivity to SEU from heavy-ion and transient irradiation [40, 41, 44, 46, 47]. In [44], the 90 nm technology node did not exhibit a significant increase in supply current until approximately 300 krad(Si). This is also the point at which “im-

printing” began to become significant across the entire test chip. Despite a dramatic increase in supply current, the devices were reported to remain completely functional while maintaining the programmed state to a total dose of 1 Mrad(Si).

Yao *et al.* used Monte Carlo simulations to infer the change in inverter transfer characteristics as a result of TID in a 90 nm technology node, which can be seen in Fig. 2.14. The thin blue and dashed green lines show the post-irradiation SNM, while the thick red lines show the pre-irradiation response. The worst-case, i.e., the smallest box that fits within the “eyes” is improved after irradiation. The transfer characteristics shown in Fig. 2.14 are drastically different from the symmetric response discussed previously regarding the 22 nm node and shown in Fig. 2.2. Fig. 2.15 shows the pre- and post-irradiation SRAM cell switching points for the bit-line and bit-line complement. The pre-irradiation data show a very symmetric, balanced cell response, indicating that neither cell state is preferred by the SRAM cell. After exposure to 1.5 Mrad(Si) the characteristics shift forcing the cell into an asymmetric state where the BL is easier to write than the \overline{BL} . Within some margin this effectively constitutes functional SRAM cell failure, where it becomes nearly impossible, or at least exceedingly difficult, to read or write an SRAM cell and maintain valid data in the standby mode.

2.2.5 Impact of Transient Radiation on SRAMs

When semiconductor materials are exposed to high-intensity, penetrating radiation, such as X -rays or γ -rays, e - h pairs are generated that may be collected and contribute to the cumulative photocurrent. Photocurrents arise from high-flux irradiation conditions, such as those obtained from flash X -ray and pulsed reactor sources, and are “global” currents resulting from irradiation across an entire chip. Because generated photocurrents are “global”, every device on a common substrate will contribute to

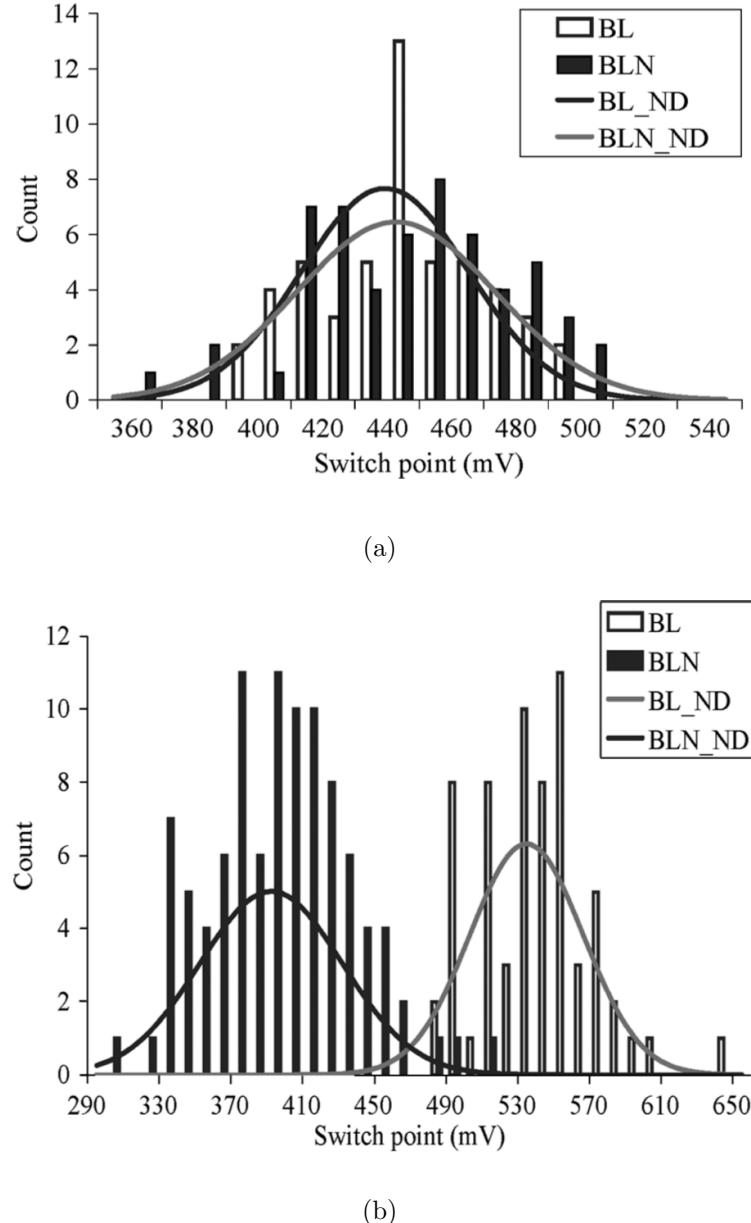


Figure 2.15 Pre-irradiation SRAM cell trip points measured driving the BL and \overline{BL} , shown in (a). BL_{ND} and \overline{BL}_{ND} are normal distribution curves for the SRAM DC switch point. In (b), measured SRAM cell node trip points after irradiation to 1.5 Mrad(Si). The BL trip points are shifted up, i.e., the write margin is increased (easier write) and the \overline{BL} write margin is reduced (it becomes more difficult to write). After [44].

the collection of generated $e\text{-}h$ pairs during irradiation.

In 1964, Wirth and Rogers developed a mathematical model based on the continuity and diffusion equations that describes the transient currents generated as a result of high-intensity irradiation [48]. The model presented by Wirth and Rogers was refined and applied to the case of bipolar transistors by Long *et al.* in [49], which accounted for differences in diffusion length and carrier lifetimes associated with an epitaxial layer on a highly doped substrate. The conditions evaluated in [49] are analogous to the case of SRAM cell well junction photocurrents when exposed to a transient radiation environment.

Massengill *et al.* applied the models and analysis presented in [49] to the case of transient radiation upsets in CMOS SRAMs in [50–52]. Fig. 2.16 plots the photocurrent produced at the drain nodes and p -well within an SRAM cell resulting from transient irradiation corresponding to a dose-rate of 5 Grad(Si)/sec. The largest photocurrents clearly correspond to the p -well contact in both the bulk (2.16(a)) and epitaxial (2.16(b)) cases. These photocurrents, which occur in every device across the entire chip, contribute to a non-negligible increase in power supply current.

Fig. 2.16 shows that errors occurring in a single SRAM cell are unlikely to be a local effect, since the magnitude of transients corresponding to the drain nodes within the SRAM cell are significantly smaller than the well photocurrent. Instead, the onset of upsets resulting from transient irradiation of an SRAM test chip are related to the collective photocurrent of each well contact on the test chip [50]. This is due to the finite resistance of metal interconnects, the resulting photocurrents cause a voltage drop in V_{DD} and an increase in V_{SS} across the entire test chip. The resulting decrease in rail voltage ($V_{DD}\text{-}V_{SS}$) results in a higher than expected SRAM sensitivity to errors during transient irradiation [50]. An example of the equivalent circuit diagram of an SRAM cell including interconnect resistances for V_{DD} and V_{SS} is shown in Fig. 2.17.

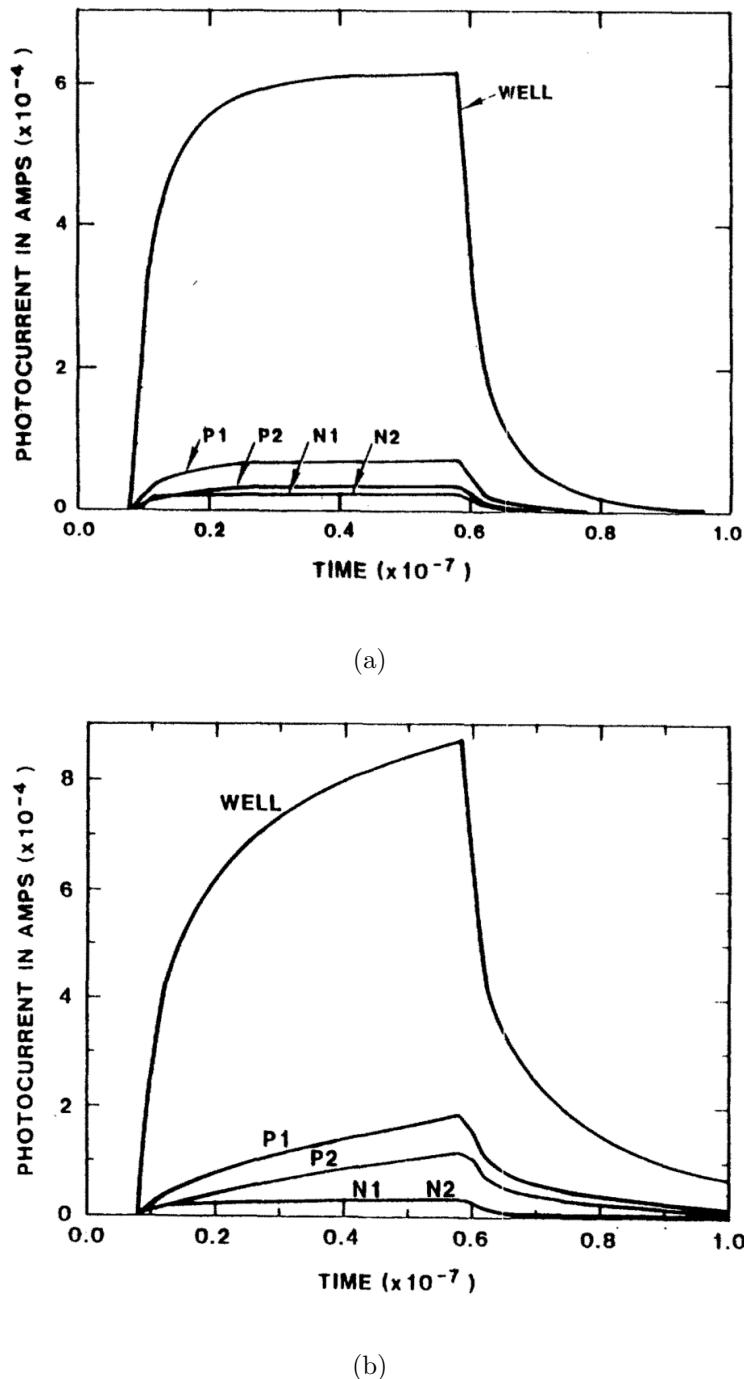


Figure 2.16 Photocurrent waveforms, at a dose rate of 5×10^9 rad(Si)/sec for the (a) bulk and (b) epi cases [50].

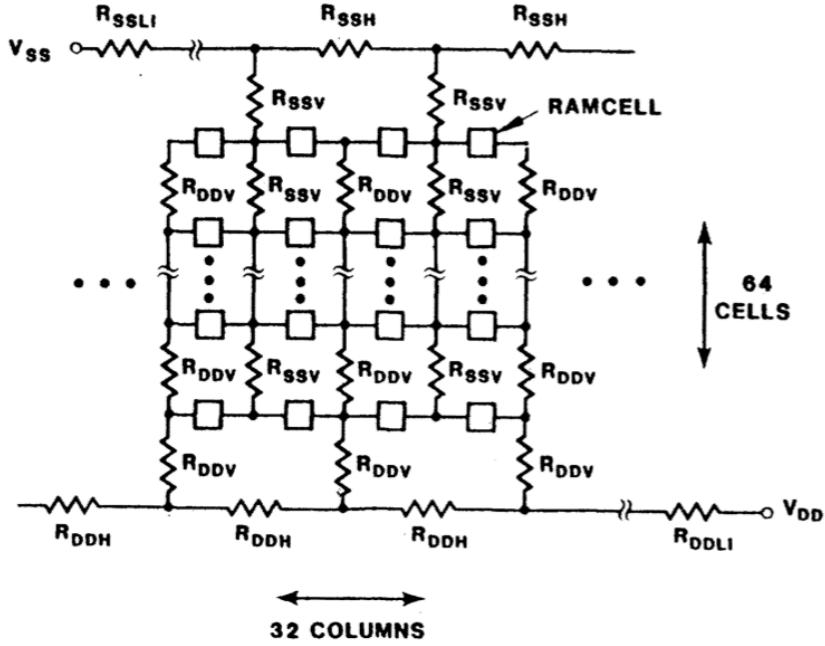


Figure 2.17 Schematic representation of the power distribution with the SRAM cells shown as “black boxes” [50].

The resistances shown in parallel are labeled R_{DDV} and R_{SSV} corresponding to the finite resistance drop between individual SRAM cells on the high and low voltage rails, respectively. Because the highest photocurrents are associated with charge collection on the p -well node of an SRAM cell, the largest change in supply voltage occurs for SRAM cells furthest from the V_{SS} supply lines [50–52].

Ultimately, it is the SRAM cells furthest from the V_{SS} supply lines that are most sensitive under transient irradiation conditions. This can be seen in Fig. 2.18 where the lower left corner of the presented bit-map corresponds to SRAM bit locations furthest from the V_{SS} supply line. The SRAM test chips were exposed to dose-rates of 1.02×10^9 , 1.08×10^9 , and 1.16×10^9 rad(Si)/sec. The increased density of bit-errors near the lower-left corner of the test chip indicates that railspan collapse is the dominant mechanism contributing to upsets under these experimental conditions.

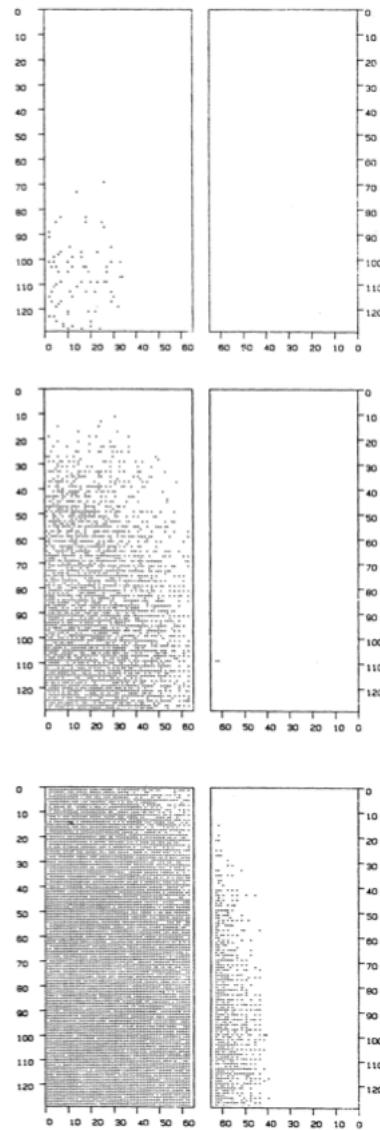


Figure 2.18 Upset bit-map with no pre-test total dose for (a) 1.02×10^9 , (b) 1.08×10^9 and (c) 1.16×10^9 rad(Si)/sec.

It is important to note that the dose-rates used in transient radiation experiments (on the order of Grad(Si)/sec) are *extremely* high and do not represent typical dose-rates in either the space radiation or terrestrial environments (outside of the specific environments mentioned previously). The signature of errors corresponding to railspan collapse, clusters of errors far from the V_{SS} supply line, is useful for easily identifying the physical mechanism contributing to errors in SRAM experiments.

2.3 Physics of Photon–Matter Interactions

Three physical processes dominate energy loss by incident photons in matter, the photoelectric effect, Compton scattering, and pair production. While pair production is an important interaction mechanism, this discussion focuses on the photoelectric and Compton scattering effects, which are most relevant to the work presented in Chapters 3 and 4. Fig. 2.19 shows the energy dependence of the three dominant physical processes for photons incident on material.

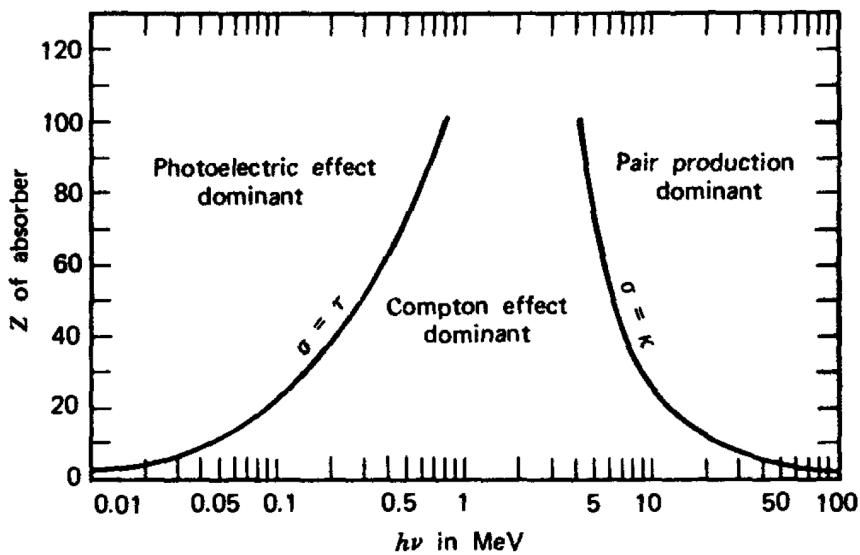


Figure 2.19 The energy dependence of the three major types of photon interactions are shown. The lines shows the values of material Z and photon energy $\hbar\omega$ for which the two neighboring effects are approximately equal [53].

In silicon, the dominant interaction of photons with energy less than 70 keV is the photoelectric effect. The photoelectric effect is a point interaction where the incident

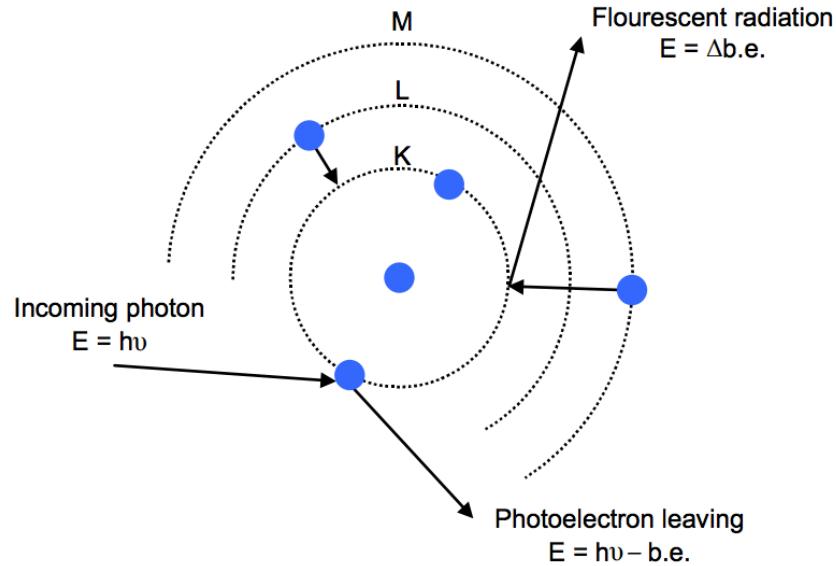


Figure 2.20 Absorption of an incident photon with energy $\hbar\omega$ resulting in the generation of an energetic photo-electron and emission of fluorescent radiation [54].

photon is completely absorbed by a target atom, leaving the atom in an excited state. Fig. 2.20 shows a cartoon description of a photoabsorption event from [54]. An energetic photo-electron is ejected from the material band structure as a result of the excited atomic state. Subsequently an *X*-ray is emitted with energy equal to the binding energy, E_b , of the generated photo-electron due to the relaxation of an electron from an *L* or *M*–shell into the lower energy state. Generated photo-electrons are typically emitted omnidirectionally from a tightly bound state, such as the *K*–shell, assuming the incident photon has energy greater than the binding energy of the *K*–shell. The energy transferred to the photo-electron can be described as

$$E_{e^-} = \hbar\omega - E_b \quad (2.3)$$

where $\hbar\omega$ is the energy of the photon and E_b is the binding energy of the photo-electron in its initial shell. For highly energetic photons (where $\hbar\omega \gg E_b$) most of the absorbed photon energy is transferred to the photo-electron.

Photons with energy in the range of 70 keV to 12 MeV interact primarily through the Compton scattering process. The Compton effect involves the incoherent scattering of a photon by a bound electron. The scattering event results in energy loss by the incident photon, corresponding to a reduction in frequency, and the generation of a *recoil* electron. A diagram of a Compton scattering event is shown in Fig. 2.21. Since the collision must obey both conservation of energy and momentum it can be

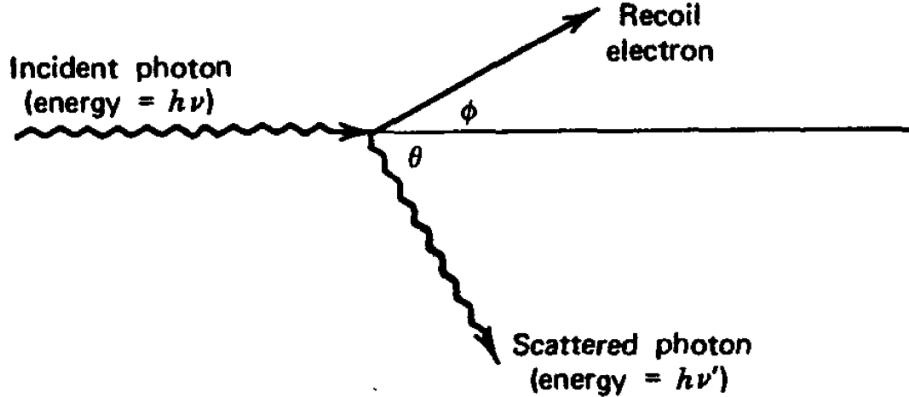


Figure 2.21 Diagram of a Compton scattering event between an incident photon with energy $\hbar\omega$ and an electron.

shown that the transfer of energy from the photon can be described by

$$E_e = \hbar\omega \frac{\frac{\hbar\omega}{m_e c^2} (1 - \cos \theta)}{1 + \frac{\hbar\omega}{m_e c^2} (1 - \cos \theta)} \quad (2.4)$$

where $\hbar\omega$ is the energy of the incident photon, $m_e c^2$ is the electron rest energy, and θ is the scattering angle of the photon as seen in Fig. 2.21.

Eq. (2.4) shows that for small scattering angles (where $\theta \approx 0$) very little energy is transferred to the generated recoil electron. The maximum energy transfer occurs

when the incident photon is back-scattered (where $\theta \approx \pi$) and the recoil electron has initial momentum along the incident photons original trajectory. The initial energy of all recoil electrons generated in Compton scattering events fall within the Compton continuum, an energy range bounded by the minimum and maximum energy transferred in a scattering event.

The total attenuation cross-section, μ , can be expressed as the superposition of the attenuation cross-section for each physical process shown in Fig. 2.19. The expression for total attenuation cross-section can be expressed as

$$\mu = \tau + \sigma + \kappa \quad (2.5)$$

where τ , σ , and κ are the photoelectric, Compton, and pair production cross-sections, respectively. The total attenuation cross section, μ , (in units of cm^2/g) versus incident photon energy in silicon is shown in Fig. 2.22. The discontinuity seen at 1.839 keV

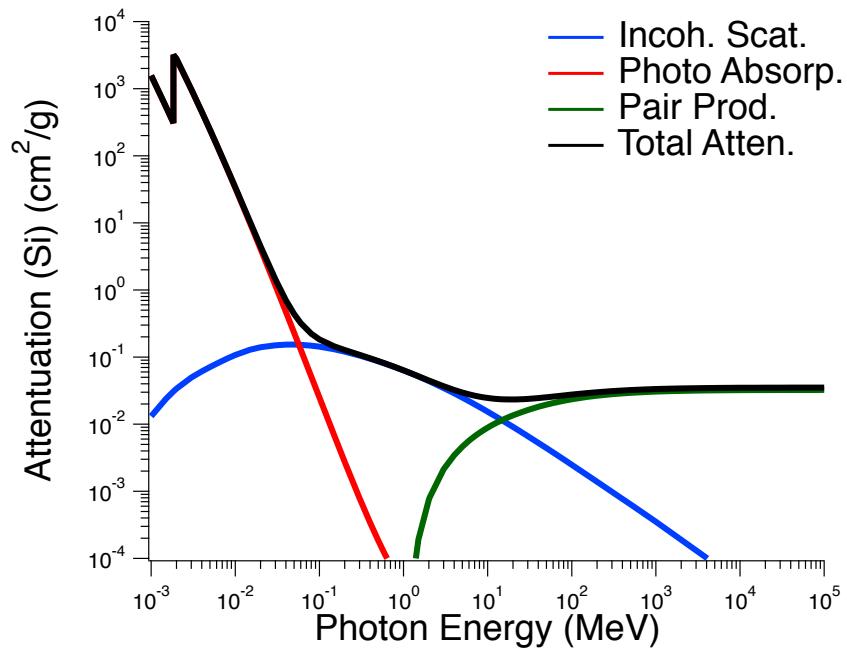


Figure 2.22 The attenuation cross-section, μ , versus incident photon energy in silicon.

corresponds to the silicon K -shell edge, this corresponds to the minimum energy required to emit an electron from the K -shell [55]. For incident photons with energy less than 1.839 keV, interactions involve the emission of photo-electrons from the L - or M -shells. The absorption edge corresponding to the L_1 , L_2 , and L_3 -shells in silicon occur at 149.7 eV, 99.8 eV, and 99.2 eV, respectively.

The attenuation of energetic photons transporting through material can be calculated using the Beer-Lambert law, which is given as

$$N = N_0(E) e^{-(\mu(E)/\rho)(\rho x)} \quad (2.6)$$

where $N_0(E)$ is the initial number of photons with energy E , $\mu(E)/\rho$ is the energy-dependent mass attenuation coefficient (obtained from Fig. 2.22), and ρx is the mass thickness of the target material. Eq. 2.6 provides a straight forward method for calculating the attenuation of photons and can be used to determine the energy absorbed within a specific range of the target material.

2.4 Ionizing Particle Track Structure

Work by Kobetich [56] and Katz [57] provided early understanding of ionization track structure in matter by modeling the range and stopping power of δ -rays. The Katz model represents the average energy deposited within a volume as a function of radial distance from an ion trajectory [56–59]. Energy deposition occurs in regions surrounding an incident ion trajectory due to the scattering of δ -rays, which results in spatially non-uniform, highly localized energy deposition events.

In [58], Zhang formulates an analytical expression of the dose deposited in the Katz model as a function of radial distance t ,

$$D(t) = \frac{Ne^4 Z^{*2}}{\alpha m_e c^2 \beta^2 t} \frac{(1 - \frac{t-\theta}{T+\theta})^{1/\alpha}}{T + \theta} \quad (2.7)$$

where N is the electron density, e is elementary charge, m_e is the electron mass, Z^* is the effective charge state of the incident particle with relative velocity β , c is the speed of light in vacuum, T is the range of δ -rays with energy W , θ is the range of δ -rays with kinetic energy equal to the ionization potential I , and α is a fitting parameter as defined in [23, 58, 59].

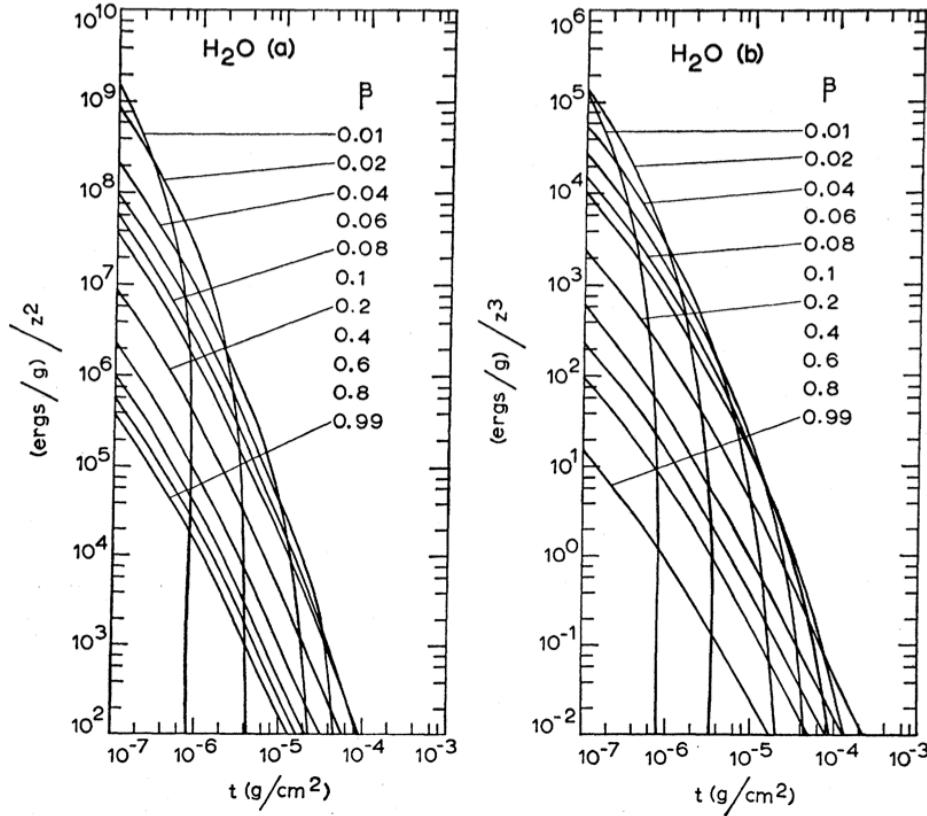


Figure 2.23 The spatial distribution of ionization energy in water for incident particles with differing relative velocity [56]. These calculations, based on Katz theory, describe the average dose deposited as a function of radial distance, t , from the incident ion track.

Fig. 2.23 shows the radial dose profile in water for several incident ion energies. The radial extension of the ionization track structure depends on the energy of the incident ion due to the kinematics of δ -ray generation and their range. For small values of incident ion energy, Fig. 2.23 shows the radial dose deposited is larger near

the core of the ion track. As β increases, Fig. 2.23 shows that the dose near the ion track core decreases, while the corresponding maximum radial distance energy is deposited increases.

The kinematics of δ -ray generation limit the maximum energy transferable in a collision between an incident ion and a single electron. This limitation on energy transfer restricts a δ -ray's transport range within the target material. The expression for maximum energy transfer, W , is given by

$$W = 2m_e c^2 \gamma^2 \beta^2 \quad (2.8)$$

where m_e is the rest mass of an electron, c is the speed of light, β is the relative velocity of the incident ion, and γ is the Lorentz factor (defined as $(1 - \beta^2)^{-1/2}$). Equation (2.8) is valid for the case $\gamma m_e / M_{ion} \ll 1$, where M_{ion} is the mass of the incident ion. Equation (2.8) scales monotonically with incident ion energy; this implies that for very energetic particles, generated δ -rays may transport far from their point of generation. As the incident ion loses energy, the track radius decreases, forming a conical shape as a function of distance into the target material [21].

In 1988, Stapor *et al.* described how two particles with similar LETs would have vastly differing charge generation profiles, and therefore the possibility for differing SEU responses [21]. In Fig. 2.24, $e-h$ pair density is plotted as a function of radial distance from the ion trajectory at a depth of 1 μm in silicon. Fig. 2.24 illustrates the difference in the resulting charge generation profiles for two ions with similar LETs but differing energies [21]. While the LET of a 25 MeV and 395 MeV Cu ion is the same, the resulting charge generation profiles differ, with the less energetic particle having a very dense charge generation region around the core of the ion trajectory, and the more energetic ion having a greater radial extension from the incident ion trajectory. As the incident particle loses energy, the maximum energy of generated δ -rays also

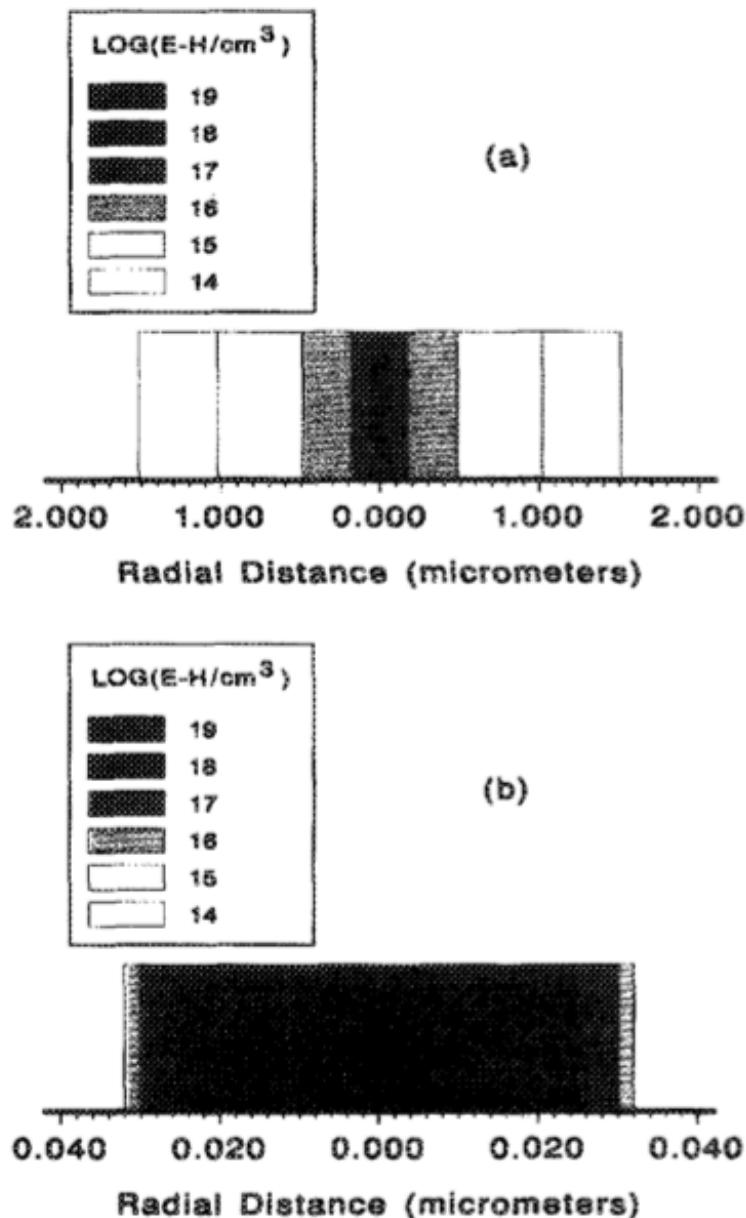


Figure 2.24 Calculated $e\text{-}h$ pair density generation is shown as a function of radial distance from the ion track at a depth of $1 \mu\text{m}$ within a volume of silicon for (a) 395 MeV Cu and (b) 25 MeV Cu [21].

decreases, causing the ion track radius to decrease with increasing penetration depth into the material.

In 1992, Xapsos [60] outlined a statistical framework for the application of LET to microelectronics that considered the track structure of an incident ion. This firmly established a metric for determining the validity of LET for technology nodes with well-established sensitive volume geometries. Dodd *et al.* [24] published measurements six years later showing the LET metric was sufficient to characterize CMOS technology nodes larger than 250 nm. In [24], Dodd effectively demonstrates that for older technology nodes that exhibit a critical charge greater than 10 fC the LET of the primary particle is sufficient to predict the device- and circuit-level response.

More recently, interest has reemerged in evaluating the potential contribution of electrons and δ -rays to the SEU response of modern technology nodes. Murat *et al.* evaluated technology nodes with feature sizes less than $0.5 \mu\text{m}$, determining that the energy of the incident ion does contribute to the SEU response [61]. Later, King *et al.* demonstrated the potential for contributions to the SEU cross section from individual δ -rays depositing energy within the sensitive volume of a 22 nm SRAM [9]. Raine *et al.* published several papers utilizing the Katz model to evaluate energy deposition contributions from δ -rays in a single ionizing particle event to the SEU rate. These studies concluded that the ionization profile of heavy ions does not contribute to multiple-bit upsets in the 32 nm SOI technology node [7]. However, it has been shown that while the average energy deposition profile is modeled very well by the Katz model, variation between the average and individual δ -ray energy deposition events can be quite significant [10].

The track radius of ionizing radiation events is large compared to the spacing of adjacent transistors and pitch of neighboring SRAM cells in a 22 nm technology node, shown in Fig. 2.25. This implies that modern technology nodes have scaled to a point

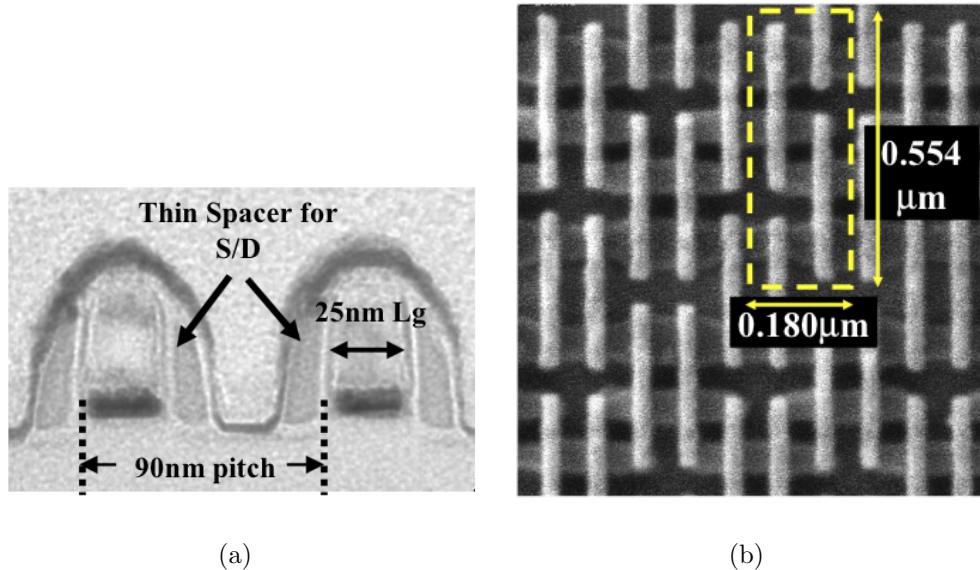


Figure 2.25 2.25(a) Cross-sectional TEM image showing thin composite oxide-nitride spacer on 25 nm wide gate at 90 nm pitch. 2.25(b) Top-down SEM image of the $0.1 \mu\text{m}^2$ 6T-SRAM cell after STI fill and gate-first metal gate patterning, with cell dimensions of $0.18 \mu\text{m}$ and $0.554 \mu\text{m}$. After [18].

where electron/ δ -ray energy deposition events may be of sufficient magnitude and interact frequently enough to become a reliability concern. This leads to the potential for contributions to the single- and multiple-bit upset event rate from the primary ion and δ -rays generated in ionizing particle events. Consequently, for technologies that exhibit critical charges lower than 0.2 fC, the role of δ -rays must be reconsidered when evaluating the SEU response of SRAM fabricated in these technology nodes [9, 10]. It is therefore necessary to have a thorough understanding of the potential implications of δ -rays on these devices in order to understand the SEU response of SRAMs fabricated in that technology nodes that exhibit small critical charge. These issues are discussed in detail in Chapter 4.3, which focuses on the impact of incident ion species, energy, mass, and the implications of δ -rays interactions on the SEU response of current- and next-generation technology nodes.

Chapter 3

Experimental Investigation of Electron-Induced SEUs

This chapter presents experimental methods for *in situ* X-ray irradiation and SEU measurements as a technique for investigating electron-induced SEUs in SRAMs. Extensive parametric and functionality testing of SRAM test chips fabricated in 28 nm and 45 nm bulk silicon technology was performed to determine the range of operational stability. SRAM test chips were shown to be stable and hold valid data over a wide range of supply voltage conditions. Test boards were designed and integrated to allow independent, simultaneous control of the SRAM test chips and power supply conditions during the experiment. Test chips were exposed to a source of energetic X-rays from an ARACOR 4100 X-ray irradiator. SRAMs were programmed into either an all zero (*0000*), all one (*1111*), checkerboard (*1010*), or reverse checkerboard (*0101*) pattern during irradiation. Once exposure of the SRAM test chip to X-rays was complete, the final state of the data pattern was read back and compared to the initial, programmed, state. The data pattern and address location of any errors was logged and recorded for further analysis. Section 3.1 discusses the relevant experimental setup and methods. Section 3.2 provides a full discussion of the experimental results and analyzes critical experimental parameters. Section 3.3 compares the sup-

ply voltage dependence of electron-induced SEUs to similar data obtained in muon and low-energy proton irradiations.

3.1 Experimental Setup and Methods

A diagram of the experimental setup used to investigate electron-induced SEUs is shown in Fig. 3.1. An automated test system was developed to allow independent control of two Keithley 2410 SourceMeters® for the SRAM test chip and SRAM test board through a GPIB/LAN gateway while sending control commands to the SRAM test board through a USB connection. This configuration allows remote control of the SRAM supply voltage and allows the power supply current to be monitored while performing parametric testing of the SRAM test chip.

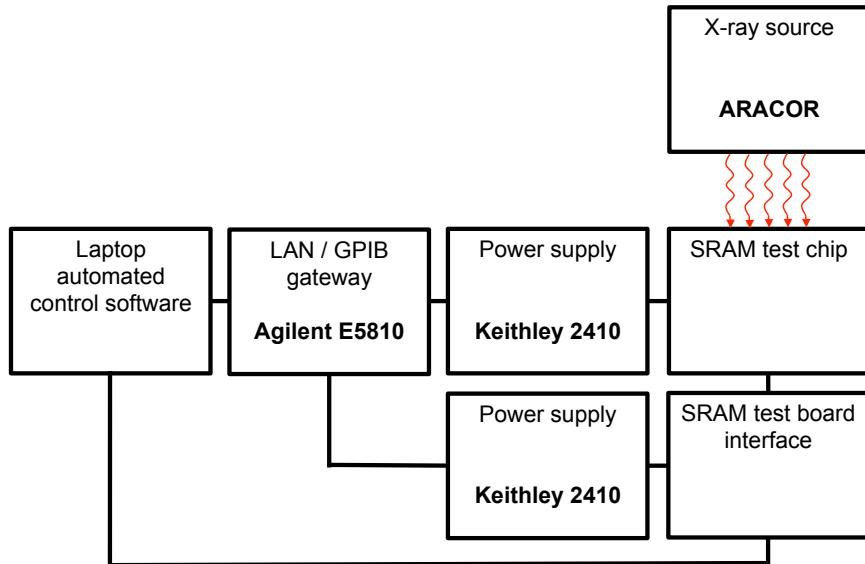


Figure 3.1 An automated test system allows independent control of two Keithley 2410 SourceMeters for the SRAM test chip and test board interface through a LAN/GPIB gateway. Control commands are transmitted to the SRAM test board through a USB connection from a laptop. This system allows the supply voltage of the SRAM to be modulated *in situ*. The device under test is exposed to energetic *X*-rays under varied supply voltage conditions.

Reduced supply voltage conditions are employed to determine the susceptibility of the SRAM to singly-charged particles and compare the bias dependence of electron-induced upset rates to that of upsets known to be caused by low-energy protons and muons [1, 2]. As discussed in Section 2.1, low-voltage operation has practical significance, since it is common for SRAMs in standby mode to operate at 70-80% of the nominal supply voltage to reduce power consumption [16, 17]. Low-power applications, mobile communications, mobile computing, and medical devices also frequently employ power-saving techniques that include reducing V_{DD} during standby and idle modes of operation, making this a relevant testing approach.

Fig. 3.2 shows the applied bias as a function of time for a representative testing sequence employed in this study. An initial write and read, using either an all one, all zero, checkerboard or reverse checkerboard pattern, is performed at nominal bias conditions prior to X -ray exposure of the device under test (DUT). The supply voltage is then lowered while the DUT is irradiated. In the case of Fig. 3.2, the total exposure time was 30 seconds. In other experiments the total exposure time was varied from 30 seconds to several minutes. Once the X -ray source was turned off, the supply voltage was returned to nominal conditions and the final state of the memory was read. The final and initial states of the memory were compared to identify any errors that may have occurred, noting the address and data patterns of observed errors for post-processing.

During the experimental period the range of supply voltages used in this study varies from 0.35-1.0 V. The SRAM test chips used in this work are commercial parts *designed* to operate and remain stable between 0.5-1.0 V. In functionality and parametric bench testing, the test chips were confirmed to be stable down to 0.35 V during a one hour testing period, which is much longer than typical X -ray exposure times. Extensive testing was done prior to irradiation to demonstrate that no bit flips oc-

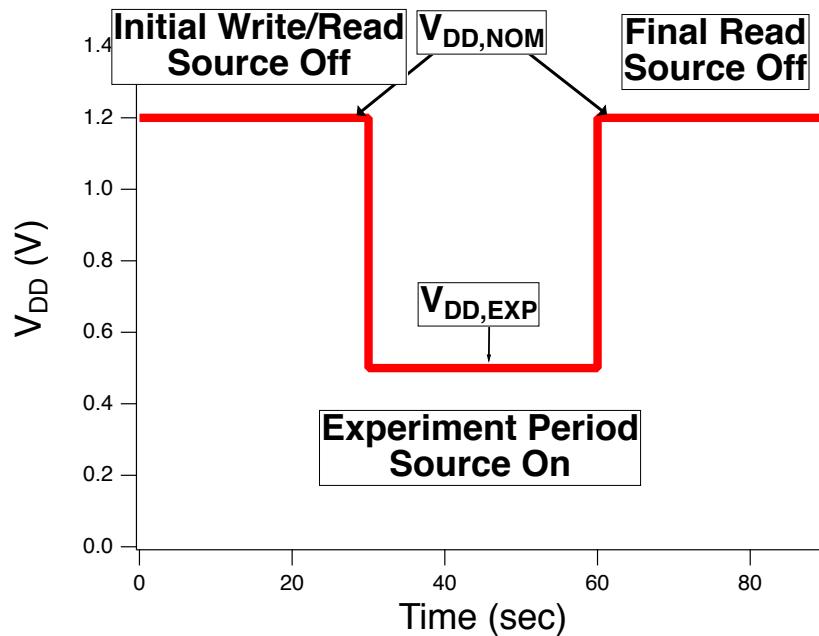


Figure 3.2 Example timing diagram for measuring upsets at reduced bias. Read and write operations are performed under nominal bias condition, V_{DDNOM} . During exposure the rail is reduced to a value, V_{DDEXP} , for the duration of the experiment. Upon conclusion of the exposure, the nominal rail is restored, a final read operation is performed, and any errors recorded.

curred under any bias conditions, indicating the memory was written properly and held valid information through the timing sequence shown in Fig. 3.2 and in all other cases shown in this work. Functionality and parametric testing was performed before and after each radiation exposure for equivalent time periods to ensure the integrity of the SRAM under all bias conditions. This procedure verifies that the data remain intact and stable at all supply voltage conditions and that no degradation due to TID has occurred during or after each X -ray exposure.

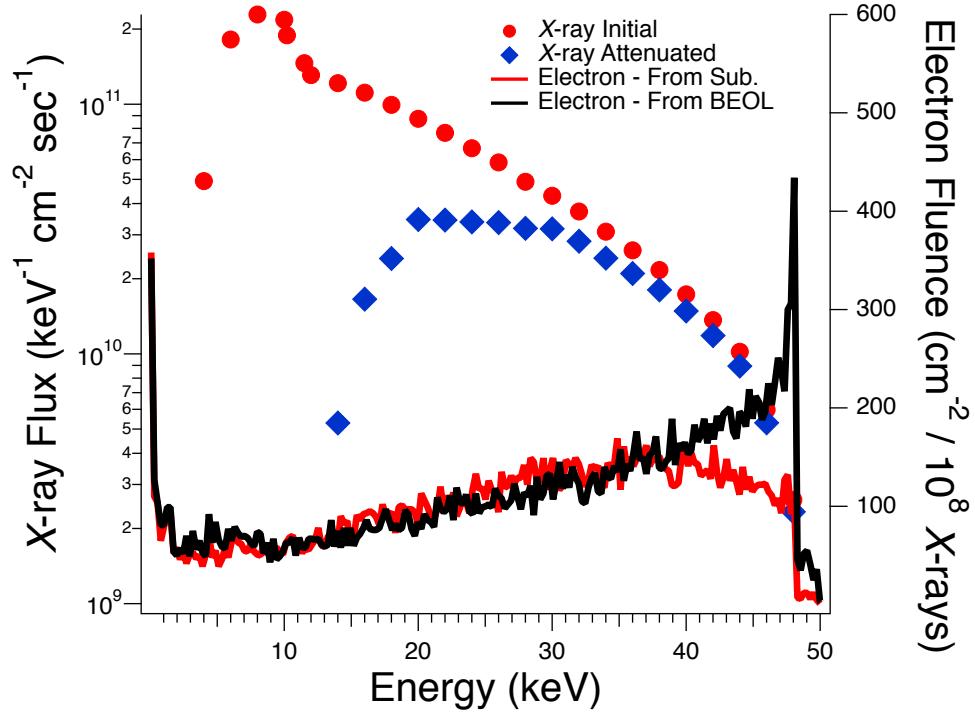


Figure 3.3 X -ray and electron spectra produced by the ARACOR 4100 X -ray irradiator. The average energy is 10 keV and the maximum energy is 50 keV, corresponding to the endpoint bremsstrahlung energy [62, 63]. For the error rate testing in this study, the spectrum is modified by a 1 mm aluminum attenuator, which reduces the flux of low-energy X -rays incident onto the DUT. The electron fluences corresponding to monoenergetic 50 keV X -rays interacting with the active silicon region in the “forward” (scattering events in the active device overlayer materials, denoted BEOL) and “reverse” (scattering events in the device substrate) beam directions are shown on the right.

Irradiation was performed with a beam current of 1 mA and beam voltage of 50 kV. The X -ray spectra produced under these conditions are shown in Fig. 3.3 [62,63]. For the unattenuated spectrum in Fig. 3.3, 10 keV is the average energy and 50 keV is the endpoint bremsstrahlung energy. The interaction between X -rays in this energy range and electrons is dominated by the photoelectric effect, however, near the bremsstrahlung edge Compton scattering becomes a non-negligible contribution. The generated photo-electrons in these interactions are emitted omnidirectionally. As discussed in Section 2.3, for highly energetic photons, where the energy of the incident photon is much greater than the photo-electron shell binding energy ($\hbar\omega \gg E_b$), most of the absorbed photon energy is transferred to the photo-electron.

A 1 mm aluminum attenuator was placed above the DUT with an air gap of 3.5 cm between the attenuator and the test chip. The attenuator filters the low-energy X -ray spectrum, passing the more energetic X -rays that are more likely to produce observable electron-induced effects. This reduces the dose-rate and TID effects. Attenuation of the initial spectrum by the 1 mm layer of aluminum is calculated using the Beer-Lambert law, Eq. 2.6 and plotted in Fig. 3.3. The prominent 10 keV X -ray peak is absent from the attenuated spectrum; only the high energy tail of the X -ray distribution is capable of transporting through the attenuator and interacting with the DUT. The majority of photo-electrons generated in the attenuator are reabsorbed before leaving the Al.

Fig. 3.4 shows the transport of maximal energy, 50 keV, photo-electrons generated at the Al-to-air interface. The Al is on top and the air gap is the large rectangle. The DUT is very thin and on the bottom of the figure. Photo-electrons have random trajectories. The few electrons that transport through the air gap to the DUT stop within the first few micrometers of the back end of line (BEOL) materials (metalization and dielectric layers) [64]. Therefore, only X -rays absorbed within the DUT

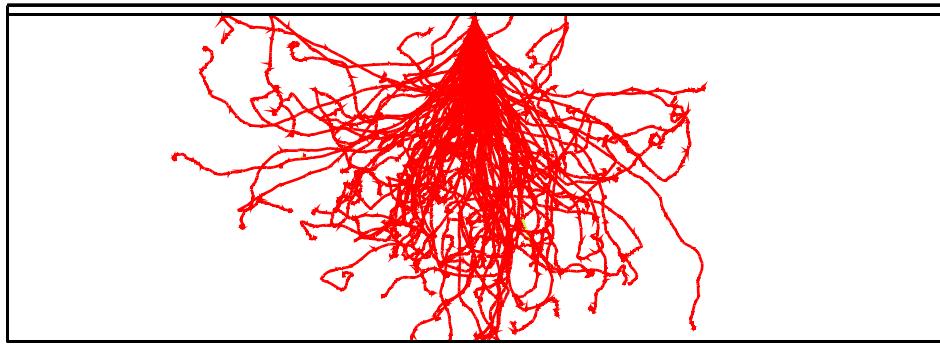


Figure 3.4 50 keV photo-electrons exiting the aluminum attenuator have insufficient energy to transport through the 3.5 cm air gap and back end of line (BEOL) materials to reach the active silicon. Only photo-electrons generated in the DUT itself can interact with the device material in the sensitive silicon region.

itself generate photo-electrons that can interact with the device material in the sensitive volume of the device. An example of this type of interaction is shown in Fig. 3.5 where the absorption of an incident 10 keV X -ray leads to the generation of an initially free, nearly ballistic electron that deposits 9.3 keV of energy when it scatters within the sensitive volume of a 45 nm SRAM.

The electron fluence spectrum corresponding to a monoenergetic beam of 50 keV X -rays in the “forward” and “reverse” beam direction is plotted on the right hand side of Fig. 3.3. The most frequent energy corresponds to the incident X -ray energy in the forward direction, which corresponds to photo-electrons generated in the BEOL materials and the active silicon region. In the reverse beam direction, corresponding to electrons generated in the substrate that transport back to the active silicon, the situation is more complicated due to the random trajectory of the generated photo-electrons. This demonstrates the random nature, in energy and trajectory, of the electron environment local to the sensitive volume.

Following the method used in [63], flatband voltage, V_{FB} , shifts were measured

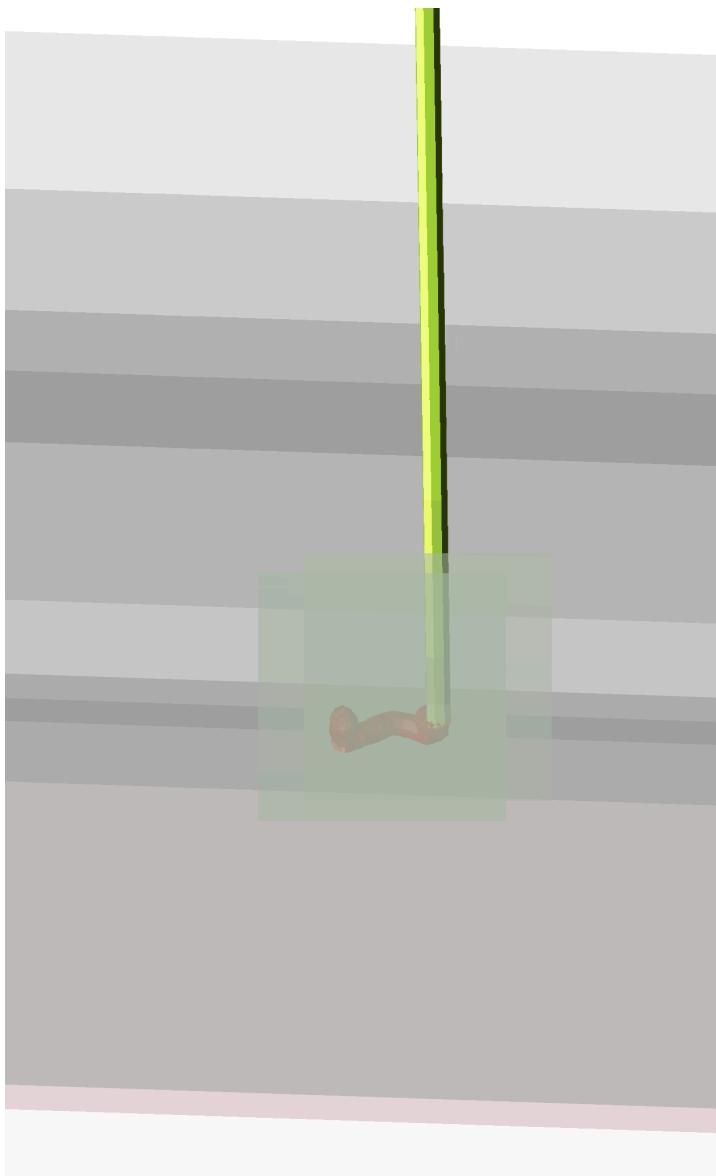


Figure 3.5 A 10 keV X -ray is normally incident on the simulated device structure of a 45 nm SRAM. It subsequently undergoes photoabsorption resulting in the generation of an energetic electron. The resulting electron then transports through the device material, depositing energy in excess of 9.3 keV within the sensitive volume of the SRAM.

with MOS capacitors to calibrate the dose-rate. The devices were fabricated and packaged at Sandia National Laboratories; lids were removed for the X -ray irradiations. The calibration devices were n -type substrate MOS capacitors featuring aluminum dot gates with an area of 0.01 cm^2 and SiO_2 gate oxide thickness of 101 nm [65]. The dose-rate calibration data are plotted in Fig. 3.6, which shows the change

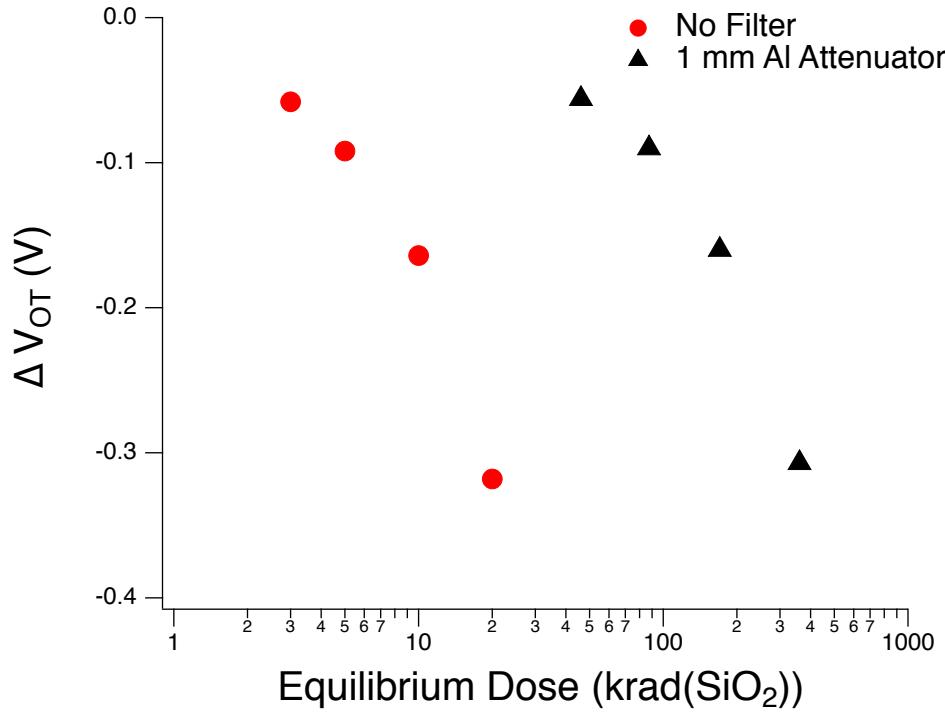


Figure 3.6 ΔV_{OT} as a function of equilibrium dose for MOS capacitors irradiated with beam current and voltage of 1 mA and 50 kV, respectively. Devices were biased with 10 V on the gate during irradiation. The use of a 1 mm Al attenuator causes a increase in equilibrium dose required to achieve equivalent shifts in ΔV_{OT} by a factor of 17, indicating the nominal dose rate of 1.7 krad(SiO_2)/min is reduced to 100 rad(SiO_2)/min.

in oxide-trapped charge as determined by shifts in C - V characteristics. The equilibrium dose shown in Fig. 3.6 represents the nominal, unattenuated dose from the X -ray source. The measured dose-rate incident on the MOS capacitor is reduced by a factor of 17 when compared to the nominal dose-rate [63]. The attenuated dose-rate is 100 rad(SiO_2)/min.

The X -ray flux is calculated by integrating over the attenuated energy spectrum in Fig. 3.3 and can be calculated as

$$\phi_{total} = \sum_{i=0}^{\infty} \phi(E_i) \quad (3.1)$$

where $\phi(E_i)$ is the flux of photons with energy E_i , and ϕ_{total} represents a cumulative photon flux. Evaluating Eq. (3.1) with the attenuated photon spectrum yields a cumulative photon flux of $1.5 \times 10^{12} \text{ cm}^{-2} \text{ s}^{-1}$. Similarly, the electron flux corresponding to 50 keV X -rays is calculated to be $1.16 \times 10^6 \text{ cm}^{-2} \text{ s}^{-1}$.

3.2 Experimental Results

Using the methods described in Section 3.1, several experiments exposing SRAMs to energetic X -rays were performed to investigate the plausibility of electron-induced upset events. Four types of devices were used. Test Chips A and B are 28 nm SRAMs with a capacity of 23 Mbit and nominal operating voltage of 0.9 V in triple-well (TW) and dual-well (DW) processes, respectively. Test Chip C is a 28 nm SRAM with a capacity of 32 Mbit and nominal operating voltage of 1.0 V. Test Chip D is a 45 nm SRAM with a capacity of 4 Mbit and nominal operating voltage of 1.1 V. Normalized cross-sections are obtained for each applied bias condition using the following relationship,

$$\sigma(V_{DD}) = \frac{N}{A_{cell}\Phi} \quad (3.2)$$

where N is the number of observed errors, A_{cell} is the cell area of the SRAM being tested, and Φ is the photon fluence. Error bars are shown at the one-sigma confidence interval in all experimental and simulated cross-sections. Table 3.1 shows the experimental supply voltage conditions, exposure time, and corresponding X -ray fluence for measurements on each test chip.

Table 3.1 X-ray Supply Voltage, Exposure Time, and Fluence

V_{DD} (V)	Test Chip A		Test Chip B	
	Time (s)	Fluence (cm^{-2})	Time (s)	Fluence (cm^{-2})
0.35	40	6×10^{13}	40	6×10^{13}
0.4	130	1.95×10^{14}	120	1.8×10^{14}
0.5	310	4.65×10^{14}	300	4.5×10^{14}
0.6	620	9.3×10^{14}	630	9.45×10^{14}
0.7			1260	1.89×10^{15}
0.8			630	9.45×10^{14}

V_{DD} (V)	Test Chip C		Test Chip D	
	Time (s)	Fluence (cm^{-2})	Time (s)	Fluence (cm^{-2})
0.45	90	1.35×10^{14}	270	4.05×10^{14}
0.5	180	2.7×10^{14}	30	4.5×10^{13}
0.55	180	2.7×10^{14}	360	5.4×10^{14}
0.6	540	8.1×10^{14}	860	1.29×10^{15}
0.65	300	4.5×10^{14}	1080	1.62×10^{15}
0.7	600	9×10^{14}	528	7.92×10^{14}

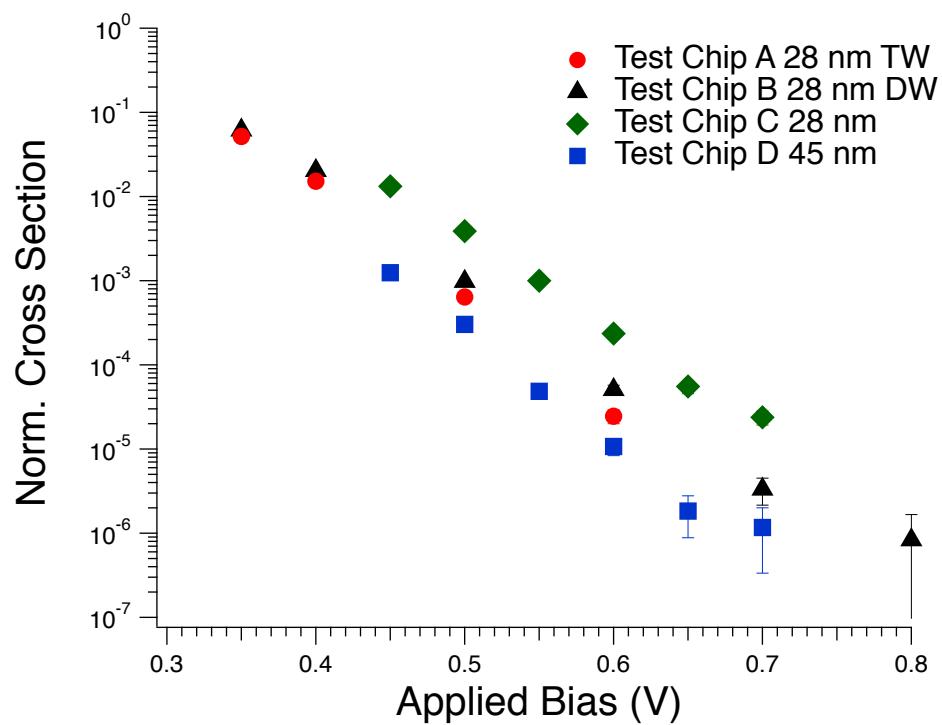


Figure 3.7 Experimental errors induced during irradiation with X -rays in an ARACOR 4100 X -ray irradiator. The bias sensitivity of critical charge in SRAMs provides strong evidence of energetic electron-induced upsets in modern SRAMs.

Fig. 3.7 plots the normalized cross-section, as described in Eq. (3.2), as a function of supply voltage for SRAM test chips exposed to X -rays. Fig. 3.7 shows that errors are observed when these devices are biased between 0.35 V and 0.8 V while exposed to X -rays. The resulting upset cross-section of all test chips exhibits an exponential dependence on applied bias because of the voltage dependence on critical charge. This is consistent with well established test procedures used for assessing the single-event error rates for protons and muons [1, 2]. In the case of Test Chip B, upsets were observed within 10% of the nominal supply voltage of 0.9 V, which is within the designed operating voltage range for the SRAM. Each of the SRAM test chips exhibits a cross-section less than the total cell area at all supply voltages, resulting in normalized cross-sections less than unity. All observed errors had unique memory addresses, strongly suggesting that errors occurred randomly within the memory array during experiments and were not caused by repeated bit-flips in “weak” cells. Again it is noted that no bit-flips occurred due to reduced bias conditions during functionality and parametric tests before and after X -ray irradiation of all test chips under all bias conditions, indicating the memory operated under stable conditions during experiments.

Photocurrents produced by the overall photon flux are generated as the result of X -ray irradiation. The generated photocurrent produced by the collective effect of the X -ray source can be calculated as

$$I_{PC} = qV\dot{D}_{SiO_2}\dot{R}_{SiO_2} \quad (3.3)$$

where q is elementary charge, V is the volume of an SRAM cell, \dot{D}_{SiO_2} is the dose-rate in SiO_2 , and \dot{R}_{SiO_2} is the density of electron-hole pairs generated per $rad(SiO_2)$. The generated collective photocurrent in an individual SRAM cell is calculated with Eq. (3.3) to be approximately 1 fA. SPICE simulations were performed for 28 nm

SRAM test chips A and B for each experimental bias condition. The simulation results indicate restoring currents are greater than 100 nA at the lowest experimental supply voltage, 0.35 V. Fig. 3.8 shows the cross-section for Test Chip B at 0.35 V as a function

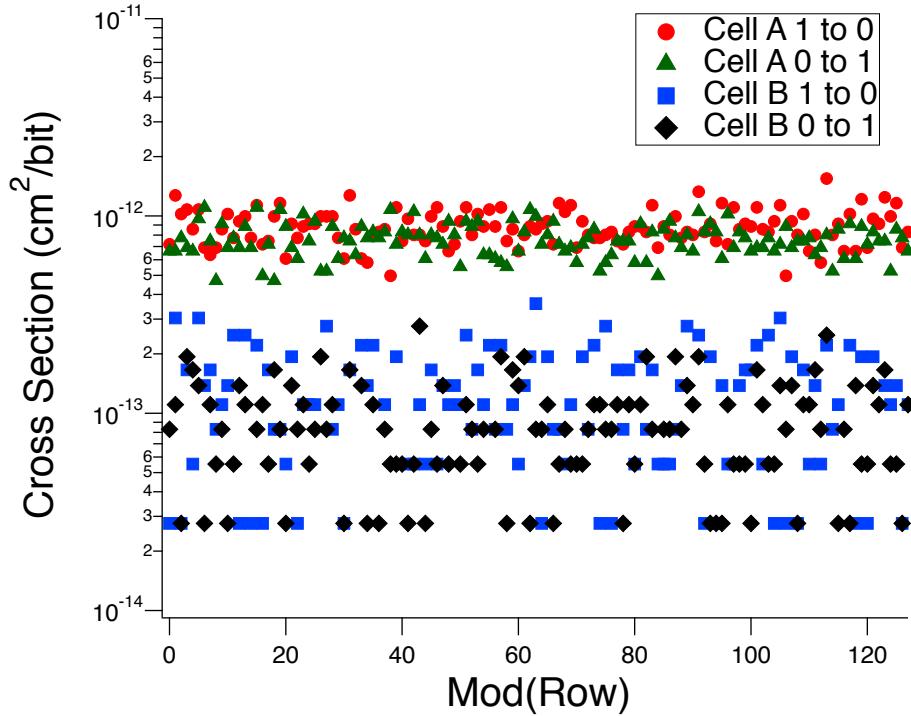


Figure 3.8 Experimental errors induced during irradiation with X -rays in an ARACOR 4100 X -ray irradiator. Results are for Test Chip B, errors are plotted as a function of distance from row 0, corresponding to V_{DD} lines, and row 128, corresponding to V_{SS} lines at a supply voltage of 0.35 V. Errors occur randomly within the SRAM cell and do not preferentially occur near supply voltage or ground rails.

of distance from V_{DD} and V_{SS} lines. Errors are shown to occur randomly between supply voltage and ground power metallization and do not preferentially occur near the supply voltage or ground lines, indicating that dose-rate effects do not contribute to the error rate in these experiments. Hence, as expected, collective photocurrents generated in X -ray experiments are significantly smaller than the restoring current of SRAM cells and are incapable of causing the observed errors.

Furthermore, the probability of coincident photon events contributing to the error rate can be calculated as,

$$Pr(X_1||X_2) = (\phi A_{cell} \tau)^2 \quad (3.4)$$

where ϕ is the incident photon flux, A_{cell} is the cell area, and τ is the characteristic time for an upset event (assumed to be 10 ns). Evaluation of Eq. (3.4) for the 28 nm and 45 nm SRAMs results in probabilities of 6.45×10^{-10} and 1.9×10^{-9} , respectively, of coincident photons contributing a single upset to the experimental results. The contribution of coincident photons to the observed upsets on the time scale considered is therefore negligible.

Lastly, it is important to monitor the TID accumulated by the test chip, since this can lead to degradation of the memory and result in a loss of functionality [66]. The dose accumulated in the experiments for the triple-well 28 nm bulk SRAM, Test Chip A, was less than 1.9 krad(SiO₂). The dual-well SRAM, Test Chip B, accumulated 5 krad(SiO₂) during the experiments. Test Chip C, a 28 nm SRAM, accumulated a dose of 5.4 krad(SiO₂), and Test Chip D, a 45 nm SRAM, accumulated a total dose of 11.1 krad(SiO₂). Test Chip C, a 28 nm, 32 Mbit bulk SRAM, underwent the largest change in power supply current based on measurements before and after irradiation, where the pre- and post-irradiation power supply currents were 82.7 mA and 81.5 mA, respectively. This is a decrease in power supply current of less than 1.5%. Similarly, none of the other devices discussed in these experiments accumulated sufficient dose to compromise memory operation or cell integrity.

The above results and analysis demonstrate that, for the experimental conditions considered here, single energetic electrons produced by *X*-ray irradiation are by far the most likely cause of the observed errors within the SRAMs.

3.3 Comparison to Low-Energy Proton and Muon SEUs

With the observation of electron-induced SEU, it is quite useful to quantify the significance of this effect relative to other well-understood phenomena. To this purpose, the data set presented in Fig. 3.7 is compared to SEU data sets obtained with low-energy protons and muons.

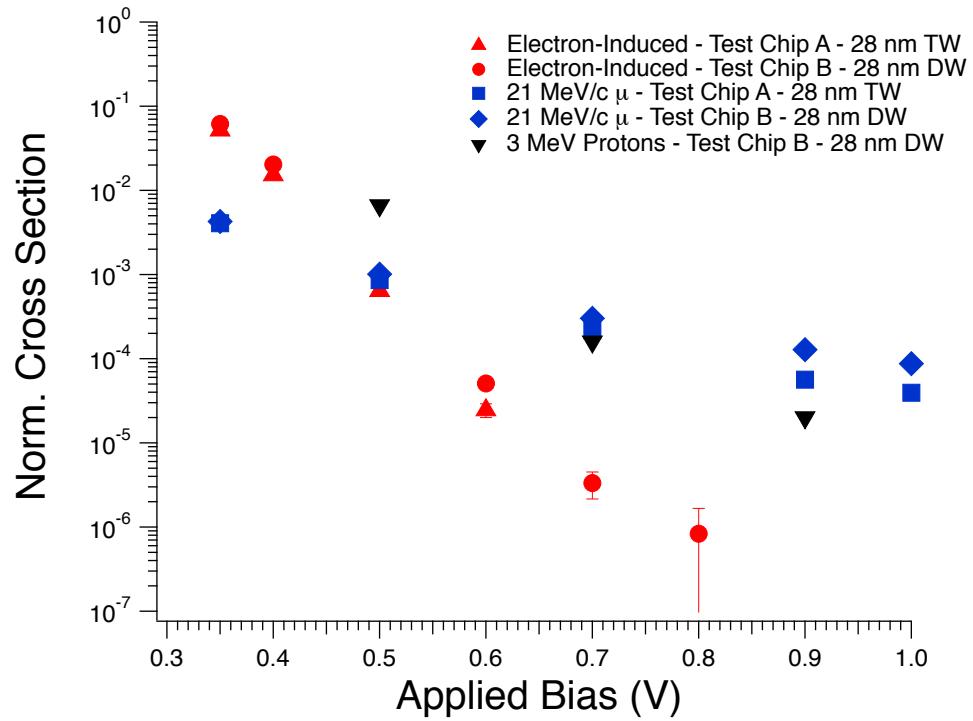


Figure 3.9 SEU cross-section dependence on supply voltage for electron-induced SEU cross-sections observed during X-ray irradiation, compared to low-energy protons and muons in 28 nm (3.9) SRAMs. Results show that under nominal bias conditions protons and muons are capable of inducing upsets in 28 nm SRAMs while this sensitivity is absent for energetic X-ray electrons generated during X-ray exposure. Under reduced bias conditions, electron-induced SEUs exhibit a larger dependence on supply voltage than muons and protons in the 28 nm technology nodes.

Low-energy proton experiments were performed in the Pelletron facility at Vanderbilt University. Experiments were performed under vacuum with a monoenergetic

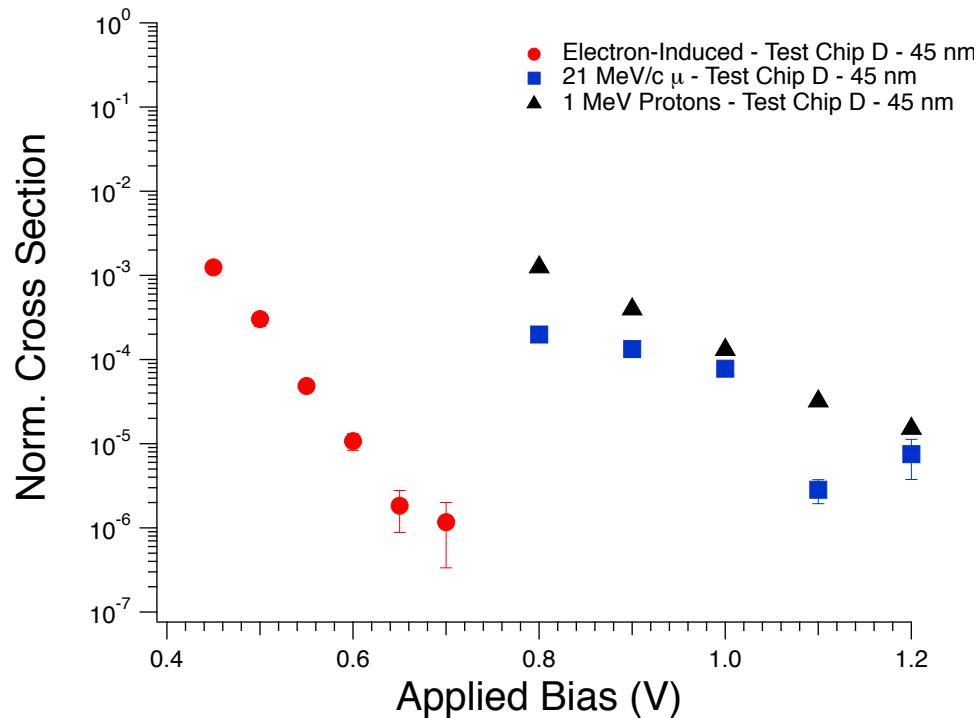


Figure 3.10 SEU cross-section dependence on supply voltage for electron-induced SEU cross-sections observed during X-ray irradiation, compared to low-energy protons and muons in 45 nm (3.10) SRAMs. Results show that under nominal bias conditions protons and muons are capable of inducing upsets in 45 nm SRAMs while this sensitivity is absent for energetic X-ray electrons generated during X-ray exposure. Under reduced bias conditions, electron-induced SEUs exhibit a larger dependence on supply voltage than muons and protons in the 45 nm technology nodes.

proton beam at an energy of 3 MeV normally incident on Test Chip B and 1 MeV normally incident on Test Chip D. The sensitivity of the 28 nm SRAM test chip was investigated for supply voltage in the range of 0.35-1.0 V. The 45 nm SRAM test chip was investigated for applied biases of 0.8-1.2 V. The timing sequence for applied bias during experiments with low-energy protons is identical to that of Fig. 3.2. Parts were tested to a fluence of 10^{12} cm^{-2} .

Muon experiments were performed at TRIUMF using the M15 beam line. Low-energy positively charged muons with a known energy distribution were normally incident on Test Chips A and B, 28 nm bulk SRAM, and Test Chip D, a 45 nm SRAM. The muon beam energy characterization at TRIUMF is described in [2]. The incident muon energy was varied by means of a tunable momentum filter [2, 15]. The timing sequence for applied bias during experiments with low-energy muons is identical to that of Fig. 3.2. Parts were exposed to a total fluence of $6.2 \times 10^8 \text{ cm}^{-2}$. A normalized upset cross-section is obtained for muons and low-energy proton experiments from Eq. (3.2).

Figs. 3.9 and 3.10 show SEU data from low-energy proton and muon experiments plotted alongside electron-induced SEU data from Fig. 3.7 for 28 nm and 45 nm test chips. All test chip samples exhibit exponential SEU cross-section dependence on applied bias, consistent with previous results [1, 2]. Electron sensitivity is observed within 10% of nominal bias conditions for test chip B, indicating that SEUs initiated by high energy electrons may be observable in more sensitive present-generation ICs, and at nominal supply voltages for future technology nodes. It is noted that, under nominal bias conditions, test chips A, B, and D exhibit sensitivity to muons and protons, while no events initiated by single high-energy electrons are observed. This indicates that high-energy electrons are much less important than protons and muons for SRAMs from these technology nodes, operating at or near nominal bias conditions.

As the applied bias is reduced, electron-induced SEUs exhibit a larger dependence on supply voltage (a larger slope) than muons and protons in the 28 nm and 45 nm technology nodes.

Chapter 4

Simulation of Electron-Induced SEUs

The experimental results from Chapter 3 show that 28 and 45 nm SRAMs exhibit SEU sensitivity when exposed to energetic X -rays. Data analysis of those results indicates that the observed errors are electron-induced SEUs. Using Monte Carlo radiation transport codes this chapter presents simulation work and analysis supporting the experimental results and conclusions of Chapter 3. Section 4.1 presents simulations of monoenergetic X -rays incident on a target structure representative of 45 nm bulk SRAMs. Simulation results are shown to be in good agreement with the experimental data from Chapter 3 and show that photo-electrons generated by incident X -rays deposit energy in excess of the estimated critical charge under a wide range of applied bias. The relative impact of electron-induced SEUs in the space radiation environment is presented by performing error rate calculations for a 45 nm SRAM in the geosynchronous orbit environment during the solar minimum cycle in Section 4.2. Analysis of δ -ray contributions to single- and multiple-bit upset rates for SRAMs irradiated with heavy ions is discussed in Section 4.3.

4.1 Simulation of X-ray Energy Deposition in SRAMs

Radiation transport simulations were performed with MRED [67], a Geant4-based code [68] with Fortran extensions that include PENELOPE 2008 [69], to evaluate the potential impact of electrons produced by energetic *X*-rays on the device SEU response. The use of the PENELOPE 2008 package [69] increases the fidelity and resolution of calculations involving low energy (less than 50 keV) electrons, photons and positrons. PENELOPE 2008 extends the low-energy range for electromagnetic processes from 250 eV down to approximately 100 eV and also tracks electrons with greater spatial resolution. These refinements produce increased fidelity of energy deposition estimates in the small sensitive volumes of interest in this work.

High-energy protons cause single-event effects primarily through secondary ions produced in nuclear reactions [1, 12, 13, 32]. For a given proton energy, experimental cross-sections are expressed with reference to the primary proton flux, regardless of the upset mechanism. In this sense, the case of single-event effects caused by secondary electrons is analogous. Results in this work are therefore plotted as a function of the incident *X*-ray fluence, which provides the most consistent reference for analyzing SEUs caused by secondary photo-electrons. The *X*-ray energy used in the simulations, 50 keV, is representative of the end-point bremsstrahlung within the *X*-ray spectrum and results in the generation of the most energetic and ionizing secondary electrons. A 4 kbit SRAM array is simulated, using a sensitive volume structure consistent with a 45 nm bulk SRAM using MRED. Energy deposition is calculated for individual *X*-rays on an event-by-event basis. The sensitive volume geometry used was $0.22 \mu\text{m}^2 \times 500 \text{ nm}$, which is representative of 45 nm processes in the ITRS roadmap [20]. Additionally, the simulated structure includes the 1 mm aluminum attenuator and appropriate BEOL thickness with 15 μm of oxide and metallization. The SRAM

was simulated to a total 50 keV photon fluence of $2 \times 10^9 \text{ cm}^{-2}$. This fluence was found to be sufficient to determine the energy deposited and ultimately estimate the resulting error rate with adequate precision to compare with the experimental data. The vertical black lines in Fig. 4.1 represent estimates of critical charge for 45 nm

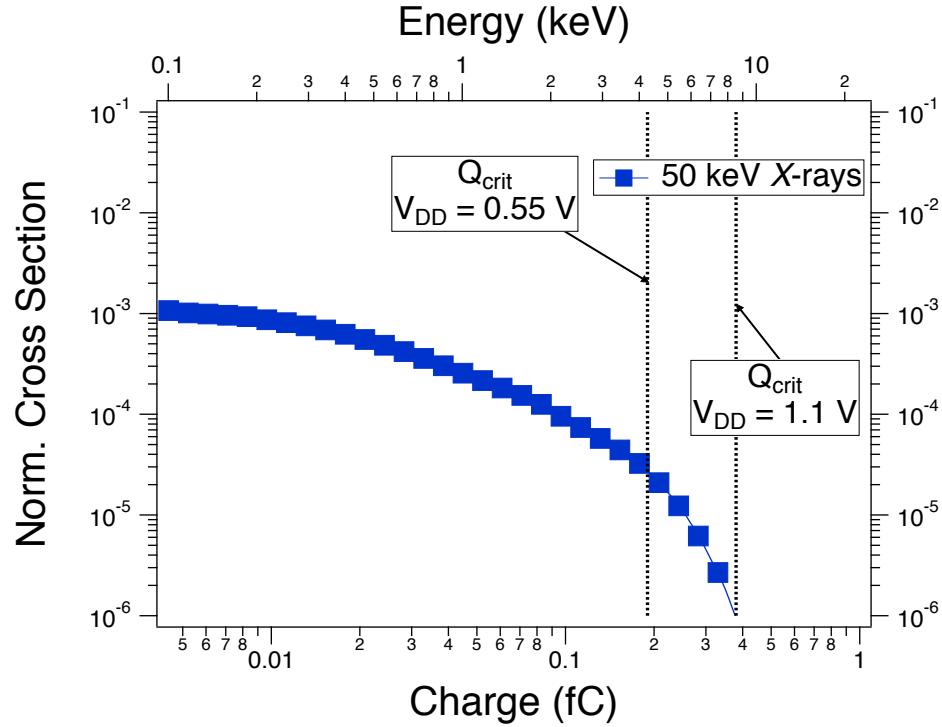


Figure 4.1 MRED simulation results of mono-energetic, 50 keV X -rays normally incident on a 45 nm bulk SRAM structure. The vertical black lines represent the lower-limit estimates of critical charge for a 45 nm SRAM. The results provide supporting evidence suggesting that energetic electrons generated by incident X -rays are capable of depositing sufficient energy to exceed the estimated upset threshold.

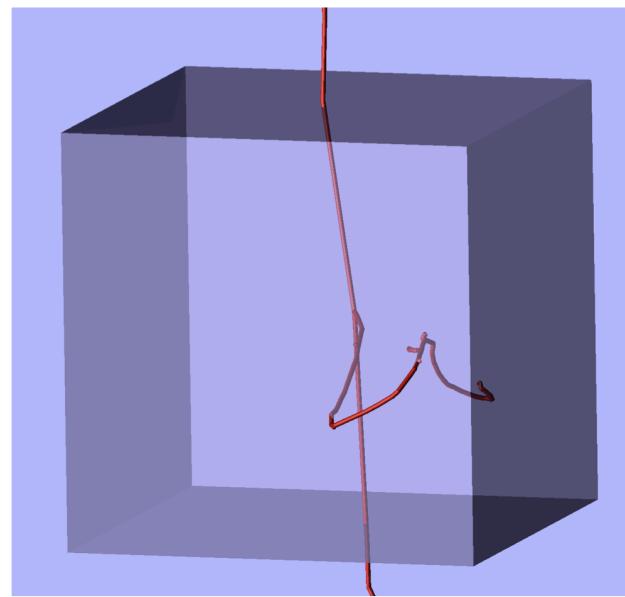
SRAMs as in [9] for supply voltages of 0.55 V and 1.1 V, which correspond to 0.19 fC and 0.38 fC of generated charge, respectively, and are used to indicate the charge generation required to upset cells.

Simulated integral cross-sections are shown in Fig. 4.1, indicating that secondary electrons generated by incident X -rays are capable of depositing sufficient energy to exceed the critical charge estimate of a 45 nm SRAM. The eventual upsets result from

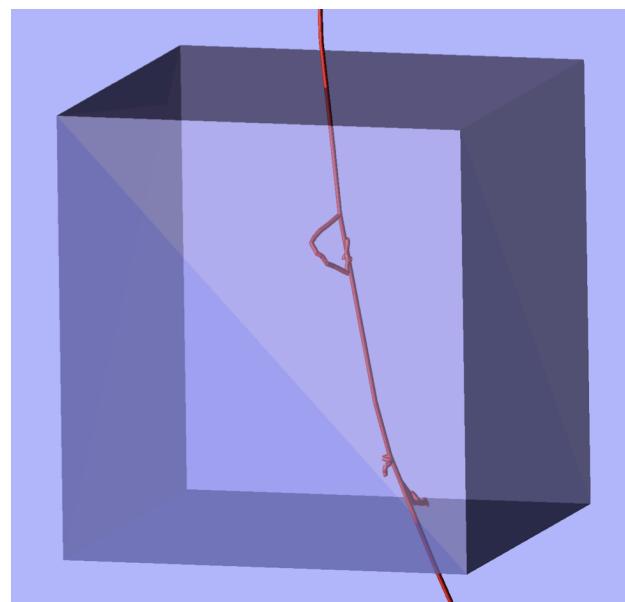
collection of thermalized electron-hole pairs generated by the high-energy electrons. These results, suggesting energetic electrons are capable of depositing sufficient ionizing energy to exceed the critical charge of 45 nm SRAMs operating under reduced supply voltage, are consistent with previous computational results reported in [9, 10]. The normalized cross-section in Fig. 4.1 at a supply voltage of 0.55 V agrees with experimental test results from Test Chip D in Fig. 3.7 within a factor of two. These results suggest that the 45 nm SRAM is relatively insensitive to single-electron SEU at nominal supply voltage, consistent with the SEU data in Fig. 3.7.

Further analysis of individual events shows that single electrons scattering within the sensitive volumes representative of sub-65 nm bulk and SOI technology frequently deposit energy in excess of the estimated critical charge thresholds in Fig. 4.1. Fig. 4.2 shows 10 keV electrons transporting through a 500 nm silicon cube and depositing 2.1 keV and 2.6 keV within an embedded 50 nm cube as shown in Figs. 4.2(a) and 4.2(b), respectively. Each event shown in Fig. 4.2 results in the generation of additional nearly free electrons, in either a single or multiple scattering events, that subsequently transport entirely within the sensitive volume structure, losing all of their energy and reabsorbing into the material. While the incident electron does not stop within the 50 nm silicon cube in either of the events depicted in Fig. 4.2, energy is transferred to secondary electrons. The total energy deposited in these volumes exceeds the estimation of critical energy required to produce a SEU in the sub-65nm nm bulk and SOI technology operated at reduced voltage [1].

These simulation results confirm that energy deposition from energetic electrons generated in photoabsorption events is the most likely explanation for the experimentally observed upsets in Fig. 3.7.



(a)



(b)

Figure 4.2 Incident 10 keV δ -rays are shown scattering in a 50 nm cube of silicon. Event 4.2(a) shows a 2.1 keV energy deposition event that produces additional δ -rays in a chain of inelastic scattering events. Event 4.2(b) shows a 2.6 keV energy deposition event that produces several tertiary δ -rays in a series of inelastic scattering events.

4.2 Electron-Induced SEU Event Rates

Comparing the experimental cross-sections in Figs. 3.9 and 3.10 indicates the sensitivity of SRAMs to protons, muons, and electron, but event rates depend on the flux of these particles for different environments. Trapped electrons form two different belts in the near Earth radiation environment, each with distinct characteristics [3,4].

Simulations were performed to estimate SEU event rates for trapped electrons at geosynchronous orbit during solar maximum with 150 mils of aluminum shielding using spectra obtained from the AE-8 model. The differential flux spectrum of incident electrons through 150 mils of aluminum shielding is plotted in Fig. 4.3. The presence of 150 mils of aluminum shielding was sufficient to stop the entire spectrum of protons under the same conditions. The trapped electron environment described in Fig. 4.3 is much more energetic than the generated electron spectrum used in *X*-ray experiments. The most energetic electrons at geosynchronous orbit during solar maximum have energy of approximately 5 MeV, which would require 500 mils of aluminum shielding to attenuate completely. MRED was used to model the interaction of the electron particle spectrum with the semiconductor materials. The material structure is identical to the structure from Fig. 4.1, corresponding to a 45 nm bulk SRAM.

Fig. 4.4 shows the resulting simulated event rates (left axis) as a function of generated charge (bottom axis) within the sensitive volume of a single SRAM cell. Electron energy deposition events rarely exceed 10 keV, which is consistent with Fig. 4.1 and [9,10]. Fig. 4.4 demonstrates the rare nature of electron-induced SEU events in the space radiation environment, indicating that many years of flight time may elapse before the observation of such an event is expected for a typical 45 nm bulk SRAM operating under nominal bias conditions. Fig. 4.4 shows that the event rate depends strongly on the critical charge of the SRAM; a reduction of critical charge

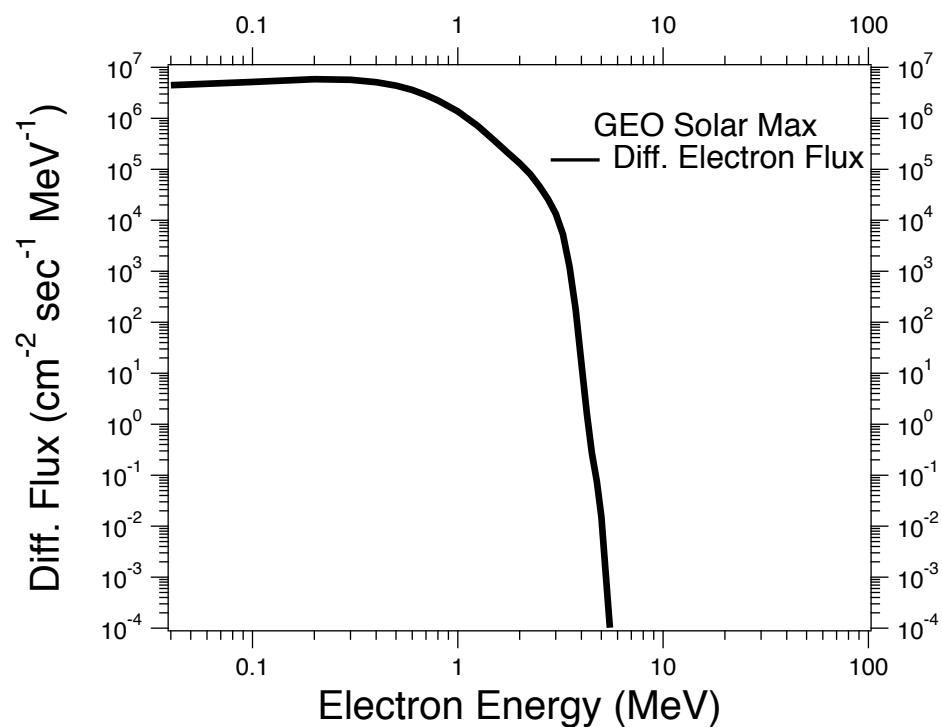


Figure 4.3 The differential flux spectrum of incident electrons is plotted using the AE-8 description of the electron environment, at geosynchronous orbit during solar maximum with 150 mils aluminum shielding. It is noted that 150 mils of aluminum is sufficient to shield the simulated SRAM from protons in this environment.

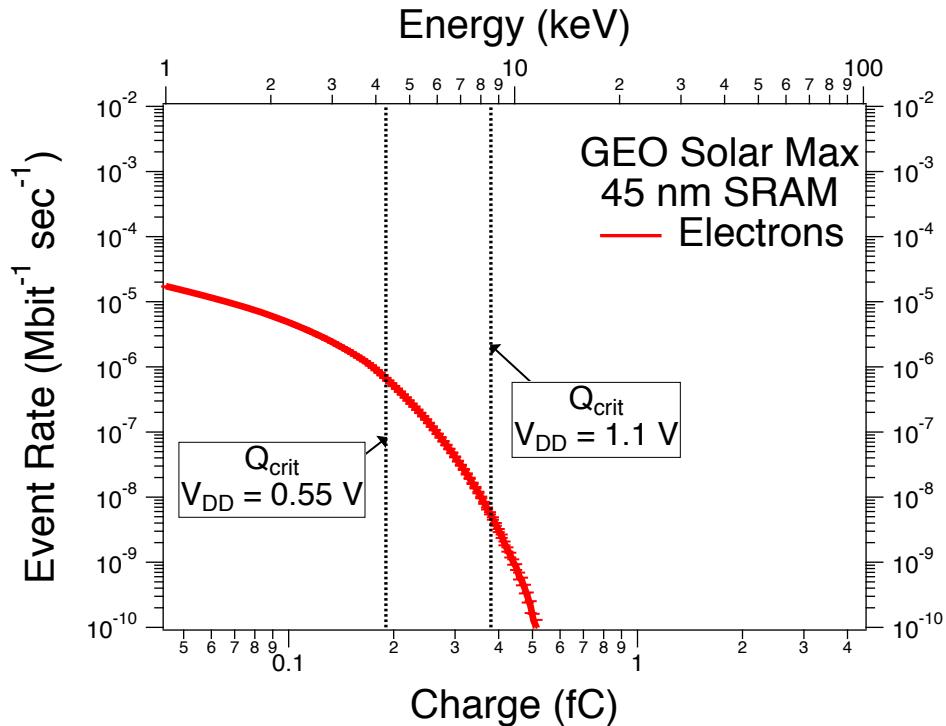


Figure 4.4 MRED simulations performed on the 45 nm structure from Fig. 4.1 using the AE-8 description of the electron environment, at geosynchronous orbit during solar maximum with 150 mils aluminum shielding. Simulation results show that the event rate of electrons is small for devices operated under nominal supply voltage, as seen in 4.4. However, more sensitive devices will experience a significant increase in single electron events. These results suggest that operating SRAMs under reduced bias conditions will result in a dramatic increase in single electron events.

from 0.4 fC to 0.2 fC results in a change in event rate of approximately two orders of magnitude. Employing more sensitive SRAM technologies or operating at reduced supply voltage conditions has a direct and significant impact on SRAM error rates. In contrast, total error rate predictions for a 65 nm SRAM at geosynchronous orbit in the solar minimum environment are on the order of 2.4×10^{-6} Mbit $^{-1}$ sec $^{-1}$ [14]. At geosynchronous orbit in “worst-day” conditions, error rates for the same 65 nm SRAM are as high as 3.6×10^{-3} Mbit $^{-1}$ sec $^{-1}$ [14]. This indicates that the error rates at geosynchronous orbit of larger technology nodes with higher critical charge are roughly 2.5–5 orders of magnitude higher than estimates of electron-induced error rates at nominal bias conditions.

4.3 Impact of Delta-rays on Microelectronics

In this section, single ionizing particles are simulated. The resulting tracks are analyzed, and energy deposited by δ -rays within small volumes is evaluated as a function of position within a large silicon structure. The evaluation volumes are 50 nm cubes, representing regions where energy deposition results in the generation and collection of charge that contributes to the device response.

The sensitive volume model and approach for evaluating upset events in SOI used in this section is consistent with [10, 70, 71]. The sensitive volumes are 50 nm cubes that are representative of typical active regions in modern SOI technology [71]. A concentric cylindrical target of silicon is utilized to characterize the radial dependence of energy deposition from the incident ion track structure; the thickness of the target structure is 50 μ m. The range of all incident particles evaluated in this section is much longer than the thickness of the target. The threshold for an upset event is defined as in previous sections, the amount of energy deposited in the sensitive volume required to generate the devices critical charge. IBM has reported their 65 nm SOI

technology node to have a critical charge between 0.14-0.28 fC [1], which corresponds to energy deposition of 3.15-6.3 keV within the sensitive volume. Additionally, the critical charge estimate of 0.08 fC for upset from [70] corresponds to 1.8 keV of energy deposited within the sensitive volume and is used to evaluate the sensitivity of future technology nodes. It is assumed that energy below this threshold does not result in an upset event, and energy deposition greater than or equal to the threshold results in an upset.

Events are simulated using He and Ne ions; the energy distribution of δ -rays generated will be similar for fixed incident ion energy, their generation rate will depend on the incident ion LET. The target geometry is chosen to be cylindrically symmetric about the incident ion path, energy deposition is evaluated as a function of orthogonal distance from the trajectory of the incident ion. The energy deposited within a 50 nm cube is sorted by the orthogonal distance from the incident ion trajectory and the magnitude of energy deposited. The resulting histograms are described by a function $f(E, R)$ which represents the differential energy spectrum in a 50 nm cube at radius R .

Using this method, the sensitive volumes generated consistently account for the largest energy deposited by the ensemble of δ -rays in a local region of target material during a simulated heavy-ion event. Consequently, this calculation represents a worst-case analysis of “track structure” contributions to SEUs. The representation of a 560 MeV N event using this technique can be seen in Fig. 4.5. Each cube represents the location of energy deposited by δ -ray(s) and illustrates the spatial non-uniformity and variation in magnitude of δ -ray energy deposition events along their trajectory. The color intensity scale shows the magnitude of energy deposited, where warmer colors, red for example, represent larger energy deposition events and cooler colors, such as green, represent smaller energy deposition. This allows the visual representation of

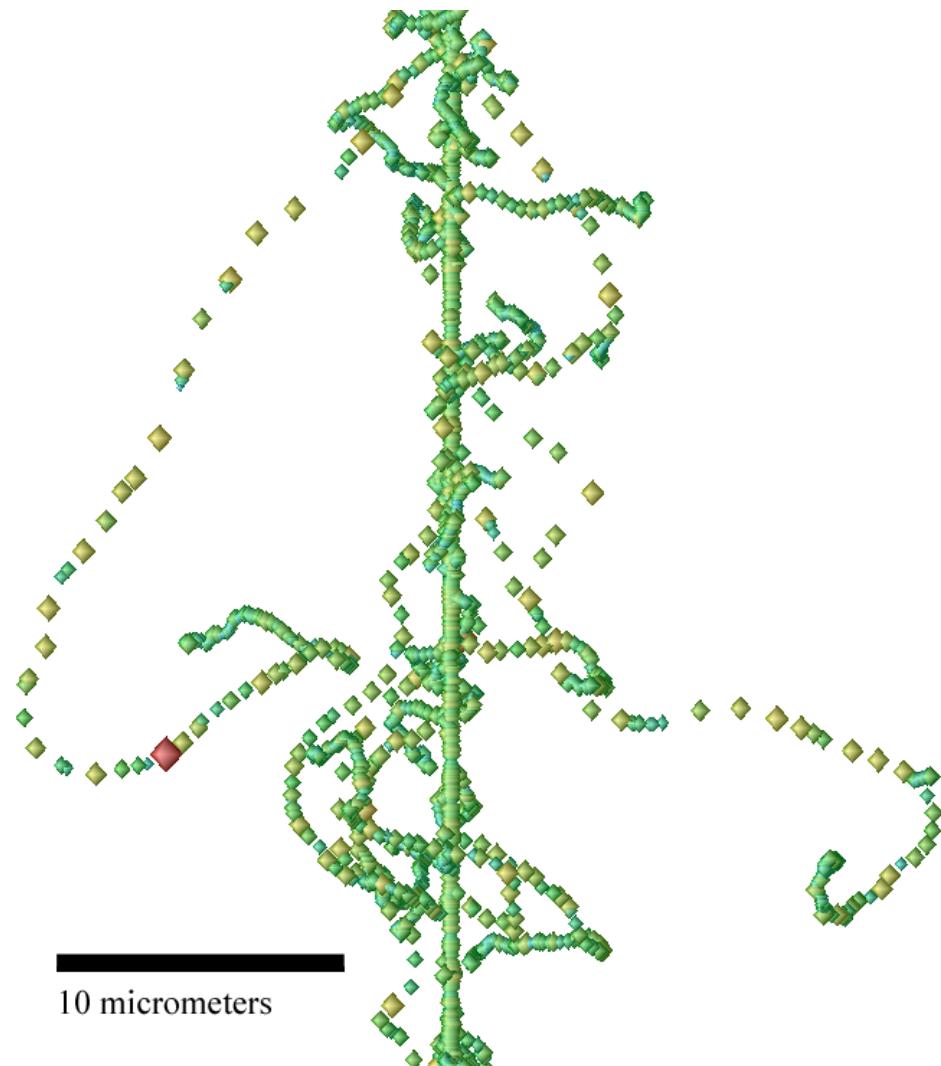


Figure 4.5 Representation of the energy deposition from δ -rays generated by a single 560 MeV N ion incident on a large silicon structure. Each box represents the energy deposited by δ -rays in a specific region. The magnitude of energy deposited at each location is represented as color intensity, where warmer colors are larger energy deposition events.

heavy-ion track structure and identification of the spatial location of large energy deposition events.

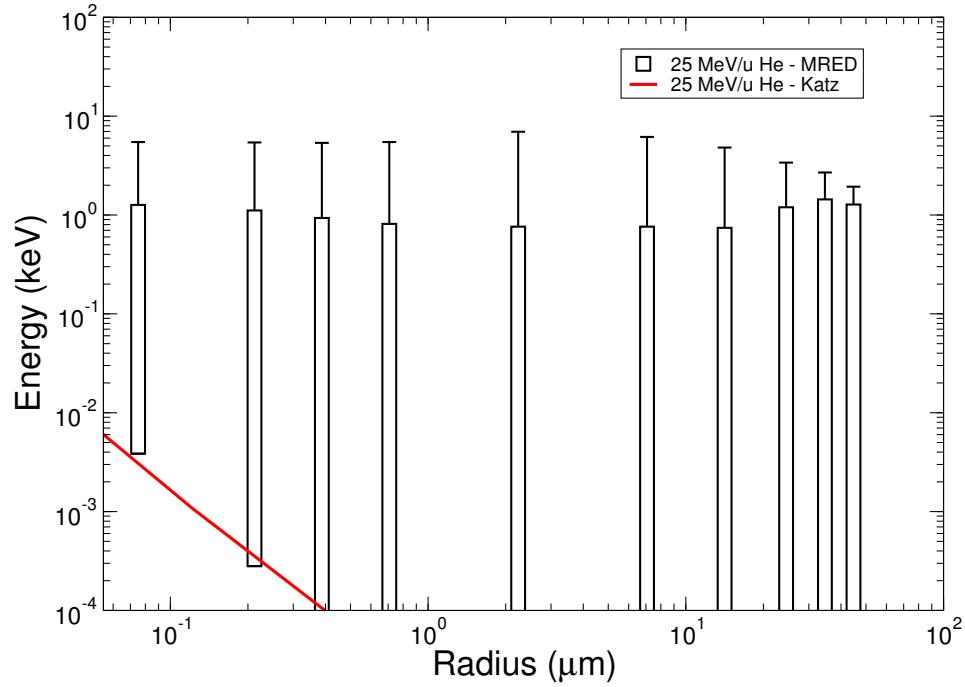


Figure 4.6 Simulation results show good agreement for energy deposited within a 50 nm cube by the Katz model (solid red line) and MRED for 25 MeV/u He. The lower edge of the box is the average energy, the upper edge of the box is the 90th percentile event, and the whisker is the largest energy deposition event. While the average energy within a 50 nm cube shows a strong dependence on the radial distance, MRED shows that large energy deposition events occur at radial distances greater than 10 μm .

Figs. 4.6 and 4.7 compare the energy deposited within a 50 nm cube for the analytical expectation of the Katz model,[58, 59] shown as the solid red line, with results obtained using MRED, represented by the box and whisker data set in black. MRED data represents the average energy within a 50 nm cube, shown as the lower edge of the box, the 90th percentile of events, shown as the upper edge of the box, and the whisker, representing the largest energy deposition event observed. Simulation results indicate that MRED agrees well with the Katz model expectation of energy within a 50 nm cube as shown by the lower edge of each box and the red line. The

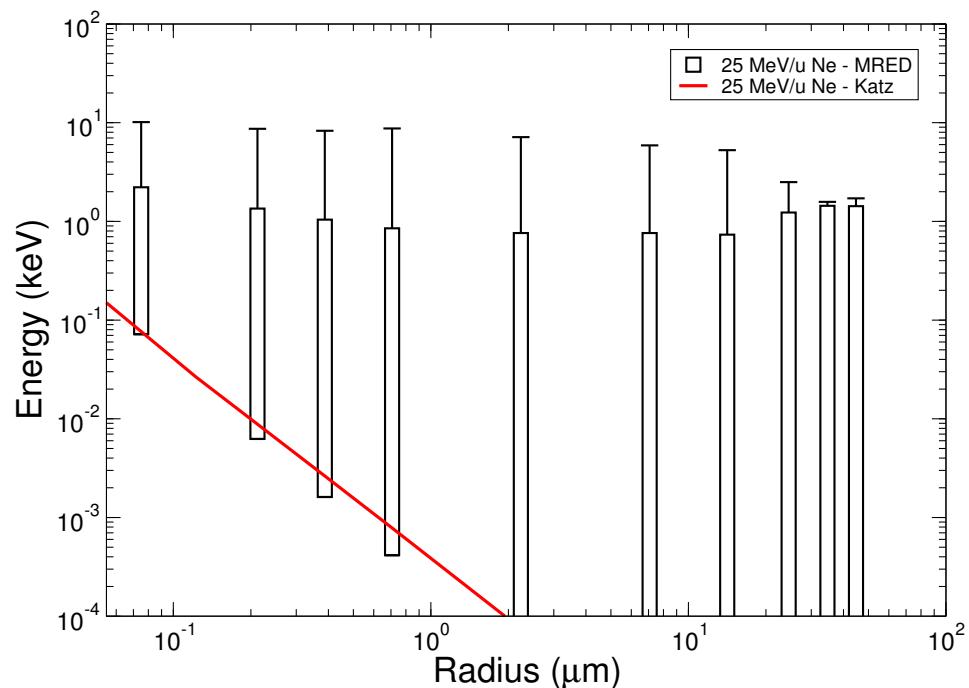


Figure 4.7 Simulation results show good agreement for energy deposited within a 50 nm cube by the Katz model (solid red line) and MRED for 25 MeV/u Ne. The lower edge of the box is the average energy, the upper edge of the box is the 90th percentile event, and the whisker is the largest energy deposition event. Large energy deposition events are again shown to occur at radial distances larger than 10 μm .

Katz model expectation represents the total energy deposited within a cylindrical shell for a single ion event. Figs. 4.6 and 4.7 demonstrate that the Katz model contains no information regarding the frequency or magnitude of individual energy deposition events involving δ -rays. Individual scattering events may deposit significantly more energy within a 50 nm cube than the average would predict, as illustrated by the 90th percentile and extreme values shown in Figs. 4.6 and 4.7. Information regarding the magnitude of energy deposited and spatial resolution of individual δ -ray scattering events is lost when averaging the total energy deposited in large volumes, as in the Katz model.

MRED indicates that δ -ray scattering events can deposit up to 10 keV of energy within a 50 nm cube at radial distances tens of micrometers away from the incident ion trajectory. By contrast, the average energy obtained from Katz model is less than 3.6 eV, the average energy required to produce a single eh pair in silicon, after several hundred nanometers for both 25 MeV/u He and Ne. Under-predicting the magnitude of energy deposited results in inaccurate charge generation and collection profiles. Scaling the expected energy deposition obtained using the Katz model into small volumes introduces error and results in inaccurate conditions for evaluating the device response. Figs. 4.6 and 4.7 demonstrate that MRED captures a level of detail greater than the Katz model provides, allowing further analysis of δ -ray events and their impact on device response.

Events occurring more than 25 μm from the incident ion trajectory are near the maximum range of δ -rays generated by 25 MeV/u He and Ne and occur with a frequency up to six orders of magnitude lower than those of events at smaller radial distances. Fifty micrometers is therefore used as the evaluation limit in these simulations. The δ -rays involved in energy deposition events at radial distances greater than 25 μm are near their stopping range, which results in a reduction in the maximum

energy deposition event and increase in the 90th percentile event as seen in Figs. 4.6 and 4.7.

The differential energy spectrum $f(E, R)$ is represented as a cumulative energy distribution by the expression

$$\frac{d}{dx}F(E_i, R) = \frac{1}{\theta(R)N} \frac{l_{cube}}{x} \sum_{j \geq i}^{\infty} f(E_j, R) \quad (4.1)$$

where R is the orthogonal distance from the incident particle trajectory, N is the number of incident particles evaluated, l_{cube} is the side length of an evaluation volume parallel to the z -axis, x is the ion path length through the target material, $\theta(R)$ is the (one-dimensional) solid angle subtended by a cubic volume at an orthogonal distance R from the incident particle trajectory, and $f(E, R)$ is the differential energy distribution. The formulation of Eq. 4.1 for a single ionizing particle event represents the probability per radian of observing a δ -ray energy deposition event greater than or equal to E_i . Equivalently, Eq. 4.1 represents the probability of a single ionizing particle event depositing a given amount of energy, E_i , or more within a cube with dimensions l_{cube} at a distance R . Normalizing to the thickness of the evaluation volume, l_{cube} , and total thickness of the target material, x , reduces the problem to a two dimensional space in the plane normal (the $y - z$ plane) to the incident ion trajectory. Because the target geometry is cylindrically symmetric about the incident ion path, normalizing to the angle θ allows a direct comparison of the probability to observe events of a given energy magnitude or greater at different radial distances from the incident ion trajectory.

From this, relationships about the frequency of δ -ray events at different radial distances can be inferred. When Eq. 4.1 evaluates close to unity, this implies a high likelihood of observing an event of a given magnitude within a geometric volume at a particular distance. A reduction in the frequency of events with increasing distance

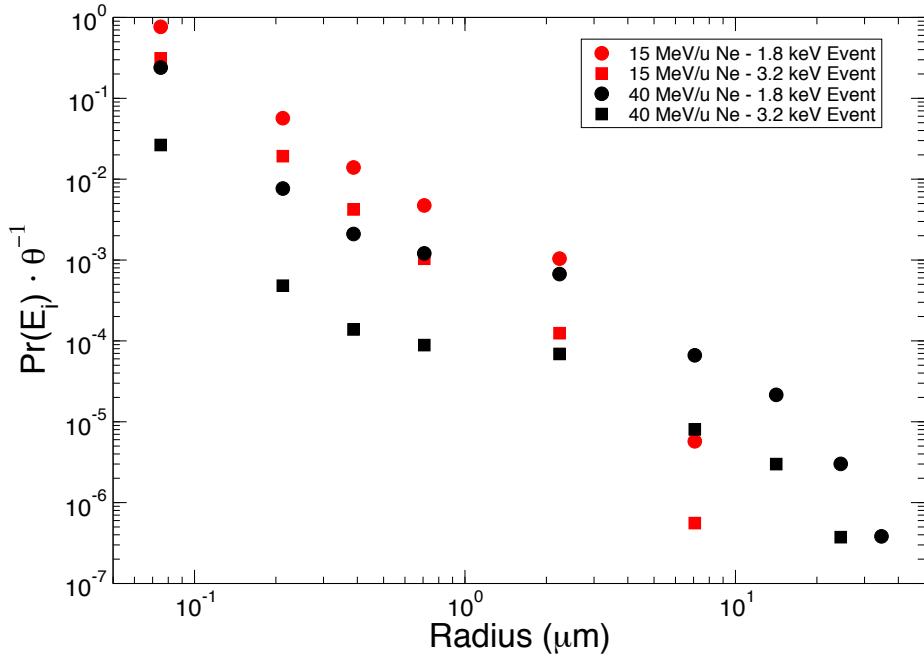


Figure 4.8 Cumulative energy distribution as a function of radial distance for 15 MeV/u and 40 MeV/u Ne ions. Results show the frequency of δ -ray energy deposition events depend on LET and energy of the incident particle.

indicates the termination of δ -ray trajectories.

Fig. 4.8 plots the cumulative energy distribution calculated by Eq. 4.1 as a function of radial distance for one thousand simulated particle events. Data points are plotted for energy deposition events greater than or equal to 1.8 keV and 3.2 keV within a 50 nm cube for 15 MeV/u and 40 MeV/u Ne. These incident ion energies are representative of several energy tunes available at the TAMU cyclotron facility. The corresponding LETs are 2.6 MeV·cm²/mg and 1.2 MeV·cm²/mg, respectively. Scattering and stopping of δ -rays is evident in Fig. 4.8 due to the construction of Eq. 4.1 and is shown by the decreasing probability of events with increasing distance. Fig. 4.8 also indicates that smaller energy deposition events occur much more frequently than larger energy deposition events as shown by the 1.8 keV curves compared to the 3.2 keV curves. The relationships shown in Fig. 4.8 also show that while

large energy deposition events, on the order of 1 keV or more, may occur at radial distances tens of micrometers from an incident ion path, as indicated in Figs. 4.6 and 4.7, the likelihood of such events occurring decreases with increasing distance from the incident ion path.

This suggests that the regions mostly likely to be affected by δ -rays in a single ionizing particle event are likely to occur within five micrometers surrounding the incident ion strike location, the distance at which the likelihood of an event depositing sufficient energy to exceed the estimated critical charge of a 22 nm SRAM falls below $Pr(E_i) = 10^{-6}$.

Fig. 4.8 also illustrates the role of incident ion LET and energy in δ -ray events. At radii near the incident ion trajectory, higher LET particles have a higher probability of depositing large amounts of energy than lower LET particles. This is easily observed in the relative frequency of 1.8 keV energy deposition events for 15 MeV/u Ne compared to 40 MeV/u Ne. This is due primarily to the generation of many low-energy, short-range δ -rays depositing energy around the incident ion's trajectory. The maximum transferable energy from Eq. 2.8 limits the radial extent of the ion track radius, as shown by decreasing probability of energy deposition events with increasing distance from the incident ion trajectory. Consequently, higher energy incident particles can produce undesirable effects in microelectronics at larger radial distances and with greater frequency than lower energy ions.

Monte-Carlo simulation results indicate that in technology nodes where less than 0.5 fC of charge result in circuit-level effects, δ -rays may contribute to the upset error rate. A comparison of MRED with the Katz model demonstrates average track structure models alone are inadequate in capturing the device response. The probability of δ -ray related effects exhibits a strong dependence on both incident ion energy and LET. Additionally, the likelihood of δ -ray induced effects exhibits a strong dependence

on radial distance from the incident ion path.

These results have strong implications for ground-based parts qualification testing and space radiation environments, where varying incident ion energy and LET result in differing contributions from δ -rays to device and circuit level effects.

Chapter 5

Summary and Conclusions

Evidence of single electron-induced SEU in 28 and 45 nm CMOS SRAMs is presented. Energetic electrons are generated by exposure of the SRAMs to an *X*-ray source and an aluminum attenuator.

The experimental SEU cross-sections depend exponentially on applied bias, consistent with previous experimental results obtained with muons and low-energy protons. No errors were observed in functionality and parametric testing before and after irradiation of all test chips under all applied bias conditions. This demonstrates that test chips remained stable during *X*-ray irradiation. Thus, errors are not due to “weak bits” or photocurrents resulting from the collective energy deposition of the *X*-rays. Instead, experimental results and analysis strongly suggest that the observed errors are the result of single energetic electron scattering events within SRAM cells.

The event rate of electron-induced SEU is low at geosynchronous orbits for the devices that were evaluated. Moreover, electron-induced upsets only occur at measurable rates under reduced bias conditions for present-generation technology. This suggests that the overall contribution of energetic electrons to error rates is small in present-generation technology. The conclusion being that electronics designed to operate with ultra-low power likely will exhibit higher relative sensitivity to ener-

getic electron induced upsets. This represents an additional design concern for both space and terrestrial environments, to avoid unexpectedly high upset/error rates from lightly ionizing particles.

Monte Carlo radiation transport simulation results indicate that in technology nodes where less than 0.5 fC of charge result in circuit-level effects, δ -rays generated in heavy-ion irradiation may contribute to the single- and multiple-bit error rate. Error rates of δ -ray and electron-induced upsets for SRAMs in ground-based parts qualification testing and the space radiation environment are likely dominated by extreme energy deposition events. A comparison of MRED with the Katz model demonstrates average track structure models alone are inadequate in capturing the SEU response of small sensitive geometries with low critical charge that are susceptible to electron/ δ -ray effects. The probability of δ -ray related effects exhibits a strong dependence on the incident ion species, energy, and LET. Additionally, the probability of δ -ray induced effects exhibits a strong dependence on radial distance from the incident ion trajectory. These results have strong implications for ground-based parts qualification testing and space radiation environments, where varying incident ion energy and LET result in differing contributions from δ -rays to device and circuit level effects.

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