8-BIT SIGMA DELTA ANALOG TO DIGITAL CONVERTER

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Abstract

Data converter plays very important role in all communication system. In today's CMOS technology and mixed signal design, ADC with low noise and low power consumption are in major demand. As the complexity of System-on-Chip (SoC) increases, the requirement to reduce chip area, power consumption optimization, noise shaping made these converters the preferred choice. Sigma-Delta ADC based on oversampling technique which provides better noise rejection with low power consumption. The mixed-signal approach combines the analog and digital work flow to reduce costs and verification time in development.

Reference Circuit Diagram

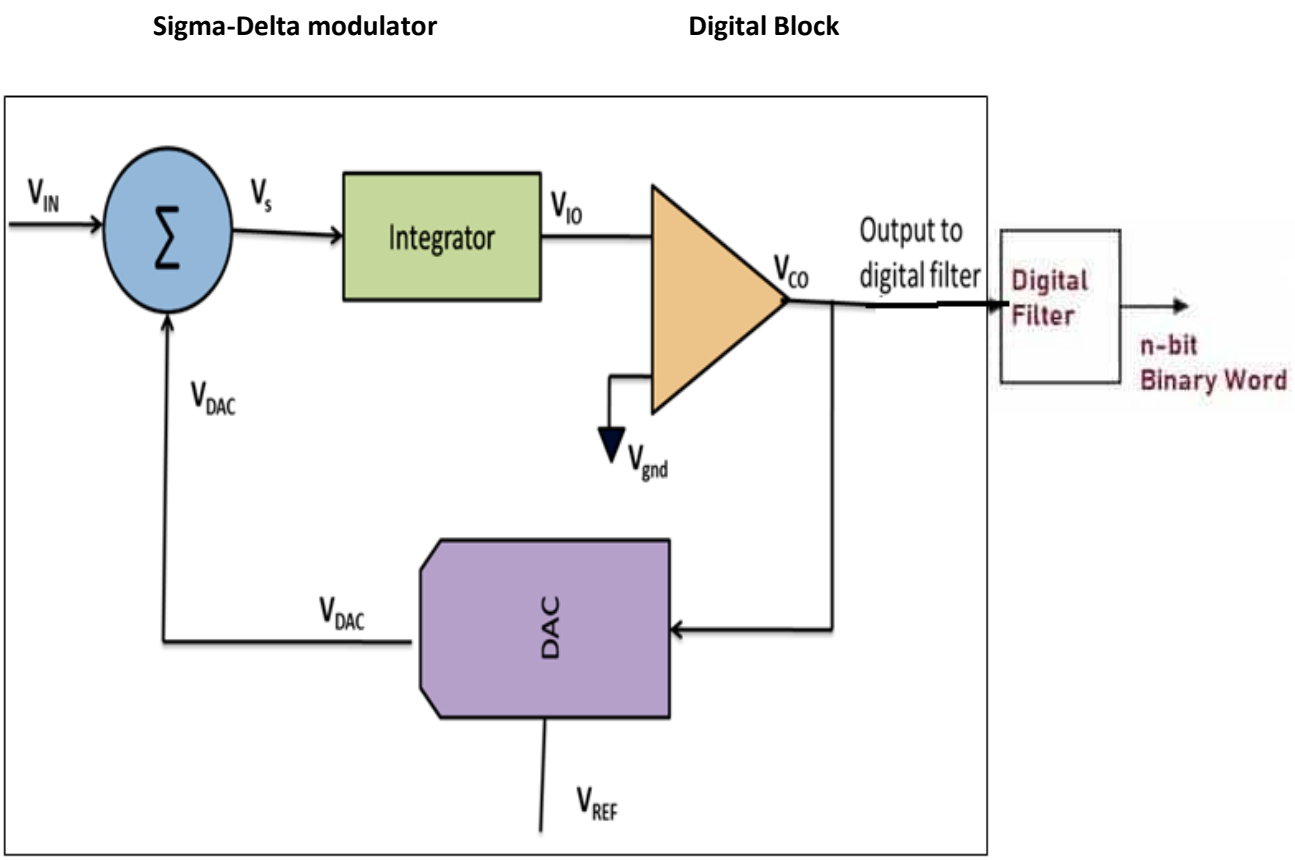


Figure 1 Sigma-Delta Analog to Digital Converter

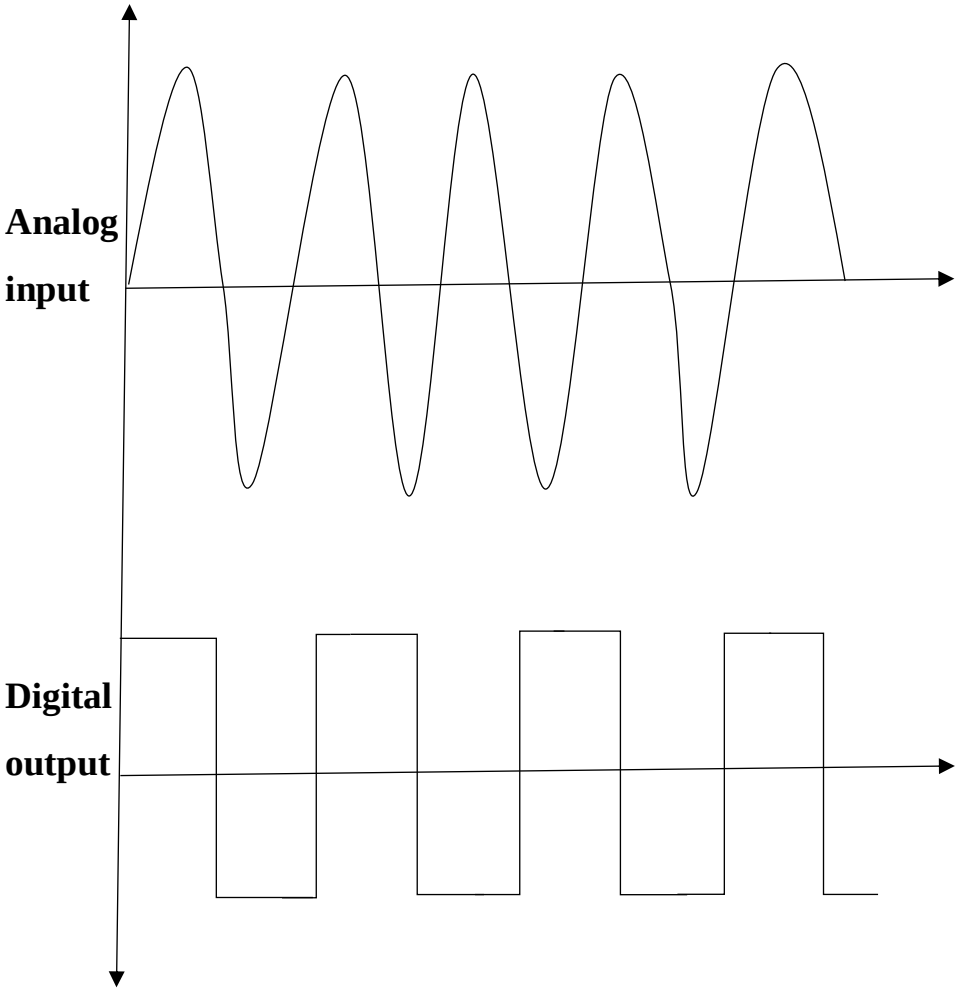
Circuit Details

A sigma-delta ADC consists of an analog block of modulator and a digital block of decimator. The modulator samples the input signal at an oversampling rate, generating a one-bit output stream and decimator is a digital filter or down sampler where the actual digital signal processing is done. The modulator block contains a summing amplifier, an integrator, a comparator and a digital to analog converter. The ADCs also contain a digital filter, which lets them work at a high oversampling rate without a separate anti-aliasing filter at the input.

The principle of operation can be understood from the circuit diagram shown in figure 1. The input voltage Vin sums algebraically with the output voltage of the DAC, and the integrator adds the summing point output Vs to a value it stored previously. When the integrator output is equal to or greater than zero, the comparator output switches to logic one, and when the integrator output is less than zero, the comparator switches to logic zero.

The DAC modulates the feedback loop, which continually adjusts the output of the comparator equal to the analog input and maintain the integrator output at zero. The DAC keeps the integrator's output near the reference voltage level. Through a series of iterations, the output signal becomes a one-bit data stream (at a high sample rate) that feeds a digital filter. The digital filter averages the series of logic ones and zeros, determines the bandwidth and settling time, and outputs multiple-bit data.

Reference Waveform



Truth table

Sample Number(n)	V_{IN}	V_S	V_{IO}	V_{CO}	V_{DAC}
1	**1/2**	**0**	**0**	**0**	**0**
2	**1/2**	**1/2**	**1/2**	**1**	**+1**
3	**1/2**	**-1/2**	**0**	**1**	**+1**
4	**1/2**	**-1/2**	**-1/2**	**0**	**-1**
5	**1/2**	**3/2**	**1**	**1**	**+1**
6	**1/2**	**-1/2**	**1/2**	**1**	**+1**
7	**1/2**	**-1/2**	**0**	**1**	**+1**
8	**1/2**	**-1/2**	**-1/2**	**0**	**-1**
9	**1/2**	**3/2**	**1**	**1**	**+1**
10	**1/2**	**-1/2**	**1/2**	**1**	**+1**

Software Used

eSim

eSim is an Open-Source EDA tool for circuit design, simulation, analysis and PCB design. It is developed by FOSSEE, IIT Bombay. It can serve as an alternative to commercially available/licensed software tools like OrCAD, Xpedition and HSPICE.

For more details refers:

https://esim.fossee.in/home

NgSpice

Ngspice is an open-source mixed-level/mixed-signal electronic circuit simulator. NgSpice offers a wealth of device models for active, passive, analog, and digital elements.

For more details refer:

http://ngspice.sourceforge.net/docs.html

Circuit Diagram in eSim

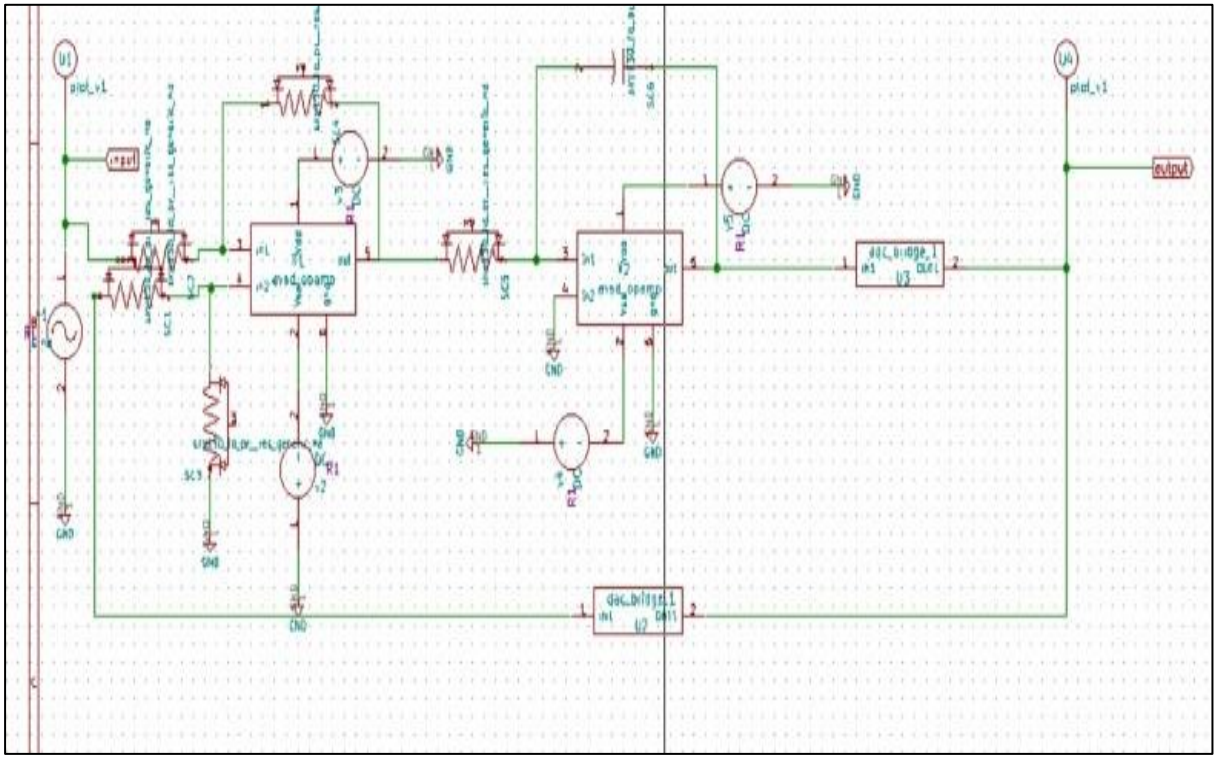


Figure 2 Schematic of Sigma-Delta Analog to Digital Converter in eSim

Acknowledgements

1. FOSSEE, IIT Bombay
2. Kunal Ghosh, Co-founder, VSD Corp. Pvt. Ltd. - kunalpghosh@gmail.com
3. Sumanto Kar, eSim Team, FOSSEE

References

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[3] Tembhre, Y. and Sahu, A.K., 2016, September. Testing of an 8-bit Sigma Delta ADC Based on Code Width Technique Using 45nm Technology. In 2016 International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE) (pp. 416-420). IEEE.