Towards cache-optimal address allocation:

How slow is your code?

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Master's Thesis

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University of Salzburg

Problem Statement

Given a trace T of load and store instructions

find metrics that characterize the trace performance
for a given cache C and

implement an execution engine for computing their
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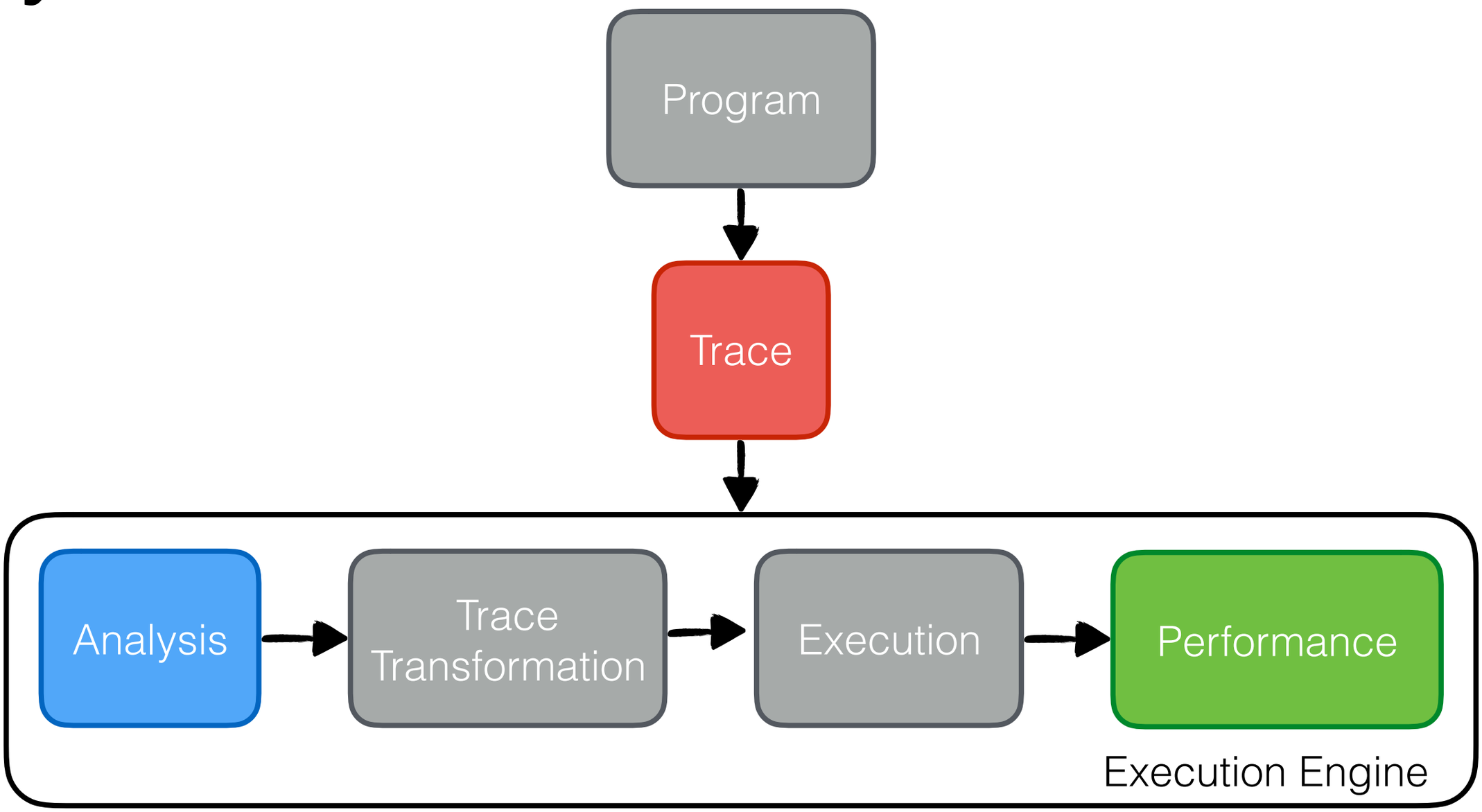
Collaboration with Alexander Miller

Overview
System



Preparation
Memory Access Trace

```
void main ()
{
   int sum, x, y, z;
   sum = 0;
   x = 1;
   y = 2;
   sum = sum + x;
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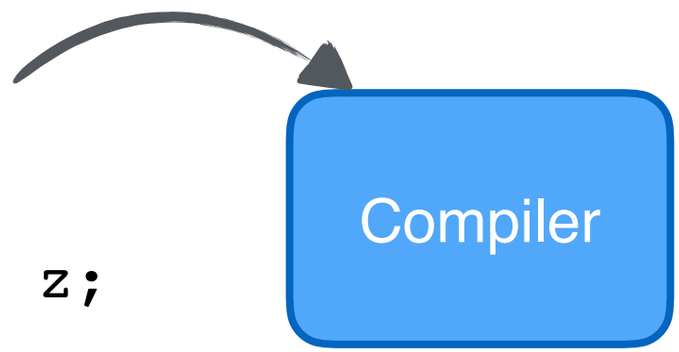


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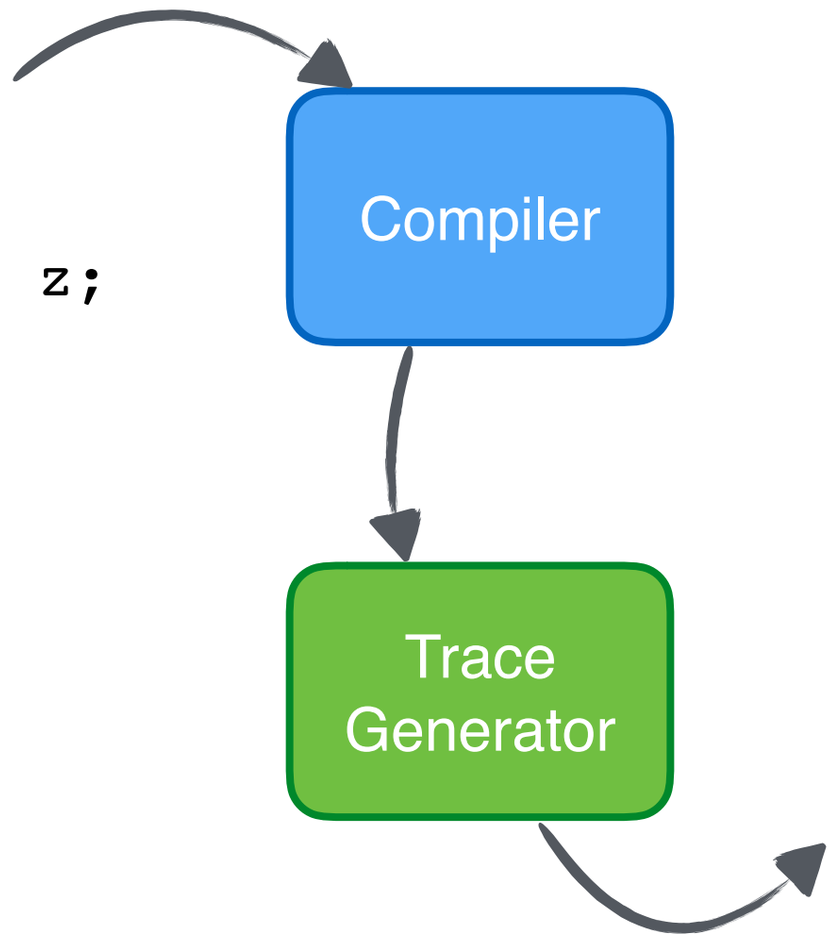


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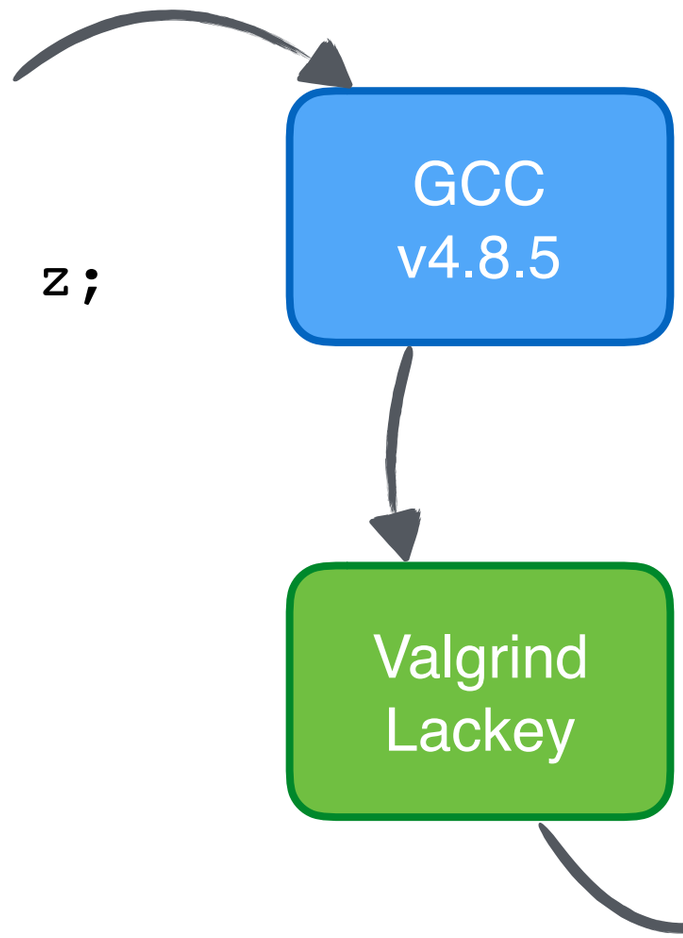


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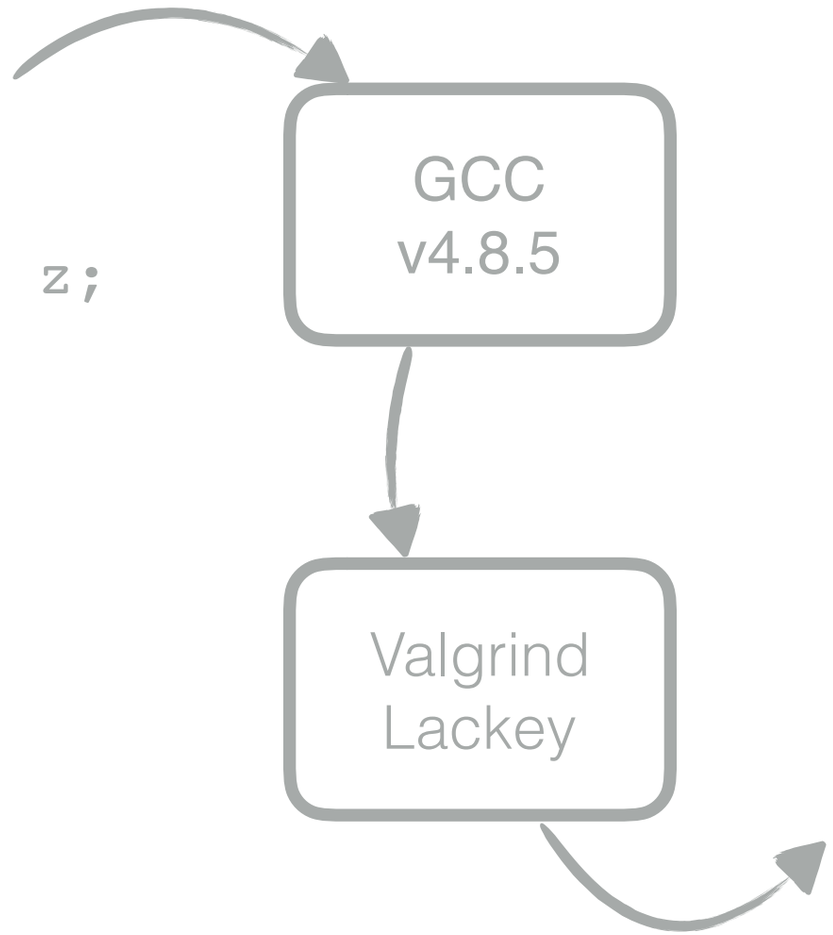


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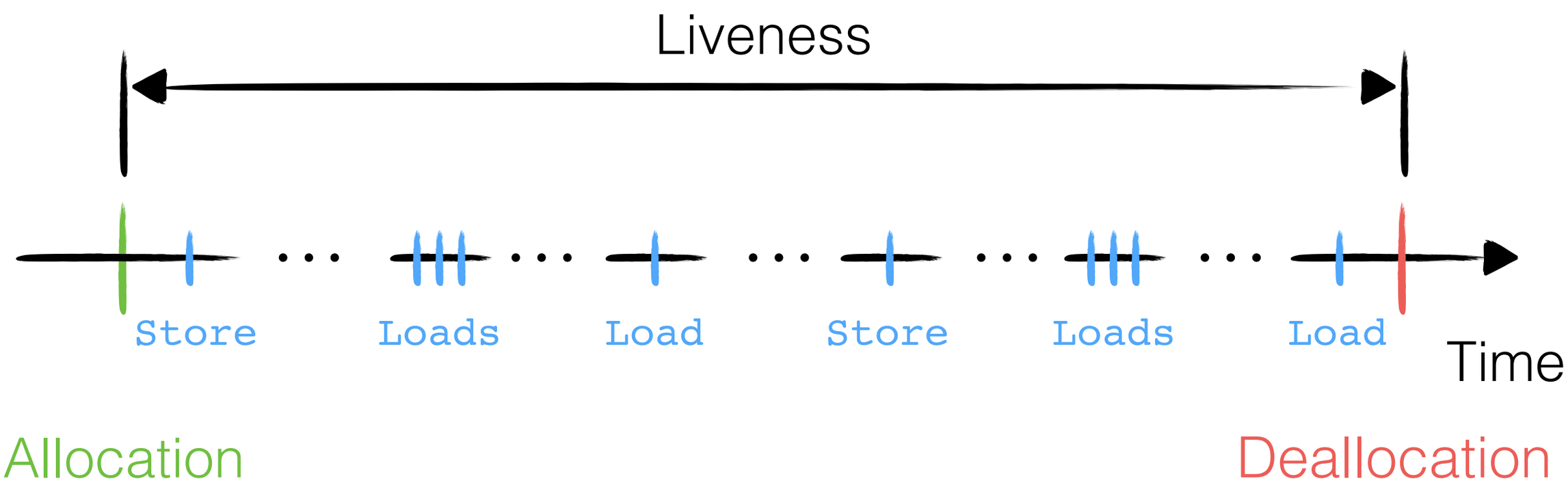
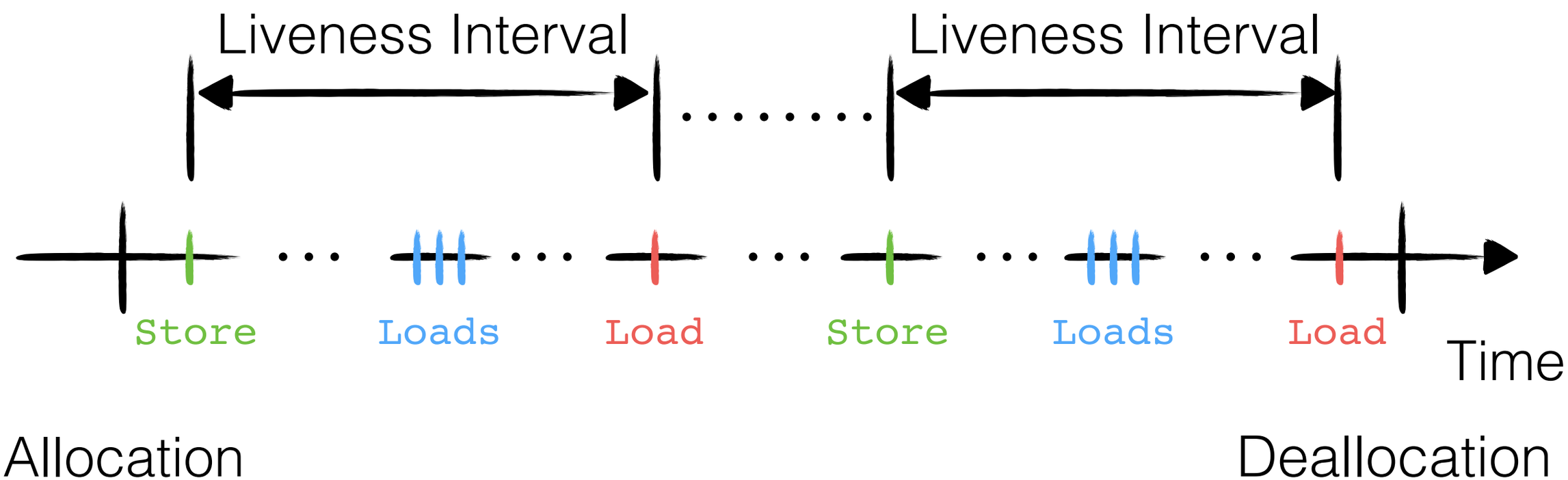
Analysis
Liveness



Analysis
Liveness Intervals (LI)



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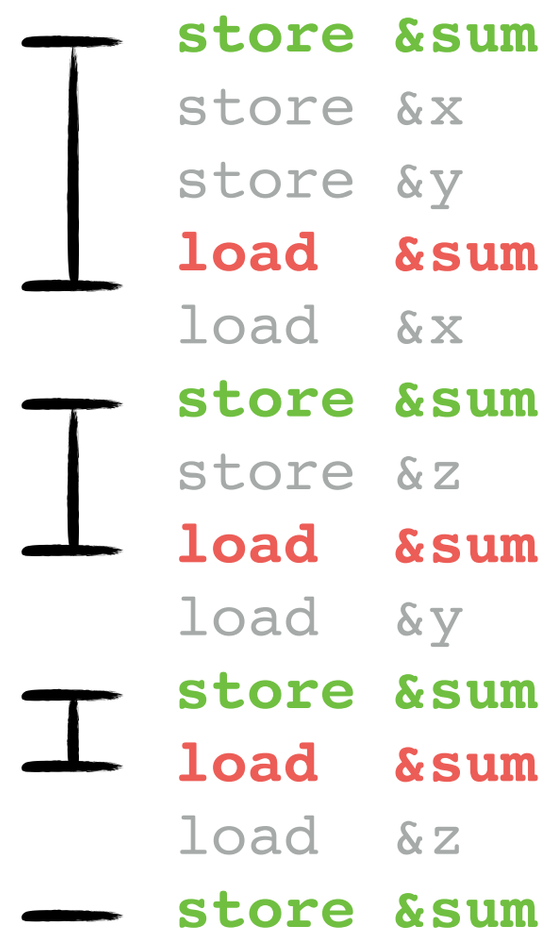
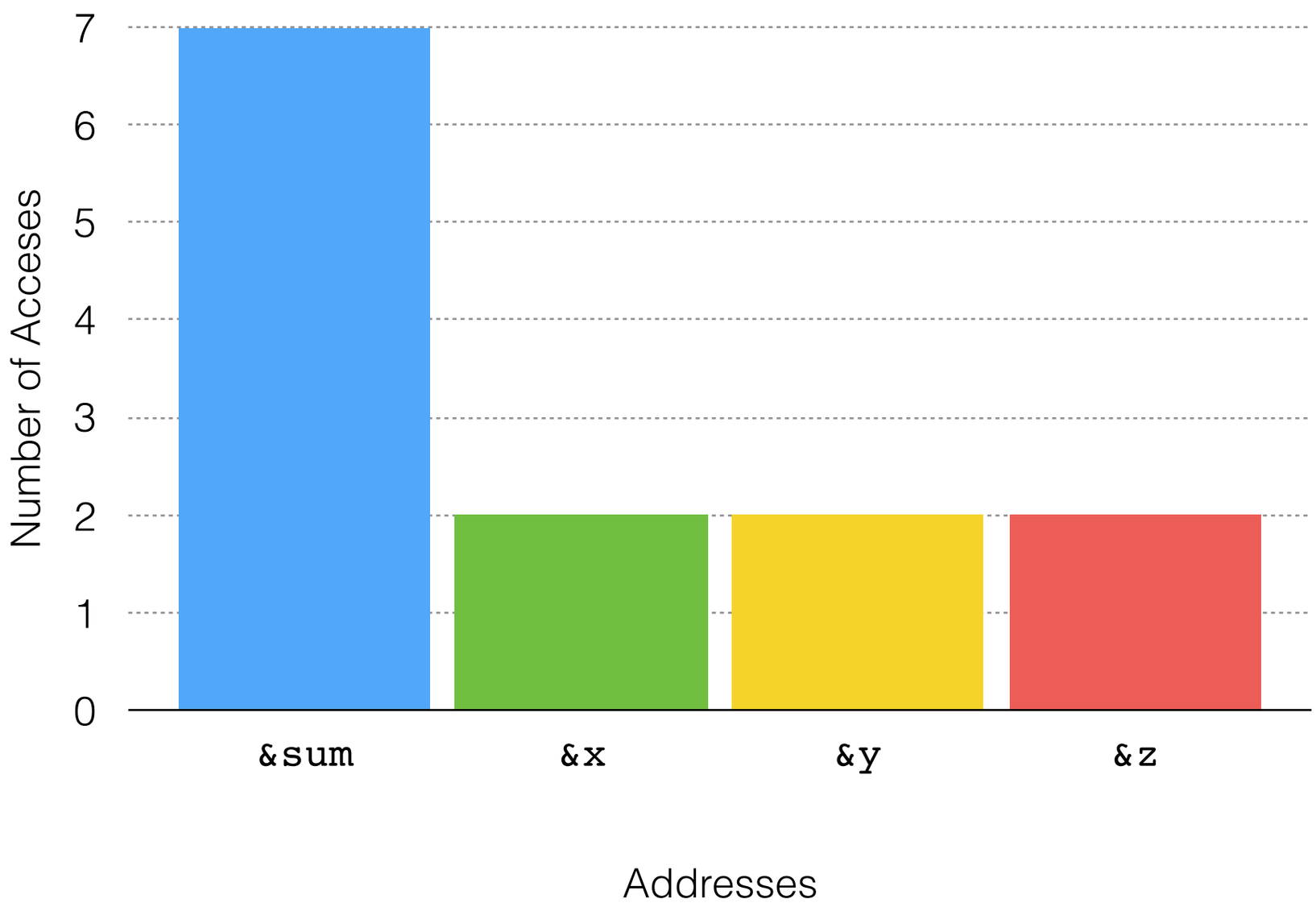


Analysis
Metric: Accesses

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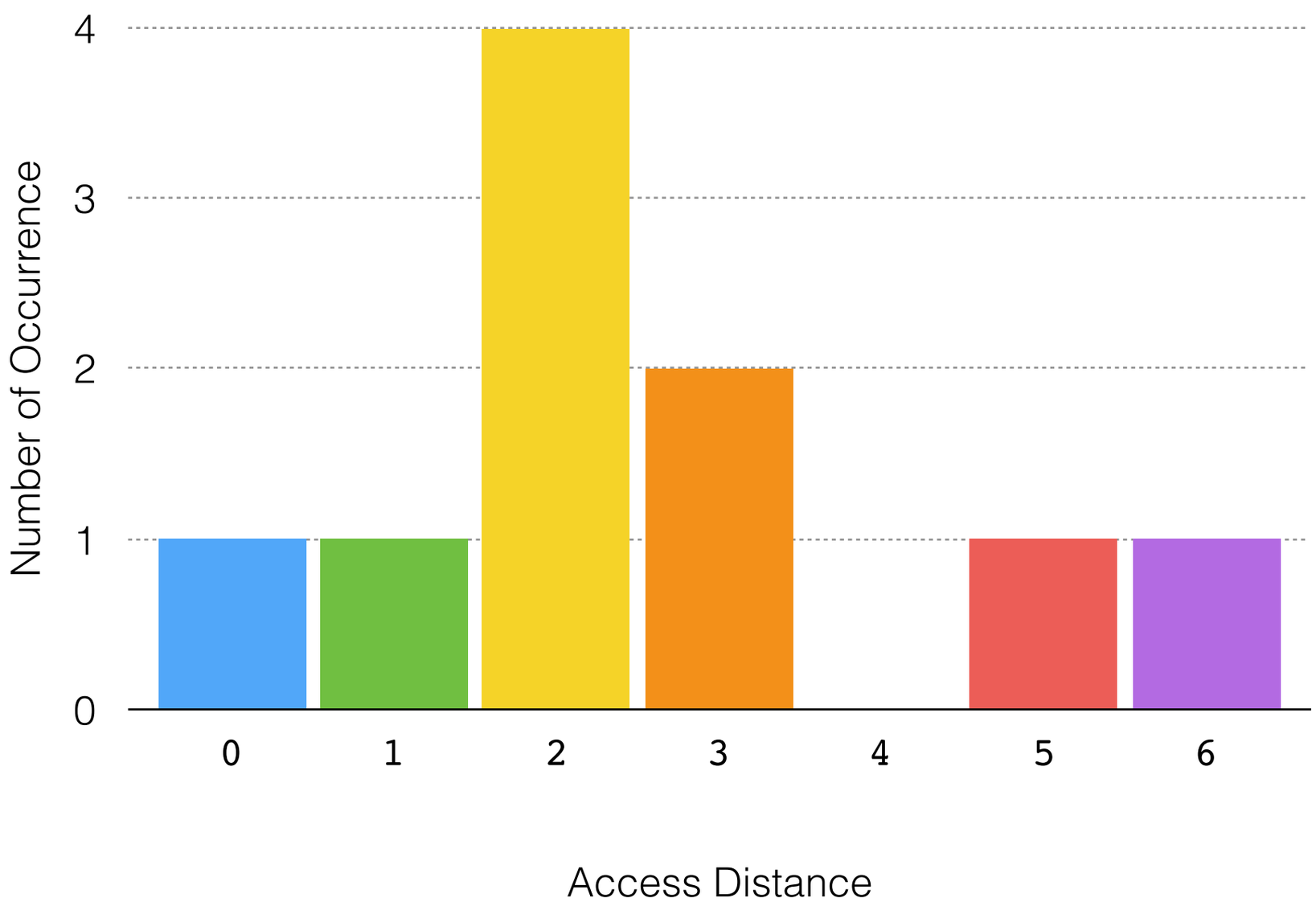
Analysis

Metric: Access Distance

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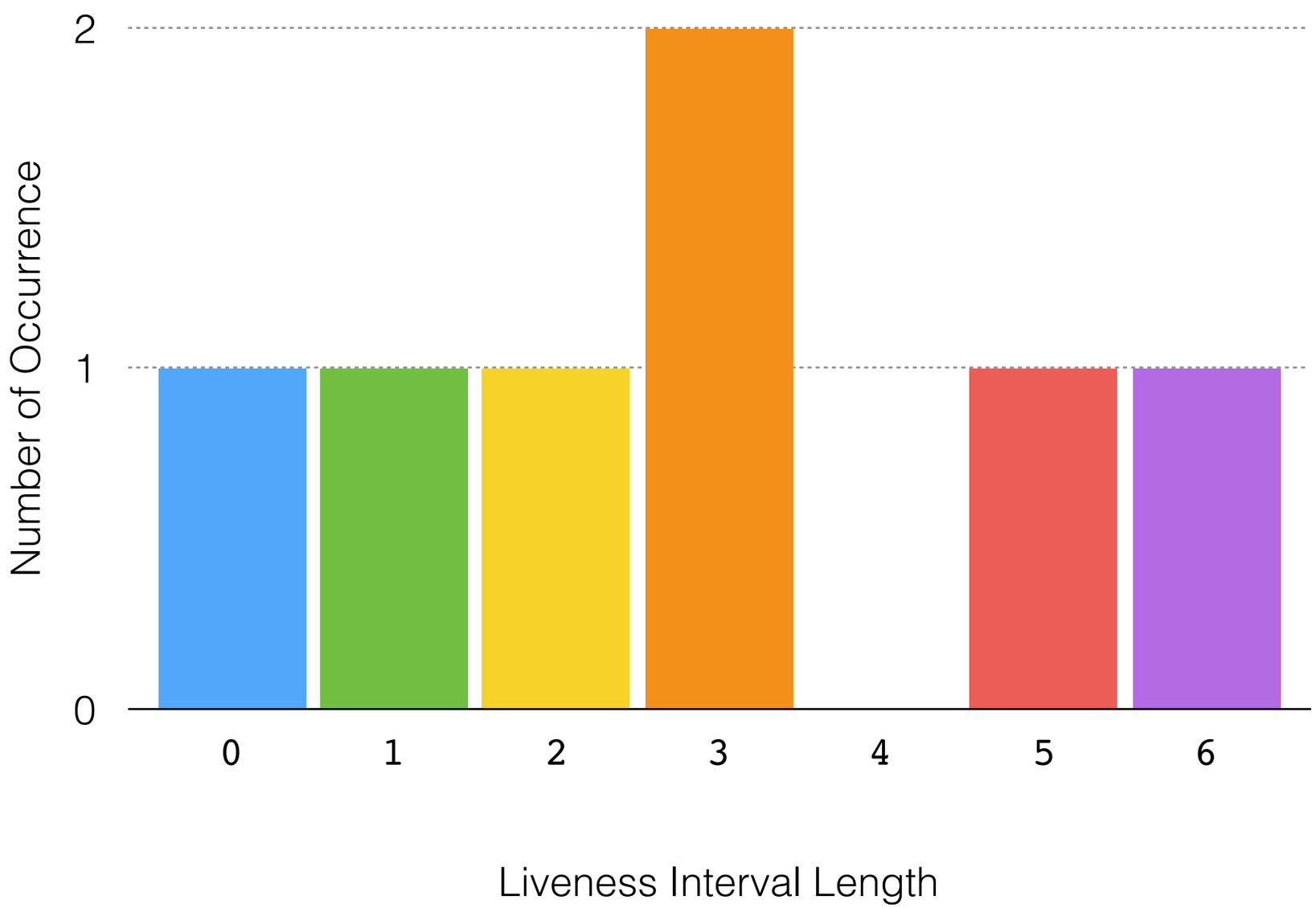
Analysis
Metric: LI Length

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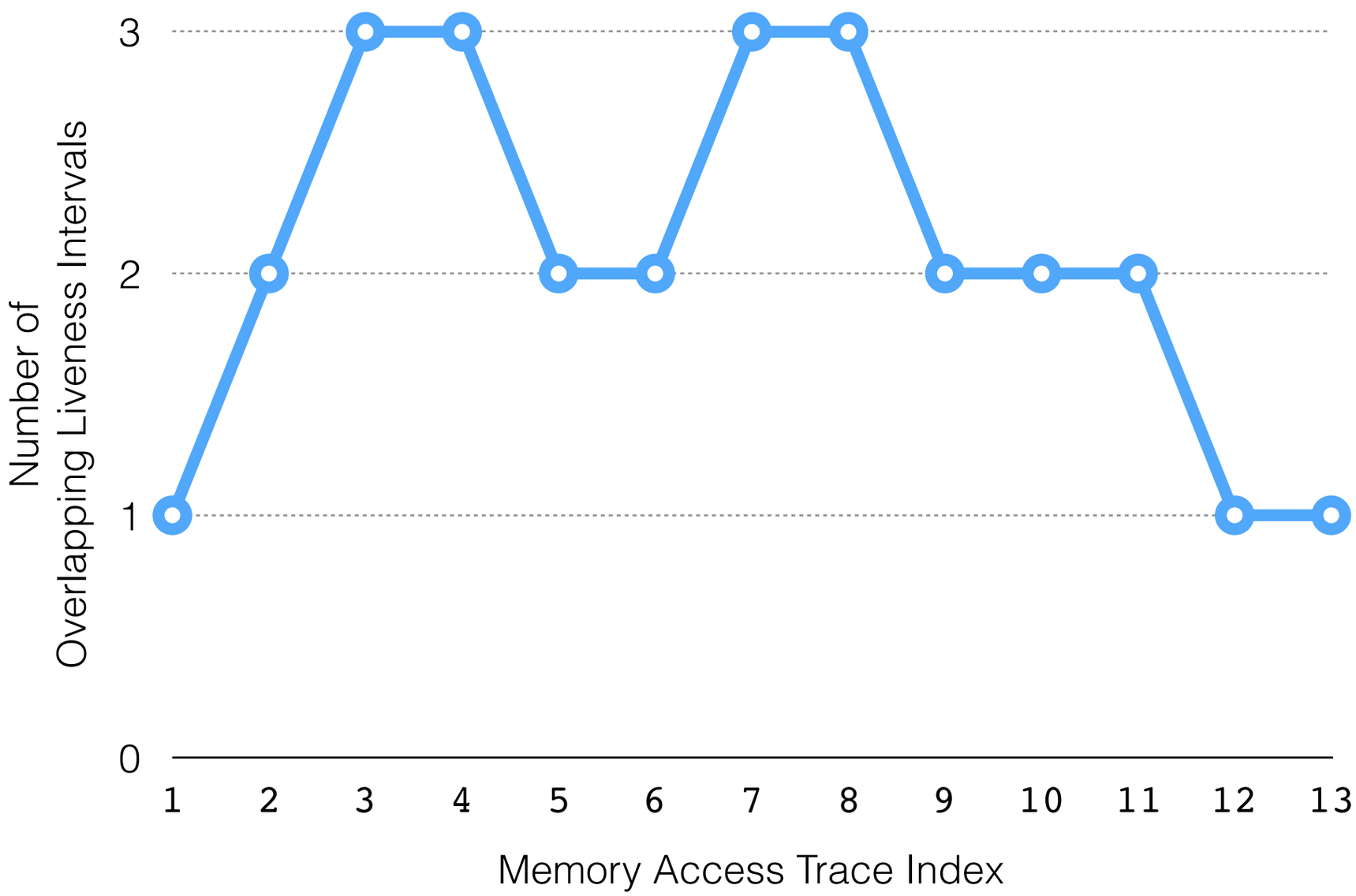
Analysis

Metric: Overlapping LI

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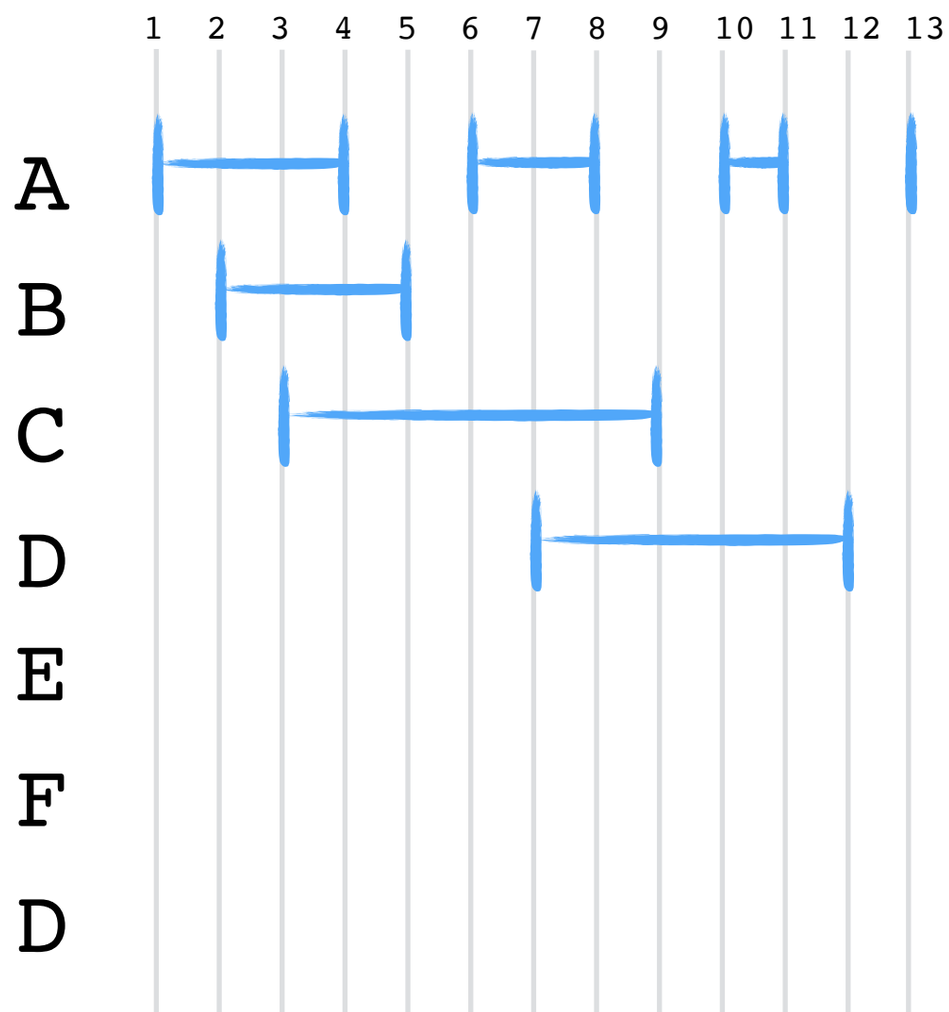
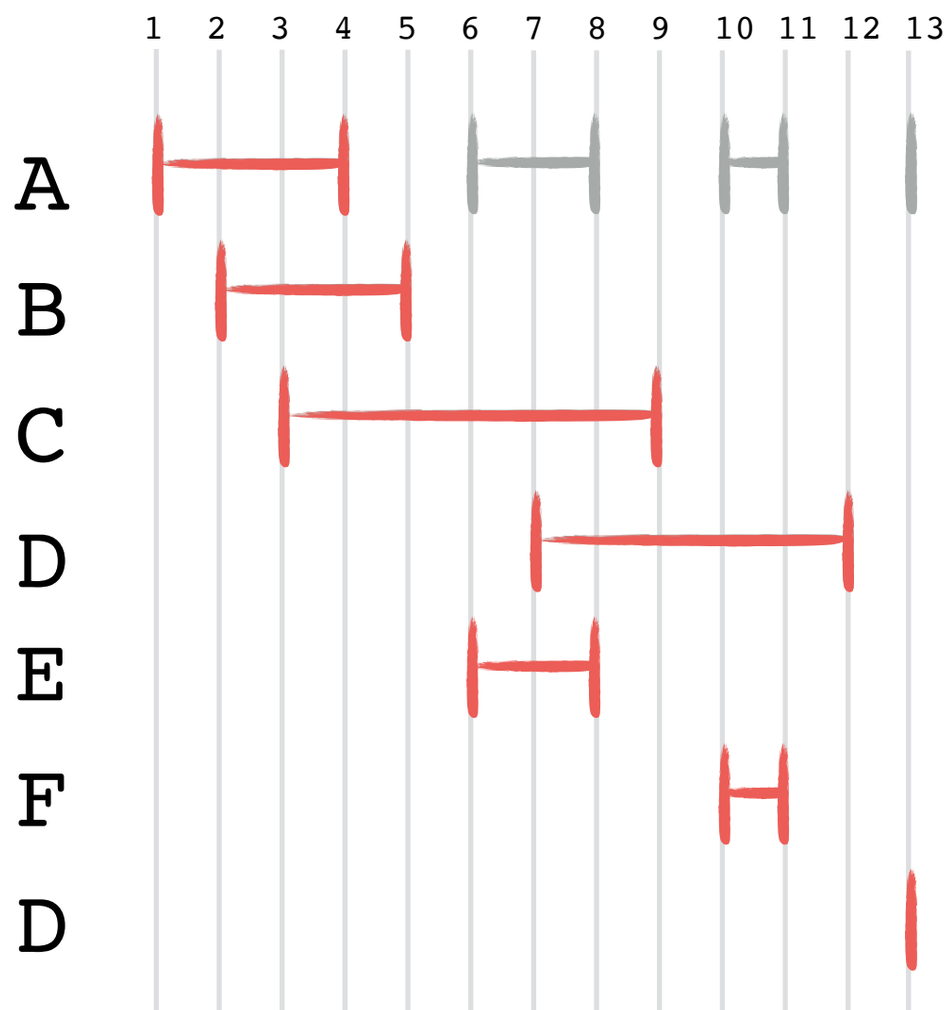
Trace Transformation

Identity



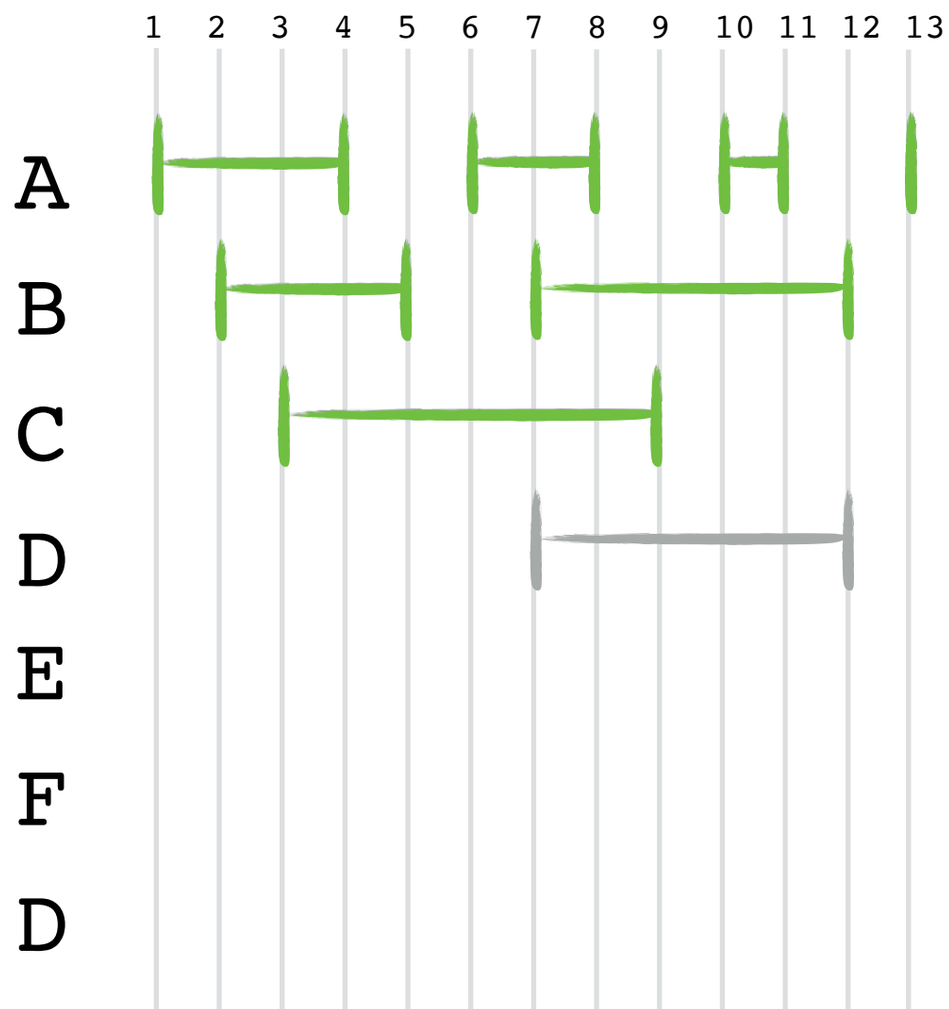
Trace Transformation

Single Assignment

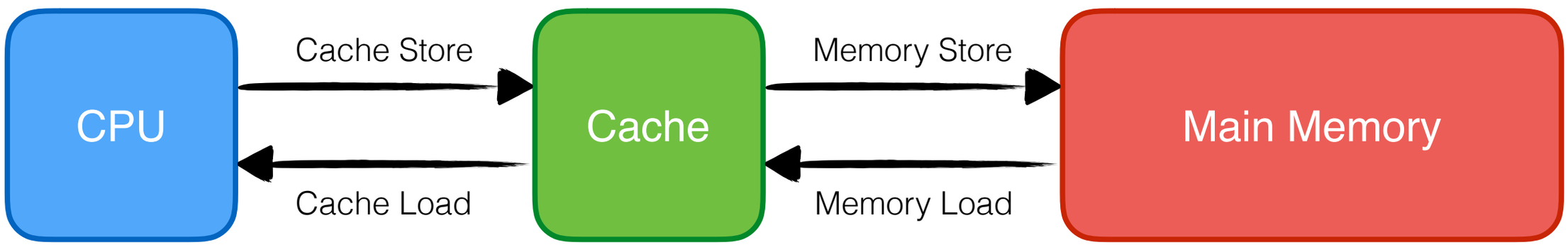


Trace Transformation

Compact



Execution
Hardware Model



Execution
Performance

$$\texttt{CPA(T,C)} = \frac{\texttt{Sum of cycles(T,C)}}{\texttt{Sum of accesses(T)}}$$

Key

Trace … `T`

Cache … `C`

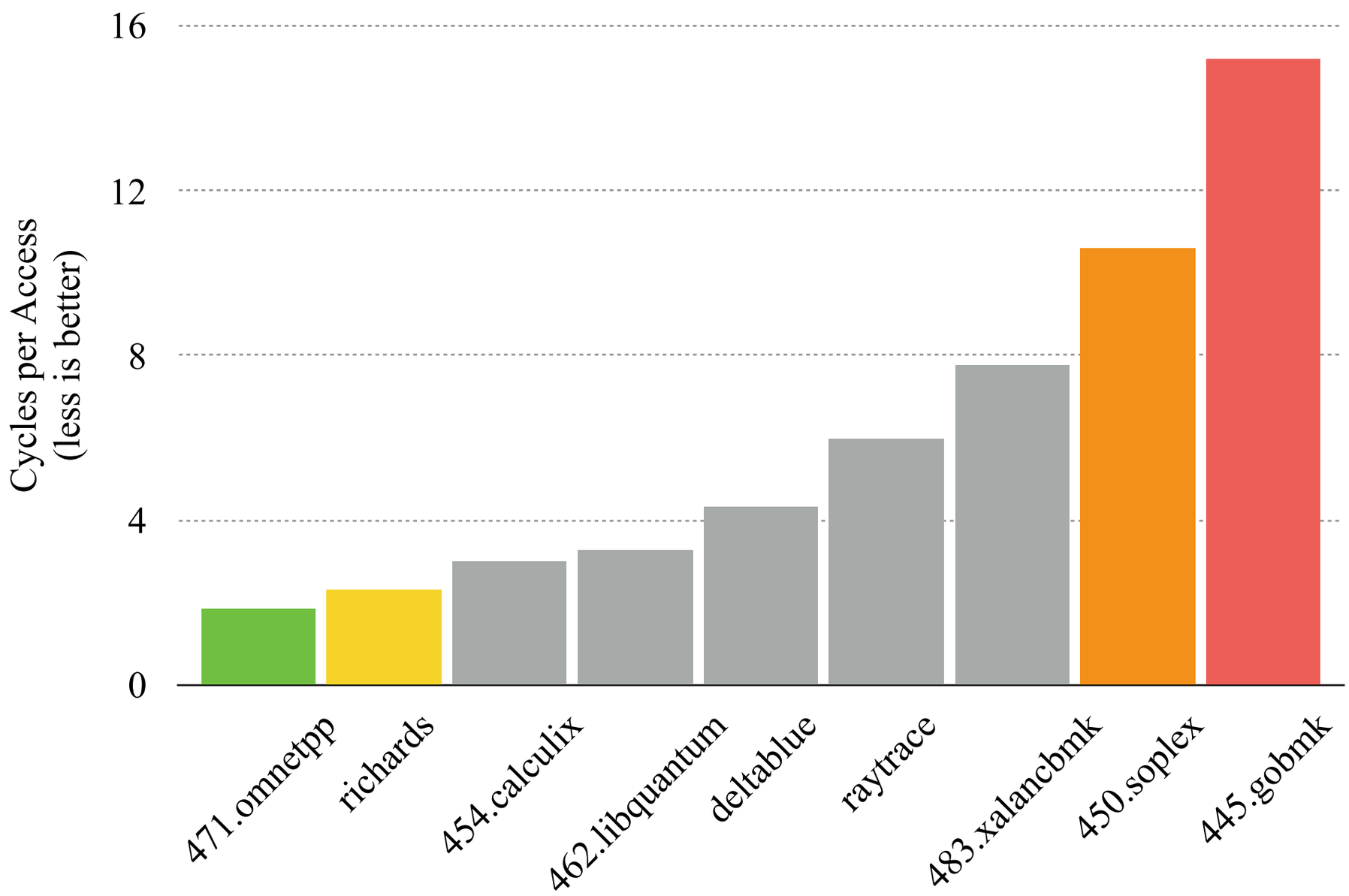
Cycles per Access … `CPA`

Costs in Cycles

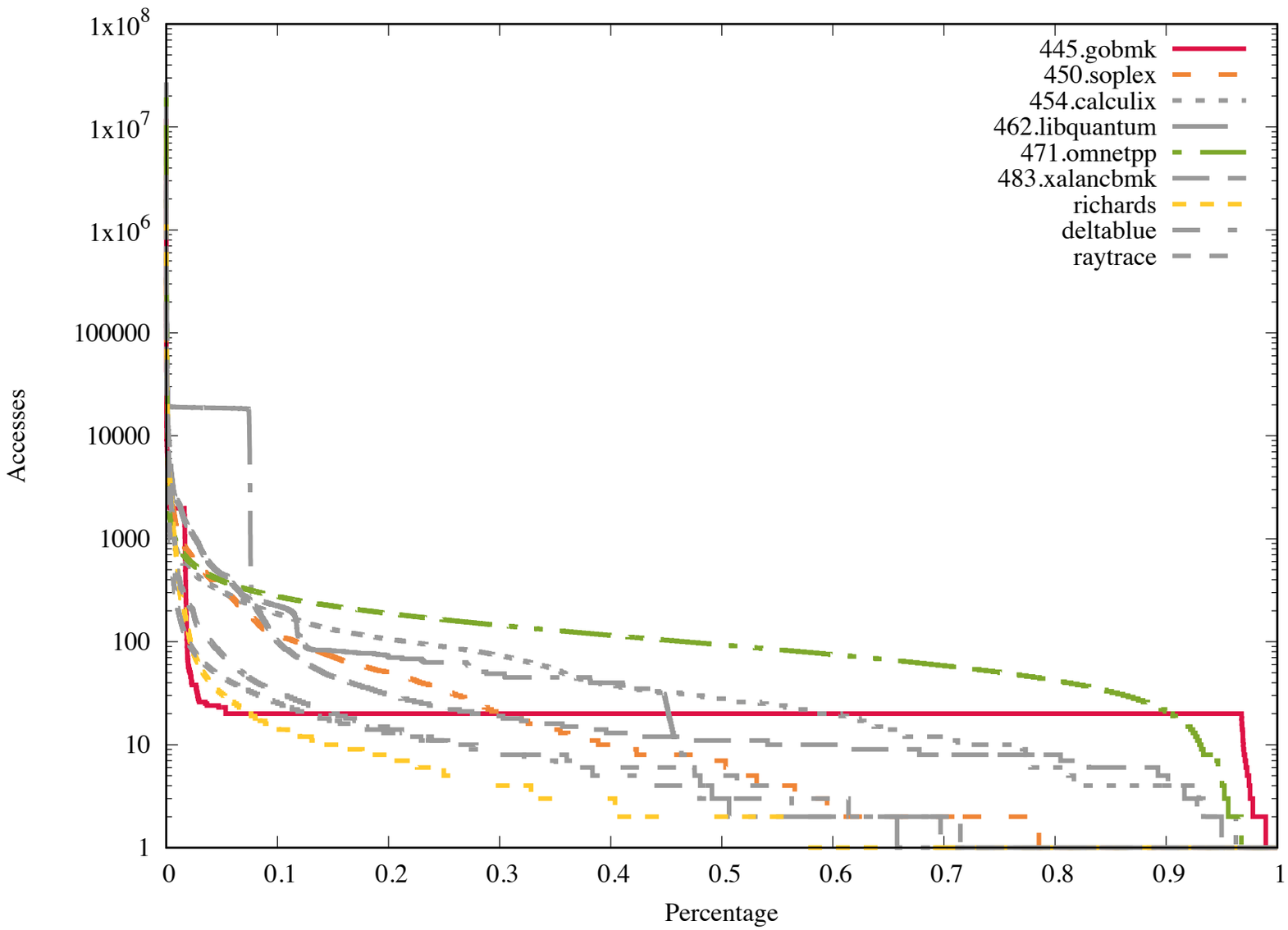
Cache Load / Store: **1**

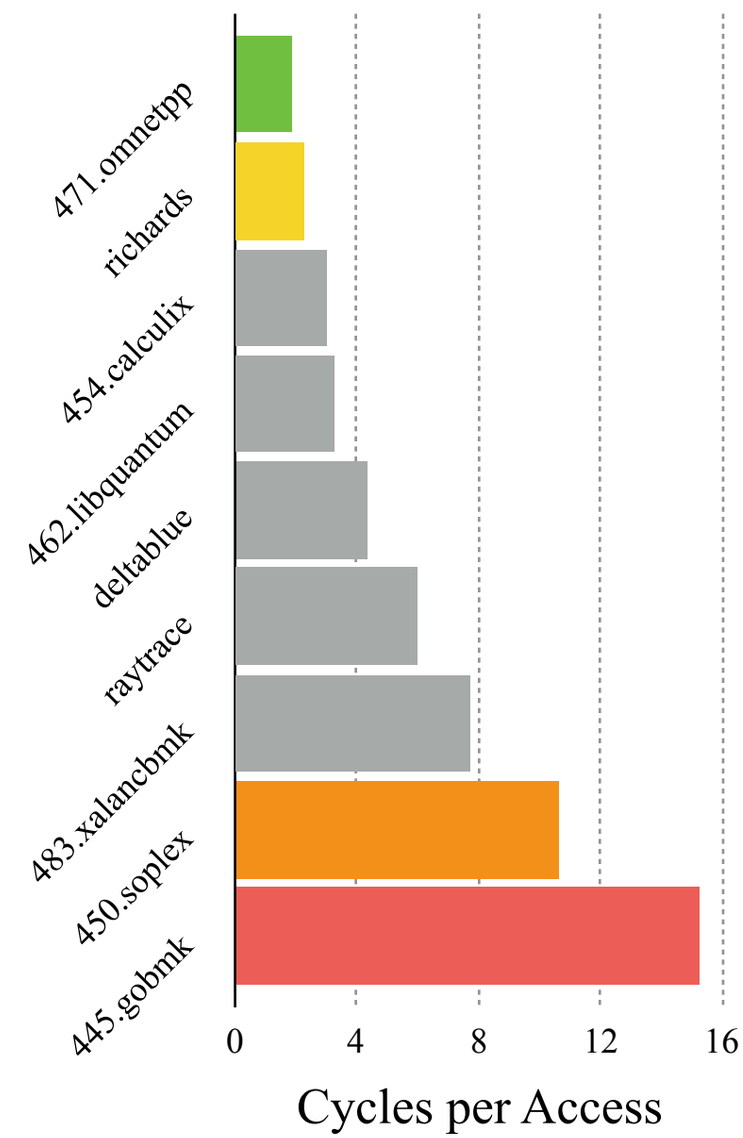
Memory Load / Store: **5**

Experiment
Performance



Experiment
Metric: Accesses





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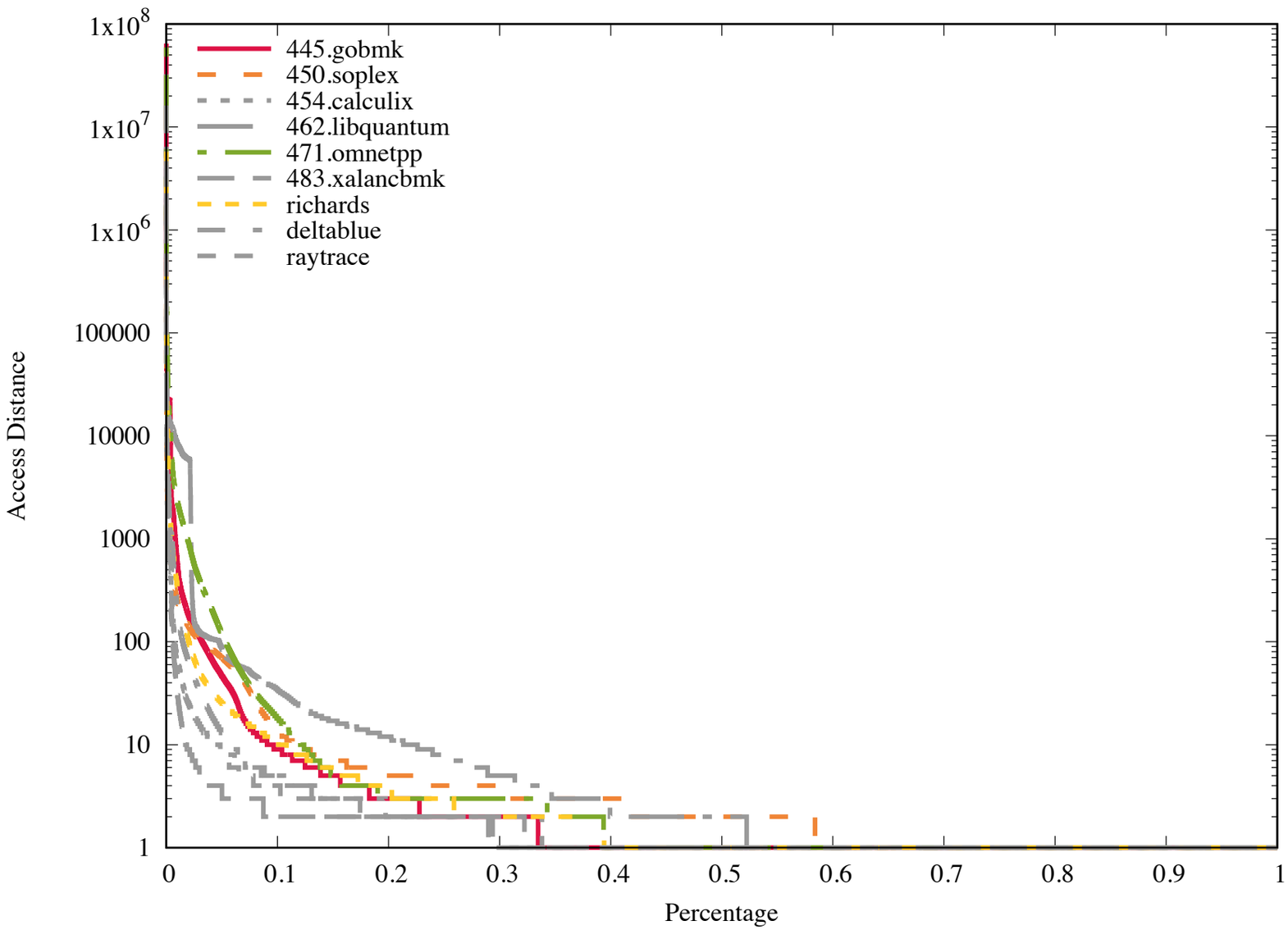
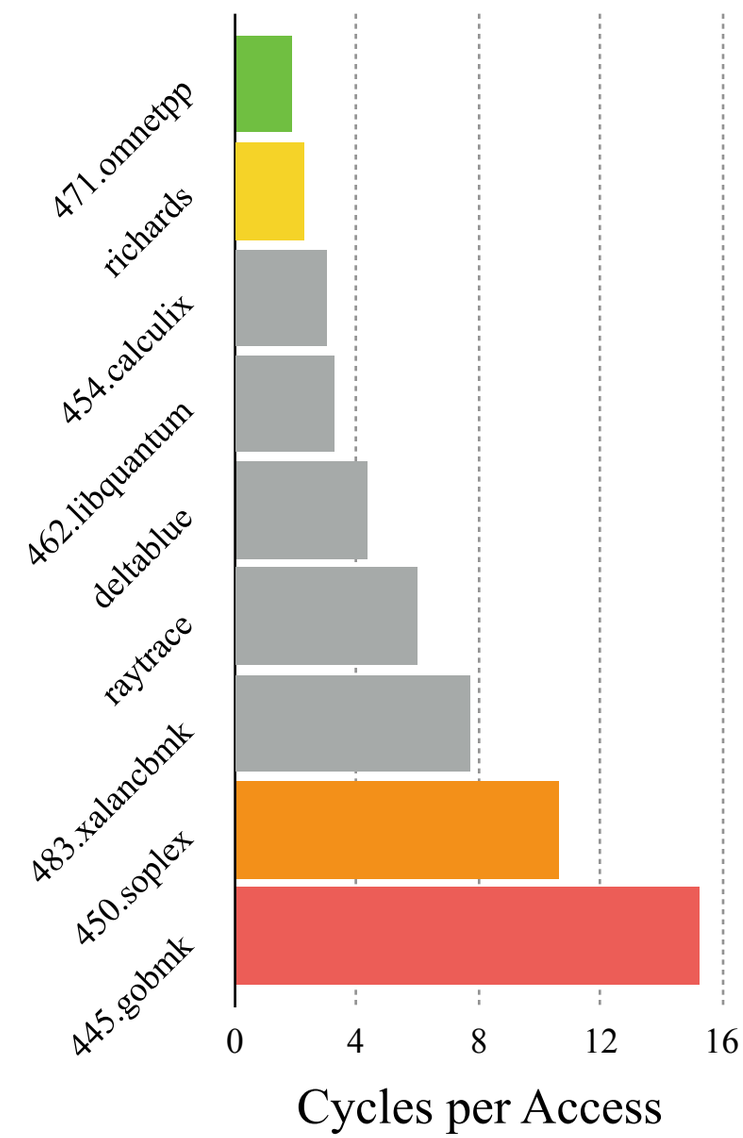
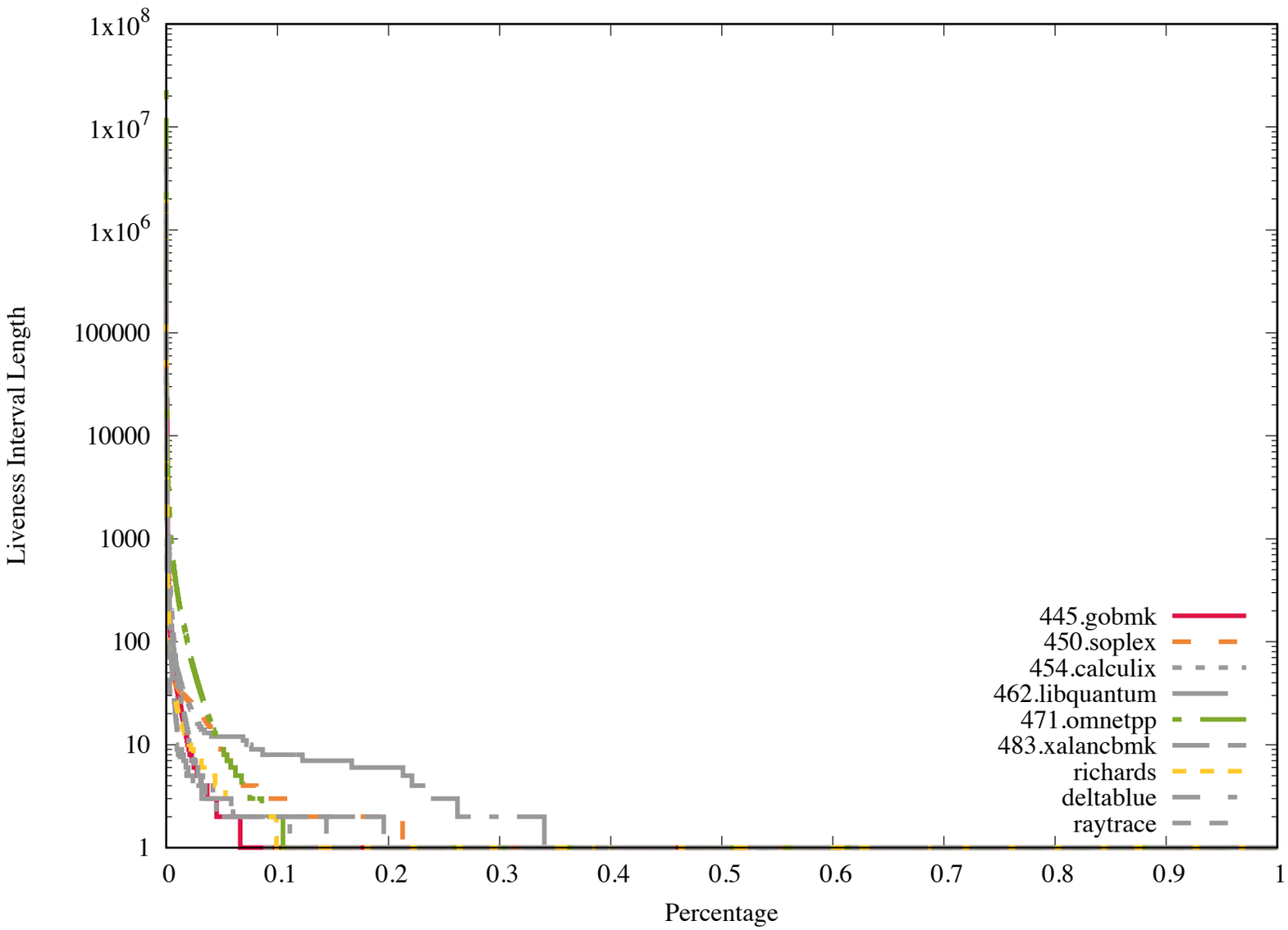
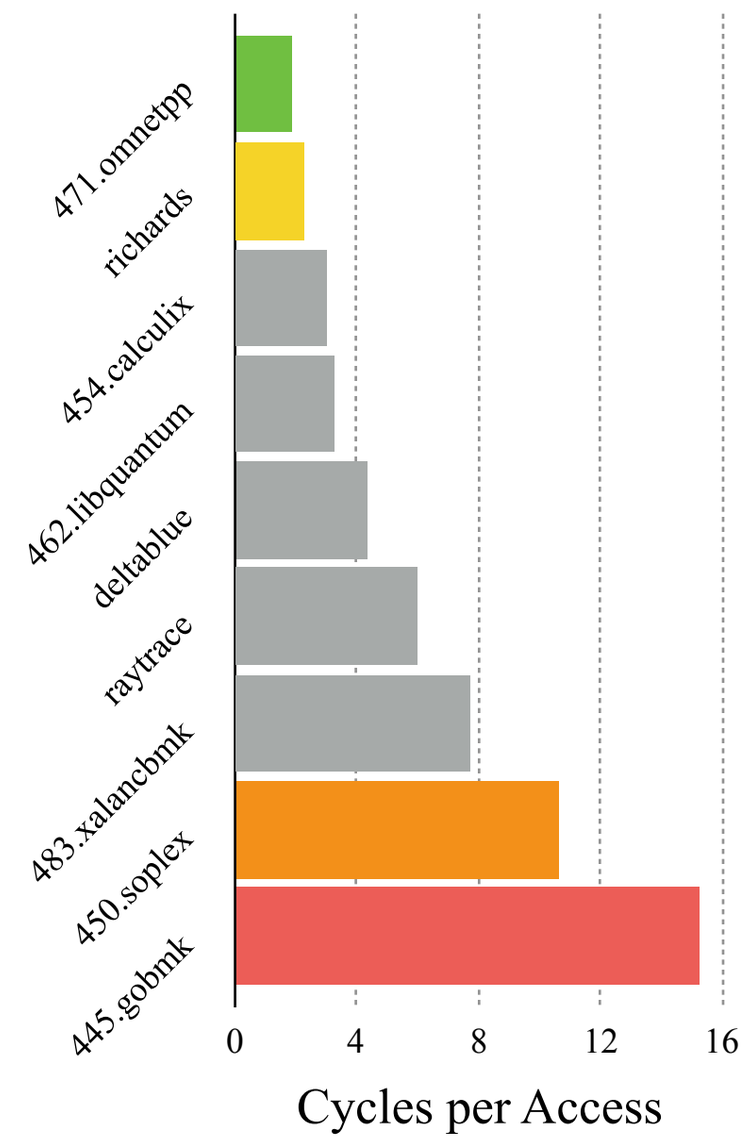




Experiment

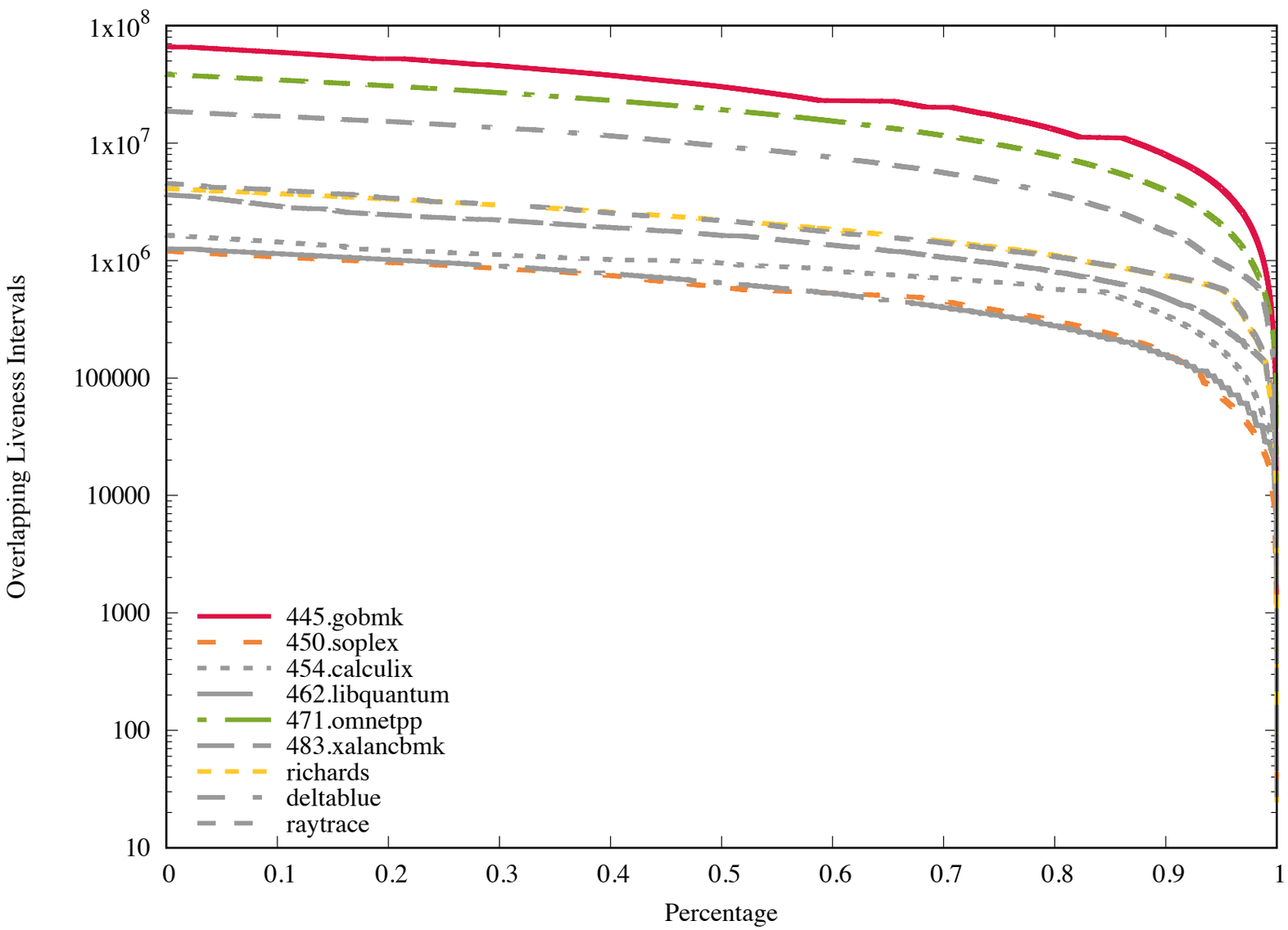
Metric: LI Length

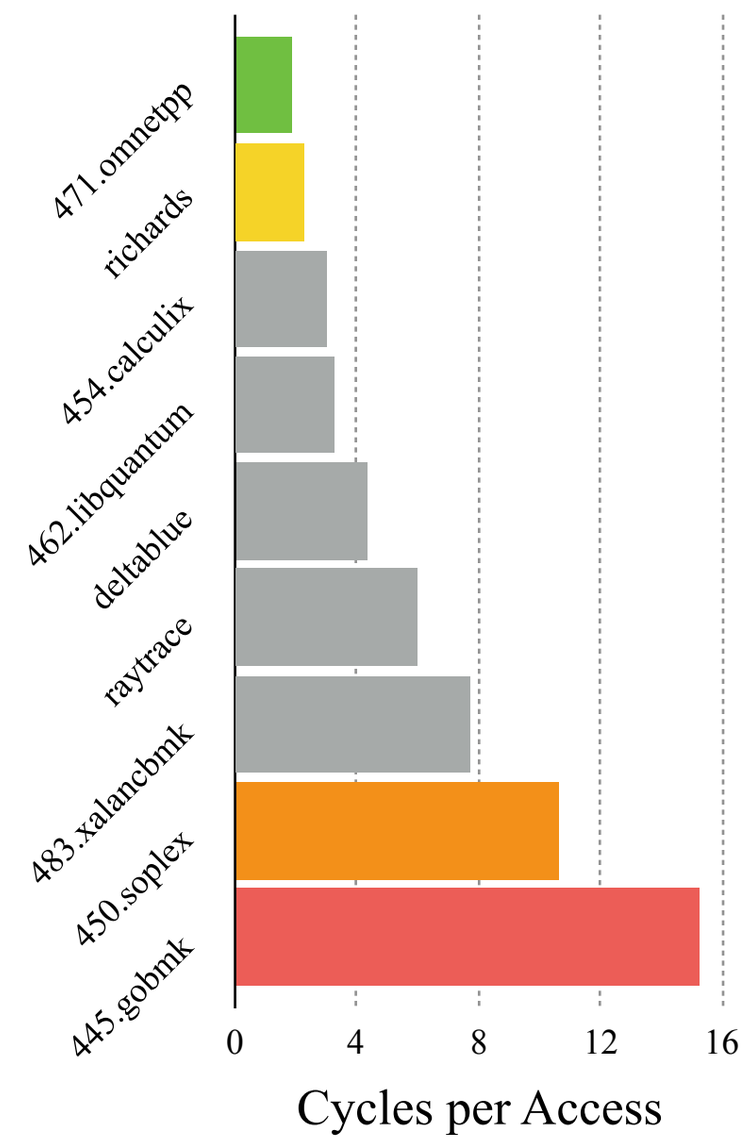




Experiment

Metric: Overlapping LI





Conclusion
Metrics

445.gobmk

- Few accesses on the majority of address
- Nearly constant number of accesses
- Many overlapping liveness intervals

471.omnetpp

- Many accesses per address
- Few addresses with significantly more accesses
- Many overlapping liveness intervals

Conclusion

4 metrics

- accesses
- access distance
- liveness interval length
- overlapping liveness

9 benchmarks from 2 benchmark suits

- SPEC 2006
- V8

The defined metrics illustrate tendencies for improvement rather than unique characteristics.

Thank you.

Q&A