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Power supplies

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USB 2.0 interface, LPC4370 USB, reset, crystal, jtag/swd

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Boot mode, LPC4370 IOs, external spi flash

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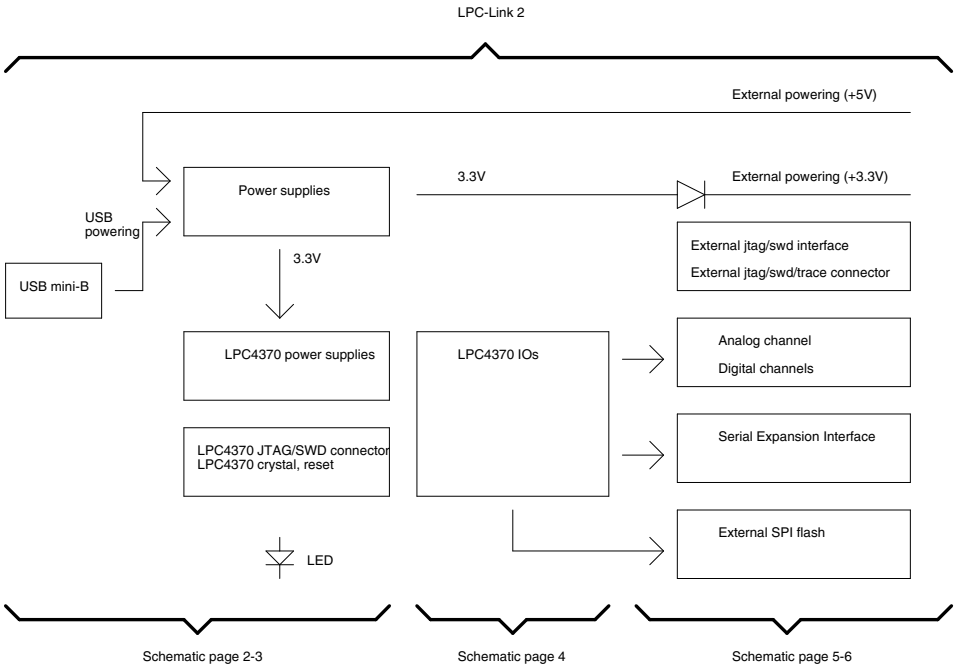
External JTAG/Cortex debug interface

Page 6

Analog channel, digital channels, jtag/swd/trace interface

Design Overview



UL = UnLoaded = normally not mounted component.

Default jumper settings are indicated in the schematic.
However, always check jumper positions on actual boards since there is no guarantee that all jumpers are in default place.

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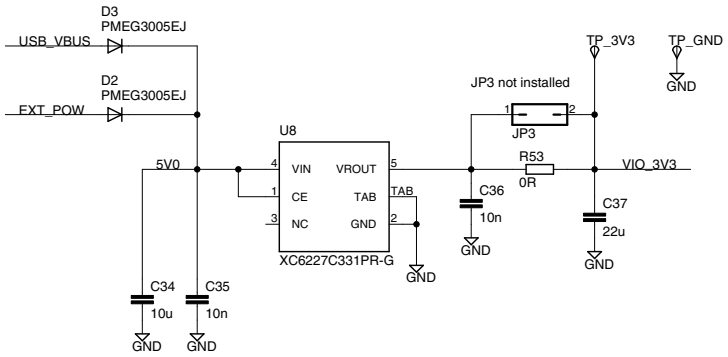
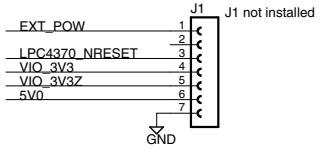
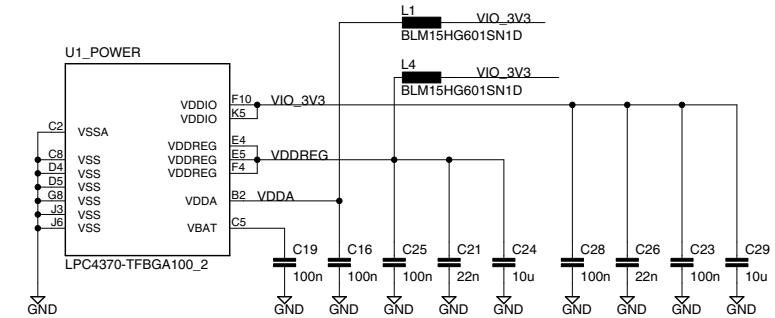
Power supply



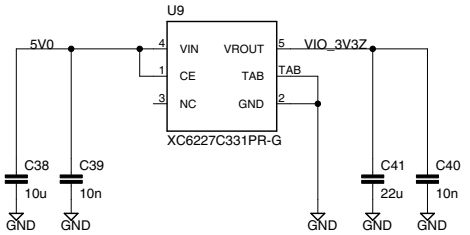
Power Supply Access connector



LPC4370 power supplies



Target Power supply



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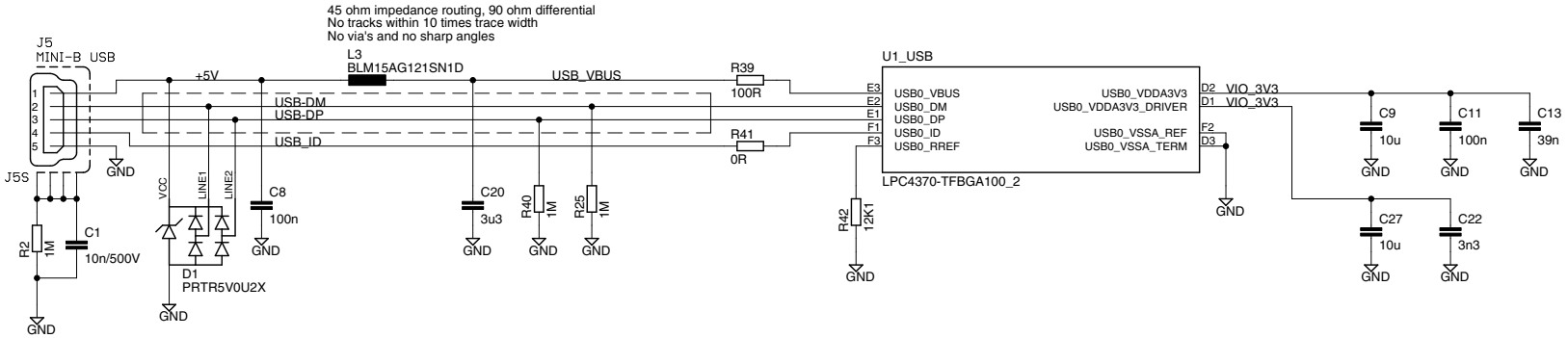
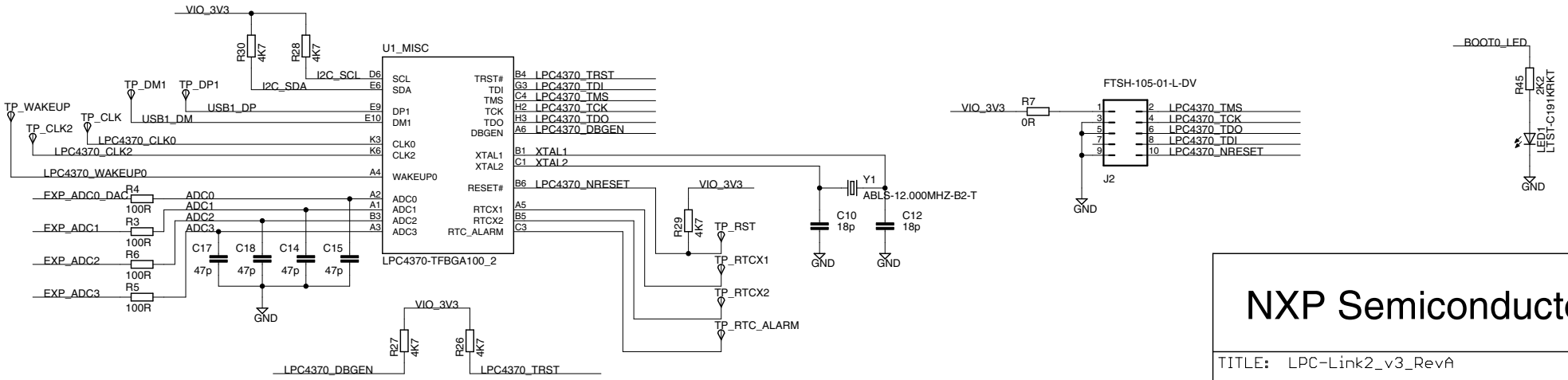
USB 2.0 OTG Interface

LPC4370 USB



LPC4370 reset, crystal, JTAG/SWD

LED



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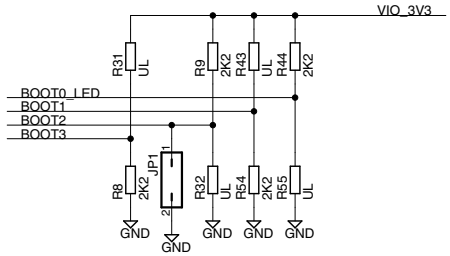
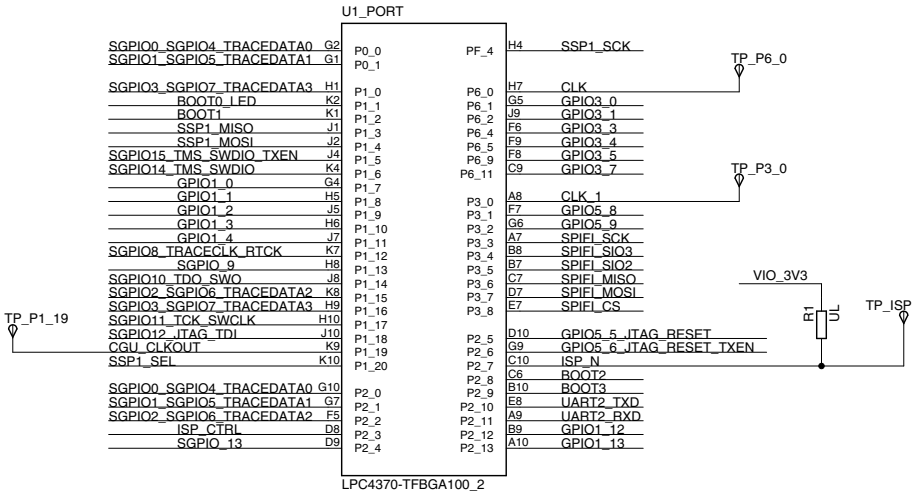
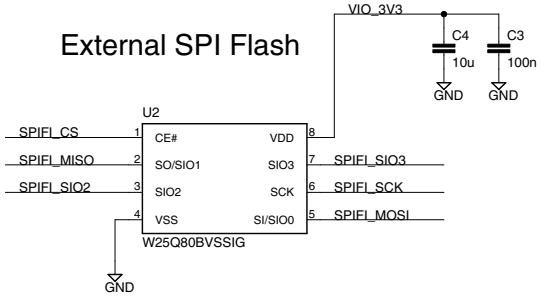
Boot mode - DFU USB0 (0b0101)
- SPIFI (0b0001)



LPC4370 IOs



External SPI Flash



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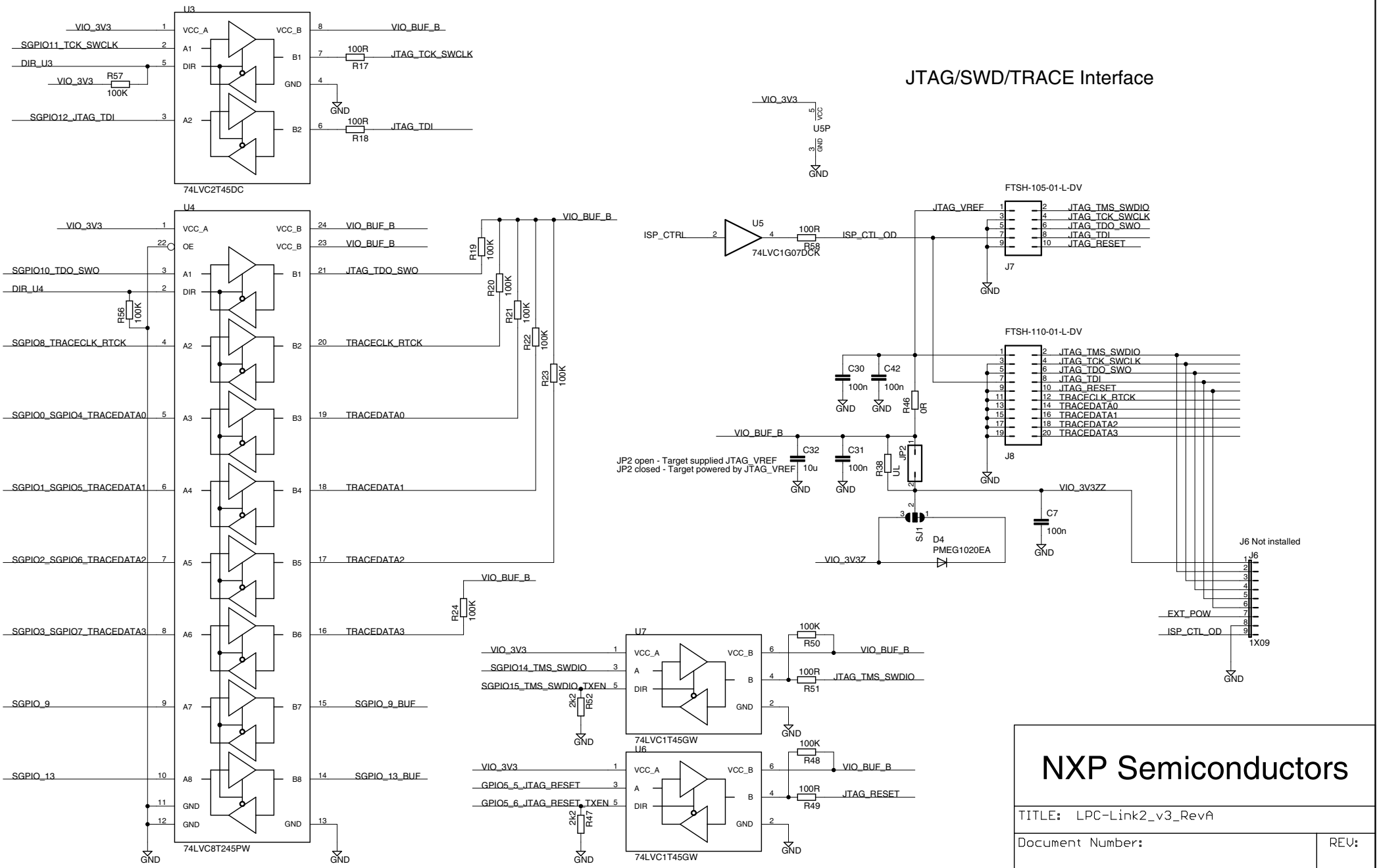
JTAG/SWD/TRACE Interface
U3
74LVC2T45DC
U4
74LVC8T245PW
U5
74LVC1G07DCK
U5P
U6
74LVC1T45GW
U7
74LVC1T45GW
FTSH-105-01-L-DV
J7
FTSH-110-01-L-DV
J8
J6 Not installed
1X09
D4
PMEG1020EA
JP2 open - Target supplied JTAG_VREF
JP2 closed - Target powered by JTAG_VREF
VIO_3V3
VIO_BUF_B
VIO_3V3Z
GND
JTAG_TCK_SWCLK
JTAG_TDI
JTAG_TDO_SWO
JTAG_TMS_SWDIO
JTAG_RESET
TRACECLK_RTCK
TRACEDATA0
TRACEDATA1
TRACEDATA2
TRACEDATA3
SGPIO_9_BUF
SGPIO_13_BUF
ISP_CTRL
ISP_CTL_OD
JTAG_VREF
EXT_POW
SGPIO11_TCK_SWCLK
SGPIO12_JTAG_TDI
SGPIO10_TDO_SWO
SGPIO8_TRACECLK_RTCK
SGPIO0_SGPIO4_TRACEDATA0
SGPIO1_SGPIO5_TRACEDATA1
SGPIO2_SGPIO6_TRACEDATA2
SGPIO3_SGPIO7_TRACEDATA3
SGPIO_9
SGPIO_13
SGPIO14_TMS_SWDIO
SGPIO15_TMS_SWDIO_TXEN
GPIO5_5_JTAG_RESET
GPIO5_6_JTAG_RESET_TXEN
DIR_U3
DIR_U4
R17 100R
R18 100R
R19 100K
R20 100K
R21 100K
R22 100K
R23 100K
R24 100K
R46 0R
R47 2k2
R48 100K
R49 100R
R50 100K
R51 100R
R52 2k2
R56 100K
R57 100K
R58 100R
C7 100n
C30 100n
C31 100n
C32 10u
C42 100n
JP2
SJ1
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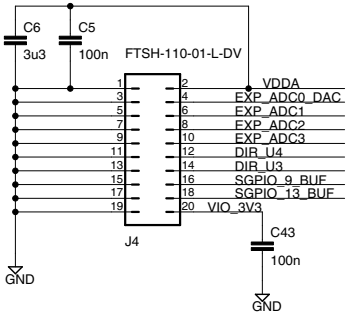
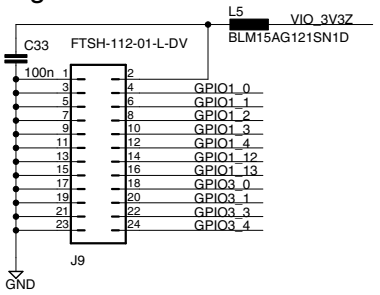
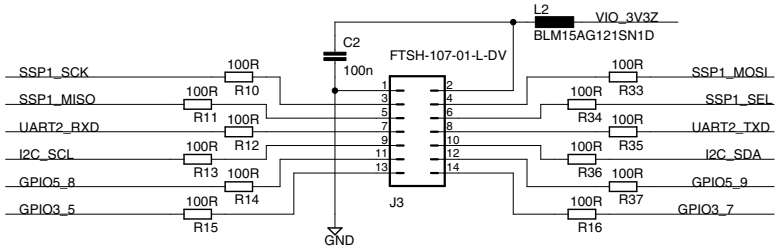
Analog + Digital channels



Digital channels



Serial Expansion Interface



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