Ming Qian Tang

217 766 5671 | mingqiantang@gmail.com

EDUCATION

University of Illinois, Urbana-Champaign   Expected Graduation: May 2026
Bachelor of Science in Computer Engineering   *GPA: 3.47*

Related Coursework:
Computer Organization and Design(CPU Architecture), Computer Systems Engineering(Operating Systems)

EXPERIENCE

University of Illinois, Urbana-Champaign   Jan 2025 – Present
Undergraduate Assistant, Computer Systems Laboratory — FPGA, SystemVerilog, AMD/Xilinx Vivado
- Resolved 300+ questions from undergraduate students during office hours, clarifying complex course material and debugging technical challenges related to FPGA and SystemVerilog.
- Mentored more than 10 student groups in hands-on projects, providing direct support for design, simulation, and implementation of complex FPGA projects.

Seiko Precision   Jun 2024 – Aug 2024
Engineering Intern
- Automated production workflows by programming and integrating robotic arms, increasing operational efficiency by 75% by reducing manual intervention.
- Collaborated with 3 teams from engineering, maintenance, and management to identify bottlenecks and resolve technical issues at the production line.

PROJECTS

OoO RISC-V Processor — *SystemVerilog, RISC-V, VCS, Verdi, Python Scripting*   Oct 2025 – Present
- Architected a 2-way superscalar Out of Order (OoO) 32-bit RISC-V (RV32IM) processor in SystemVerilog targeting an 1.4+ IPC on core benchmarks.
- Designed a gshare (GHR/PHT) branch predictor targeting over 90% hit accuracy and implemented Early Branch Recovery (EBR) logic, targeting a 40% reduction in the misprediction penalty.
- Validated the design using a self-checking testbench with a Python-based random instruction generator, wrote 8+ automatic SystemVerilog testbenches using assertions with Verdi waveform analysis to debug complex hazards.

RISC-V OS Kernel — *C, GDB, RISC-V, UART, Virtual Memory, File System*   Jan 2025 – May 2025
- Built a preemptive multitasking kernel entirely in C, implementing a 100ms time slice round-robin scheduler to manage up to 16 concurrent processes.
- Implemented a complete virtual memory system using 3-level Sv39 paging, providing a 500MB virtual address space per process and managing memory in 2048B pages.
- Developed an interactive shell supporting 4 commands and inter-process piping, enabling complex operations like 2 simultaneous program execution.

FPGA Rhythm Game — *SystemVerilog, AMD/Xilinx Vivado, SPI, USB, DDR, VGA*   Sep 2024 – Dec 2024
- Archtected a fully functional rhythm game from the ground up, architecting 12 custom RTL modules in SystemVerilog using a Spartan-7 FPGA.
- Designed a VGA controller with a 460KB frame buffer to render real-time 640x480 graphics at 60Hz and integrated custom SPI and USB modules to interface with 1 game controller or peripherals.
- Implemented a dedicated audio module to parse and play back 44.1kHz, 8-bit unsigned stereo .wav files from SD card using DDR3 memory as a buffer.

TECHNICAL SKILLS

Skills: SystemVerilog, C, C++, Embedded Firmware, Verdi, RISC-V, PCB Design, HDL Verification, Arduino, Assembly Language, Python
Tools: AMD/Xilinx Vivado, GDB, VCS, Verdi, KiCAD, Fusion 360
Technologies: UART, VGA, Double Data Rate (DDR), Serial Peripheral Interface(SPI), Universal Serial Bus (USB)