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B.Tech (CSE)

VHDL

Lab 6

Q] Write program to implement 4:1 MUX

Ans]
```
library IEEE;
use IEEE.std_logic_1164.all;

entity mux_4to1 is
    port (A,B,C,D: in std_logic;
          S0,S1: in std_logic;
          z: out std_logic);
end mux_4to1;

architecture bhv of mux_4to1 is
begin
process (A,B,C,D,S0,S1) is
begin
    if (S0='0' and S1='0') then
        z<=A;
    elsif (S0='1' and S1='0') then
        z<=B;
    elsif (S0='0' and S1='1') then
        z<=C;
    else
        z<=D;
    end if;
end process;
end bhv;
```