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BTech CSE 5th Sem

VHDL

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Q. Write a program to implement 4:1 MUX

Ans

```
library IEEE;
use IEEE.std_logic_1164.all;

entity mux_4to1 is
    port ( A,B,C,D : in std_logic;
           S0,S1 : in std_logic;
           Z : out std_logic;);
end mux_4to1;

architecture bhv of mux_4to1 is
begin
proress (A,B,C,D,S0,S1) is
begin
    if (S0='0' and S1='0') then
        Z<=A;
    elseif (S0='1' and S1='0') then
        Z <= B;
    elseif (S0='0' and S1='1') then
        Z <= C;
    else
        Z <= D;
    end if;

end proress;
end bhv;
```