Roman Yadav [0301640321 9]
B. Tech [CSE] IV
VHDL
Lab - 5

Q] Write a VHDL program to design 7-segment display decoder circuit.

Ans]
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL

entity BCDdecoder is
    port ( x: in std_logic_vector (3 down to 0);
           y: out std_logic_vector (6 down to 0));
end BCDdecoder;

architecture behave of BCDdecoder is
signal temp: std_logic_vector (15 downto 0);

begin
    temp <= "0000000001111111" when (x = "0000")
    else "0000000000000110" when (x = "0001")
    else "0000000001011011" when (x = "0010")
    else "0000000001001111" when (x = "0011")
    else "0000000001100110" when x = "0100"
    else "0000000001101101" when (x = "0101")
    else "0000000001111101" when (x = "0110")
    else "0000000000000111" when x = "0111"
    else "0000000001111111" when (x = "1000")
    else "0000000001100111" when (x = "1001")
        (others => z);
    y <= temp (6 down to 0) and
        temp (15 down to 7) <= '0';
end Behave;
```