HIMESH NAYAK
0121640321 9
BTech CSE 5th Sem

VHDL

Page No:
Date: / /

LAB : 3

Q- Write a VHDL program to design 4-bit adder using a macro of half adder and full adder.

Ans-

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity ha is
  Port ( x: in std_logic;
         y: in std_logic;
         s: out std_logic;
         c: out std_logic; );
end ha;
architecture Behavioral of ha is
begin
      S <= x xor y;
      c <= x and y;
end Behavioral;

entity fa_comp is
   Port ( a: in std_logic;
          b: in std_logic;
          cin: in std_logic;
          sum: out std_logic;
          carry: out std_logic; );
end fa_comp;
architecture Behavioral of fa_comp is
        component ha is
   Port ( x: in std_logic;
          y: in std_logic;
          s: out std_logic;
          c: out std_logic; );
```

```
        end component;
        signal temp1, temp2, temp3 : std_logic;
begin
        ha1 : ha port map ( x => a, y => b, s => temp1,
                            c => temp2);
        ha2 : ha port map ( x => temp1, y => cin, s => sum,
                            c => temp3 );
              carry <= temp2 or temp3;
end Behavioral;

entity adder4bit is
    Port ( a : in std_logic_vector (3 downto 0);
           b : in std_logic_vector (3 downto 0);
           carryin : in std_logic;
           sum : out std_logic_vector (3 downto 0);
           carryout : out std_logic);
end adder4bit;
architecture Behavioral of adder4bit is
        component fa_comp is
    Port (a : in std_logic;
           b : in std_logic;
           cin : in std_logic;
           sum : out std_logic;
           carry : out std_logic; );
    end component fa_comp;
signal temp : std_logic_vector (2 downto 0);
begin
u1 : fa_comp port map (a => a(0), b => b(0),
        cin => carryin , sum => sum(0), carry => temp(0));
u2 : fa_comp port map (a => a(1), b => b(1),
        cin => temp (0), sum => sum (1), carry => temp(1));
u3 : fa_comp port map (a => a(2), b => b(2),
```

```
        cin => temp(1), sum => sum(2), carry => temp(2));
u4 : fa_comp port map (a => a(3), b => b(3),
        cin => temp(2), sum => sum(3), carry => carryout);
end Behavioral;
```