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BTech CSE 5th Sem

VHDL

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LAB 4

Q. Write a VHDL program to design BCD adder.

Ans.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity BCDadder is
    Port ( bcd1 : in std_logic_vector (3 downto 0);
           bcd2 : in std_logic_vector (3 downto 0);
           bcd carry in : in std_logic;
           bcdsum : out std_logic_vector (3 downto 0);
           bcd carryout : out std_logic);
end BCDadder;
architecture Behavioral of BCDadder is
        component adder_4Bit is
    Port ( a : in std_logic_vector (3 downto 0);
           b : in std_logic_vector (3 downto 0);
           carry in : in std_logic;
           sum : out std_logic_vector (3 downto 0);
           carryout : out std_logic );
    end component adder4bit;
    signal s, x : std_logic_vector (3 downto 0);
    signal c, k : std_logic;
begin
    u1 : adder4bit port map (a(3) => bcd1(3),

        cin => temp(1), sum => sum(2), carry => temp(2));
u4 : fa_comp port map (a => a(3), b => b(3),
    cin => temp(2), sum => sum(3), carry => carryout);
end Behavioral;
```

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a(2) => bcd1(2), a(1) => bcd1(1),
a(0) => bcd1(0), b(3) => bcd2(3),
b(2) => bcd2(2), b(1) => bcd2(1),
b(0) => bcd2(0), carryin => bcdcarryin,
sum(3) => s(3), sum(2) => s(2), sum(1) => s(1),
sum(0) => s(0), carryout => c);
   k <= (s(3) and s(2)) or (s(3) and s(1)) or(c);
   x <= "0110" when k = '1' else "0000";

u2 : adder4bit port map(a(3) => s(3),
   a(2) => s(2), a(1) => s(1), a(0) => s(0),
   b(3) => x(3), b(2) => x(2), b(1) => x(1),
   b(0) => x(0), carryin => '0', sum(3) => bcdsum(3),
   sum(2) => bcdsum(2), sum(1) => bcdsum(1),
   sum(0) => bcdsum(0), carryout => bcdcarryout);
end Behavioral;
```