VHDL LAB ASSIGNMENT 1

Submitted to- Prof. Amit Prakash Singh

Submitted by- Rohan Yadav

03016403219

B. Tech [CSE]

Q1. Explain Synthesizer, Simulation and Compiler and also write few names of synthesizer.

Soln.

1)Synthesizer - The synthesizer does what the code tells it to do. If the designer uses the expression (a + b) three

different places in the code, the synthesizer will allocate three adders when mapping the logic. The designer

can help the synthesizer map logic with the use of variables

- 2)Simulation: A simulation is the imitation of the operation of a real-world process or system over time. Simulations require the use of models; the model represents the key characteristics or behaviours of the selected system or process, whereas the simulation represents the evolution of the model over time.
- 3)Compiler -: A compiler is a special program that processes statements written in a particular programming language and turns them into machine language or "code" that a computer's processor uses.

4) Name of some synthesizer: - Moog Minimoog.

EMS VCS3.

Sequential Circuits Prophet-5.

PPG Wave 2.2/3.