EC 305 MICROPROCESSOR & MICROCONTROLLER

SOUMYA S
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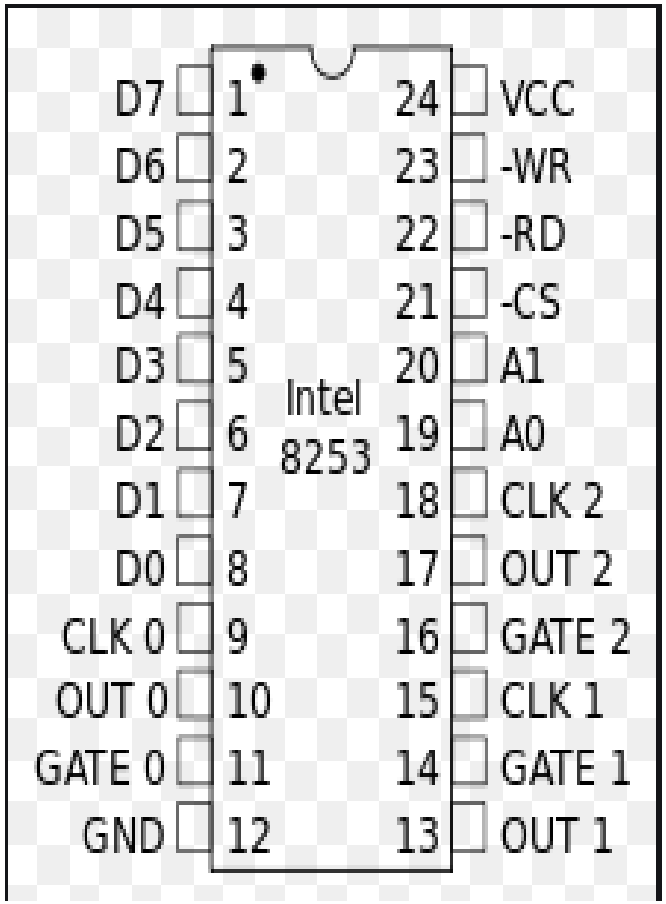
CEMP

8253 / 8254 PROGRAMMABLE INTERVAL TIMER

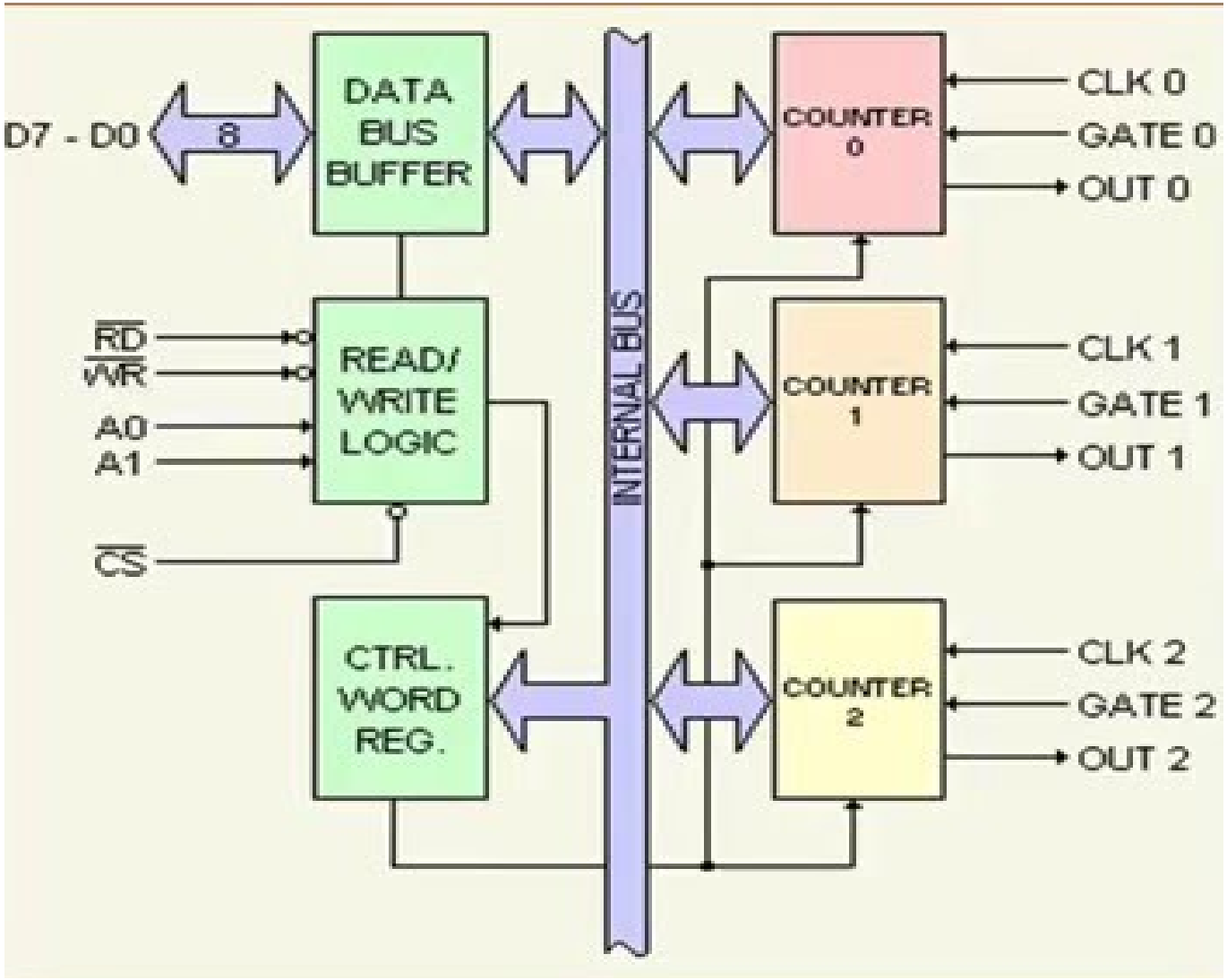
- Specially designed chip for microprocessors to perform timing and counting operations.
- Timing and counting operations are implemented through S/W.
- **Features of 8253**
- 8253 / 8254 consists of three independent 16-bit down counters.TM0,TM1,TM2
- Down counters.(100,99,98……0).
- Each timer can be programmed by the operator in any one of the 6 modes.
- The function of each timer is independent of the mode of operation of the other 2 timers.

- Timers are software programmable.
- 8253 can operate with max 2MHz.
- 8254 can operate with max 10 MHz .
- It is compatible with almost all microprocessors.
- 8254 incudes a status **Read Back Command** which allows the user to check the count value ,the programmed mode , the current mode and current status of the timer.

PIN CONFIGURATION 8254



BLOCK DIAGRAM



- **DATA BUS BUFFER**
- Bidirectional 8 bit buffer is connected to the data bus of µp.
- **READ/WRITE LOGIC**
- Read/write logic has 5 pins.
  - $\overline{RD}$: read signal
  - $\overline{WR}$: write signal
  - $\overline{CS}$: chip select signal
  - A0, A1: address lines

CS	A1	A0	SELECETION
0	0	0	C0
0	0	1	C1
0	1	0	C2
0	1	1	Control Register

- **CONTROL WORD REGISTER**
- This register is accessed when lines A0 and A1 are at logic1.It is used to write a command word which specifies the counter to be used ,its mode , and either a Read or a Write operation.
- **COUNTERS:**
- 3- 16 bit counters
- CLK,GATE,OUT
- GATE:- initiate or enable counting .
- OUT:-provides output from the timer.

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

7.7.1 Operating Modes

The counters are fully independent and each can have separate mode configurations and counting operations, binary or BCD. Following are the different modes possible in the 8253/8254.

Mode 0—interrupt on terminal count

This mode is typically used for event counting. The GATE input is used to enable or disable the counting. When the GATE input is high, the counting is enabled and when it is low the counting is disabled. After the count is loaded into the selected count registers, the OUT remains low and the counter starts counting one cycle after the counter is loaded. On reaching the terminal count (i.e. zero), OUT will go high and remain high until the count register is reloaded or the control word is written. The OUT point can be connected to any interrupt request pin of the microprocessor.

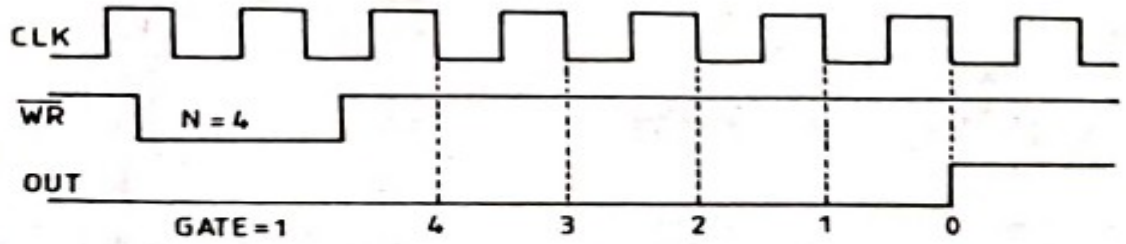
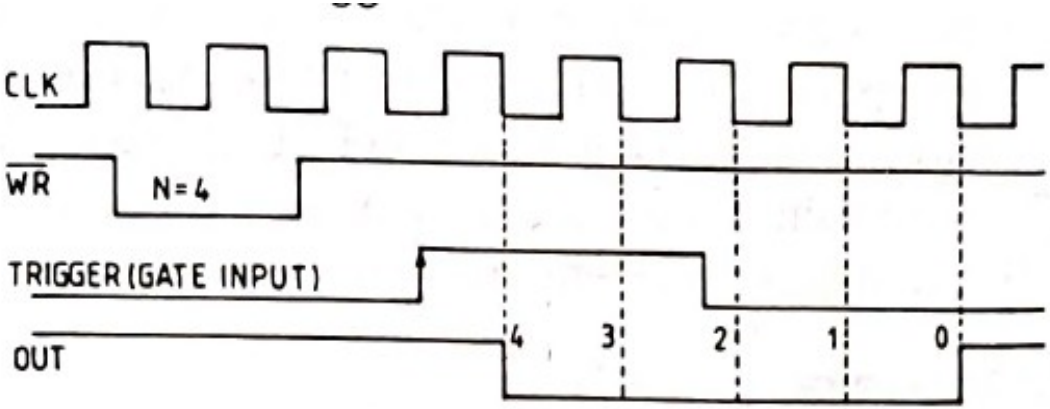


Fig. 7.30. MODE 0, Interrupt on Terminal Count.

Mode 1—programmable one-shot

The GATE input is used to trigger the OUT. The OUT will be initially high and go low on the count following the rising edge at the GATE. When the terminal count is reached, the OUT goes high and remains high until the CLK pulse after the next trigger. Thus, the duration of one-shot pulse at OUT can be programmed through the count.



Mode 2—rate Generator

The counter in this mode acts as divide-by-N counter. It is used to generate a real-time clock interrupt. The OUT will initially be high. When the count has decremented to 1, the OUT goes low for one clock pulse. The OUT then goes high again, the counter reloads the initial count and the process is repeated. The GATE input, when low, disables the counting. When the GATE input goes high, the counter starts from the initial count. The OUT gives one pulse after every N clock pulses, thus achieving the rate generator function.

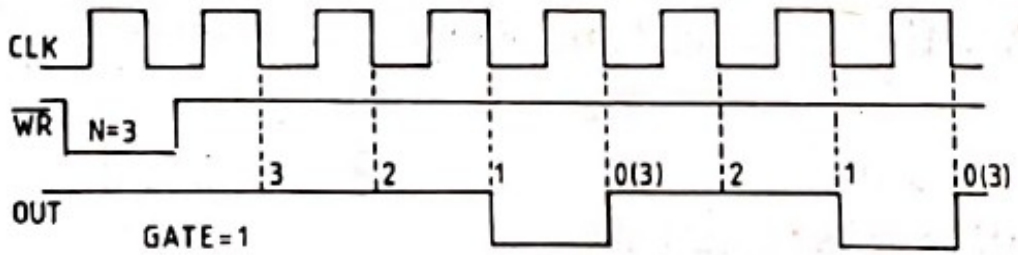


Fig. 7.32. MODE 2, Rate Generator.

Mode 3—square wave generator

It is similar to Mode 2 except that the OUT remains high for the first-half of the count and goes low for the other-half, thus generating a programmable square wave shape at OUT. Suppose n is the number loaded into the counter, then the OUT will be

- High for $n/2$ counts and low for $n/2$ counts if n = even
- High for $(n + 1)/2$ counts and low for $(n - 1)/2$ counts if n = odd. The GATE input function is the same as that in Mode 2.

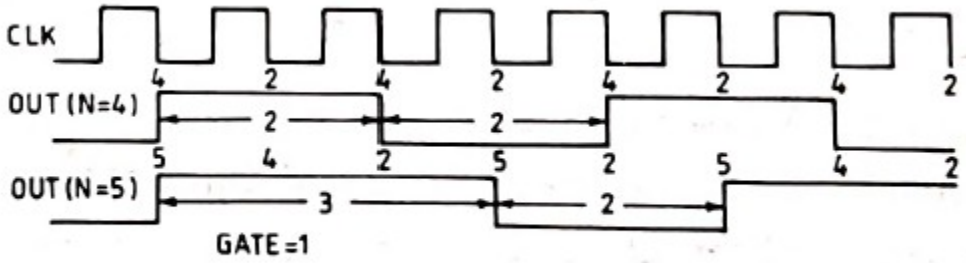


Fig. 7.33. MODE 3, Square Wave Generator.

Mode 4—software triggered strobe

The OUT is initially high and goes low for one clock period on the terminal count. Thus, a pulse can be generated by software. The GATE input when low disables the counting and when high, enables the counting. The difference between Mode 4 and Mode 2 is that in Mode 2, the OUT pulses are generated continuously after every N clock pulses (i.e. on terminal count but N is reloaded automatically), but in Mode 4, the OUT pulse is generated only once after N clock pulses (i.e. terminal count, but no automatic reloading).

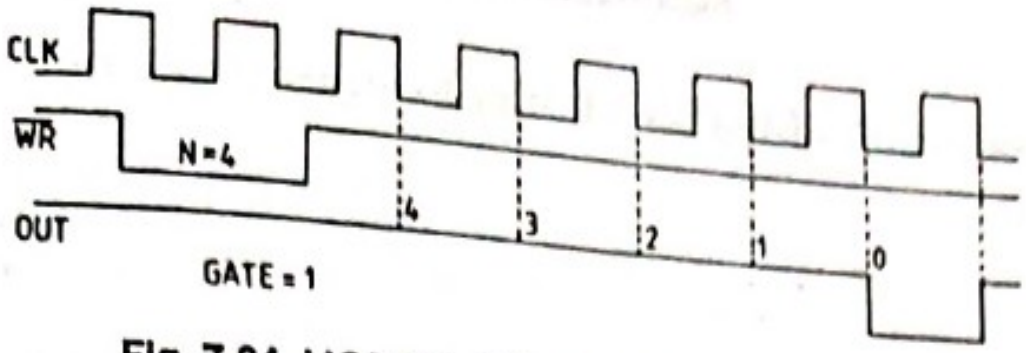


Fig. 7.34. MODE 4, Software Triggered Strobe.

Mode 5—hardware triggered strobe

The OUT is initially high. The counter will start counting after the rising edge of the GATE input and the OUT will go low for one clock period when the terminal count is reached.

The hardware circuit should trigger the GATE input to initiate the counting operation, thereby generating the OUT pulse.

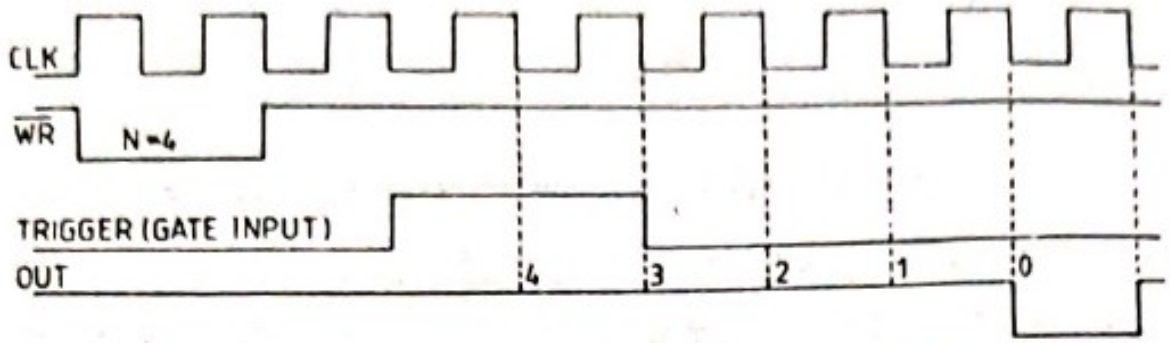


Fig. 7.35 MODE 5, Hardware Triggered Strobe

Modes \ Signal Status	Low or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	(1) Initiates counting (2) Resets output after next clock	—
2	(1) Disables counting (2) Sets output immediately high	(1) Reloads counter (2) Initiates counting	Enables counting
3	(1) Disables counting (2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

FIGURE 15.25
Gate Settings of a Counter

Interfacing the 8253/8254

shows the interfacing of the 8085 with the 8253.