PROGRAMMABLE INTERRUPT CONTROLLER 8259

What is Interrupt?

INTR

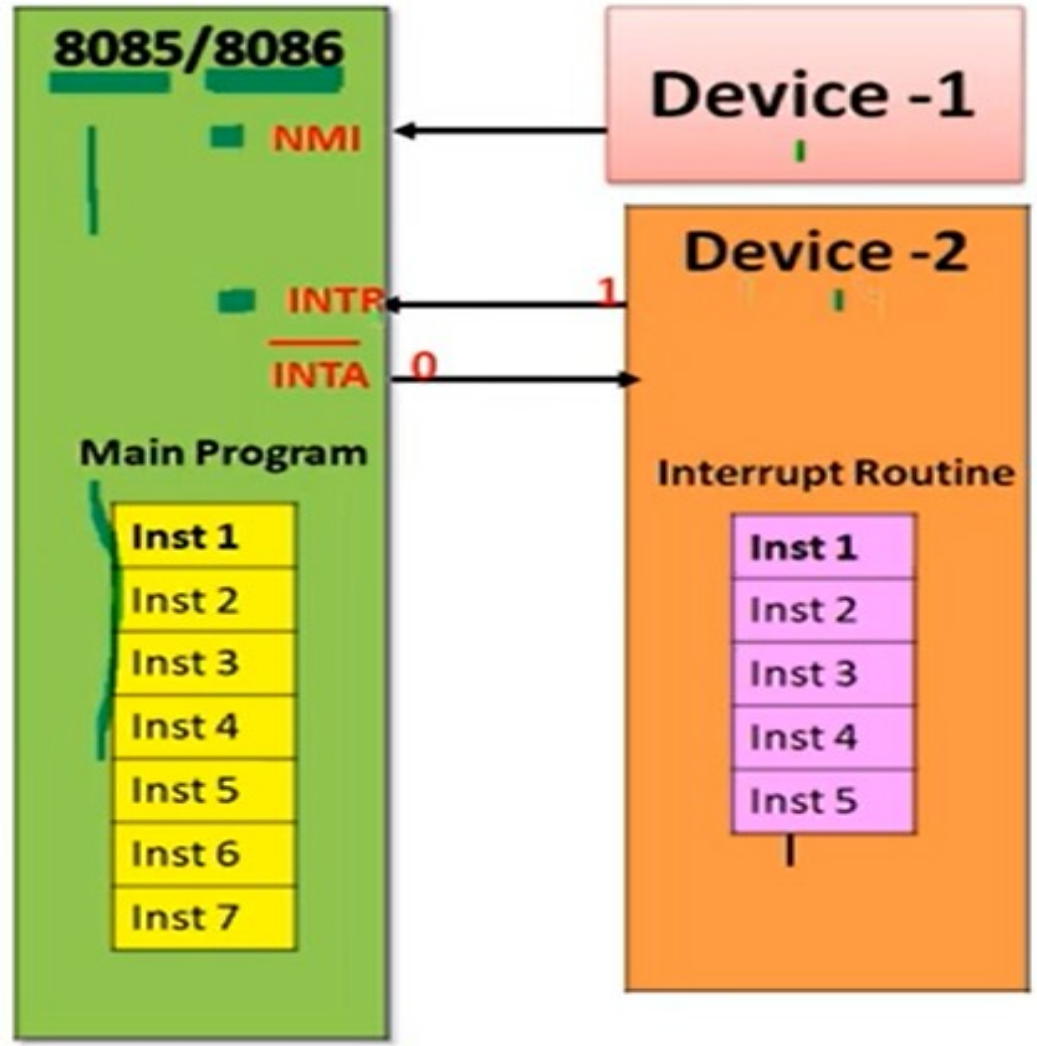
It is an interrupt request signal, which is sampled during the last clock cycle of each instruction to determine if the processor considered this as an interrupt or not.

NMI

It stands for non- interrupt It is an edge triggered inputnon maskable, which causes an interrupt request to the microprocessor.

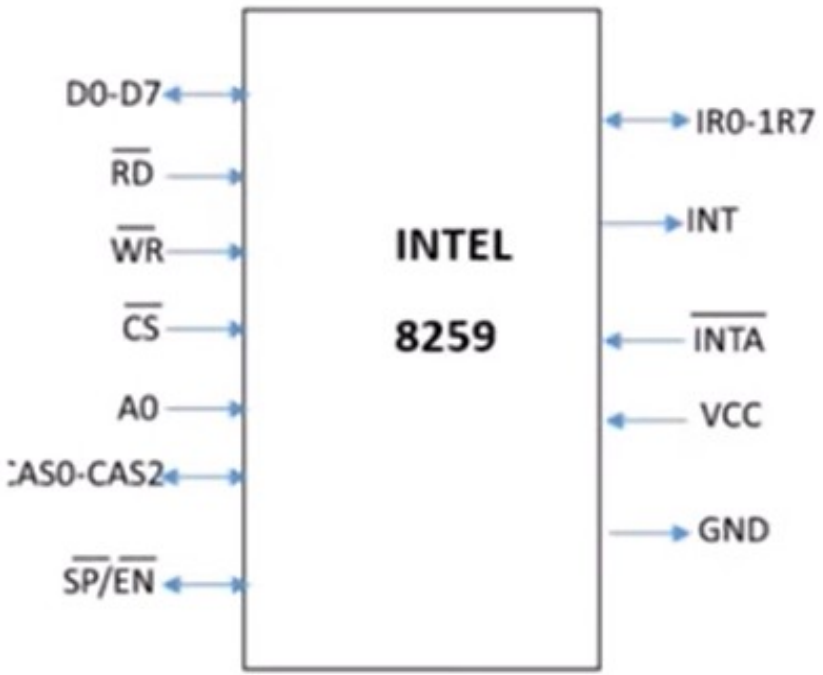
$\overline{\text{INTA}}$

It is an interrupt acknowledgement. When the microprocessor receives this signal, it acknowledges the interrupt.



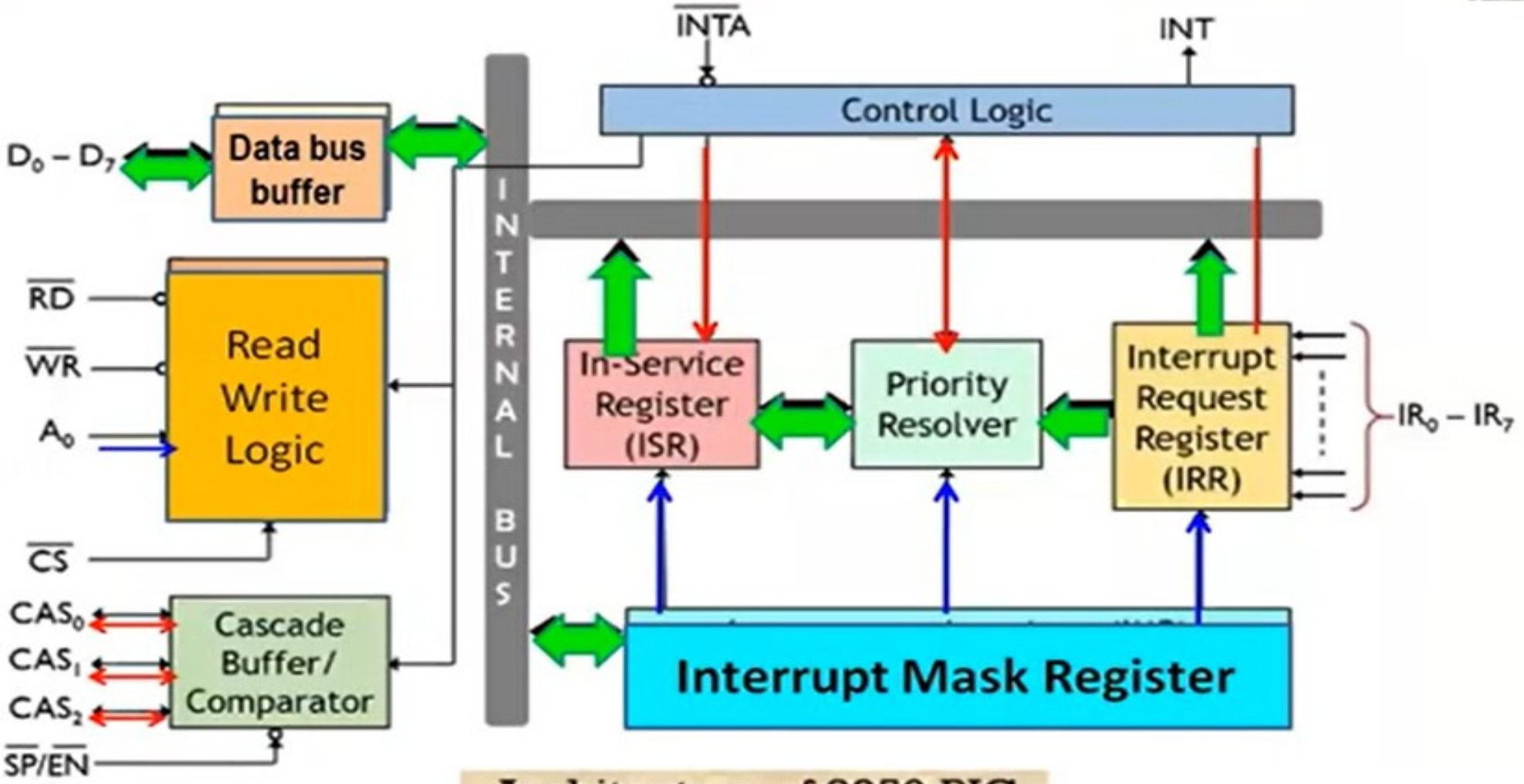
Pin details of 8259

- 28 pin IC packed in DIP

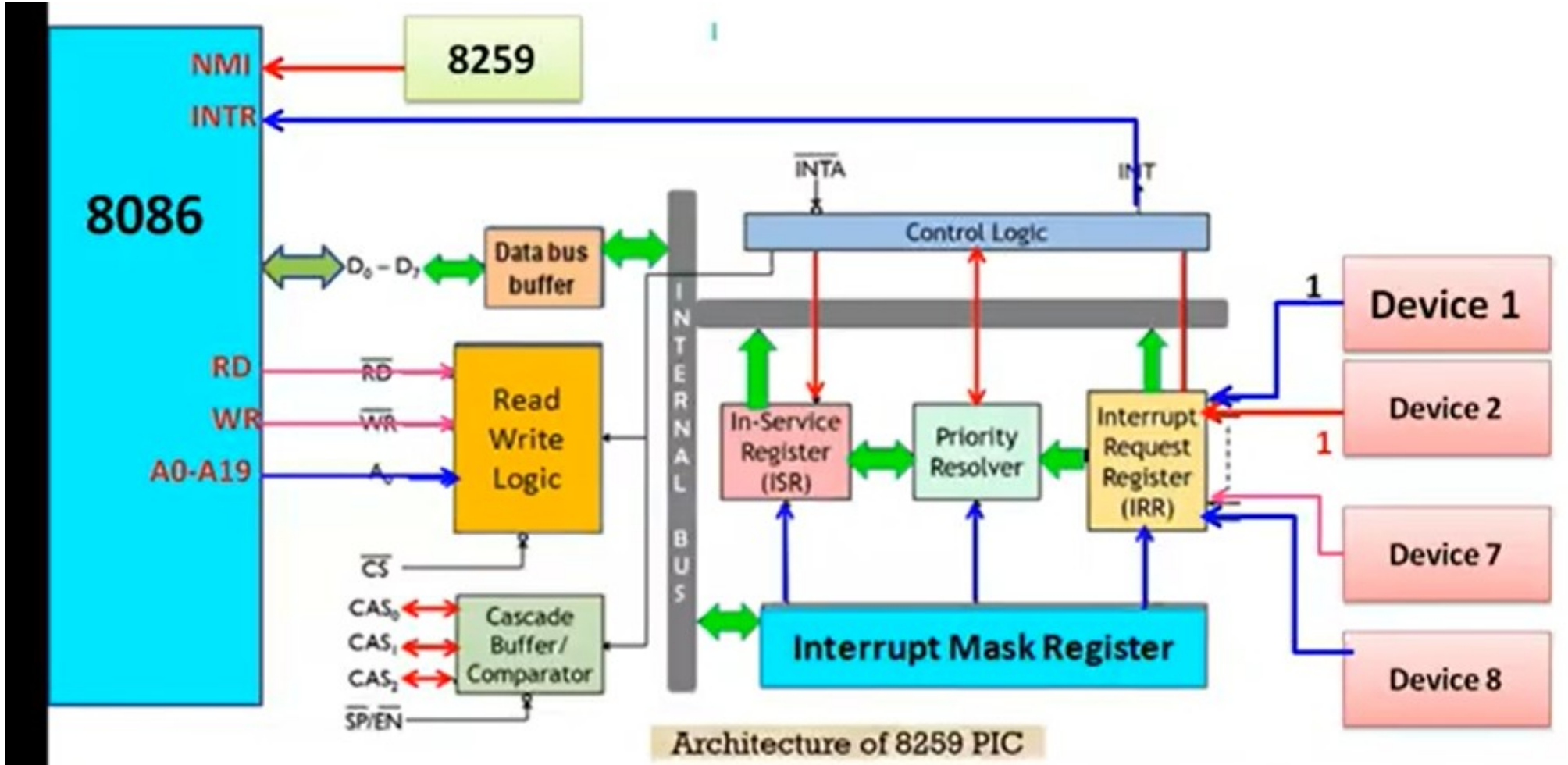


PIN	DESCRIPTION
D0-D7	Bidirectional datalines
$\overline{RD}$	Read control
$\overline{WR}$	Write control
A0	Internal address
$\overline{CS}$	Chip select
$\overline{SP}/\overline{EN}$	Slave program /enable buffer
INT	Interrupt output
$\overline{INTA}$	Interrupt aknowledge input
IR0-IR7	Interrupt request pin

8259 is defined as **Programmable Interrupt Controller (PIC)**



Architecture of 8259 PIC



Architecture of 8259 PIC

There are 5 hardware interrupts in 8085 and 2 hardware interrupts in 8086.. But by connecting 8259 with CPU, we can increase the interrupt handling capability.

Data bus buffer –

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus.

Thus, shows that a maximum of 8 bits data can be transferred at a time.

Control words and status information are transferred through the Data Bus Buffer.

This Block takes the control word from the 8085/8086 (let say) microprocessor and transfer it to the control logic of 8259.

Read/Write logic –

A0 This input signal is used in conjunction with WR and RD signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

Read/Write logic –

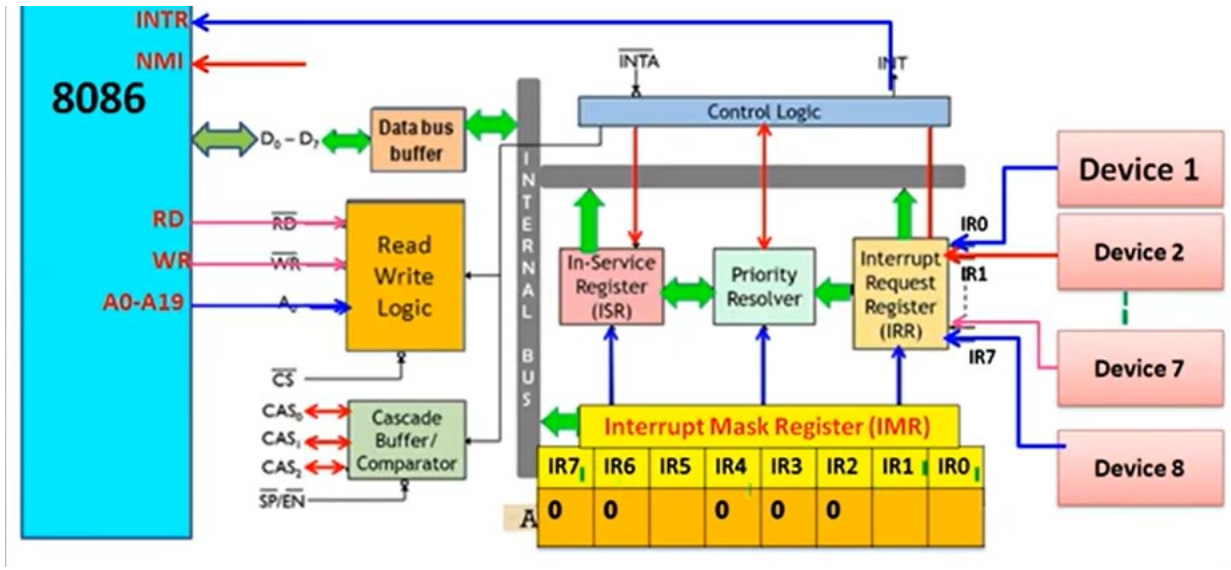
This block works only when the value of pin CS is low (as this pin is active low). This block is responsible for the flow of data depending upon the inputs of RD and WR. These two pins are active low pins used for read and write operations.

Control logic –

It is the centre of the 8259 and controls the functioning of every block. It has pin INTR which is connected with other microprocessor for taking interrupt request and pin INT for giving the output.

Interrupt mask register (IMR) –

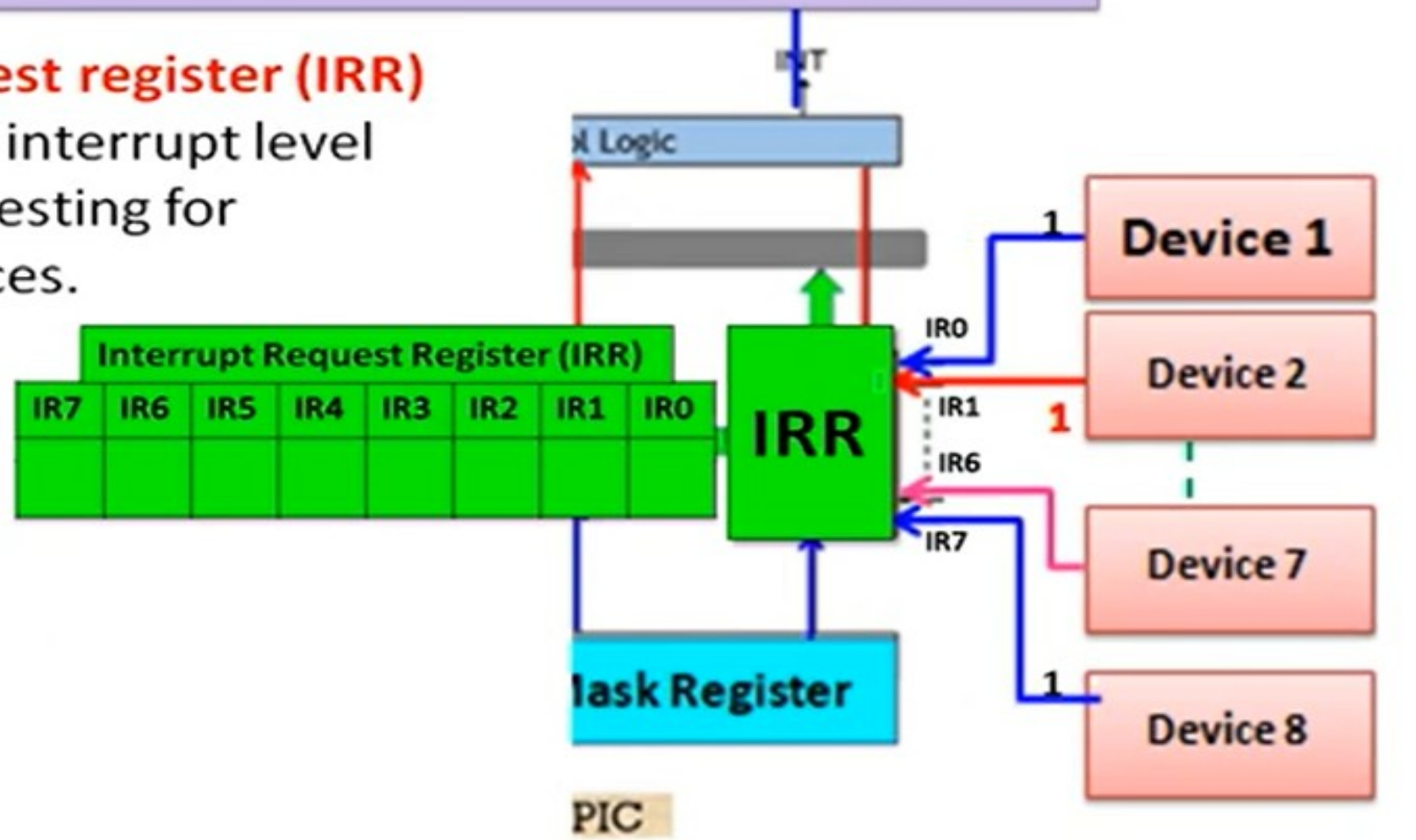
It stores the interrupt level which have to be masked by storing the masking bits of the interrupt level.



8259 combines the multi interrupt input sources into a single interrupt output. Interfacing of single PIC provides 8 interrupts inputs from IR0-IR7.

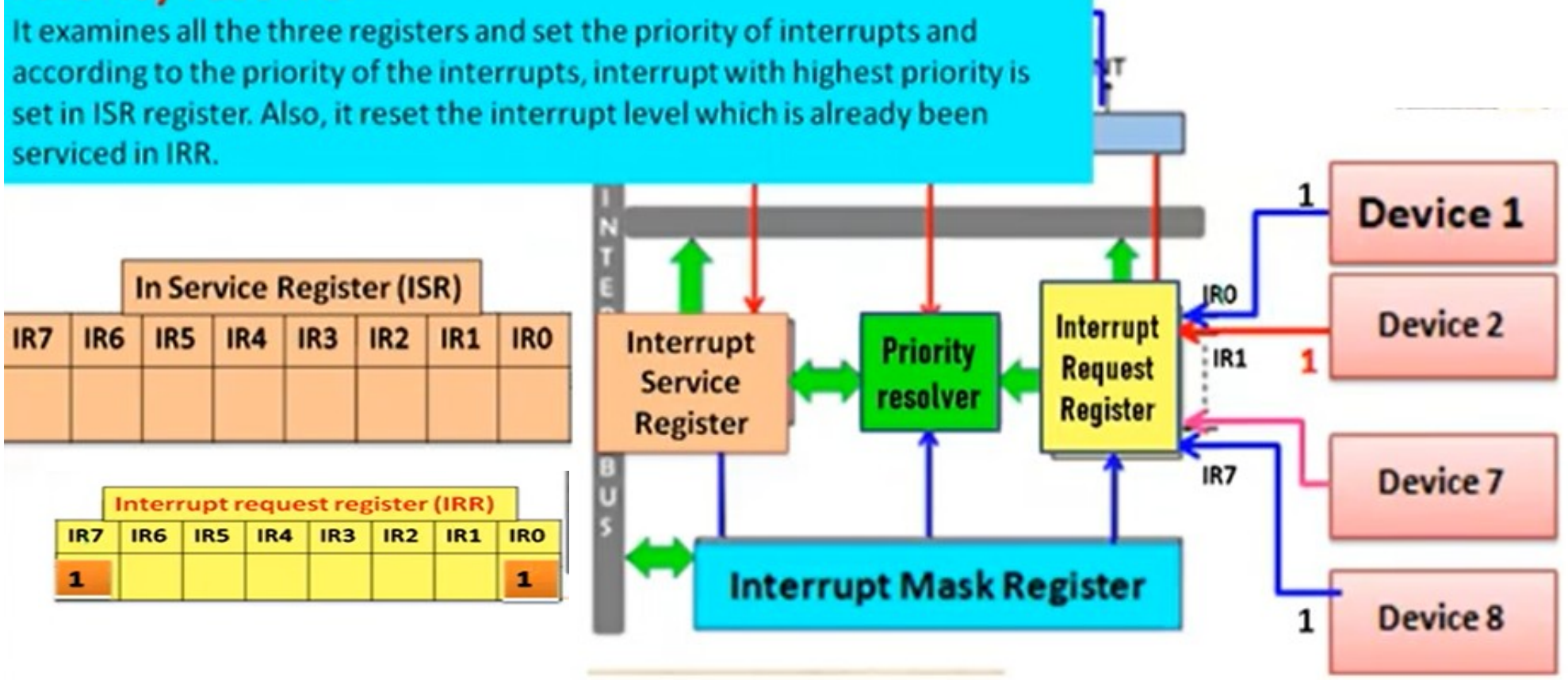
Interrupt request register (IRR)

It stores all the interrupt level which are requesting for Interrupt services.



Priority resolver –

It examines all the three registers and set the priority of interrupts and according to the priority of the interrupts, interrupt with highest priority is set in ISR register. Also, it reset the interrupt level which is already been serviced in IRR.



Interrupt service register (ISR) –

It stores the interrupt level which are currently being executed.

Cascade buffer –

To increase the Interrupt handling capability, we can further cascade more number of pins by using cascade buffer. So, during increment of interrupt capability, CSA lines are used to control multiple interrupt structure.