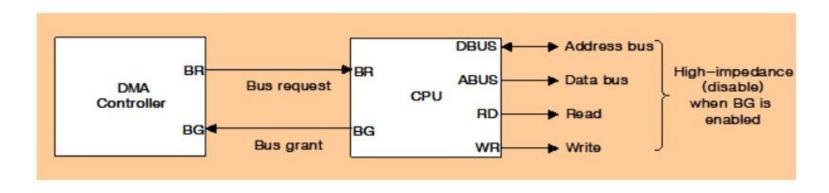
# A Presentation On

# **Direct Memory Access (DMA)**

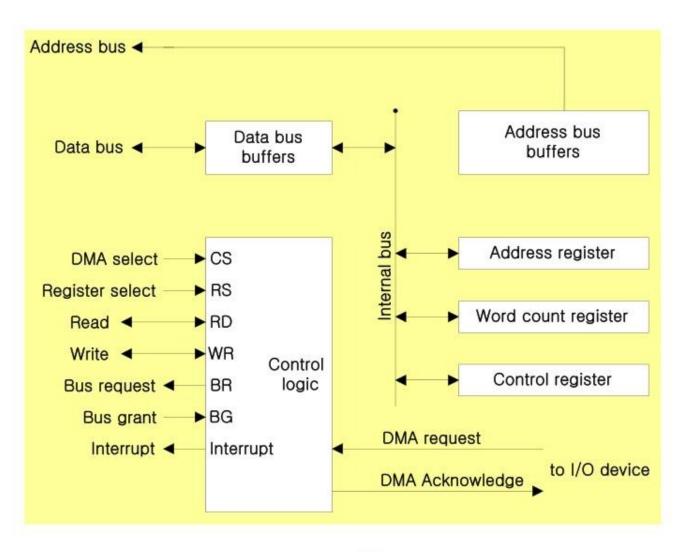
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#### Introduction

- The transfer of data between the memory and an external device without involving the micro processor improves the speed of transfer.
- This transfer technique is called DMA.



#### **DMA Controller**

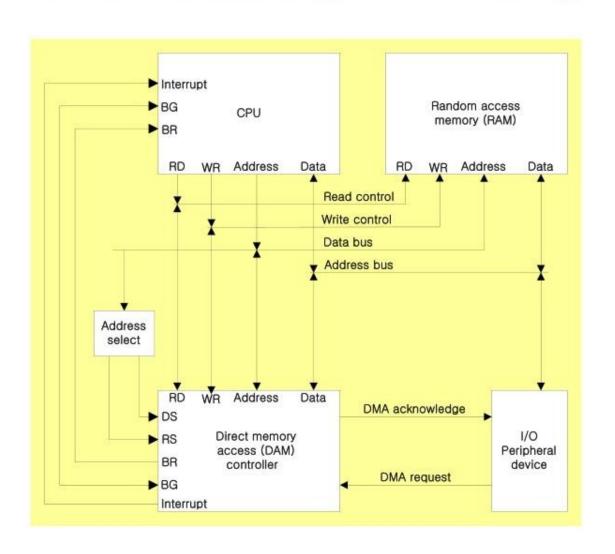


#### **DMA Controller**

- DMA controller is used to transfer the data between the memory and i/o device.
- The DMA controller needs the usual circuits to communicate with the CPU and i/o device.
- In addition to this, it needs an address register and address bus buffer.
- The address register contains an address of the desired location in memory.
- The word count register holds the number of words to be transferred. The control register specifies the mode of transfer.
- The DMA communicates with the i/o devices through the DMA request and DMA acknowledge line.
- The DMA communicates with the CPU through the data bus and control lines.

- The RD (Read) and WR (write) signals are bidirectional.
- When the BG (Bus Grant) signal are bidirectional.
- When the BG (Bus Grant) signal is 0, the CPU can communicate with the DMA registers through the data bus.
- When BG is 1, the CPU has relinquished the buses.
- Then the DMA can communicate directly with the memory.

#### **DMA Transfer (I/O to Memory)**



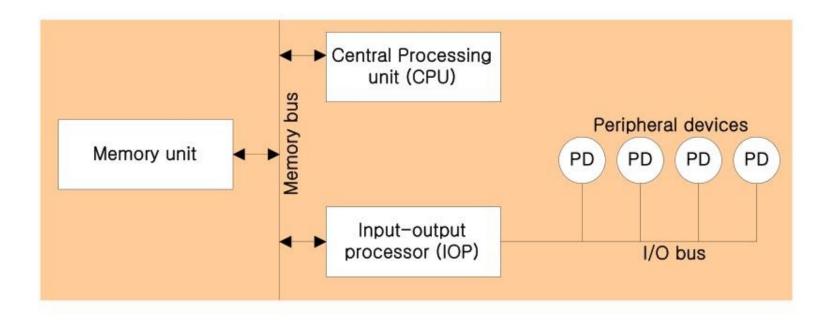
#### **Process of DMA Transfer**

- To initiate a DMA transfer, the CPU loads the address of the first memory location of the memory block (to be read or written from) into the DMA address register. It does his via an I/O output instruction, such as the OTPT instruction for the relatively simple CPU.
- It then writes the no. of bytes to be transferred into the DMA count register in the sane manner.
- Finally, it writes one or more commands to the DMA control register.

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- These commands may specify transfer options such as the DMA transfer mode, but should always specify the direction of the transfer, either from I/O to memory or from memory to I/O.
- The last command causes the DMA controller to initiate the transfer. The controller then sets BR to 1 and, once BG becomes 1, seizes control of the system buses.

#### **Input-Output Processor (IOP)**



#### Introduction

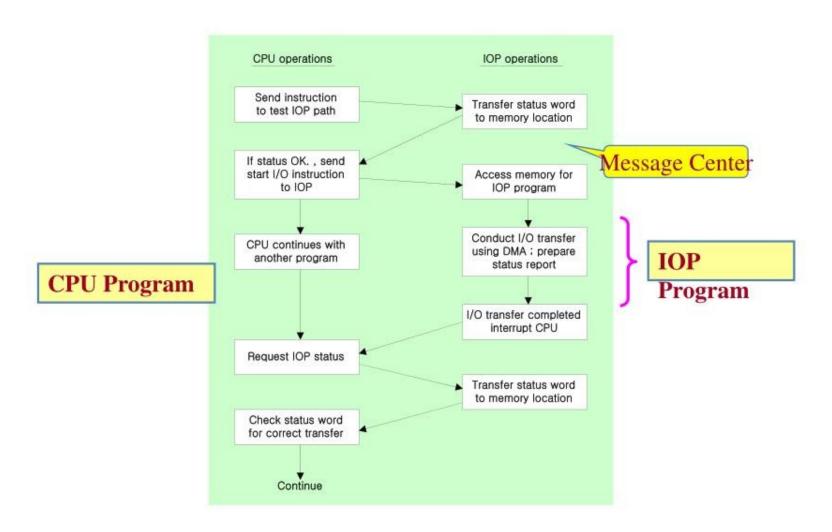
#### • **IOP**:

- Communicate directly with all I/O devices
- Fetch and execute its own instruction
  - IOP instructions are specifically designed to facilitate I/O transfer
  - DMAC must be set up entirely by the CPU
- Designed to handle the details of I/O processing

Command

- Instruction that are read form memory by an IOP
  - Distinguish from instructions that are read by the CPU
  - Commands are prepared by experienced programmers and are stored in memory
  - Command word = IOP program

#### **CPU - IOP Communication**



#### **CPU - IOP Communication**

- The communication between CPU and IOP may take different forms depending on the particular computer considered.
- The CPU sends a test I/O instruction to IOP to test the IOP path.
- The responds by inserting a status word in memory location.
- The CPU refers to the status word in memory. If everything is in order, the
   CPU sends the start I/O instruction to start the I/O transfer.
- The IOP accesses memory for IOP program.
- The CPU can now continue with another program while the IOP is busy with the program. Both programs refer to memory by means of DMA transfer.

- When the IOP terminates the execution of its program, it sends an interrupt request to the CPU.
- The CPU then issues a read I/O instruction to read the status from the IOP.
- The IOP transfers the status word to memory location.
- The status word indicates whether the transfer has been completed satisfactorily or if any error has occurred during the transfer.

#### The End

#### Thank U