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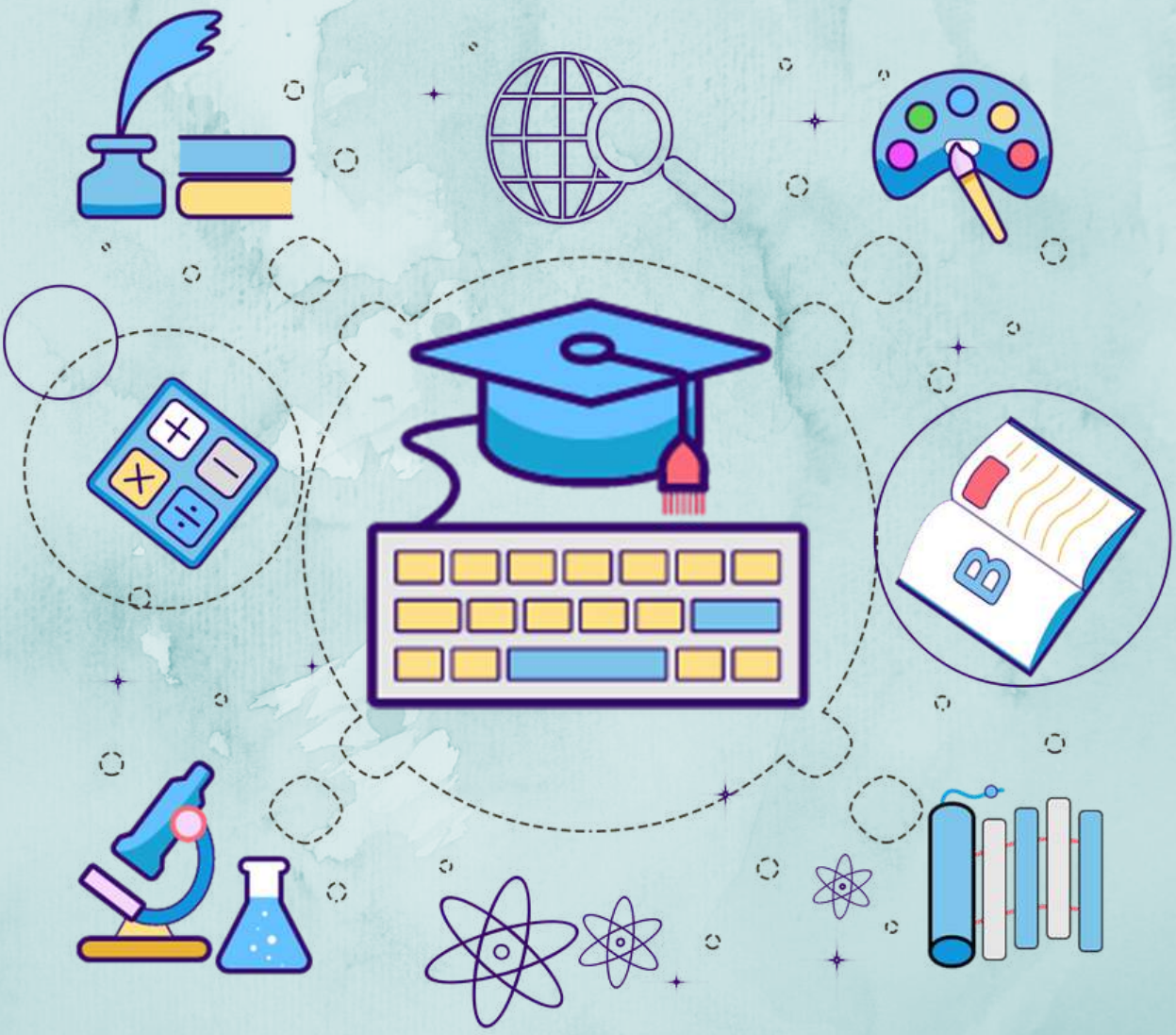

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COMPUTER ORGANIZATION AND ARCHITECTURE

Multiple choice questions

1. SIMD represents an organization that_____.
   (A) refers to a computer system capable of processing several programs at the same time.
   (B) *represents organization of single computer containing a control unit, processor unit and* a memory unit.
   (C) includes many processing units under the supervision of a common control unit
   (D) none of the above.

2. Floating point representation is used to store
   (A) Boolean values (B) whole numbers (C) real integers (D) integers

3. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?
   (A) 1 Megabyte/sec (B) 4 Megabytes/sec
   (C) 8 Megabytes/sec (D) 2 Megabytes/sec

4. Assembly language
   (A) uses alphabetic codes in place of binary numbers used in machine language
   (B) is the easiest language to write programs
   (C) need not be translated into machine language
   (D) None of these

5. In computers, subtraction is generally carried out by
   (E) 9's complement (B) 10's complement
   (C) 1's complement (D) 2's complement

5. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to
   (A) the time its takes for the platter to make a full rotation
   (B) the time it takes for the read-write head to move into position over the appropriate track
   (C) the time it takes for the platter to rotate the correct sector under the head
   (D) none of the above

6. What characteristic of RAM memory makes it not suitable for permanent storage?
   (A) too slow (B) unreliable (C) it is volatile (D) too bulky
7. Computers use addressing mode techniques for_____.
   (A) giving programming versatility to the user by providing facilities as pointers to memory counters for loop control
   (B) to reduce no. of bits in the field of instruction
   (C) specifying rules for modifying or interpreting address field of the instruction
   (D) All the above
8. The circuit used to store one bit of data is known as
   (A) Register (B) Encoder (C) Decoder (D) Flip Flop
9. (2FAOC) 16 is equivalent to
   (A) (195 084) 10 (B) (001011111010 0000 1100) 2
   (C) Both (A) and (B) (D) None of these

10. The average time required to reach a storage location in memory and obtain its contents is called the
    (A) seek time (B) turnaround time (C) access time (D) transfer time
11. Which of the following is not a weighted code?
    (A) Decimal Number system (B) Excess 3-cod
    (C) Binary number System (D) None of these

12. The idea of cache memory is based
    (A) on the property of locality of reference (B) on the heuristic 90-10 rule
    (C) on the fact that references generally tend to cluster (D) all of the above

13. Which of the following is lowest in memory hierarchy?
    (A) Cache memory
    (B) Secondary memory
    (C) Registers
    (D) RAM
    (E) None of these

14. The addressing mode used in an instruction of the form ADD X Y, is
    (A) Absolute (B) indirect (C) index (D) none of these

15. If memory access takes 20 ns with cache and 110 ns with out it, then the ratio (cache uses a 10 ns memory) is

(A) 93% (B) 90% (C) 88% (D) 87%

16. In a memory-mapped I/O system, which of the following will not be there?
(A) LDA (B) IN (C) ADD (D) OUT

17. In a vectored interrupt.
(A) the branch address is assigned to a fixed location in memory.
(B) the interrupting source supplies the branch information to the processor through an interrupt vector.
(C) the branch address is obtained from a register in the processor
(D) none of the above

18. Von Neumann architecture is
(A) SISD (B) SIMD (C) MIMD (D) MISD

19. The circuit used to store one bit of data is known as
(A) Encoder (B) OR gate (C) Flip Flop (D) Decoder

20. Cache memory acts between
(A) CPU and RAM (B) RAM and ROM (C) CPU and Hard Disk (D) None of these

21. Write Through technique is used in which memory for updating the data
(A) Virtual memory (B) Main memory
(C) Auxiliary memory (D) Cache memory

22. Generally Dynamic RAM is used as main memory in a computer system as it
(A) Consumes less power (B) has higher speed
(C) has lower cell density (D) needs refreshing circuitary

23. In signed-magnitude binary division, if the dividend is (11100) 2 and divisor is (10011) 2 then the result is
(A) (00100) 2 (B) (10100) 2 (C) (11001) 2 (D) (01100) 2

24. Virtual memory consists of
(A) Static RAM (B) Dynamic RAM
(C) Magnetic memory (D) None of these

25. In a program using subroutine call instruction, it is necessary
(A) initialise program counter (B) Clear the accumulator
(C) Reset the microprocessor (D) Clear the instruction register

26. A Stack-organised Computer uses instruction of

(A) Indirect addressing (B) Two-addressing (C) Zero addressing (D) Index addressing

27. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be
(A) 11 bits (B) 21 bits (C) 16 bits (D) 20 bits

30 A-Flip Flop can be converted into T-Flip Flop by using additional logic circuit
(A) n TQD =• (B) T D = (C) D = T . Q n (D) n TQD =⊕

31. Logic X-OR operation of (4ACO) H & (B53F) H results
(A) AACB (B) 0000 (C) FFFF (D) ABCD

32. When CPU is executing a Program that is part of the Operating System, it is said to be in (A) Interrupt mode (B) System mode (C) Half mode (D) Simplex mode

33. An n-bit microprocessor has
(A) n-bit program counter (B) n-bit address register
(C) n-bit ALU (D) n-bit instruction register

34. Cache memory works on the principle of
(A) Locality of data (B) Locality of memory
(C) Locality of reference (D) Locality of reference & memory

35. The main memory in a Personal Computer (PC) is made of
(A) cache memory. (B) static RAM
(C) Dynamic Ram (D) both (A) and (B) .

36. In computers, subtraction is carried out generally by
(A) 1's complement method (B) 2's complement method
(C) signed magnitude method (D) BCD subtraction method

37. PSW is saved in stack when there is a
(A) interrupt recognised (B) execution of RST instruction
(C) Execution of CALL instruction (D) All of these

38. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be
(A) (812) 10 (B) (-12) 10 (C) (12) 10 (D) (-812) 10

39. The circuit converting binary data in to decimal is
(A) Encoder (B) Multiplexer (C) Decoder (D) Code converter

40. A three input NOR gate gives logic high output only when
(A) one input is high (B) one input is low
(C) two input are low (D) all input are high

41. n bits in operation code imply that there are possible distinct operators
(A) 2n (B) 2n (C) n/2 (D) n2

42. _register keeps tracks of the instructions stored in program stored in memory.
(A) AR (Address Register) (B) XR (Index Register)
(C) PC (Program Counter) (D) AC (Accumulator)

43. Memory unit accessed by content is called
(A) Read only memory (B) Programmable Memory
(C) Virtual Memory (D) Associative Memory

44. 'Aging registers' are
(A) Counters which indicate how long ago their associated pages have been referenced.
(B) Registers which keep track of when the program was last accessed.
(C) Counters to keep track of last accessed instruction.
(D) Counters to keep track of the latest data structures referred.

45 The instruction 'ORG O' is a
(A) Machine Instruction. (B) Pseudo instruction.
(C) High level instruction. (D) Memory instruction.

46 Translation from symbolic program into Binary is done in
(A) Two passes. (B) Directly (C) Three passes. (D) Four passes.

47 A floating point number that has a O in the MSB of mantissa is said to have
(A) Overflow (B) Underflow (C) Important number (D) Undefined

48 The BSA instruction is
(A) Branch and store accumulator (B) Branch and save return address
(C) Branch and shift address (D) Branch and show accumulator

49 State whether True or False.
(i) Arithmetic operations with fixed point numbers take longer time for execution as compared to with floating point numbers. True
.
(ii) An arithmetic shift left multiplies a signed binary number by 2. False

50 Logic gates with a set of input and outputs is arrangement of
(A) Combinational circuit (B) Logic circuit (C) Design circuits (D) Register

51. MIMD stands for
(A) Multiple instruction multiple data (B) Multiple instruction memory data
(C) Memory instruction multiple data (D) Multiple information memory data

52 A k-bit field can specify any one of
(A) 3k registers (B) 2k registers
(C) K2 registers (D) K3 registers

53 The time interval between adjacent bits is called the
(A) Word-time (B) Bit-time (C) Turn around time (D) Slice time

54 A group of bits that tell the computer to perform a specific operation is known as
(A) Instruction code (B) Micro-operation (C) Accumulator (D) Register

55 The load instruction is mostly used to designate a transfer from memory to a processor register known as
(A) Accumulator (B) Instruction Register
(C) Program counter (D) Memory address Register

56 The communication between the components in a microcomputer takes place via the address and
(A) I/O bus (B) Data bus (C) Address bus (D) Control lines

57 An instruction pipeline can be implemented by means of
(A) LIFO buffer (B) FIFO buffer (C) Stack (D) None of the above

58 Data input command is just the opposite of a
(A) Test command (B) Control command (C) Data output (D) Data channel

59 A microprogram sequencer
(A) generates the address of next micro instruction to be executed.
(B) generates the control signals to execute a microinstruction.
(C) sequentially averages all microinstructions in the control memory.
(D) enables the efficient handling of a micro program subroutine.

60 . A binary digit is called a
(A) Bit (B) Byte (C) Number (D) Character

61 A flip-flop is a binary cell capable of storing information of
(A) One bit ✓ (B) Byte (C) Zero bit (D) Eight bit

62 The operation executed on data stored in registers is called
(A) Macro-operation (B) Micro-operation ✓
(C) Bit-operation (D) Byte-operation

63 MRI indicates
(A) Memory Reference Information. (B) Memory Reference Instruction. ✓
(C) Memory Registers Instruction. (D) Memory Register information

64 Self-contained sequence of instructions that performs a given computational task is called
(A) Function ✓ (B) Procedure (C) Subroutine (D) Routine

65 Microinstructions are stored in control memory groups, with each group specifying a
(A) Routine ✓ (B) Subroutine (C) Vector (D) Address

66 An interface that provides a method for transferring binary information between internal storage and external devices is called
(A) I/O interface ✓ (B) Input interface (C) Output interface (D) I/O bus

67 Status bit is also called
(A) Binary bit (B) Flag bit ✓ (C) Signed bit (D) Unsigned bit

68 An address in main memory is called
✓ (A) Physical address (B) Logical address (C) Memory address (D) Word address

69 If the value V(x) of the target operand is contained in the address field itself, the addressing mode is
(A) immediate. (B) direct. ✓ (C) indirect. (D) implied.

70 can be represented in a signed magnitude format and in a 1's complement format as
(A) 111011 & 100100 ✓ (B) 100100 & 111011
(C) 011011 & 100100 (D) 100100 & 011011

71 The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called
✓ (A) Data transfer instructions. (B) Program control instructions.
(C) Input-output instructions. (D) Logical instructions.

72 A device/circuit that goes through a predefined sequence of states upon the application of input pulses is called

(A) register (B) flip-flop (C) transistor. (D) counter.

73. The performance of cache memory is frequently measured in terms of a quantity called

(A) Miss ratio. (B) Hit ratio. (C) Latency ratio. (D) Read ratio.

74. The information available in a state table may be represented graphically in a

(A) simple diagram. (B) state diagram. (C) complex diagram. (D) data flow diagram.

75 Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called.

(A) relative address mode. (B) index addressing mode.

(C) register mode. (D) implied mode.

76 An interface that provides I/O transfer of data directly to and form the memory unit and peripheral is termed as

(A) DDA. (B) Serial interface. (C) BR. (D) DMA.

77 The 2s compliment form (Use 6 bit word) of the number 1010 is

(A) 111100. (B) 110110. (C) 110111. (D) 1011.

78 A register capable of shifting its binary information either to the right or the left is called a

(A) parallel register. (B) serial register. (C) shift register. (D) storage register.

79 What is the content of Stack Pointer (SP)?

(A) Address of the current instruction (B) Address of the next instruction

(C) Address of the top element of the stack (D) Size of the stack.

80 Which of the following interrupt is non maskable

(A) INTR. (B) RST 7.5. (C) RST 6.5. (D) TRAP.

81 Which of the following is a main memory

(A) Secondary memory. (B) Auxiliary memory.

(C) Cache memory. (D) Virtual memory.

82 Which of the following are not a machine instructions

(A) MOV. (B) ORG. (C) END. (D) (B) & (C) .

83 In Assembly language programming, minimum number of operands required for an instruction is/are

(A) Zero. (B) One. (C) Two. (D) Both (B) & (C) .

84 The maximum addressing capacity of a micro processor which uses 16 bit database & 32 bit address base is

(A) 64 K. (B) 4 GB. (C) both (A) & (B) . (D) None of these.

85 The memory unit that communicates directly with the CPU is called the

(A) main memory (B) Secondary memory

(C) shared memory (D) auxiliary memory.

86 The average time required to reach a storage location in memory and obtain its contents is called

(A) Latency time. (B) Access time.

(C) Turnaround time. (D) Response time.

State True or False

87 A byte is a group of 16 bits. False

88 A nibble is a group of 16 bits. False

89 When a word is to be written in an associative memory, address has got to be given. False

90 When two equal numbers are subtracted, the result would be +zero and not -zero.

.

91 A microprocessor development system and an assembler are essential tools for writing large assembly language programs.

92 In an operation performed by the ALU, carry bit is set to 1 if the end carry C 8 is one. It is cleared to 0 (zero) if the carry is zero .

93 A successive A/D converter is

(A) a high-speed converter. (B) a low speed converter.

(C) a medium speed converter. (D) none of these.

94 When necessary, the results are transferred from the CPU to main memory by

(A) I/O devices. (B) CPU. (C) shift registers. (D) none of these.

96 A combinational logic circuit which sends data coming from a single source to two or more separate destinations is

(A) Decoder. (B) Encoder. (C) Multiplexer. (D) Demultiplexer.

97 In which addressing mode the operand is given explicitly in the instruction

(A) Absolute. (B) Immediate . (C) Indirect. (D) Direct.

98 A stack organized computer has

(A) Three-address Instruction. (B) Two-address Instruction.

(C) One-address Instruction. (D) Zero-address Instruction.

99 A Program Counter contains a number 825 and address part of the instruction contains the number 24. The effective address in the relative address mode, when an instruction is read from the memory is

(A) 849. (B) 850. (C) 801. (D) 802.

102 A page fault

(A) Occurs when there is an error in a specific page.

(B) Occurs when a program accesses a page of main memory.

(C) Occurs when a program accesses a page not currently in main memory.

(D) Occurs when a program accesses a page belonging to another program.

103. The load instruction is mostly used to designate a transfer from memory to a processor register known as_____.

A. Accumulator B. Instruction Register

C. Program counter D. Memory address Register

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A. (812)10 B. (-12)10
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C. Dynamic Ram D. bothA.and (B).

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B. 10's complement
C. 1's complement
D. 2's complement

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b. is the easiest language to write programs
c. need not be translated into machine language
d. None of these

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B. 4 Megabytes/sec
C. 8 Megabytes/sec
D. 2 Megabytes/sec

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B. whole numbers
C. real integers
D. integers

155. SIMD represents an organization that_____.

a. refers to a computer system capable of processing several programs at the same time.
b. represents organization of single computer containing a control unit, processor unit and a memory unit.
c. includes many processing units under the supervision of a common control unit
d. none of the above.

156. Processors of all computers, whether micro, mini or mainframe must have
a. ALU b. Primary Storage
c. Control unit d. All of above

157. What is the control unit's function in the CPU?
a. To transfer data to primary storage
b. to store program instruction
c. to perform logic operations
d. to decode program instruction

158. What is meant by a dedicated computer?
a. which is used by one person only
b. which is assigned to one and only one task
c. which does one kind of software
d. which is meant for application software only

159. The most common addressing techiniques employed by a CPU is
a. immediate b. direct
c. indirect d. register e. all of the above

160. Pipeline implement
a. fetch instruction b. decode instruction
c. fetch operand d. calculate operand
e. execute instruction f. all of abve

161. Which of the following code is used in present day computing was developed by IBM corporation?
a. ASCII b. Hollerith Code
c. Baudot code d. EBCDIC code

162. When a subroutine is called, the address of the instruction following the CALL instructions stored in/on the
a. stack pointer b. accumulator
c. program counter d. stack

163. A microprogram written as string of 0's and 1's is a
a. symbolic microinstruction b. binary microinstruction
c. symbolic microprogram d. binary microprogram

164. Interrupts which are initiated by an instruction are
a. internal b. external c. hardware d. software

165. Memory access in RISC architecture is limited to instructions

a. CALL and RET b. PUSH and POP
c. STA and LDA d. MOV and JMP

166. A collection of lines that connects several devices is called .....
A) bus B) peripheral connection wires
C) Both a and b D) internal wires

167. A complete microcomputer system consist of .....
A) microprocessor B) memory
C) peripheral equipment D) all of the above

168. PC Program Counter is also called .....
A) instruction pointer B) memory pointer
C) data counter D) file pointer

169. In a single byte how many bits will be there?
A) 8 B) 16 C) 4 D) 32

170. CPU does not perform the operation .....
A) data transfer B) logic operation
C) arithmetic operation D) all of the above

171. The access time of memory is the time required for performing any single CPU operation.
A) Longer than B) Shorter than
C) Negligible than D) Same as

172. Memory address refers to the successive memory words and the machine is called as .....
A) word addressable B) byte addressable
C) bit addressable D) Tera byte addressable

173. A microprogram written as string of 0's and 1's is a .....
A) Symbolic microinstruction B) binary microinstruction
C) symbolic microinstruction D) binary microprogram

175. A pipeline is like .....
A) an automobile assembly line B) house pipeline
C) both a and b D) a gas line

176. Data hazards occur when .....
A) Greater performance loss
B) Pipeline changes the order of read/write access to operands

C) Some functional unit is not fully pipelined
D) Machine size is limited

177. Where does a computer add and compare data?
A. Hard disk B. Floppy disk
C. CPU chip D. Memory chip

178. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?
A. Memory Address Register
B. Memory Data Register
C. Instruction Register
D. Program Register

179. A complete microcomputer system consists of
A) microprocessor
B) memory
C) peripheral equipment
D) all of above

180. CPU does not perform the operation
A. data transfer
B. logic operation
C. arithmetic operation
D. all of above

181. Pipelining strategy is called implement
A. instruction execution
B. instruction prefetch
C. instruction decoding
D. instruction manipulation

182. A stack is
A. an 8-bit register in the microprocessor
B. a 16-bit register in the microprocessor
C. a set of memory locations in R/WM reserved for storing information temporarily during the execution of computer
D. a 16-bit memory address stored in the program counter

183. A stack pointer is
A. a 16-bit register in the microprocessor that indicate the beginning of the stack memory.

B. a register that decodes and executes 16-bit arithmetic expression.
C. The first memory location where a subroutine address is stored.
D. a register in which flag bits are stored

184. The branch logic that provides decision making capabilities in the control unit is known as
A. controlled transfer
B. conditional transfer
C. unconditional transfer
D. none of above

185. Interrupts which are initiated by an instruction are
A. internal
B. external
C. hardware
D. software

186. A time sharing system imply
A. more than one processor in the system
B. more than one program in memory
C. more than one memory in the system
D. None of above

187. Virtual memory is –
(1) an extremely large main memory
(2) an extremely large secondary memory
(3) an illusion of an extremely large memory
(4) a type of memory used in super computers

(5) None of these

188. Fragmentation is -
(1) dividing the secondary memory into equal sized f ragments
(2) dividing the main memory into equal size f ragments
(3) f ragments of memory words used in a page
(4) f ragments of memory words unused in a page
(5) None of these

189. Which memory unit has lowest access time?
(1) Cache (2) Registers
(3) Magnetic Disk (4) Main Memory
(5) Pen drive

190. Cache memory-
(1) has greater capacity than RAM
(2) is f aster to access than CPU Registers
(3) is permanent storage
(4) f aster to access than RAM
(5) None of these

191. When more than one processes are running concurrently on a system-
(1) batched system
(2) real-time system
(3) multi programming system
(4) multiprocessing system
(5) None of these

192. Which of the following memories must be refreshed many times per second?
a. Static RAM b. Dynamic RAM c. EPROM
d. ROM e. None of these

193. RAM stands for
a. Random origin money b. Random only memory
c. Read only memory d. Random access memory
e. None of these

194. CPU fetches the instruction from memory according to the value of
a) program counter
b) status register
c) instruction register
d) program status word

195.A memory buffer used to accommodate a speed differential is called
a) stack pointer
b) cache

c) accumulator
d) disk buffer

196. Which one of the following is the address generated by CPU?
a) physical address
b) absolute address
c) logical address
d) none of the mentioned

197. Run time mapping from virtual to physical address is done by
a) memory management unit
b) CPU
c) PCI

198. none of the mentionedMemory management technique in which system stores and retrievesdata from secondary storage for use in main memory is called
a) fragmentation
b) paging
c) mapping
d) none of the mentioned

199.The address of a page table in memory is pointed by
a) stack pointer
b) page table base register
c) page register
d) program counter

200.Program always deals with
a) logical address
b) absolute address
c) physical address
d) relative address

1. Cache memory acts between

(A) CPU and RAM

(B) RAM and ROM

(C) CPU and Hard Disk

(D) None of these

Answer: A

2. Memory unit accessed by content is called

(A) Read only memory

(B) Programmable Memory

(C) Virtual Memory

(D) Associative Memory

Answer: D

3 .RAM stands for

a. Random origin money

b. Random only memory

c. Read only memory

d. Random access memory

e. None of these

Answer: Random access memory

4. An instruction pipeline can be implemented by means of

(A) LIFO buffer

(B) FIFO buffer

(C) Stack

(D) None of the above

Answer: B

5. Data input command is just the opposite of a

(A) Test command

(B) Control command

(C) Data output

(D) Data channel

Answer: C

6. Status bit is also called

(A) Binary bit

(B) Flag bit

(C) Signed bit

(D) Unsigned bit

Answer: B

7. An address in main memory is called

(A) Physical address

(B) Logical address

(C) Memory address

(D) Word address

Answer: A

8. In which addressing mode the operand is given explicitly in the instruction

(A) Absolute.

(B) Immediate .

(C) Indirect.

(D) Direct.

Answer: B

9. Data hazards occur when ……

A) Greater performance loss

B) Pipeline changes the order of read/write access to operands

C) Some functional unit is not fully pipelined

D) Machine size is limited

Ans. B

10. Which of the following registers is used to keep track of address of the memory location where the next instruction is located?

A. Memory Address Register

B. Memory Data Register

C. Instruction Register

D. Program Register

Ans. D

11. A complete microcomputer system consists of

A) microprocessor

B) memory

C) peripheral equipment

D) all of above

Ans. D

12. CPU does not perform the operation ……

A) data transfer

B) logic operation

C) arithmetic operation

D) all of the above

Ans. A

13. Assembly language

(A) uses alphabetic codes in place of binary numbers used in machine language

(B) is the easiest language to write programs

(C) need not be translated into machine language

(D) None of these

Answer: A

14. What characteristic of RAM memory makes it not suitable for permanent storage?

(A) too slow

(B) unreliable

(C) it is volatile

(D) too bulky

Answer: C

15. The average time required to reach a storage location in memory and obtain its contents is called the

(A) seek time

(B) turnaround time

(C) access time

(D) transfer time

Answer: C

16. The idea of cache memory is based

(A) on the property of locality of reference

(B) on the heuristic 90-10 rule

(C) on the fact that references generally tend to cluster

(D) all of the above

Answer: A

17. The addressing mode used in an instruction of the form ADD X Y, is

(A) Absolute

(B) indirect

(C) index

(D) none of these

Answer: C

18. Generally Dynamic RAM is used as main memory in a computer system as it

(A) Consumes less power

(B) has higher speed

(C) has lower cell density

(D) needs refreshing circuitary

Answer: B

19. A collection of lines that connects several devices is called …….

A) bus

B) peripheral connection wires

C) Both a and b

D) internal wires

Ans. A

20.Which of the following memories must be refreshed many times per second?

a. Static RAM

b. Dynamic RAM

c. EPROM

d. ROM

e. None of these

ans. Static RAM

21. A memory buffer used to accommodate a speed differential is called

a) stack pointer

b) cache

c) accumulator

d) disk buffer

Answer:b.

22.Which one of the following is the address generated by CPU?

a) physical address

b) absolute address

c) logical address

d) none of the mentioned

Answer:c.

23. Write Through technique is used in which memory for updating the data

(A) Virtual memory

(B) Main memory

(C) Auxiliary memory

(D) Cache memory

Answer: D

24. Logic X-OR operation of (4ACO) H & (B53F) H results

(A) AACB

(B) 0000

(C) FFFF

(D) ABCD

Answer: C

25. When CPU is executing a Program that is part of the Operating System, it is said to be in

(A) Interrupt mode

(B) System mode

(C) Half mode

(D) Simplex mode

Answer: B

26. An n-bit microprocessor has

(A) n-bit program counter

(B) n-bit address register

(C) n-bit ALU

(D) n-bit instruction register

Answer: D

26. Cache memory works on the principle of

(A) Locality of data

(B) Locality of memory

(C) Locality of reference

(D) Locality of reference & memory

Answer: C

27. The main memory in a Personal Computer (PC) is made of

(A) cache memory.

(B) static RAM

(C) Dynamic Ram

(D) both (A) and (B) .

Ans: D

28. In computers, subtraction is carried out generally by

(A) 1’s complement method

(B) 2’s complement method

(C) signed magnitude method

(D) BCD subtraction method

Answer: B

28. _____ register keeps tracks of the instructions stored in program stored in memory.

(A) AR (Address Register)

(B) XR (Index Register)

(C) PC (Program Counter)

(D) AC (Accumulator)

Answer: C

29. Memory unit accessed by content is called

(A) Read only memory

(B) Programmable Memory

(C) Virtual Memory

(D) Associative Memory

Answer: D

30. The time interval between adjacent bits is called the

(A) Word-time

(B) Bit-time

(C) Turn around time

(D) Slice time

Answer: B

31. The time interval between adjacent bits is called the

(A) Word-time

(B) Bit-time

(C) Turn around time

(D) Slice time

Answer: B

32. A group of bits that tell the computer to perform a specific operation is known as

(A) Instruction code

(B) Micro-operation

(C) Accumulator

(D) Register

Answer: A

33. A binary digit is called a

(A) Bit

(B) Byte

(C) Number

(D) Character

Ans: A

34. The operation executed on data stored in registers is called

(A) Macro-operation

(B) Micro-operation

(C) Bit-operation

(D) Byte-operation

Answer: B

35. Self-contained sequence of instructions that performs a given computational task is called

(A) Function

(B) Procedure

(C) Subroutine

(D) Routine

Answer: A

36. An interface that provides a method for transferring binary information between internal storage and external devices is called

(A) I/O interface

(B) Input interface

(C) Output interface

(D) I/O bus

Answer: A

37. An address in main memory is called

(A) Physical address

(B) Logical address

(C) Memory address

(D) Word address

Answer: A

38. The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called

(A) Data transfer instructions.

(B) Program control instructions.

(C) Input-output instructions.

(D) Logical instructions.

Answer: A

39. A register capable of shifting its binary information either to the right or the left is called a

(A) parallel register.

(B) serial register.

(C) shift register.

(D) storage register.

Answer: C

40. What is the content of Stack Pointer (SP)?

(A) Address of the current instruction

(B) Address of the next instruction

(C) Address of the top element of the stack

(D) Size of the stack.

Answer: C

41. Which of the following is a main memory

(A) Secondary memory.

(B) Auxiliary memory.

(C) Cache memory.

(D) Virtual memory.

Answer: C

42. When necessary, the results are transferred from the CPU to main memory by

(A) I/O devices.

(B) CPU.

(C) shift registers.

(D) none of these.

Answer: C

43. Memory unit accessed by content is called_____.

A. Read only memory

B. Programmable Memory

C. Virtual Memory

D. Associative Memory

Answer: D

44. _____ register keeps tracks of the instructions stored in program stored in memory.

A. AR (Address Register)

B. XR (Index Register)

C. PC (Program Counter)

D. AC (Accumulator)

Answer: C

45. The access time of memory is …… the time required for performing any single CPU operation.
A. Longer than

B Shorter than

C Negligible than

D Same as

Answer: A

46. The circuit converting binary data in to decimal is

(A) Encoder

(B) Multiplexer

(C) Decoder

(D) Code converter

Answer: D

47. A three input NOR gate gives logic high output only when

(A) one input is high

(B) one input is low

(C) two input are low

(D) all input are high

Ans: D

48. n bits in operation code imply that there are _____ possible distinct operators

(A) 2n

(B) 2n

(C) n/2

(D) n2

Ans: B

49. 'Aging registers' are

(A) Counters which indicate how long ago their associated pages have been referenced.

(B) Registers which keep track of when the program was last accessed.

(C) Counters to keep track of last accessed instruction.

(D) Counters to keep track of the latest data structures referred.

Ans: A

50 The instruction 'ORG O' is a

(A) Machine Instruction.

(B) Pseudo instruction.

(C) High level instruction.

(D) Memory instruction.

Ans: B

51 A microprogram sequencer

(A) generates the address of next micro instruction to be executed.

(B) generates the control signals to execute a microinstruction.

(C) sequentially averages all microinstructions in the control memory.

(D) enables the efficient handling of a micro program subroutine.

Ans: A

52 The operation executed on data stored in registers is called

(A) Macro-operation

(B) Micro-operation

(C) Bit-operation

(D) Byte-operation

Ans: B

53 An interface that provides a method for transferring binary information between internal storage and external devices is called

(A) I/O interface

(B) Input interface

(C) Output interface

(D) I/O bus

Ans: A

MULTIPLE CHOICE QUESTIONS - COA

1. In Reverse Polish notation, expression A*B+C*D is written as
(A) AB*CD*+ (B) A*BCD*+ (C) AB*CD+* (D) A*B*CD+
Ans: A

2. SIMD represents an organization that _____.
(A) refers to a computer system capable of processing several programs at the same time.
(B) represents organization of single computer containing a control unit, processor unit and a memory unit.
(C) includes many processing units under the supervision of a common control unit
(D) none of the above.
Ans: C

3. Floating point representation is used to store
(A) Boolean values (B) whole numbers (C) real integers (D) integers
Ans: C

4. Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus?
(A) 1 Megabyte/sec (B) 4 Megabytes/sec (C) 8 Megabytes/sec (D) 2 Megabytes/sec
Ans: D

5. Assembly language
(A) uses alphabetic codes in place of binary numbers used in machine language
(B) is the easiest language to write programs
(C) need not be translated into machine language
(D) None of these
Ans: A

6. In computers, subtraction is generally carried out by
(A) 9's complement (B) 10's complement (C) 1's complement (D) 2's complement **Ans:** D

7. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to (A) the time its takes for the platter to make a full rotation
(B) the time it takes for the read-write head to move into position over the appropriate track
(C) the time it takes for the platter to rotate the correct sector under the head
(D) none of the above **Ans:** A

8. What characteristic of RAM memory makes it not suitable for permanent storage?
(A) too slow (B) unreliable (C) it is volatile (D) too bulky **Ans:** C

9. Computers use addressing mode techniques for _____.
(A) giving programming versatility to the user by providing facilities as pointers to memory counters for loop control
(B) to reduce no. of bits in the field of instruction
(C) specifying rules for modifying or interpreting address field of the instruction
(D) All the above
Ans: D

10. The circuit used to store one bit of data is known as
(A) Register (B) Encoder (C) Decoder (D) Flip Flop
Ans: D

11. (2FAOC) 16 is equivalent to
(A) (195 084) 10 (B) (001011111010 0000 1100) 2 (C) Both (A) and (B) (D) None of these
Ans: B

12. The average time required to reach a storage location in memory and obtain its contents is called the
(A) seek time (B) turnaround time (C) access time (D) transfer time
Ans: C

13. Which of the following is not a weighted code?
(A) Decimal Number system (B) Excess 3-cod
(C) Binary number System (D) None of these
Ans: B

14. The idea of cache memory is based
(A) on the property of locality of reference (B) on the heuristic 90-10 rule
(C) on the fact that references generally tend to cluster (D) all of the above
Ans: A

15. Which of the following is lowest in memory hierarchy? (A) Cache memory (B) Secondary memory (C) Registers (D) RAM (E) None of these
Ans (B)

16. The addressing mode used in an instruction of the form ADD X Y, is
(A) Absolute (B) indirect (C) index (D) none of these
Ans: C

17. If memory access takes 20 ns with cache and 110 ns with out it, then the ratio (cache uses a 10 ns memory) is
(A) 93% (B) 90% (C) 88% (D) 87%
Ans: B

18. In a memory-mapped I/O system, which of the following will not be there?
(A) LDA (B) IN (C) ADD (D) OUT

Ans: A

19. In a vectored interrupt.
(A) the branch address is assigned to a fixed location in memory.
(B) the interrupting source supplies the branch information to the processor through an interrupt vector.
(C) the branch address is obtained from a register in the processor
(D) none of the above
Ans: B

20. Von Neumann architecture is
(A) SISD (B) SIMD (C) MIMD (D) MISD
Ans: A

21. The circuit used to store one bit of data is known as
(A) Encoder (B) OR gate (C) Flip Flop (D) Decoder
Ans: C

22. Cache memory acts between
(A) CPU and RAM (B) RAM and ROM (C) CPU and Hard Disk (D) None of these
Ans: A

23. Write Through technique is used in which memory for updating the data
(A) Virtual memory (B) Main memory
(C) Auxiliary memory (D) Cache memory
Ans: D

24. Generally Dynamic RAM is used as main memory in a computer system as it
(A) Consumes less power (B) has higher speed
(C) has lower cell density (D) needs refreshing circuitary
Ans: B

25. In signed-magnitude binary division, if the dividend is (11100) 2 and divisor is (10011) 2 then the result is
(A) (00100) 2 (B) (10100) 2 (C) (11001) 2 (D) (01100) 2
Ans: B

26. Virtual memory consists of
(A) Static RAM (B) Dynamic RAM
(C) Magnetic memory (D) None of these
Ans: A

27. In a program using subroutine call instruction, it is necessary
(A) initialise program counter (B) Clear the accumulator
(C) Reset the microprocessor (D) Clear the instruction register
Ans: D

28. A Stack-organised Computer uses instruction of
(A) Indirect addressing (B) Two-addressing (C) Zero addressing (D) Index addressing
Ans: C

29. If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be
(A) 11 bits (B) 21 bits (C) 16 bits (D) 20 bits
Ans: C

30 A-Flip Flop can be converted into T-Flip Flop by using additional logic circuit
(A) n TQD =• (B) T D = (C) D = T . Q n (D) n TQD =⊕
Ans: D

31. Logic X-OR operation of (4ACO) H & (B53F) H results
(A) AACB (B) 0000 (C) FFFF (D) ABCD
Ans: C

32. When CPU is executing a Program that is part of the Operating System, it is said to be in (A) Interrupt mode (B) System mode (C) Half mode (D) Simplex mode
Ans: B

33. An n-bit microprocessor has
(A) n-bit program counter (B) n-bit address register
(C) n-bit ALU (D) n-bit instruction register
Ans: D

34. Cache memory works on the principle of
(A) Locality of data (B) Locality of memory
(C) Locality of reference (D) Locality of reference & memory
Ans: C

35. The main memory in a Personal Computer (PC) is made of
(A) cache memory. (B) static RAM
(C) Dynamic Ram (D) both (A) and (B) .
Ans: D

36. In computers, subtraction is carried out generally by
(A) 1's complement method (B) 2's complement method
(C) signed magnitude method (D) BCD subtraction method
Ans: B

37. PSW is saved in stack when there is a
(A) interrupt recognised (B) execution of RST instruction
(C) Execution of CALL instruction (D) All of these
Ans: A

38. The multiplicand register & multiplier register of a hardware circuit implementing booth's algorithm have (11101) & (1100). The result shall be
(A) (812) 10 (B) (-12) 10 (C) (12) 10 (D) (-812) 10
Ans: A

39. The circuit converting binary data in to decimal is
(A) Encoder (B) Multiplexer (C) Decoder (D) Code converter
Ans: D

40. A three input NOR gate gives logic high output only when
(A) one input is high (B) one input is low
(C) two input are low (D) all input are high
Ans: D

41. n bits in operation code imply that there are _____ possible distinct operators (A) 2n (B) 2n (C) n/2 (D) n2
Ans: B

42. _____ register keeps tracks of the instructions stored in program stored in memory.
(A) AR (Address Register) (B) XR (Index Register)
(C) PC (Program Counter) (D) AC (Accumulator)
Ans: C

43. Memory unit accessed by content is called
(A) Read only memory (B) Programmable Memory
(C) Virtual Memory (D) Associative Memory
Ans: D

44. 'Aging registers' are
(A) Counters which indicate how long ago their associated pages have been referenced.
(B) Registers which keep track of when the program was last accessed.
(C) Counters to keep track of last accessed instruction.
(D) Counters to keep track of the latest data structures referred.
Ans: A

45 The instruction 'ORG O' is a
(A) Machine Instruction. (B) Pseudo instruction.
(C) High level instruction. (D) Memory instruction.
Ans: B

46 Translation from symbolic program into Binary is done in
(A) Two passes. (B) Directly (C) Three passes. (D) Four passes.
Ans: A

47 A floating point number that has a O in the MSB of mantissa is said to have

(A) Overflow (B) Underflow (C) Important number (D) Undefined
Ans: B

48 The BSA instruction is
(A) Branch and store accumulator (B) Branch and save return address
(C) Branch and shift address (D) Branch and show accumulator
Ans: B

49 State whether True or False.
(i) Arithmetic operations with fixed point numbers take longer time for execution as compared to with floating point numbers.
Ans: True.

(ii) An arithmetic shift left multiplies a signed binary number by 2. **Ans: False.**

50 Logic gates with a set of input and outputs is arrangement of
(A) Combinational circuit (B) Logic circuit (C) Design circuits (D) Register
Ans: A

51. MIMD stands for
(A) Multiple instruction multiple data (B) Multiple instruction memory data
(C) Memory instruction multiple data (D) Multiple information memory data
Ans: A

52 A k-bit field can specify any one of
(A) 3k registers (B) 2k registers
(C) K2 registers (D) K3 registers
Ans: B

53 The time interval between adjacent bits is called the
(A) Word-time (B) Bit-time (C) Turn around time (D) Slice time
Ans: B

54 A group of bits that tell the computer to perform a specific operation is known as
(A) Instruction code (B) Micro-operation (C) Accumulator (D) Register
Ans: A

55 The load instruction is mostly used to designate a transfer from memory to a processor register known as
(A) Accumulator (B) Instruction Register
(C) Program counter (D) Memory address Register
Ans: A

56 The communication between the components in a microcomputer takes place via the address and
(A) I/O bus (B) Data bus (C) Address bus (D) Control lines

Ans: B

57 An instruction pipeline can be implemented by means of
(A) LIFO buffer (B) FIFO buffer (C) Stack (D) None of the above
Ans: B

58 Data input command is just the opposite of a
(A) Test command (B) Control command (C) Data output (D) Data channel
Ans: C

59 A microprogram sequencer
(A) generates the address of next micro instruction to be executed.
(B) generates the control signals to execute a microinstruction.
(C) sequentially averages all microinstructions in the control memory.
(D) enables the efficient handling of a micro program subroutine.
Ans: A

60 . A binary digit is called a
(A) Bit (B) Byte (C) Number (D) Character
Ans: A

61 A flip-flop is a binary cell capable of storing information of
(A) One bit (B) Byte (C) Zero bit (D) Eight bit
Ans: A

62 The operation executed on data stored in registers is called
(A) Macro-operation (B) Micro-operation
(C) Bit-operation (D) Byte-operation
Ans: B

63 MRI indicates
(A) Memory Reference Information. (B) Memory Reference Instruction.
(C) Memory Registers Instruction. (D) Memory Register information
Ans: B

64 Self-contained sequence of instructions that performs a given computational task is called
(A) Function (B) Procedure (C) Subroutine (D) Routine
Ans: A

65 Microinstructions are stored in control memory groups, with each group specifying a (A) Routine
(B) Subroutine (C) Vector (D) Address
Ans: A

66 An interface that provides a method for transferring binary information between internal storage and external devices is called
(A) I/O interface (B) Input interface (C) Output interface (D) I/O bus

Ans: A

67 Status bit is also called
(A) Binary bit (B) Flag bit (C) Signed bit (D) Unsigned bit
Ans: B

68 An address in main memory is called
(A) Physical address (B) Logical address (C) Memory address (D) Word address
Ans: A

69 If the value V(x) of the target operand is contained in the address field itself, the addressing mode is
(A) immediate. (B) direct. (C) indirect. (D) implied.
Ans: B

70 can be represented in a signed magnitude format and in a 1's complement format as (A) 111011 & 100100 (B) 100100 & 111011
(C) 011011 & 100100 (D) 100100 & 011011
Ans: A