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CSE 240A – Branch Predictor Project Submission

Custom Branch Predictor:

A tournament predictor: Gshare and local predictor and a chooser to choose between them was used as custom branch predictor.

- It used 3bit counters for all the BHTs (gshare, local and chooser) to increase the accuracy.
- All the BHTs (gshare, local and chooser) are 3 bits per element – done using malloc – to use reduced hardware
- PHT for local is 11 bits equal to lhistoryBits – to reduce hardware
- The chooser was accessed/indexed by (pc XOR ghr), same as gshare indexing scheme – again to increase accuracy and reduce aliasing for chooser.
- Gshare is given more bits than local branch predictor, as gshare performs better than local predictor
    - Gshare : gHistoryBits = 13 bits
    - Local : lhistoryBits = 11, pcIndexBits = 11 bits

Papers referred:

1. Kessler, R. E. (1999). "The Alpha 21264 Microprocessor". IEEE Micro,1999
2. http://mixteco.utm.mx/~merg/AC/pdfs/alpha_21264.pdf
3. S. McFarling. “Combining Branch Predictors”. TN 36,Compaq Computer Corporation Western Research Laboratory, June 1993
4. http://courses.cs.tamu.edu/ejkim/614/tournament_predictors.pdf
5. Referred to Dean Tullsen’s 240A slides, Onur Multu’s CMU Comp Arch slides, Udacity HPCA Course