CSE 237D: SoC Security
Milestones Report

Mahima Rathore | Richa Pallavi

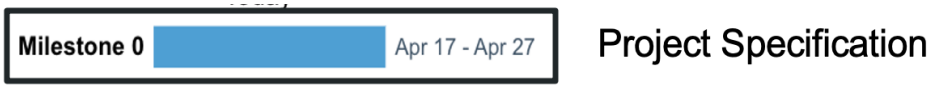
Milestones & Deliverables:

Ownership: All the milestones are joint milestones. Both the team members will be working together on all of them. This was done to encourage better discussion, brainstorming and debugging for various design code/specifications.

Following are the milestones and future goals for this project:

Milestone 0 -

A complete plan for the project SoC Security after understanding the past developments within the project. Requires a detailed discussion with project leads Francesco & Armita.



Weekly Milestones:

- Understood the current progress of the SoC progress - meeting with project leads.
- Read documentation on firmware security with security policies, AXI protocol & development of fair interconnect for AXI.
- Had a detailed discussion with team leader (Francesco) to figure out where we best fit in keeping our past experience in mind.
- Prepared a quarter-long plan for this project and got it reviewed by the project lead.

Deliverable: Project Specification Document

Due on: 04/23/2020, Thursday

Progress: Completed

Milestone 1 -

Demonstrating working simulation & successful build of the current SoC - CEP Architecture.

Understanding & Setting up CEP SoC

Weekly Milestones:

- Spent time to understand the AXI protocol (AXI4 full & lite standard interface).
- Spent time understanding the CEP Architecture and module hierarchy within it.
- Faced some issues related to software and platform required for this project (specifically w.r.t. fabricant server & 'sudo' permissions) - couldn't resolve them
  Workaround:
  - Migrated some files (immediately required for developing AXI Machines) to our local machines.
  - Used ModelSim on our systems for their compilation. But without any testbench for this design architecture correct compilation or simulation couldn't be done.
- Kept the build of the CEP architecture (design + RISC-V toolchain) on hold for now.

Deliverable:

- Due to unsuccessful build of CEP design on fabricant server, there are no results to display.
- But with the help of the workaround, further delay was avoided for future design development.

Due on: 05/05/2020, Tuesday

Progress: Completed with a workaround for build

Milestone 2 -

Development & verification of AXI Masters & complete test-planning for it.

Developing & Integrating AXI Master

Weekly Milestones:

- Set up project web presence for better information exchange.
  https://github.com/mr103/SoC-Security
- Spent time to understand the AXI Master skeleton code from Xilinx.
- Integrated an AXI full master machine with the CEP hardware accelerator (md5).
- Developed a testbench to emulate an AXI slave to verify this integrated module - using the burst feature allowed by the AXI standard.

- Developed internal registers & a register access interface within the hardware accelerator, accessible to the AXI master.

Deliverable: Report presenting code-design & details of the developed module.

- Report_milestone2

Due on: 05/12/2020, Tuesday

Progress: Completed.

Milestone 3 -

Development & verification of AXI Interconnect & complete test-planning for it.

Weekly Milestones:

PART A

- Understand the AXI interconnect code from Xilinx to integrate with CEP.
- Develop and integrate AXI Interconnect with the hardware accelerator core.
- Make this interconnect configurable for 3 slave interfaces & 1 master interface to handshake with hardware accelerators and scratchpad respectively.

PART B

- Design and Implement an access control mechanism on the AXI Interconnect (Multi-memory region), for the hardware accelerators to access just a limited portion of the memory.

PART C

- Testbench development to verify the interconnect handshake and register access feature.

Deliverable: Report presenting code-design & details of the developed module.

Due on: 05/21/2020, Thursday

Progress: Ongoing - Understanding the Data AXI Interconnect design specifications for coding.

Milestone 4 -

Development and verification of AXI Slaves & complete test-planning for it.

Weekly Milestones:

- Understand the AXI Slave module w.r.t. the interface it communicates within the CEP SoC and its proposed functionality.
- Development of AXI slave and handshake with AXI interconnect master interface.
- Integrate a slave configuration port and registers to the AXI Interconnect to set the memory boundaries.
- Develop testbench to verify this handshaking.

Deliverable: Report presenting code-design & details of the developed module.

Due on: 05/29/2020, Friday

Progress: Not started yet

Milestone 5/ Future Goal-

Integration of AXI Modules developed, with the CEP Architecture.

Weekly Milestones:

- Complete verification from Master (Hardware accelerator) → Interconnect → Slave(scratchpad) handshake.
    - Develop a verification environment for the AXI Modules with testbench, drivers and monitors.
- Complete the verification by running the test cases and fixing design bugs.
- **Future Goals -- If time permits, we can go ahead integrating our AXI machines with CEP SoC and verify it.**

Deliverable: Report presenting the verification summary.

Due on: 06/05/2020, Friday

Progress: Not started yet

Milestone 6 -

Develop a final report for the project.

Weekly Milestones:

- Develop the final report for this project explaining in detail each milestone accomplished, challenges faced and how they were resolved.

Deliverable: Final Report

Due on: 06/10/2020, Wednesday

Progress: Not started yet

Grading:

Assigned grades for milestones in mid quarter:

Grade	Milestones
B+	0, 1, 2
A-	0, 1, 2, 3(part A)
A	0, 1, 2, 3(part B & C)
A+	0, 1, 2, 3, 4