Hardware Test Sheet

MSc in Digital Systems Engineering
Department of Electronics
University of York

Group Project

Contents

1 Test #1

2 Tester name: Matt Reynolds

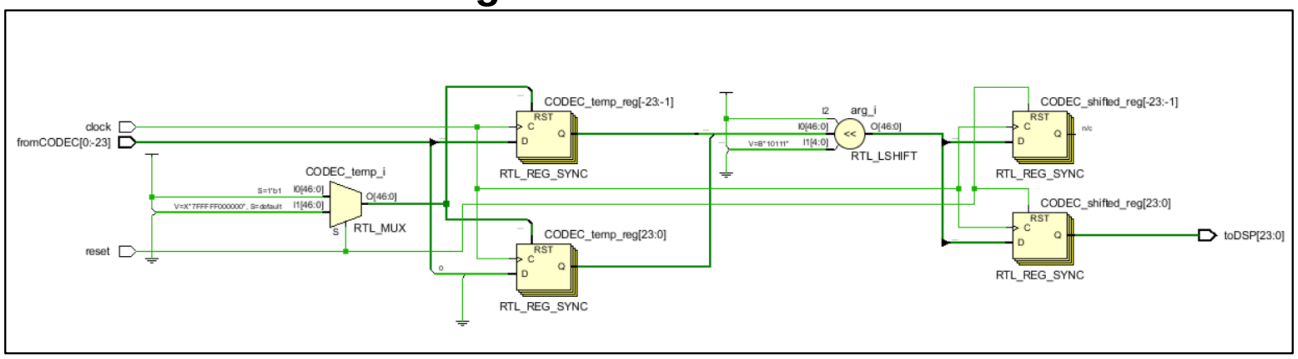
3 Test date start: 29/06/2020

4 Test date finish: 01/07/2020

5 UUT typology (VHDL entity / ~~custom IP / subsystem~~)

6 UUT name: fixedPoint_to_signed

7 Hardware block design screenshot



8 Objective of test

1. Verify converted output data is correct across the full value range.
2. Verify the signed information is maintained.

The following test is ran in compliance with the V-model testing strategy

9 Testbench description / test strategy overview:

The input samples to the UUT are in the format S1.23 fixed point notation. The output of the UUT uses signed(23 downto 0) notation. The UUT shifts the input samples left by 2^{23} to remove the fractional part and then converts this to signed.

The test uses a single process to provide test data and stimulus to the UUT and a separate process to verify the results. Input data is provided by a .dat file in the sim directory. This file has been generated using a custom C programme. It contains a list of floating point values (double) between the values of -1 and 1, increasing by 0.002 each time. This creates a dataset of 1000 samples, spread across the full input range.

The verify process tests the output data using an ASSERT statement and reports an error message if it is incorrect. As the UUT has a clock cycle delay between input and output, the verify process accounts for this using two variables, to delay the samples being checked by the assert statement.

10 Test results:

An error message is printed during setup, as there are a number of clock cycles which occur prior to the input data being activated. However, as indicated by the TCL console output below, the output and input data are still equivalent. The issue is that initialising the VHDL type *sfixed* to zero requires extra processing, which is not required here. Therefore, the testbench values receive 'U' while the circuit is reset and initialised. Once input data is supplied via the .dat file, this problem is removed.

> *Time: 160 ns Iteration: 0 Process: /fixedConvert_TB/verify_p File: C:/Users/Matt/Documents/Group_Project/VivadoProjects/Distortion_Proj_1/Distortion_Proj_1.srcs/sim_1/new/fixedConvert_TB.vhd*
> *Warning: Incorrect data conversion*
> *Output: 0*
> *Input: 0*

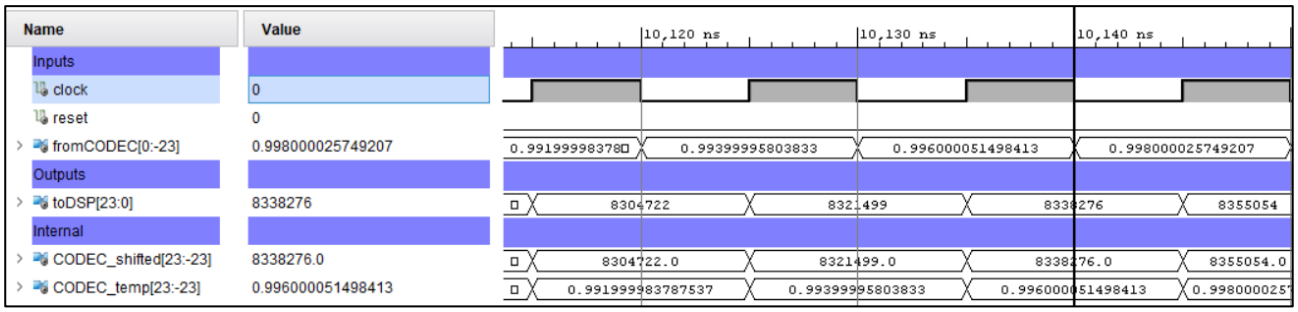
It then follows that all values pass the assert statement, once the test begins.

> *Time: 170 ns Iteration: 0 Process: /fixedConvert_TB/verify_p File: C:/Users/Matt/Documents/Group_Project/VivadoProjects/Distortion_Proj_1/Distortion_Proj_1.srcs/sim_1/new/fixedConvert_TB.vhd*
> *Note: +++ Correct output +++*
>
> *Time: 180 ns Iteration: 0 Process: /fixedConvert_TB/verify_p File: C:/Users/Matt/Documents/Group_Project/VivadoProjects/Distortion_Proj_1/Distortion_Proj_1.srcs/sim_1/new/fixedConvert_TB.vhd*
> *Note: +++ Correct output +++*
>
> *…*
>
> *Time: 10150 ns Iteration: 0 Process: /fixedConvert_TB/verify_p File: C:/Users/Matt/Documents/Group_Project/VivadoProjects/Distortion_Proj_1/Distortion_Proj_1.srcs/sim_1/new/fixedConvert_TB.vhd*
> *Note: +++ Correct output +++*

There is one instance where a value is truncated. This is only a result of the VHDL REPORT statement. It is required that values are reported as INTEGER'IMAGE, this method only supports values of a certain size.

> *Time: 10140 ns Iteration: 0 Process: /fixedConvert_TB/verify_p File: C:/Users/Matt/Documents/Group_Project/VivadoProjects/Distortion_Proj_1/Distortion_Proj_1.srcs/sim_1/new/fixedConvert_TB.vhd*
> *Warning: :fixed_pkg:TO_SFIXED(REAL): vector truncated*

I have verified the samples at this time (10140 ns) by hand, and can confirm that they are correct.



11 Observations:

There is an internal signal (CODEC_temp) which loses the signed information. Any future user of this entity, should note that this is by design and does not produce incorrect results at the output. It is related to the temporary transfer of data before shifting and the signed information is preserved at the output.

12 Grade (pass/fail): Pass

13 Hardware manager approval signature

01/07/2020	18/08/2020
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