Hardware Test Sheet

MSc in Digital Systems Engineering
Department of Electronics
University of York

Group Project

Contents

1 Test #1

2 Tester name: Matt Reynolds

3 Test date start: 29/06/2020

4 Test date finish: 03/07/2020

5 UUT typology (~~VHDL entity / custom IP~~ / subsystem)

6 UUT name: distortion_TopLevel

7 Hardware block design screenshot

Figure 1 gives an RTL overview of the implemented distortion effect. Inside the done_control component are two counters, one which is used when the effect is enabled and one for when it is disabled. The hardClipping component contains the clipping circuit, overflow register, and the LED indicator control.

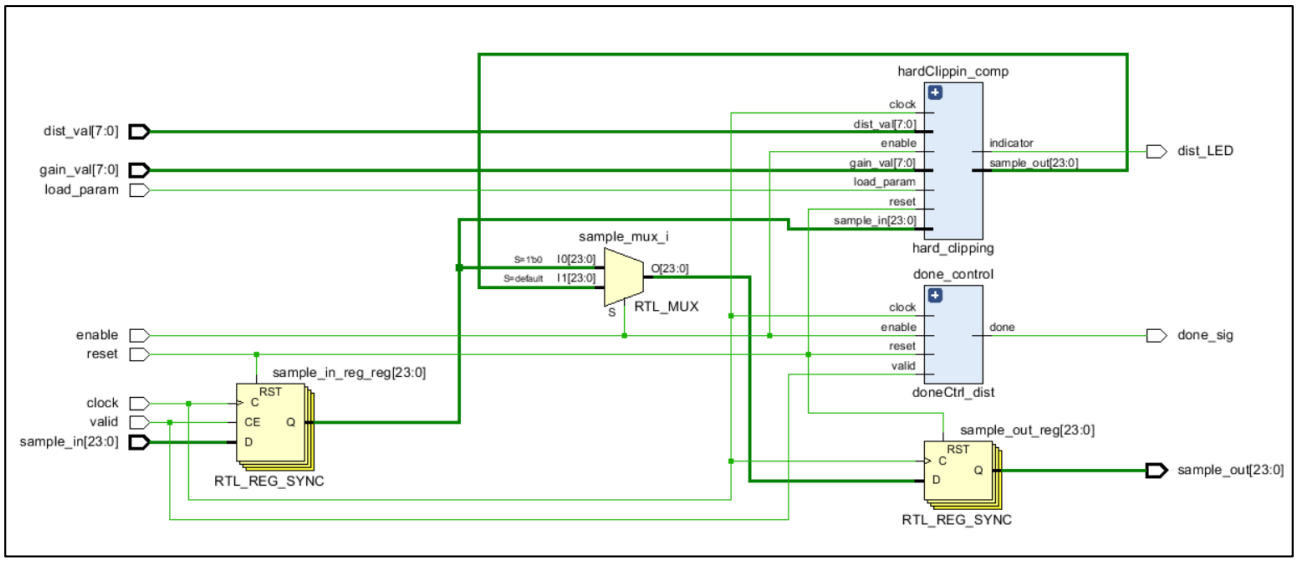

Figure 1 - RTL Schematic of Distortion

8 Objective of test

1. Create an observable set of test data which can be plotted
2. Identify correct linear response to the gain stage
3. Identify circuit resilience to data overflow
4. Test for appropriate clipping values (numerically)

The following test is ran in compliance with the V-model testing strategy

9 Testbench description / test strategy overview:

The test for the distortion entity is aimed at producing a clear output waveform which will allow the tester to easily identify correct operation. Although it is possible to test on a purely numerical basis, the use of graphical data when testing for wave behaviour is extremely useful.

Observe correct linear response to gain control: Gain is increased to max at a rate of one increment per two-wave periods. It is then decreased to its minimum value at the same rate. The output wave should show a linear increase and decrease, respectively when plotted.

Test for data overflow: Gain is increased to max to identify if the output signal can be driven into an overflow state, whereby the multiplier output is incorrect. Easily identified, by non-conforming samples displayed in the plotted data. When sample points are connected with approximation curves, these incorrect results will distort the output waveform in an obvious way.

Test for appropriate clipping values: The distortion is set to max to observe that the counter is functioning correctly. Then it is reduced to half so that the introduction of clipping can be observed as the gain is once again increased. As gain is increased past the point of clipping, the top of the wave form should become wider and flatter (squarer).

NOTE: This test strategy relies on two-parts: the VHDL testbench (written here) and an audio test. While this TB can test the circuit functionality and verify correct implementation it lacks the ability for the sound to be tested subjectively. The audio output must be tested by a listener in the system it is design to operate in.

10 Test results:

Figure 2 shows that clipping occurs on the lowest distortion value (control = 1) when the gain is increased up to 17, for a relatively small input signal. This shows that the gain stage provides a good range of amplification which is useful to the user and that the effects of clipping can be heard even at lower volumes. This is seen again as distortion is reduced to half (10) toward the end of the test and clipping is introduced at a much lower gain value.

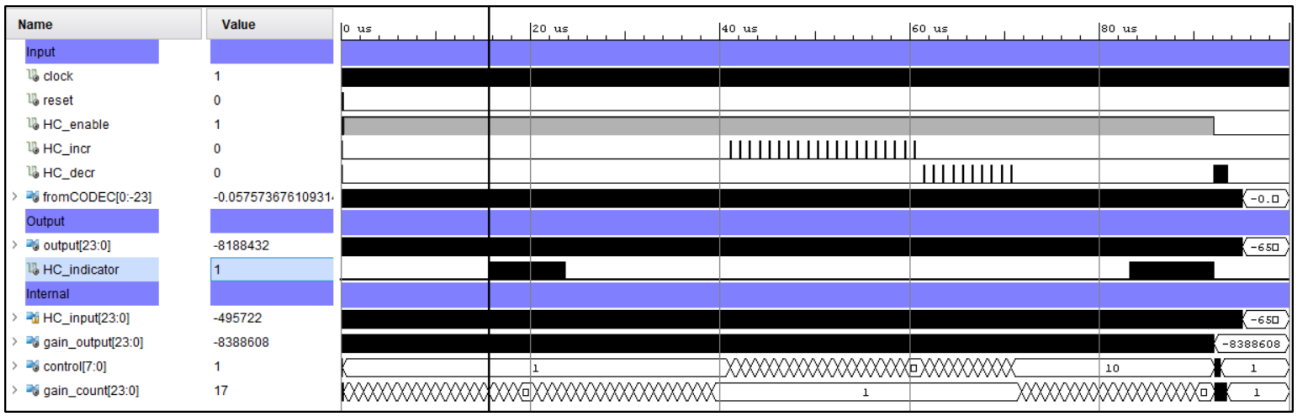

Figure 2 - Vivado Waveform Overview

The gain and distortion control counters can also be observed as working correctly from this data and are seen more clearly in Figure 3.

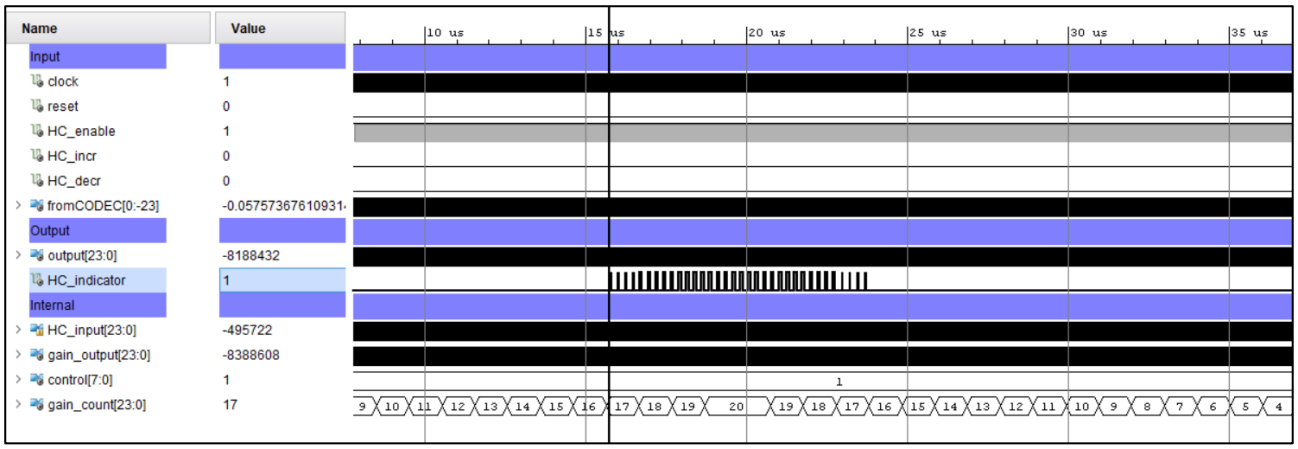

Figure 3 - Gain counter and HC_indicator

Figure 4 clearly shows the linear gain response at the output as the gain stage controls are increased to max and decreased again. Notice that there is a flat part to the output waveform, near the centre. This is the introduction of clipping in the circuit and is the correct functionality.

Frequency and phase are preserved.

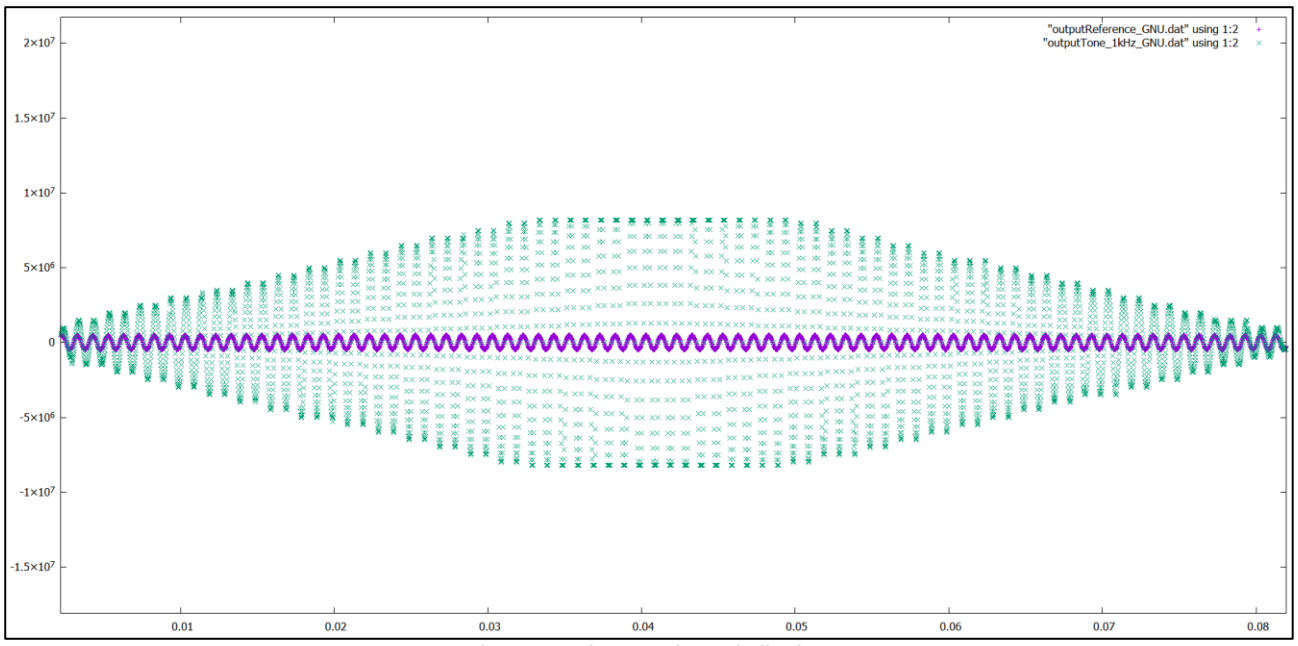

Figure 4 - Linear gain and clipping

Figure 5 shows many interesting features of the circuit. First the matching of the input waveform, where the gain is reduced to one and no amplification occurs. Note also that at this level no distortion occurs, even though in the testbench the distortion control is set to max and reduced again. This is by design as it was felt that distortion on a signal this small would be too aggressive and not desirable to the user.

However, if during audio testing this appears to not be true, then this may be updated to allow earlier distortion. The circuit has been designed such that it is very easy to do this, by updating a single constant in the VHDL.

Second, the linear gain is once again observed. However, the distortion has been increased this time and clipping of the output signal occurs much earlier, producing a longer flat section.

Finally, the true bypass is verified, as enable is set low and the output immediately returns to match the input signal.

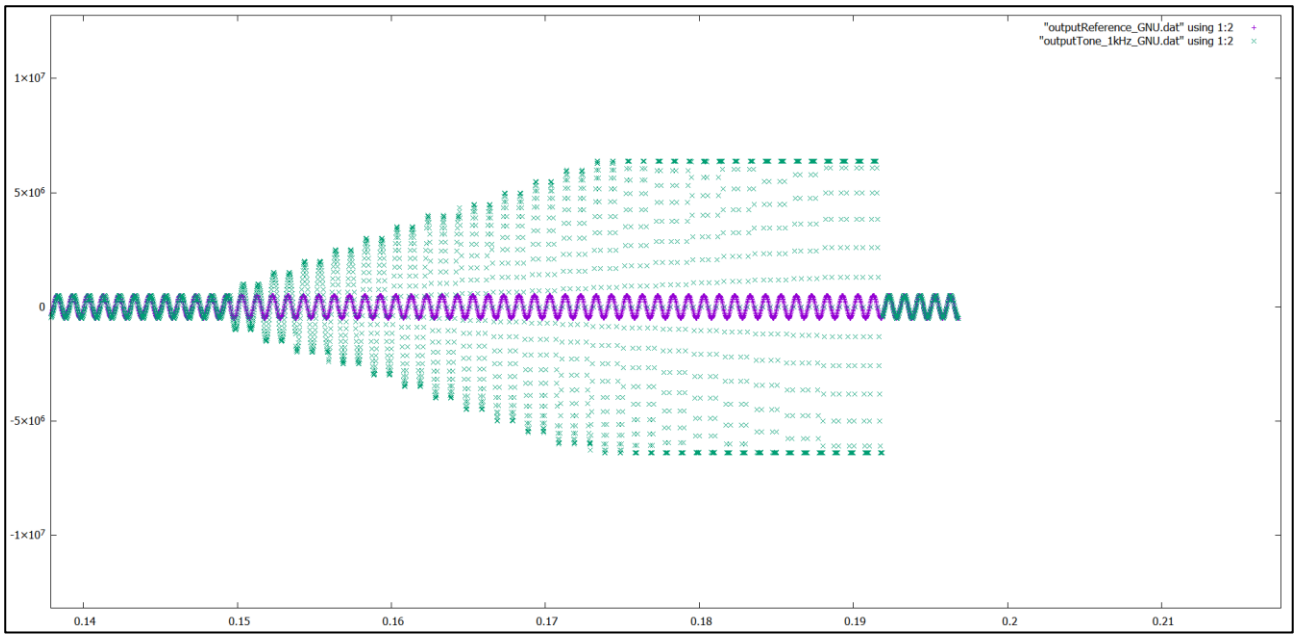

Figure 5 - Distortion output waveform

Figure 6 shows a more zoomed in version of the waveform. This shows that the wave period is the same is the input and that overflow is not occurring.

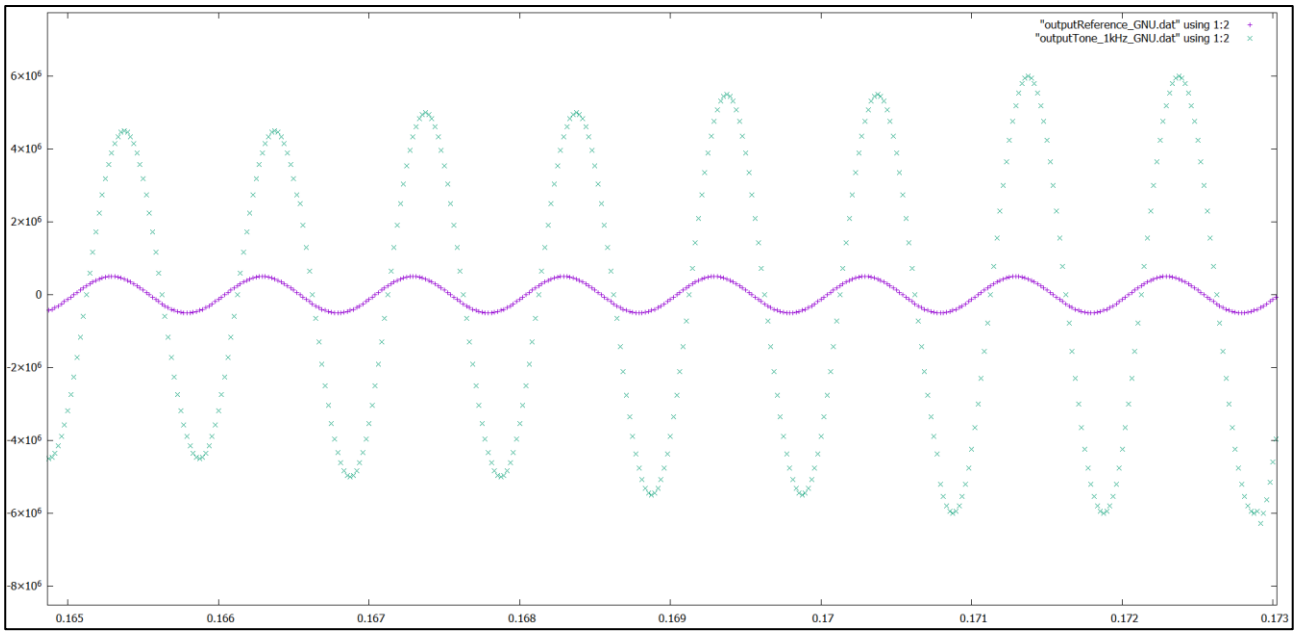

Figure 6 - Distortion output zoomed

11 Observations:

The clipping may need to be rescaled once an audio test has been carried out. However, the design is operating as intended and appears fit for purpose at this stage.

12 Grade (pass/fail): Pass

13 Approval signatures

Recoverable Signature

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Hardware Manager
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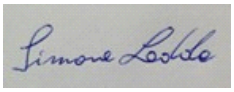
Recoverable Signature

X 

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