EE 705: VLSI DESIGN LAB

ASSIGNMENT-4 | Team: Design Dynamos

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Icache Memory:

Terminal screenshot:

```
[2025-03-24 00:38:47.356319] |=============================================================================|
[2025-03-24 00:38:47.374331] |=========                    OpenRAM v1.2.48                      =========|
[2025-03-24 00:38:47.377386] |=========                                                         =========|
[2025-03-24 00:38:47.380438] |=========              VLSI Design and Automation Lab             =========|
[2025-03-24 00:38:47.384494] |=========       Computer Science and Engineering Department       =========|
[2025-03-24 00:38:47.387795] |=========           University of California Santa Cruz           =========|
[2025-03-24 00:38:47.390847] |=========                                                         =========|
[2025-03-24 00:38:47.394044] |=========         Usage help: openram-user-group@ucsc.edu         =========|
[2025-03-24 00:38:47.397104] |=========       Development help: openram-dev-group@ucsc.edu       =========|
[2025-03-24 00:38:47.401784] |=========               See LICENSE for license info              =========|
[2025-03-24 00:38:47.404977] |=============================================================================|
[2025-03-24 00:38:47.408032] ** Start: 03/24/2025 00:38:47
[2025-03-24 00:38:47.411201] Technology: sky130
[2025-03-24 00:38:47.414471] Total size: 5120 bits
[2025-03-24 00:38:47.419117] Word size: 20
Words: 256
Banks: 1
[2025-03-24 00:38:47.422297] RW ports: 1
R-only ports: 1
W-only ports: 0
[2025-03-24 00:38:47.425381] DRC/LVS/PEX is only run on the top-level design to save run-time (inline_lvsdrc=True to do inline checking).
[2025-03-24 00:38:47.428512] Characterization is disabled (using analytical delay models) (analytical_delay=False to simulate).
[2025-03-24 00:38:47.434332] Only generating nominal corner timing.
[2025-03-24 00:38:47.437799] Words per row: None
[2025-03-24 00:38:47.440866] Output files are:
[2025-03-24 00:38:47.443894] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.lvs
[2025-03-24 00:38:47.446975] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.sp
[2025-03-24 00:38:47.451375] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.v
[2025-03-24 00:38:47.454409] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.lib
[2025-03-24 00:38:47.457422] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.py
[2025-03-24 00:38:47.460399] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.html
[2025-03-24 00:38:47.463466] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.log
[2025-03-24 00:38:47.468956] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.lef
[2025-03-24 00:38:47.472077] /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.gds
[2025-03-24 00:39:16.746831] ** Submodules: 29.1 seconds
[2025-03-24 00:39:16.811204] ** Placement: 0.1 seconds
[2025-03-21 16:06:11.280487] ** Routing: 1916.5 seconds
[2025-03-21 18:36:06.666895] ** Verification: 8995.3 seconds
[2025-03-21 18:36:06.672887] ** SRAM creation: 10932.9 seconds
[2025-03-21 18:36:06.676498] SP: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.sp
[2025-03-21 18:36:07.597518] ** Spice writing: 0.9 seconds
[2025-03-21 18:36:07.597648] DELAY: Writing stimulus...
[2025-03-21 18:36:08.610595] ** DELAY: 1.0 seconds
[2025-03-21 18:36:08.721252] GDS: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.gds
[2025-03-21 18:36:10.245983] ** GDS: 1.5 seconds
[2025-03-21 18:36:10.246270] LEF: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.lef
[2025-03-21 18:36:10.270898] ** LEF: 0.0 seconds
[2025-03-21 18:36:10.271000] LVS: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.lvs.sp
[2025-03-21 18:36:10.421675] ** LVS writing: 0.2 seconds
[2025-03-21 18:36:10.422051] LIB: Characterizing...
[2025-03-21 18:36:11.373709] ** Characterization: 1.0 seconds
[2025-03-21 18:36:11.374399] Config: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.py
[2025-03-21 18:36:11.374676] ** Config: 0.0 seconds
[2025-03-21 18:36:11.423257] Datasheet: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.html
[2025-03-21 18:36:11.429729] ** Datasheet: 0.1 seconds
[2025-03-21 18:36:11.429832] Verilog: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20/sky130_sram_1kbytes_1rw1r_20x256_20.v
[2025-03-21 18:36:11.430197] ** Verilog: 0.0 seconds
[2025-03-21 18:36:11.623390] [openram.globals/cleanup_paths]: Preserving temp directory: /tmp/openram_anubh_791_temp/
[2025-03-21 18:36:11.623559] ** End: 10937.9 seconds
```

Output Folder Content :

```
root@AnubhavPC:~# cd /mnt/d/Work/Tools/OpenRAM/
root@AnubhavPC:/mnt/d/Work/Tools/OpenRAM# cd riscv_icache/
root@AnubhavPC:/mnt/d/Work/Tools/OpenRAM/riscv_icache# cd sky130_sram_1kbytes_1rw1r_20x256_20/
root@AnubhavPC:/mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20# ls
datasheet.info      run_lvs.sh                                  sky130_sram_1kbytes_1rw1r_20x256_20.py
delay_meas.sp       setup.tcl                                   sky130_sram_1kbytes_1rw1r_20x256_20.sp
delay_stim.sp       sky130_sram_1kbytes_1rw1r_20x256_20.gds     sky130_sram_1kbytes_1rw1r_20x256_20.v
functional_meas.sp  sky130_sram_1kbytes_1rw1r_20x256_20.html    sky130_sram_1kbytes_1rw1r_20x256_20_TT_1p8V_25C.lib
functional_stim.sp  sky130_sram_1kbytes_1rw1r_20x256_20.lef     sram.sp
run_drc.sh          sky130_sram_1kbytes_1rw1r_20x256_20.log     trimmed.sp
run_ext.sh          sky130_sram_1kbytes_1rw1r_20x256_20.lvs.sp
root@AnubhavPC:/mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20#
```

1. The screenshot of .lvs.rpt file :

2. Top Module

Open

icache_mem.v
~/OpenLane/designs/icache_flow/src

```
module icache_mem(
    input rst_n,
    input clk,
    input cs,
    input we,
    input [7:0] addr,
    input [7:0] write_allow,
    input [19:0] datain,
    output [19:0] dataout
);
    reg [19:0] dataout_stored;
    reg cs_int;

    wire [19:0] dataout_int;

    always @(posedge clk) begin
        if(!rst_n) begin
            cs_int <= 1;
            dataout_stored <= 0;
        end else begin
            if(cs)
                dataout_stored <= dataout_int;
            cs_int <= cs;
        end
    end

    assign dataout = cs_int ? dataout_int : dataout_stored;


    wire [19:0] dout1;

     sky130_sram_1kbytes_1rw1r_20x256_20 sram0(
        .clk0(clk),
        .csb0(!cs),
        .web0(!we),
        //.wmask0(write_allow[3:0]),
        .addr0(addr),
        .din0(datain[19:0]),
        .dout0(dataout_int[19:0]),

        .clk1(1'b0),
        .csb1(1'b1),
        .addr1(8'b0),
        .dout1(dout1[19:0])
    );


endmodule
```

3. Config.json and macro_placement.cfg file screenshot

Open | config.json ~/OpenLane/designs/icache_flow | Save

```
{
    "PDK": "sky130A",
    "DESIGN_NAME": "icache_mem",
    "VERILOG_FILES": "dir::src/icache_mem.v",
    "VERILOG_FILES_BLACKBOX": "dir::src/sky130_sram_1kbytes_1rw1r_20x256_20/
sky130_sram_1kbytes_1rw1r_20x256_20.v",
    "CLOCK_PORT": "clk",
    "CLOCK_PERIOD": 25.0,
    "DESIGN_IS_CORE": true,
    "FP_SIZING": "absolute",
    "DIE_AREA": "0 0 490 490",
    "PL_TARGET_DENSITY": 0.25,
    "VDD_NETS": "vccd1",
    "GND_NETS": "vssd1",
    "FP_PDN_MACRO_HOOKS": "sram0 vccd1 vssd1 vccd1 vssd1",
    "MACRO_PLACEMENT_CFG": "dir::macro_placement.cfg",
    "EXTRA_LEFS": "dir::src/sky130_sram_1kbytes_1rw1r_20x256_20/
sky130_sram_1kbytes_1rw1r_20x256_20.lef",
    "EXTRA_GDS_FILES": "dir::src/sky130_sram_1kbytes_1rw1r_20x256_20/
sky130_sram_1kbytes_1rw1r_20x256_20.gds",

    "RUN_KLAYOUT_XOR": false,
    "MAGIC_DRC_USE_GDS": false,
    "QUIT_ON_MAGIC_DRC": false
}
```

Open | macro_placement.cfg ~/OpenLane/designs/icache_flow | Save

```
sram0 125 125 N
```

4. Layout of the design on Magic screenshot.

5.

Clock Frequency (MHz)	40
Worst case setup slack (ns)	18.19
Worst case hold slack (ns)	0.29
Design area (μm2)	158,406
Total Power Consumption (μW)	92.5

Dcache :

Terminal screenshot :

```
[2025-03-23 17:41:41.969513] |============================================================================|
[2025-03-23 17:41:41.987064] |=========                    OpenRAM v1.2.48                       =========|
[2025-03-23 17:41:41.989715] |=========                                                          =========|
[2025-03-23 17:41:41.992130] |=========              VLSI Design and Automation Lab              =========|
[2025-03-23 17:41:41.994854] |=========        Computer Science and Engineering Department        =========|
[2025-03-23 17:41:41.997159] |=========            University of California Santa Cruz            =========|
[2025-03-23 17:41:42.000035] |=========                                                          =========|
[2025-03-23 17:41:42.002657] |=========         Usage help: openram-user-group@ucsc.edu          =========|
[2025-03-23 17:41:42.004615] |=========        Development help: openram-dev-group@ucsc.edu       =========|
[2025-03-23 17:41:42.007477] |=========               See LICENSE for license info              =========|
[2025-03-23 17:41:42.010102] |============================================================================|
[2025-03-23 17:41:42.012405] ** Start: 03/23/2025 17:41:42
[2025-03-23 17:41:42.014745] Technology: sky130
[2025-03-23 17:41:42.017582] Total size: 16384 bits
[2025-03-23 17:41:42.019833] Word size: 32
Words: 512
Banks: 1
[2025-03-23 17:41:42.021571] RW ports: 1
R-only ports: 1
W-only ports: 0
[2025-03-23 17:41:42.023551] DRC/LVS/PEX is only run on the top-level design to save run-time (inline_lvsdrc=True to do inline checking).
[2025-03-23 17:41:42.026206] Characterization is disabled (using analytical delay models) (analytical_delay=False to simulate).
[2025-03-23 17:41:42.028603] Only generating nominal corner timing.
[2025-03-23 17:41:42.031457] Words per row: None
[2025-03-23 17:41:42.034137] Output files are:
[2025-03-23 17:41:42.035871] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.lvs
[2025-03-23 17:41:42.038043] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.sp
[2025-03-23 17:41:42.040239] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.v
[2025-03-23 17:41:42.042405] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.lib
[2025-03-23 17:41:42.044589] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.py
[2025-03-23 17:41:42.046785] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.html
[2025-03-23 17:41:42.049172] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.log
[2025-03-23 17:41:42.051842] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.lef
[2025-03-23 17:41:42.053581] /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.gds
[2025-03-22 20:14:34.711995] ** Submodules: 71.3 seconds
[2025-03-22 20:14:34.737555] ** Placement: 0.0 seconds
[2025-03-23 00:18:44.258882] ** Routing: 14649.5 seconds
[2025-03-23 20:01:02.344486] ** Verification: 70938.0 seconds
[2025-03-23 20:01:02.347566] ** SRAM creation: 85658.9 seconds
[2025-03-23 20:01:02.348545] SP: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.sp
[2025-03-23 20:01:03.031532] ** Spice writing: 0.7 seconds
[2025-03-23 20:01:03.031661] DELAY: Writing stimulus...
[2025-03-23 20:01:04.032445] ** DELAY: 1.0 seconds
[2025-03-23 20:01:04.196614] GDS: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.gds
[2025-03-23 20:01:05.854587] ** GDS: 1.7 seconds
[2025-03-23 20:01:05.854770] LEF: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.lef
[2025-03-23 20:01:05.876407] ** LEF: 0.0 seconds
[2025-03-23 20:01:05.876506] LVS: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.lvs.sp
[2025-03-23 20:01:06.070108] ** LVS writing: 0.2 seconds
[2025-03-23 20:01:06.070250] LIB: Characterizing...
[2025-03-23 20:01:07.132079] ** Characterization: 1.1 seconds
[2025-03-23 20:01:07.132725] Config: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.py
[2025-03-23 20:01:07.132842] ** Config: 0.0 seconds
[2025-03-23 20:01:07.150799] Datasheet: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.html
[2025-03-23 20:01:07.154731] ** Datasheet: 0.0 seconds
[2025-03-23 20:01:07.154805] Verilog: Writing to /mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/sky130_sram_2kbytes_1rw1r_32x512_32.v
[2025-03-23 20:01:07.155284] ** Verilog: 0.0 seconds
[2025-03-23 20:01:07.249250] [openram.globals/cleanup_paths]: Preserving temp directory: /tmp/openram_anubh_791_temp/
[2025-03-23 20:01:07.249358] ** End: 85663.9 seconds
```

Output folder content :

```
root@AnubhavPC:/mnt/d/Work/Tools/OpenRAM/riscv_icache/sky130_sram_1kbytes_1rw1r_20x256_20# cd ../..
root@AnubhavPC:/mnt/d/Work/Tools/OpenRAM# cd riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32/
root@AnubhavPC:/mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32# ls
datasheet.info      run_lvs.sh                                sky130_sram_2kbytes_1rw1r_32x512_32.py
delay_meas.sp       setup.tcl                                 sky130_sram_2kbytes_1rw1r_32x512_32.sp
delay_stim.sp       sky130_sram_2kbytes_1rw1r_32x512_32.gds   sky130_sram_2kbytes_1rw1r_32x512_32.v
functional_meas.sp  sky130_sram_2kbytes_1rw1r_32x512_32.html  sky130_sram_2kbytes_1rw1r_32x512_32_TT_1p8V_25C.lib
functional_stim.sp  sky130_sram_2kbytes_1rw1r_32x512_32.lef   sram.sp
run_drc.sh          sky130_sram_2kbytes_1rw1r_32x512_32.log   trimmed.sp
run_ext.sh          sky130_sram_2kbytes_1rw1r_32x512_32.lvs.sp
root@AnubhavPC:/mnt/d/Work/Tools/OpenRAM/riscv_dcache/sky130_sram_2kbytes_1rw1r_32x512_32#
```

1. The screenshot of .lvs.rpt file :

2. Top Module

Open

dcache_mem.v
~/OpenLane/designs/dcache_flow/src

```
module dcache_mem(
    input         rst_n,
    input         clk,
    input         cs,
    input         we,
    input  [10:0] addr,
    //input  [3:0]  write_allow,
    input  [31:0] datain,
    output [31:0] dataout
);
    reg  [31:0] dataout_stored;
    reg         cs_int;
    reg  [31:0] dataout_mux;  // muxed output from one of the four SRAM blocks

    // Wires for each SRAM instance output
    wire [31:0] dataout_int0;
    wire [31:0] dataout_int1;
    wire [31:0] dataout_int2;
    wire [31:0] dataout_int3;

    // Bank selection and local address extraction.
    // The two MSBs of addr select the bank.
    wire [1:0] bank_select = addr[10:9];
    wire [8:0] local_addr  = addr[8:0];

    wire [31:0] dout1;
    wire [31:0] dout2;
    wire [31:0] dout3;
    wire [31:0] dout4;

    // Instantiate SRAM 0 (bank 00)
    sky130_sram_2kbytes_1rw1r_32x512_32 sram0 (
        .clk0(clk),
        .csb0(!(cs && (bank_select == 2'b00))), // Enable only if bank_select is 00
        .web0(!we),
        .addr0(local_addr),
        .din0(datain),
        .dout0(dataout_int0),

        .clk1(1'b0),
        .csb1(1'b1),
        .addr1(9'b0),
        .dout1(dout1)
    );
```

Open

dcache_mem.v
~/OpenLane/designs/dcache_flow/src

```
    // Instantiate SRAM 2 (bank 10)
    sky130_sram_2kbytes_1rw1r_32x512_32 sram2 (
        .clk0(clk),
        .csb0(!(cs && (bank_select == 2'b10))), // Enable only if bank_select is 10
        .web0(!we),
        .addr0(local_addr),
        .din0(datain),
        .dout0(dataout_int2),

        .clk1(1'b0),
        .csb1(1'b1),
        .addr1(9'b0),
        .dout1(dout3)
    );

    // Instantiate SRAM 3 (bank 11)
    sky130_sram_2kbytes_1rw1r_32x512_32 sram3 (
        .clk0(clk),
        .csb0(!(cs && (bank_select == 2'b11))), // Enable only if bank_select is 11
        .web0(!we),
        .addr0(local_addr),
        .din0(datain),
        .dout0(dataout_int3),

        .clk1(1'b0),
        .csb1(1'b1),
        .addr1(9'b0),
        .dout1(dout4)
    );

    // Multiplexer: select the output from the correct SRAM block based on bank_select.
    always @(*) begin
        case (bank_select)
            2'b00: dataout_mux = dataout_int0;
            2'b01: dataout_mux = dataout_int1;
            2'b10: dataout_mux = dataout_int2;
            2'b11: dataout_mux = dataout_int3;
            default: dataout_mux = 32'd0;
        endcase
    end

    // Register the output when chip select is active.
    always @(posedge clk) begin
        if (!rst_n) begin
            cs_int         <= 1;
            dataout_stored <= 32'd0;
        end else begin
            if (cs)
                dataout_stored <= dataout_mux;
            cs_int <= cs;
        end

    // Output logic: when cs was active on the previous clock, pass the muxed output.
    assign dataout = cs_int ? dataout_mux : dataout_stored;

endmodule
```

3. Config.json and macro_placement.cfg file screenshot

Open | config.json ~/OpenLane/designs/dcache_flow | Save

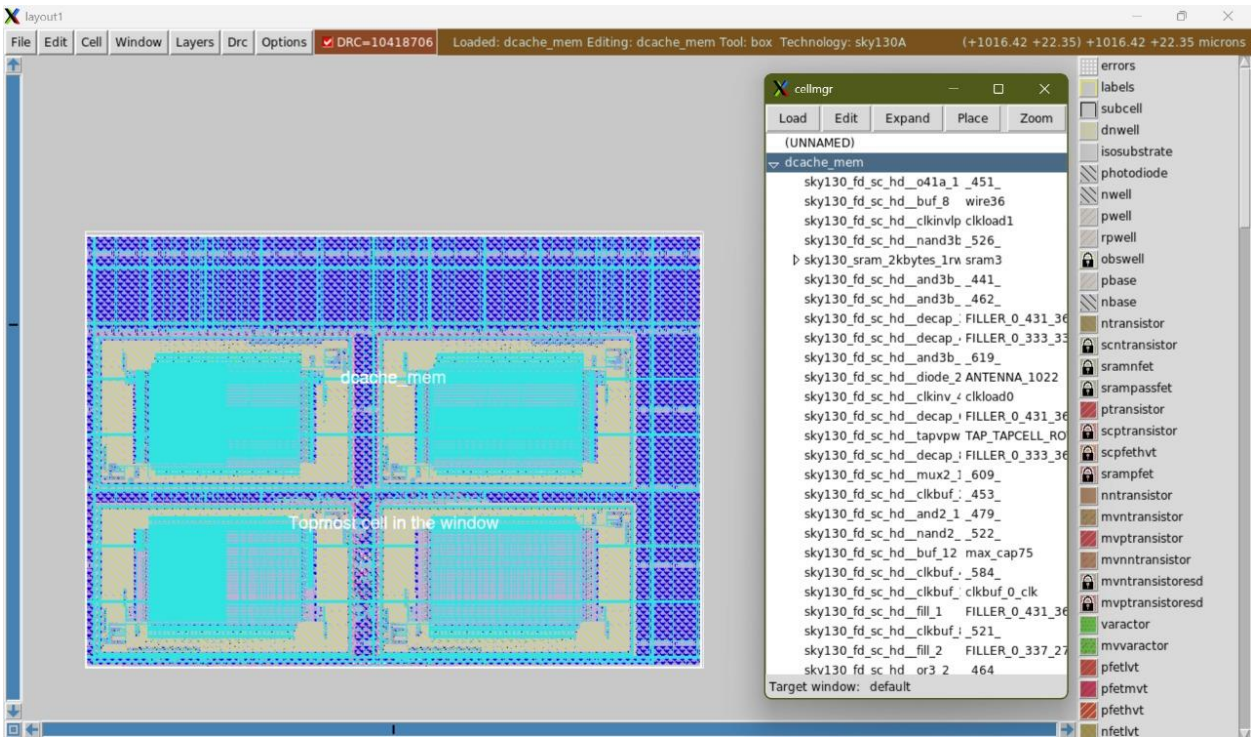
```
{
    "PDK": "sky130A",
    "DESIGN_NAME": "dcache_mem",
    "VERILOG_FILES": "dir::src/dcache_mem.v",
    "VERILOG_FILES_BLACKBOX": "dir::src/sky130_sram_2kbytes_1rw1r_32x512_32/
sky130_sram_2kbytes_1rw1r_32x512_32.v",
    "BLACKBOX_MODULES": "sky130_sram_2kbytes_1rw1r_32x512_32",
    "CLOCK_PORT": "clk",
    "CLOCK_PERIOD": 25.0,
    "DESIGN_IS_CORE": true,
    "FP_SIZING": "absolute",
    "DIE_AREA": "0 0 1700 1200",
    "PL_TARGET_DENSITY": 0.55,
    "VDD_NETS": "vccd1",
    "GND_NETS": "vssd1",
    "FP_PDN_MACRO_HOOKS": "sram0 vccd1 vssd1 vccd1 vssd1, sram1 vccd1 vssd1 vccd1 vssd1, sram2
vccd1 vssd1 vccd1 vssd1, sram3 vccd1 vssd1 vccd1 vssd1",
    "MACRO_PLACEMENT_CFG": "dir::macro_placement.cfg",
    "EXTRA_LEFS": "dir::src/sky130_sram_2kbytes_1rw1r_32x512_32/
sky130_sram_2kbytes_1rw1r_32x512_32.lef",
    "EXTRA_GDS_FILES": "dir::src/sky130_sram_2kbytes_1rw1r_32x512_32/
sky130_sram_2kbytes_1rw1r_32x512_32.gds",
    "RUN_KLAYOUT_XOR": false,
    "MAGIC_DRC_USE_GDS": false,
    "QUIT_ON_MAGIC_DRC": false
}
```

Loading file "/home/running_courses/EE705/EE705_8/OpenLane/desig... JSON Tab Width: 8 Ln 1, Col 1 INS

Open | macro_placement.cfg ~/OpenLane/designs/dcache_flow | Save

```
sram0 35 35 N
sram1 35 500 S
sram2 810 35 N
sram3 810 500 S
```

4. Layout of the design on Magic screenshot.



5.

Clock Frequency (MHz)	40
Worst case setup slack (ns)	12.89
Worst case hold slack (ns)	0.20
Design area (μm2)	1163102
Total Power Consumption (μW)	260