1. Description

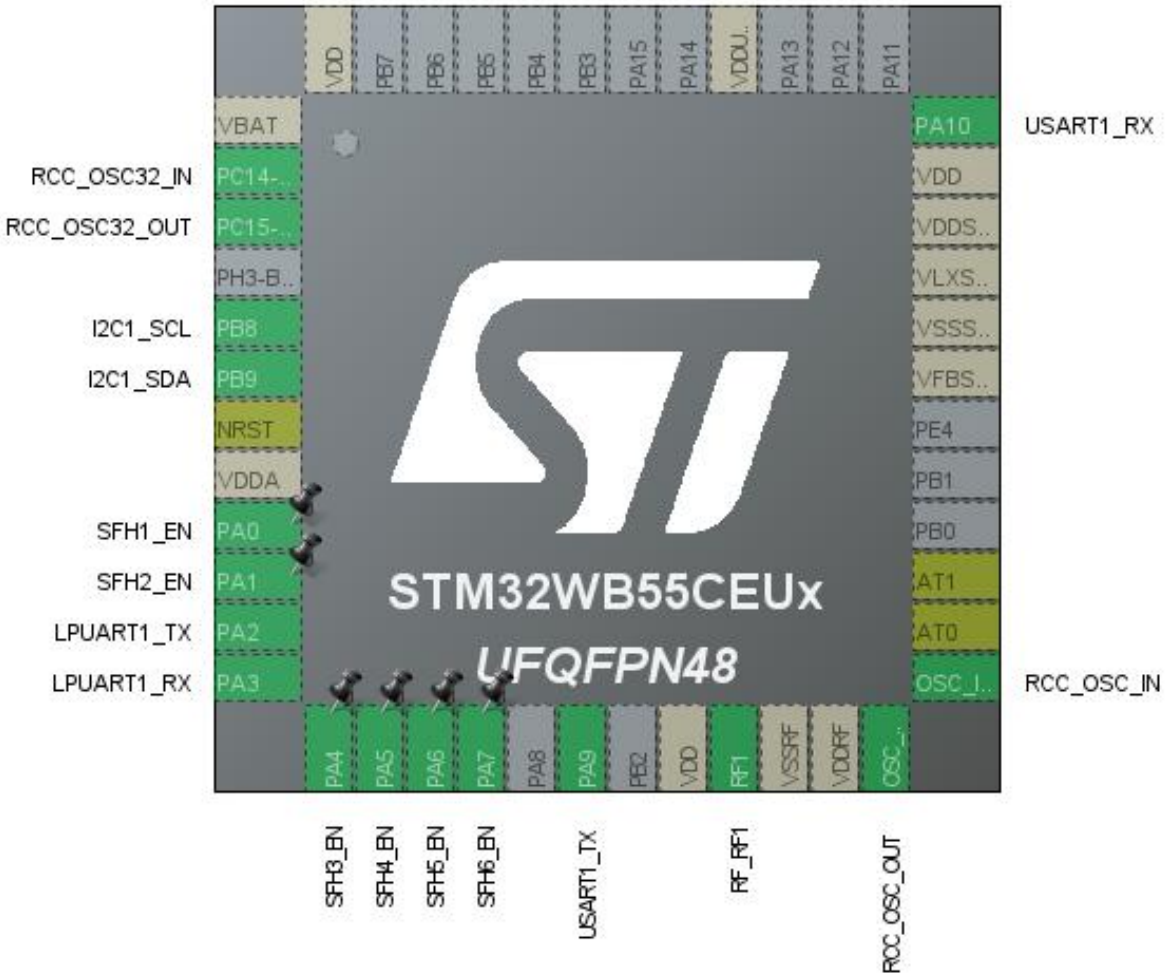
1.1. Project

Project Name	Zungenmaus_Prototype
Board Name	custom
Generated with:	STM32CubeMX 5.4.0
Date	11/25/2019

1.2. MCU

MCU Series	STM32WB
MCU Line	STM32WBx5
MCU name	STM32WB55CEUx
MCU Package	UFQFPN48
MCU Pin number	48

2. Pinout Configuration

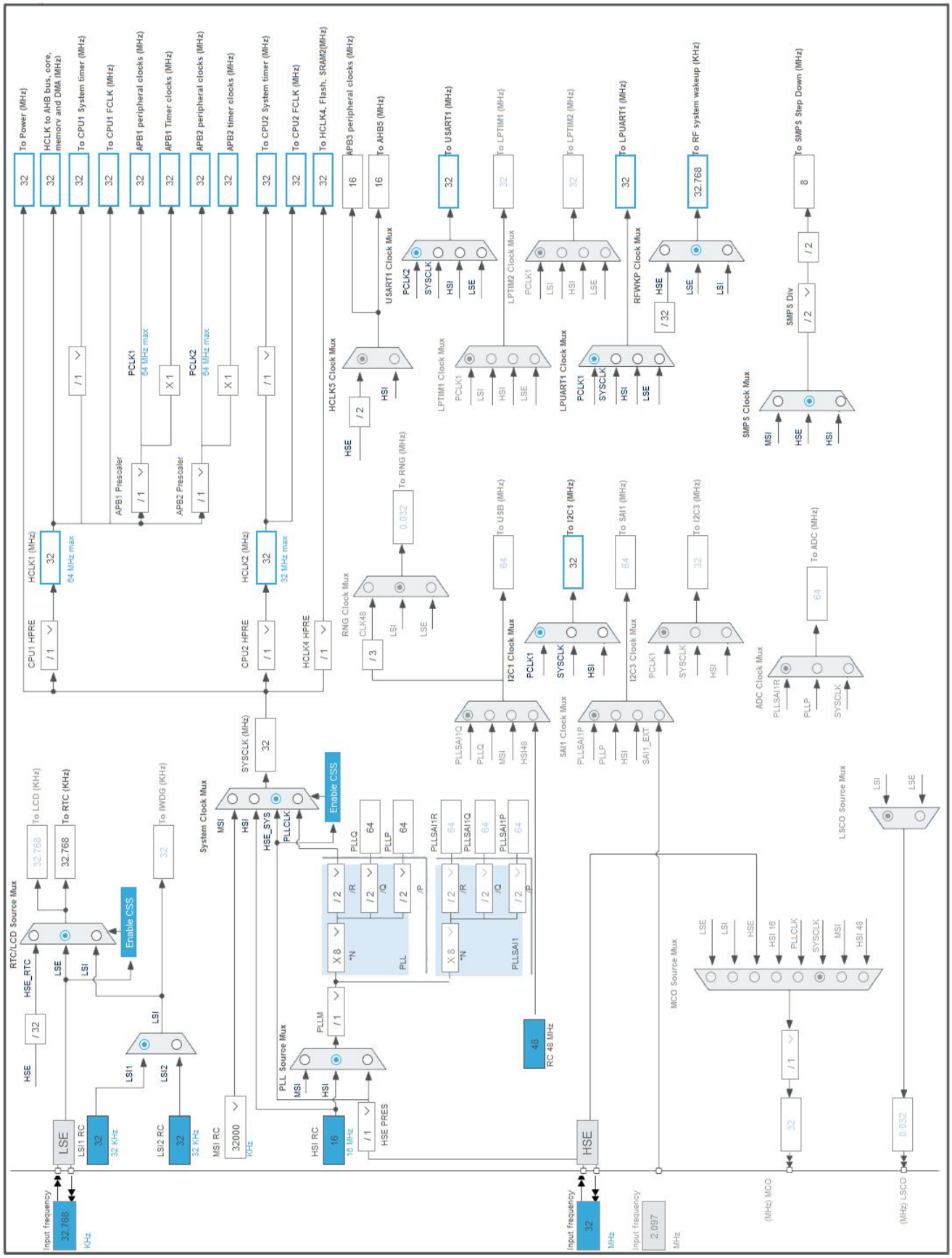


3. Pins Configuration

Pin Number UFQFPN48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
3	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PB8	I/O	I2C1_SCL	
6	PB9	I/O	I2C1_SDA	
7	NRST	Reset		
8	VDDA	Power		
9	PA0 *	I/O	GPIO_Output	SFH1_EN
10	PA1 *	I/O	GPIO_Output	SFH2_EN
11	PA2	I/O	LPUART1_TX	
12	PA3	I/O	LPUART1_RX	
13	PA4 *	I/O	GPIO_Output	SFH3_EN
14	PA5 *	I/O	GPIO_Output	SFH4_EN
15	PA6 *	I/O	GPIO_Output	SFH5_EN
16	PA7 *	I/O	GPIO_Output	SFH6_EN
18	PA9	I/O	USART1_TX	
20	VDD	Power		
21	RF1	MonoIO	RF_RF1	
22	VSSRF	Power		
23	VDDRF	Power		
24	OSC_OUT	MonoIO	RCC_OSC_OUT	
25	OSC_IN	MonoIO	RCC_OSC_IN	
26	AT0	NC		
27	AT1	NC		
31	VFBSMPS	Power		
32	VSSSMPS	Power		
33	VLXSMPS	Power		
34	VDDSMPS	Power		
35	VDD	Power		
36	PA10	I/O	USART1_RX	
40	VDDUSB	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Zungenmaus_Prototype
Project Folder	C:\Users\XHBH\Desktop\Studiearbeit\lyx\Hardware_STM32
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_WB V1.3.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32WB
Line	STM32WBx5
MCU	STM32WB55CEUx
Datasheet	DS11929_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. GPIO

7.2. HSEM

mode: Activated

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x00707CBB ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. LPUART1

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
MSI State	Enabled
HSI State	Enabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.6. RF

mode: Activate RF1

7.7. RTC

mode: Activate Clock Source

7.7.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	CFG_RTC_ASYNCH_PRESCALER
Synchronous Predivider value	CFG_RTC_SYNCH_PRESCALER

7.8. SEQUENCER

mode: Enabled

7.9. SYS

Timebase Source: SysTick

7.10. TINY_LPM

mode: Enabled

7.11. USART1

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	8 Samples

Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.12. STM32_WPAN

mode: BLE

7.12.1. BLE Applications and Services:

BLE Application Type:

BLE Application Type	Server profile

Server Mode:

BT SIG Beacon	Disabled
BT SIG Blood Pressure Sensor	Disabled
BT SIG Health Thermometer Sensor	Disabled
BT SIG Heart Rate Sensor	Disabled
Custom P2P Server	Enabled
Custom Template	Disabled

BLE Services Configuration:

The device needs to support the Peripheral Role	1
The device needs to support the Central Role	0
BLE_CFG_SVC_MAX_NBR_CB	7
BLE_CFG_CLT_MAX_NBR_CB	0

P2P Service:

P2P_SERVER_NUMBER	P2P_SERVER1

Local Name:

LOCAL_NAME	**ZungenM ***

7.12.2. Configuration:

HW Timer Server:

CFG_HW_TS_MAX_NBR_CONCURRENT_TIMER	6
CFG_HW_TS_NVIC_RTC_WAKEUP_IT_PREEMPTPRIO	3
CFG_HW_TS_NVIC_RTC_WAKEUP_IT_SUBPRIO	0
CFG_HW_TS_USE_PRIMASK_AS_CRITICAL_SECTION	1
CFG_HW_TS_RTC_HANDLER_MAX_DELAY	(10 * (LSI_VALUE/1000))
CFG_HW_TS_RTC_WAKEUP_HANDLER_ID	RTC_WKUP_IRQn

HW UART:

CFG_HW_LPUART1_ENABLED	**Enabled ***
CFG_HW_LPUART1_DMA_TX_SUPPORTED	Disabled
CFG_HW_USART1_ENABLED	**Enabled ***
CFG_HW_USART1_DMA_TX_SUPPORTED	Disabled

Generic parameters:

CFG_HW_RESET_BY_FW	Enabled
CFG_LPM_SUPPORTED	Disabled
CFG_DEBUGGER_SUPPORTED	Enabled
CFG_DEBUG_BLE_TRACE	Disabled
CFG_DEBUG_APP_TRACE	Disabled
CFG_DEBUG_TRACE_LIGHT	Disabled
CFG_DEBUG_TRACE_FULL	Disabled

Application parameters:

CFG_DEBUG_TRACE_UART	**hw_uart1 ***
CFG_CONSOLE_MENU	**hw_lpuart1 ***
CFG_ADV_BD_ADDRESS	0
CFG_FAST_CONN_ADV_INTERVAL_MIN	80
CFG_FAST_CONN_ADV_INTERVAL_MAX	100
CFG_LP_CONN_ADV_INTERVAL_MIN	1000
CFG_LP_CONN_ADV_INTERVAL_MAX	2500
CFG_IO_CAPABILITY	Display Yes No
CFG_MITM_PROTECTION	MITM protection required
L2CAP_REQUEST_NEW_CONN_PARAM	0
CFG_RTCCLK_DIVIDER_CONF	0

Debug options:

BLE_DBG_APP_EN	Disabled
BLE_DBG_P2P_STM_EN	Disabled

7.12.3. Parameter Settings:

No CTS for USART1

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	Low	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Low	
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
RF	RF1	RF_RF1	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PA0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SFH1_EN
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SFH2_EN
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SFH3_EN
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SFH4_EN
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SFH5_EN
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SFH6_EN

8.2. DMA configuration

DMA request	Stream	Direction	Priority
LPUART1_TX	DMA1_Channel1	Memory To Peripheral	Low
USART1_TX	DMA1_Channel4	Memory To Peripheral	Low

LPUART1_TX: DMA1_Channel1 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA1_Channel4 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel4 global interrupt	true	0	0
USART1 global interrupt	true	0	0
LPUART1 global interrupt	true	0	0
PVD/PVM0/PVM2 interrupts through EXTI lines 16/31/33	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CPU2 SEV interrupt through EXTI line 40 and PWR CPU2 HOLD wake-up interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
PWR switching on the fly, end of BLE activity, end of 802.15.4 activity, end of critical radio phase interrupt	unused		
HSEM global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report