UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, ECE 894, Fall 1401
Computer Assignment 1-2
Basic Switch and Gate Structures in Verilog
Week 6-7

Name:
Date:

1. Generate a switch level description for a 2-input NAND using NMOS and PMOS transistors. Use #(3, 4, 5) delay for the NMOS transistors and #(5, 6, 7) for the PMOS transistors. Generate a testbench and test your circuit.
2. In a testbench instantiate your NAND of Part 1 and a Verilog **nand** primitive. Adjust **nand** primitive delays to make it as close as possible to the timing behavior of the NAND of Part 1.
3. Generate a switch level description for a 3-input NAND using NMOS and PMOS transistors. Use #(3, 4, 5) delay for the NMOS transistors and #(5, 6, 7) for the PMOS transistors. Generate a testbench and test your circuit.
4. In a testbench instantiate your NAND of Part 3 and a Verilog **nand** primitive. Adjust **nand** primitive delays to make it as close as possible to the timing behavior of the NAND of Part 1.
5. Using the above NAND gates, build a 4-bit comparator with an equal (E) output that becomes 1 when A[3:0] and B[3:0] operands of the comparator are equal.
6. In a SystemVerilog testbench, instantiate the circuit of Part 5, and apply test data to test the comparator. Apply test data to force the comparator to exhibit its worst-case delay values.
7. Use SystemVerilog relational operator (?:) to write a description for the above 4-bit comparator. Use delay values from Part 6 to annotate your description.
8. In a SystemVerilog testbench, instantiate the circuits of Part 5 and Part 7, and apply test data to test the comparator. Compate the responses to the two descriptions in terms of their timing behavior.

Deliverables:

Generate a report that includes all the items below:

A. Do Parts 1 and 3, do the circuit diagram on paper and calculate the delay values manually before running the simulation.
B. For Parts 2 and 4, show your extract delay values from the waveforms and compare them with the values you calculated in A.
C. For Parts 5, 6, 7, and 8, show circuit diagrams, hand calculations and waveforms. Your SystemVerilog descriptions must correspond to the circuit diagrams. Your simulation run and the project built for this purpose must be demonstrated to the TA.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.