UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, ECE 894, Fall 1401
Computer Assignment 3
Basic Switch and Gate Structures in Verilog
Week 10-11

In this assignment, you are to describe an 8-bit Carry-lookahead adder that is based on Ripple Carry of 4-bit CLAs. You will use this adder for the implementation of an 8-bit ALU. For arithmetic operations, inputs are considered as positive 8-bit 2's complement numbers. The descriptions are to be at the expression or behavioral level and must be annotated with delay values based on their gate level implementation. Assume the delay of a 2-input gate is 7 ns, and each additional input adds 0.1 ns to the delay value.

A) Write a module description for an 8-bit CLA as follows and adjust its delays according to delay values stated above. As mentioned, use **assign** or **always** statements and annotate the delay values to the outputs based on your CLA paper design schematic.

CLAdder (input [7:0] dataA, dataB, input carryIn, output [7:0] dataOut, output carryOut)

B) Write a testbench and verify the timing and operation of the adder of Part A.

C) Using the above adder, show the design of the ALU as specified here. Table shown lists functions that the ALU can perform and their corresponding opcodes. The ALU inputs are data A[7:0] and B[7:0], and the 3-bit function F[2:0]. The ALU outputs are W[7:0], carry (c), and zero (z), where W is defined as defined in the table below, c is the carry output for arithmetic operations, and z becomes 1 when the ALU output is 8'b0. Since an adder usually forms the bottleneck of an ALU as far as delay is concerned, we will use the adder of Part A for the first four ALU operations. Show the block diagram of this circuit using the Rippled Carry CLA adder, multiplexers, other RTL components discussed in class, as well as a minimum number of discrete logic gates where needed.

Opcode	**Function**
000	W = A + B
001	W = A + 2×B
010	W = Min (A, B)
011	W = A + 0.5×B
100	W = 0
101	W = A | B
110	W = A & B
111	W = 2×B

D) Write a SystemVerilog description that corresponds to the block diagram of Part C. Based on the logic implementation and using delay values stated above, adjust delay of each ALU operation.

E) Develop a testbench for the ALU, test each operation and verify its timing.

Deliverables:

Generate a report that includes all the items below:

A. For all the above problems hand-drawn schematic diagrams and partial timing diagrams are required. Your SystemVerilog descriptions must correspond to the circuit diagrams. Your simulation run and the project built for this purpose must be demonstrated to the TA. *For the Graduate students: Show Yosys reports and be able to justify the hardware used.*
B. For Parts C and D, be able to justify the delays used in D based on hardware used in C. Be prepared to answer questions asked about the timing and gate counts of the various circuits in these problems.
C. In your testbench make use you include several test cases for each operation.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.