UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, ECE 894, Fall 1401
Computer Assignment 4
Basic Switch and Gate Structures in Verilog
Week 12

Name:
Date:

1. Generate a clocked SR-latch with active low S, R, and Clock inputs. Show this circuit in terms of an all-NAND circuit. Describe this circuit in Verilog using NAND primitives.
2. Annotate the circuit of Part 1 with gate delays that are based on switch level delays of 4 NS for the NMOS and 6 NS for the PMOS transistors.
3. Simulate the circuit of Part 2 to verify its operation. Apply simultaneous active inputs (S and R) and see the loss of memory.
4. Use an inverter to convert the SR latch of Part 2 to a clocked D-latch. Simulate this circuit to verify its operation.
5. Form an 8-bit register by wiring eight latches of Part 4.
6. Form an 8-bit shift register using the above latch. From left to right (*i* to 0), the output of latch *i* connects to the D input of latch *i-1*. The D input of latch *i* is the *sin* (serial input) of the shift register.
7. Simulate the circuit of Part 6 and explain why or why-not this circuit works as expected.
8. Use two D-latches of Part 4 to build a master-slave D-type flip-flop.
9. Create a synchronous reset (*rs*) for the flip-flop of Part 4 such that when this input becomes 1, the output becomes 0 with the clock.
10. Build an 8-bit register using the flip-flop of Part 8 in a **generate** statement. Simulate this register and verify its clocking and resetting operations.
11. Write a testbench for the circuit of Part 10 and test its resetting, and shifting operations. Explain why this circuit works and that of Part 6 does not.
12. Write an 8-bit register using an **always** statement.
13. Using the shift register of Part 12 design an LFSR with $x^8+x^6+x^5+x^4+1$ polynomial. For this, number shift-register flip-flops from 7 to 0 from left to right. A feedback from output of bit 0 (x^0 in the polynomial) connects to the input of bit 7 (x^8 in the polynomial). In the polynomial, the coefficient of term (x^i) is 1 where flip-flop *i* output connects to the feedback through an XOR gate. Coefficient of 0 for a term means that the corresponding output does not contribute to the feedback. Initialize this circuit to 8'b0 and start clocking it. The serial output from bit 0 has pseudo-random serial data. What is the period of this polynomial, i.e., how many clock cycles you have to give it to repeat itself. Learn about the period of this polynomial and answer questions when asked by the TA.