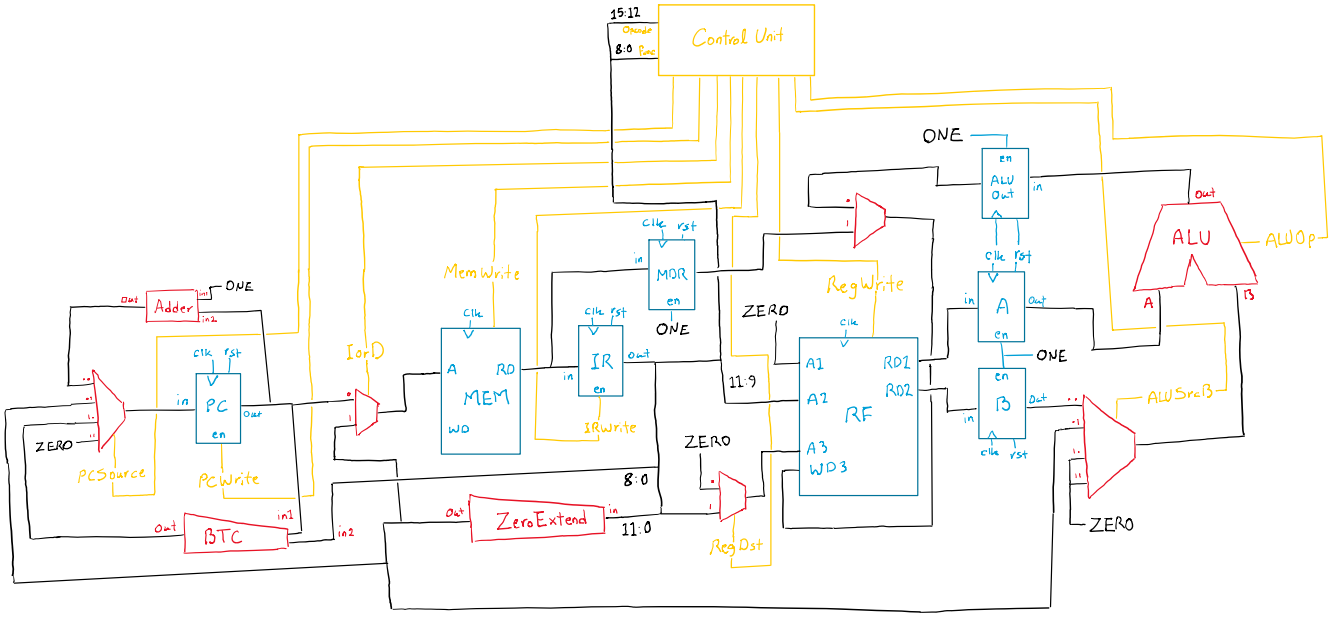
معماری کامپیوتر - تمرین کامپیوتری سوم

پنجشنبه, 1 آبان 1404 PM 05:59

معراج رستگار 810102576
معراج پورحسینی 810102420

طراحی دیتاپس:



طراحی کنترلر:

State	PCWrite	IRWrite	MemRead	MemWrite	IorD	RegWrite	MemtoReg	ALUSrcB	ALUOp	RegDst	Description
FETCH	1	1	1	0	0	0	0	0	0	0	Instruction Fetch
DECODE	0	0	0	0	0	0	0	0	0	0	Decode & Reg Read
MEM_ADDR	0	0	0	0	0	0	0	0	0	0	Address Calculation
MEM_READ	0	0	1	0	1	0	0	0	0	0	Memory Access (Load)
MEM_WB	0	0	0	0	0	1	1	0	0	0	Write-back from Memory
MEM_WRITE	0	0	0	1	1	0	0	0	0	0	Memory Access (Store)
EXEC_TYPE_C	0	0	0	0	0	0	0	0	Func	0	R-type Execution
EXEC_TYPE_D	0	0	0	0	0	0	0	1	Opcode	0	I-type Execution
WB_ALU	0	0	0	0	0	1	0	0	0	Note A	ALU Write-back
BRANCH	1*	0	0	0	0	0	0	0	1	0	Branch Completion
JUMP	1	0	0	0	0	0	0	0	0	0	Jump Completion

Function Bit	ALUOp	Operation
Func[0]	3'b101	Pass In1
Func[1]	3'b110	Pass In2
Func[2]	3'b000	Addition (+)
Func[3]	3'b001	Subtraction (-)
Func[4]	3'b010	Bitwise AND (&)
Func[5]	3'b011	Bitwise OR (|)
Func[6]	3'b100	Bitwise NOT (~)

Opcode	ALUOp	Operation
4'b1100	3'b000	ADDI (Add Immediate)
4'b1101	3'b001	SUBI (Sub Immediate)
4'b1110	3'b010	ANDI (And Immediate)
4'b1111	3'b011	ORI (Or Immediate)

Mux Name	Selection Signal	sel=0 Output	sel=1 Output
AdrMux	IorD	PC_Out	IR_Address_Ext
WDMux	MemtoReg	ALU_Result_Reg	MDR_Out
RegDstMux	RegDst	3'b000	IR_Out[11:9]
SrcBMux	ALUSrcB	B_Out (if 00)	Imm_Ext (if 01)

Signal	Condition	Value	Description
RegDst	Opcode == 4'b1000 AND Func[0] == 1	1	Write to IR[11:9]
	Otherwise	0	Write to 3'b000
PCSource	current_state == JUMP	2'b01	Jump Target Address
	current_state == BRANCH AND Zero == 1	2'b10	Branch Target Address
	Otherwise	2'b00	PC + 1 (Default)