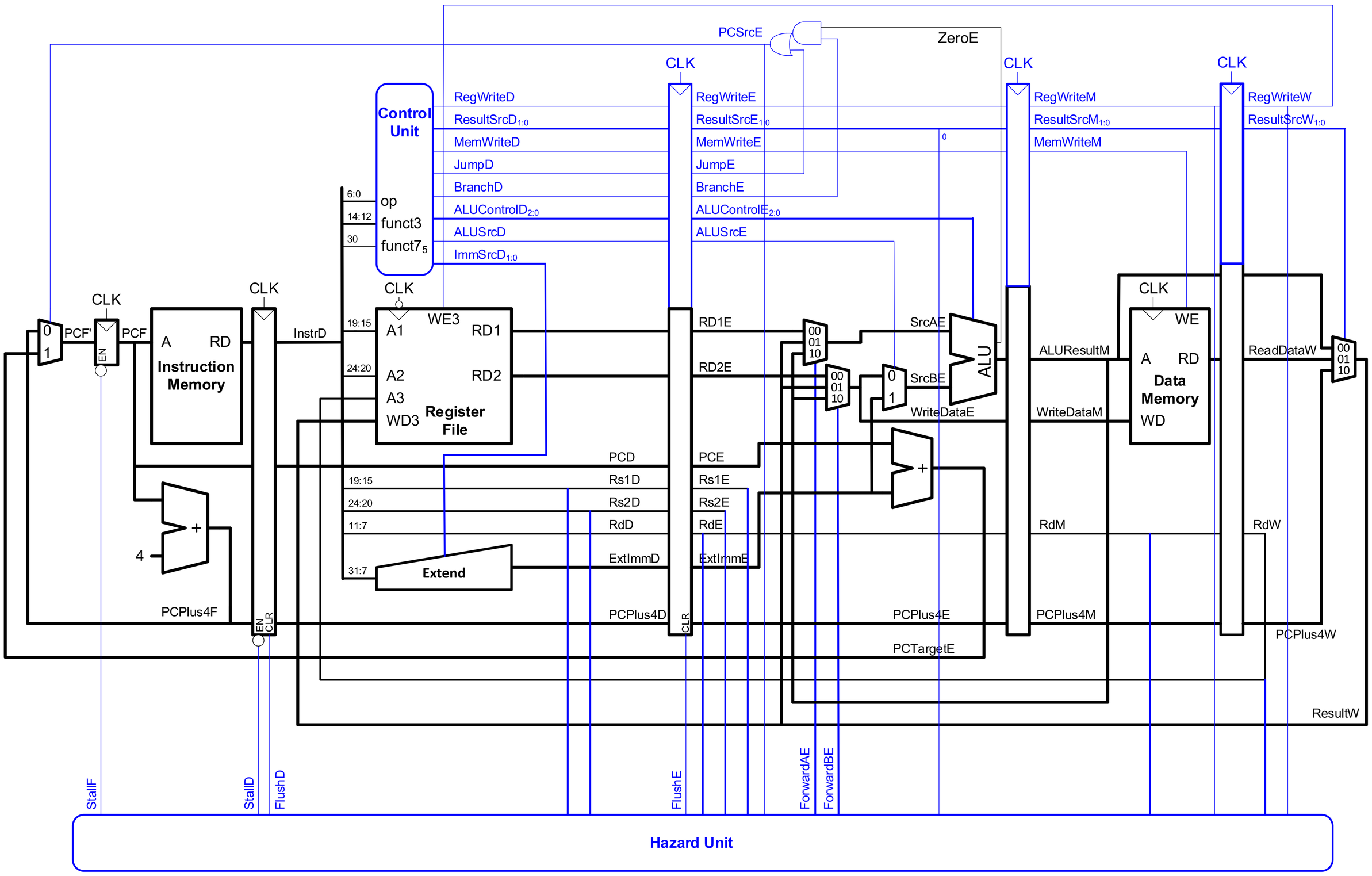
معراج رستگار 810102576
معراج پورحسینی 810102420

معماری کامپیوتر - تمرین کامپیوتری چهارم

جمعه, 12 دی 1404 04:12 AM

طراحی دیتاپس:



طراحی کنترل یونیت:

Command Type	Command	Opcode (7-bit)	RegWrite	ALUSrc	MemWrite	ResultSrc	ImmSrc	ALUOp	Jump	Branch
R-Type	add, sub, ...	110011	1	0	0	00 (ALU)	xxx	10	0	0
I-Type	addi, xori, ...	10011	1	1	0	00 (ALU)	0	10	0	0
Load	lw	11	1	1	0	01 (Mem)	0	0	0	0
Store	sw	100011	0	1	1	xx	1	0	0	0
Branch	beq, bne	1100011	0	0	0	xx	10	1	0	1
J-Type	jal	1101111	1	x	0	10 (PC+4)	11	0	1	0
I-Type	jalr	1100111	1	1	0	10 (PC+4)	0	0	1	0
U-Type	lui	110111	1	1	0	00 (ALU)	100	11	0	0

ALUOp	Funct3	Funct7 (bit 30)	Command	ALUControl	ALU
0	x	x	lw, sw, jal	0	Add (A + B)
1	x	x	beq, bne	1	Sub (A - B)
11	x	x	lui	110	Pass B (Imm)
10	0	0	add, addi	0	Add
10	0	1	sub	1	Sub
10	10	x	slt, slti	101	SLT (Set Less Than)
10	100	x	xor, xori	100	XOR
10	110	x	or, ori	11	OR
10	111	x	and, andi	10	AND

@mragetsars

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طراحی هازارد یونیت:

	Condition	ForwardAE	Source
1	(Rs1E == RdM) & RegWriteM & (Rs1E != 0)	10	ALUResultM (Memory)
2	(Rs1E == RdW) & RegWriteW & (Rs1E != 0)	1	ResultW (Writeback)
3	Else	0	Rd1E (RegFile)

	Condition	ForwardBE	Source
1	(Rs2E == RdM) & RegWriteM & (Rs2E != 0)	10	ALUResultM (Memory)
2	(Rs2E == RdW) & RegWriteW & (Rs2E != 0)	1	ResultW (Writeback)
3	Else	0	Rd2E (RegFile)

Condition	Stall/Flush
ResultSrcE0 (Is Load) AND (RdE == Rs1D OR RdE == Rs2D)	StallF = 1 StallD = 1 FlushE = 1

Condition	Flush
PCSrcE (Branch Taken OR Jump)	FlushD = 1 FlushE = 1