Hybrid Approach of Error Detection And Correction on board Nano Satellite

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Abstract

The nanosatellite is constantly evolving and growing significantly over the world. This system establishes a huge necessity for advanced, efficient and reliable error detection and correction systems that are capable of fast and huge data transmission with fewer errors. The hybrid approach has been recognized as an applicable scheme to avoid single and multiple events affecting onboard nanosatellites in Leo. In this thesis, We introduced a hybrid approach of Error Detection and Correction method which is based on four different systems of EDAC algorithms such as Parity check, Hamming codes, Cyclic redundancy check, and Reed Solomon Code. We will establish a hybrid system of EDAC that has error counting methods that will change the error correction algorithm based on error types. EDAC methods codes are tested both in verilog and field-programmable gate array. This technique is simple and also achieves high reliability and accuracy, compared to other similar methods.

Acknowledgements

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Publication List

The main contributions of this research are either published or accepted or in preparation in journals and conferences as mentioned in the following list:

Conference Papers

1. Mahmudul Hasan Sarker, Most. Ayesha Khatun Rima, Md. Abdur Rahman, A.B.M. Naveed Hossain, Noibedya Narayan Ray and Md. Motaharul Islam "A Comparative Approach of Error Detection and Correction for On-board Nano Satellite", International Conference on Sustainable Computing, SCOPUS Indexed Springer Book Series, 'Advances in Intelligent Systems and Computing (AISC),March 19-20, 2021.

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Chapter 1

Introduction

Error detection and correction devices on board Nano satellites aim to secure data transmission between satellite and Ground station. They are subject to unstable data corruption because of interference, thermal noise or any other type of noise. Mainly there are two general types of error: single and burst error, a single bit error means a one bit changed from 0 to 1 or 1 to 0. Burst error means more than one conjugated bit corrupted[1]. Error detection process is a first step to Error correction, which is dependent on adding extra bits to the original data. These redundancy bits are added at the transmitter and removed by the receiver. Redundancy bits are achieved through two main coding schemes like convolution coding and block coding. In error correction, it is necessary to know the number of corrupted bits and their location in the received message. Error correction can be classified as an Automatic repeat request, Forward error correction, and Sometime ARQ and FEC can be combined, this method is called hybrid automatic repeat-request. There are many systems designed to detect and correct errors, but with a separated technique or with other correction code, such as EDAC using Parity check technique only, CRC technique, Hamming technique, Reed Solomon code. Here we have Nano satellite which transmitted data to the ground station from there error can be checked by the help of some algorithms. In the ground station the algorithm which are used to check if errors are present in our data with the help of cyclic redundancy check. After that steps with type of errors we get from the data specified by detection methods[2]. In the detection methods we figure out whether errors are present in our data if we can detect there are errors then we go to the correction method. Based on our errors we need to change our algorithms according to the size of errors. According to the bits of error we have separate algorithms to work on each type of it. In this correction method we would correct our data with the help of algorithms set of errors. With the help of this correction methods we would now finally get our desired error less data.

1.1 Thesis Overview

Nanosatellite is any object that moves in a curved path around a planet. The earth observation satellite is all about information collection regarding the structure of the earth. Earth observation satellite is one of the fundamental tools for the research of the earth's environment. From Earth's surface, EO Sat applies smart image sensors to observe and obtains information on the earth's surface and also infrared is utilize for beneath observation. By overserving the earth from the space EO satellites provide essential information on weather monitoring, urban monitoring, Natural Disasters, Agricultural Growth Monitoring and Environmental monitoring etc. We identify some of the problems in the Bangabandhu Satellite communication system and our target is to obtain solve those problems and get high reliability and accuracy.

1.2 Motivation

Bangladesh as its unique geographical view is deeply discovered for natural disasters possibility. Bangladesh telecommunication infrastructure has always been suffering from interruptions and complications as rational disasters hit the country. Satellite networks can play a necessary role in ensuring continuous communication in Bangladesh, during such an emergency situation. Bangabandhu Satellite launched May 12, 2018. Bangabandhu Satellite has made it possible to connect remote assets such as real-time observation on agriculture and geographical environments. It also has facilitated mobile banking and retails, contributed to the development of sustainable cities, and derived the use of sensor networks along with the transformation of transportation infrastructures. Bangabandhu Satellite has escalated the broadband speed at an affordable cost which has brought positive impacts on the economy. Bangabandhu Satellite operation encounters technical errors while handling a vast quantity of operations. To protect and authorize the data certain error detection and correction methods are implemented from the ground station. Therefore, the Bangabandhu Satellite communication system and our target is mutual which is to obtain the solution to those problems and get high reliability and accuracy.

1.3 Contributions

The main contributions is summarized as follows:
• proposing a hybrid approach suitable EDAC scheme and a model for use in satellites.
• Studying the anomalies recorded by several LEO satellites.
• Implemented the algorithm based on Verilog language and Spartan-6 FPGA
• Evaluated the performance with the existing solution such as Parity check, Hamming code, Cycle Redundancy check, and Reed Solomon technique.
• We have proposed an architecture that consist of EDAC method for the nano satellites.

• We have studied, analyzed and compared the Error detection and correction algorithms that are used by the satellites.
• We have identified the number of erroneous bits. Based on that we have also proposed a suitable error correction methods.
• We have implemented the scheme for CRC, Parity check, Hamming Code and Reed Solomon code.
• Proposing a model for the Bangabandhu Satellite Communication system.
• Finally We have identified the limitations of our proposed methods.

1.4 Methodology

We have proposed a hybrid EDAC scheme for and a model for Bangabandhu Satellite communication system. This system will reduce the error in satellite communication. Error Detection And Correction Process are show in figure 1.1.

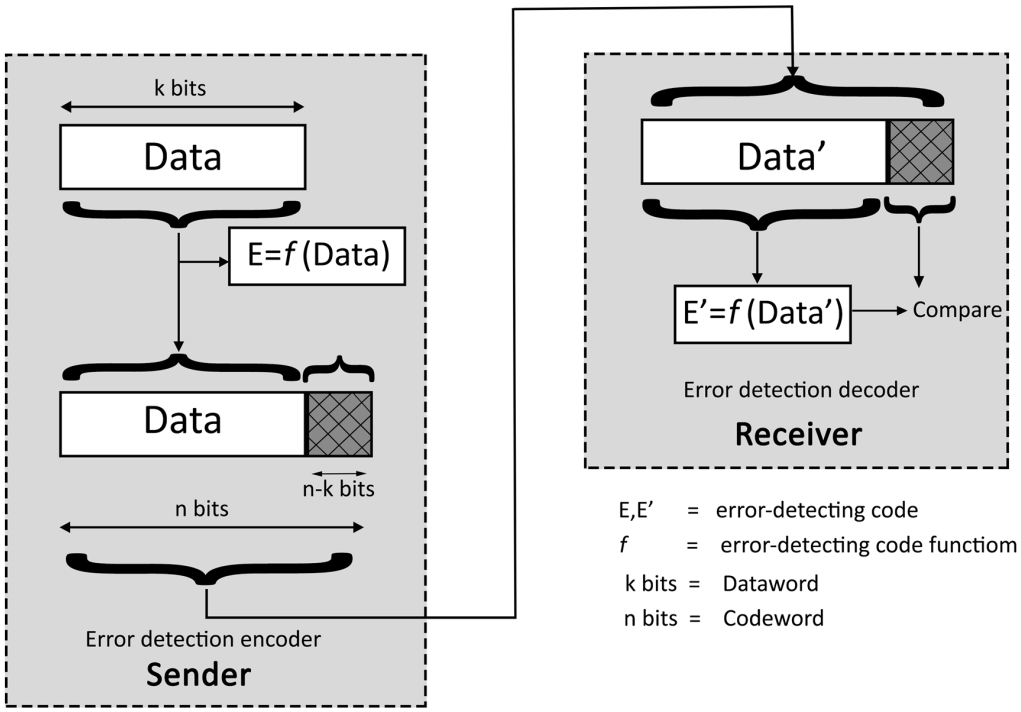

Figure 1.1: Error Detection Process

1.5 Thesis Outcome

• Developing an algorithm that will provide significantly high reliability and accuracy with respect to other existing methods.
• The algorithm is compact so that the spartan-6 FPGA will consume less amount of power.

1.6 Organization of the Report

The remaining of the report has been described in the following manner.
Chapter 2 is getting conversant with our project related works and literature review.
Chapter 3 exhibits the design of our project and analysis of our works and our proposed methodology.
Chapter 4 presents our implementation of works and the evaluation of results and accuracy.
Chapter 5 describes the standards, impacts and constraints we are acquiescing to our work.
Chapter 6 discusses the conclusion, limitations and future work of our project.

Chapter 2

Background

We believe it's fundamental to get familiar with the background of our thesis. In this section, we will introduce the main problems and get to know what extent previous studies have explored this problem. For this, we will discuss similar applications to our project and go into detail with previous literature works.

2.1 Preliminaries

In this section we explore the essential parts in preparation for our main work.

2.2 Similar Applications

Different types of applications are used developed EDAC sytem for the Nanosatellite communication.

*1.***Vivado Simulator**[1]

Xilinx software is a design collection that grants taking a design from entry over Xilinx accessory program. This software creates a high-level design used HDL such as VHDL, Verilog or using simplified. The solution of this software is a valuable, connected, or different system, high levels of software-based intelligence with hardware development, and any connectedness. Xilinx used industrial, military, aerospace, space grade products, and defense industry. Xilinx has a free trial version available for student accounts only another version.

Features:

- System Verilog
- VHDL language
- Real time simulation check
- Graphical view

Missing Features:

- Mixed HDL simulation

[1]https://www.xilinx.com/products/design-tools/vivado.html

*2.***ModelSim:**

The Modeltech simulator was the first mixed-language simulator that capable of simulating both VHDL and Verilog design entities together. ModelSim is a simple to use so far flexible VHDL, System Verilog, System-C simulator by the graphical view. It is computing detectable, register transfer level, and gate-level modeling. Modeltech simulator provides high accuracy and performance Verilog and SystemVerilog simulation. It expands the verification capabilities to more advanced methodologies such as assertion-based verification and functional coverage. The leading simulator for FPGA design is still the Modeltech simulator.

Features:

- Advanced Code Coverage Mixed HDL Simulation
- Debug Environment
- Verilog language
- VHDL language
- Graphical view

Missing Features:

- API interface
- Real time simulation check

*3.***MATLAB**[2]

Matlab is a high-level programming language. Matlab good perform for matrix based work. This software most preferable for scientists and engineers. This software analyse data to create real life applications model and simulation this model data. In this software have many mathematical libraries and functions. Matlab mostly used Plotting graph, mathematical problem calculation, Data analysis, signal Processing, image Processing, video Processing, applications analysis.

Features:

- High-Level Language
- Interactive Environment
- Graphical view
- API plugins
- Free student version

Missing Features:

- System Verilog language
- VHDL language

[2]https://www.mathworks.com/products/matlab.html

*4.***ISE Simulator**[3]

ISE Simulator or ISim is an integrated HDL simulator applied in CPLD designs and Xilinx FPGA simulations.ISE Simulator Lite and complete version ISE simulator are the configurable versions of the ISE simulator. There is an ISE Design Suite pack which is included in Xilinx Bundle and another one is the ISE Web pack. Mixed-mode language simulation and Xilinx's FPGA based designs can be implemented with the ISim.

Features:

- Differents language support
- VHDL and Verilog language
- Graphical interface
- Free student version
- Compilation of multi thread
- Post-Processing capabilities

Missing Features:

- No code coverage
- library file
- Python features

5. **MPSim**[4]

The simulator runs on your PC to simulate the actions of the various PIC and dsPIC microcontrollers. MPsim is a quick-compiled simulator with the full support for Verilog, System Verilog. It includes a Designer, integrated Verilog and SystemVerilog debugging environment and has built-in support for multi-CPU simulation. You can verify your software routines execute as designed and debug, test and inspect your code. MPLAB SIM helps you optimize your application with timing tools, trace tools, and various graphical analyzers.

Features:

- Using the built-in editor
- Assemble, compile design simulation code
- Circuit debuggers
- Timing graph with the simulator
- Real time simulatior or emulator check

Missing Features:

- MPSIM missing WREG in Watch-tool
- MPSIM cannot get symbol to display

[3]https://www.xilinx.com/products/design-tools/isim.html
[4]https://www.mathworks.com/matlabcentral/fileexchange/71478-mpsim

2.2.1 Benchmark Analysis

A number of features of the benchmark applications discussed above are shown in the Table åpp

Features	Vivado Simulator	ModelSim	MATLAB	ISE Simulator	MPSim
Verilog language	Yes	Yes	No	Yes	No
VHDL language	Yes	Yes	No	Yes	No
Graphical view	Yes	Yes	Yes	Yes	Yes
Application Program Interface	No	No	Yes	No	No
Real time simulation check	Yes	No	No	No	Yes
Mixed HDL Simulation	No	Yes	No	No	No

Table 2.1: Benchmark analysis of applications similar to our project

2.3 Related Works

Motaharul et al.[3] proposed a Hamming Code to prevent parity and parity single bit error onboard satellite in LEO. The main focus is to work on Error Detection and Correction via generating a Hamming Code matrix. After comparison with other Hamming codes, Cycle redundancy check, etc. The schematic limitations from the generated Hamming codes [16, 11, 4] were proven to be the most efficient. MATLAB is used for the implementation process. Both Single Bits and Double Bits Errors can be solved via this algorithm.

Pakartipangi et al.[4] proposed a technique to obtain wider coverage area images for low dimensions satellites. Using camera array wider and detailed images found via this system. The system handle all the errors bit using XULA2 LX9 FPGA board. Camera array was designed such way that has no overlapping area can't be found.

Ahmed Hanafi et al [5] proposed an SRAM-based FPGA technology that implements an onboard computer system and used low earth orbit Nanosatellites. The hardware and software architecture system is based on Xilinx's Spartan 6 FPGA. The system was designed for developing a payload architecture and an inherent space environment.

Ibrahim et al.[6] proposed a satellite system's design with acceptable accuracy in a low power budget. The latest FPGAs are capable of adopting orbital changes to combat external hazards. This paper presents a concept to establish avionics systems by utilizing crucial features with the available FPGAs. Scrubbing keeps the FPGA data configurations safe with frame calculation and back-tracking method.

Daniel et al.[7] proposed a technique that describes a guideline for simulating the system accuracy, providing the necessary statistics to support the decision system regarding

the necessary methodology to be implemented[7]. The system design microsatellites for monitoring air pollution in Mexican and Latin American cities. Atmospheric pollutants from cars, volcanoes, industrial areas, etc. need to be monitored to keep the spectrometer in the infrared or ultraviolet range[7]. Author design system based on COTS devices.

Wilson at el.[8] proposed two major supervise themes hybrid computing and reconfigurable computing[8]. The system survey of the impose and convenience for small satellites and also focuses on new technologies, methods, and implementation for the next generation[8].New technologies such as CHREC Space Processor, that demonstrates how system designers can feat hybrid and reconfigurable computing on SmallSats to harness these advantages for a variety of purposes[8].

Banu et al.[9] proposed an encryption method to secure terrestrial communication via small satellite. Increased quantity of sending valuable and sensitive data, a satellite can bring risks of providing access to unauthorized data. An advanced Encryption Standard method is used to protect data from such threats. Satellite operates in a harsh environment surrounded by radiation and magnetic fields which can cause malfunctions in the satellite system and cause fatal faults. The Advanced Encryption System is strong enough to handle this fault to protect the valuable data and uninterrupted data transmission from potential corruptions.

Banu et al.[10] proposed a commercial algorithm also known as Advanced Encryption Standard. In order to protect valuable and sensitive data and prevent unauthorized access in terrestrial communication, *5* modes of AES in satellite imaging has been used. To prevent fault from noisy channels and effect of SEUs, those *5* modes were analyzed and observed using Hamming error correction code. Measurements of power and throughput overhead were presented with the implementation of Field programmable gate array.

Hiler et all.[11] proposed a parity check matrix and a calculated syndrome of error detection and correction on board nano satellites. The scheme can self-detect and self-correct any single event effects error that occurs during transmission[11]. Cryptographic protection is used to secure transmissions from being hacked. MATLAB and VHDL were used to test out three types of Hamming Code methods. Among them, the most efficient version was Hamming [16, 11, 4].

BENTOUTOU et al.[12] proposed an onboard EDAC method to protect data transmission among AISAT-1 CPU and it's memory. The following paper presents the applications of double bit EDAC and implementation with FPGA. The EDAC is calibrated and computed with 3 kinds of techniques.

Authors	Contributions	Remarks
Alan D. George et al	Focused on using a hybrid and re-configurable Computing to build a fault-tolerant system.	It's not feasible.
Y. BENTOUTOU et al	EDAC approach to observe SEU and MBU activity.	CRC was not used for correction.
Alvar Saenz-Otero et al	Developed a FPGA based design with COTS component for fault tolerance.	It's feasible.
Roohi Banu et al	Proposed a fault tolerance method using AES method.	Hamming algorithm was used for error detection.
Roohi Banu et al	Enhanced the AES method with 5 modes of fault-tolerance.	EDAC was implemented using hamming code bits.
Mohamed Mahmoud Ibrahim	Developed a reconfigurable avionics system on SRAM based FPGA for fault tolerance.	Xilinx Virtex5 FPGA was used in this.
Ahmed Hanafi	Proposed a SOC approach with SRAM based FPGA with a reconfigurable architecture for LEO.	Hamming code was used in OBC subsystem.
Caleb Hillier	Focused on developing a new version of Hamming code.	MATLAB and VHDL was used for testing out the results.
Md. Motaharul Islam	Used a special Hamming code algorithm that uses the concepts of parity check and parity bits to prevent Single-bit errors.	CRC was used for correction.
Whildan Pakartipangi	Analyzed FPGA based 2*2 matrix camera for Data Handling application.	XuLa2 LX9 Spartan6 was used as FPGA board.

Table 2.2: Comparison table of literature review

2.4 Summary

In chapter 2, we have shown some similar papers and patent that is related to our project. We have investigated background work corresponding to the project. We will go over our project design and proposed solution in the next chapter.

Chapter 3

Project Design

3.1 Requirement Analysis

3.2 Methodology and Design

3.2.1 System Configuration

The proposed system is built on a Spartan-6 FPGA SP605 evaluation kit Xilinx along with six OV2640 camera module. Six OV2640 camera module has a 360-degree view of Nano-Satellite. The installation of six cameras in Nanosatellite has made the image processing advance to a new horizon. A new chapter of Nanosatellite will begin through this implementation of six OV2640 cameras. The system block diagram and schematic diagram are shown in 4.19 and 4.20. The system consisted of a processor using Xilinx Spartan-6 FPGA as onboard data handling. The six OV2640 camera modules are attached with Xilinx Spartan-6 FPGA and configure into 2 X 3 array. FPGA controls the camera data information according to the camera array. FPGA fetched the camera images and then send it to the PC. The PC arranged the image according to the camera array. Our system block contains a clock generator, UART camera controller, UART PC controller, bridge, UART camera switch.

3.2.2 Clock generator

The clock generator is a type of circuit that generates the time signal and synchronizes in circuit operations. Amplifier and resonant circuit are the primary parts that are used by all clock generators. The Amplifier sends a portion of the inverted signal to the oscillator to maintain the performance of oscillation. The Quartz Piezoelectric Oscillator is usually Resonant circuits, even though RC circuits and simplified tank circuits might be applied. For the basic signal modifications, the generator might perform them in sections.

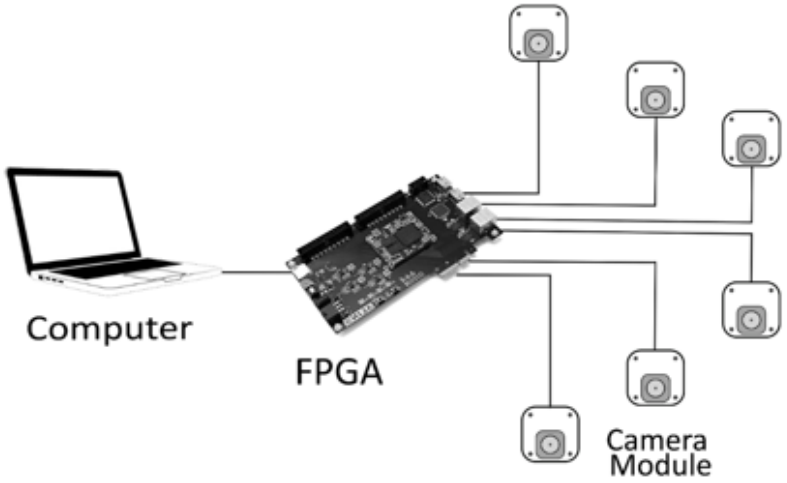

Figure 3.1: System Configuration

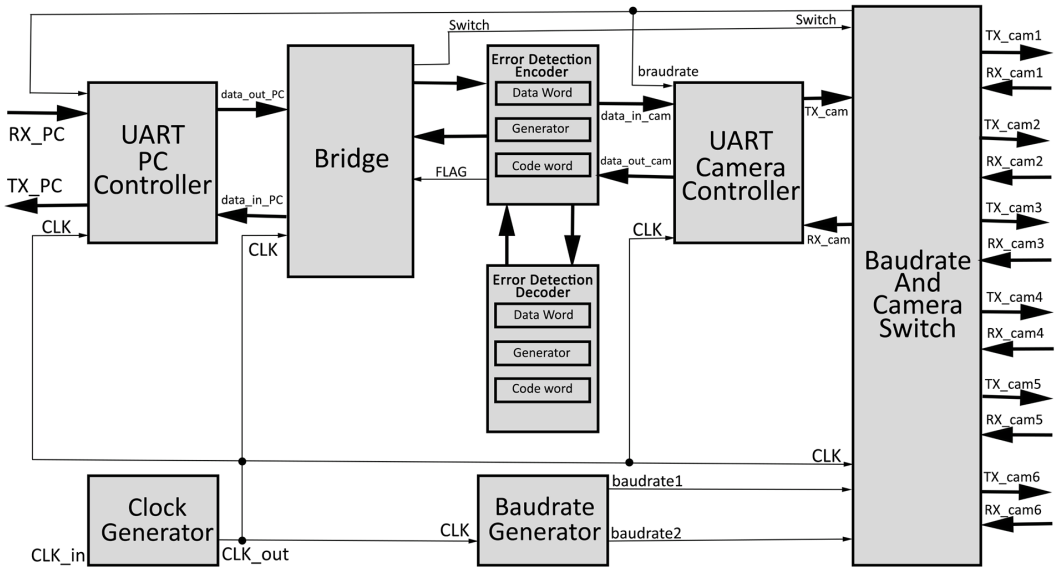

Figure 3.2: Schematic diagram of camera module interface with Spartan-6 Fpga

3.2.3 UART Camera Controller

UART camera controller is basically necessary for building up a communication channel between the camera modules and the FPGA. UART camera controller can send the data to all the camera modules simultaneously, but at a time it can communicate with one camera module. Switch block controlled the communication channel of FPGA and camera modules[4]. Which camera will communicate using UART Camera Controller that will be decided by switch block. UART Camera Controller worked with *50* MHz of clock frequency.

3.2.4 CubeSat

CubeSat is a miniature satellite which used for low Earth orbit and now it's being used for interplanetary missions also. Miniaturizing satellites reduce the cost of deployment. There are five types of CubeSat's. There are rechargeable lithium-ion batteries which get power from solar light. Solar cells used to convert the solar light into electricity.

3.2.5 Baudrate and Camera Switch

As multiplexer, switch block is used here and using UART Camera Controller which camera module can communicate that is deciding by it. And also, this block can have controlled the baud rate changing of UART Controller from 38400 to 115200 and vice versa. This block performed its work by the switch command forwarded by Bridge block[4].

3.2.6 Bridge

The uart pc controller connected with the uart camera controller by a bridge block. This block helped the received data to the camera module and the data is received from pc, vice versa also. In this controller, data flow from the camera module to the PC and data flow from the PC to the camera module.

3.2.7 Error Detection Encoder and Correction Decoder

Encoders are error detection methods that are used to change a signal or camera data into code in a nanosatellite. The encoder uses a generator that takes a copy of camera data into a dataword and generates camera data. The encoding operation must be revised to generate the correct codeword and the detector detects errors. The sender organizes codewords out of dataword by using a generator. Each codeword sent to the receiver may reduce errors during transmission. Decoders are error correction methods that are used to change code into the signal or camera data in a nanosatellite. If the error bits are corrupted during the transmission then the sender sends the error message to the codewords. The

receiver receives an error message in the dataword. If the remainder is zero no errors will occur and if the remainder is non zero, a transmission error will occur.

3.2.8 Dataword

A data word is a basic unit of data. For the block coding, basically we split our data into many blocks and each bit is known as a data word. The sender encodes the dataword sends it to the receiver. The receiver draws out the dataword. If the codeword is not valid, then it will be thrown away. During the transmission and receiving codeword gets paid off. It is a sustainable codeword. Dataword maybe figures out incorrectly by the receiver. Two of the paid off bits occurred undetectable errors.

3.2.9 Codeword

A code word is an element of a classified order or protocol. Each codeword is put together in line with the particular rules of the code and allocated a unique meaning. We add r redundant bits to individual blocks to build the length n = k + r. The appear n-bit blocks are called codewords, with n bits, we can generate a sequence 2^n codewords.since n > k the number of workable codewords is huge than the number of feasible dataword. The block coding procedure is one-to-one, the same dataword procedure is always encoded as the same codeword. This method that we have $2^k - 2^n$ codewords that are not passed down. The receiver can notice a change in the genuine codewords if the receiver has an inventory of well-founded codewords and the genuine codewords have changed to baseless one.

3.2.10 Generator

This function notices the stack of nested blocks attach to the identified explained input, generates the code for that stack, orders the code, and returns the code as a string. The generator is the procedure by which a compiler's code generator transforms some in-between presentation of source code into a form that can be gladly implemented by an appliance. The sender produces codeword out of dataword by using a generator system that puts in the order and form of encoding.

3.3 Summary

The system architecture we have designed is the main scheme for our project.

Chapter 4

Implementation and Results

4.1 Satellite on-board command data handling structure

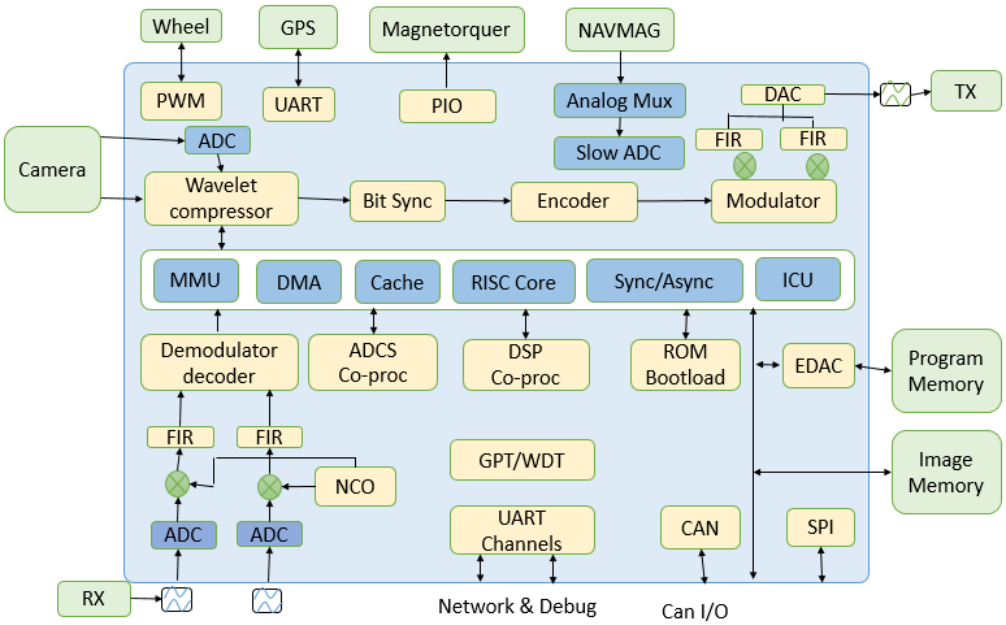

Figure 4.1: Satellite OBCHD ASIC structure

For a low-cost system of nano satellite a single chip implemented on-board command data handling (OBCDH) was proposed for a mixed mode application-specific integrated circuit (ASIC) [5]. Future Small Satellites which having data processing and control functions with data collecting and remote sensing capabilities for Earth observation Missions is the result of ASIC specification. Block diagram 4.1 consists of 4 Subsystems where a 32-bit RISC processor core modified for space use, Sub system of image handling unit, a communication connection for the satellite, and a supporting peripheral subsystem. OBC is the main components to miniature OBCDH system. To serve an initial prototype of the digital part of the OBCDH ASIC, this onboard computer system on a chip figure 3. In

the OBCDH our main priority is to upgrade the EDAC system so that we can have error free data on satellite communication.

4.2 Error Detection and Correction Mechanism V-1.1

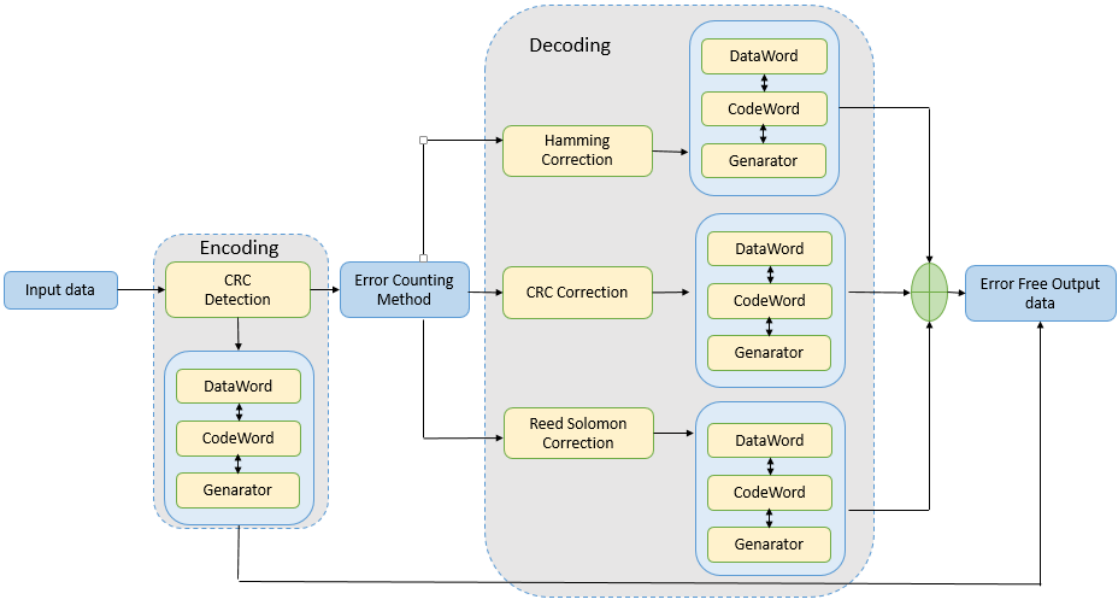

Figure 4.2: EDAC proposed algorithmic structure

Nanosatellites that transmitted data to the ground station from their errors can be checked with the help of some algorithms. In the ground station, CRC checks error data. After that step with a type of error, we can get the data specified by detection methods. In the detection methods, we figure out whether errors are present in our data if we can detect via three steps like data word codeword generator then we can identify the erroneous bit in the input stream shown in 4.2. Based on our errors we need to change our algorithms according to the size of errors. In this correction methods like Hamming correction, CRC correction, and Reed Solomon correction. With the help of these correction methods, we would now finally get our desired errorless data.

4.2.1 Algorithmic Analysis

Hamming code

Hamming code is a linear block code for error detection and correction. Hamming codes can detect one bit or two bits error at the same time and it can correct only single-bit errors. The main concept of the hamming code is to add a parity bit after the stream of data to verify that the data was received by the ground station and matches the corresponding input data stream. Satellite ground stations check the transmitted data in such a way that they identify where the error has occurred. The structure of the hamming code

has block length, message length, and distance. Block length defines as n = 2r − 1 where r >= 2 message length and distance is 2r − r − 1. Depending on the hamming code version distance value got changed. Due to adding more than one parity bit, this scheme can locate the position of the error and self-correct it by inverting the bit. Mostly three types of hamming codes are used in Nano-satellite communication such as Hamming[7,4,3], Hamming[8,4,4], and Hamming[16,11,4].

Cyclic Redundancy Check

CRC is the process of accepting emerging change errors in the communication channel. Nanosatellite data exchange is based on CRC codes and the EDAC process widely used in modern CRC code is also commonly referred to as polynomial codes -1 on a thin wire, by working on a thin wire is defined as polynomial counts. The k-bit message is considered a polynomial equation list with the words k, from $x^{(k-1)}$ to x^0. The highest order is the coefficient of $x^{(k-1)}$, the next item is the equivalent of $x^{(k-2)}$, and so on. Test digits are generated by repeating the k-bit message x^n and split the generated by $rm(n+1)$ bits polynomial code . The textit n -bit balance is passed as test digits.The complete collection sequence is divided by the same polynomial generator. If the remaining pieces are zero, no errors have occurred. If the remaining pieces are not zero, a transfer error occurred.

Reed Solomon

Reed Solomon codes are work with a burst type of data error. It also used as a broadcast system in satellite communication and also in storage system etc[13]. It detects the burst error of data transmission and corrects those error data. If the Reed Solomon codes are used then the probability of an error remaining in the decoded data will be much lower[14]. It mostly described in code gain. Reed Solomon codes are also suitable for multiple burst error correction codes as a sequence of $b+1$ consecutive errors can affect up to 2 signals of size b[15]. The t option goes to the code designer and can be selected over a wide range. Reed Solomon error correction is a forward-looking error code[16]. It works with polynomial samples of data. Polynomials have been tested in several places and these numbers are either transmitted or recorded.

4.2.2 Perfomance analysis of EDAC Structure

In this 4.3, we have designed as massage bits to parity check matrix then generator matrix and finally corrected code. At first define codeword bits per block, massage bits per block, parity sub-matrix, generator matrix and parity-check matrix. Encode message and find the position of the error in codeword (index). Then code modifies and corrected code. After all, remove error data then plot this figure.

In this 4.3, we have designed input and output messages with the help of CRC. At first, we take the input and generator matrix. Then find checksum. After find checksum

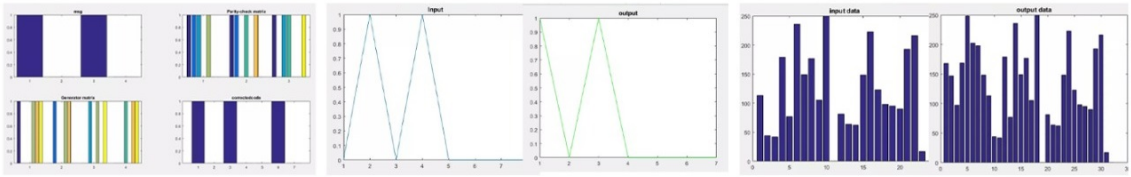

Figure 4.3: Perfomance analysis of Hamming code,Cyclic Redundancy Check and Reed Solomon Code

we add checksum to message bits then we check output is if the reminder is non-Zero a transmission error has occurred and reminder Zero no errors occurred. Then the plot output figure.

In this 4.3, we have designed Reed Solomon code as input and output messages. Reed Solomon code is used to correct the burst errors associated. This code is characterized by three parameters an alphabet size t, block length n, and message length k. Decoder characterizes this section use Reed Solomon code view of codeword as polynomial value is based on message encoded. The decoder recoups encoding polynomial from received message data.

4.3 Error Detection and Correction Mechanism V-1.2

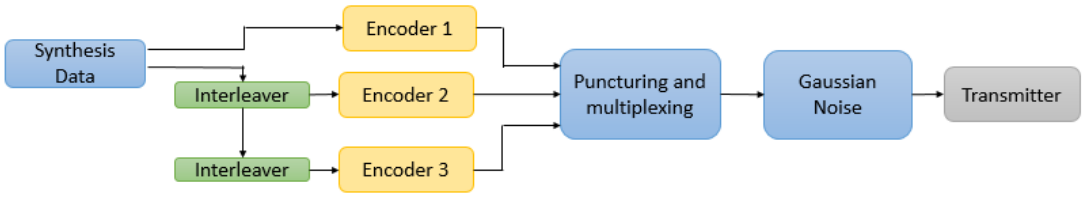

Figure 4.4: Advance Turbo Encoder mechanism for EDAC

4.3.1 Turbo Encoding mechanism

The Turbo Encoder block uses a parallel concatenated coding scheme to encode a binary input signal[17]. Three identical convolution encoders and two internal interleavers are used in this coding scheme 4.4. Each constituent encoder is terminated by tail bits autonomously. The previous block diagram shows that the performance of the Turbo Encoder block is made up of the first encoders systemic and parity bitstreams, and only the second encoders parity bitstreams. An interleaver is used between two systematic encoders of convolution as In Figure 8 seen. Here, we can hit a rate of 1/3, without puncturing and 1/2, with a form of puncturing[18]. Other code rates are also obtained by the process of puncturing. Turbo encoding process is tested with two different noise channels like AWGN Channel and Rayleigh Channel. The full communication system was maintained different bandwidth of satellite.

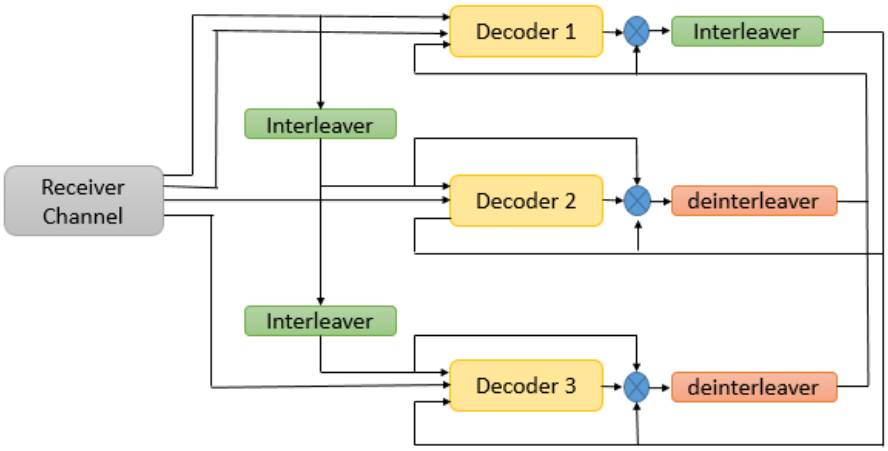

Figure 4.5: Advance Turbo Decoder mechanism for EDAC

4.3.2 Turbo decoding mechanism

Turbo decoder is applied when turbo encoded data is applied to Transmission over the AWGN channel via Base-Band, The Log-Map decoding structure offers less complex output similar to the limit of Shannon with less complexity. Turbo decoder consists of three interleaver and two de-interleaver separated SISO decoders, as shown 4.5 because of noise, encoded output data bit can get corrupted and entered the input of the decoder as r0 for the device bit, r1 for parity-1, and r2 for parity-2 and r3 for parity-3. Due to its powerful ability to correct errors, rational complexity, and versatility in terms of different block lengths and code speeds, memory element number, etc.

4.3.3 Perfomance analysis of Advance turbo mechanism

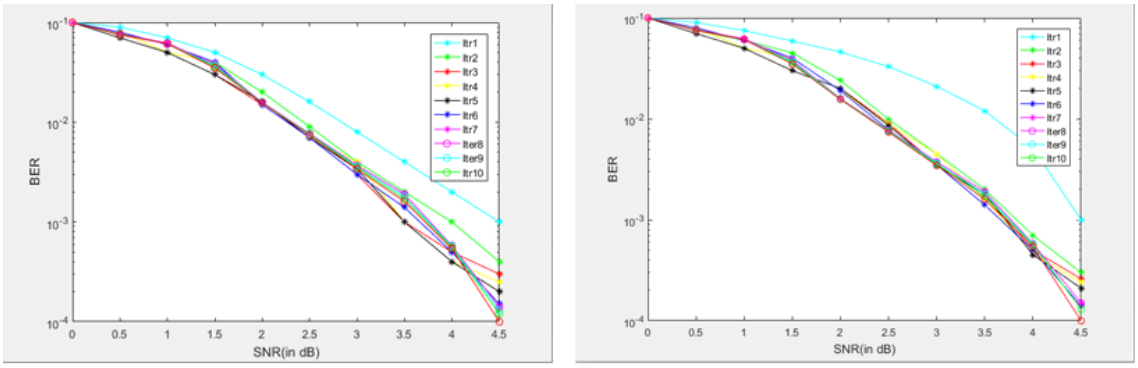

Figure 4.6: Performance analysis of turbo code Rayleigh Channel and AWGN Channel

Turbo codes are better performance codes that result from the interaction of information between recursive codes and decoders of the constitution. If the frame size is kept large and randomly selected, turbo codes can generate surprisingly low error rates at low SNRs. The more is the number of iterations more exchange of information between electoral encoders. As a result, the code can perform better. Turbo code simulated for Rayleigh faded channel for frame size $K = 40$. Frames number in each SNR taken as *500* to keep the simulation fast. Frame size was sent to get the BER at *40, 20000* by biting each SNR. SNR ranges from *0* to *5* dB were used. Iterations number of decoders chosen to be *10*. The BER for repetition is shown in 4.6. Turbo code achieved a BRR of *0.5 x 10-2* after the 1st decoder iteration. BRE improved to *1.34 x 10-4* after the 10th iteration. It can be seen that BRE performance increases as the number of iterations increases. However, the rate of advancement has slowed down. So the result is illustrated by the overlapping curve after the 5th iteration. BER *1.418 x 10-4* after *5* repetitions. BER did not show significant advancement after the 5th iteration. BER curve for frame size $K = 40$ on AWGN channel 4.6 BER for frame size $K = 40$ turbo code on AWGN channel. BRRT *3.628 x 10-4* after 1st decoder repetition. BER increases and decreases repetition at the end of 10th repetition BER *1.152 x 10-5*.

4.4 Error Detection and Correction Mechanism V-1.3

Five Identical EDAC algorithms are used as encoders LDPC, BCH, Turbo, Convolutional, Shannon's and for all the algorithms random interleaver are used in this coding scheme. Each constituent encoder is terminated by tail bits autonomously. An interleaver is Used between five systematic encoders of convolution as In 4.7. Here, we can hit a rate of 1/3, without puncturing and 1/2, with a form of puncturing. Other code rates are also obtained by the process of puncturing. The algorithm for decoding can be designed by either an A Probability posterior (APP) method or a method of maximum likelihood. Decoder consists of Five interleavers and de-interleaver separated SISO decoders, as shown 4.8

Because of noise, encoded output data bit can get corrupted and entered the input of the decoder as r0 for the device bit, r1 for parity-1, and r2 for parity-2, r3 for parity-3, r4 for parity-4, r5 for parity-5. They are fed to the first SISO decoder with these inputs. SISO first the decoder takes the obtained data bits as input, Sequence r0 and parity sequence r1 got, which is RSC generated encoder 1, Sequence of output results.

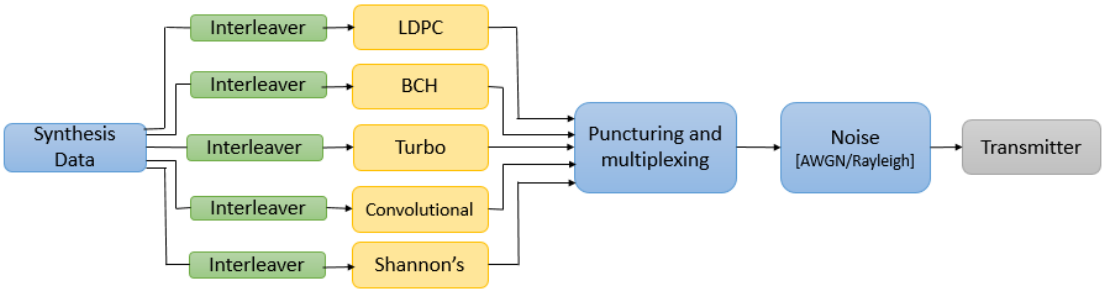

Figure 4.7: Hybrid approach of encoder mechanism for EDAC

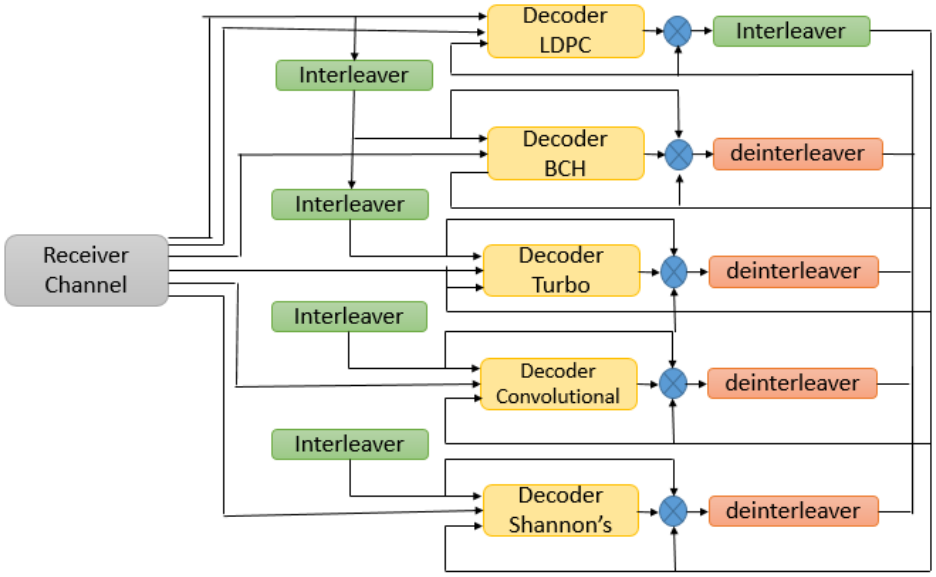

Figure 4.8: Hybrid approach of decoder mechanism for EDAC

4.4.1 Additive white Gaussian noise Channel

The Added substance White Gaussian Noise (AWGN) channel is one of the most commonly utilized channels demonstrate and is by and large utilized to show an environment with an exceptionally expansive number of added substance noise sources. Most added substance commotion sources in modern electronics are a coordinate result of zero-mean warm noise, which is caused by random electron movement inside the resistors, wires, and other components. The AWGN channel may be a well-known model to demonstrate the line of locate (LOS) conditions. This channel show is utilized to assess the contrast between a LOS show and a channel demonstrate counting fast-fading impacts. Consequently, the AWGN comes about can be seen as reference estimations.

4.4.2 Rayleigh Channel

The Rayleigh blurring model is in a perfect world suited to circumstances where there are huge numbers of flag ways and reflections[19]. Ordinary scenarios consolidate cellular broadcast communications where there's an expansive number of reflections from buildings and the like conjointly HF ionospheric communications where the uneven nature of the ionosphere suggests that the in general hail can arrive having taken various assorted ways. In this proposition, a moderate level autonomous Rayleigh blurring channel demonstrate is used for the blurring environment[20]. An autonomous Rayleigh blurring handle can be modeled as a steady irregular variable amid each image interim. In arrange to introduce the impact of the autonomous blurring channel, an arbitrary Rayleigh disseminated number is generated, to this number, we include the AWGN to mimic the total impact caused by the channel.

4.4.3 Low Density Parity check(LDPC)

Low-density parity codes are linear block codes. LDPC codes have shown a lot of attention errors performances impending the Shannon limit[21]. LDPC transmits a message bit over a noisy transmission channel. LDPC was established using a sparse Tanner graph. LDPC can be decoded block-length in linear time. LDPC codes are two classes: i) regular code ii) irregular code. A regular LDPC matrix is an N M binary matrix that has exactly one in each column and one in each row where ¡ and both are smaller than m. If H is low-density, then the number code of 1 in each row or column is called a random LDPC code if it is not continuous. The constant code is called the irregular LDPC code. It is also possible to see the regularity of these codes when viewing graphical representations. Each V-node and all C-nodes have the same number of incoming edges. The LDPC codes invented by Gallagher were regular codes. Both random codes show the best error work as N increases in the acceleration limit. The A load of code manages the hamming outpace among codewords increases as the number of entries increases. Hamming outpaces among two codewords is a defined number of separate locations in the codeword. LDPC code performance Near Shannon limit, LDPC code clean decoding method data-passing

and Low decoding difficulty. LDPC code Allows parallel implementation. LDPC codes have already been adopted as standards for satellite-based digital video broadcasting and long-hole optical communication, possibly acceptable to IEEE wireless local area network standards, and will be considered for the long-term evolution of third-generation mobiles. It is also used for 10GBase-T Ethernet Twist-pair cables that transmit data at 10 gigabytes per second[22]. One of the most popular topics in coding theory is LDPC codes. LDPC encoding difficult thing to implement. In the case of simulations, encode is done by multiplying the matrix, as most personal computer memory allocations can handle these activities by a large operation.

Low density parity check Encoder

LDPC encoding difficult thing to implement. In the case of simulations, encode is done by multiplying the matrix, as most personal computer memory allocations can handle these activities by large operations. Now determine how generated matrix G. We will use the following definition of the syndrome to determine the relationship parity bit with the H matrix. This definition is like a hamming code. Data bits multiplied and encoding applied with the help of a G matrix. G is a generator matrix of Low-Density Parity Check (LDPC) code is not requires an infrequent matrix[23]. A few design methods will be considered lower complexity of LDPC code encoding. The method is to apply the stair code. Introducing the ladder structure can be encoded at linear times as compared to repetitive decoders in H, only a single calculation is required to make the encoder effective by general multiplication. LDPC code design reversible data transmitted is used to LDPC encoder and decoder. Design circuits perform the aspect of the Tanner graph. The same circuits are using the encoding and decoding part. Such functions transfer a lot of promise in a function where the circuit area is limited.

Low density parity check Decoder

Best Effective decoders for LDPC codes can realize by applying repeat message-passing decoders[24]. LDPC code represents by parity check matrix H. Tanner's graph is a graph presentation of LDPC, parity matrix. Tanner graph using defined sets of nodes. 1st variable nodes refer to a single bit of valid codeword x with the length of the bits. The second set represents the checking node. Constraints. A flexible agreement trust extension decoder transmits the probability between checks nodes and variable nodes. This is data transfer local data using find solutions to a difficult overall complication with less complexity. However, for this type of application, it is necessary to save all the codewords that search for 2K codewords, which are increasing significantly[25]. Faith Promotion Decoder uses repeat messages to pass checks to search for codeword X and bit nodes.

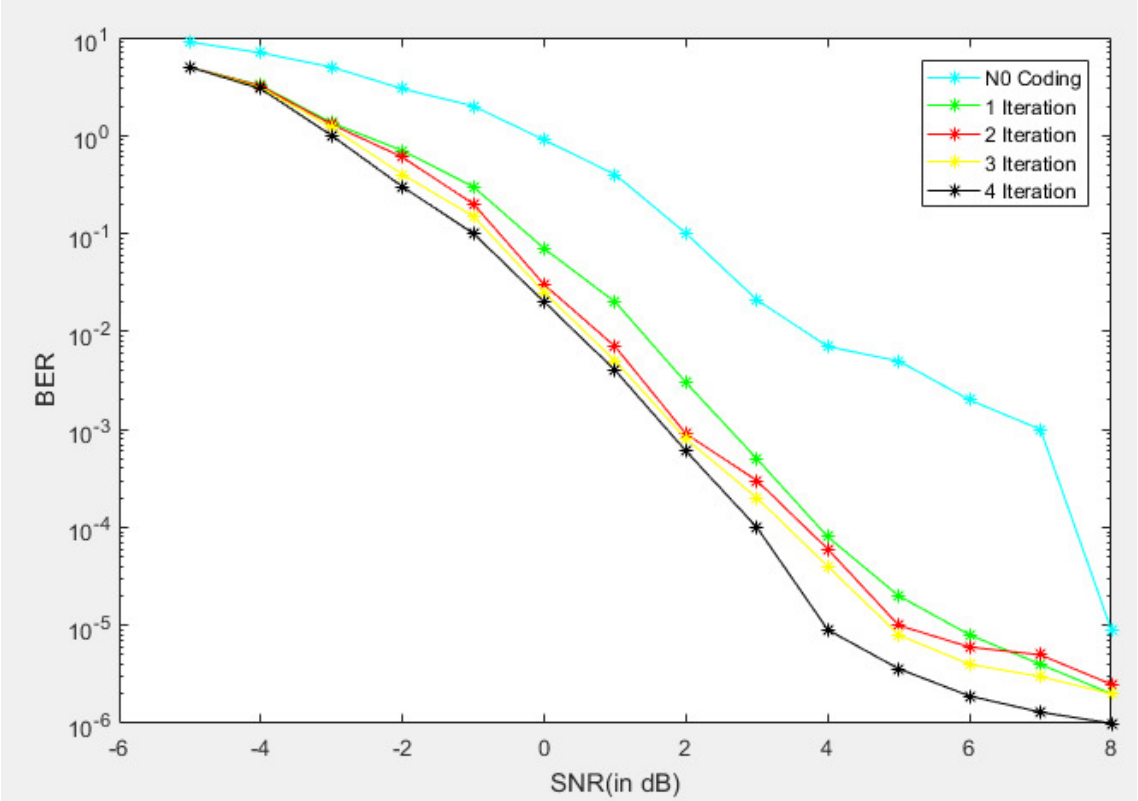

Figure 4.9: Performance analysis of LDPC code AWGN Channel

4.4.4 perfomance analysis of LDPC

AWGN Channel is considered to perform in the best possible way only reason to reduce the power of the channel[26]. The performance of LDPC on an AWGN channel in 4.9. Performance of LDPC codes 10^3 on AWGN channel at SNR = 0 dB and BRR $10^{-}1$ at the same SNR is not for any coding is higher than the original.

Rayleigh fading is considered the worst-case scenario as there is no effective way. Due to the functionality of the LDPC codes of the relay channel 4.10, multiple received signals are due to events such as reflection, scratching, and refractions[27]. For example, a comparison of curves in SNR = 5 dB implies that the code is BER 10^3 for coding and not BER $10^{-}1$ for no coding.

4.9 and 4.10 shows the effectiveness of LDPC codes on AWGN, Rayleigh channel. Here the curves are displayed at the same SNR = 2 dB BER, respectively $10^{-}4$, $10^{-}1$. The results show that the AWGN channel provides the best performance for the LDPC. It is almost impossible to encounter AWGN channels in real-life applications. In most cases, we have to consider the Rayleigh Fading system that should be built and keeping in mind the effects of the Rayleigh channel.

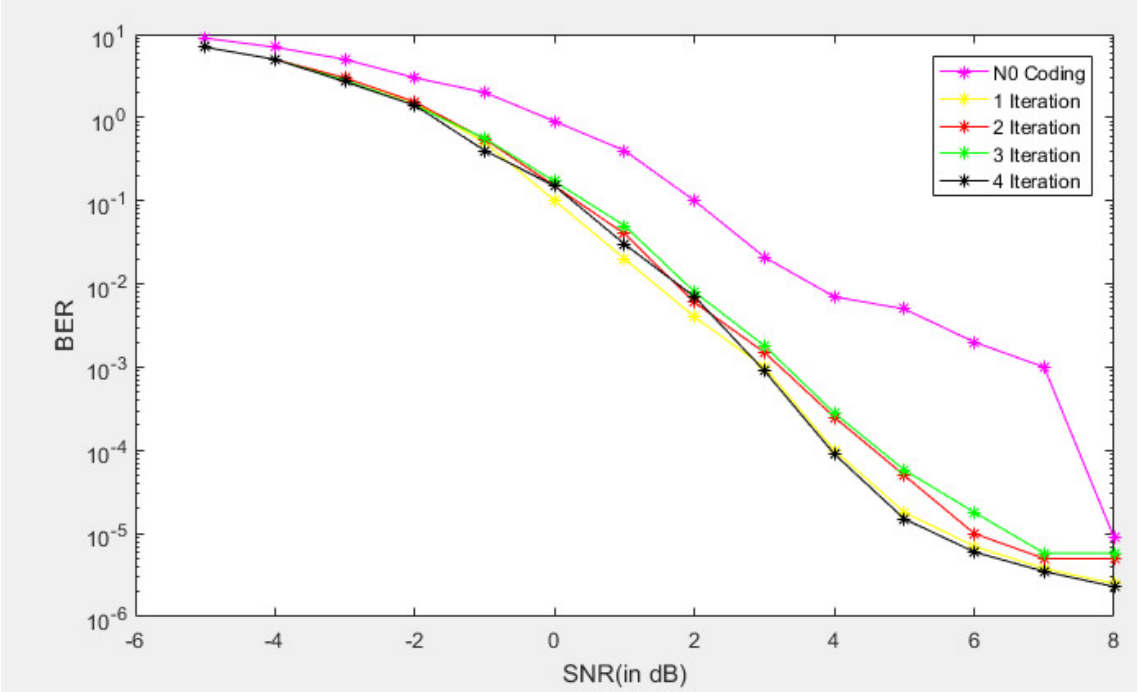

Figure 4.10: Performance analysis of LDPC code Rayleigh Channel

4.4.5 Bose Chaudhuri Hocquenghem(BCH) codes

The BCH codes give a wide assortment of straight lengths and comparing code rates. They are vital not as it were since of their adaptability within the choice of their code parameters but moreover since, at block lengths of a couple of hundred or less, numerous of these codes are among the foremost utilized codes of the same lengths and code rates[28]. Another advantage is that there exist exceptionally exquisite and effective arithmetical translating calculations for the BCH codes. The significance of the BCH codes too stems from the reality that they are competent in redressing all arbitrary designs of dread by an interpreting calculation that's both straightforward and effectively realized in a sensible sum of hardware. BCH codes possess an unmistakable put within the hypothesis and hone of multiple-error rectification.

BCH Encoder

Codewords are shaped by including leftover portion after divided the message polynomial with generator polynomial. They're products of the generator polynomial. On the encoding side, the generator polynomials are not ordinarily part because they will request more equipment and control circuitry. The polynomial is utilized as such for encoding[29]. The generator polynomial for BCH is given by $g(x) = (1 + x^3 + x^4 + x^5 + x^9 + x^12)$ BCH codes are executed as efficient cyclic codes. Consequently, can be effectively actualized and the rationale which actualizes encoder and decoder is controlled into move enroll circuits. The leftover portion can be calculated within the (n-k) straight arrange move registers

with the input association at the coefficient of the generator polynomial. BCH codeword is encoded as takes after: Amid the 1st clock cycle, m50 is given as input to the move enrolls. LFSR is initialized with seed esteem 0.

BCH Decoder

The interpreting handle of the BCH codes comprises three steps. At, to begin with, the disorder computation prepare creates 2t disorders from the gotten codeword which is the data information concatenated with the equality information. At that point, the blunder locator polynomial is computed from the disorders, of which the roots point out the blunder positions. Inevitably, by thoroughly finding out the roots of it utilizing the Chien look calculation, the mistakes are adjusted. In the event it demonstrates to be no blunder within the square, we require not one or the other to assess the mistake locator polynomial nor conduct the Chien look handle. In this way, for decreasing the interpreting time, it is exceptionally important to recognize whether there's any blunder or not as early as conceivable. Here, we propose to check the mistake event with a disorder polynomial by reusing the encoder which as it were requires the GFD, whereas the routine blunder location strategy employments the disorder values which require a much longer time for conducting a few diverse CGFMs.

4.4.6 Perfomance analysis of BCH Code

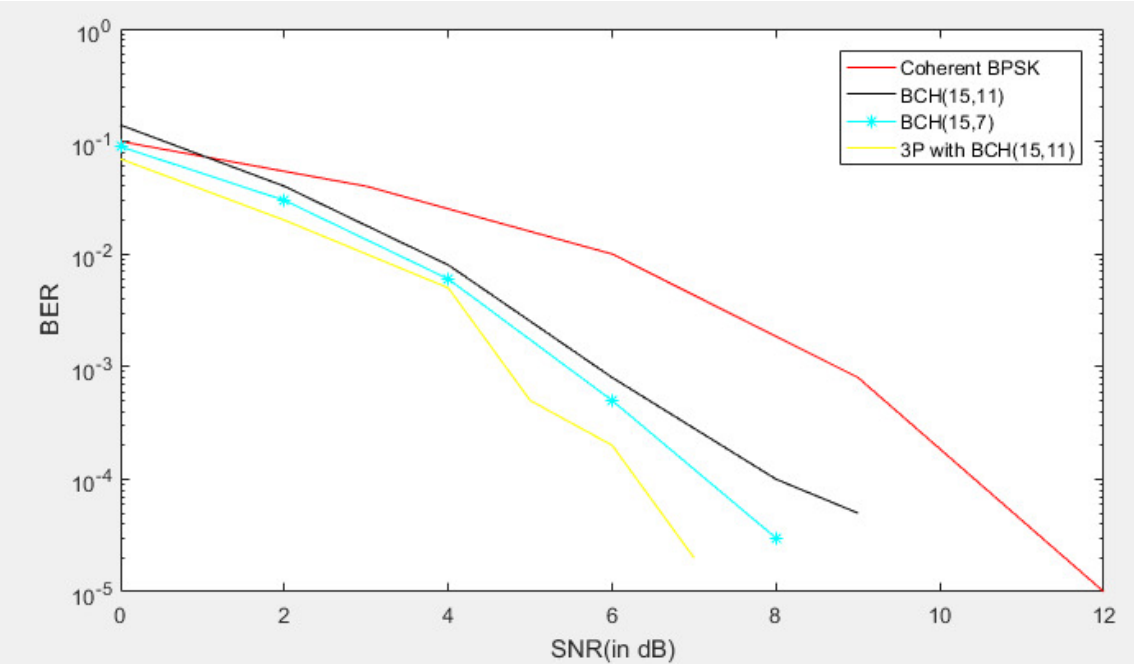

Figure 4.11: Performance analysis of BCH code AWGN Channel

4.11 and 4.12, shows the BER plots vs. threshold SNR ft. for BCH code for two values of average SNR 0, 10dB and 20dB, with different Doppler frequencies. From the figures, it

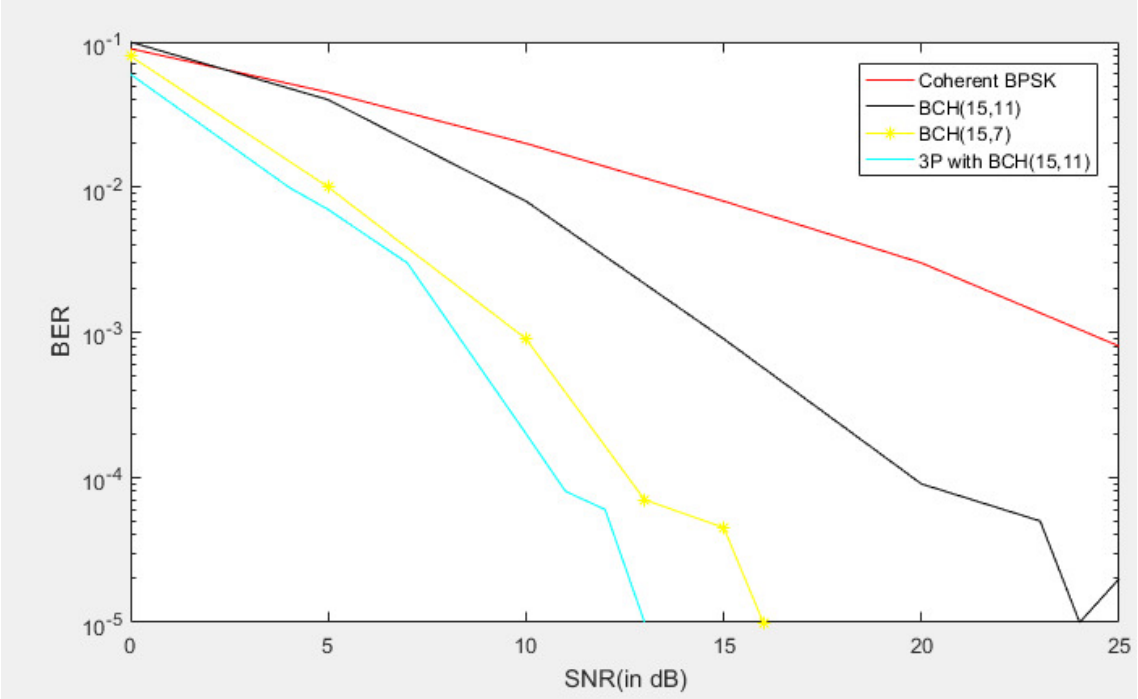

Figure 4.12: Performance analysis of BCH code Rayleigh Channel

is clear that an increase in the performance of the BCH code occurs and for large values, the errors tend to be more random as the transition probabilities b and g increase leading to good performance since the BCH code is capable to correct such random errors.

4.4.7 Convolutional Codes

In later a long time, the request for mixed media applications over remote portable communication frameworks has developed exceptionally quickly. Remote versatile communication systems show a few plan challenges coming about from the versatility of clients throughout the framework and the time-varying channel. One of the most targets when transmitting data over any communication channel is unwavering quality, which is measured by the likelihood of redress reception at the recipient. Convolutional codes on the other way are one of the preeminent broadly utilized channel codes in down to earth communication systems. These codes are essentially utilized for actual time botch correction. Convolutional codes alter the total data stream into one single code-word. The encoded bits depend not as they were on the current k input bits but in addition on past input bits. As a result of the wide affirmation of convolutional codes, there have been numerous signs of progress to extend and make strides in this basic coding plot. Convolutional coding may be a broadly utilized coding technique that isn't based on pieces of bits but or perhaps the abdicate code bits are chosen by basis operations on the appear bit in a stream and a small number of past bits.

Convolutional Encoder

Insides the encoder, data bits are input to a move enlist of length K, called the elemental length. As each bit enters at the cleared out of the select, the past bits are moved to the proper in show disdain toward of the truth that the primary orchestrated bit insides the select is evacuated. Two or more twofold summing operations, let's say r, make code bits that leave inside the center of one data stream period.

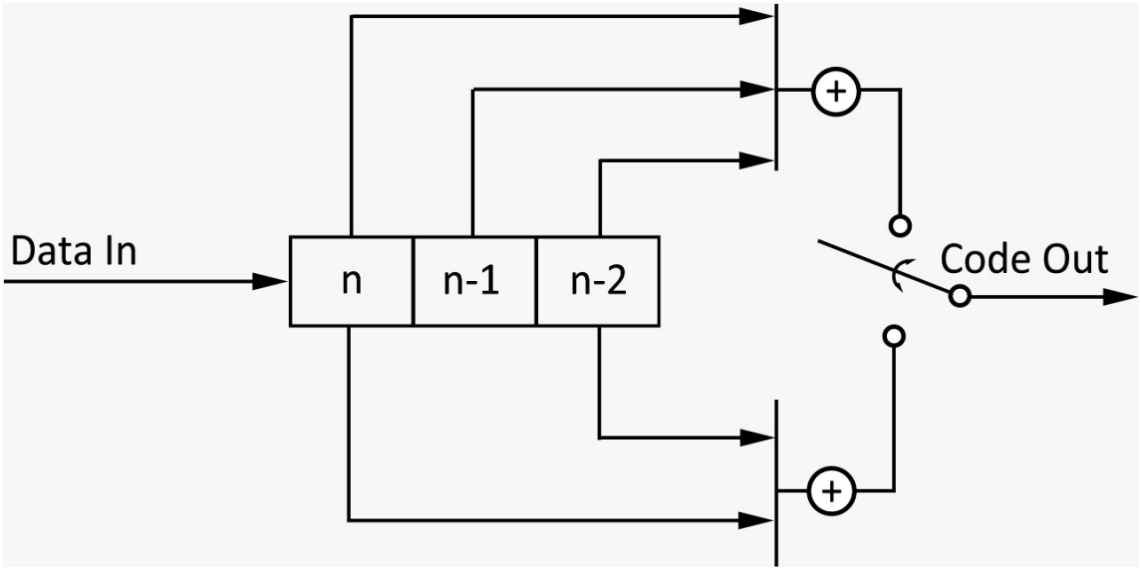

Figure 4.13: Convolutional Encoder System

In this way, the code bit rate is 1/r times the data rate, and the encoder is called a rate 1/r convolutional encoder of confinement length K. Also required to completely characterize the encoder are the affiliations from stages insides the move select to the r summing squares. These are generator vectors each of which may be on a very basic level communicated as a push of K parallel digits.

State diagram

Convolutional encoder shows up an outline with K = 3, r = 2, and the generator vectors are chosen as [1 1 1] and [1 1]. Discrete looking at times are labeled n. The data stream enters on the cleared out and the show bit at time n, the first afterward bit n 1 and the taking after a most reliable bit at n 2 have the move to enlist. Two balance bits are traded out inside the between times between n and n 1 from the upper snake and after that the lower one. When the taking after data bit arrives, the move select moves its substance to the proper. The K 1 earlier bit, in this case, two, choose the state of the encoder. They have appeared up in gray in 4.14.

Convolutional encoder There are 2K 1 states. For each encoder state, there are two conceivable comes about of yield code bits, depending on whether the input bit is "zero" or "one." The advancement of states in time, at that point, can be a work of the information

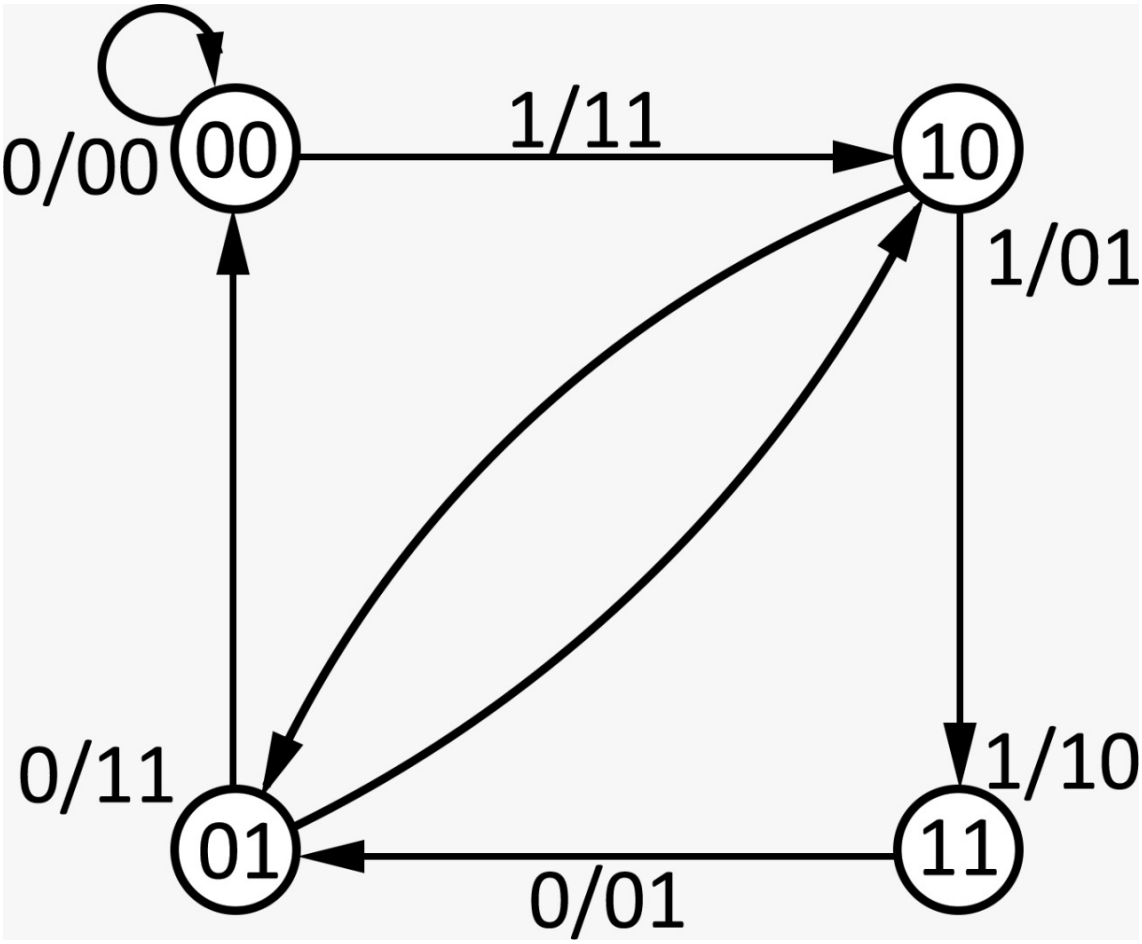

Figure 4.14: State diagram of Convolutional Code

stream. 4.14 statechart may be a state chart of our layout the development of states in time, at that point, may well be a work of the information stream. Fig. State chart may be a state chart of our diagram. Each state is appeared up insides of a circle and the alter from one state to another is showed up by a jar, recognized by the input bit, cut, yield code bits. You will be able to see that encoding can be done by and huge clear equipment.

Convolutional Decoder

Convolutional codes are frequently alluded to as 'trellis codes' due to the reality that trellis charts can effortlessly portray them. The trellis chart of a code records the diverse states of the encoder and the ways they are connected to. The trellis structure for the state diagram of 4.15 state diagram. is appeared in 4.16. Trellis structure for a four-state encoder. There exist two unmistakable approaches to translate a transmitted arrangement of bits. The begin with approach finds the foremost likely bit when they got incorrect grouping is known and is accomplished by.

The Viterbi calculation can be utilized by utilizing two primary procedures. The primary approach employments the difficult choice on the received noisy data bits by

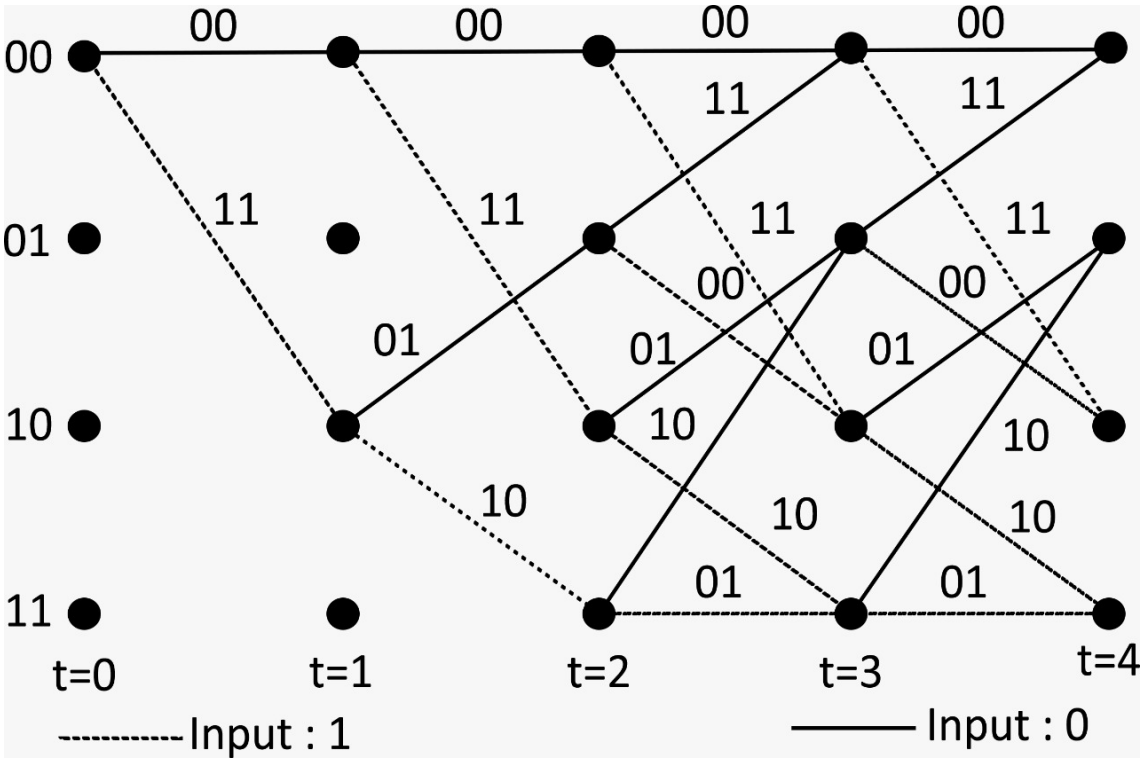

Figure 4.15: Trellis structure for a four-state

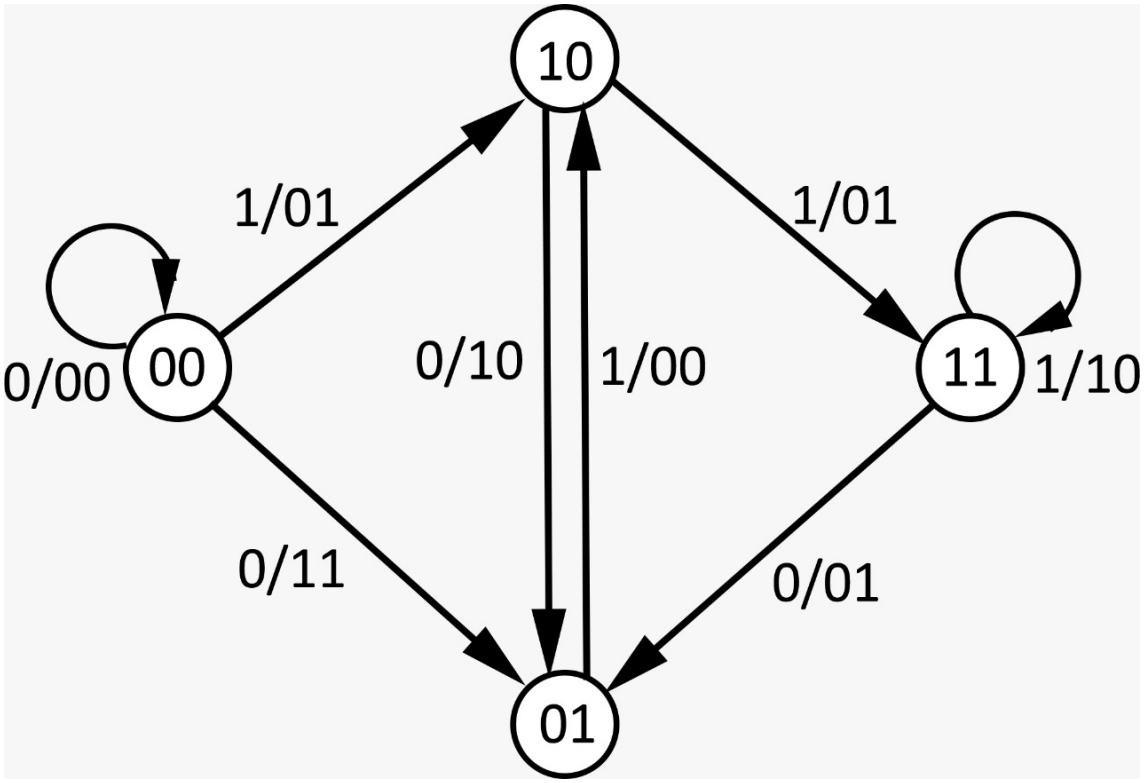

Figure 4.16: State diagram of Convolutional Code

thresholding the information to parallel digits and after that applying the calculation, whereas, the moment approach employments delicate choice to translate the information by finding the way among all the ways of the trellis which has the largest metric. Here we are going as it discussed the delicate choice approach. This approach not as it included an execution advantage over the difficult choice approach but, too will be accommodating within the taking after chapters.

4.4.8 perfomance analysis of Convolutional code

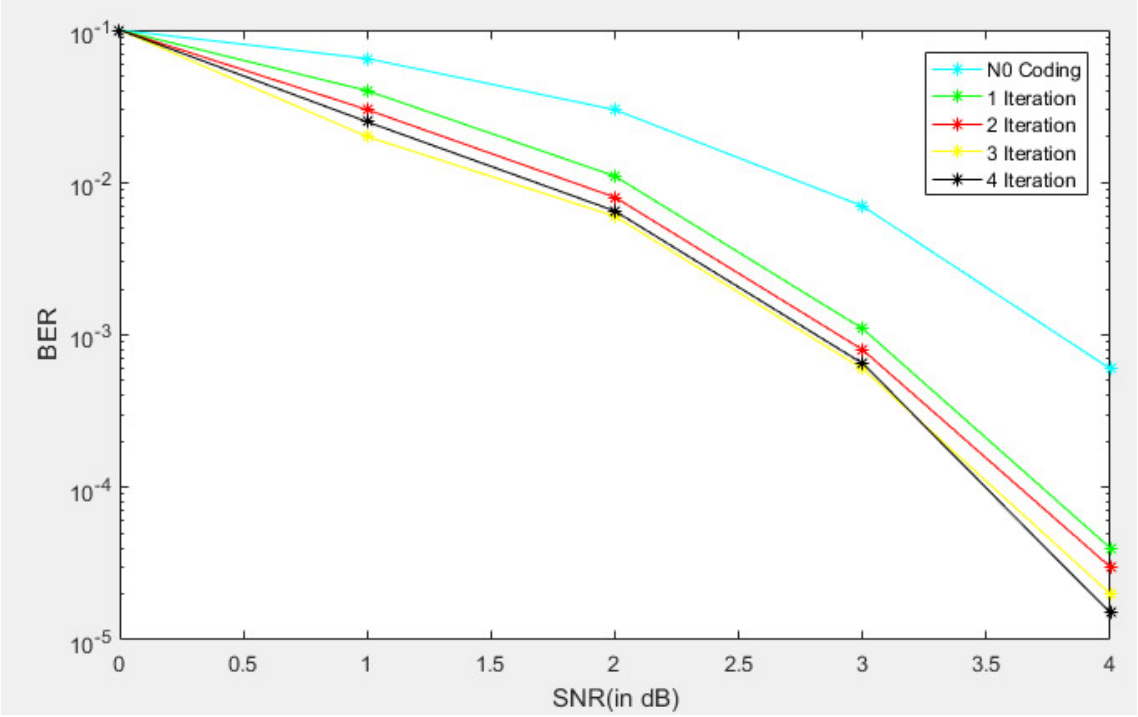

Figure 4.17: Performance analysis of Convolutional code AWGN Channel

For the event, at an SNR regard of 5dB, a bit botch rate of 10-5 was getting. That's, in this regard, 1 bit gotten in a blunder for 100000 bits sent. This was far off predominant to when the SNR was 2dB with a bit bumble rate of 10-1. That's 1 bit gotten in botch when 10 bits were sent. For the theoretical BER, the SNR ranges of 2dB, 2.5dB, and 3dB had a bit botch rate of 10-1 whereas inside the mirrored BER the SNR was observed to be of the expand 2dB, 2.5dB and had the same regard of BER of 10-1 whereas the SNR of 3dB of the imitated BER had an advanced BER of 10-2. This was as a result of the convolution coding displayed. Another characteristic was gotten by considering the incline of the hypothetical and imitated regard gotten as in 4.17 and 4.18.

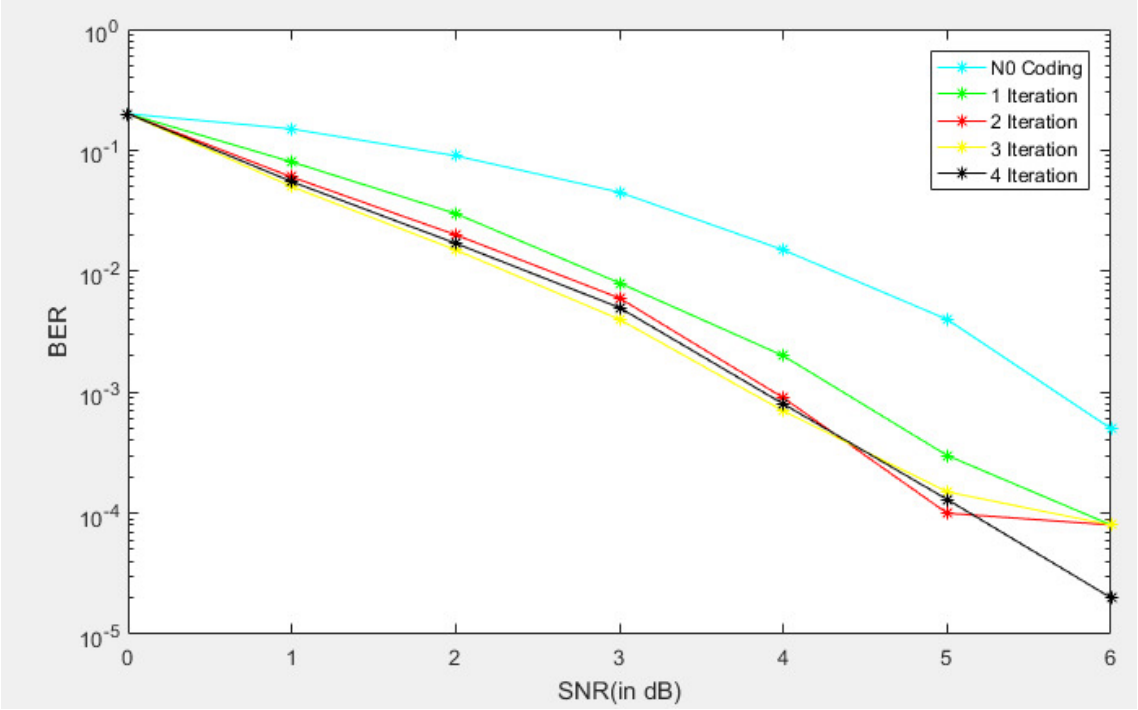

Figure 4.18: Performance analysis of Convolutional code Rayleigh Channel

4.4.9 Shannon's Theorem

Shannon's Encoding

The yield of a source is first handled by an encoder, which changes over the message from one arrange to another, ordinarily a double stream, for more proficient transmission or capacity of the data. The yield of the encoder is alluded to as a flag. There are two essential forms that an encoder can execute: source coding and channel coding. On the other hand, the objective of channel coding is to include or present additional repetition in arrange to account for conceivable unsettling influences or commotion that will influence the data amid transmission or capacity[30]. The included repetition increments the length of the flag but permits for more prominent location and adjustment of mistakes amid the translating prepare. Common causes of channel coding incorporate the utilize of equality check bits and redundancy codes. An equality check bit is essentially an additional bit that's included in a twofold sequence such that there's an indeed number of 1's. If an arrangement with an odd number of 1's is gotten, at that point, the decoder can identify that a blunder has happened amid transmission through the channel. A reiteration code basically rehashes the message a certain number of times in trusts that the clamor within the channel would degenerate as it were a little division of the flag. A common, ordinary illustration is the case of human discussion wherein the audience cannot get what is being said, so the speaker essentially rehashes what was said.

Shannon's Decoding

The yield of the channel is at that point gotten by a decoder, which attempts to change over the gotten flag back to the first message. At that point, at long last, the yield of the decoder is sent to the ultimate client or goal, which is alluded to as the data sink. W speaks to a message. We'll regularly consider that it is the yield of the compressor. The encoder gets W and encodes it to Xn. The encoder puts Xn into the channel and Y n is the yield the decoder gets. At long last, the decoder tries to appraise W through Y n. The decoders appraise is signified by Wc. Our objective is to get what kind of encodings are such that Wc is the same as W with tall likelihood and n is as little as conceivable.

4.4.10 Performance Evaluation of shannon's theorem

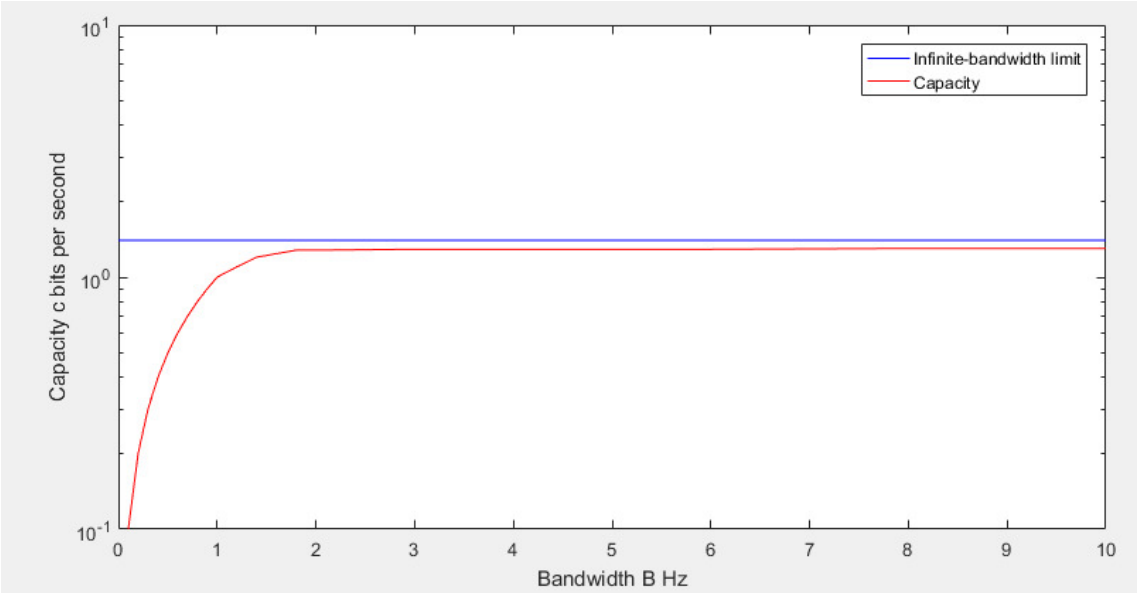

Figure 4.19: Performance analysis of Shannon's theorem AWGN Channel

In this 4.19 and4.20, AWGN Channel and Rayleigh fading we used Shannon Theorem. Higher theory a scale that can be loaded with a BER, with an enabled central signal, above the B Hz bandwidth affected by the channel. By the term "unfairly BER" means that it has provided conditions for the theorem is met, in any given BER, no matter how small, we can find the coding process that benefits this BER; the smaller the BER given, the harder it will be processed. The least accessible bit rate is called channel capacity C. S / N is a square signal that means the sound ratio, and the logarithm is in phase 2

4.5 Results and Discussion

In analytical 4.21 and 4.22, we apply two types of noise Rayleigh Channel and AWGN channel for all algorithms. AWGN Channel is considered to perform in the best possible way only reason to reduce the power of the channel. Rayleigh fading is considered the

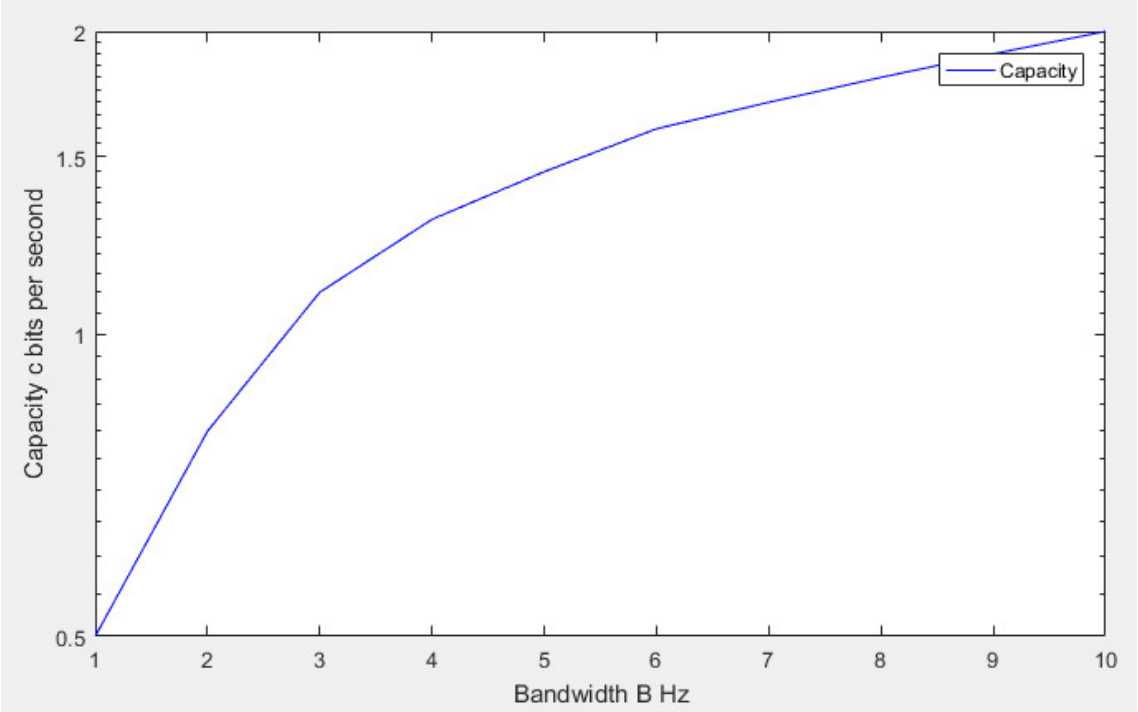

Figure 4.20: Performance analysis of Shannon's theorem Rayleigh Channel

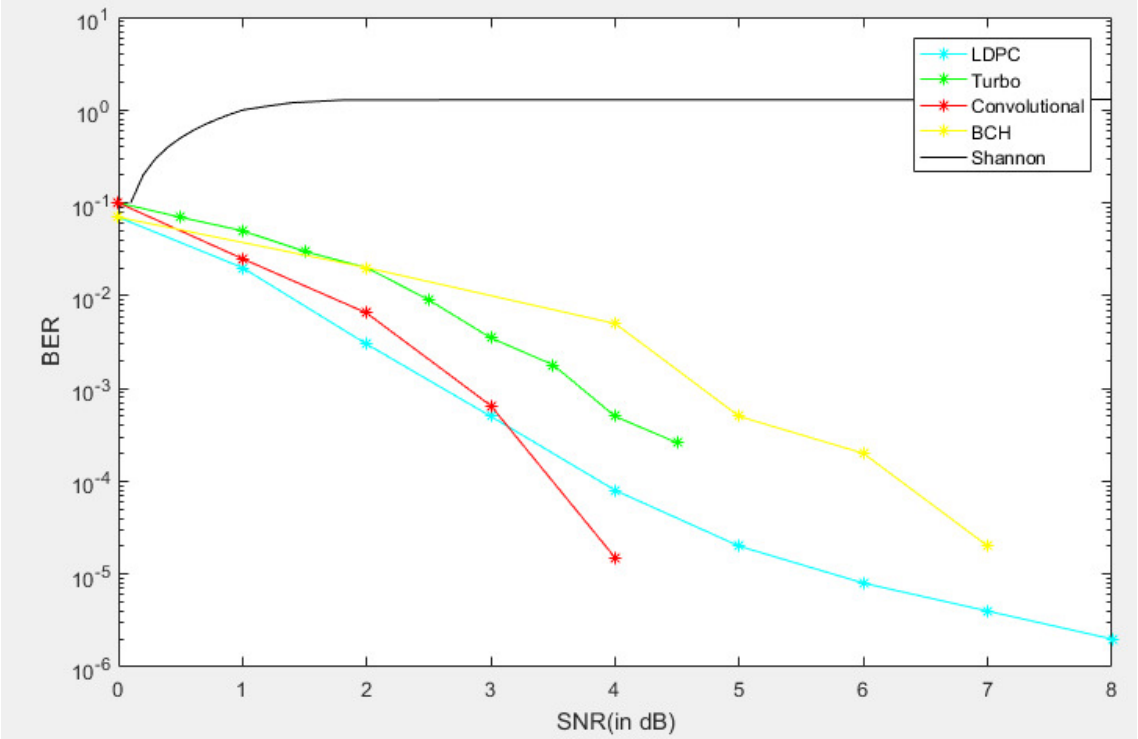

Figure 4.21: Performance analysis of hybrid approach for EDAC AWGN Channel

worst-case scenario as there is no effective way. Here we can see that LDPC, Turbo, Convolutional, BCH, and Shannon's Theorem this algorithms are best performing for different types of data. Some algorithms are good for fewer data and some algorithms are

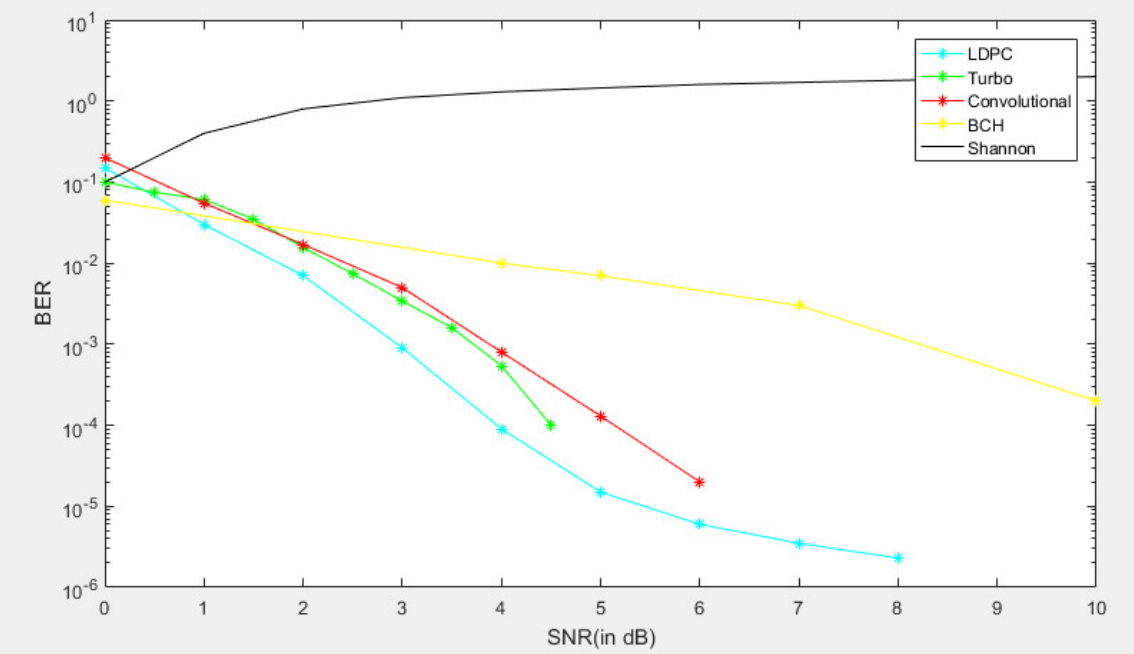

Figure 4.22: Performance analysis of hybrid approach for EDAC Rayleigh Channel

better for more data. LDPC works better when signal noise is increasing. Convolutional code works best when signal noise is medium and bit error ratio $10^{-}3$. LDPC works better for the AGWN channel. We transmitted data continuously in machine learning techniques and which type of data is best for which algorithms and identify more error data and remove error data in less time.

Chapter 5

Standards and Design Constraints

There are some specific standards that need to be maintained. During the development process of our project we might encounter various ethical constraints and designs. It is necessary to follow every principle. In this chapter, we will reflect an elaborate discussion on Standard and Design constraints.

5.1 Compliance with the Standards

We will be following these different standards through out the project.

5.1.1 Technological Standard

In figure 5, we have discussed about the necessary technological standards that we plan to implement in our research. We are using Latex as the markup language. For the programable Language we plan to use Verilog or Python. Verilog is a Hardware Description Language (HDL) which is applied in describing digital system (Network Switch, flip-flop or microprocessor etc.) and Python is an interpreted high-level programing language. Software like Xilinx Vivado and MATLAB will be used for Graphical simulations of algorithms and they are convertible in Web formats. On the other hand, PyCharm provides support for Python language. System interface and analysis can be performed thorough this high-level interpreter. Simulation and every algorithmic analysis will be processed

Programming Language	Verilog, Python
Software	Xilinx Vivado, MATLAB, PyCharm
Markup Language	Latex
ISO	ISO/IEC27001
Processor	Xilinx Spartan 6

Figure 5.1: Figure 5: Technological Standard

via Xilinx Spartan 6 processor. We are abiding by Information Security Management or ISO/IEC 27001 as ISO family standards.

5.1.2 Communication Standard

Communications	USBv2.0 (universal serial bus), Wireless- 802.11b
Data Format	Bitmap (Image), JPEG Compression (Image)
Connectors	USB, RCA, Mini-jacks, Ribbon/Pin

Figure 5.2: Communication Standard

5.2 is about Communication Standards. We will be using both wireless connections Wireless- 802.11b and wired connections such as USBv2.0. For stable connections among the hardware we will be using USB, mini-jacks and Ribbon/pin as connector. For best data format we will using Bitmap image because it is small in size and easy to be transmitted.

5.1.3 Internet Standard

As we label our research topic as Data Communication problem therefore the internet is required. We will be abiding by few RFC standards to prioritize internet standards. RFC 1122 is used for internet hosts- communication layer, RFC 1123 is required for Internet Host-Application and support, RFC 919 is used for Broadcasting Internet Diagrams and RFC 6522 is used for reporting media type, the Reporting of Mail System Administrative message 5.3. This following standards use ASCII, PDF and HTML types of files. RFC 6409 is used in message submission for mail and use ASCII, PDF, HTML, HTML with inline errata type files.

STD	Number	Files	Title
STD 3	RFC 1122	ASCII, PDF, HTML	Requirements for Internet Hosts- Communication Layer
STD 3	RFC 1123	ASCII, PDF, HTML	Requirements for Internet Hosts – Application and Support.
STD 5	RFC 919	ASCII, PDF, HTML	Broadcasting Internet Datagrams
STD 72	RFC 6409	ASCII, PDF, HTML, HTML with inline errata	Message Submission for Mail
STS 73	RFC 6522	ASCII, PDF, HTML	The Multipart / Report Media Type for the Reporting of Mail System Administrative Message.

Figure 5.3: Internet Standard

5.2 Design Constraints

In this section, we will highlight the impacts based on our research and gather all the ethical, social constraints that are relevant to our systems.

5.2.1 Economic Constraint

Revolution is happening in space technology day by day. Its impact will be life-changing, but it is happening silently and sometimes suddenly. Nanosatellites can bring revolutionary changes in business and human life. Nanosatellites cost less than traditional satellites. So, the demand for nanosatellite is getting higher. People are realizing the impact of nanosatellites to transform businesses and human life, that's why the capacity of this technology is doubling every year.

5.2.2 Environmental Constraint

Our project has some impacts on the environment. The satellite data transfer communication system consumes less than 50 percent power than the traditional data transfer communication system. It does not have that much affects on our ecosystem, but microwave frequencies of satellite produce radiation. Satellite monitors the climate changes of Bangladesh, monitoring the structure of Sundarbans and estimate biomass. The uses of satellite communication will reduce the wires of the cable communication systems from the city, which will have a great impact on the environment.

5.2.3 Ethical Constraint

Our satellite has no ethically questionable decisions. It cannot be used for unfair means as our project is a unique one. The users must treat fairly because of the terms and conditions satellite communication system.

5.2.4 Health and Safety Constraint

The health threats are negligible for nanosatellites. In our system, the data privacy of users will be ensured.

5.2.5 Social Constraint

The satellite has a great impact on society because it will work with high-speed internet and networking. It has a long term impact on society. Satellite is socially acceptable everywhere.

5.2.6 Political Constraint

Our project completely depends on government approval.

5.2.7 Manufacturability and Cost Analysis

Building a nano-satellite EDAC method is not an easy job as it depends on both hardware and software5.4.

Serilal	Particular	Description	Provider	Amount(BDT)
1	Hardware	Spartan-6 FPGA Evalution kit	Xillinx	৳52,000.00
2		Camera ov2640 (6 pc)	Arduino	৳10,000.00
3	Designing	Work hour: 24 hours	Outsource	৳16,000.00
4	Developing			
5	Reviewing			
6	Testing			
7	Deploying			
			Total	৳78,000.00

Figure 5.4: Satellite EDAC system budget and cost analysis

5.2.8 Interaction with the stakeholders

Functional Requirements

1. User(Cable and network company, Telephone company, Business Finance company, weather company, SPARRSO, Bangabandhu satellite etc.) they are register and active our system.
2. The system establish a communication link with the ground station.
3. The System be able to provide high processing power.
4. The system receive data bit and detection error used CRC method and correction bit used Hamming code, reed Solomon code, parity check method.
5. The System provide variable bits data rates. These rates shall be selectable by which correction method is suitable.
6. The system is provide precise local timing and time synchronization.
7. The system monitor battery charge level. In case of an out of limit condition, OBC will initiate satellite safe mode.
8. The system keep a list of commands which will be executed automatically in case of an emergency.
9. The system limited budgets, and short development, time 4 years.

Non-Functional Requirements

1. The system Users privacy should be protected.
2. The system should have 100 percent error free data information.
3. Information of users can be stored to maintain security.
4. The system different kind of admin they all will have some individual controlling

features. Super admin will give these access permissions to the other admins.
5. The client can only use the provide system, but client cannot change data information.
6. The User need hardware and software devices for his own to use the system.
7. The system sent image data, bits data, to process work.
8. The system first received data from sender than detection error counting method count bits rates. These bits rates shall be select able by which correction method is suitable.
9. After correction data ground station distribute data for system users.

5.2.9 Interdependence

Essentially, the hardware is controlled by the software/IDE. In our project, we have focused on Xilinx Vivado, MATLAB, and PyCharm as the software. On the other hand Spartan 6 FPGA processor and a computer as the hardware. Among the Software's, Xilinx is used for graphical and numerical analysis which uses the Verilog language. Alternatively, MATLAB can be used for similar outcomes. Pycharm is suitable for interface design using the Python language. From the hardware, the Spartan 6 FPGA will be used for data processing and a computer for monitoring the operation. When a dataset is inputted in the software/ IDE on EDAC based algorithm (Hamming Code, CRC, Reed Solomon, Parity Check, lDPC, BCH, Turbo code, Convolutional and Shannon's etc.), the FPGA runs the detection algorithm and computes the Faults from the data, and applies the correction method, and returns both graphical and numerical outputs. This output can be viewed from the Computer.

5.2.10 Impact after the implementation

If our system is used then the data transfer errors will be reduced, it will become more reliable and a safe data transmission system will be built. Satellites are bringing changes in the country's economy and GDP growth by providing the largest number of telecommunication services. It boosts the country's economy, makes the nation more aspirant and creates more job fields.

5.2.11 Sustainability

Our project is a software and hardware and software based project. But sustainability and durability will depend on many factors. This project hardware system has a lifetime but software system has no lifetime.

5.3 Summary

We have followed certain types of rules and standards for our project. These standards and constraints are efficient in accomplishing our research project.

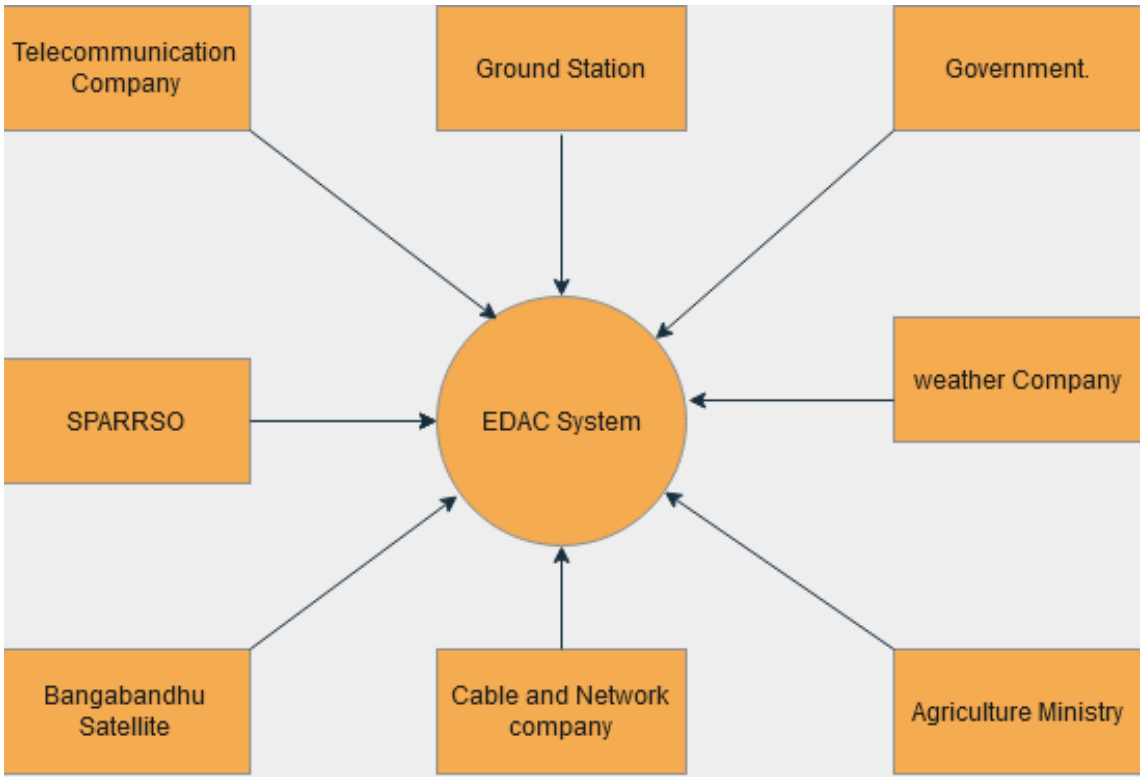

Figure 5.5: Context Diagram

Chapter 6

Conclusion

In this paper, we focused on different EDAC techniques. At the same time with a code correlation to the study was regulated. This application came up with the editor with a good concern of all regular EDAC techniques. That is especially helpful should distinct EDAC ability be required. The prototype can be expanded or EDAC of multiple bits defect by using other more complicated error detecting and error-correcting codes alter Turbo Code, LDPC, BCH, Shannon's Theorem, Reed Solomon codes, etc. The ground of nanosatellites is continuously maturing and growing in an impressive way. This is scheduled for the law that gives a plan of action from which the perimeters of space and technology are regularly being forced. The automation progresses memory chip cell architecture is becoming more and more solid, principally with the evolution of nanotechnology. As organizes an increasing requirement for a more developed and dependable EDAC system that is efficient in preserving the memory attitudes of nanosatellites.

LDPC adds to additional bits per conversation that have been transmitted through the satellite data transmission system. An LDPC cannot detect all types of bits error. Turbo Code affects single bit error correction and also detects multiple bit errors. If multiple bit error detection in this code but turbo code can only solve single bits error correction. A BCH is not suitable for security purposes. The error correction BCH alone will be a useless thing. It is more complex than a checksum and takes more processing. A strong BCH might run slowly in software. But Reed Solomon codes are not efficient as BCH codes. It cannot provide satisfying performance without BCH codes in BPSK modulation schemes.

In the future, we will introduce an advanced error detection method based on satellite transmitted data. Depending on data size, type, and importance detection algorithms will be changed. It will reduce the time of the EDAC process and get reliable safe data in a faster way. We training your system for real-time simulation. Predicted the less error mechanism in a different type of data. We will use the machine learning technique to find less error paths. Implementing the ASCI architecture in Spartan 6 FPGA. After all, we collaborating our system architecture with Bangabandhu Satellite-1.

This report represents a hybrid approach to EDAC algorithms of nanosatellite data

transmission systems. Xilinx software is used for checking the EDAC algorithm's performance. We evaluated the performance based on camera ov2640 real-time data to check the error detection and correction process. In error detection methods, it detects the error bits. Then error counting method will decide based on error types which algorithm is suitable for the error correction method.

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