9. Foundations of processor design: memory elements

EECS 370 – Introduction to Computer Organization – Winter 2015

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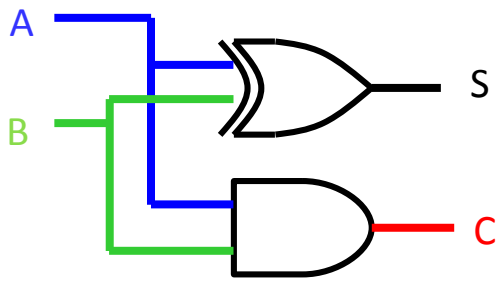
Recap: Combinational Circuits – implement Boolean expressions

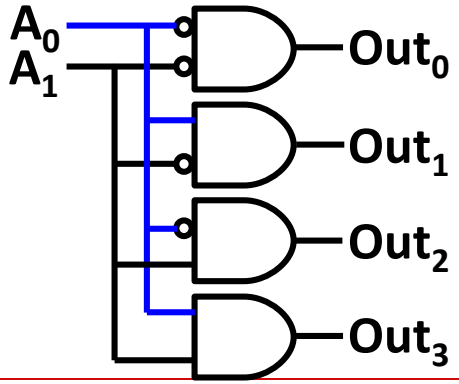
- **No memory**: Output a function only of input
- Undefined input implies undefined output

  - Adder is the basic gate of the ALU
  - Decoder is the basic gate of indexing
  - MUX is the basic gate controlling data movement

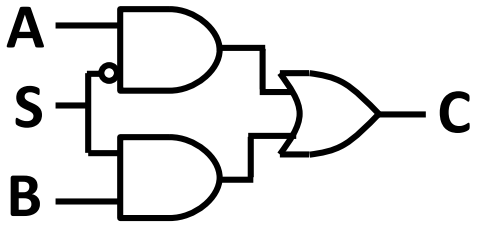
Half Adder



Decoder



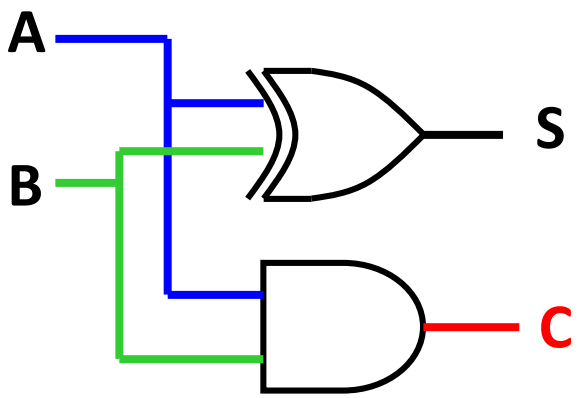
MUX



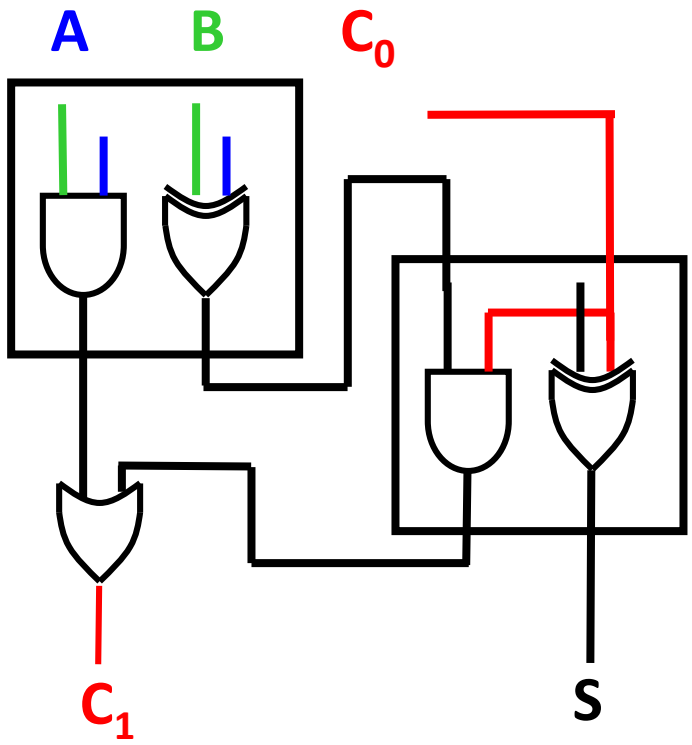
Recap:
Building combinational circuits: Half and Full adder

Half Adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Full Adder

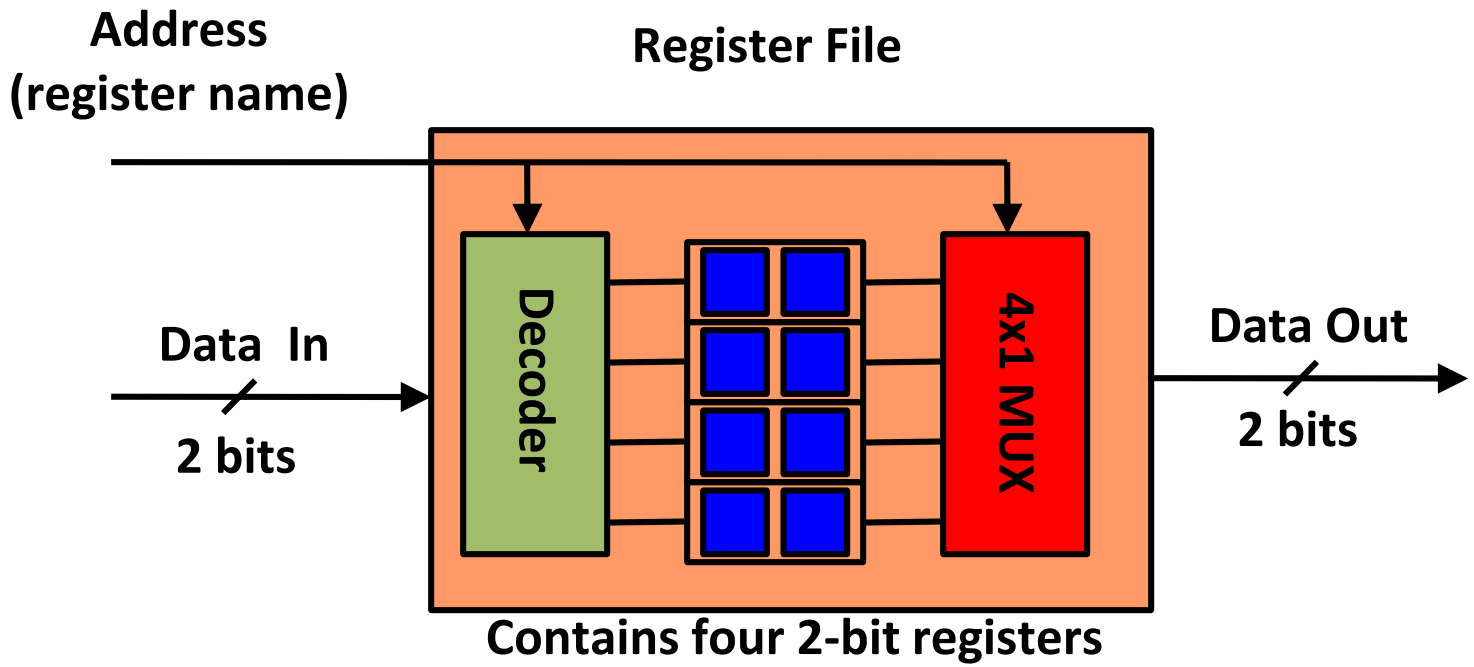


Next topic:

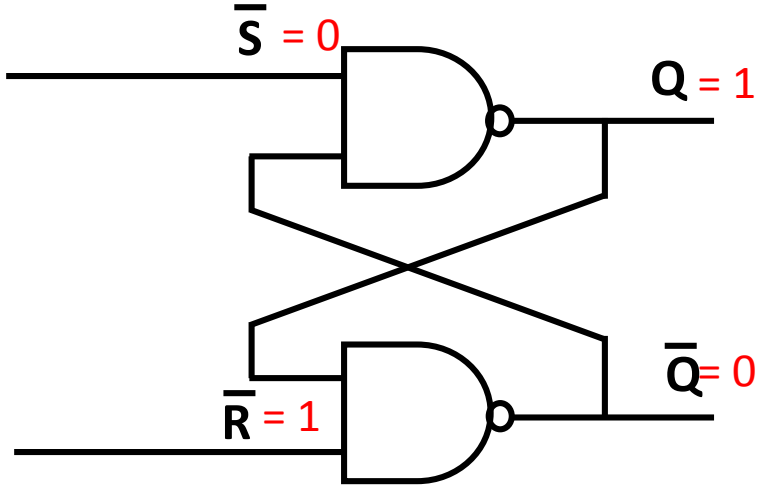
Sequential logic:

giving memory to circuits

Why do they need memory – Example: register file



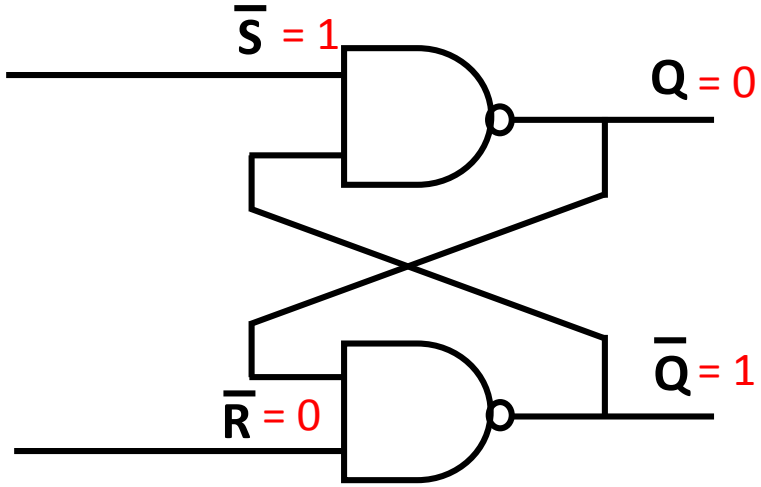
Let's look at the following circuit



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	1	1	0

What is the value of Q if $\overline{R}$ is 1 and $\overline{S}$ is 0?

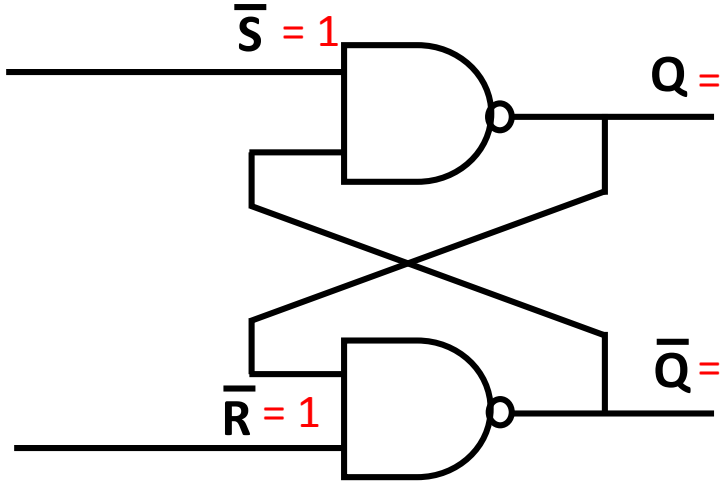
Building the Truth Table



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	1	1	0
1	0	0	1

What is the value of Q if $\overline{R}$ is 0 and $\overline{S}$ is 1?

For a Basic Memory Cell

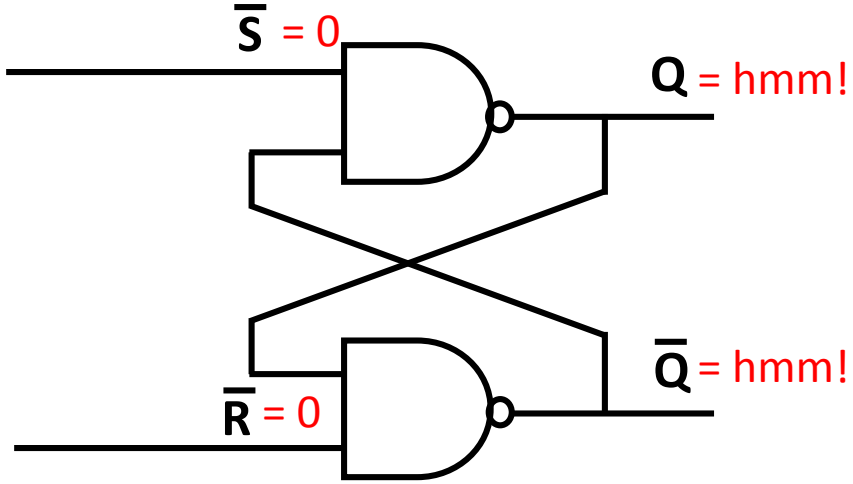


$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$

What is the value of Q if $\overline{R}$ is 1 and $\overline{S}$ is 1?

As long as R and S remain 1 then the value Q (and Q) will remain unchanged. This value is stored in this circuit. **This is a basic memory cell.**

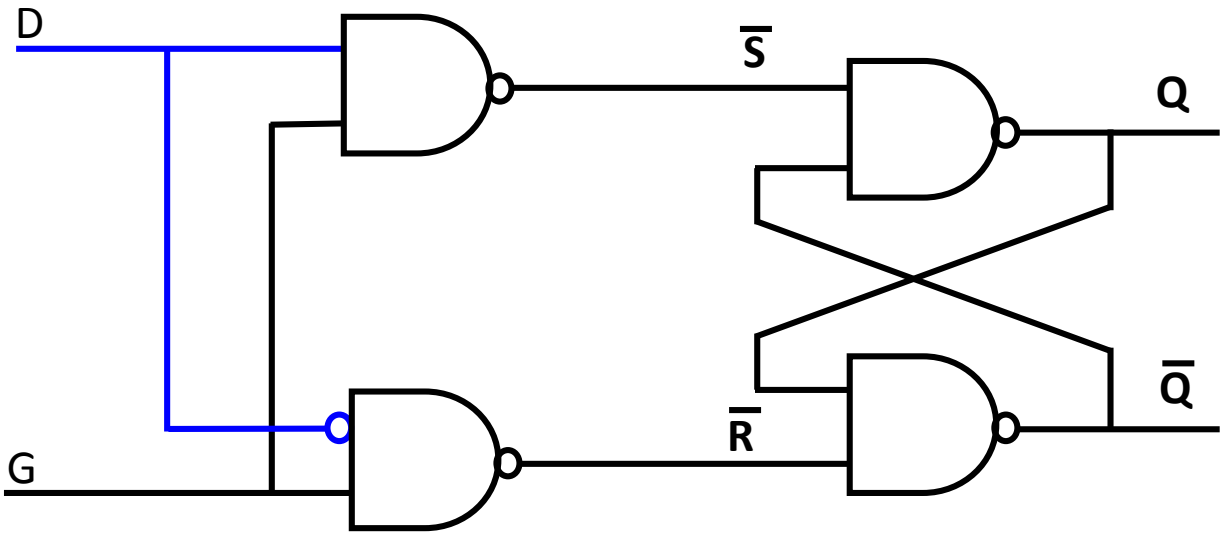
With unstable inputs 0,0



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	undef	
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$

What is the value of Q if $\overline{R}$ is 0 and $\overline{S}$ is 0?

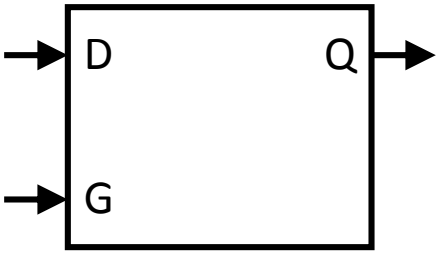
Transparent D Latch



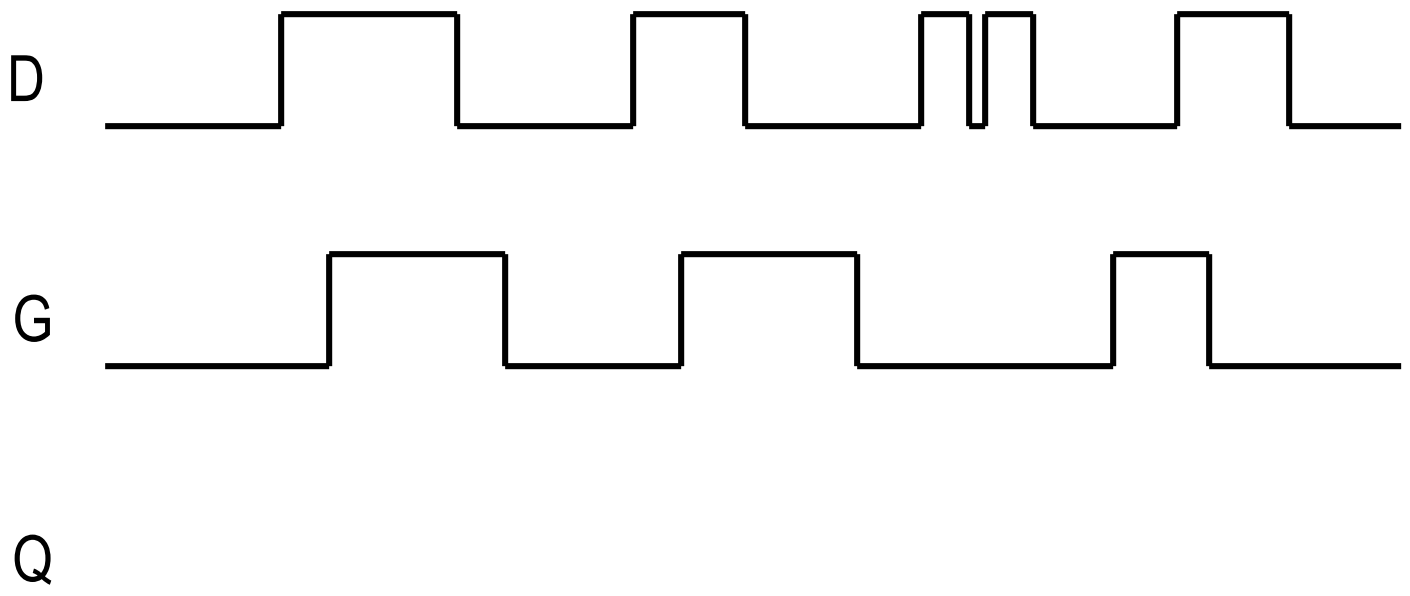
Gating signal

D	G	Q	$\overline{Q}$	
0	0	Q	$\overline{Q}$	Set state is retained
0	1	0	1	
1	0	Q	$\overline{Q}$	
1	1	1	0	

Next state is set



Q?



Adding a clock to the mix

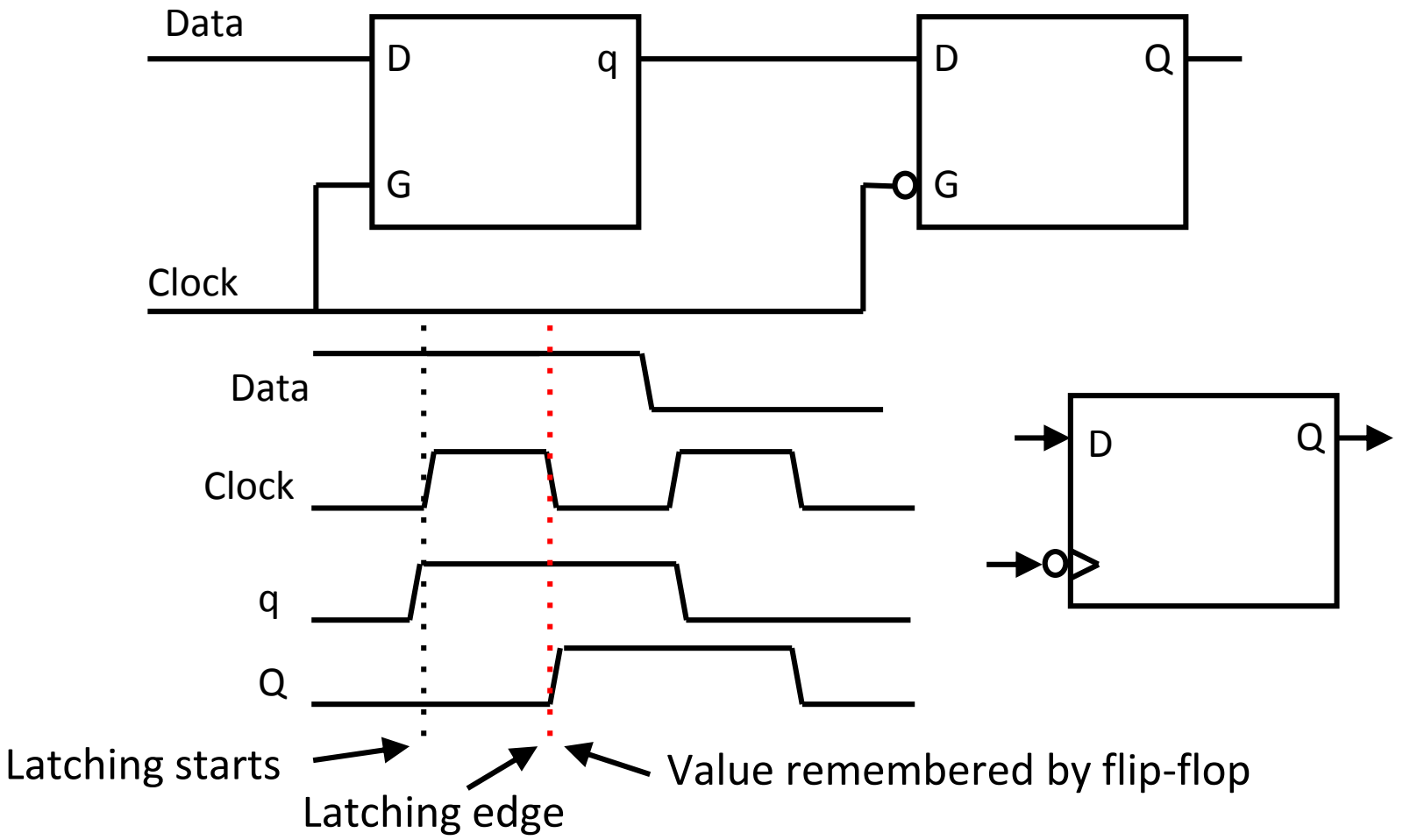
- We can design more interesting circuits if we have a clock signal
- The use of a clock enables a sequential circuit to **predictably** change state (and store information).
- A clock signal alternates between 0 and 1 states at a fixed frequency (e.g., 100MHz)
- What should the clock frequency be?

Clocks

- Clock signal
  - Periodic pulse
  - Generated using oscillating crystal or ring oscillator
  - Distributed throughout chip using clock distribution net

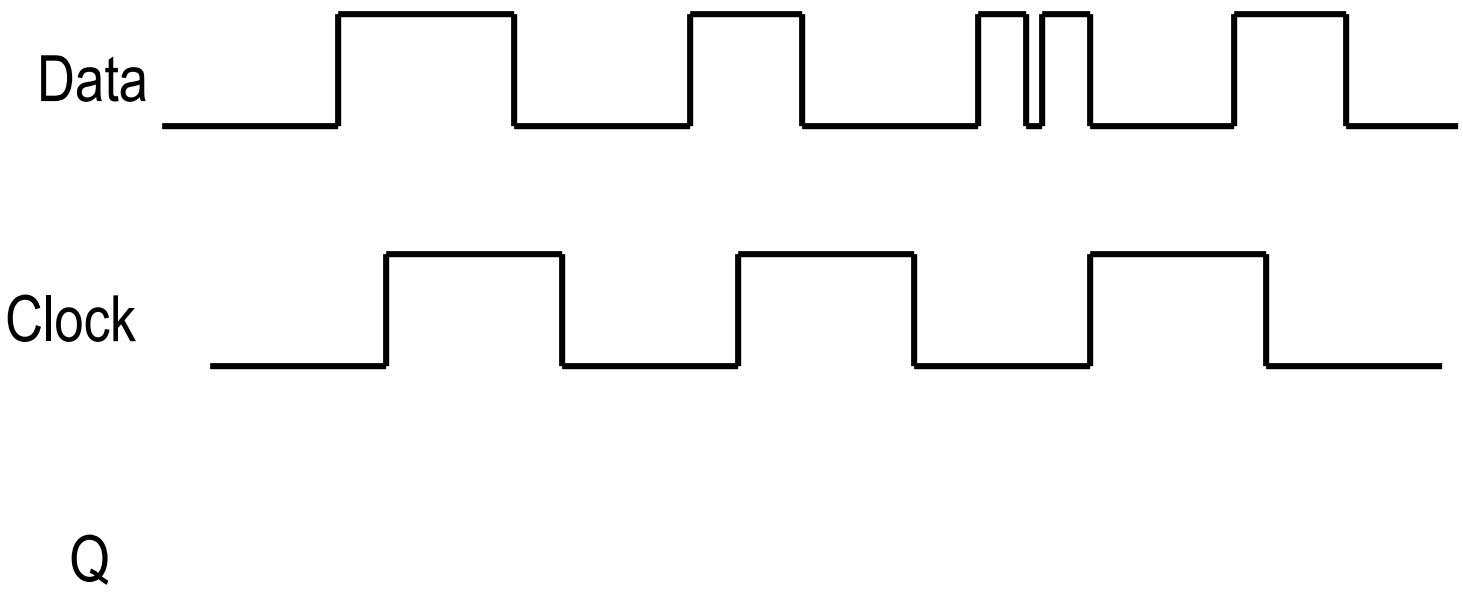
- With clock signals we can create a new class of circuits called **sequential**
  - Output determined by inputs & previous state

Edge Triggered D Flip-flop

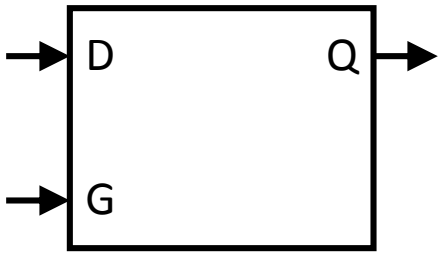


Value should remain valid and stable during latching!

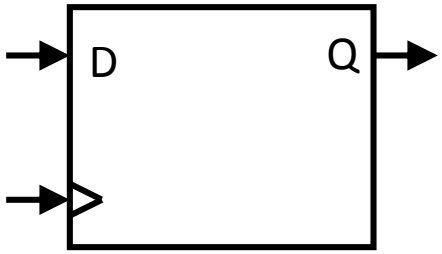
Q?



Why edge-triggered flip-flops?



IS LIKE A TOLL-GATE

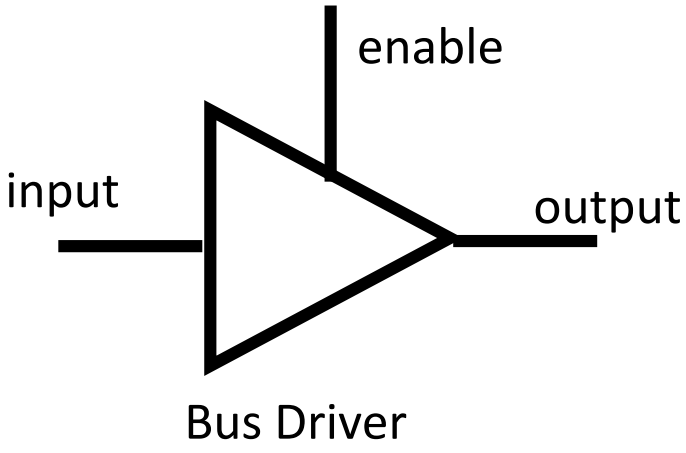


IS LIKE AN AIR-LOCK

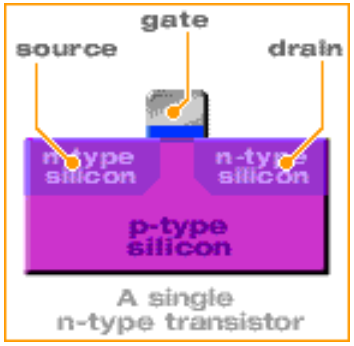
In edge-triggered flip-flops, the latching edge provides convenient abstraction of “instantaneous” change of state.

Tri-state Logic

- The output of a gate can be any of three different states: one, zero or not connected
  - Need to disconnect the circuit. How?

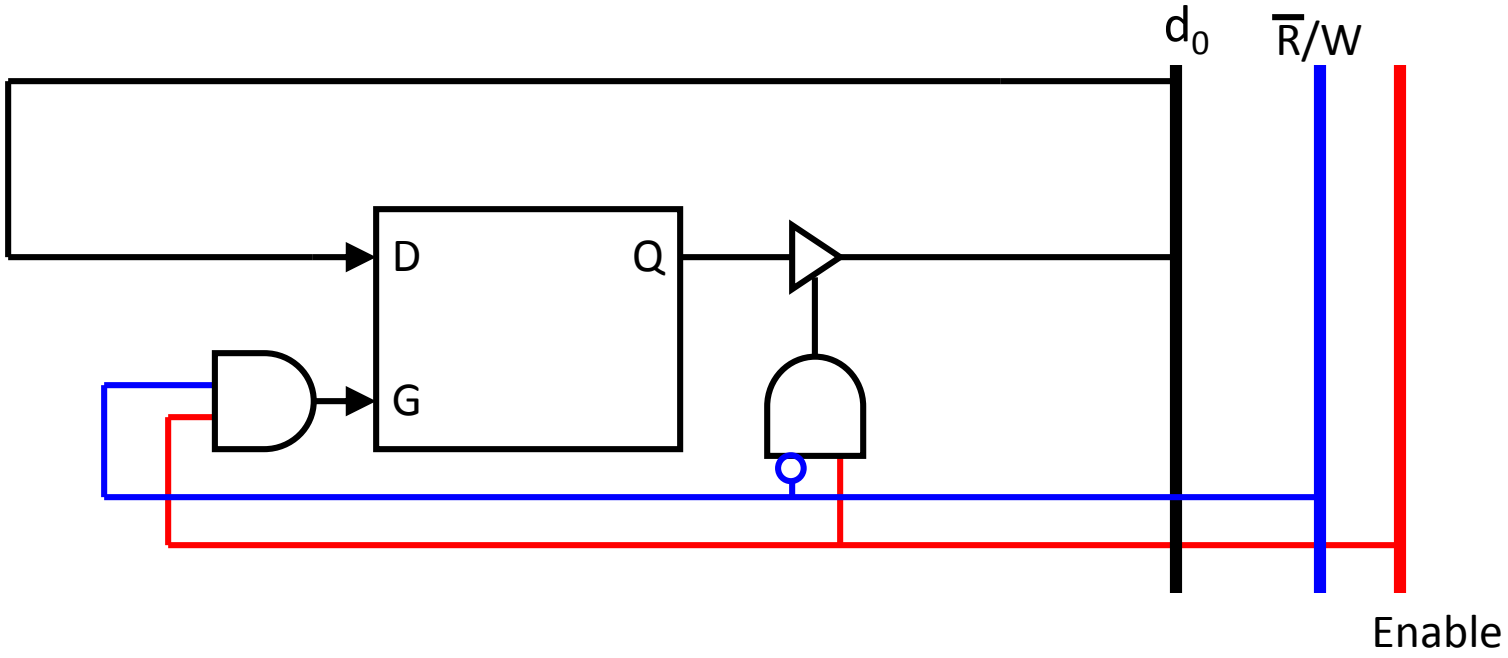


Bus Driver

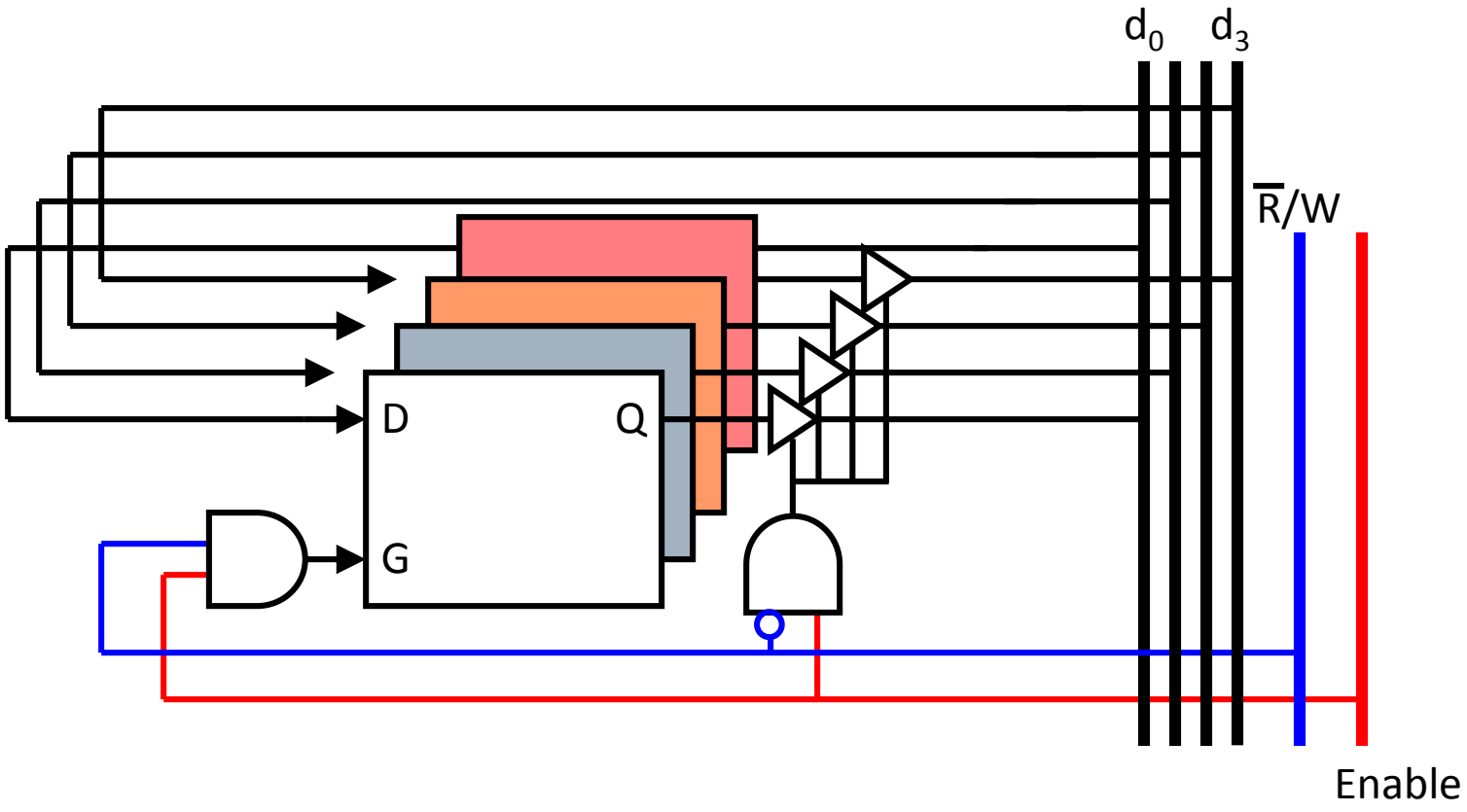


Implemented as a single transistor

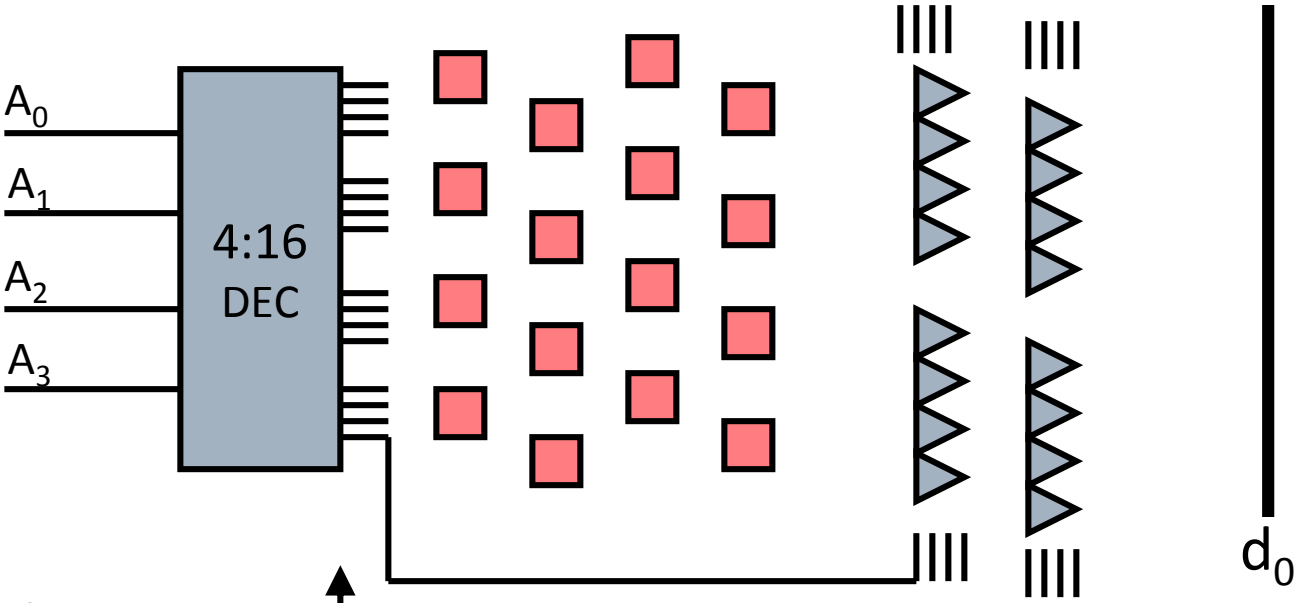
A Static Memory Cell



A 4-Bit Register



Addressing Memory Arrays

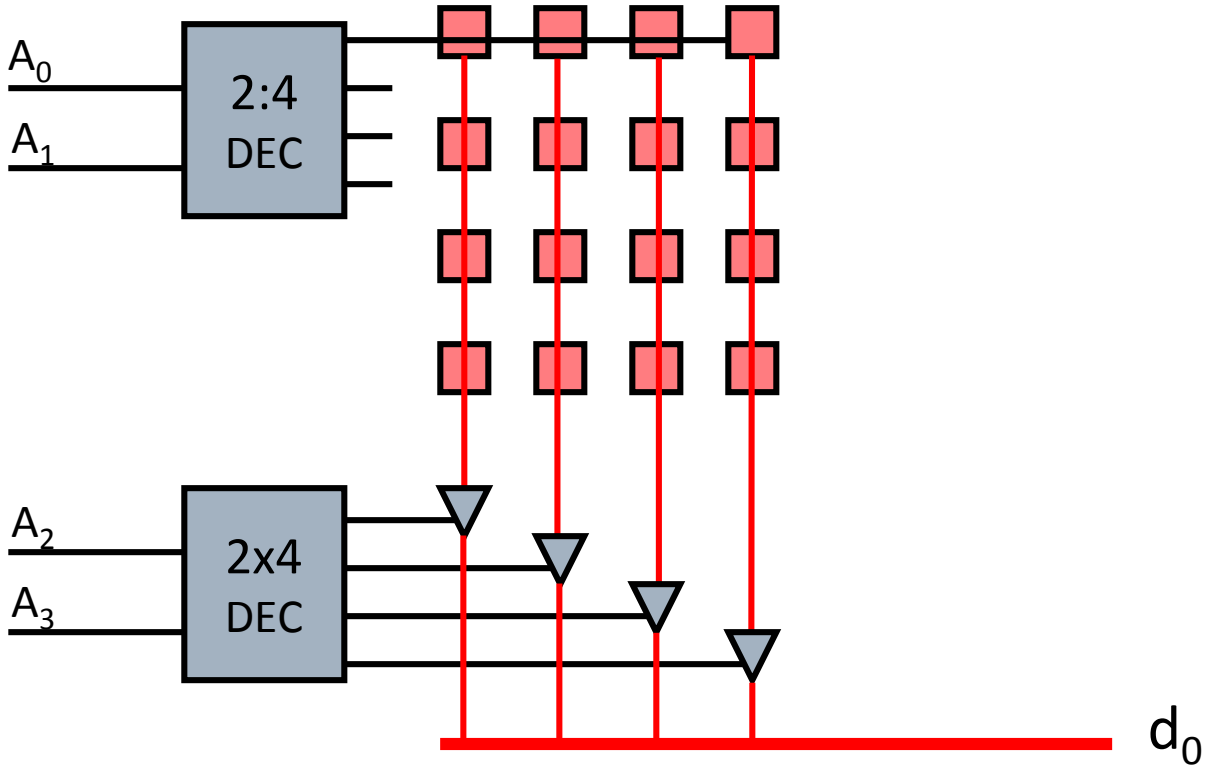


One of the 2^4 enable lines is turned ON

Implements 16:1 MUX

16:1 BIT MEMORY

A Scheme with Fewer Components



16 X 1 BIT MEMORY

Putting it in a package

18-bit X 2M MEMORY (36 MBits)

Other Memories

- Static RAM
  - Built from sequential circuits
    - Takes 4-6 transistors to store 1 bit
    - Fast access (< 1 ns access possible)
- Dynamic RAM
  - Built using a single transistor and a capacitor
    - 1's must be refreshed often to retain value
    - Slower access than static RAM
    - Much more dense layout than static RAM
- ROM, PROM, Flash memory, etc. ⇨ Later