1. Introduction and Overview

EECS 370 – Introduction to Computer Organization – Winter 2015

Robert Dick, Andrew Lukefahr, and Satish Narayanasamy

EECS Department
University of Michigan in Ann Arbor, USA

Your profs

- Prof. Robert Dick (2417-E EECS)
  http://robertdick.org/

- Andrew Lukefahr (2733 BBB)
  http://www.eecs.umich.edu/~lukefahr

- Prof. Satish Narayanasamy (4712 BBB)
  http://www.eecs.umich.edu/~nsatish

Your student instructors

- Animesh Jain
- Matt Skach
- Inal Batu
- Aaron Podell
- Wade Bonkowski
- Asher Perlmutter
- Devin Gurung
- Nathan Immerman

Class resources

Course homepage: http://www.eecs.umich.edu/courses/eecs370

Piazza forum: https://piazza.com/umich/winter2015/eecs370/home

use this to:

- ask general questions on lectures, projects and homeworks
- discuss with your classmates

Administrative requests (SSD, Medical emergencies, etc.)

http://goo.gl/forms/G6qHcuoFLi

For other issues, email **eecs370staff@umich.edu** (reaches all teaching staff)

Goals of the course

- To understand how computer systems are organized and what tradeoffs are made in the design of these systems
  - Instruction set architecture
  - Processor microarchitecture
  - Systems architecture
    - Memory systems
    - I/O systems

Where does EECS 370 fit in our curriculum?

- Software view
  - EECS 183/ENGR 101, EECS 280, EECS 281
  - Turning specs into high level language

- Hardware view
  - EECS 270, **EECS 370**
  - gates $\rightarrow$ logic circuits $\rightarrow$ computing structures

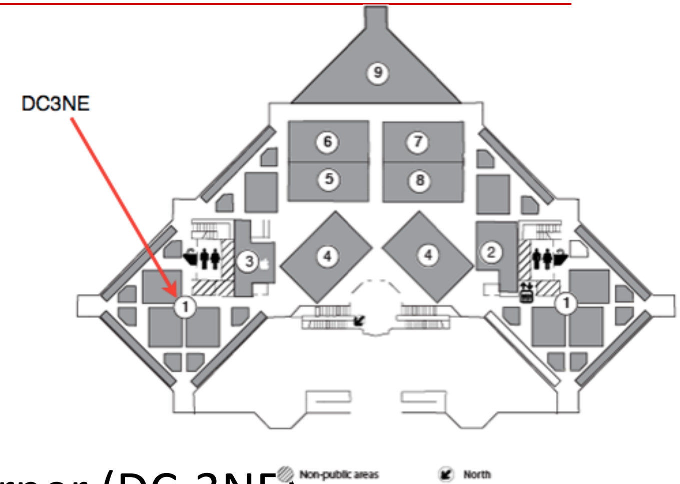
- Prereqs: C or C++ programming experience

Basics: lectures and discussions

- Lectures:
  - Attend any section you want, as long as there are enough seats
- Discussions:
  - Attend any section you want, as long as there are enough seats
  - Discussions begin next week

Office hours

- Profs. Dick, Lukefahr, Narayanasamy
  - Office hours: T/Th 2:00-3:00pm
  - When teaching, in their office



- Student instructors
  - Office hours in Duderstadt 3rd floor NE corner (DC-3NE)
  - Office hours are available every day, utilize them!
  - Office hours schedule: check course home page / Google calendar

- Additional office hours on need basis
  - e.g. around exam times, project deadlines, etc.
- Watch announcements on Piazza and website

Your work in 370

- Programming assignments (4 x 10% each)
  - Assembly / functional processor simulation
  - Processor datapath simulation
  - Pipeline simulation
  - Cache simulation

- Two exams (50% total)
  - 1 midterm @ 25% - Feb. 24 @ 7:00-9:00pm
  - 1 final @ 25% - April 24 @ 7:00-9:00pm

- Homeworks (10% total)
  - Total of 7 homeworks, drop lowest grade

Grades will be posted in ctools

Programming assignments

- 4 programming assignments simulating the execution of a simple microprocessor
- First programming assignment available on 13th Jan
- Using C to program, C is a subset of C++ without several features like classes
- The challenge is to understand computer organization enough that you can build a complete computer emulator

Auto-grading assignments

- We use a program to grade your assignments
  - Program submitted using <u>submit370</u> script available from CAEN machines

- **Assignments due at 6:00pm on due date**;
  assignment must have been received by 11:59pm on due date

- Assignments require access to a CAEN workstation
  (to run submit370 and use the same compiler)

- Due today: **make sure to have a CAEN account**

- Help on C/C++ available from GSIs

Don’t be a cheater!

- All projects must be your OWN work
  - Using others’ code, algorithm details, previous semester solutions is NOT permitted
- Suspected violations will result in initiation of formal procedures with the Engineering Honor Council
  - Violators receive 0 on the project and grade penalties recommended by EHC
- Auto-correlation program used to identify unacceptable collaboration
  - We check your work against submissions from previous semesters
  - It is good enough that the work needed to avoid detection is at least as much as the work needed to do the projects
- Do not post your work online

Homework assignments

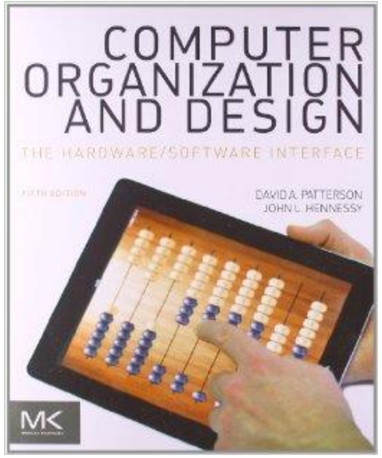
- 7 written homework assignments
  - Cover lecture material
  - Good practice problems
  - No late days
- We will only record your 6 best homework grades
- You can discuss homework problems with your classmates, however you need to turn in your own write-up of the solution.
- First homework posted on Tue, Jan 13th

How we assign course grades

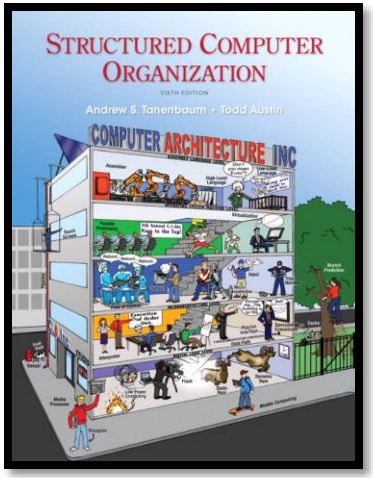
- Class is curved
- Historically, about 1/3 As, 1/3 Bs, 1/3 other
- Disclaimer: Past grading is no evidence of future results!

Course textbooks

Computer Organization and Design
5th Edition
by Patterson and Hennessy (e-copy)



Structured Computer Organization
6th Edition
by Tanenbaum and Austin



On reserve @AAEL:

- Fundamentals of Computer Organization and Architecture
  by Abd-El-Barr and El-Rewin(e-copy)
- Digital Design
  by Frank Vahid

Reading assignments

- Reading assignments will be posted on the website, along with the lecture notes

- You are responsible for knowing the reading material, as well as the lecture content

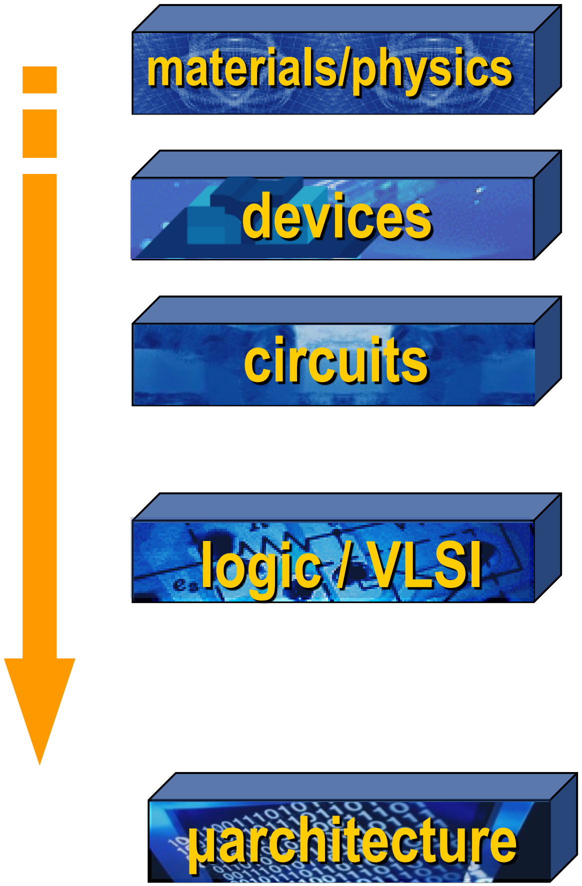
Course topics

- Introduction (this lecture)
- ISAs and Assembly (2-3 weeks)
- Processor implementation (2-3 weeks)
- Pipelining/Performance (2 weeks)

- Memory (2 weeks)
- I/O, parallel processing (1 week)
- Advanced topics (1 week)

- Exams/reviews (2 weeks)

Where this course material fits in the system stack

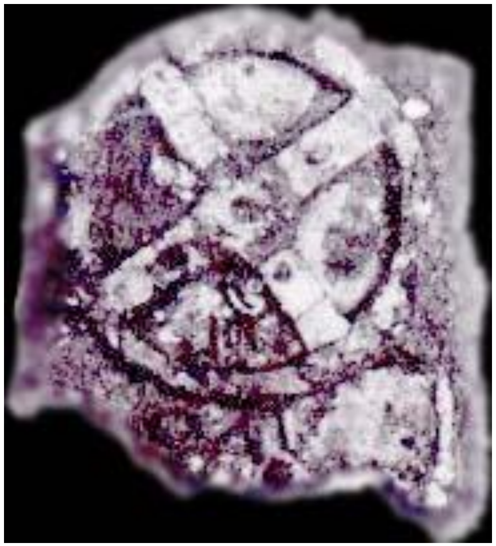


- Quantum-level, solid state physics
- Conductors, Insulators, Semiconductors.
- Doping silicon to make diodes and transistors.
- Building simple gates, boolean logic and truth tables
- Combinatorial logic: muxes, decoders, adders
- Clocks
- Sequential logic: latches memory
- State machines
- Processor Control: Machine instructions
- Computer Architecture: Defining a set of instructions

Exercise: What kind of chip is in your devices?

- Look up a device you have (or want!)
  - Example: Google “Galaxy S5 chip”
- What make and model chip does it have?
  - Example: Qualcomm Snapdragon 801
- How many cores does it have? What is the clock speed?
  - Example: 4 cores at 2.5GHz
- 32 bit? 64 bit? Process technology
  You might need to search the chip “snapdragon 801 specs”
  - Example: 32 bit
  - 28nm process technology
- What does all this *mean*? We will learn in this class!

Computer ancient history



"Astrolavos" artifact discovered in ship wreckage (ca. 65BC) outside Anticethira, Greece, in 1900.

Complicated cogwheel system made of brass (16x32x9 cm).

Chronological data entry.

Used as a "differential" cogwheel system to compute moon phases and rising/setting of moon and planets.

Derek Price, "An ancient Greek computer," *Scientific American*, June 1959.

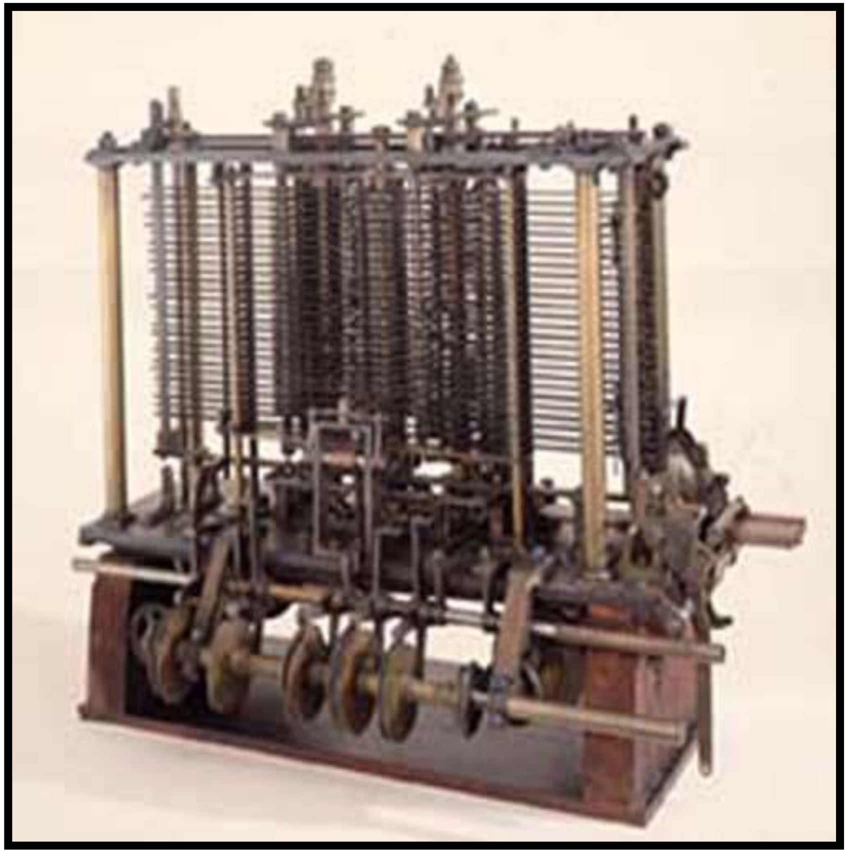
Other early "computers"

Music Box

Tipu's tiger – 1795 A.D

Automaton – early '1800

About 1,800 years later



- Charles Babbage

- Analytical Engine
- Started in 1834
  - Never finished
- No Hertz Rating
  - Heinrich Hertz 1857-1894

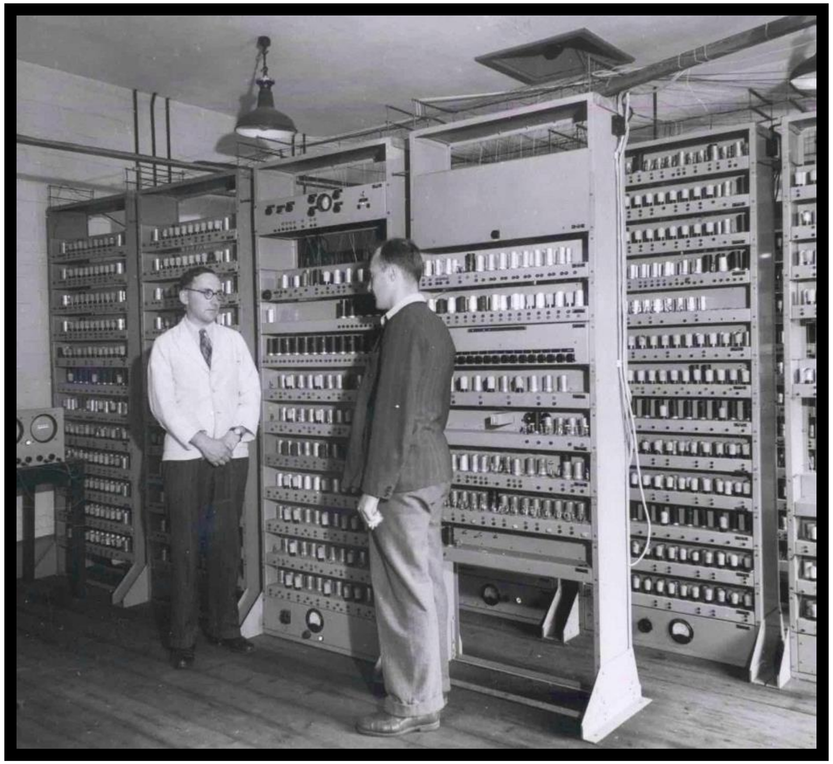
Modern computer history

ENIAC

Eckert and Mauchly

- 1^{st} working electronic computer (1946)
- 18,000 Vacuum tubes
- 1,800 instructions/sec
- 3,000 ft^3

Computer history in the UK



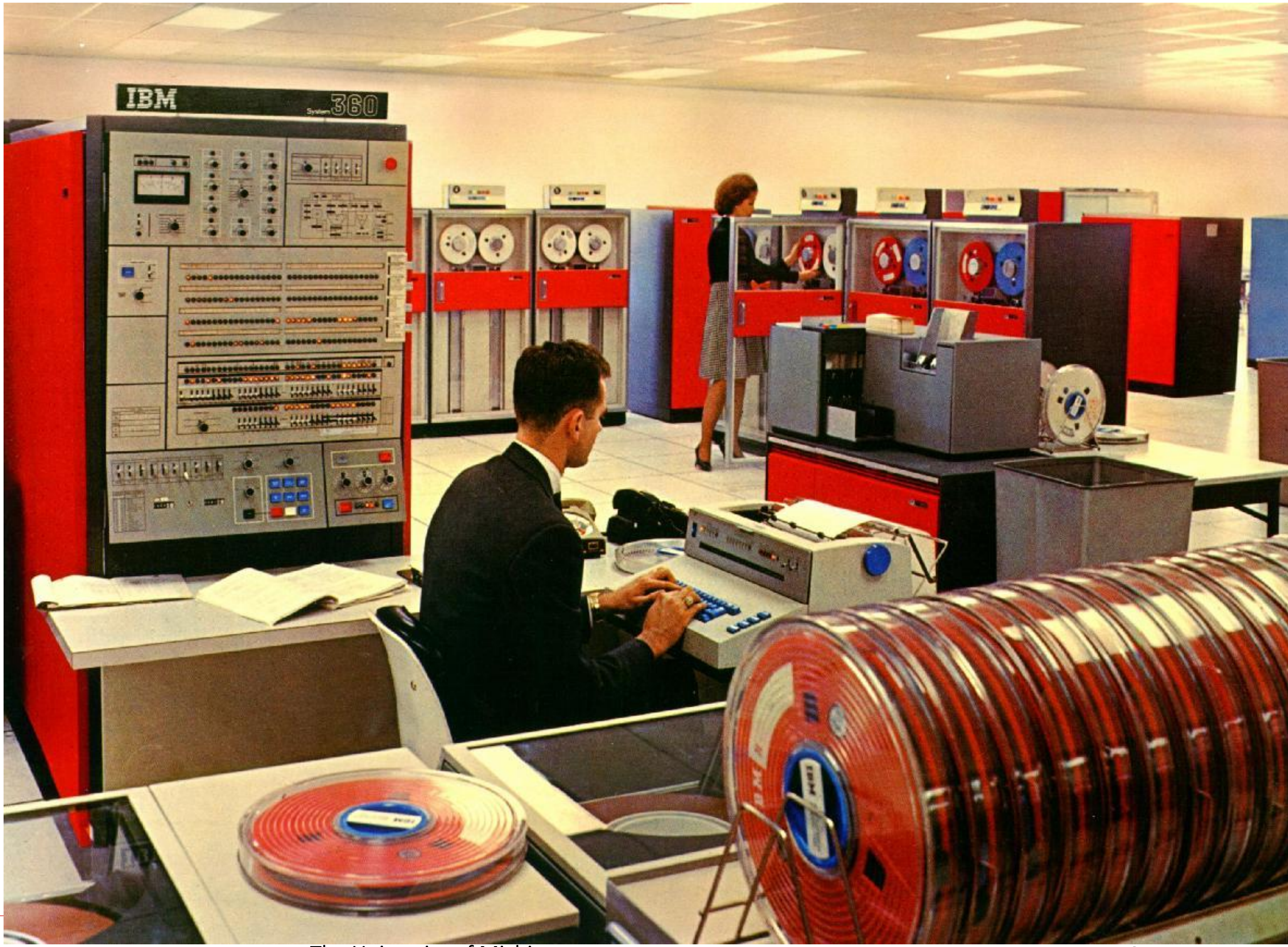
EDSAC 1 (1949)

- Maurice Wilkes

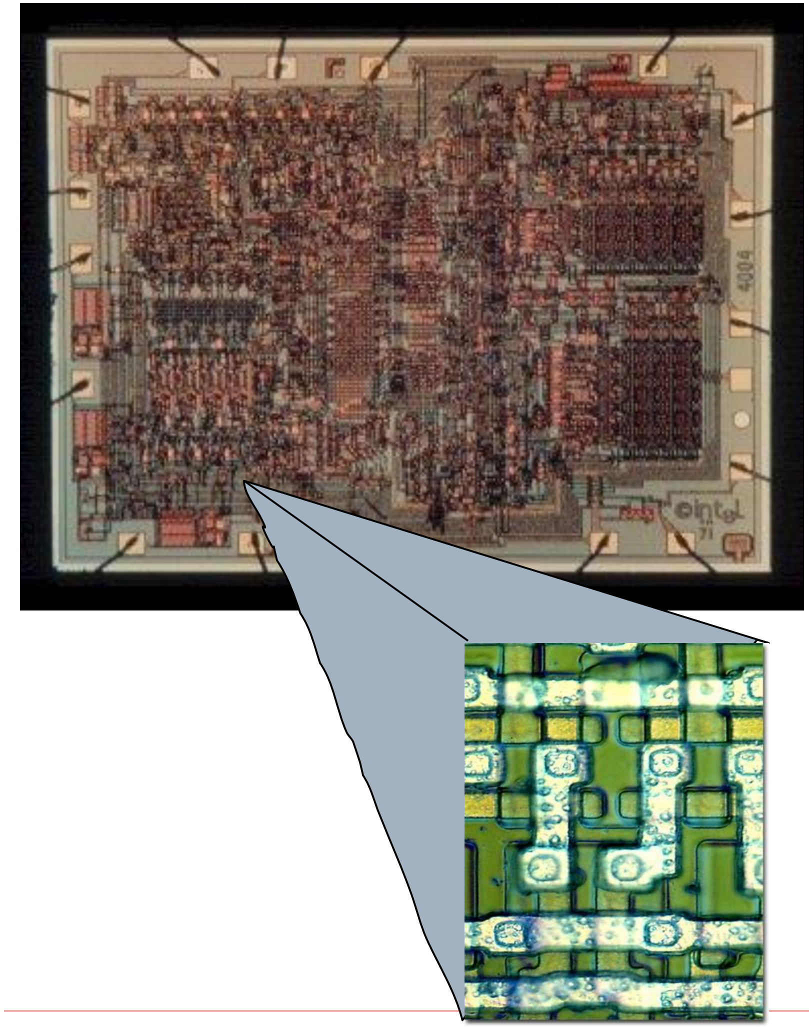
- 1st stored program computer
- 650 instructions/sec
- 1,400 ft^3

http://www.cl.cam.ac.uk/UoCCL/misc/EDSAC99/

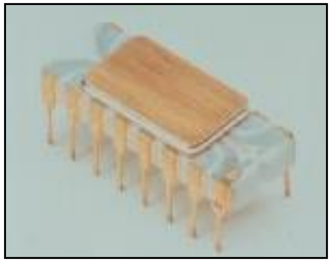
The mainframe era - IBM 360   - circa 1970



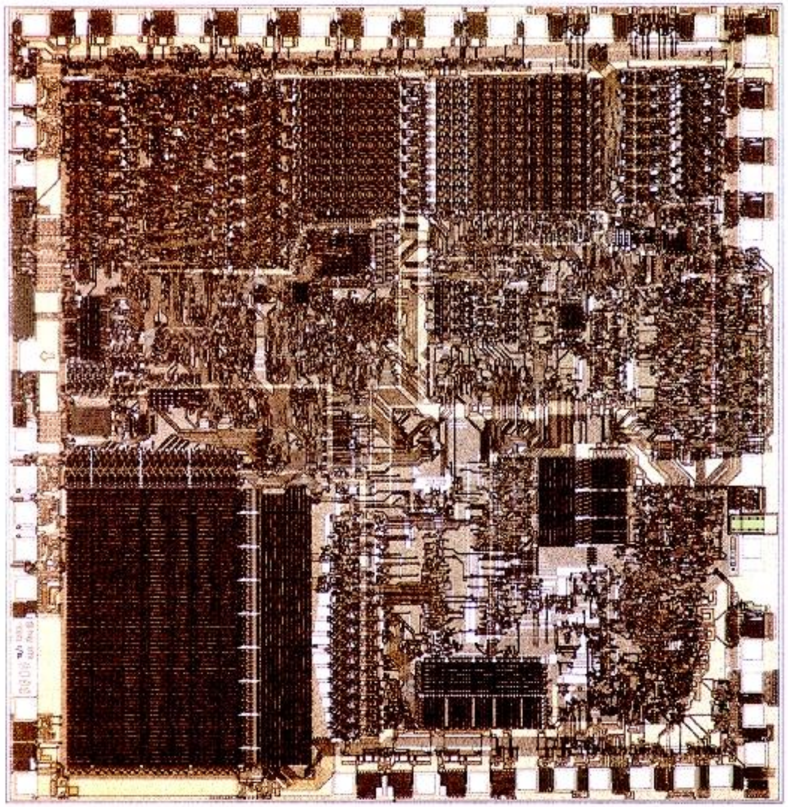
Intel 4004 die photo



- Introduced in 1970
  - First microprocessor
- 2,250 transistors
- 12 mm^2
- 108 KHz

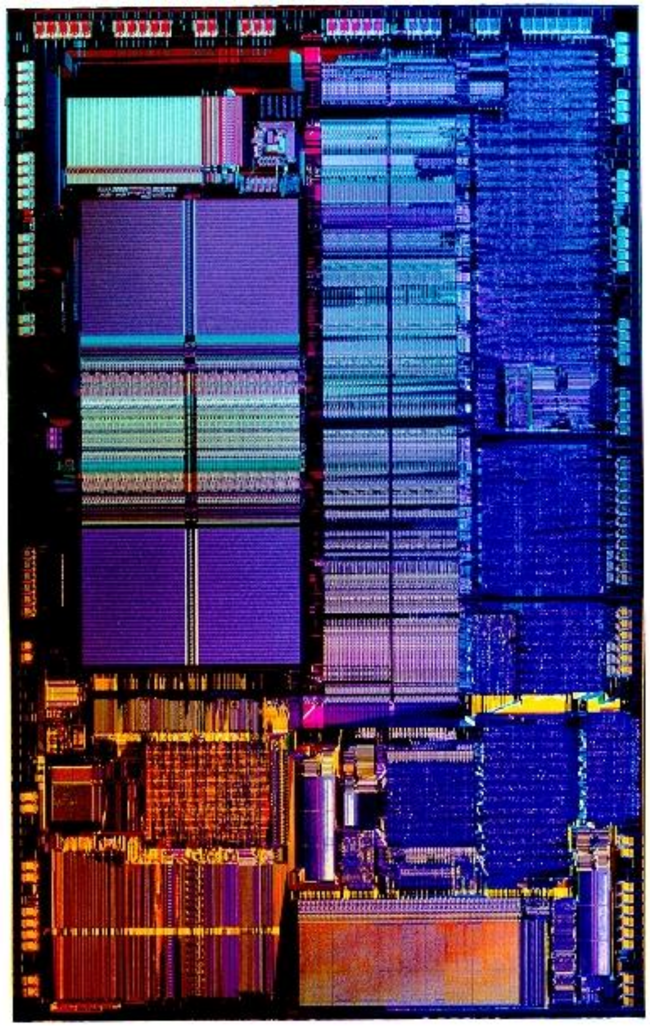


Intel 8086 die scan



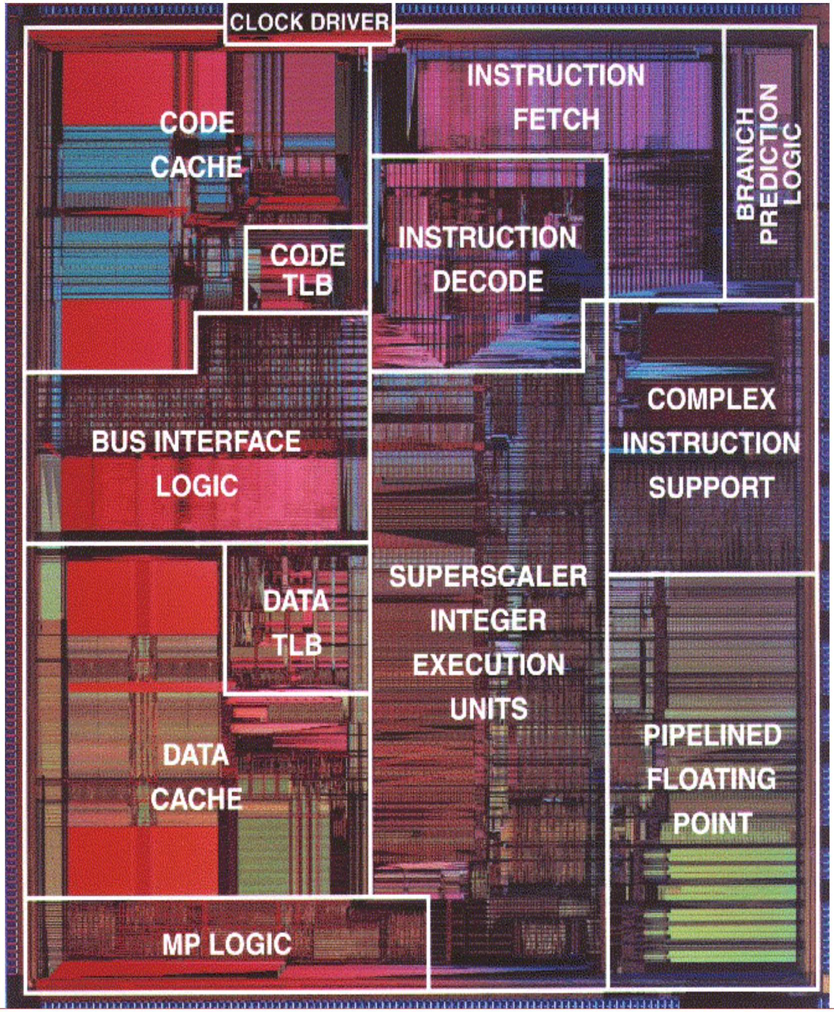
- 29,000 transistors
- 33 mm^2
- 5 MHz
- Introduced in 1979
  - Basic architecture of the IA32 PC

Intel 80486 (i486) die scan



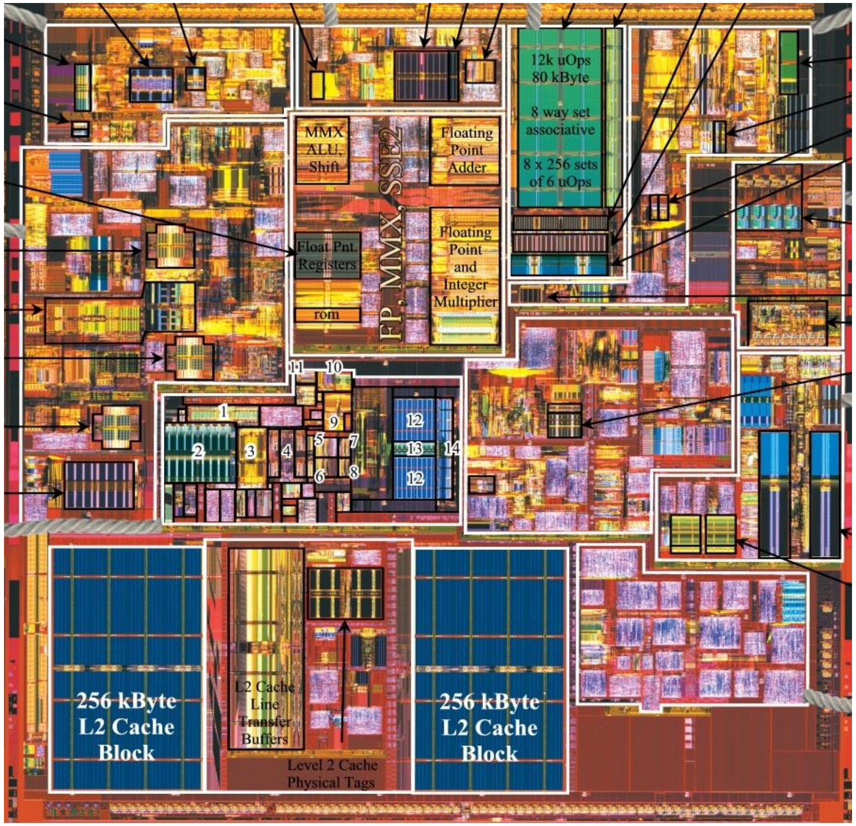
- 1,200,000 transistors
- 81 mm^2
- 25 MHz
- Introduced in 1989
  - 1st pipelined implementation of IA32

Pentium die photo (overlays)



- 3,100,000 transistors
- 296 mm^2 (0.8μm technology)
- 60 MHz
- Introduced in 1993
  - 1st superscalar implementation of IA32

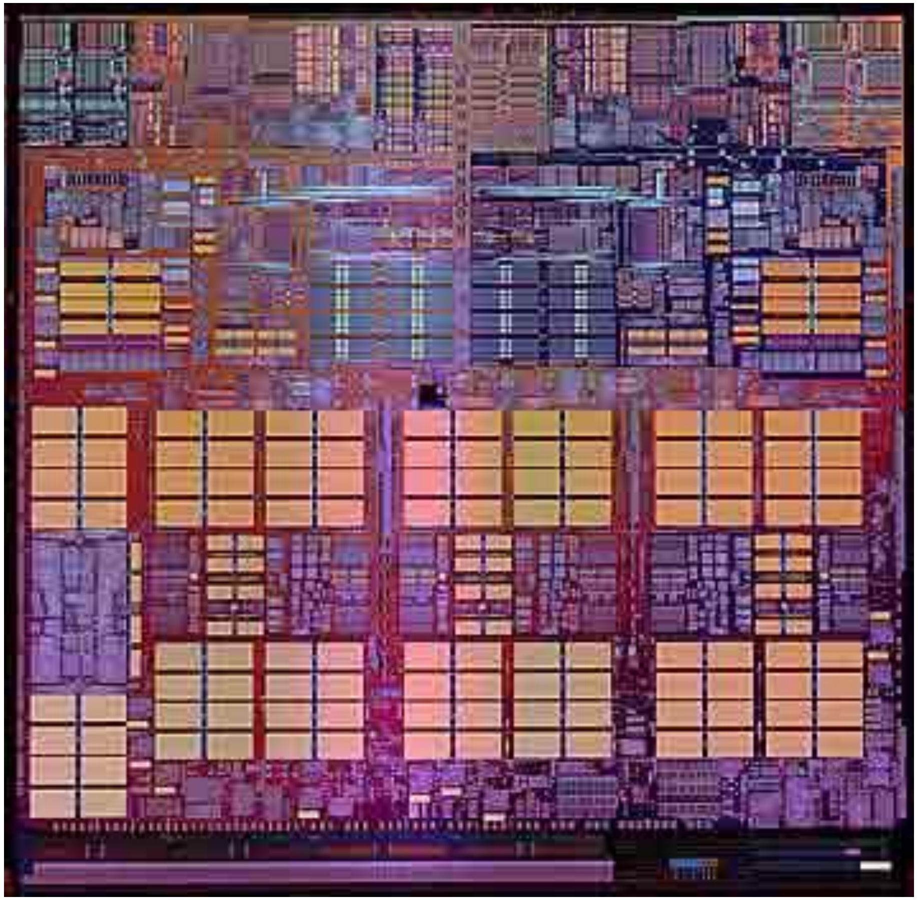
Pentium 4



http://www.chip-architect.com

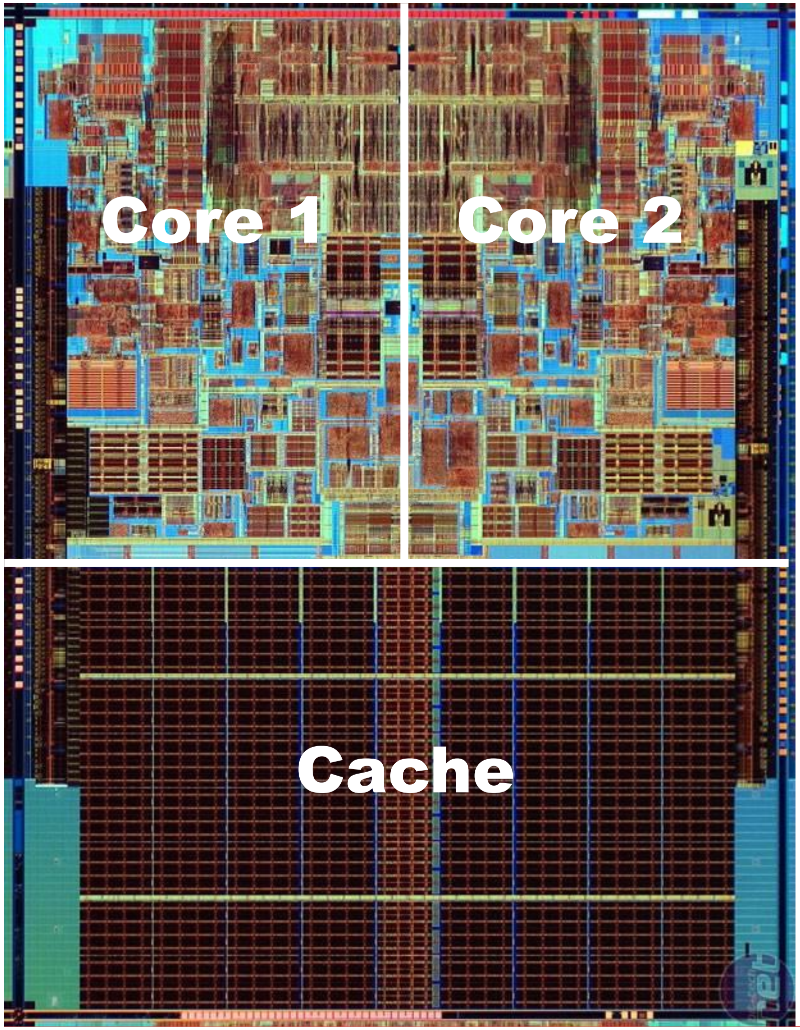
- 55,000,000 transistors
- 146 mm^2 (180nm technology)
- 3 GHz
- Introduced in 2000
- Out-of-order execution (not the first)

IBM POWER4



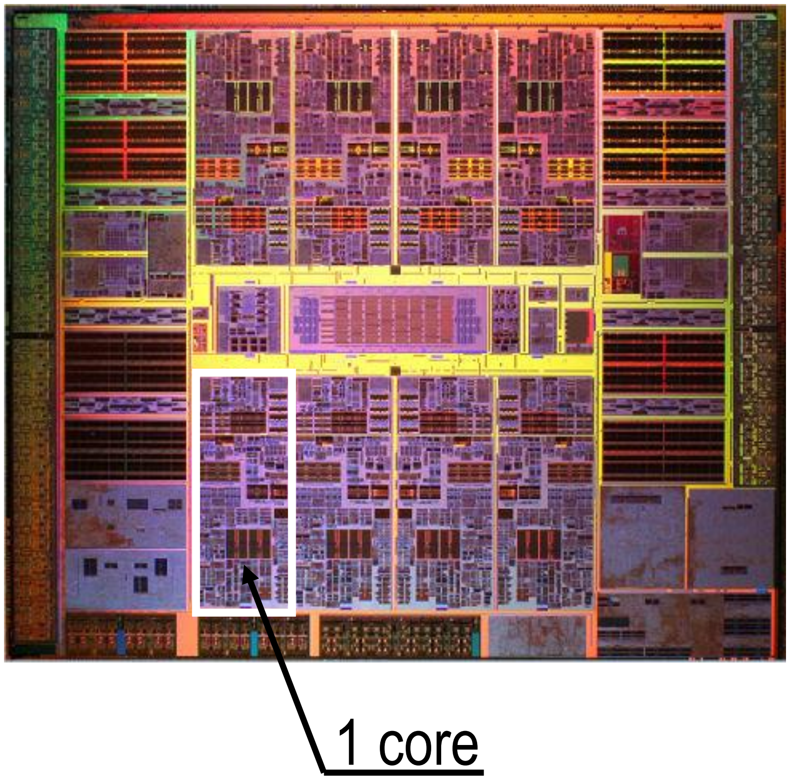
- 174,000,000 transistors
- 412 mm^2 (180nm technology)
- 1.3 GHz
- Introduced in 2001
- 1st commercial multi-core

Intel core duo



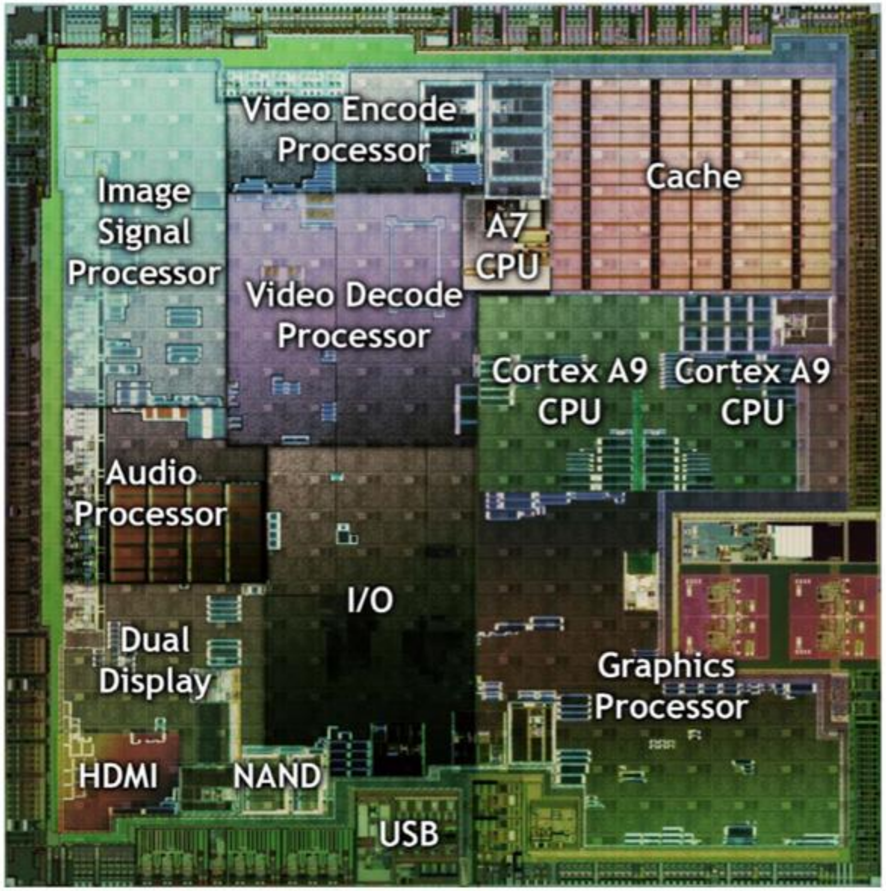
- 291,000,000 transistors
- 143 mm^2 (65nm technology)
- 3 GHz
- Introduced in 2006

UltraSparc T2 (Niagara 2)



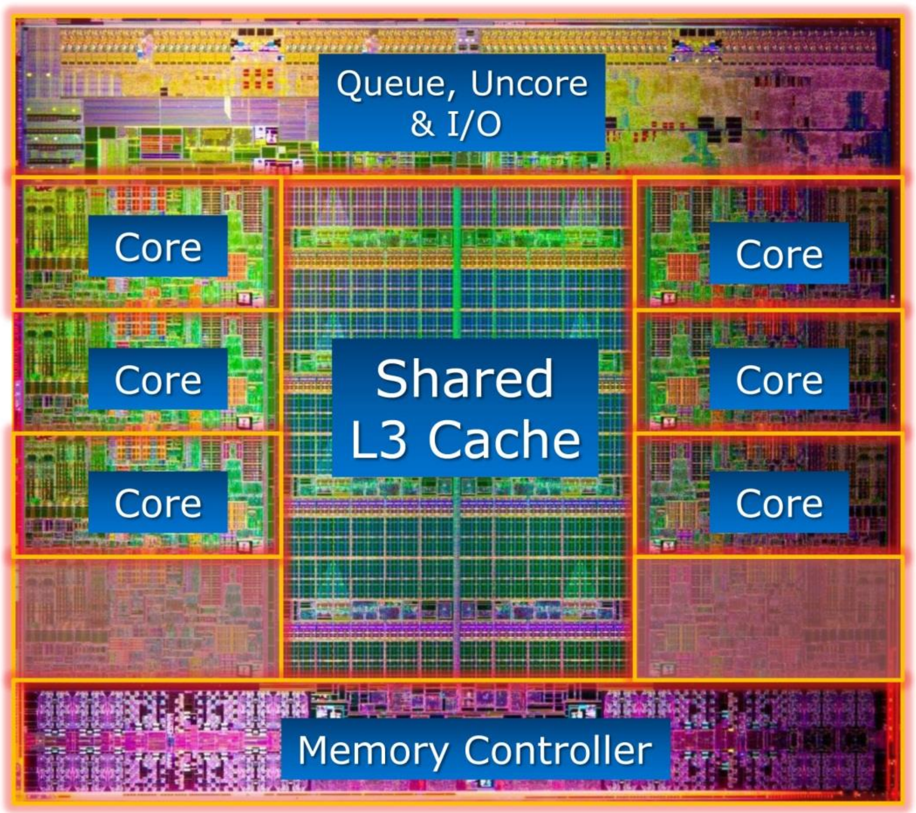
- 500,000,000 transistors
- 342 mm^2 - 65nm
- 1.2 – 1.4 GHz
- 8 cores – 64 threads
- 1 FPU per core
- Introduced in 2007

NVIDIA Tegra 2 System-on-a-Chip (SoC)



- 260,000,000 transistors
- Dual ARM cores
- Plus, GPU and DSP
- 49 mm^2 - 65nm
- 1.2 GHz
- Introduced in 2010
- Integrated in Tesla and Audi cars

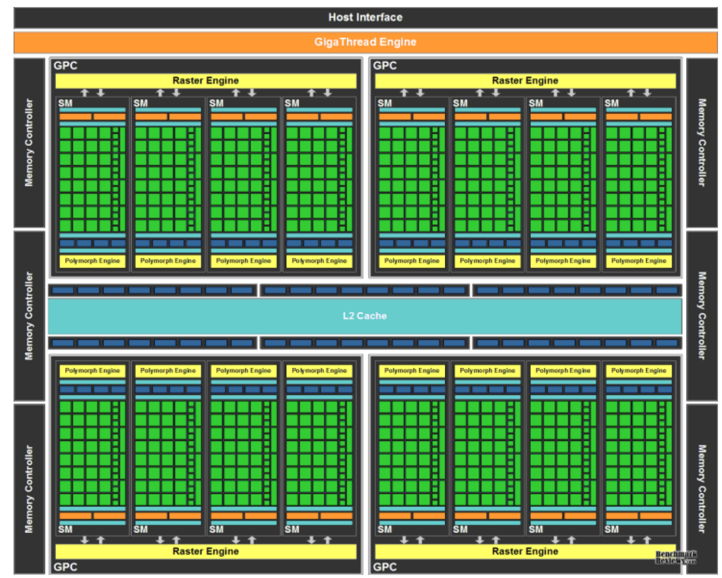
Intel Core i7 (Sandy Bridge E)



- 2,270,000,000 transistors
- 6-cores (8 for Xeon)
- SSE (vector) execution
- 435 mm^2 – 32nm
- 3.5 GHz
- Introduced in 2012
- 150W !

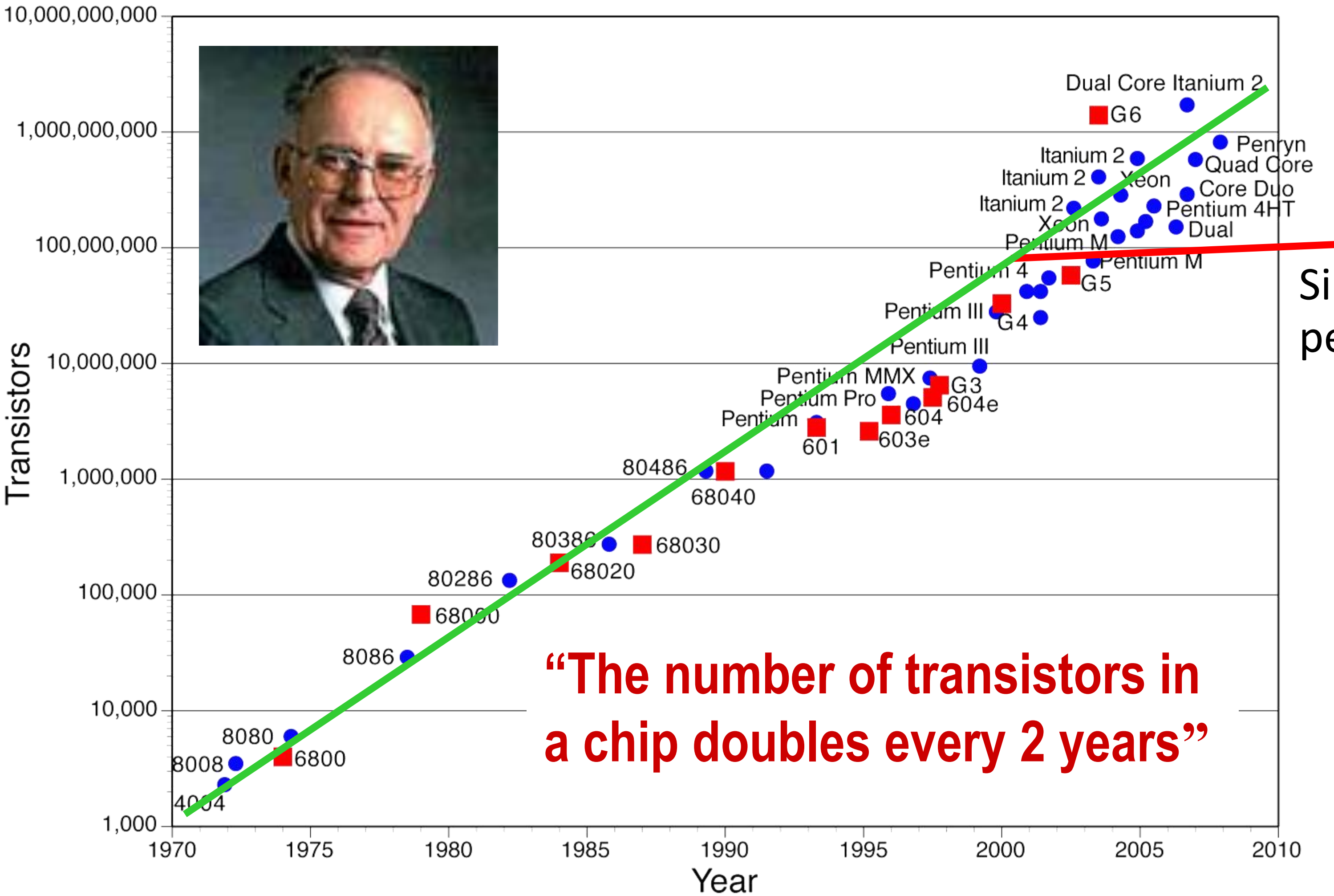
The near future of computing: many cores and GPUs

- Intel Polaris chip: 80 cores – experimental design
- Tilera TILE-Gx: 100-core processor
- Nvidia: 512-core Fermi GPU array



- Implications to you:
  - The hardware designer: designs getting bigger and more complex
  - The programmer: coding will be much more difficult

Computer architecture's secret sauce: "Moore's Law"



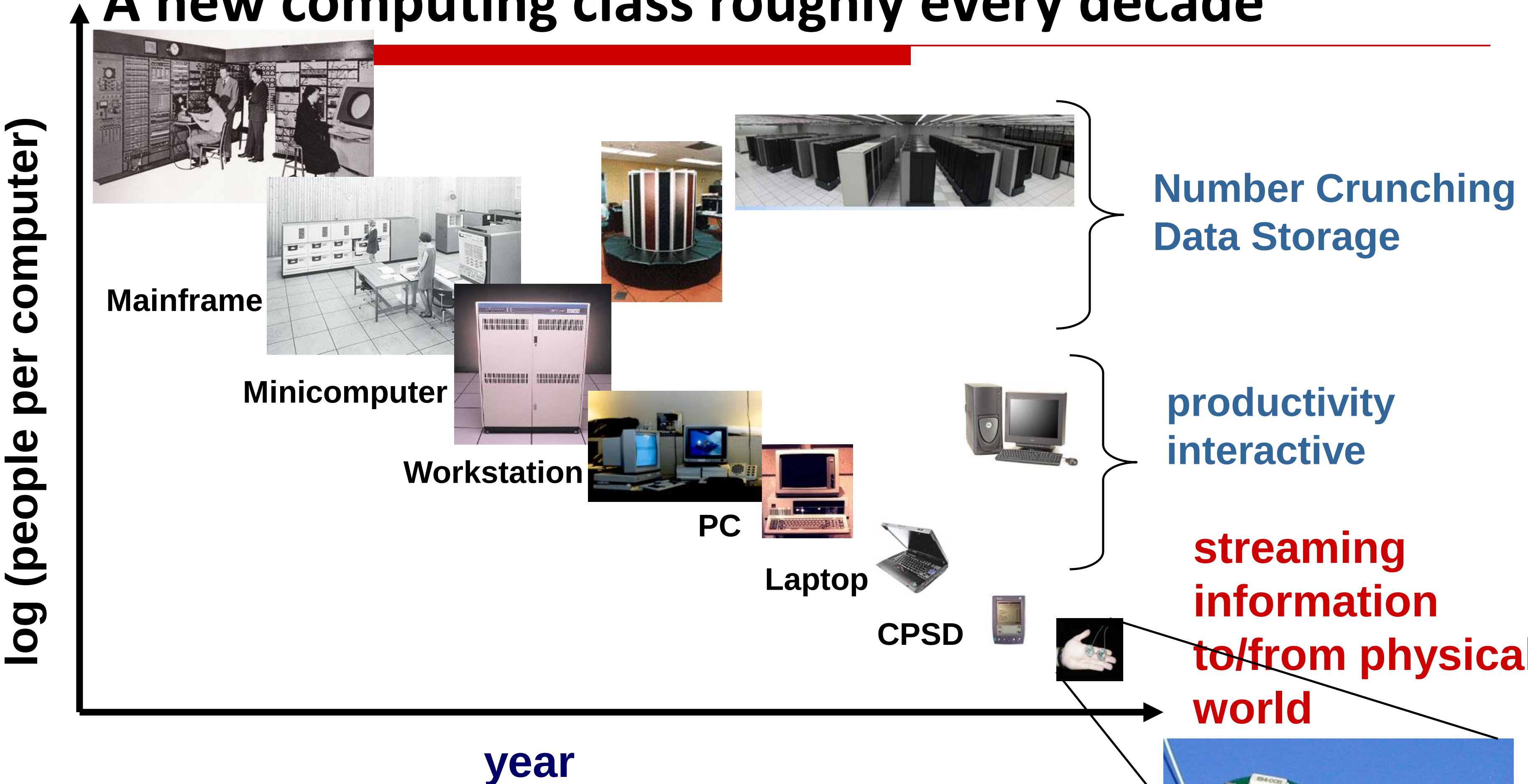
"The number of transistors in a chip doubles every 2 years"

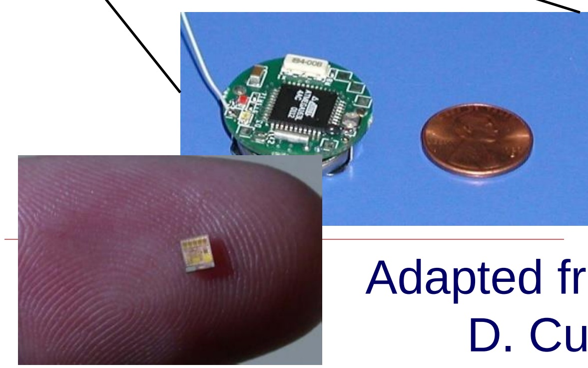
Single-core performance

Denard Scaling

- Denard Scaling: as transistors get smaller their power density stays constant
- Translation: as the number of transistors on a chip grows (Moore’s Law), the power stays roughly constant
- Mid-2000’s Denard Scaling broke. Why? Transistors got so small that they began to leak a lot of power. Leaking lots of power caused a chip heat up a lot.
- Conclusion: you can put lots of transistors on a chip, but you can’t use them all at full power at the same time.

Bell's Law of Computer Classes:
A new computing class roughly every decade



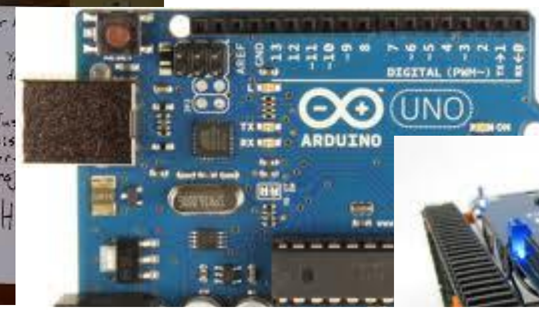


"Roughly every decade a new, lower priced computer class forms based on a new programming platform, network, and interface resulting in new usage and the establishment of a new industry."

Adapted from
D. Culler

The computer spectrum

- Disposables
- Microcontrollers
- Mobile/game
- PC
- Servers/clusters
- Mainframes






Reminder

- Make sure you have a CAEN account! (today)
- Homework 1 to be posted on 1/13
- Project 1 to be posted on 1/13
- Discussion section starts tomorrow
  - learn about C programming, debugging methods and tools, and more.