ECE505 Project RISC-V Processor - IP Cores

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IP Cores Instruction

Tips:

change top-level: *"boost::filesystem::remove: The process cannot access the file because another process "*

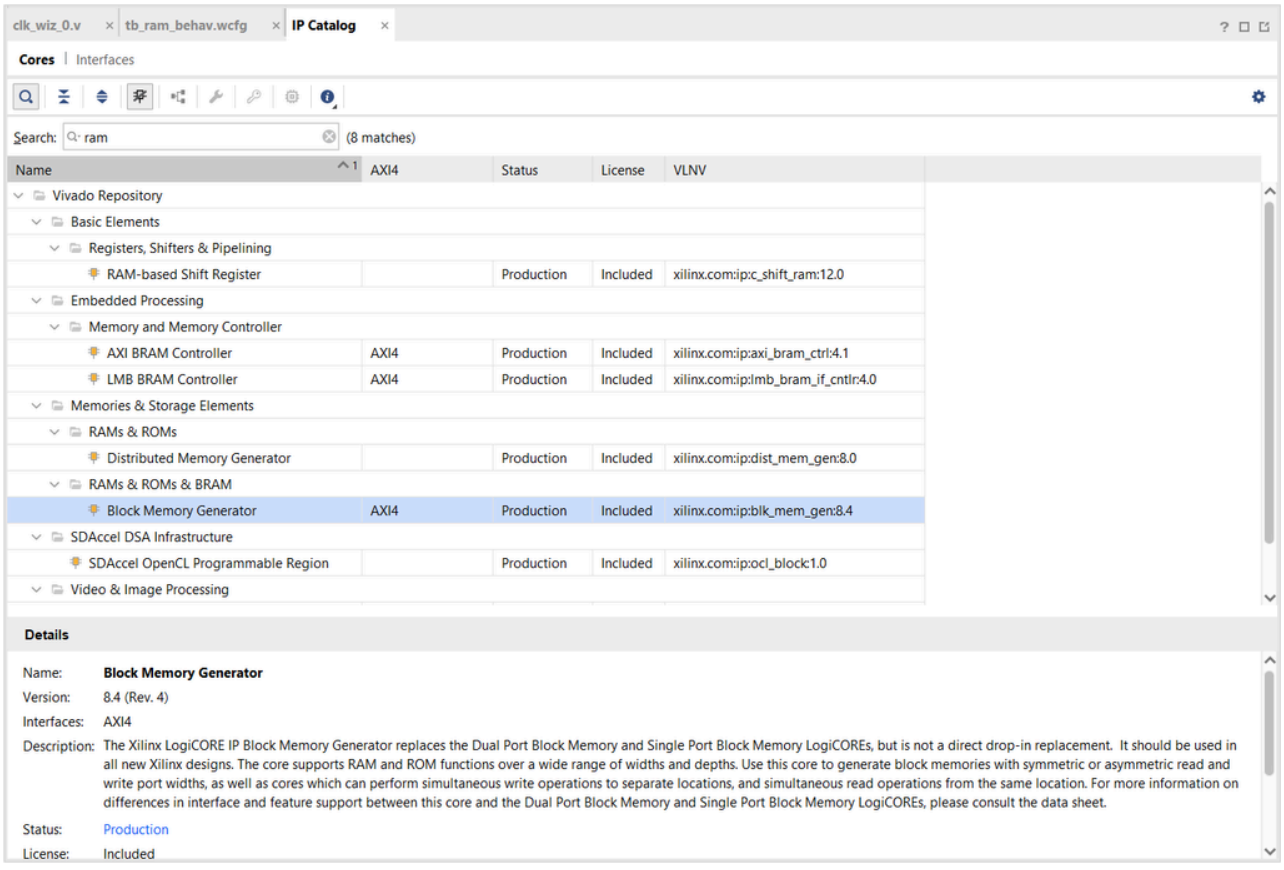
locked signal in MMCM: What is the *locked signal and how to use it?*

Memory IP and Read

- IP is available for BRAM
- Memory Content Read is not available till video 2020.1
  Solution: Toggle the memory object to read the values

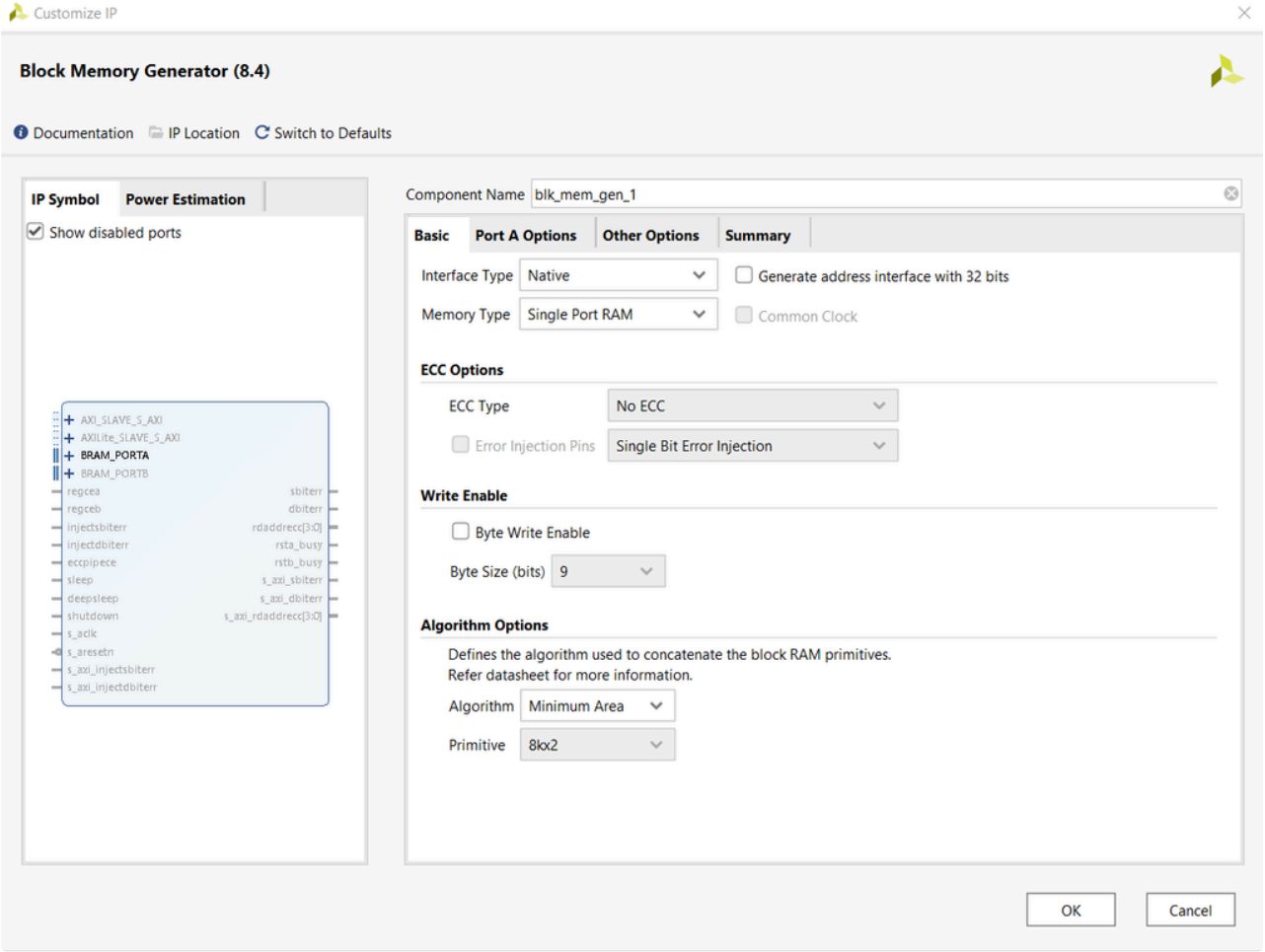
Instance the BRAM

> IP Catalog

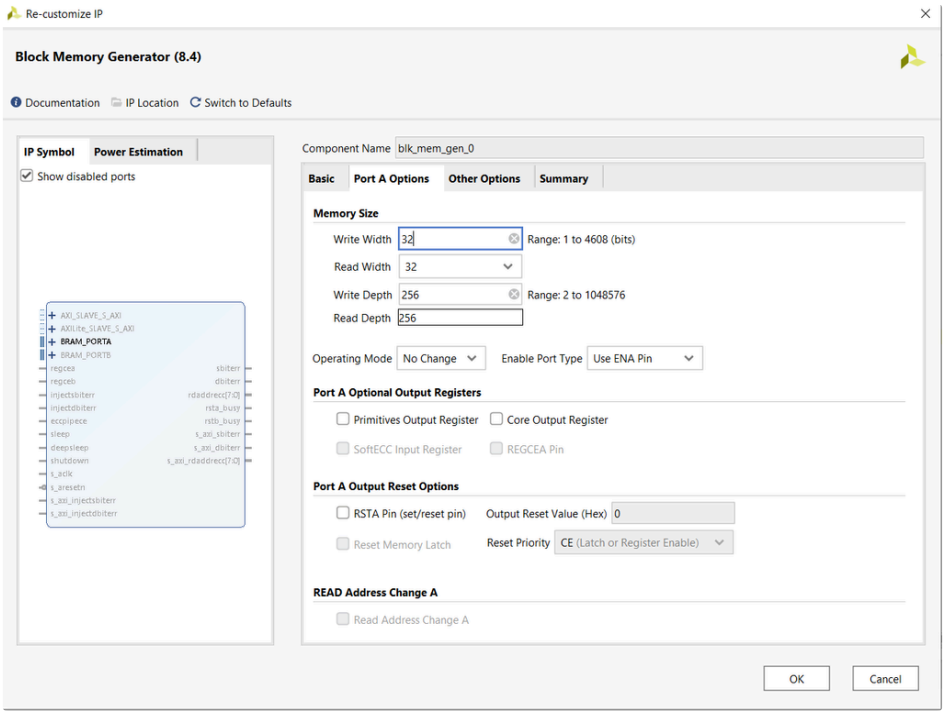


> IP Catalog > Block Memory Generator

- Basic → Singe Port RAM

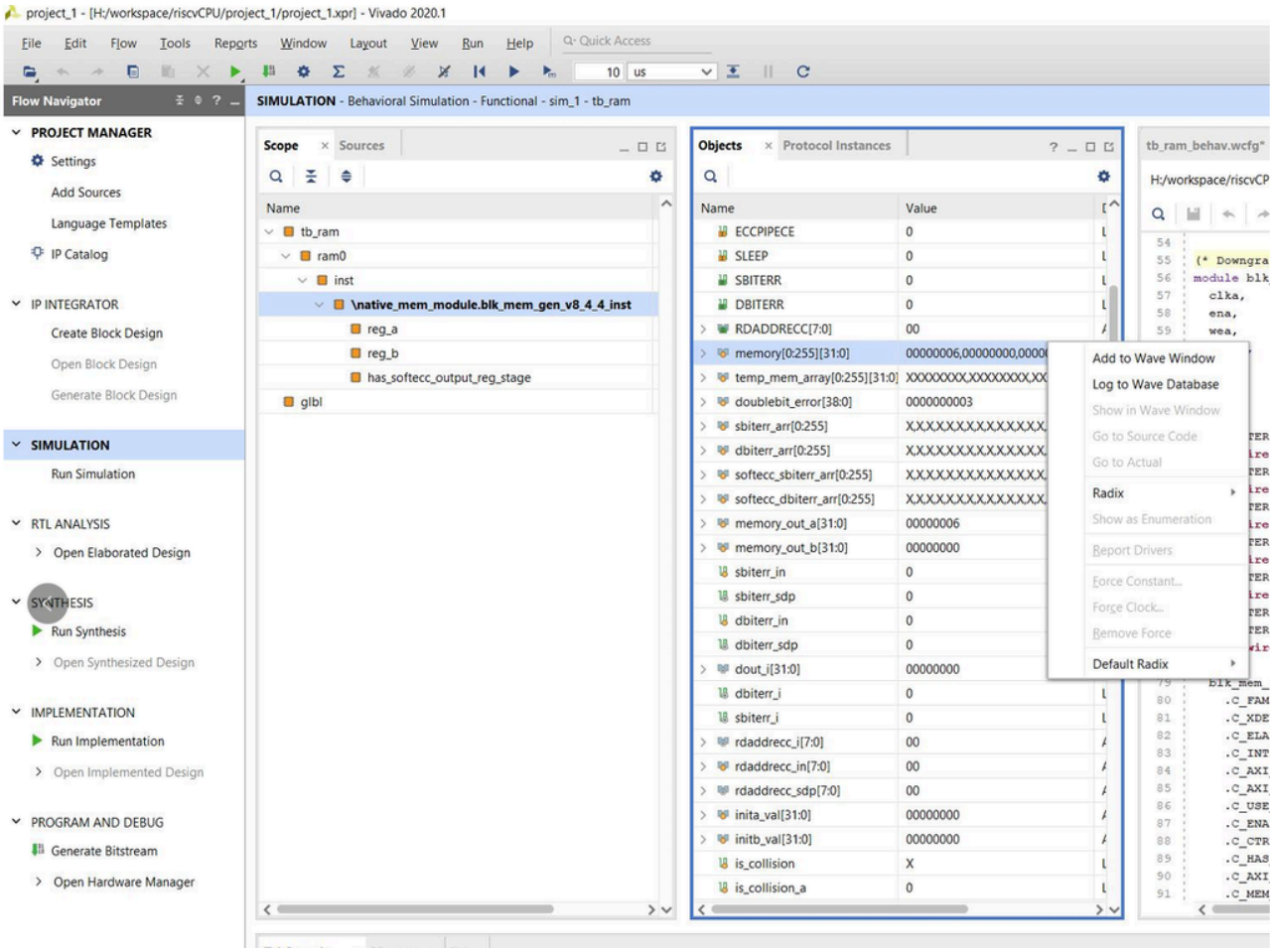


- Port A Options → W/R Width Depth Specification
  Remember to uncheck the "*Primitives Output Register*" otherwise, the Extra cycle read latency will cause the **Single Cycle Processing** to fail.

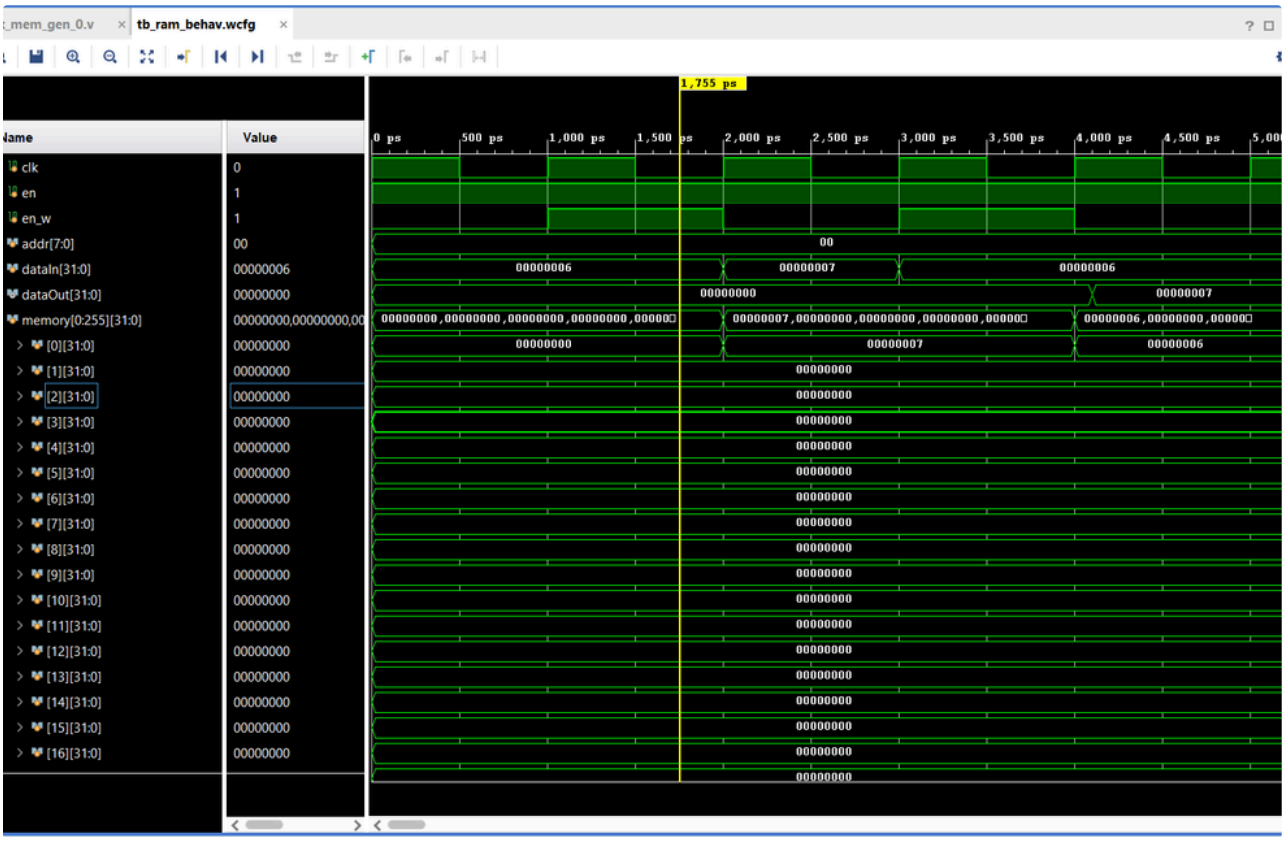


Simulation - Memory Read

- In the simulation phase → Add the *memory[0:255][31:0]* object to the **Wave Window**



- Re-Run the simulation

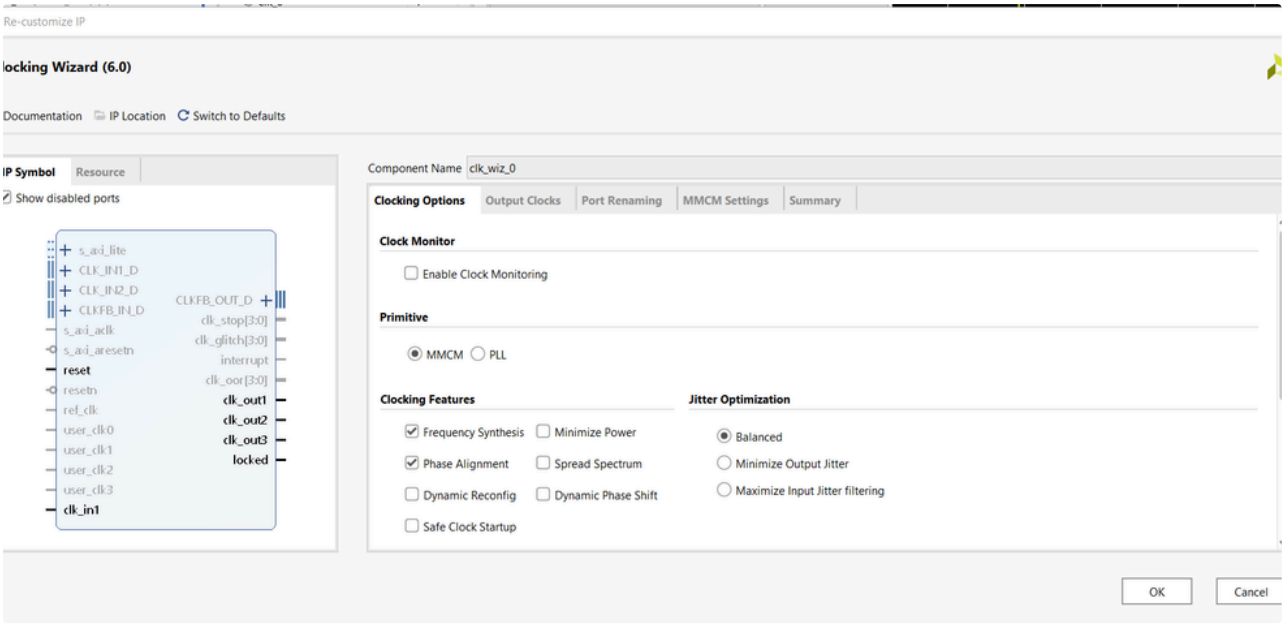


Clk Shift

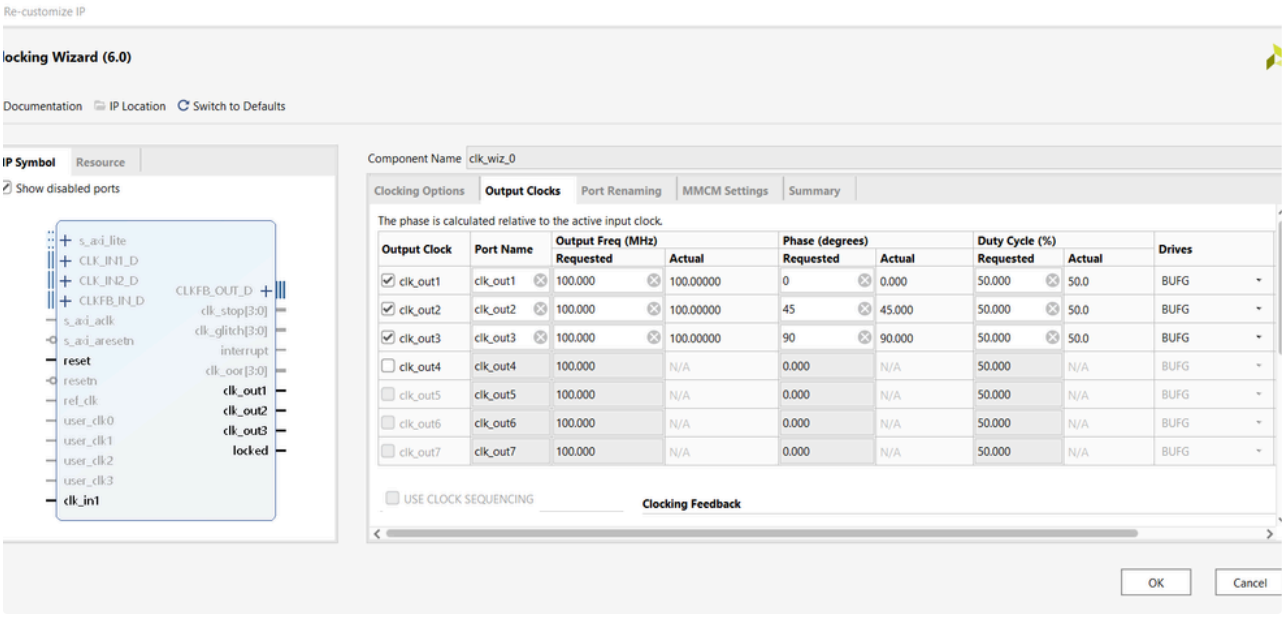
- The Clocking Wizard allows you to generate clocks with different frequencies/phases.

Instance

> IP Catalog > Clocking Wizard

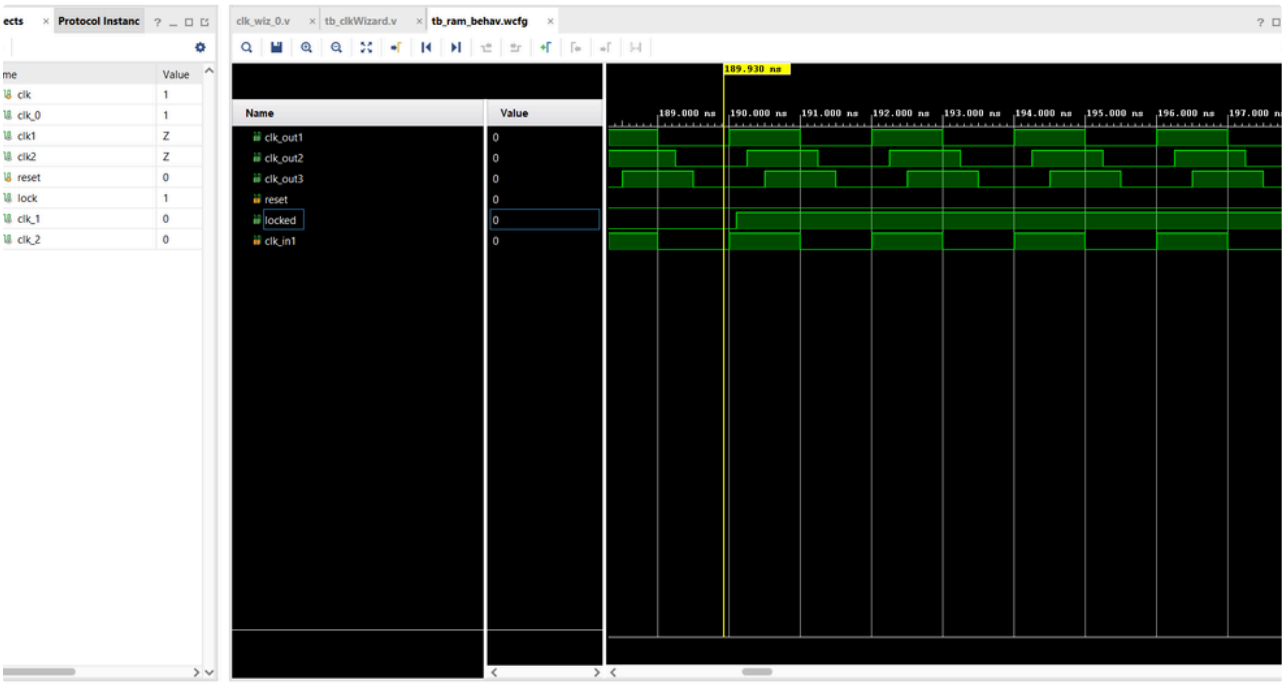


> Output Clocks → Phase Shift (Degrees)



Simulation

- Generate three new clock



Tips: What is the *locked signal and how to use it?*