

# ECE505 Project RISC-V Processor - IP Cores

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## IP Cores Instruction

### Tips:

change top-level: `"boost::filesystem::remove: The process cannot access the file because another process "`

locked signal in MMCM: [What is the locked signal and how to use it?](#)

## Memory IP and Read

- IP is available for BRAM
- Memory Content Read is not available till video 2020.1  
Solution: Toggle the memory object to read the values

## Instance the BRAM

IP Catalog

clk\_wiz\_0.v   tb\_ram\_behav.wcfg   IP Catalog

Cores | Interfaces

Search: ram (8 matches)

Name	AXI4	Status	License	VLNV
Vivado Repository				
Basic Elements				
Registers, Shifters & Pipelining				
RAM-based Shift Register		Production	Included	xilinx.com:ip:xc_shift_ram:12.0
Embedded Processing				
Memory and Memory Controller				
AXI BRAM Controller	AXI4	Production	Included	xilinx.com:ip:axi_bram_ctrl:4.1
LMB BRAM Controller	AXI4	Production	Included	xilinx.com:ip:lmb_bram_if_cntlr:4.0
Memories & Storage Elements				
RAMs & ROMs				
Distributed Memory Generator		Production	Included	xilinx.com:ip:dist_mem_gen:8.0
RAMs & ROMs & BRAM				
Block Memory Generator	AXI4	Production	Included	xilinx.com:ip:blk_mem_gen:8.4
SDAccel DSA Infrastructure				
SDAccel OpenCL Programmable Region		Production	Included	xilinx.com:ip:ocl_block:1.0
Video & Image Processing				

Details

Name: Block Memory Generator

Version: 8.4 (Rev. 4)

Interfaces: AXI4

Description: The Xilinx LogiCORE IP Block Memory Generator replaces the Dual Port Block Memory and Single Port Block Memory LogiCOREs, but is not a direct drop-in replacement. It should be used in all new Xilinx designs. The core supports RAM and ROM functions over a wide range of widths and depths. Use this core to generate block memories with symmetric or asymmetric read and write port widths, as well as cores which can perform simultaneous write operations to separate locations, and simultaneous read operations from the same location. For more information on differences in interface and feature support between this core and the Dual Port Block Memory and Single Port Block Memory LogiCOREs, please consult the data sheet.

Status: Production

License: Included

- Basic → Single Port RAM

Customize IP

Block Memory Generator (8.4)

Documentation

IP Location

Switch to Defaults

AXI\_SLAVE\_S\_AXI

AXI4Lite\_SLAVE\_S\_AXI

BRAM\_PORTA

BRAM\_PORTB

regcea

regceb

injectsbiterr

injectdbiterr

eccpipece

sleep

deepsleep

shutdown

s\_ack

s\_aresetn

s\_axi\_injectsbiterr

s\_axi\_injectdbiterr

sbiterr

dbiterr

rdaddrecc[3:0]

rsta\_busy

rstb\_busy

s\_axi\_sbiterr

s\_axi\_dbiterr

s\_axi\_rdaddrecc[3:0]

Component Nameblk\_mem\_gen\_1

BasicPort A OptionsOther OptionsSummary

Interface TypeNativeGenerate address interface with 32 bits

Memory TypeSingle Port RAMCommon Clock

ECC Options

ECC TypeNo ECC

Error Injection PinsSingle Bit Error Injection

Write Enable

Byte Write Enable

Byte Size (bits)9

Algorithm Options

Defines the algorithm used to concatenate the block RAM primitives. Refer datasheet for more information.

AlgorithmMinimum Area

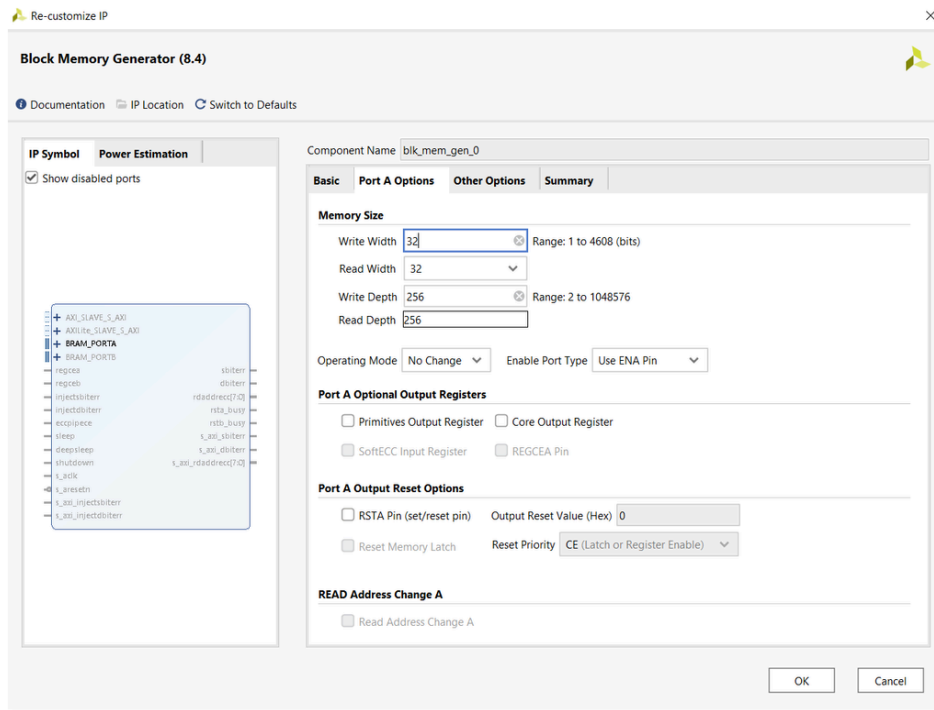
Primitive8kx2

OK

Cancel

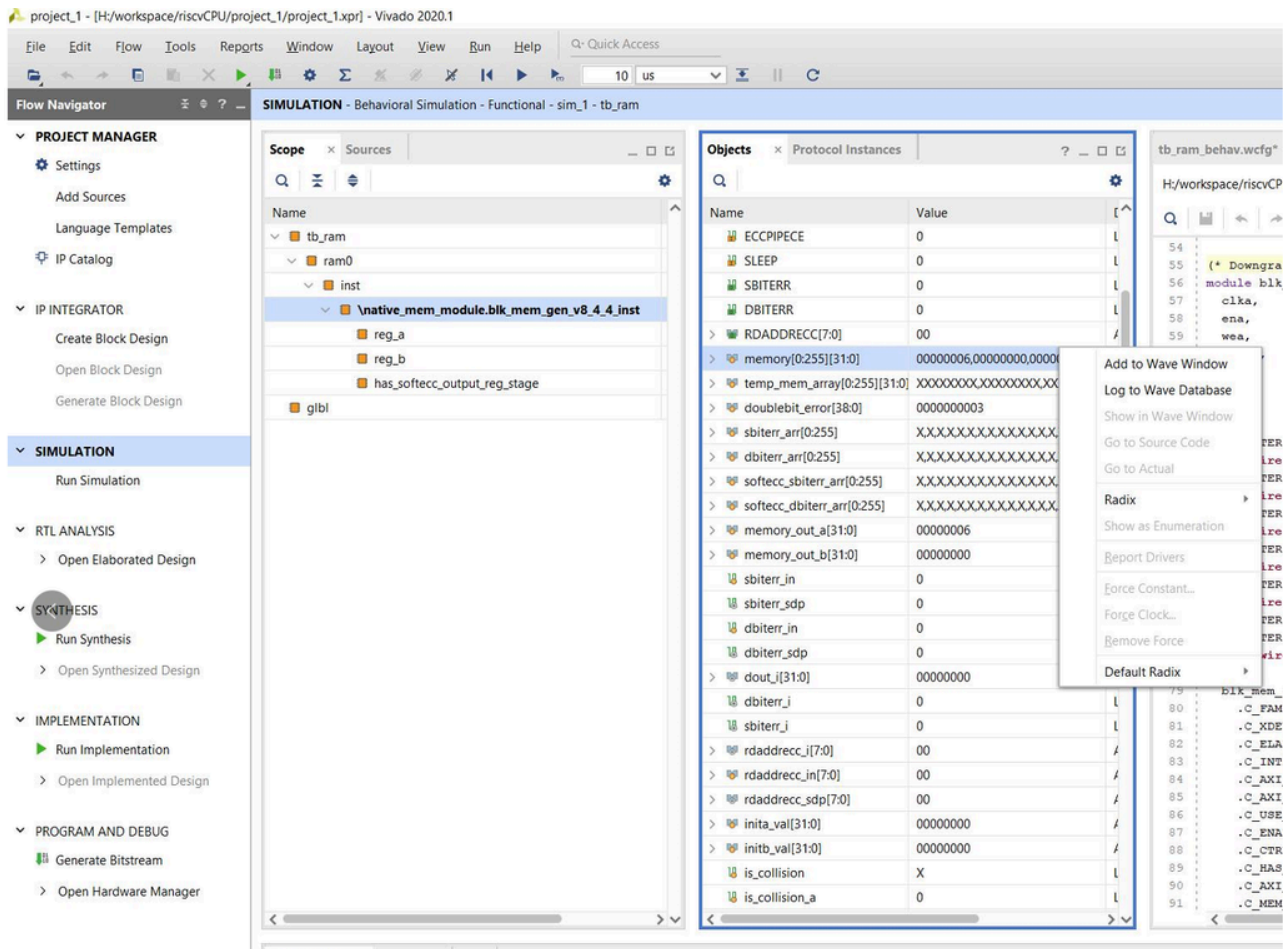
- Port A Options → W/R Width Depth Specification

Remember to uncheck the “*Primitives Output Register*” otherwise, the Extra cycle read latency will cause the **Single Cycle Processing** to fail.

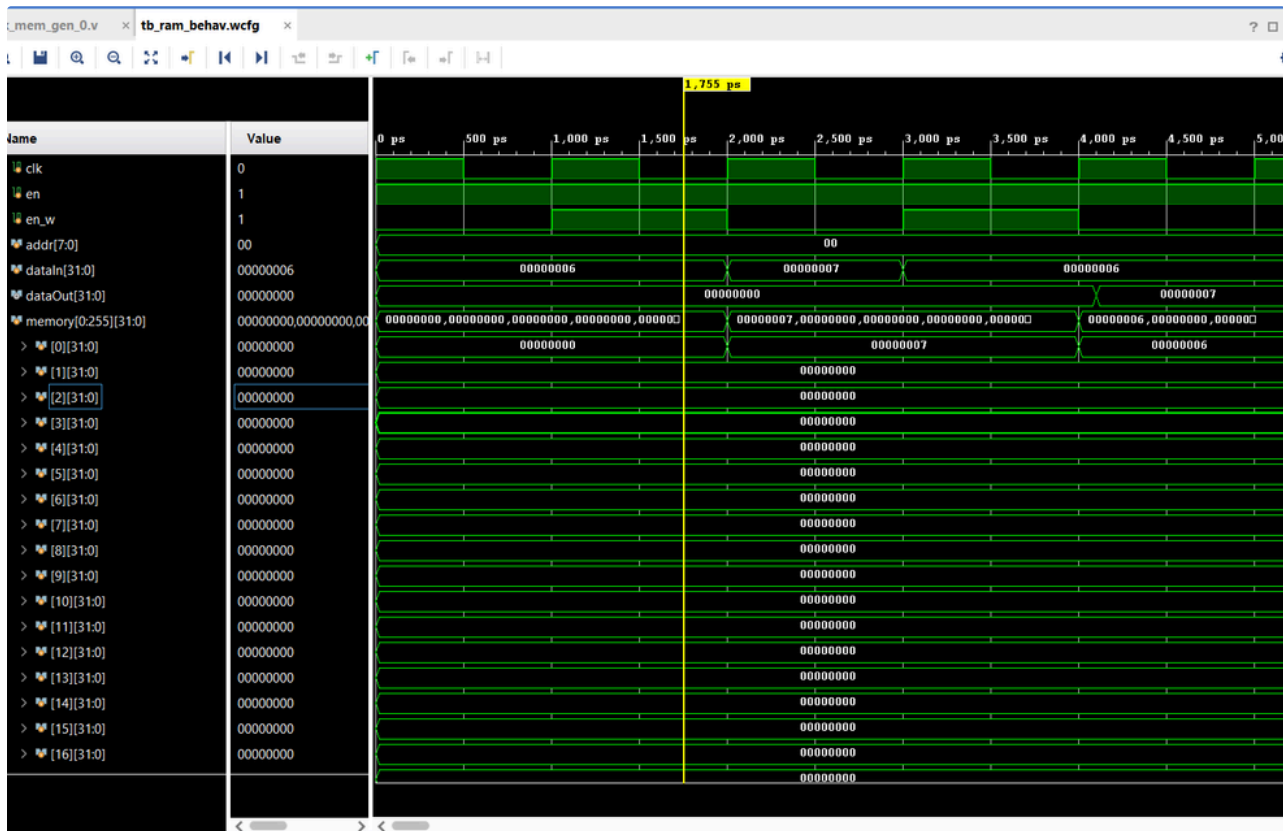


## Simulation - Memory Read

- In the simulation phase → Add the `memory[0:255][31:0]` object to the **Wave Window**



- Re-Run the simulation



## Clk Shift

- The Clocking Wizard allows you to generate clocks with different frequencies/phases.

## Instance

IP Catalog > Clocking Wizard

Re-customize IP

**Clocking Wizard (6.0)**

Documentation IP Location Switch to Defaults

Component Name: clk\_wiz\_0

**Clocking Options** Output Clocks Port Renaming MMCM Settings Summary

**Clock Monitor**

☐ Enable Clock Monitoring

**Primitive**

☒ MMCM ☐ PLL

**Clocking Features**

☒ Frequency Synthesis ☐ Minimize Power

☒ Phase Alignment ☐ Spread Spectrum

☐ Dynamic Reconfig ☐ Dynamic Phase Shift

☐ Safe Clock Startup

**Jitter Optimization**

☒ Balanced ☐ Minimize Output Jitter

☐ Maximize Input Jitter filtering

OK Cancel

## Output Clocks → Phase Shift (Degrees)

Re-customize IP

### locking Wizard (6.0)

Documentation IP Location Switch to Defaults

IP Symbol Resource

Show disabled ports

Component Name: clk\_wiz\_0

Clocking Options Output Clocks Port Renaming MMCM Settings Summary

The phase is calculated relative to the active input clock.

Output Clock	Port Name	Output Freq (MHz)		Phase (degrees)		Duty Cycle (%)		Drives
		Requested	Actual	Requested	Actual	Requested	Actual	
<input checked="" type="checkbox"/> clk_out1	clk_out1	100.000	100.000000	0	0.000	50.000	50.0	BUFG
<input checked="" type="checkbox"/> clk_out2	clk_out2	100.000	100.000000	45	45.000	50.000	50.0	BUFG
<input checked="" type="checkbox"/> clk_out3	clk_out3	100.000	100.000000	90	90.000	50.000	50.0	BUFG
<input type="checkbox"/> clk_out4	clk_out4	100.000	N/A	0.000	N/A	50.000	N/A	BUFG
<input type="checkbox"/> clk_out5	clk_out5	100.000	N/A	0.000	N/A	50.000	N/A	BUFG
<input type="checkbox"/> clk_out6	clk_out6	100.000	N/A	0.000	N/A	50.000	N/A	BUFG
<input type="checkbox"/> clk_out7	clk_out7	100.000	N/A	0.000	N/A	50.000	N/A	BUFG

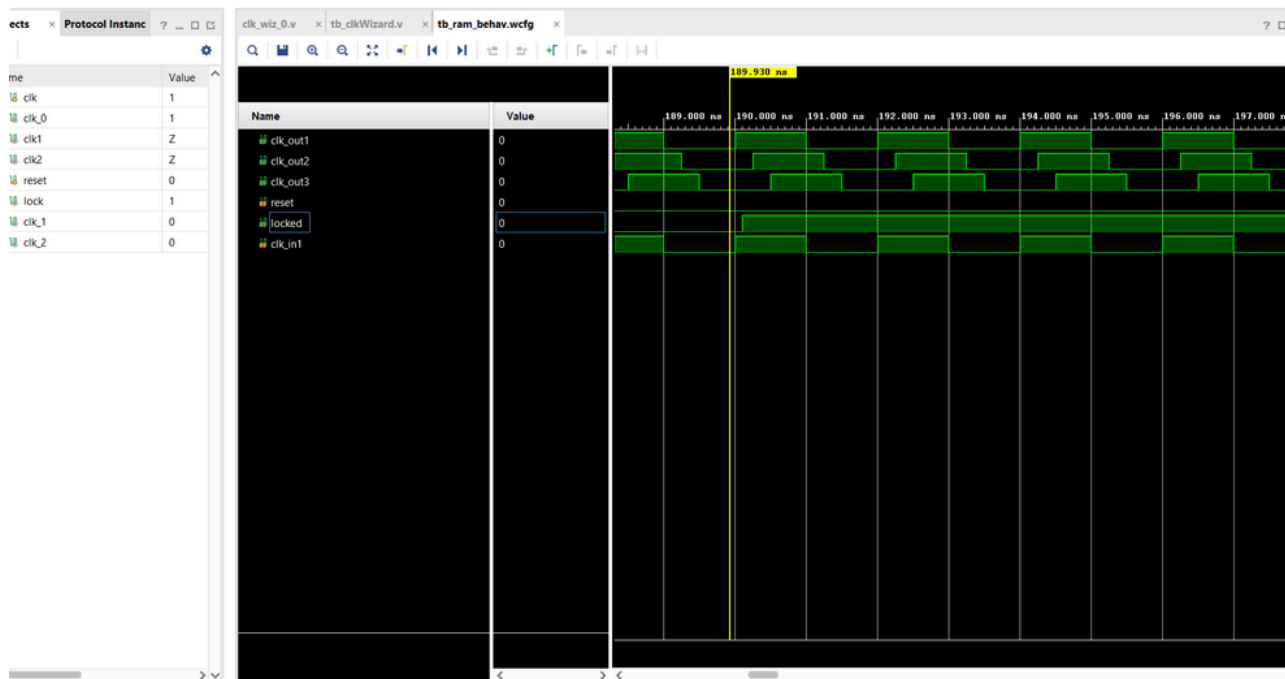
☐ USE CLOCK SEQUENCING

Clocking Feedback

OK Cancel

## Simulation

- Generate three new clock



Tips: What is the locked signal and how to use it?