CDA 4203L Spring 2025
Computer System Design Lab
Lab 4 – Finite State Machine on FPGA

Lab Date: Mar. 4
Report Due Date: Mar. 14 on Canvas

Teaming allowed. No hardware needed, only ISE.
No demonstration is needed.

Objective: To learn and practice synthesizable Finite State Machine construction.

Note: This lab does not need your FPGA boards. It is a simulation-only lab with ISE. No demonstration is needed to the TAs.

Description: Design an FSM for use as a controller for a vending machine. The system has five (5) inputs: quarter, nickel, dime, soda, and diet. The quarter input will go high, then go low when a 25¢ coin is added to the machine. The dime and nickel inputs work in a similar manner for the 10¢ and 5¢ coins. The sodas (regular and diet) cost 45¢ each. The user presses the soda button to select a regular soda, and the diet button to select a diet soda. The GiveSoda output will pulse high, then low when a regular soda is released. Similarly, the GiveDiet output will pulse high, then low when a diet soda is released. There will be no change back. For example, if user inserts two 25 cents which is 50 cents (or for instance, five 10 cents which is 50 cents, or for example four 10 cents and then a 25 cents, which is 65 cents), soda is released but no change is returned. When the user has inserted enough money to buy a soda, the user cannot insert more money. You look at the soda/diet input then and release the can and go back to start state. Use Moore or Mealy as appropriate.

Your design must be a pure FSM based on the templates provided in the file FSM Templates.docx. This means that there should be no complex operations (addition, subtraction) in your design. It must function solely on states and transitions.

(50 pts.) Design the vending machine FSM and verify its functionality using simulation.

Deliverables (Only one .zip file per group) A zipped file (.zip) which includes these two items:
(a) Your group design files (Verilog Models and test benches). (b) A concise PDF group report (that includes your Verilog code and simulation results) needs to be included in the submitted .zip file.

Who submits? Only the team leader identified on Canvas needs to submit. TAs will mark all group members based on that equally. Do not submit the same .zip file for each student.

PDF Report Organization to be included in your ZIP submission (A template is provided on Canvas):

- □ Cover sheet and the state diagram and a brief description
- □ Verilog Code, Test Bench, and Simulation Results (Waveforms)
- □ Feedback: Hours spent, Exercise difficulty (Easy, Medium, Hard)
- □ You need to submit your group report on Canvas in ZIP format (only one .zip file).