Task 1

```
#5 operation = 4'b1100; // SRL
#5 operation = 4'b1110; // SRA
#5 operation = 4'b0000; // AND
#5 operation = 4'b0001; // OR
#5 operation = 4'b1000; // EQ
#5 operation = 4'b1000; // EQ
#5 operation = 4'b1010; // LT
#5 operation = 4'b1010; // LT
#5 operation = 4'b1011; // GEQ
    27
28
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37
                                                                                                              1 `timescale 1ns / 1ps
                                                                                                                module alu (
input [31:0] A,
input [31:0] B,
input [3:0] operation,
output reg signed [31:0] ALUResult
                                                                                                           // Modify A and B for second test case (Signed Arithmetic)

A = 10; B = 5;
operation = 4'b0010; // ADD
#5 operation = 4'b0110; // SUB
    38
    39
40
41
42
43
                    // Wait and finish simulation
#10 $finish;
 [2025-02-26 20:04:51 UTC] iverilog '-Wall' '-g2012' design.sv testbench.sv && unbuffer vvp a.out
Time | A
                      l B
                                     | OpCode | ALUResult
                   -12 I
                                          -5 | 0000
                                                                            -16
5000 I
                                              -5 | 0010
                                                                                -17
10000
                        -12
                                                -5 | 0110
                                                                                   -7
                         -12
                                                -5 | 0111
                                                                                   60
15000
20000
                         -12
                                                -5 | 1111
25000
                         -12
                                                -5 | 0100
                                                                                    0
30000
                        -12
                                                -5 | 1100
                                                                                    0
                        -12
35000
                                                -5 | 1110
                         -12
                                                -5 I 0000
                                                                                  -16
45000
                         -12
                                                -5 | 0001
                                                                                   -1
50000
                        -12
                                                -5 | 0011
                                                                                   15
55000
                         -12
                                                -5 I 1000
                                                                                    0
60000
                         -12
                                                -5 | 1001
65000
                         -12
                                                -5 | 1010
70000
                          10
                                                 5 | 0010
                                                                                   15
75000
                          10
                                                 5 | 0110
testbench.sv:43: $finish called at 85000 (1ps)
```

Task 2

```
#5 operation = 4'b1100; // SRL

#5 operation = 4'b1110; // SRA

#5 operation = 4'b0000; // AND

#5 operation = 4'b001; // OR

#5 operation = 4'b001; // KNO

#5 operation = 4'b1001; // KNO

#5 operation = 4'b1000; // LT

#5 operation = 4'b1010; // LT

#5 operation = 4'b1011; // GEQ
                                                                                                          1 'timescale 1ns / 1ps
                                                                                                          2 module alu (
4 input [31:0] A,
5 input [31:0] B,
6 input [31:0] Operation,
7 output reg signed [31:0] ALUResult
                                                                                                        // Modify A and B for second test case (Signed Arithmetic)

A = 10; B = -5;
operation = 4'b0010; // ADD
#5 operation = 4'b0110; // SUB
   38
39
40
41
42
43
                    // Wait and finish simulation
#10 $finish;
⊚ Log

    Share

-5 I 0000
                  -12 I
5000 I
                                             -5 | 0010
                                                                              -17
                      -12
10000
                        -12
                                               -5 | 0110
15000
                                              -5 | 0111
                        -12
25000
                        -12
                                              -5 | 0100
                        -12
                                               -5 | 1100
35000
                        -12
                                              -5 | 1110
                        -12
                                                   1 0000
                                                                                -16
                                              -5 | 0001
-5 | 0011
45000
                        -12
50000
                        -12
55000
                        -12
                                               -5 I 1000
                                                                                 0
60000
                        -12
                                                       1001
                                              -5 | 1010
-5 | 0010
65000
                        -12 I
                         10
70000
75000 I
                         10
                                               -5 | 0110
                                                                                15
testbench.sv:43: $finish called at 85000 (1ps)
```

Task 3

```
1 'timescale 1ns / 1ps
                                                                                                                                         1 `timescale 1ns / 1ps
       module alu_testbench();
reg [31:0] A;
reg signed [31:0] B;
reg [3:0] operation;
wire signed [31:0] ALUResult;
                                                                                                                                            module alu (
input [31:0] A,
input [31:0] B,
input [3:0] operation,
output reg signed [31:0] ALUResult
                                                                                                                                         wire signed [31:0] ALUResult;

// Instantiate the ALU module
alu ut (.A(A), B(B), operation(operation),
ALUResult(ALUResult));

initial begin
// Display header for readability
Sdisplay("Time | A | B | OpCode |
ALUResult ();

Sdisplay("");
o Log < Share
 0 | 4294967284 |
5000 | 4294967284 |
                                                          -5 | 0010 | |
-5 | 0110 | |
-5 | 01111 |
-5 | 01111 |
-5 | 0100 |
-5 | 1111 |
-5 | 0100 |
-5 | 1110 |
-5 | 0000 |
-5 | 0001 |
-5 | 0001 |
-5 | 0100 |
-5 | 0110 |
-5 | 0110 |
-5 | 00110 |
-5 | 00110 |
                                                                                                     -17
                                                          -5 | 0010
10000 | 4294967284 |
15000 | 4294967284 |
20000 | 4294967284 |
25000 | 4294967284 |
                                                                                                         -7
                                                                                                         60
0
 30000
                 4294967284
 35000
                 4294967284
                4294967284
4294967284
4294967284
 40000
45000
                                                                                                         -1
15
0
1
 50000
55000
                4294967284
 60000
65000
                 4294967284
 70000
                   10 I
10 I
 75000 I
                                                             -5 | 0110
                                                                                                         15
 testbench.sv:43: $finish called at 85000 (1ps)
```

```
Task 4
                     1 'timescale 1ns / 1ps
                                                                                                                                                                                                                                                                                                                                                        1 `timescale 1ns / 1ps
                    module alu_testbench();
4 reg [31:0] A;
5 reg [31:0] B;
6 reg [3:0] operation;
7 wire signed [31:0] ALUResult;
                                                                                                                                                                                                                                                                                                                                                            module alu (
input [31:0] A,
input [31:0] B,
input [3:0] operation,
output reg signed [31:0] ALUResult
                7 wire signed [31:0] ALUResult;
9 alu uut (.A(A), .B(B), operation(operation),
-ALUResult(ALUResult));
11 initial begin // Disploy header for readability
14 ALURESULT // Day("Time | A | B | OpCode |
15 ALURESULT // Day("Time | A | B | OpCode |
16 ALURESULT // Day("Time | A | B | OpCode |
17 ALURESULT // Day("Time | A | B | OpCode |
18 ALURESULT // Day("Time | A | B | OpCode |
19 ALURESULT // Day("Time | A | B | OpCode |
10 ALURESULT // Day("Time | A | B | OpCode |
11 ALURESULT // Day("Time | A | B | OpCode |
12 ALURESULT // Day("Time | A | B | OpCode |
13 ALURESULT // Day("Time | A | B | OpCode |
14 ALURESULT // Day("Time | A | B | OpCode |
15 ALURESULT // Day("Time | A | B | OpCode |
16 ALURESULT // Day("Time | A | B | OpCode |
17 ALURESULT // Day("Time | A | B | OpCode |
18 ALURESULT // Day("Time | A | B | OpCode |
19 ALURESULT // Day("Time | A | B | OpCode |
10 ALURESULT // Day("Time | A | B | OpCode |
10 ALURESULT // Day("Time | A | B | OpCode |
10 ALURESULT // Day("Time | A | B | OpCode |
10 ALURESULT // Day("Time | A | B | OpCode |
10 ALURESULT // Day("Time | A | B | OpCode |
10 ALURESULT // Day("Time | A | B | OpCode |
10 ALURESULT // Day("Time | A | B | OpCode |
11 ALURESULT // Day("Time | A | B | OpCode |
12 ALURESULT // Day("Time | A | B | Opcode |
13 ALURESULT // Day("Time | A | B | Opcode |
14 ALURESULT // Day("Time | A | B | Opcode |
15 ALURESULT // Day("Time | A | B | Opcode |
16 ALURESULT // Day("Time | A | B | Opcode |
16 ALURESULT // Day("Time | A | B | Opcode |
17 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18 ALURESULT // Day("Time | A | B | Opcode |
18
                                                                                                                                                                                                                                                                                                                                                     ich.sv && unbuffer vvp a.out
    0 | 4294967284 | 4294967291 | 0000 |
5000 | 4294967284 | 4294967291 | 0010
10000 | 4294967284 | 4294967291 | 0110
15000 | 4294967284 | 4294967291 | 0110
15000 | 4294967284 | 4294967291 | 1111
                                                                                                                                                                                                                                           -16
                                                                                                                                                                                                                                                        -17
       25000
                                    1 4294967284
                                                                                                      1 4294967291
                                                                                                                                                                      0100
     30000
35000
40000
45000
                                             4294967284
4294967284
4294967284
                                                                                                     | 4294967291
| 4294967291
| 4294967291
| 4294967291
                                                                                                                                                                            1100
1110
0000
                                                                                                                                                                                                                                                              -16
                                             4294967284
                                                                                                                                                                              0001
                                                                                                                                                                                                                                                                 -1
       50000
                                       1 4294967284
                                                                                                      1 4294967291
                                                                                                                                                                              0011
                                                                                                                                                                                                                                                                15
       55000 | 4294967284 | 4294967291
60000 | 4294967284 | 4294967291
65000 | 4294967284 | 4294967291
                                                                                                                                                                            1000
1001
1010
```