深圳市富满电子集团股份有限公司
SHENZHEN FUMAN ELECTRONICS CO., LTD

# FM6363 Control and Programming Guide

## Control Instructions

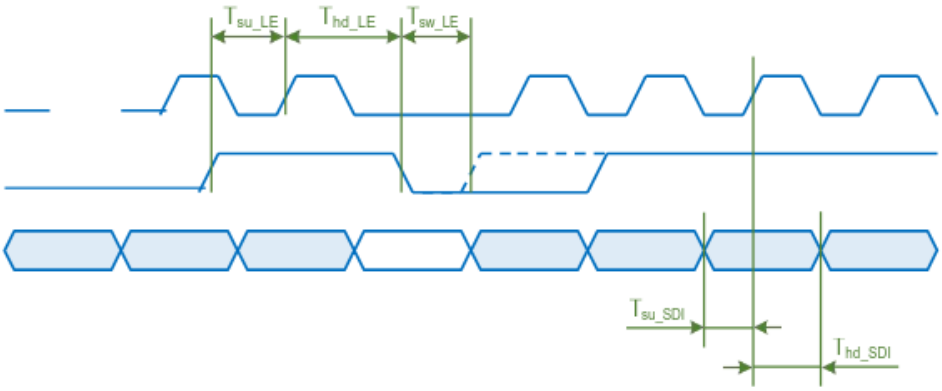
The chip contains a simple 16-bit shift register, and the grayscale value and configuration value are latched into the shift register. The control command is parsed by counting the length of the LE signal. Different LE lengths represent different commands. For example, an LE signal with a length of 1 represents the "Data Latch" command, which is used to control the shift register to latch the grayscale value and send the 16-bit data in the shift register to the SRAM. Table 1 lists all the commands and their meanings.

Table 1. Control Instructions:

| Instruction | LE | Description |
|---|---|---|
| DATA_LATCH | 1 | Latch 16-bit data to SRAM |
| WR_DBG | 2 | Write debug register (register 5) |
| VSYNC | 3 | Update display data |
| WR_CFG1 | 4 | Write configuration register 1 |
| WR_CFG2 | 6 | Write configuration register 2 |
| WR_CFG3 | 8 | Write configuration register 3 |
| WR_CFG4 | 10 | Write configuration register 4 |
| EN_OP | 12 | Enable all output channels |
| DIS_OP | 13 | Disable all output channels |
| PRE_ACT | 14 | Write enable |
| MBIST | 15 | Enable SRAM checksum read status |

*Note 1: The length of LE refers to the number of rising edges of DCLK when LE is high. As shown in Figure 2, the length of the first LE signal is 1, which means that the command is a "Data Latch" command. Note 2: PRE_ACT and EN_OP are sent first in each frame, and then the register is configured. Before configuring each register, PRE_ACT must also be sent first.*

## LE waveform



The setup and hold time of LE signal and SDI signal are shown in the following table:

Table 2. Dynamic characteristics of LE and SDI signals

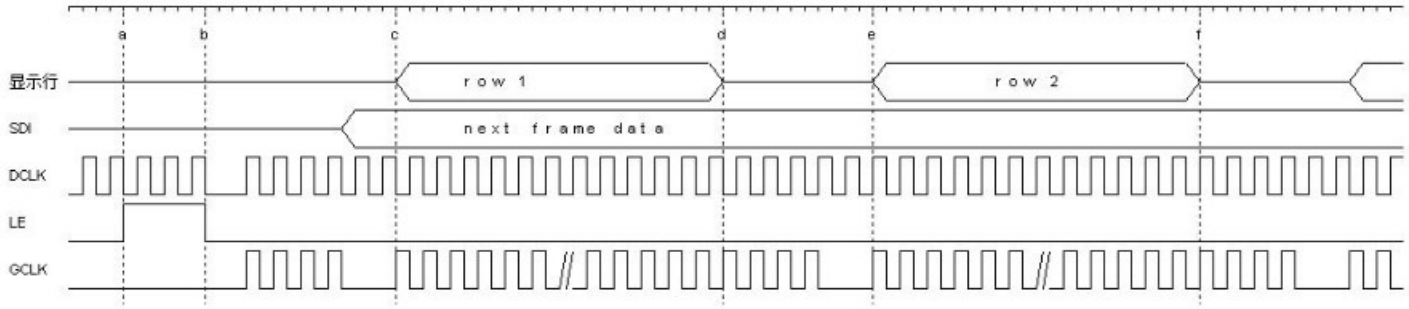
| **Signal name** | **MIN** | **Notes** |
|---|---|---|
| $T_{su}$_LE | 7ns | |
| $T_{hd}$_LE | 7ns | |
| $T_{sw}$_LE | 10ns | |
| $T_{su}$_SDI | 3ns | |
| $T_{hd}$_SDI | 3ns | |

The grayscale data is latched by the "Data Latch" command. The first 16-bit data is used as the first line of data for channel 15, the second 16-bit data is used as the first line of data for channel 14, and the 17th 16-bit data is used as the second line of data for channel 15. Table 3 shows the corresponding data instructions for all 64 lines of data.

Table 3. Grayscale data loading order

| Data Order | Line | Channel |
|---|---|---|
| 1 | Line 1 | Channel 15（OUT15） |
| 2 | | Channel 14（OUT14） |
| …… | | …… |
| 16 | | Channel 0（OUT0） |
| 17 | Line 2 | Channel 15（OUT15） |
| 18 | | Channel 14（OUT14） |
| …… | | …… |
| 32 | | Channel 0（OUT0） |
| …… | | |
| 497 | Line 64 | Channel 15（OUT15） |
| 498 | | Channel 14（OUT14） |
| …… | | …… |
| 512 | | Channel 0（OUT0） |

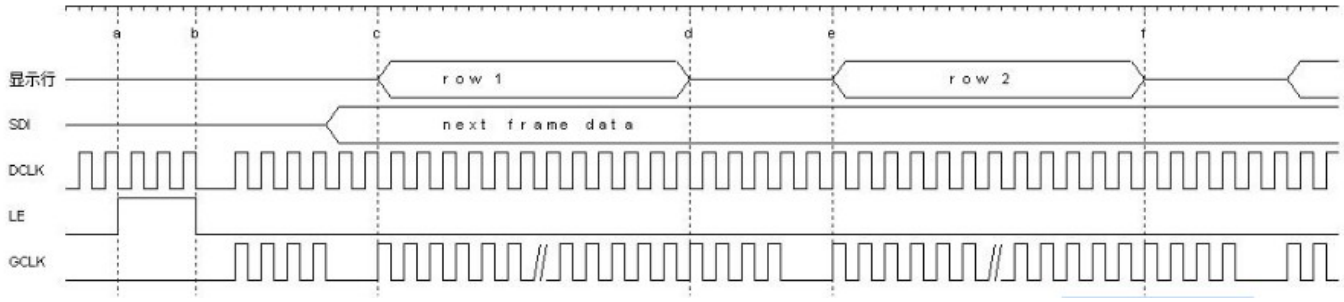
Display Timing




The display timing is shown in the figure above:

a) **a->b**, first send **VSYNC** (LE high level of **3 DCLK** width), change frame, and start latching the data of the next frame after time b;
b) **b->c**, send **4 GCLKs;**
c) **c->e**, the display time of one line, a total of **74 GCLKs;**
d) **d**, line change time;
e) **d->e**, line change time, after time d, it is necessary to send **4 GCLKs** continuously (included in **74GCLKs** );
f) **e** is the start of the next line.

Configuration register timing




g) **a->b**, send **PRE_ACT** (**14 DCLK** width LE high level);
h) **c->d**, send **EN_OP** (**12 DCLK** width LE high level);
i) **e->f**, send **PRE_ACT**;
j) **g->h**, write register 1 (**4 DCLK** width LE high level);
k) **i->j**, send **PRE_ACT;**
l) **k->l**, write register 2 (**6 DCLK** width LE high level);
m) Configure register 3 and register 4 according to steps k) and l).

Config Registers

CFG 1

| Bit | Name | Description |
|---|---|---|
| 15 | OPEN_DET | Open circuit detection:<br>0: Disable<br>1: Enable |
| 14 | GCLK_N | This bit controls the number of GCLKs for frames and lines:<br>1: 6 GCLKs for the frame header and 78 GCLKs for each subsequent line;<br>0: 4 GCLKs for the frame header and 74 GCLKs for each subsequent line; |
| 13:8 | SCAN_LINE | Number of scan lines:<br>0: 1 line<br>1: 2 lines<br>2: 3 lines<br>……<br>63: 64 lines |
| 7:6 | OPT | Low gray dot/high light coupling optimization:<br>00: Test mode<br>01: Level 2 optimization (recommended value)<br>10: Level 3 optimization (optimized high light coupling recommended value)<br>11: Test mode |
| 5:4 | TEST | CFG1<5:4>=01 & CFG3<9:8>=11 Enable REG5<8:0><br><br>CFG1<5:4>=01 Enable REG4<3:1><br><br>CFG1<5:4>=01 & CFG3<9:8>=01<br>Enable CFG_DBGX configuration (not listed) |
| 3 | Cross-board Coupling | 0: Off<br>1: On |
| 2:0 | TEST | Force minimum grayscale output:<br>001~111 Output grayscale 1~7 respectively |

CFG 2

| Bit | Name | Description |
|---|---|---|
| 15 | TEST | 0: Line scan configuration 33~64 scans (default)<br>1: Line scan configuration 1~64 scans |
| 14:10 | ADJ | Blanking control register:<br>1-31 levels correspond to register cfg2[14:10]=00000-11111<br>Enable register cfg3[2]<br>Recommended R=31, G=28, B=23 |
| 9 | I_DIV4N | Current gear adjustment<br>1: High current gear<br>0: Low current gear |
| 8:1 | IGAIN | Constant current source output configuration register,<br>IOUT=19*IGAIN/(Rext*256) @ I_DIV4N=1<br>IOUT=19*IGAIN/(Rext*1024) @ I_DIV4N=0<br>Igain≥64 (required) |
| 0 | Blanking mode | 0: Fixed blanking (default)<br>1: Pulse blanking |

CFG 3

| Bit | Name | Description |
|---|---|---|
| 15 | Reserved | -- |
| 14:12 | TEST | Adjusts VDS (for core circuit), range 160mV~520mV<br>From 000~111, the configured VDS level increases in sequence |
| 11:10 | TEST | PWM output delay<br>Default configuration "00" |
| 9:8 | TEST | Scan chain configuration<br>Configure CFG1<5:4>=01 before writing |
| 7:4 | PWM _ALL | Low gray color cast compensation adjustment<br>Levels 1-16 correspond to registers cfg3[7:4]=1111-0000<br>Enable register cfg4[14] |
| 3 | TEST | Frequency multiplier switch<br>0: Off<br>1: On |
| 2 | UP_SEL | Void switch:<br>0: Off<br>1: On |
| 1:0 | VLDO | VLDO voltage<br>4 levels of voltage adjustable |

CFG 4

| Bit | Name | Description |
|---|---|---|
| 15 | TEST | Blanking Widening 1GCLK<br>0: Off<br>1: On |
| 14 | PWM_ADD_EN | Low Gray Color Cast Compensation Switch<br>0: Off<br>1: On |
| 13 | TEST | SDI to SDO Delay Control<br>0: Delay<br>1: No Delay |
| 12 | Non_clp_en | 0: Off<br>1: On |
| 11:10 | TEST | Channel Closing Speed<br>00: Slowest<br>11: Fastest |
| 9:8 | TEST | Channel Opening Speed<br>00: Slowest<br>11: Fastest |
| 7 | OPEN_SCAN | Open Data Write Enable<br>0: No Update<br>1: Updateable |
| 6 | TEST | Clamp Switch<br>0: Off<br>1: On |
| 5:4 | TEST | Difference between Blanking (V+) and Clamp (V-)<br>The upper two bits of VA |
| 3 | TEST | Force PWM to output full brightness grayscale<br>0: Off<br>1: On<br>Used with open circuit |
| 2 | TEST | Black screen energy saving switch<br>0: Off<br>1: On |
| 1 | VRG_BUF | VRG_BUF bias current<br>0: Default<br>1: Double |
| 0 | TEST | Display grayscale is halved<br>0: Off (default)<br>1: On |

CFG 5

| Bit | Name | Description |
|---|---|---|
| 15 | Reserved | -- |
| 14 | | Clamp/Blanking Enhancement<br>0: Disable (default)<br>1: Enable |
| 13 | Non_clp_v_sel | 0: (default)<br>1: |
| 11:12 | | The difference between blanking (V+) and clamping (V-)<br>The lower two bits of VA |
| 10 | | Blanking Enhancement<br>0: Disable (default)<br>1: Enable |
| 9 | | Clamp Enhancement<br>0: Disable (default)<br>1: Enable |
| 8 | | CFG1~4 Value Reading<br>0: Disable<br>1: Enable |
| 7 | Reserved | -- |
| 5:6 | TEST | 00: SDO output SDI<br>01: SDO output is always 0<br>10: SDO output LDO<br>11: SDO output VGR |
| 4:2 | | 010 Automatic current gear adjustment<br>000/001/111 correspond to the 4 gears of automatic gear shifting |
| 0:1 | | 00/01: Open circuit detection<br>11: Forced open circuit<br>10: Forced normal |

Main interface settings

1. Grayscale
**FM6363** uses dual-edge display, please calculate the grayscale according to the dual-edge of **GCLK**

2. Refresh rate
The refresh rate is fixed at 8 times, **74 GCLKs** per line, register value **cfg1[5:4]=11, cfg1[14]=0.**

3. Refresh frequency
Fixed at 8 times, recommended refresh frequency **3840Hz**

## Extended interface suggestions

1. Blanking settings
To turn on the blanking function, use the check menu. When checked, **cfg3[2]=1**, unchecked **cfg3[2]=0**. To adjust the blanking capability, use the left and right sliders, and the right side with the up and down menu. There are 32 levels in total, and levels 0-31 correspond to registers **cfg2[14:10]=00000-11111** respectively.
The default value is checked, and the levels are: R=31, G=25, B=23

2. Low gray and white balance adjustment
To turn on the low gray and white balance adjustment, use the check menu. When checked, **cfg4[14]=1**, unchecked **cfg4[14]=0**. To adjust the low gray and white balance, use the left and right sliders, and the right side with the up and down menu. There are 16 levels in total, and levels 1-16 correspond to registers **cfg3[7:4]=1111-0000** respectively.
Default value is unchecked.

3. Low gray dot optimization
Use the up and down selection menu, a total of 4 levels. Levels 1-4 correspond to registers **cfg1[7:6]=00-11**
Default value is level 2. It is recommended to default to level 2.

4. LED open cross elimination
1. Turn off GCLK.
2. Write reg1[15]=1, reg4[7]=1, and send 5 GCLKs (to clear the original open state).
3. Send VSYNC instruction.
4. Send 16’hffff (all 1) data to all pixels.
5. Change the A signal in the row address letter ABCDE from 0->1, wait for 10 clks, and then change the A signal from 1->0 (to prevent 74LS74 from locking).
6. Send VSYNC command
7. Send 16 GCLKs
8. Wait 400us, send the remaining GCLKs, and change lines
9. Repeat steps 7 to 8, send all the GCLKs of all lines, and complete the first set of data display of all lines
10. Write reg4[7]=0 to complete the open circuit detection
FM6363 turns off the open circuit detection: write reg1[15]=0, reg4[7]=0

5. Current gain
Add a current gain button, and set it in the same way as the external current gain and link it. The current gain corresponds to the register cfg2[9:1],
Igain=DEC cfg2[8:1].
When cfg2[9]=1, Iout=18.5x Igain/(Rext x 256)
255≥Igain≥64 50%-200%
When cfg2[9]=0, Iout=18.5x Igain/(Rext x 1024)
255≥Igain≥64 12.5-50%

## Extended advanced settings

1. Add an advanced settings button in the extended properties, click the button to pop up the advanced settings interface.
2. Place a 'Default Settings' button, click it to restore all register values to their default values. A confirmation menu should be added to prevent misoperation.
3. Place a 'Last Modified' button to remember the last manually modified value, and click to restore.
4. Place 4 groups of register filling boxes, in hexadecimal.
5. The register values on this interface should be synchronized with the extended properties interface.