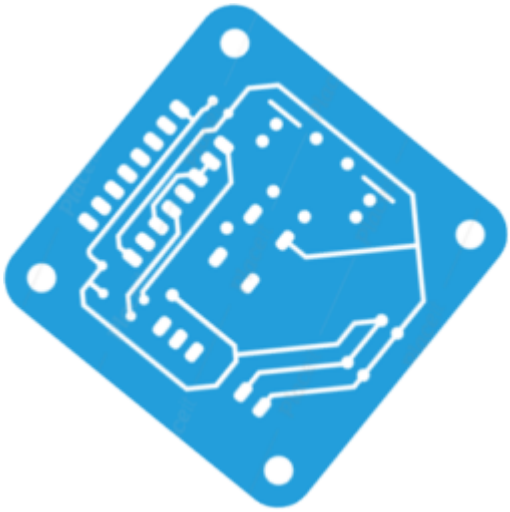
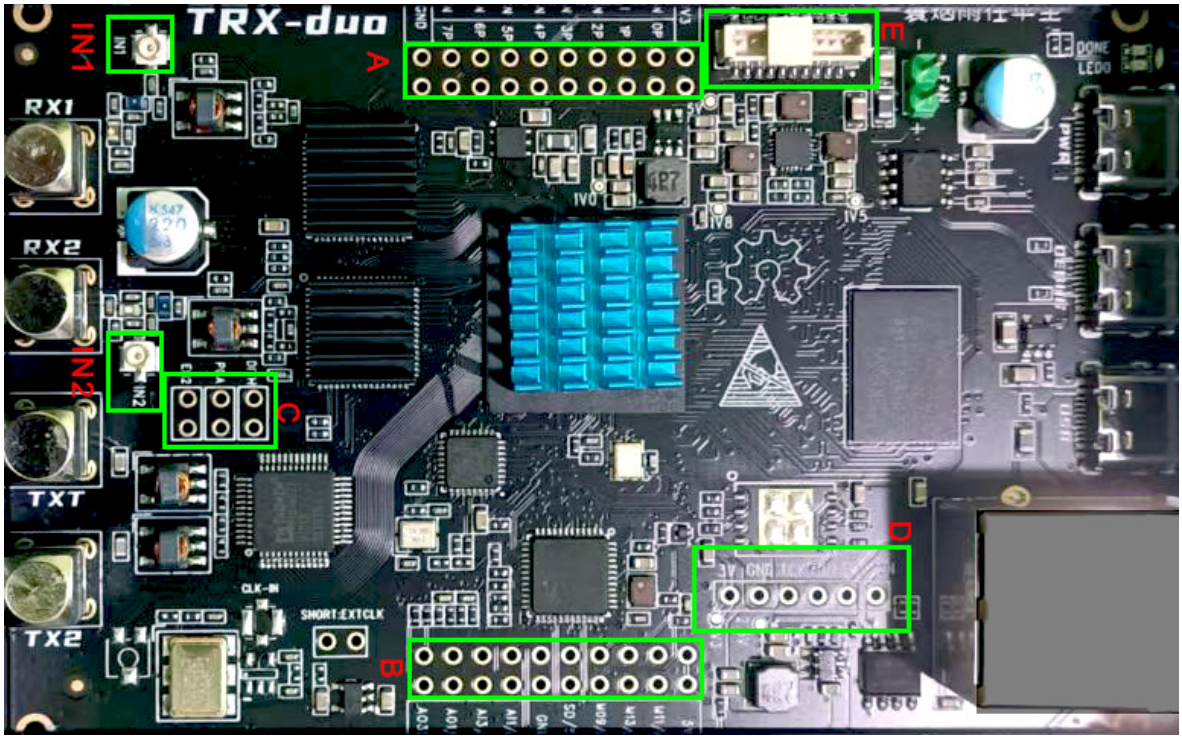


TRX Duo SDR GPIOs and Connectors Guide

Product Guide / By Ampear

There are 5 groups of GPIOs on TRX DUO SDR for external connections, ADC configuration and debugging. Two RF IN ports reserved for bypassing the

input filters on RX1 and RX2. Click to see the product here.



Port A

Pin	Description	FPGA pin number	FPGA pin description	Logic levels
1	3V3			
2	3V3			
3	DIO0_P	G17	IO_L16P_T2_35 (EXT TRIG)	3.3V
4	DIO0_N	G18	IO_L16N_T2_35	3.3V
5	DIO1_P	H16	IO_L13P_T2_MRCC_35	3.3V
6	DIO1_N	H17	IO_L13N_T2_MRCC_35	3.3V
7	DIO2_P	J18	IO_L14P_T2_AD4P_SRCC_35	3.3V
8	DIO2_N	H18	IO_L14N_T2_AD4N_SRCC_35	3.3V

9	DIO3_P	K17	IO_L12P_T1_MRCC_35	3.3V
10	DIO3_N	K18	IO_L12N_T1_MRCC_35	3.3V
11	DIO4_P	L14	IO_L22P_T3_AD7P_35	3.3V
12	DIO4_N	L15	IO_L22N_T3_AD7N_35	3.3V
13	DIO5_P	L16	IO_L11P_T1_SRCC_35	3.3V
14	DIO5_N	L17	IO_L11N_T1_SRCC_35	3.3V
15	DIO6_P	K16	IO_L24P_T3_AD15P_35	3.3V
16	DIO6_N	J16	IO_L24N_T3_AD15N_35	3.3V
17	DIO7_P	M14	IO_L23P_T3_35	3.3V
18	DIO7_N	M15	IO_L23N_T3_35	3.3V
19	GND			
20	GND			

Port B

Pin	Description	FPGA pin number	FPGA pin description	Logic level
1	5V			
2	5V			
3	SPI(MOSI)	E9	PS_MIO10_500	3.3V
4	SPI(MISO)	C6	PS_MIO11_500	3.3V
5	SPI(SCK)	D9	PS_MIO12_500	3.3V
6	SPI(CS#)	E8	PS_MIO13_500	3.3V
7	UART(TX)	C8	PS_MIO08	3.3V

8	UART(RX)	C5	PS_MIO09	3.3V
9	I2C(SCL)	B9	PS_MIO50_501	3.3V
10	I2C(SDA)	B13	PS_MIO51_501	3.3V
11	GND			GND
12	GND			
13	Analog Input 0			0-3.3V
14	Analog Input 1			0-3.3V
15	Analog Input 2			0-3.3V
16	Analog Input 3			0-3.3V
17	Analog Output 0			0-1.8V
18	Analog Output 1			0-1.8V
19	Analog Output 2			0-1.8V
20	Analog Output 3			0-1.8V

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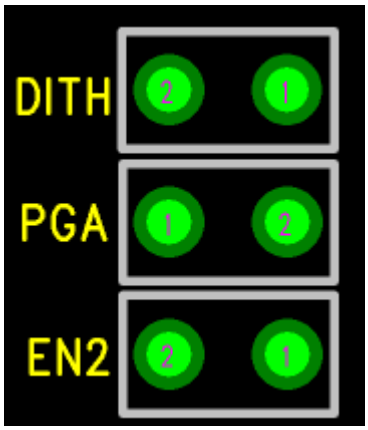
Port C

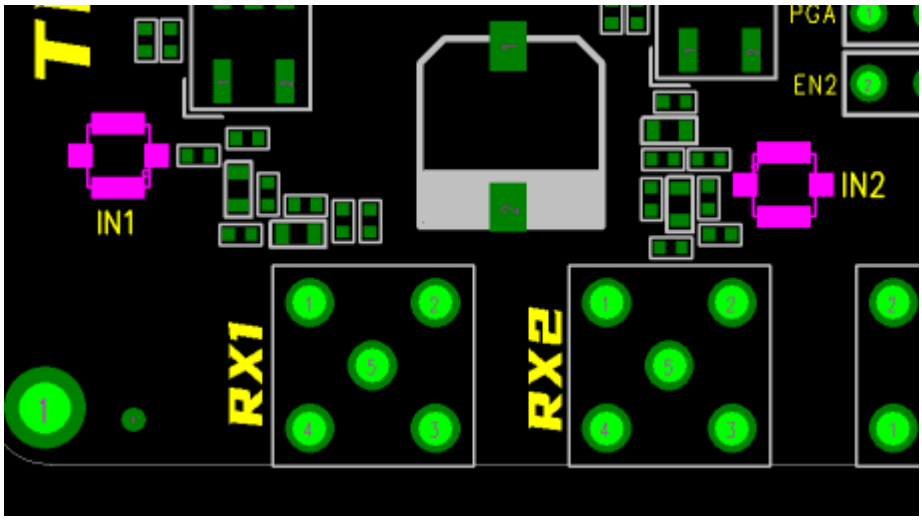
Name	Description	Note
DITH	**short to enable Internal Dither**	Internal Dither The LTC2208 is a 16-bit ADC with a very linear transfer function; however, at low input levels even slight imperfec◁tions in the transfer function will result in unwanted tones. Small errors in the transfer function are usually a result of ADC element mismatches. An optional internal dither mode can be enabled to randomize the input location on the ADC transfer curve, resulting in improved SFDR for low signal levels.
PGA	**short to set PGA =0**	The PGA pin selects between two gain settings for the ADC front-end. PGA = 0 selects an input range of 2.25VP-P;

		PGA = 1 selects an input range of 1.5VP-P. The 2.25V input range has the best SNR; however, the distortion will be higher for input frequencies above 100MHz. For applications with high input frequencies, the low input range will have improved distortion; however, the SNR will be 1.8dB worse
EN2	**short to disable ADC2**	Can reduce 1.2W power consumption and reduce heat generation



Port IN1 & IN2

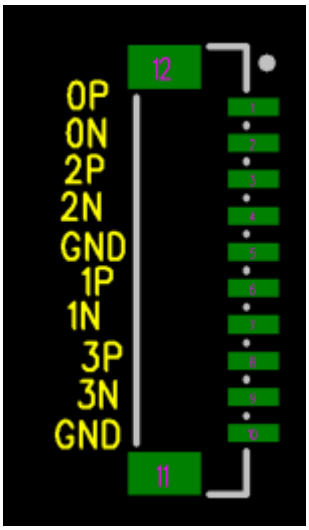
RF IN1 and RF IN2 will bypass the input Lowpass filter on RX1 and RX2 path, this could be used for under-sampling.



Port E

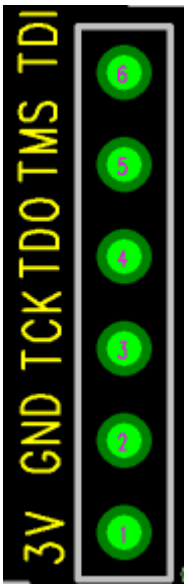
PIN Name	Description
0P	IO_L2P_T0_34
0N	IO_L2N_T0_34
1P	IO_L11P_T1_SRCC_36
1N	IO_L11N_T1_SRCC_36
2P	IO_L6P_T0_34

2N	IO_L6N_T0_34
3P	IO_L13P_T2_MRCC_34
3N	IO_L13N_T2_MRCC_34



Port D

This is the JTAG connector, used for debugging.



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