**BL40A1601** **9/16/2015**

**Embedded System Design**

**Exercise 2:** Clock signals and blinking leds

1. Review the previous exercise and make sure you understand how it works.
   - See the previous week example from Noppa
   - Hierarchy layers, creation of new components, UCF?

2. Coding exercise
   - Start a new project. We'll use and expand this project in next three exercises.
   - Create a top layer (a new VHDL module titled **top**).
     - Include at least mclk, rst, led(7 downto 0), btn(3 downto 0), sw(7 downto 0) in entity.
     - Add the provided UCF file in project, comment/uncomment the required parts.
   - Make a new VHDL module. Title it as **TimeManager**
     - Pass there master clock (mclk) and low active reset (rst) as input
     - Set led signal (led) as output
   - Implement the following **processes** in **TimeManager** module
     - Clock divider that divides mclk (50 MHz) to 100 kHz clock signal
     - Make a led flash on 1 Hz frequency (1 flashes/s) that uses the generated 100 kHz clock signal.
   - Route the flash led into led(0) in the top layer and set all other leds to follow the position of the switches.
   - If you have time, move the led blinker process to a new VHDL module, make two instances of it in the top module, modify the signals and port maps a bit and blink two different leds!