1. Seek infromation

- Seek information about pulse width modulation.
  - Wikipedia : http://en.wikipedia.org/wiki/Pulse-width_modulation

2. VHDL coding excercise

- Create Dimmer.vhd component on the existing project
- Use mclk, rst, and switches (7 downto 0) as input and led as output.
- Insert type definition for.Design DIMM_LED state machine as follows:
  - The state machine consists of two functional states UPDATE and PWM (and RESET)
  - In UPDATE state, update duty cycle reference. Duty cycle reference can be selected with switches SW0 – SW7.
    - => 8 bits => Maximum duty cycle = 255
  - In PWM state, create a pulse width modulation according to the duty cycle reference. The PWM pulse is set to led (output).
    - Hint: compare up counting value (0 to 255) to the reference value (duty).

NOTE!

This exercise will be assessed and will stand for 25% of your final grade. It is **mandatory** to return maximum **one page** report of the implementation of this exercise. The report should show how the pulse width modulator has been designed and implemented. The PWM operation must be presented by simulating the component (not the top level operation). The answer must be sent via e-mail to juhamatti.kohonen@lut.fi by 4.12.2015.