

EMBEDDED SYSTEM DEIGNS ASSIGNMENT

FARID ALIJANI (0422513)

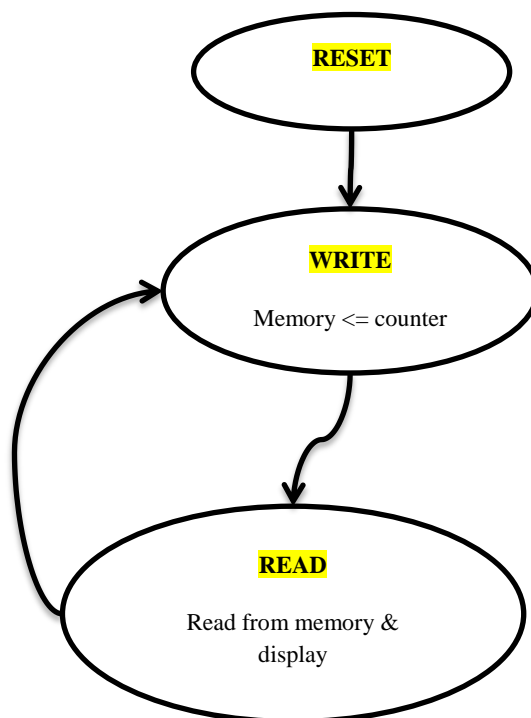
The idea of the assignment is to design a circular buffer which stores eight counter values with a range of 0 to 9999 with 16 bits data width.

Master clock, four buttons including up counter, down counter, reset and write and dip switch for changing reading and writing state are among inputs, while LED and seven - seven segments display are considered as the main design's outputs.

The input buttons are designed such that each press stores only a value into the buffer. It has been implemented by designing the slow clock cycle, one second for the buffer, for instance. One second clock cycle is also used for the counter process in the design. There is another clock pre-scaler process used for refreshing the seven-segment display in the FPGA board though. This process scales down the clock into 500 Hz.

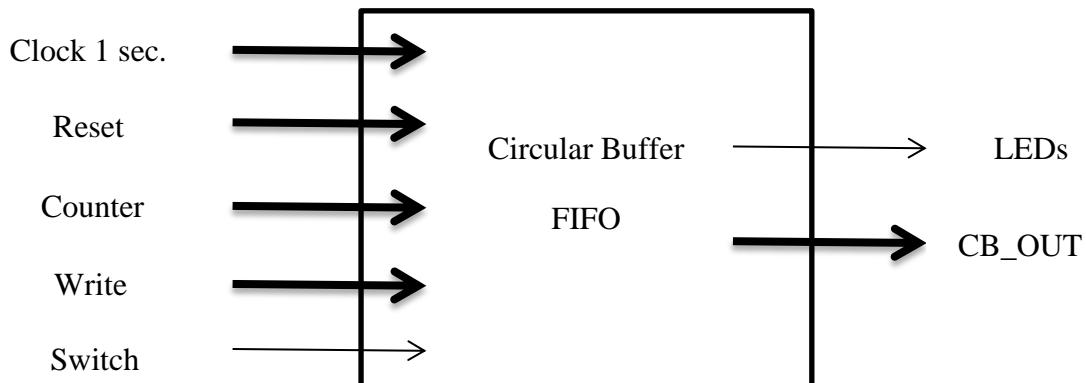
Converting the binary numbers to binary coded decimal is implemented in the process called double dabble. Technically, it is an algorithm which stores the original number to be converted in the register that is n bits wide. The sensitivity lists for this process include master clock, reset and the output of the circular buffer. It outputs vector signal called *data out* with 16 bits width and divided into four separate segments. These segments are used in the display refresh process to update the values on the display.

The circular buffer consists of writing and reading operations which are storing data into the memory and representing them to user, respectively. The idea is implemented with state machine concept as represented below.

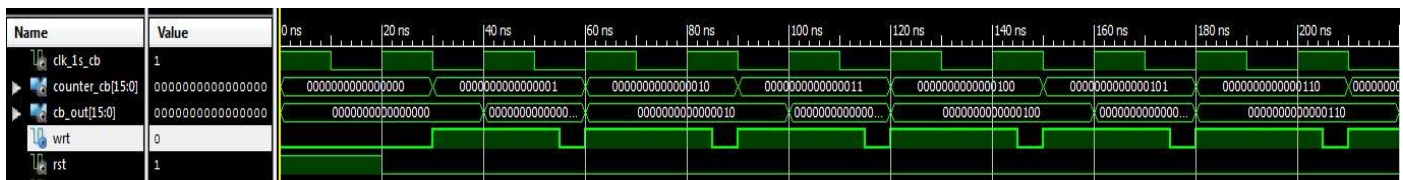


In the writing operation, each value can be written to the memory when user pushes the write button. The values are in the range of 0 – 9999 which are chosen by up and down counter buttons. The reading state is dealing with depicting written values from the memory. After the buffer gets full with written values in memory, the LED would be an indicator for showing full buffer.

The results of simulation have been depicted for the circular buffer. Test bench has been made for this section of the whole project with all its inputs and outputs components.



The following figure shows 8 counter inputs when write button has pressed. The output (CB_OUT) shows the memory output with its saved values accordingly.



The buffer is implemented as a first in first out (FIFO) method for organizing and manipulating data in which the oldest (first) entry is proceed first and would be overwritten if more than eight values are stored. Therefore, the buffer can overflow. The overwritten data are depicted in the figure below though in which old values (first entries) are replaced or overwritten by new counter inputs.

The last value (counter <= "0000000000001000") is overwritten by (counter <= "0000000000001001")

