Lifeng Li（李立丰）

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Basic Info

- Name : **Lifeng Li**
- Gender : **Male**
- Birthday : **Oct. 30th, 1984**
- Birthplace : **Jiangsu, China**

Education

Sep.2007 - Jun.2010	Southeast University	Micro and Solid Electronic	**Master**
Sep.2003 - Jun.2007	Southeast University	Electronic Science and Technology	**Bachelor**

Work Experience

2012.04 - Now Marvell Senior Physical Design Engineer

- 8 Blocks in different Chips (40nm, 28nm & 16nm Tapeout, 2 for Production)
- 3 Chips (40nm & 28nm Tapeout for Production)
- 2 IPs (Test Chip)

2010.04 - 2012.03 Marvell Physical Design Engineer

- 16 IPs (40nm)
- 3 Blocks in different Chips (40nm Tapeout)

Specialized Skill

1. Expert knowledge of Physical Design Tools, IC Compiler (I & II) / Encounter (Innovus) / Olympus (Nitro);
2. Strong working knowledge of Synthesis Tools, Design Compiler / RTL Compiler;
3. Expert knowledge of timing closure tools, Prime Time / IC Scape;
4. Proficiency in CPF/UPF driven Low-Power implementation, STA;
5. Strong Physical Design experience in PERL/TCL/SHELL/VIM scripting;
6. Good working experience in DFT Scan Insertion, ATPG flow;
7. Familiarities with Development of design methodology, flow automation / improvements;
8. Master open tools or libraries, SDC parser, Liberty parser, DEF/LEF parser;
9. Familiarities with TK GUI programing with Tcl-based EDA tool;
10. Ability to handle ImageMagick API;

Communication and English Skill

1. English skill with CET 6 Pass ;
2. Cooperate with global team in US company and experience of travelling to US for project support;
3. Good communication with FE team for FP, CTS, STA and etc.
4. Work closely with Power Analyze Team and Physical Verification Team for physical sign off.
5. Be Good at document writing, using Perl to deal with excel and Latex to deal with PDF;
6. Some knowledge about HTML and javascript for report ;

■ Digital/Analog Mix Design Physical Implementation

IC Compiler / Milkyway / Design Compiler / Calibre / PrimeTime 40nm, 28nm, 16nm

Responsibility and Achievement

Take the task of physical design for the digital part in high-speed analog design. The target customer is high-speed interface SOC.

The floorplan and placement is not difficult, as there is no any hard macro in the design and the height of die is fixed. The main challenge is CTS. Clock has special requirement according to the analog design pattern.

We also do a lot of timing ECO, as design always change and clock spec also change sometimes.

Start from that time, I suggested to setup a clock SPEC document for physical design and I also help on the document. I also developed a set of scripts for custom clock tree physical implementation and check.

■ CPU Sub System Physical Implementation

Encounter / IC Compiler / Milkyway / Design Compiler / Calibre / PrimeTime 40nm, 28nm

Responsibility and Achievement

Work with Front-end team from DCG, through Floorplan, Place, CTS, Routing and Timing Closure, to Tape-out.

The target speed for CPU is 1G more in typical corner. Moreover, we achieve almost 200M more. Useful skew helps a lot. Write a flow to automatic find the local useful skew and apply it at placement stage.

First time, we push power switch to block design in the project and I help to build the top-level power networks.

■ Communication Processor Physical Implementation

Encounter / IC Compiler / Milkyway / Design Compiler / Calibre / PrimeTime 40nm, 28nm

Responsibility and Achievement

We have different modems, from 2G, 3G to 4G. I have done physical implementation for the blocks of GB, TD, LTE and the combination block of different modems.

For the stable block design, floorplan is my main subject. In addition, for the combination block, all become the challenge. As this is a totally new design, and power domain definition is not good at the very begging, I and front-end team together re-define the power domain in order to achieve the physical design closure.

This is also a hierarchical design, we together solve a lot of floorplan issue using hole, island, in-die-pad methodology. Timing is always our target.

■ Top Level Experience

IC Compiler / PrimeTime — 28nm (TSMC & UMC)

Responsibility and Achievement

First top-level experience is a test chip for analog team. It is Pad-limited and IP-limited. The most valuable thing is that I learn a lot top-level tasks, like pad work, custom routing task, partition jobs and etc.

Then I do a mobile SOC chip, I tried this design to placement stage. At last, project assigned me to do the whole PG mesh for the complex and multiple top power domains, custom routing and power switch connection. Take care of special cells, TCD, ESD, DECAP, ENDCAP and BOUNDARY. I also do the most DRC/LVS work for this chip. I learned a lot of detail information from this task.

For mobile series chip, I build a top level PG flow, and make a lot of work automatic.

■ 16nm Design Experience

Innovus / IC Compiler (I & II) / PrimeTime / Tempus / Calibre — 16nm (TSMC)

Responsibility and Achievement

When the 16nm first introduced to our team, I am one of flow develop person in the team, and I am testing 16nm in ICC/EDI using Communication Processor design. I contributed a lot of library issues, tech file issues and helped to build PNR & starRC flow.

Then I take part in one tape-out design, and do a small block for top. And I helped to do 16nm top STA and timing closure task.

I am now validating IC Compiler II using 16nm technology and GPU design with 4 million instances. I am also running DCG and verify the SDC constraint.

■ Hybrid P&R flow Development

Encounter / IC Compiler / Olympus

Responsibility and Achievement

Each P&R tool has its advantages and disadvantages. In order to make full use of each tool, I lead a hybrid flow project. DEF format is designed as a design exchange format, but in real project, there are lots of issues need to be resolved. I define the SPEC and architecture.

My team and I use many open tools and solve the flow problems. Like SDC parser, Liberty parser, DEF/LEF API etc.

Our commonly usage is floorplan in ICC, Placement in Encounter or Olympus, then CTS in Encounter. At last, Route and Timing ECO are back into ICC.

■ P&R Audit and Checklist System

Encounter / IC Compiler / Olympus

Responsibility and Achievement

Lead and develop the methodology of design setting and quality check flow. Develop the methodology of Useful Skew. In-design problem solving and scripting.

Write the whole flow, which can use both for Encounter and for IC Compiler. Write some check items for Encounter and IC Compiler.

■ Synthesis and STA

Prime Time / Tempus / Design Compiler / RTL Compiler **65nm, 40nm, 28nm, 16nm**

Responsibility and Achievement

Do the Synthesis for ARM7, GPU and SOC top using SMIC-65nm technology. Do DCG job for GPU using 16nm technology.

Sign-off the blocks which I did the Synthesis.

■ DFT Checklist Platform and Practise

TeraMax / TestKompress / Tcl / Perl / Python / Git

Responsibility and Achievement

Build the platform for DFT review. Discuss the check items for scan, mbist and jtag. Review the DFT designs.

I also write some checks for the system.

■ ATPG for GPU block and ATPG flow enhancement

TestKompress / Tcl

Responsibility and Achievement

Work on ATPG for block design and enhance the central ATPG flow.