Lifeng Li（李立丰）

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Basic Info

- Name : **Lifeng Li**
- Gender : **Male**
- Birthday : **Oct. 30th, 1984**
- Birthplace : **Jiangsu, China**

Education

Sep.2007 - Jun.2010	Southeast University	Micro and Solid Electronic	**Master**
Sep.2003 - Jun.2007	Southeast University	Electronic Science and Technology	**Bachelor**

Work Experience

2012.04 - Now Marvell Senior Physical Design Engineer

- 6 Blocks in different Chips (40nm, 28nm & 16nm Tapeout, 2 for Production)
- 3 Chips (40nm & 28nm Tapeout for Production)
- 2 IPs (Test Chip)

2010.04 - 2012.03 Marvell Physical Design Engineer

- 16 IPs (40nm)
- 3 Blocks in different Chips (40nm Tapeout)

Specialized Skill

1. Expert knowledge of Physical Design Tool, IC Compiler / Encounter ;
2. Strong working knowledge of Synthesis Tools, Design Compiler / RTL Compiler ;
3. Expert knowledge of timing closure tools, Prime Time / IC Scape ;
4. Proficiency in CPF/UPF driven Low-Power implementation, STA ;
5. Strong Physical Design experience in PERL/TCL/SHELL/VIM scripting ;
6. Familiarities with Development of design methodology, flow automation / improvements.
7. Master open tools or libraries, SDC parser, Liberty parser, DEF/LEF parser.
8. Ability to handle ImageMagick API.

Communication and English Skill

1. English skill with CET 6 Pass ;
2. Cooperate with global team in US company and experience of travelling to US for project support;
3. Good communication with FE team for FP, CTS, STA and etc.
4. Work closely with Power Analyze Team and Physical Verification Team for physical sign off.
5. Be Good at document writing, using Perl to deal with excel and Latex to deal with PDF;
6. Some knowledge about HTML and javascript for report ;

Project Experience (1 / 3)

■ SYN & STA - Synthesis and STA **Sep. 2008 - Sep. 2009**

Tool: Design Compiler / Prime Time

Description: Synthesis for SMIC-65nm SOC chip which includes ARM7, GPS, Data Interface and etc. Do STA for Sign off.

Responsibility: Chip level and ARM7 Synthesis; Chip level and ARM7 STA and timing closure.

■ PNR - Digital Part of Analog block Physical Implement **Apr. 2010 - Mar. 2011**

Tool: IC Compiler / Milkyway / Design Compiler / Calibre / PrimeTime

Description: Take the block design of digital part in Analog PHYs. Be responsible for all aspects of design physical implementation, including Floorplan, Placement, CTS, Routing and working closely with the analog team designer for special requirement of design. Finish 16 digital parts of analog IPs. Work close to the frontend of analog team about timing.

Responsibility: Block level P&R implement, Both Physical and Logic tasks.

■ PNR - Test Chip Physical Implement of Analog IPs **Aug. 2010 - Nov. 2010**

Tool: IC Compiler / Milkyway / Design Compiler / Calibre / PrimeTime

Description: Do 4onm test chip physical implement for multiple analog IPs. Custom routing and special custom routing requirement is the challenge of this design. CTS is not complex but has a few custom task. Timing is also has some special requirement. Build my strength and experience about design related to analog.

Responsibility: Chip level P&R implement, Both Physical and Logic tasks.

■ PNR - Application Processor Physical Implement **Mar. 2011 - Jul. 2012**

Tool: Encounter / IC Compiler / Milkyway / Design Compiler / Calibre / PrimeTime

Description: Take the block design of Application Processor in Mobile SOC Chip. Some are Low-Power designs and do evaluate power/performance/area trade-offs. Be responsible for all aspects of design implementation, including Floorplan, Placement, CTS, Routing and working closely with the Front-End design team for timing closure. Also working closely with Power Analyze team to fix power weakness and with PV team to fix DRC/LVS issues. Some for TSMC-40nm and some for UMC-40nm.

Responsibility: Block level P&R implement from netlist to GDS, Both Physical and Logic tasks.

■ PNR - Chip level Physical Implementation **Jul.2012 - Apr. 2013**

Tool: IC Compiler / Encounter / Calibre / PrimeTime

Description: Do the Power/Ground mesh for the whole chip, custom routing and pad/power switch connection. Take care of Special cell, such as TCD, DECAP, ESD, EndCap and Boundary cell. At the Tapeout stage, debug and fix the DRC/LVS issues. One for UMC-40nm and one for TSMC-28nm.

Responsibility: Top level Power mesh and Physical related tasks. Work with PV team to fix DRC/LVS for signoff.

Project Experience (2 / 3)

■ CAD & PNR - P&R Audit and Checklist System — Mar.2013 - Apr.2014

Tool: Perl / Tcl / Encounter / IC Compiler / HTML / ImageMagick

Description: Lead and develop the methodology of design setting and quality check flow. Develop the methodology of Useful Skew. In-design problem solving and scripting.

Responsibility: Write the whole flow which can use both for Encounter and IC Compiler. Write some check items for Encounter and IC Compiler.

■ PNR - Block of 16nm technology memory test chip — Jun.2013 - Nov.2013

Tool: Encounter / IC Compiler / Calibre / Milkyway / StarRC / PrimeTime

Description: Build the flow for latest technology node and verify the issues. Work with library team to clear the DRC issues. Finish the whole netlist to gds flow for block design and verify its power, congestion, timing and etc.

Responsibility: Finish the PNR work for latest technology node and verify the flow and library quality.

■ PNR - Communication Processor Physical Implementation — Dec.2013 - Apr.2014

Tool: Encounter / IC Compiler / Calibre / Milkyway / StarRC / PrimeTime / IC Escape

Description: New design for communicate processor, work with Frontend team to study and implement the physical design, including floorplan, CTS and timing closure. Use both ICC and EDI to finish the work, EDI for place and CTS and ICC for routing, ECO and timing closure.
Responsibility: Finish the PNR work, do timing closure and clean the DRC/LVS issue in PNR tool.

■ CAD & PNR - Hybrid P&R Flow Development — Jun.2014 - Current

Tool: Encounter / IC Compiler / Olympus / C / C++ / Tcl / Perl

Description: Each P&R tool has its advantages and disadvantages. In order to make full use of each tool, I lead a hybrid flow project. I define the SPEC, and architecture. I and my team use a lot of open tool and solve the flow problems. Like SDC parser, Liberty parser, Def/Lef api and etc.
Responsibility: Define the flow spec and architecture, master the different P&R tool usage and behaviors and code review.

■ CAD - IC Script Development Platform — Dec.2014 - Mar.2015

Tool: Encounter / IC Compiler / VimL / Tcl / Python / Perl / Makefile / Git

Description: In order to write script efficiently. Built a platform to develop scripts for physical design projects. Finish most functions using one command. Coding, documenting and testing work well with different EDA tools.
Responsibility: Develop the whole platform, test with colleagues and maintain the platform.

Project Experience (3 / 3)

■ PNR & CAD - Top level PG mesh for multi-domains **Dec.2014 - Apr. 2015**

Tool: IC Compiler / Calibre / Milkyway / StarRC / PrimeTime / IC Escape

Description: Do PG work and make automatic flow for multiple power domain top design in ICC. The flow is mostly used for mobile chip design.
Responsibility: Finish the physical work; contribute to the central PG flow.

■ CAD & DFT - DFT Checklist Platform and Practice **Dec.2014 - Current**

Tool: TeraMax / TestKompress / Tcl / Perl / Python / Git

Description: Build the platform for DFT review. Discuss the check items for scan, mbist and jtag. Review the DFT designs.
Responsibility: Build the check flow, write the check scripts and review the DFT quality.

■ PNR - Block of 16nm technology SOC test chip **Jun.2015 - Current**

Tool: Encounter / IC Compiler / Calibre / Milkyway / StarRC / PrimeTime

Description: Work on cpu wrapper module. Test the placement, CTS and routing function of EDI and ICC.

Responsibility: Finish the PNR work for latest technology node.

C.V. of Lifeng Li