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Broadband High Power Amplifier Design Using GaN HEMT Technology

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***Abstract*—This paper presents the design and measurements of a broadband GaN HEMT power amplifier intended for point-to-point radios, electronic warfare systems, and test and measurement applications. The proposed power amplifier is fabricated, and small/large-signal measurements are collected. Fabricated design is conducted for an input power of 26 dBm and obtained between 39.6 - 40.9 dBm output power. Power added efficiency (PAE) of 45.9 % to 61.4 % is reached over the band (0.5 - 2.5 GHz). In this study, Wolfspeed's CGH40010F transistor is used in CW mode. In order to decide optimum source and load impedances of the transistor, load- & source-pull simulations are conducted. After load- & source-pull simulations, proper source and load matching networks are established to obtain optimum output power and efficiency values over the band.**

Keywords—power amplifier (PA), power added efficiency (PAE), high efficiency, wideband, GaN HEMT.

I. Introduction

A Power amplifier (PA) is one of the most important devices for radar, guidance, radio communication, and electronic warfare systems [1]. It is the most dominant component determining overall power consumption and, therefore, the heat dissipation of these systems. Further, PA output power and linearity are critical in establishing reliable communications in modern radios [2], [3], [4], [5]. In order to reduce power consumption and self-heating and improve reliability of modern RF transmitters, power amplifiers operating over wide bandwidths with high efficiency are needed [6].

In this paper, a high power, high efficiency, broadband power amplifier using GaN HEMT technology and operating from 0.5 to 2.5 GHz is presented. The design employs Wolfspeed's CGH40010F transistor in continuous-wave (CW) mode. The proposed amplifier is fabricated, and small- large-signal measurements are collected.

The literature research is conducted, and some state-of-the-art power amplifier studies are investigated. In addition to this, the studies using the same transistor as the proposed design examined [1], [2], [5], [9], [11]. The proposed system offers a new design to the literature with its high fractional bandwidth, good gain, and PAE values.

The remainder of this paper is organized as follows. In Section II, the design approach for the proposed design is described. In Section III, measured performance is compared with simulation results. Finally, concluding remarks are given in Section IV.

II. Design Approach

This section describes the design process of the proposed power amplifier. This work is conducted to design high power, high efficiency wideband power amplifier from 0.5 to 2.5 GHz. To be able to meet sufficient power and PAE, class AB design is decided. Class AB design offers higher efficiency than class A mode, but it causes some increased nonlinear effects, which can be tolerated or neglected in some applications [7]. In this study, simulations are carried out in Cadence AWR Design Environment.

A. Transistor Choice & Bias Point Selection

The first step in power amplifier design is to select a proper transistor that can meet application requirements. In this work, the primary goal is to achieve higher than 50 % PAE and 10 W output power from 0.5 to 2.5 GHz. As such, it is necessary to use a transistor that can operate over this frequency range with acceptable gain and PAE. In this study, Wolfspeed's CGH40010F GaN HEMT device is selected [8]. Once the transistor is selected, a suitable DC bias point must be determined to meet the specifications on gain, PAE, output and harmonic suppression. For CGH40010F, the bias point is selected as V_{DS} = 28 V, V_{GS} = -2.1 V, I_{DQ} = 336 mA for class AB operation. A DC bias network, consisting of RF chokes and DC blocks, is then designed to operate the transistor at the selected bias point while minimizing noise from power lines.

B. Load- & Source-pull Analyses & Matching Network Design

Load-pull/source-pull is a design technique wherein source, and load impedances presented to a transistor are varied to find their optimum value to achieve desired performance from the device [7], [9]. In this paper, load- & source-pull simulations are carried out using the large-signal model of the CGH40010F transistor in Cadence AWR Design Environment. Load- & source-pull analyses are executed in an iterative fashion. First, the analyses are performed to obtain Γ_L (reflection coefficient seen looking into load) and Γ_S (reflection coefficient seen looking into source), respectively, using power vs. efficiency contours on the Smith chart. Then, the process is repeated

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using thus obtained reflection coefficients until desired output power and PAE are simultaneously achieved in simulations. Fig. 1 and Fig. 2 represent the load- & source-pull contours for 2500 MHz, respectively. As seen in Fig. 1, the output power of 41 dBm and PAE of 65 % contours are highest grade contours; thus, it is aimed to use impedance points located at the intersection of these contours for output matching network design. The output power of 42 dBm and PAE of 65 % contours are the highest grade contours in Fig. 2. Similarly, it is aimed to use impedance points located at the intersection of these contours for input matching network design.

Load- & source-pull contours are plotted to determine Γ_L and Γ_S points that meet design criteria for both output power and PAE. After that, Γ_L and Γ_S from the load- and source-pull analyses need to be realized with suitably designed input and output matching networks. Taking advantage of the network synthesis tool in Cadence AWR Design Environment, microstrip-based matching networks are designed with DC blocking capacitors on gate and drain lines. AWR Design Environment's network synthesis tool allows a designer to select things such as network topology, dielectric substrate properties, design goals (requested output power and PAE). After obtaining input and output matching networks, the schematic of the proposed power amplifier is composed as given in Fig. 3.

The theory behind impedance matching circuit design is based on the transmission line impedance equation given following equation.

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l} \quad (1)$$

- Z_{in} : Transmission line input impedance
- Z_L : Load impedance
- Z_0 : Characteristic impedance
- βl : Electrical length

C. Stability

To design unconditionally stable power amplifier Rollet's stability formula must be satisfied over the entire frequency range [10].

A stabilization resistor is employed, which ensures stable operation, especially at low frequencies. In this study, stability factor K is greater than 1 over the entire frequency band in the simulation. Stability simulation is performed in Cadence AWR Design Environment with different values of resistors. In this design, 75 Ω resistor is used for stability. Actually, a smaller value resistor than 75 Ω is preferred but to meet Rollet's stability condition, 75 Ω is used in this work.

Effect of 75 Ω stability resistor on impedance, output power, and PAE is analyzed and seen that there is no impact on

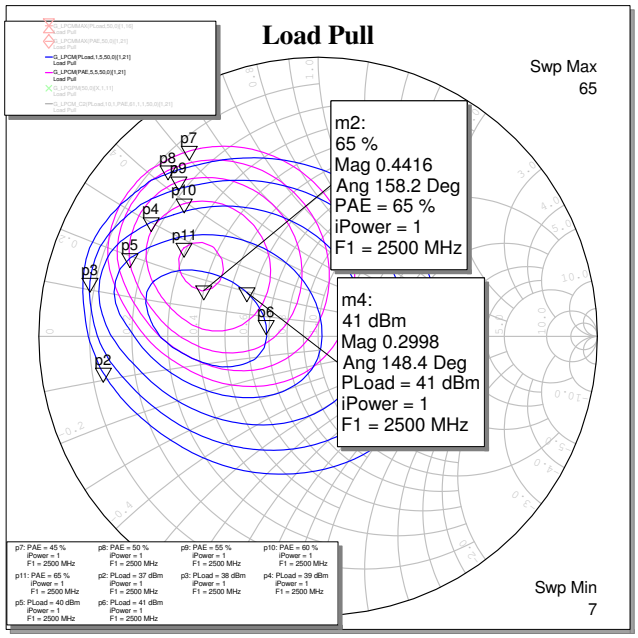

Fig. 1. Load-pull contours.

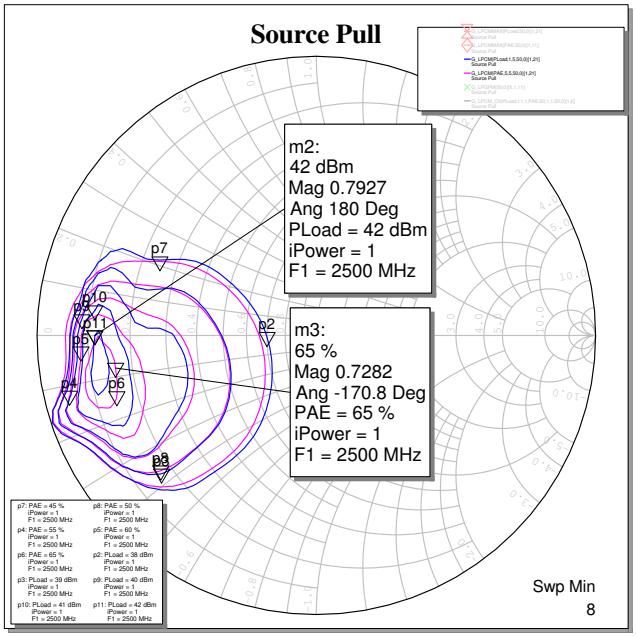

Fig. 2. Source-pull contours.

impedance up to 1.8 GHz. After this point, impedance begins to change on the smith chart slightly. However, change in impedance does not affect output power and PAE up to 2.4 GHz. Beyond 2.4 GHz, it occurs slight gain and efficiency degradation.

III. Implementation and Measurement Results

The design is fabricated on 0.508 mm thick Rogers RO4350B substrate with ϵ_r = 3.66 and is shown in Fig. 4 [12]. The dimension of the realized design is 120 mm x 40

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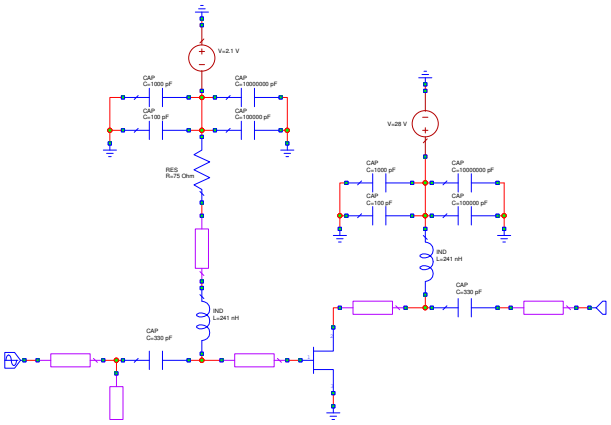

Fig. 3. Input and output matching network.

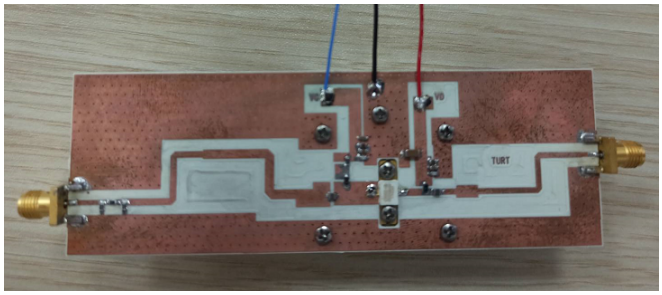

Fig. 4. Implemented proposed power amplifier.

mm. Measurement results and discussions of simulation versus measurements follow.

A. Small-signal Measurements

The small-signal analysis is conducted for the proposed system. Simulated and measured small-signal S_{11}, S_{21} are provided in Fig 5. Simulated S_{11} varies between -4.5 - -6.5 dB, while measurements show better than -4.8 dB input reflection throughout the band. On the other hand, small-signal gain, S_{21}, exhibits more divergence between simulations and measurements. While the measured gain is higher at the low end of the band (0.5 - 1.2 GHz), it is lower than simulations in the upper half by as much as 2 dB.

VSWR analysis is also conducted in Fig. 6 for both simulated and fabricated designs to show small-signal performance from another point of view. As seen from Fig. 6, measurement results are better than the simulation. Simulated VSWR varies between 2.8 and 3.9, while measurement results fluctuate between 2 and 3.7. Both S-parameters and VSWR graphs show that the input matching performance of the proposed amplifier is better at the upper half band.

B. Large-signal Measurements

The large-signal analysis is conducted for the proposed system from 0.5 to 2.5 GHz. In this section, output power, gain, PAE are analyzed for the fabricated and simulated systems under CW input signals. Measurements are conducted for an input power level of 26 dBm with swept frequencies. Fig. 7 presents the measured output power and gain versus simulation, while Fig. 8 illustrates measured PAE versus simulation over the band.

The measured output power is between 39.6 - 40.9 dBm and measured PAE is between 45.9 % - 61.4 % over the band. On the other hand, the simulated output power is between 40.2 - 41.5 dBm, and simulated PAE is between 54.1 % - 63.3 % over the band. For output power, PAE and gain, measured results are better than simulations at most points between 0.5 - 1.3 GHz; however, beyond this point, there is a drop in measured results compared to simulated results. A large-signal gain comparison between simulated and fabricated designs is also given in Fig 7. Large-signal gain of the fabricated system varies between 13.6 - 14.9 dB, while it is between 14.2 - 15.5 dB in simulations.

Levels of the simulated higher harmonic products are provided to reveal large-signal analysis in depth. Fig. 9 shows the levels of the fundamental tone, second and third harmonic

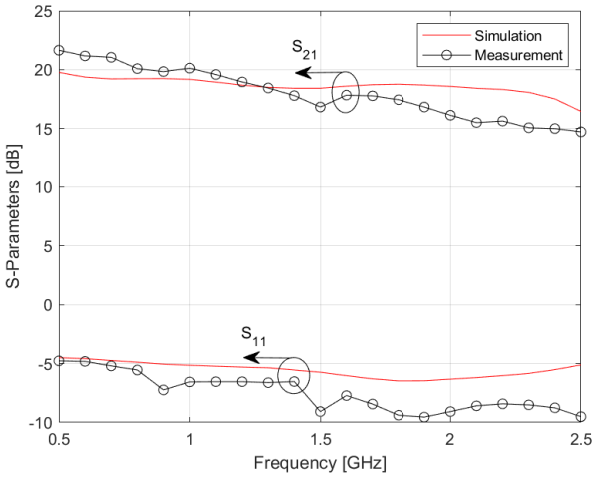

Fig. 5. Measured and simulated small-signal S_{11} and S_{21} graph.

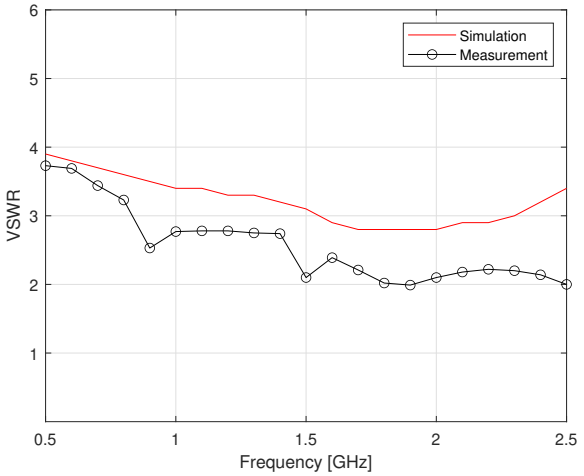

Fig. 6. Measured and simulated VSWR graph.

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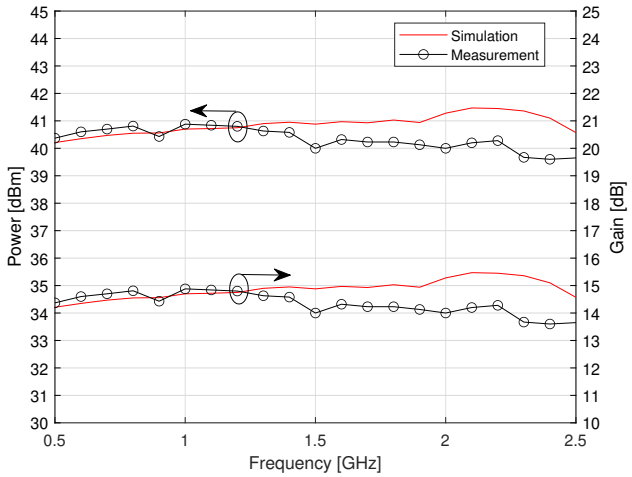

Fig. 7. Measured and simulated power and large-signal gain graph.

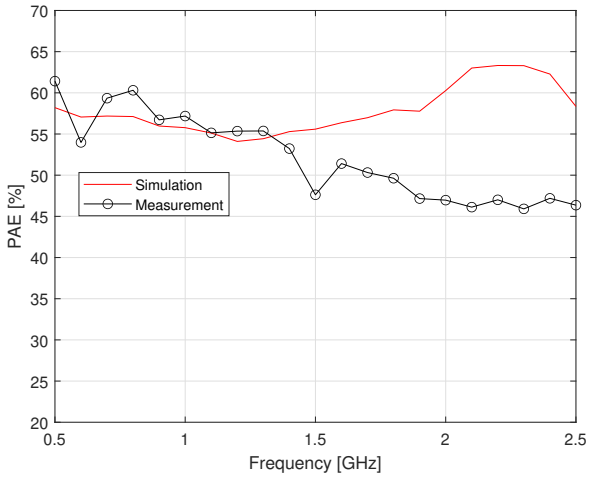

Fig. 8. Measured and simulated PAE graph.

products. The highest second harmonic level is 18.1 dBc at 0.8 GHz, and the highest third harmonic level is 10.9 dBc at 1.9 GHz. Fig. 9 also depicts the simulated OIP3 level for the proposed system. The minimum level of the OIP3 is 50 dBm at 0.9 GHz.

Simulation is performed by taking into account the large-signal model of the transistor with the designed microstrip lines. Because S-parameters of the RF connectors used at the input and output of the RF lines are not available, this part could not be simulated. In addition, fabrication defects on the implemented design lead to some degradation in the output power and PAE, especially at the high end of the band. These factors are thought to be the cause of the difference between simulation and implementation results.

Table I presents a comparison of some recent state-of-the-art designs and proposed work in terms of bandwidth, output power, gain and PAE. This work achieves the widest with good gain, and PAE when compared to literature.

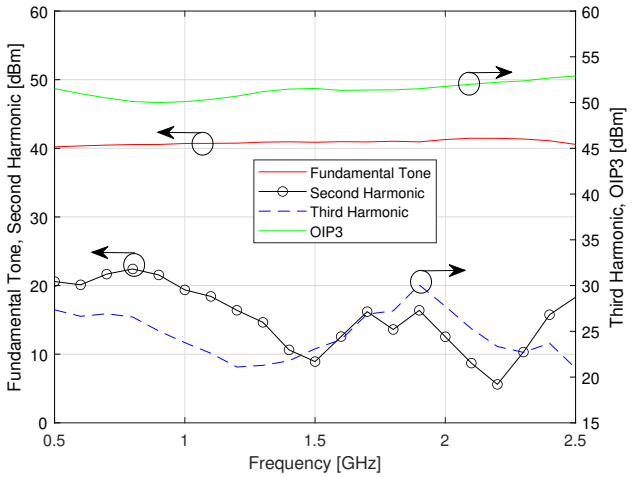

Fig. 9. Simulated fundamental tone, second harmonic, third harmonic and OIP3 graph.

TABLE I
STATE-OF-THE-ART PAS

Reference	BW [GHz]	Fractional BW [%]	Pout [dBm]	Gain [dB]	PAE [%]
[2]	1.9 - 2.9	42	36 - 39.5	11.5 - 15.5	37 - 69
[3]	1.2 - 2.7	77	38.5 - 39.2	10 - 12	17 - 33
[4]	2.0 - 2.8	33	47 - 48.5	28.3 - 29	50 - 65
[6]	1.4 - 1.6	13	45 - 46.1	12 - 13.3	60 - 67.4
[11]	1.0 - 2.5	85	33 - 41	5 - 13	48 - 55
This Work	0.5 - 2.5	133	39.6 - 40.9	13.6 - 14.9	45.9 - 61.4

IV. CONCLUSION

In this paper, a broadband high power amplifier design that uses GaN HEMT technology at 0.5 - 2.5 GHz operating frequency is presented. For the proposed design, Wolfspeed's CGH40010F transistor is used in CW mode. In order to decide the optimum source and load impedances of the transistor, load- & source-pull simulations are conducted. After load- & source-pull simulations, proper source and load matching networks are established to obtain optimum output power and efficiency values over the band. The proposed amplifier is fabricated, and small/large-signal measurements are conducted. Fabricated design is conducted for an input power of 26 dBm and obtained between 39.6 - 40.9 dBm output power. PAE of 45.9 % to 61.4 % is reached over the band (0.5 - 2.5 GHz). For output power, PAE and gain, measured results are better than the simulation between 0.5 - 1.3 GHz; however, beyond this point, there is a drop in measured results compare to simulated results. This drop is thought to be due to fabrication and assembly tolerances and some parameters that could not be simulated, for example RF connector loss. Further measurements and simulations are currently in progress to understand the root cause of this difference.

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