

# MARINNA HEICHBERGER

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(716) 270-7878

**EDUCATION** **Rochester Institute of Technology**, Rochester, NY  
Bachelor of Science in Electrical Engineering, expected May 2026  
Masters of Science in Electrical Engineering, expected December 2026  
**GPA:** 3.55/4.0

## **SKILLS**

**Hardware Description & Simulation:** Verilog, VHDL, Quartus Prime, ModelSim, LTSpice, Simulink  
**Programming and Scripting:** C, C++, MATLAB, Assembly, Python, NumPy, scikit-learn, UART, SPI, I2C  
**Digital Design & Concepts:** FSMs, pipelining, RTL, testbench development, MOSFETS, OP-AMPS, Fourier transforms  
**Hardware:** Oscilloscope, Multimeter, Altera FPGA, Logic Analyzer, Microcontrollers, Network Analyzer, Breadboard

## **PROJECTS/LABS**

### **RISC Design**

- Designed a 3-bus, 8-bit Von Neumann RISC processor from top-down architecture to structural RTL Verilog implementation, including datapath, control unit, ALU, register file, and memory interface.
- Implemented 12+ instructions including arithmetic, logic, shift/rotate, load/store, and stack operations; verified functionality via comprehensive ModelSim testbenches with waveform analysis.
- Optimized instruction sequencing, achieving 129-instruction multiplication in 477 cycles; utilized ~499 logic elements and 159 registers on FPGA synthesis.

### **Embedded Oscilloscope on MSP430**

- Configured TimerA to trigger ADC reads at precise intervals (10 ms/5 ms); optimized register setup to avoid capacitance interference
- Implemented dual-scale data mapping (linear via shifts; logarithmic via LUT-driven MSB detection)
- Output UART at 9600 bps and employed dual lookup tables and software delays for LED multiplexing; used SMCLK dividers and up-mode timing for 0.5 s display refresh to output display

### **Digital Systems 1**

- Designed a Bit Serial Adder Subtractor Finite State Machine that has the ability to perform back to back addition and subtraction operations, with 2, five bit operands; designed with Quartus and tested on Altera FPGA board.

## **EMPLOYMENT EXPERIENCE**

### **Symbotic LLC – Boston, Massachusetts**

**May 2025- August 2025**

#### **Industrial Controls Engineer**

- Designed and implemented modular ladder logic using Studio 5000 to automate conveyor control, based on encoder and photoeye feedback; logic accounted for encoder rollover using modulus operation array indexing, and conditional logic.
- Integrated JSON and CSV configuration files into an Ignition HMI system, demonstrating hands on experience with industrial data flow and software-hardware interfacing

### **Bridgestone Americas - Nashville, Tennessee**

**June 2024 – December 2024**

#### **Electrical Engineering Intern**

- Modified and debugged PLC logic in RSLogix 5 to implement real time fault detection systems for automated tire handling, improving system uptime and protecting product integrity
- Programmed conveyor control using VFD 525 drives and photoeye sensors to enable autonomous tire spacing, detection and movement
- Interpreted electrical schematics to analyze signal flow and ensure accurate sensor-actuator integration
- Applied embedded control principals, structured logic development and sensor-actuator interfacing experience

## **LEADERSHIP/INVOLVEMENT**

### **Rochester Institute of Technology – Rochester, New York**

**August 2023 - Present**

#### **Resident Assistant**

- Served as a live-in mentor and community leader for a residence hall of 20–40 students.
- Resolved conflicts, communicated effectively with diverse groups, and upheld university policies.

#### **Varsity Track and Field**

- Practiced, traveled, and competed at least 20 hours per week in the D3 Liberty League Conference while balancing a full-time academic course load

